# Ballast Design for 54W UV-C Disinfection Lamp (Voltage Mode Preheating) with Controller IC ICB2FL03G & 600V CoolMOS™ PFD7

**ICB2FL03G**

## About this document

### Product Highlights

- Lowest count of external components
- 650 V half-bridge driver with Coreless Transformer Technology
- Supports customer in-circuit test mode for reduced tester time
- Supports multi-lamp designs (in series connection)
- Integrated digital timers up to 40 seconds
- Numerous monitoring and protection features for highest reliability
- Very high accuracy of frequencies and timers over the whole temperature range
- Very low standby losses

### Features PFC

- Discontinuous mode PFC for load ranges 0 to 100 %
- Integrated digital compensation of PFC control loop
- Improved compensation for low THD of AC input current, also in DCM operation
- Adjustable PFC current limitation

### Features Lamp Ballast Inverter

- Adjustable detection of overload and rectifier effect (EOL)
- Detection of capacitive load operation
- Improved ignition control allows for operation close to magnetic saturation of inductors
- Restart with skipped preheating at short interruptions of line voltage (for emergency lighting)
- Parameters adjustable by resistors only
- Pb-free lead plating; RoHS-compliant

In our UV-C ballast design we have deployed 600V CoolMOSTM from the new PFD7 family. The PFD7 family of products combine highest efficiency with a very high level of robustness. In order to reduce system cost we decided to use a version in a low cost SOT223 package. The ballast was designed for 54W T5 lamp, but can be used with L55 W 2G11UV-C lamp.

# Table of contents

**Table of contents**

# 1 Introduction

The fluorescent lamp ballast Controller ICB2FL03G is designed to control a boost converter as an active power factor correction (PFC) filter in critical/discontinuous conduction mode (CritCM/DCM) and in half-bridge topologies as a lamp inverter. The intelligent control concept enables designers to develop cost-effective ballasts for fluorescent lamps (FL) that fulfill the requirements of a high-performance T5 lamp ballast as well as multi-lamp topologies (series connection), T8 and T4 designs. A state machine controlling the operating modes, a completely integrated digital control loop for the PFC output voltage and low tolerances for reference voltages and operating frequency over the whole temperature range are a result of the advanced mixed signal technology with only few components required externally. Combined with a high-voltage level shift driver with Coreless Transformer Technology for the half-bridge inverter, the IC offers a significant number of exceptional features for FL ballasts.

The FL ballast controller ICB2FL03G has improved and extended functionality to enable high-quality single or multi-lamp ballasts (series connection) with a low number of external components. It helps to save system costs and to easily achieve class A2 of the energy efficiency index (EEI) for fluorescent lamp ballasts.

Further information and the data sheet can be found at: ***http://www.infineon.com/smartlighting***

Unless otherwise specified, all values given in this Application Note are typical values.

## 1.1 Functional Description

The functional description is given based on the circuit diagram of a lamp ballast for the T5 fluorescent lamps (***Figure 1***).

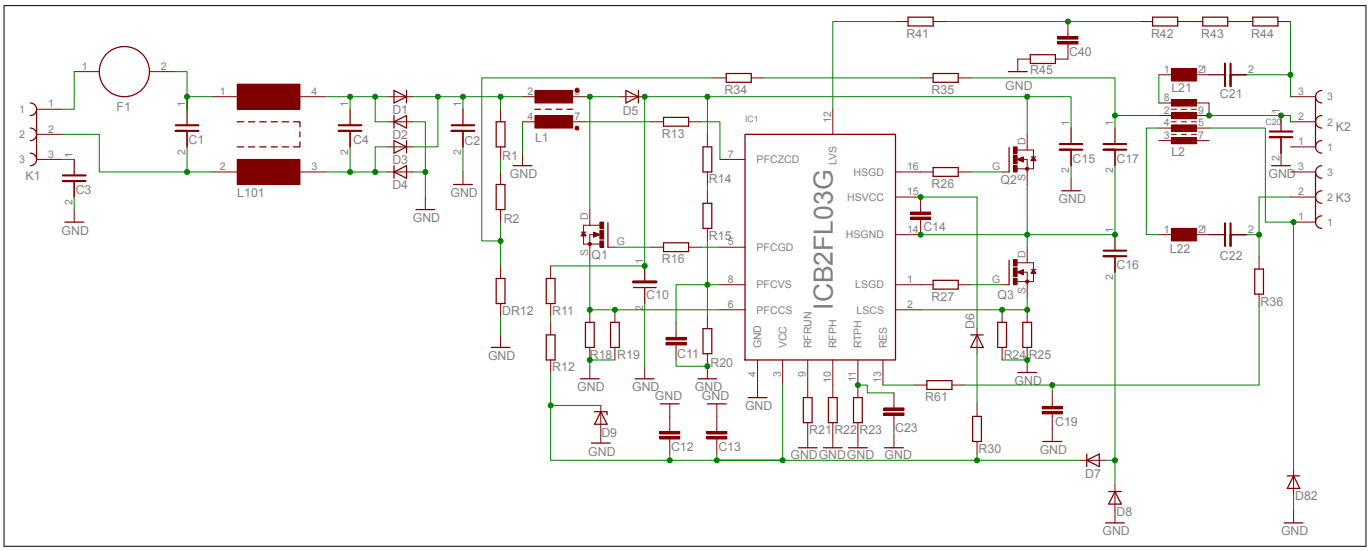



**Figure 1 Schematic for 54W T5 demo board**

The schematic shows the circuit of the demo board with the reference name of each component for a single lamp design with voltage mode preheating. This schematic supports all protection functions of the IC.

After switching on the mains, the filter capacitor $C_2$ and the bulk capacitor $C_{10}$ are charged to the peak voltage of the mains supply. The capacitors $C_{12}$ and $C_{13}$, which support the IC supply voltage VCC, are charged via the startup resistors $R_{11}$ and $R_{12}$. The current consumption of the IC at this stage is typically below 90 µA until the supply voltage has reached typ. 10.6 V. Above this level the current consumption is typ. 120 µA, and a current source of typically 21.3 µA at the RES pin is activated, which detects a connected low-side filament. As long as the voltage level at the RES pin is below 1.6 V, the filament is assumed to be undamaged. A resistor $R_{36}$ is placed on the path of the measured current to adjust the voltage drop and – in conjunction with the capacitor $C_{19}$ – filters the alternating voltage on the filament during run mode. A current is fed through the resistors $R_{34}$ and $R_{35}$ to the high-side filament and through the resistors $R_{41}$, $R_{42}$, $R_{43}$ and $R_{44}$ to the LVS pin. A filament is detected if

the current is above typ. 12 µA. If the measured current at the LVS pin is too small, this fault generates a higher current level of typically 42.6 µA at the RES pin. The following points are checked in the sequence below before the IC activates the driver outputs.

- Connected filaments
- VCC > VVCCOn (14.0 V)
- Bus voltage between 12.5 % and 105 %

### Inverter section

With the first pulse the low side MOSFET $Q_3$ of the half-bridge is turned on. Then the floating capacitor $C_{14}$, which supplies the high-side control logic like a battery, is charged from capacitor $C_{13}$ via $R_{30}$ and the diode $D_6$. The resistor $R_{30}$ prevents activation of the overcurrent protection at the LSCS pin. This means that the high-side MOSFET $Q_2$ can already be turned on with the next half cycle. The capacitor $C_{16}$ together with the diodes $D_7$ and $D_8$ acts as a charge pump at the output of the half-bridge inverter. The continuous recharging of $C_{16}$ with the inverter frequency shifts energy for the supply voltage VCC of the IC to $C_{13}$. A surplus of energy is dissipated by the zener diode $D_9$. In addition, $C_{16}$ is used to limit the voltage slew rate and to produce zero voltage switching conditions.

During operation $C_{16}$ is recharged without losses in the deadtime periods of MOSFET $Q_2$ and $Q_3$ by the inductively driven current of the load circuit. Consequently, the succeeding turn-on of the MOSFET occurs at zero voltage. At turn-off, $C_{16}$ limits the voltage slew rate in such a way that the MOSFET channel is already turned off before the drain-to-source voltage has reached considerable levels. The inverter therefore creates negligible switching losses in normal operation. The load circuit of the inverter consists of a series resonant circuit with the resonance inductor $L_2$ and the resonance capacitor $C_{20}$. The lamp is connected in parallel to the resonance capacitor. This example shows voltage-controlled preheating. This means that the resonance-inductor $L_2$ has two additional windings. Each of those windings drives a current in the filament via the band-pass consisting of $L_{21}/C_{21}$ and $L_{22}/C_{22}$. The band-pass filter ensures that the current in the filaments is only flowing during the preheat phase. By reducing the frequency during run mode, the heating current is almost completely blocked by the band-pass. The load circuit also contains a capacitor $C_{17}$. This capacitor is charged to half the value of the bus voltage – operating the lamp symmetrically to the ground potential of the rectified mains supply is possible as a result.

### PFC

The MOSFET $Q_1$ of the PFC boost converter starts the operation simultaneously with the inverter. This circuit consists of the inductor $L_1$, diode $D_5$, MOSFET $Q_1$ together with the bulk capacitor $C_{10}$. Such a boost converter can transform the input voltage to any arbitrary higher output voltage. Using a suitable control method this converter is used as an active harmonic filter and for correction of the power factor. The input current follows the same sinusoidal waveform as the AC mains supply voltage. At the output of the PFC preconverter a feedback-controlled DC voltage is available at capacitor $C_{10}$ for the application. The PFC stage is operated with a controlled turn-on time without input voltage sense. A turn-on time set by the control unit is followed by a turn-off time, which is determined by the duration until the current in the inductor and hence in the diode too has reached the level zero. This point of time is detected by the voltage level at the zero current detector winding on the inductor $L_1$ and is fed to the IC via the resistor $R_{13}$ and the PFCZCD pin. The result is a gapless triangularly shaped current through inductor $L_1$ (so-called critical conduction mode), which is sustained for a turn-on time in the range of 24.0 µs down to 270 ns. A further reduction of the energy flow extends the turn-off time of the PFC MOSFET, causing triangularly shaped currents with gaps (discontinuous conduction mode). Such a control method allows stable operation of the boost converter over a large range of input voltage as well as output power. The current into the PFCZCD pin is used to perform THD correction for optimized THD.

The IC includes a couple of protection features for the PFC preconverter. The overcurrent is sensed at the PFCCS pin. The bus voltage, overvoltage and undervoltage are monitored at the PFCVS pin as well as the open loop detection. The ICB2FL03G includes the error amplifier with entire compensation built up by a digital PI regulator and a self-calibrating notch filter to suppress the voltage ripple of the bulk capacitor.

### Startup

The inverter starts at a frequency of 135 kHz. The frequency is reduced within 10 ms in 15 steps to the preheating frequency, which is adjustable by the resistor $R_{22}$. The duration of preheating can be selected

between zero and 2500 ms by the resistor $R_{23}$. Subsequently, the frequency is further reduced in 127 steps and a time period of 40 ms to the run frequency $f_{RUN}$, which is adjustable by the resistor $R_{21}$. The ballast should be designed in such a way that during the preheating phase the voltage across the lamp is low and at the same time the current in the filaments is large.

In the ignition phase following the preheating period the frequency of the inverter should be at – or at least close to – the resonance frequency of the resonant circuit in order to reach a voltage sufficient for ignition of the lamp. After successful ignition and frequency reduction to the run frequency the current in the lamp should reach its nominal value and the current in the filaments should become minimal. During the ignition period a high voltage at the lamp and a large current in the resonant circuit are generated due to the unloaded resonant circuit. The current in the resonant circuit is monitored by the resistors $R_{24}$ and $R_{25}$. As soon as the voltage at pin LSCS exceeds a level of 0.8 V, the operating frequency is controlled by the integrated ignition regulator, which works stable close to magnetic saturation of the resonant choke. If the level of 0.8 V at pin LSCS is not crossed any more, the operating frequency of the inverter decreases with the typical step width of the ignition phase towards the run frequency. As a result of this measure the ignition phase is extended from 40 ms up to 235 ms with a lamp not willing to ignite, while the voltage at the lamp remains on the level of the ignition voltage. If the run frequency is not achieved within 235 ms after finishing the preheating period, the IC switches to the failure mode. In such a situation the gate drives will be shut down, the current consumption of the IC will be reduced to max. 170 µA and the detection of the filaments and the input voltage will be activated. A restart is initiated dependent on the failure counter directly or either by lamp removal or after a new cycle of turn-off and turn-on of the mains voltage. After successful ignition a fixed pre-run time of typ. 625 ms is implemented to block several protection functions until stable lamp operation can be guaranteed.

### Protection functions

Numerous protection functions complement the basic functions of the ICB2FL03G. As soon as the level at pin LSCS exceeds the voltage threshold of 0.8 V for longer than 500 ns, it is recognized as a risky operating condition as it can occur during lamp removal in a running device or during transients in the mains voltage, and the IC switches to the failure mode. During run mode of the inverter a deviation from the typical zero voltage switching is recognized as an operation with capacitive load. Under such operating conditions, peak currents occur during turnon of the MOSFETs due to switched charging of the charge pump capacitor $C_{16}$. The IC distinguishes between two different types of capacitive load as follows:

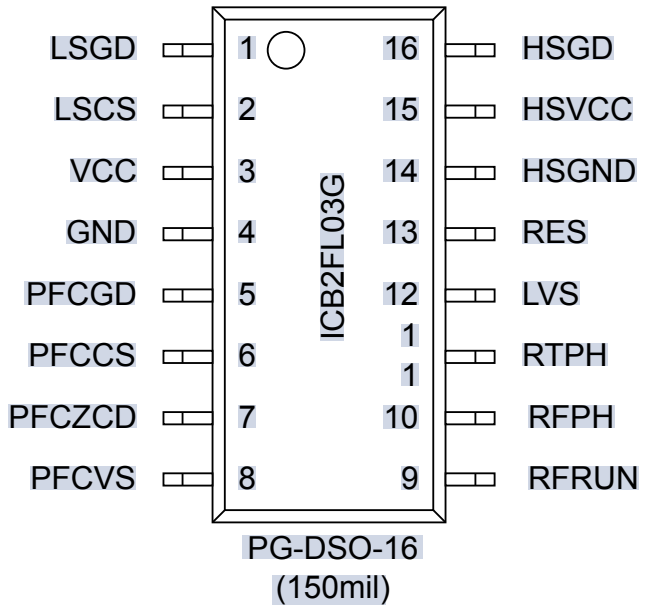
- Cap load 1 (idling detection / current mode preheating) ***Cap Load 1 (Idling Detection / Current Mode Preheating)***
- Cap load 2 (overcurrent / operation below resonance) ***Cap Load 2 (Overcurrent / Operation Below Resonance)***

Finally, dangerous operating conditions can arise when the fluorescent lamp reaches the end of lifetime or under operating conditions leading to thermal instability of the lamp. As a consequence, the lamp voltage becomes unsymmetrical or increases. To detect such operating conditions, the resistors $R_{41}$, $R_{42}$, $R_{43}$, $R_{44}$, $R_{45}$ and the capacitor $C_{40}$ measure the lamp voltage by evaluating the current through these resistors at the pin LVS. The turnoff threshold for EOL1 (End of Life 1) is at 210 $\mu A_{PP}$ with a duration of 620 µs. The rectifier effect with unsymmetrical lamp voltage is called EOL2 (End of Life 2) and the turn-off threshold is at +/- 42 µA with a duration of typ. 2500 ms. Due to intelligent failure differentiation, the ICB2FL03G is able to detect a surge at the input voltage without latching this failure.

The IC controls the operating frequency of the inverter during the different operating sequences, such as soft start, preheat, ignition, pre-run and run mode. During the different operating sequences only some of the protection features are active at first. All the protection features are active during run mode only. The integrated circuit ICB2FL03G has a unique combination of features that make design of high-quality lamp ballast with a low number of external components possible.

## 1.2 Pinning and Picture of the Demo Board

The following section shows the pinning of the IC and a picture of the demo board described in this document.




| Pin | Symbol | Function |
|---|---|---|
| 1 | LSGD | Low side Gate drive (inverter) |
| 2 | LSCS | Low side current sense (inverter) |
| 3 | VCC | Supply voltage |
| 4 | GND | Low side Ground |
| 5 | PFCGD | PFC Gate drive |
| 6 | PFCCS | PFC current sense |
| 7 | PFCZCD | PFC zero current detector |
| 8 | PFCVS | PFC voltage sense |
| 9 | RFRUN | Set R for run frequency |
| 10 | RFPH | Set R for preheat frequency |
| 11 | RTPH | Set R for preheating time |
| 12 | LVS | Lamp voltage sense |
| 13 | RES | Restart after lamp removal |
| 14 | HSGND | High side ground |
| 15 | HSVCC | High side supply voltage |
| 16 | HSGD | High side Gate drive (inverter) |

**Figure 2 Pinning of IC**

The pinning and a short pin description is given in ***Figure 2***. A detailed pin description can be found in the data sheet.

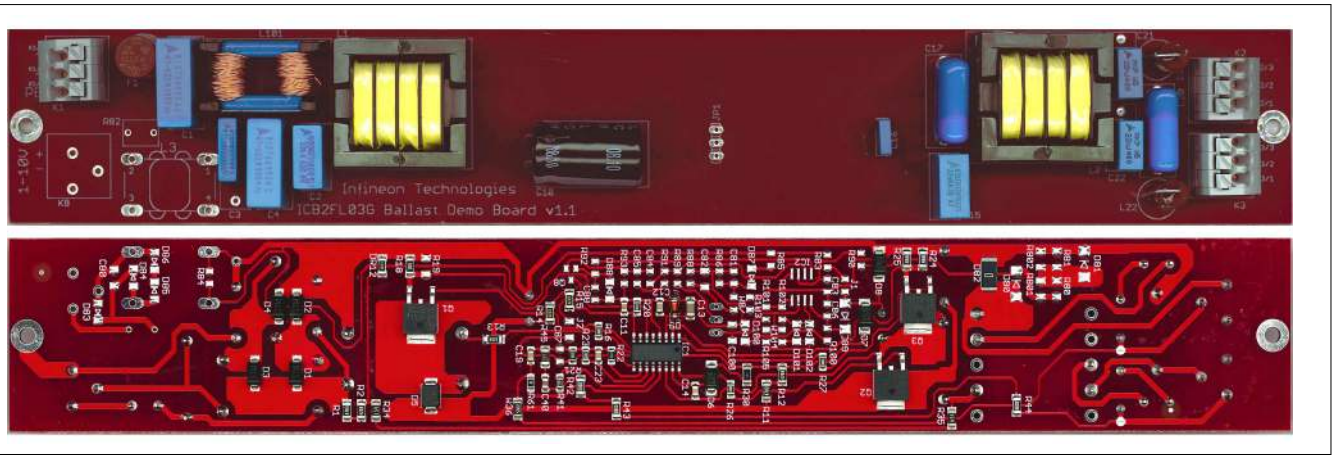



**Figure 3 Top and Bottom Views of the Demo Board**

***Figure 3*** shows a picture of the demo board for the 54W T5 design with voltage mode preheating. Please visit the Infineon Smart Lighting website (***http://www.infineon.com/smartlighting***) for further information.

## 1.3 Parameters of the Demo Board

***Table 1*** gives an overview of the operational characteristics of the demo board.

**Table 1 Operational characteristics of the 54W T5 demo board**

| | Value | Unite | Comment |
|---|---|---|---|
| $V_{IN}$ | 230 | $V_{ACRMS}$ | (180 V - 270 V) |

**Table 1 Operational characteristics of the 54W T5 demo board (continued)**

| | Value | Unite | Comment |
|---|---|---|---|
| $I_{IN}$ | 257 | $mA_{RMS}$ | @ 230 V input voltage |
| $P_{IN}$ | 59.1 | $W_{RMS}$ | @ 230 V input voltage (EEI = A2 CELMA efficiency class) |
| $V_{BUS}$ | 410 | $V_{RMS}$ | |
| $f_{PH}$ | 106.4 | kHz | |
| $f_{RUN}$ | 45.5 | kHz | |
| $t_{PH}$ | 1000 | ms | |
| $V_{Lamp}$ | 118 | $V_{RMS}$ | |
| $I_{Lamp}$ | 460 | $mA_{RMS}$ | |
| $V_{IGN}$ | > 620 | $V_{RMS}$ | |
| n | > 91 | % | With lamp after 30 min. operation in run mode @ 230 $V_{ACRMS}$ |
| PF | > 0.99 | | @ 230 $V_{ACRMS}$ input voltage |
| $A_{THD}$ | < 4 | % | @ 230 $V_{ACRMS}$ input voltage |

## 1.4 Description of Normal Start-up Steps

This section describes the normal start-up procedure from phase 1 (UVLO) to phase 8 (run mode). ***Figure 4*** shows a measurement and diagram from the start-up procedure. Dependent on the voltage at the RES pin, the current consumption of the IC can be higher due to $I_{RES1}$ to $I_{RES4}$.

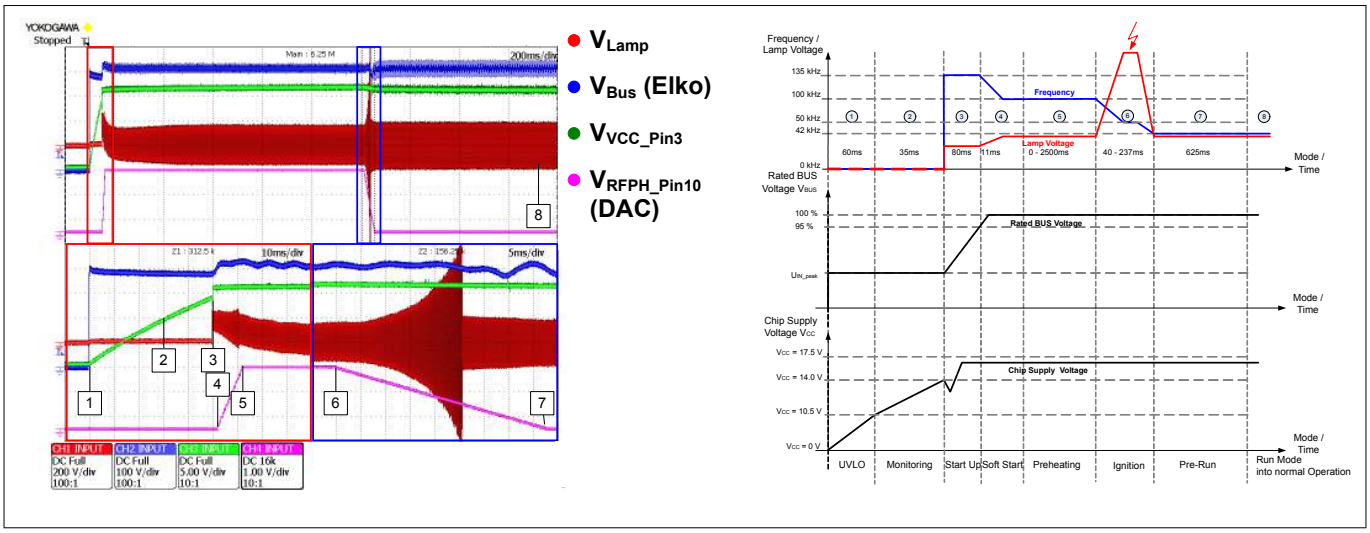



**Figure 4 Start-up Procedure**

The current consumption of the IC in Phase 1 (UVLO) is $I_{VCCqu1}$. The current fed via the high ohmic VCC start-up resistors ($R_{11}$ and $R_{12}$) charges the VCC capacitor and delivers this quiescent current. After reaching

a first threshold of $V_{VCCOff}$ the IC goes into monitoring mode and checks for connected cathodes. The current consumption in this Phase 2 is $I_{VCCqu2}$ and has to be also delivered via the start-up resistors. The voltage at the VCC pin rises up to $V_{VCCOn}$ and the IC becomes active and starts inverter switching (provided that both cathodes are present). Phase 3, also called start-up, activates the whole IC and leads to a current consumption of $I_{VCCSupply}$.

The internal reference starts up within the first 130 µs and the IC checks the level of the bus voltage. If the bus voltage is in the specified range of 12.5 % and 105 %, the LSGSD switches on several times to charge the HSVCC capacitor via $R_{30}$ and $D_6$. After reaching the HSVCC turn-on threshold of $V_{HSVCCOn}$ the HSGD also starts working (HSGD and LSGD alternating) and supplies the IC via a charge pump, and the VCC voltage rises to the voltage clamped by $D_9$. The inverter works with a start-up frequency of $f_{StartUp}$. To prevent the IC reaching the UVLO threshold of $V_{VCCOff}$ when all gate drives become active at the same time, the PFC section starts working with a delay of about 200 µs (see also ***Figure 5***). After reaching a bus voltage of 95 % the IC enters soft start, phase 4.

In this phase the IC shifts the frequency down to the adjusted preheating frequency. This frequency shift can be seen at the signal at the RFPH pin when the voltage rises from GND to 2.5 V (***Figure 4***).

After reaching the preheating frequency the IC stays in this preheating phase (Phase 5) for the adjusted preheating time. At the end of the preheating time the IC enters ignition mode (Phase 6) and begins reducing the frequency down to the adjusted run frequency. This can also be seen on the signal at the RFPH pin. The voltage at this pin falls until the voltage at the LSCS pin reaches the threshold of 0.8 V. Then the ignition regulator begins regulating the ignition voltage to this maximum level, also during magnetic saturation of the resonant choke. While regulating the ignition voltage, the voltage at the RFPH pin remains at the achieved level between 2.5 V and GND.

After successful ignition during $t_{NOIgnition}$ (limited duration of the ignition phase) the IC enters the pre-run mode, Phase 7, and the voltage at the RFPH pin falls to GND. The pre-run mode is a safety mode (with limited protection functions active for $t_{PRERUN}$) in order to prevent a malfunction of the IC due to an instable system – e.g., the lamp parameters are not in a steady state condition. In this phase the ignition regulator is also active in order to re-ignite the lamp if the lamp shows very poor ignition behavior. After a duration of $t_{PRERUN}$ the IC disables the ignition regulator and switches to the run mode (Phase 8) and all protection functions become active.

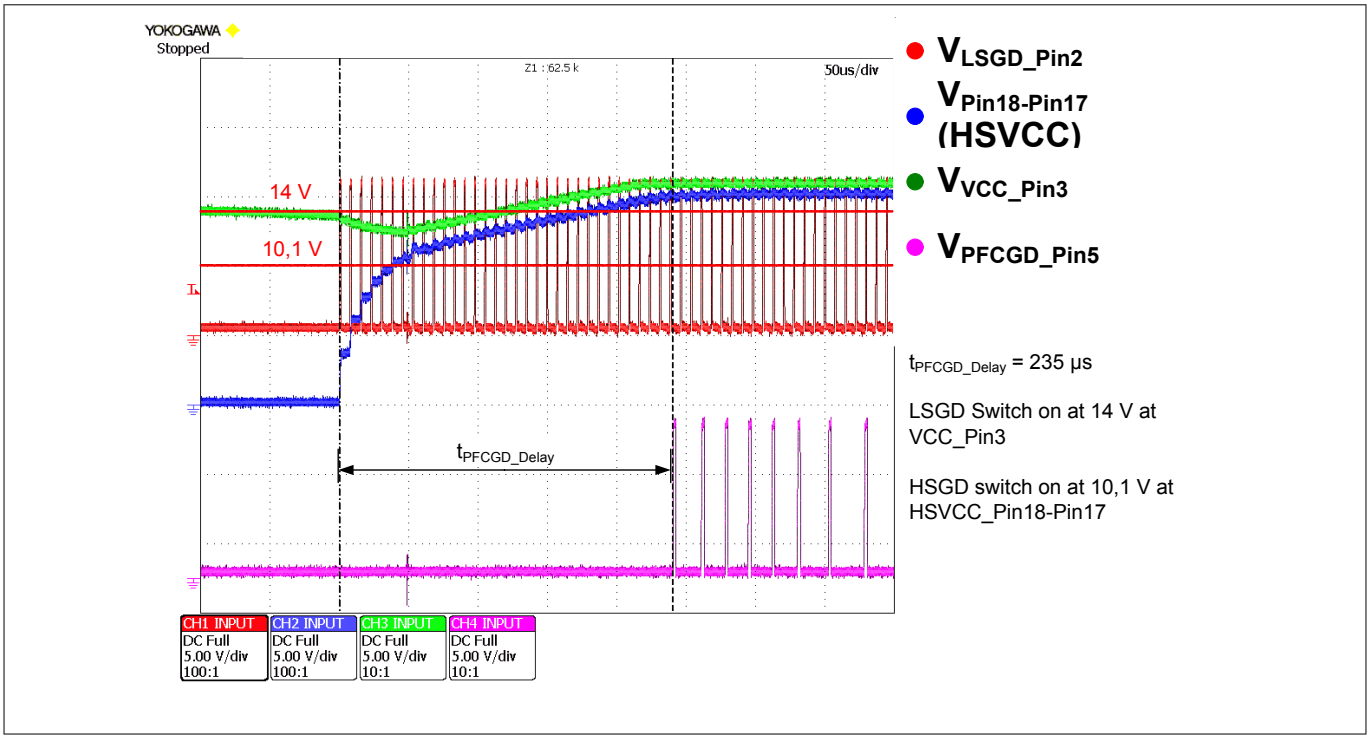



**Figure 5 PFCGD Start-up Delay**

## 1 Introduction

A detailed evaluation of the start-up is shown in ***Figure 5***. After reaching the $V_{VCCO}n$ threshold the IC enters power-up mode and starts LSGD switching with a short internal delay. The LSGD turns on several times to charge the HSVCC. In this time the voltage at the VCC pin breaks down a little bit because the IC current consumption is now higher than the current fed from the high ohmic start-up resistors $R_{11}$ and $R_{12}$. The VCC capacitors $C_{12}$ and/or $C_{13}$ must be large enough to store the energy needed for charging the HSVCC capacitor $C_{14}$ to the $V_{HSVCCOn}$ threshold without reaching the UVLO threshold at VCC. After reaching the $V_{HSVCCOn}$ threshold (typ. 10.4 V) the HSGD starts working too, and the VCC supply is now generated from the working half-bridge via the charge pump and the energy provided is high enough to increase the VCC voltage up to the clamped limit of the external Z-diode $D_9$. The PFCGD starts working with a delay of about 235 µs. This delay is implemented in the IC to ensure a stable VCC supply before the current consumption of the IC becomes higher due to the additional working PFCGD. This feature prevents UVLO during the start-up process. ***Troubleshooting*** provides advice on how to react to malfunctions in the functional sequence described here.

# 2 VCC Chip Supply

The high ohmic resistors ($R_{11}$ and $R_{12}$) for the startup supply have to be connected to the bus electrolytic capacitor to ensure an IC supply during start-up mode, latch mode and short interruption of the input voltage (emergency lighting feature according to VDE 0108). The IC logic implements an ability for self-generated reset. The condition for reset is an active IC with a current consumption of about $I_{VCCSupply}$ with inactive gate drives. This results in a falling VCC voltage down to the $V_{VCCOff}$ threshold, also called UVLO (Undervoltage Lockout), which resets the IC via the VCC. At this self-generated UVLO the IC goes into active mode with inactive gate drives. Without a working half-bridge there is no supply via the charge pump and the VCC capacitor discharges down to $V_{VCCOff}$ (UVLO threshold), leading to a restart of the IC.

Please refer to Sections 3.2 and 3.3 of the Data Sheet for further information to functional restrictions in cases in which the start-up resistors or an external supply can provide too much current, and the IC cannot discharge the VCC capacitor. In latched failure mode the IC has a current consumption of $I_{VCCLatch}$ and this current has to be delivered by the start-up resistors. The current out of the RES pin has to be considered for calculation of the start-up resistors together with $I_{VCCLatch}$.

## 2.1 Operation with Half-Bridge not Working

Without an active inverter section the start-up resistors have to supply the IC with a minimum current of $I_{VCCLatch}$. Please note that this current must be possible at the minimum input voltage. (This range is necessary for correct restart after internally generated UVLO and correct function of the hiccup mode). A maximum current of 2 mA is a good design proposal for correct IC function at self-generated UVLO.

For the start-up of the IC supply it is important to check the voltage level at the RES pin. Due to the capacitor and resistor at the RES pin, the dv/dt at this pin is limited and, for example, might be slower than the VCC dv/dt at external supply or with low-ohmic start-up resistors. The voltage $V_{RES}$ must reach the filament detection level before the IC supply voltage VCC reaches the $V_{VCCOn}$ threshold. Otherwise, removed filaments cannot be detected correctly because the filament detection status is checked between $V_{VCCOff}$ and $V_{VCCOn}$.

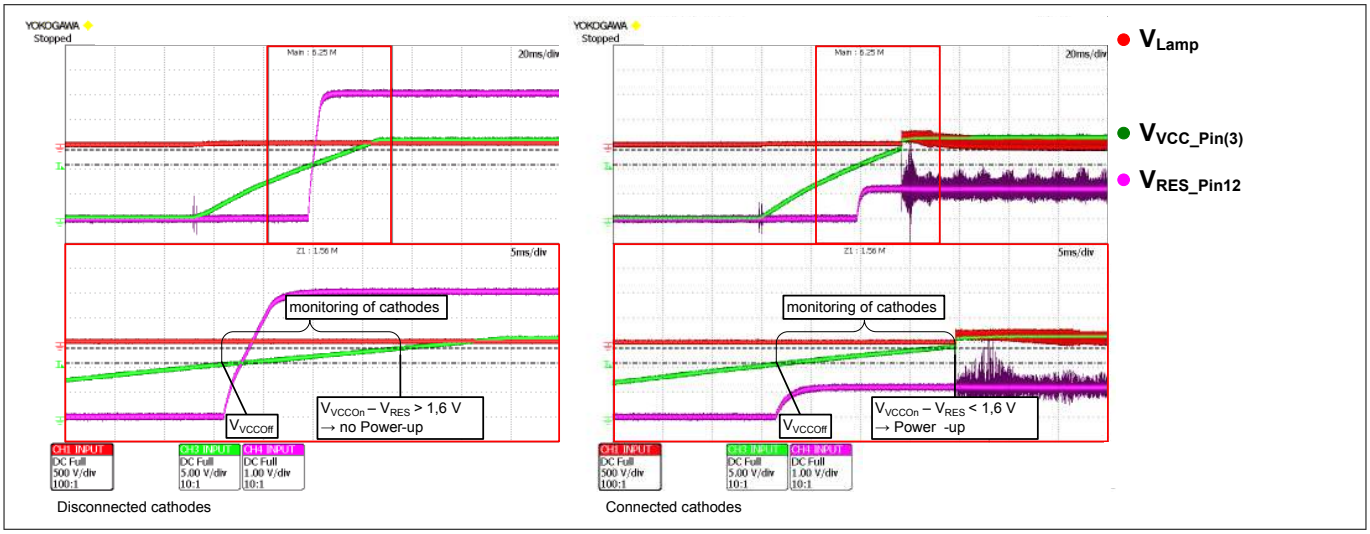



**Figure 6 dv/dt at VCC and RES Pins @ Start-up**

*Figure 6* shows two oscillograms with the signals at the VCC and RES pins when connecting the input voltage. The left oscillogram shows the signals when the cathodes are open and the voltage at the RES pin rises to > 1.6 V. This voltage level must be reached while the IC monitors the cathodes for correct filament detection. The right oscillogram shows that the IC goes into power-up when the cathodes are connected.

## 2.2 Operation with Half-Bridge Working

With continuous working of the inverter section (LSGD and HSGD) the IC is supplied mainly via the charge pump ($C_{16}$, $D_7$ and $D_8$) connected to the half-bridge. With this solution of a VCC supply during run mode, the IC can generate an UVLO by itself by stopping the inverter.

An example of a self-generated UVLO is shown in ***Figure 7***. To understand the following explanation, the state diagram in the Data Sheet (Section 3.3) must be viewed. Removing the board supply $V_{IN}$ in run mode leads to discharging of the bus electrolytic capacitor. After $V_{BUS}$ reaches the 75 % threshold the IC detects bus undervoltage and goes into “Fault U” failure handling with deactivation of the gate drives and entry to the powerdown mode. After about 750 ms the state machine exits the decision block “Counter Skip Preheat > 7” with “Y” and then goes into active mode with inactive gate drives. As a consequence, the VCC capacitor is discharged to the $V_{VCCOff}$ threshold (red circle). This UVLO resets the IC logic.

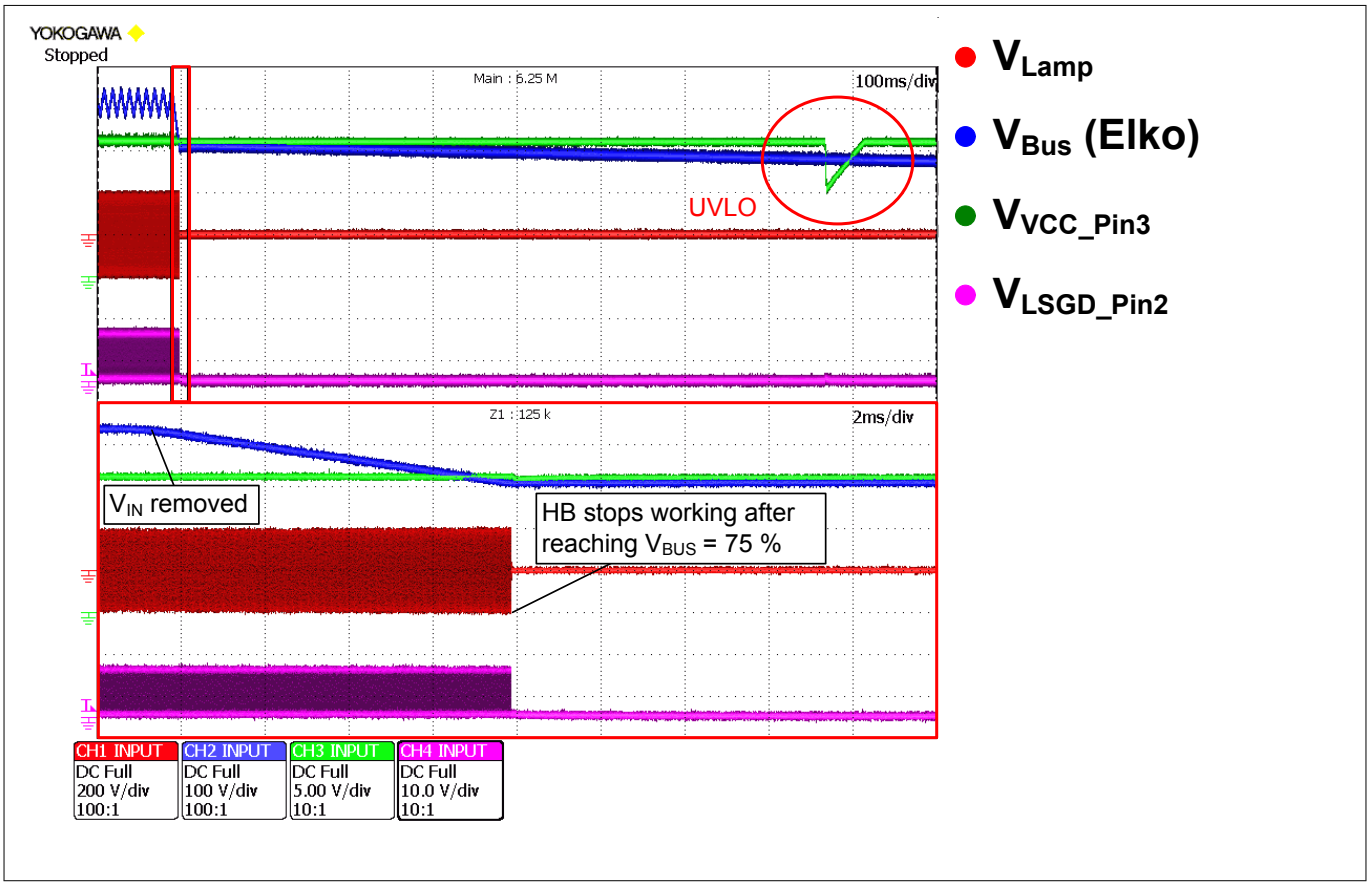



**Figure 7 Example of Self-Generated UVLO after Counter Skip Preheat > 7 = Y**

# 3 PFC

The control of the PFC starts with a fixed operating frequency and increasing on-time, and changes over into critical conduction mode (CritCM) operation (also called borderline/transition conduction mode) as soon as a sufficient signal level at the pin PFCZCD is available. The benefit of this feature is to save external components for the compensation and for the synchronization with the AC input voltage. The dynamic response and the suppression of the superimposed ripple of the bus voltage fulfill even high requirements. Finally, during light load conditions the PFC control changes the operating mode from CritCM to DCM (discontinuous conduction mode) which provides stable operation even down to no load.

A detailed description of the digital control loop for PFC can be found in the Data Sheet (Section 2.4.3)

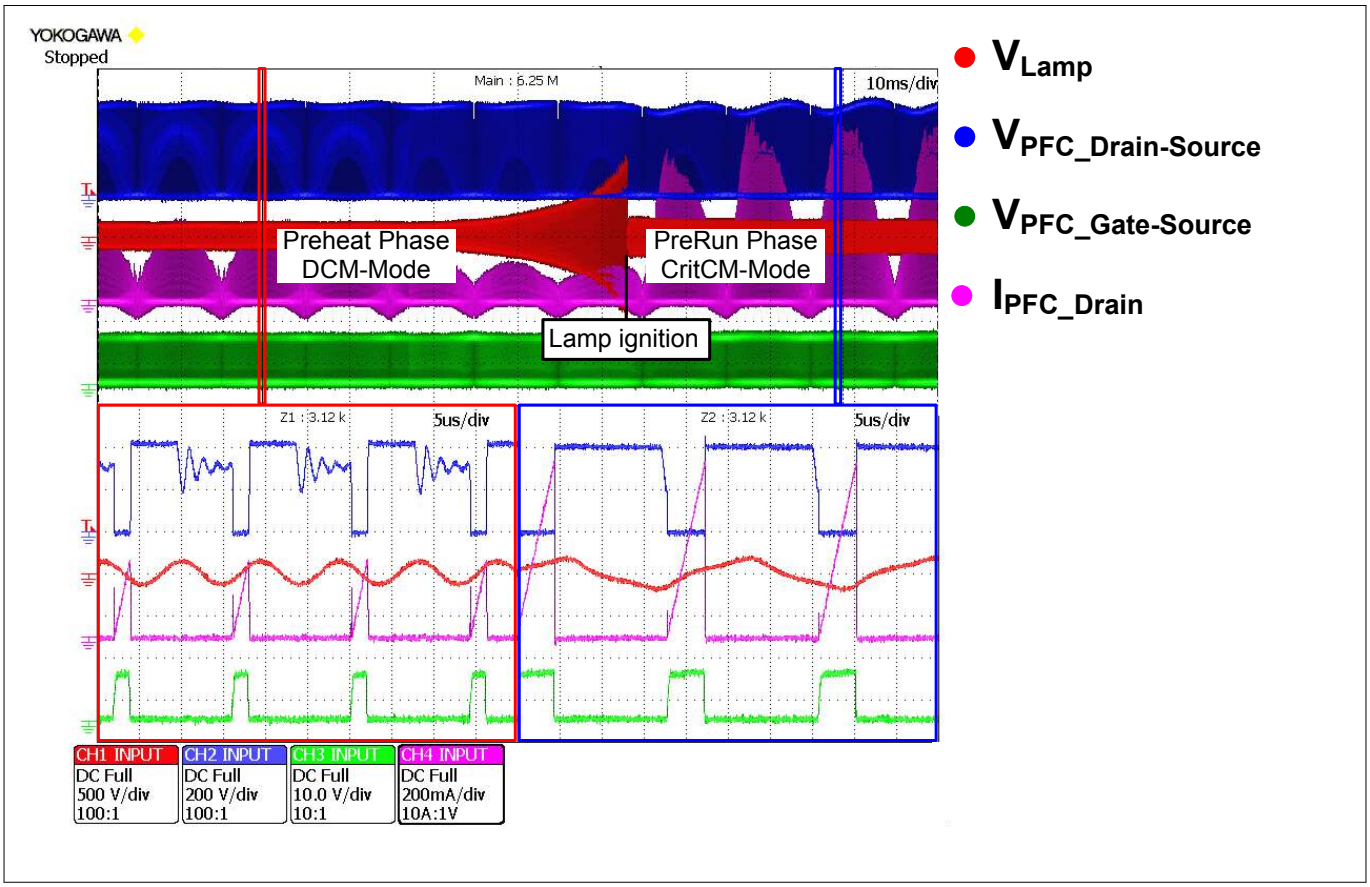



**Figure 8 DCM and CritCM Mode of the PFC Stage**

***Figure 8*** shows an oscillogram of the two operating modes DCM and CritCM of the PFC. The bottom left of the oscillogram shows the DCM waveforms under light load in the preheating phase. The bottom right illustrates the CritCM waveforms during run mode with a higher load.

## 3.1 THD Correction

Figure 3-2 shows two oscillograms at different input voltages. The bottom thirds of the oscillograms show the PFCGD on-time over one input voltage half-wave. When the input voltage is decreasing, the on-time of the PFCGD increases and has its maximum at the minimum of the input voltage. The oscillogram on the left side shows the on-time at 180 $V_{AC}$ input voltage and the oscillogram on the right side is taken at an input voltage of 230 $V_{AC}$. The oscillograms demonstrate the excellent performance of the PFC stage. In both cases the THD is below 4 % and no gap in current flowing near the input voltage minimum is visible. For proper THD correction in other designs it is necessary to modify the resistance at the PFCZCD pin in respect to the ratio and value of the PFC choke and the MOSFET size. A good way to find an optimum is to calculate $R_{ZCD}$ with ***#unique_14/unique_14_Connect_42_equation-block_uj3_xzq_nnb*** in a first step.

Calculation of $R_{ZCD}$:

$$R_{ZCD} = \frac{\frac{R_{ZCD}}{N_{PFC}} \cdot V_{BUS}}{1.5\,mA}$$

In a second step a potentiometer can be used to evaluate the optimal value for best THD optimization.

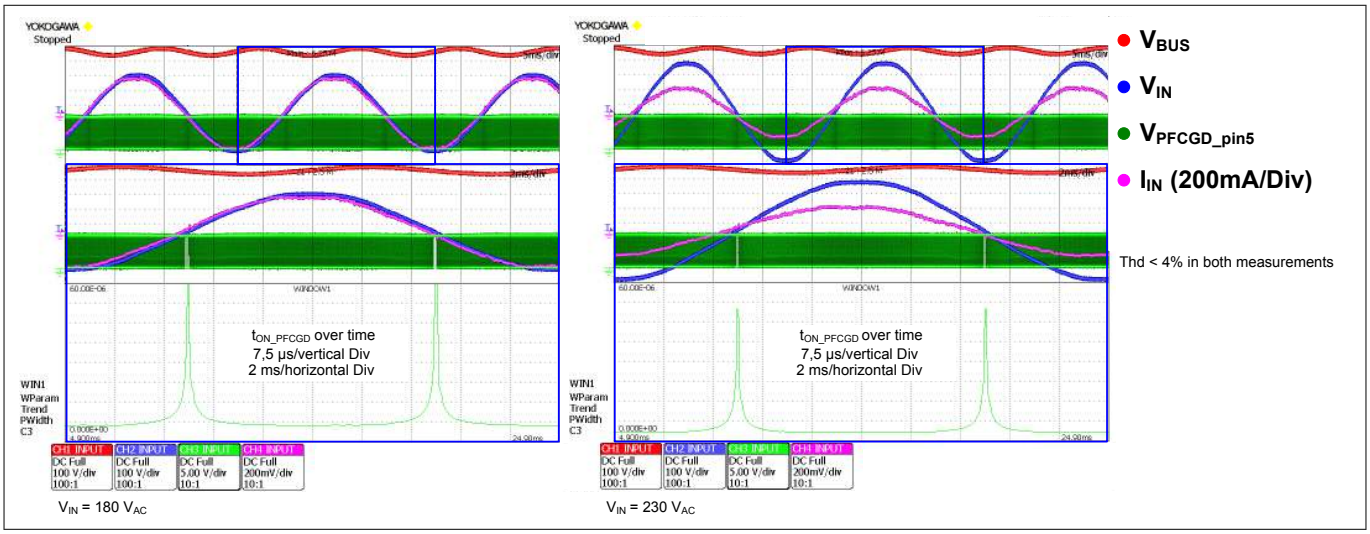



**Figure 9 THD Correction: PFC On-time Extension over Input Half-Wave**

***Figure 9*** shows the waveform of the input current with a THD-optimized resistor at the PFCZCD pin. The overall THD for the input current harmonics is < 4 % with a gapless input current (magenta waveform). The bottom third of the oscillogram shows the on-time of the PFC MOSFET. Near to the zero-crossing of the input voltage, the on-time is increased by the IC via the signal at the PFCZCD pin for THD optimization.

# 4 Ignition Regulator – Control during Ignition

After entering the ignition mode, the frequency decreases from the preheating frequency to the run frequency. This frequency shift (generated by the internal digital logic) can be measured at the RFPH pin. The voltage is 2.5 V during preheating mode and decreases down to GND potential. When the adjusted ignition voltage is reached for the first time, the digital frequency control stays at its working point and an analog regulator takes over the ignition voltage regulation in respect to the adjusted frequency of the digital logic. The digital logic readjusts the frequency only when the working point leaves the regulation area of the analog regulator. After lamp ignition, the resonant circuit is damped by the lamp and the IC reduces the frequency down to the adjusted run frequency (Figure 4-1). The ignition regulator is also active in the pre-run phase to improve the ignition of lamps with bad ignition behavior.

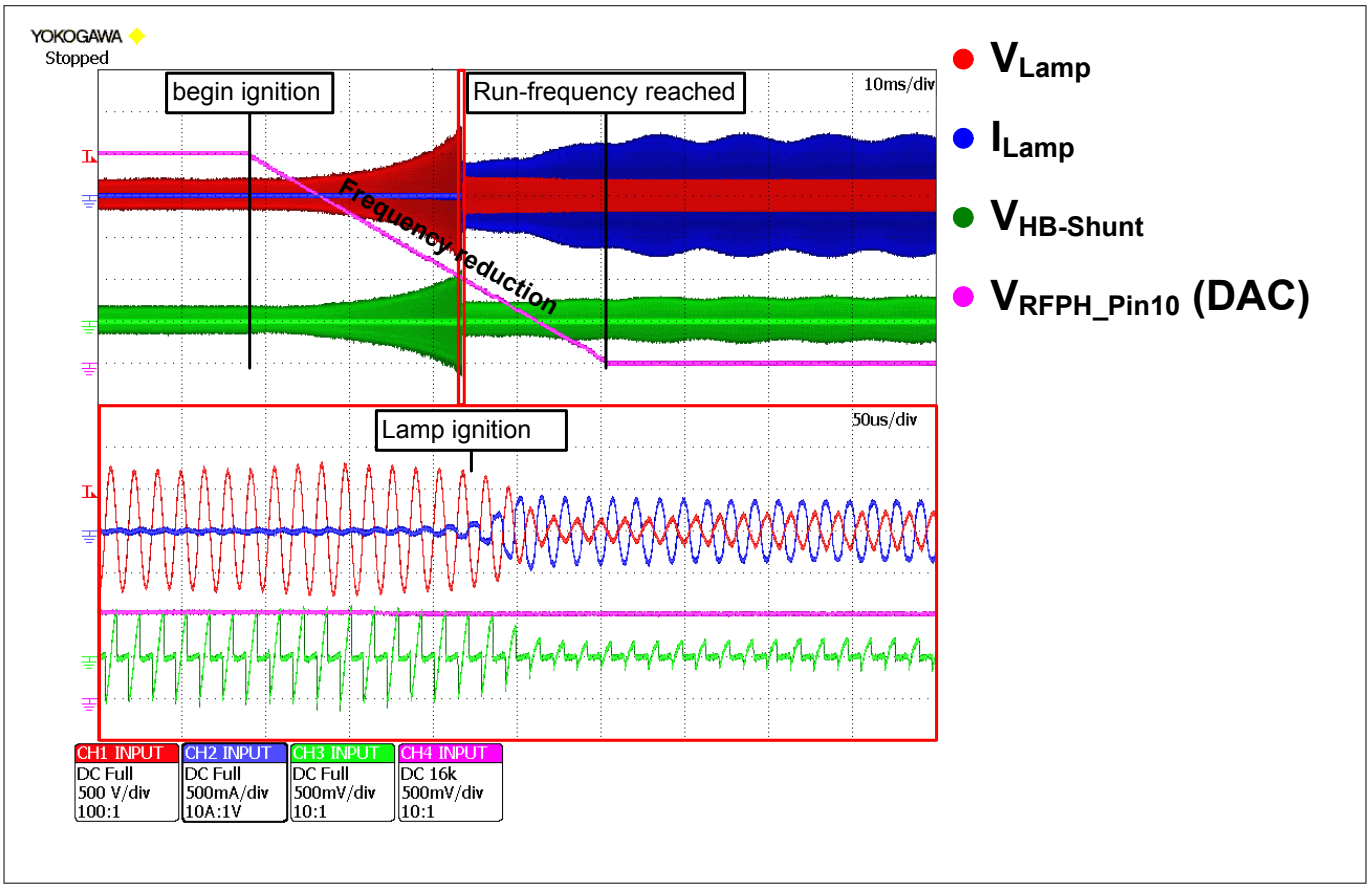



**Figure 10 Normal Ignition Phase**

If the voltage at the RFPH pin (DAC) reaches 0 V during the ignition phase without successful lamp ignition, the sequence control enters the pre-run phase with the ignition regulator still activated. This can be caused due to very high EMI at the LSCS pin, or due to a calculation of the resonant circuit and/or LSCS shunt resistors, that the ignition frequency is close to or below the run frequency. Several heavy bus voltage breakdowns during ignition can cause this behavior too. The ignition timeout timer cannot be set and the ignition voltage can stay about 625 ms longer than the maximum ignition time at the lamp.

## 4.1 Operation Close to Different Saturation Levels

***Figure 11*** shows four oscillograms taken with chokes of different saturation levels. The top-left oscillogram was taken with the standard choke of the demo board, the other ones use modified chokes with a smaller current capability and saturation effects. The ignition voltage is approximately constant over the saturation behavior of the lamp choke and best ignition voltage regulation (also at high temperatures of the lamp choke) is possible.

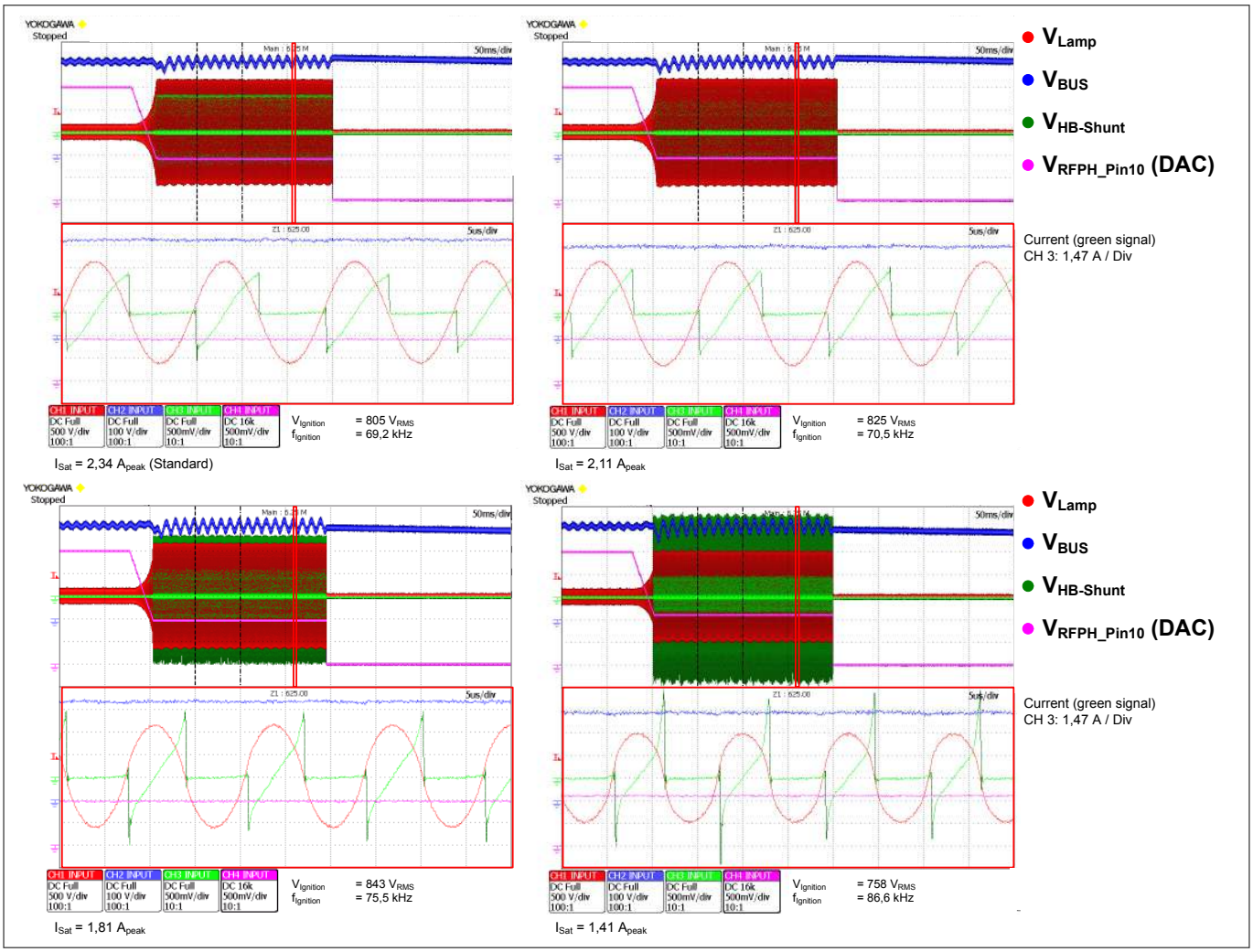



**Figure 11 Ignition voltage @ different levels of saturation of the resonant choke**

These oscillograms demonstrate the performance of the ignition regulator at different levels of saturation. Actually, at relatively low saturation levels the ignition voltage is a little bit higher than with the standard choke. Even at very high saturation levels the ignition voltage breakdown is only about 5 %. Consequently, this ignition control concept is very suitable for designs working close to the magnetic saturation of the resonant choke and enables best ignition voltage regulation, also at higher temperatures of the ballast components. Due to the thermal behavior of the ferrite, the ability of the ignition regulator to work with saturated chokes offers a great advantage for restarts with a warmed-up ballast – for example, after a certain running time.

## 4.2 Bus Voltage Breakdown during Ignition

The following measurements of the ignition regulator at bus voltage breakdown were taken with small modifications to the demo board. The resonant capacitor $C_{20}$ was mounted in a direction to realize current mode preheating. The demo board was prepared with 10 Ω substitution resistors for each cathode. This results in very high power consumption during ignition mode. The input voltage was also reduced to 170 $V_{AC}$ to provoke bus voltage breakdown during ignition mode because of the limited power that can be transferred by the PFC stage. ***Figure 12*** shows two oscillograms taken under these conditions to demonstrate that the ignition voltage control concept is also very suitable for current mode preheating ballasts in which the load during ignition becomes very high.

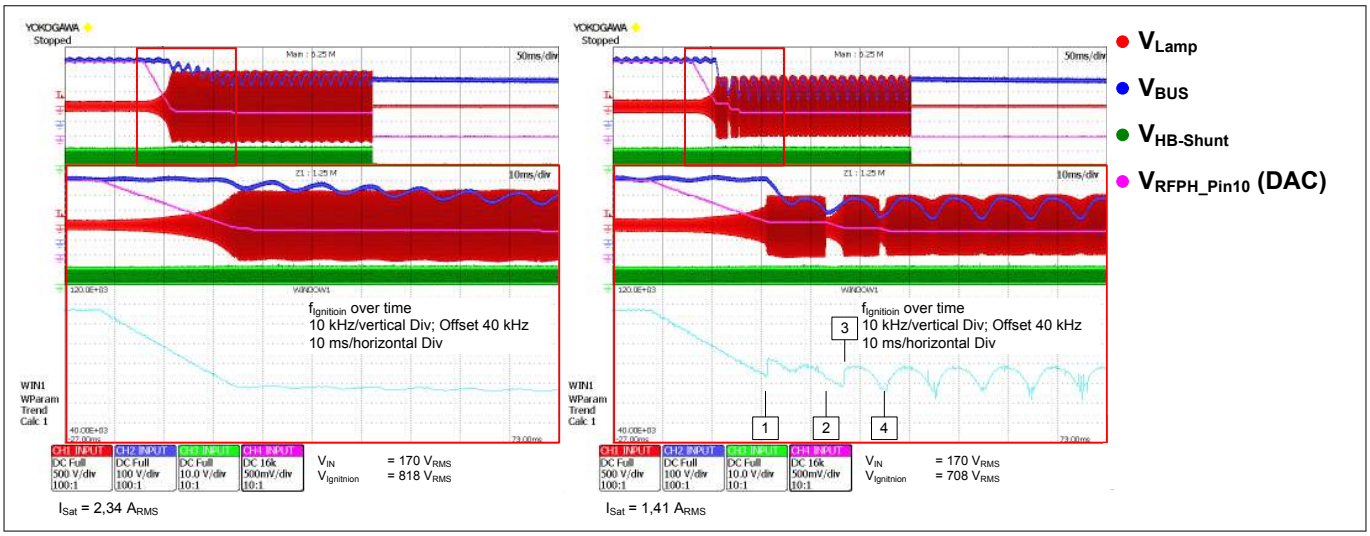



**Figure 12 Ignition Regulator at BUS Voltage Breakdown during Ignition Phase**

The left oscillogram shows the ignition voltage without saturation effects of the resonance inductor. The ignition frequency over time is illustrated in the bottom third of the oscillograms. After entering the ignition mode, the frequency decreases from about 107 kHz down to 70 kHz. At this point the frequency is regulated by the analog ignition voltage regulator to the maximum ignition voltage level. The oscillogram shows that there is no influence of the heavy bus voltage breakdown on the ignition voltage. The ignition regulator can compensate the bus voltage breakdown of about 25 % from 400 V down to 300 V completely

The oscillogram on the right shows the behavior in the same application under the same conditions but with heavy saturated choke – see ***Figure 11***, bottom right. The digital logic reduces the inverter frequency down to about 75 kHz, then the ignition voltage reaches the adjusted ignition voltage and the analog regulator takes over the voltage control (Point 1). Due to the high bus voltage breakdown the analog regulator reaches the end of its working area and the digital logic compensates for this by reducing the inverter frequency again (Point 2 to Point 3). After this, the analog regulator takes over the regulation as seen at Point 1. At Point 4 the working area of the analog regulator is left again and the digital frequency control reduces the frequency. From this point onward, the analog ignition control regulator takes over and almost entirely eliminates the high bus voltage ripple of about 150 V.

# 5 Filament Detection

The high-side filament is detected via the LVS pin while the low-side filament is monitored via the RES pin. For proper filament detection the LVS and RES circuits have to be dimensioned correctly because they act together and not independently of each other. The RES pin acts as a current source and in order of the voltage at this pin (generated with a resistor $R_{36}$, connected via the low-side filament to GND) the IC detects the filaments. The current flowing out of the RES pin depends on the voltage level $V_{RES}$ and the status of the high-side filament.

When there is no current or a current below the filament detection limit flowing into the LVS pin, the current out of the RES pin is doubled and, as a consequence, the voltage at this pin rises and reaches the level for detecting missing filaments. In this way, the result from the high-side filament detection is mirrored at the RES pin. If the lowside filament at the RES pin is not inserted, the voltage at this pin rises and also reaches the level for detecting missing filaments because there is no GND connection.

## 5.1 LVS Pin

This pin has the function of detecting the high-side cathode before the IC starts and lamp removal in failure mode. In the run mode the pin detects the EOL1 (overload) and EOL2 (rectifier effect) conditions. This is realized by analyzing the amplitude and the DC offset of the lamp voltage via an equivalent current into the pin. If the functions are not needed, the LVS pin can be deactivated by connecting the pin directly to GND. In this case EOL1 and EOL2 detection via this pin is not possible. A deactivated LVS pin can be reactivated when the voltage at this pin goes higher than $V_{LVSEnable1}$ during run mode. For correct functioning of the LVS pin, the resistors for filament detection have to be connected directly after the line rectifier to ensure that the short input voltage interruption can be detected with the LVS pin. The charge of the preheating capacitor $C_{21}$ must be covered by the capacitor in the EOL network $C_{40}$ in such a way that no fail detection of inserted cathode occurs. If the capacitor in the preheating circuit $C_{21}$ has a high capacitance and $C_{40}$ is relatively low, a transient current flows via $C_{21}$ and $L_{21}$ that can be high enough to lead to high-side filament detection. An internal voltage of 5 V can be used for calculation of the LVS current before startup (not specified in the Data Sheet – see also ***The IC Starts without a High-Side Filament***). This means that the current flowing into the LVS pin can be calculated with the voltage over the LVS series resistor (between $R_{41}$ and $R_{42}$) related to GND subtracted by 5 V and divided by the value of $R_{41}$. The safest solution is to design the LVS network in such a way that the voltage at $C_{40}$ stays below 5 V without a connected HS filament.

Calculation of $I_{LVSstartup}$:

$$I_{\mathrm{LVSstartup}} = \frac{V_{C40\mathrm{toGND}} - V_{\mathrm{BUS}}}{R_{41}}$$

***Figure 13*** shows an oscillogram with the waveforms for start-up without a connected high-side filament. The voltage across $C_{40}$ in reference to GND is below 5 V (green signal). Due to the internal voltage of 5 V there is no current flowing into the LVS pin and no wrong high-side filament detection can occur. If this voltage rises above $5V+I_{LVSSink}$ multiplied by the value of $R_{41}$, wrong high-side filament detection can provoke a single start-up of the IC. In this case the value of $C_{40}$ or $R_{41}$ can be increased. If possible, decreasing the capacitance in the preheating circuit can help to reduce the current flowing into the LVS pin. A third option is to reduce the feeding voltage by the divider $R_1$, $R_2$, $D_{R12}$ from the rectified AC input voltage.

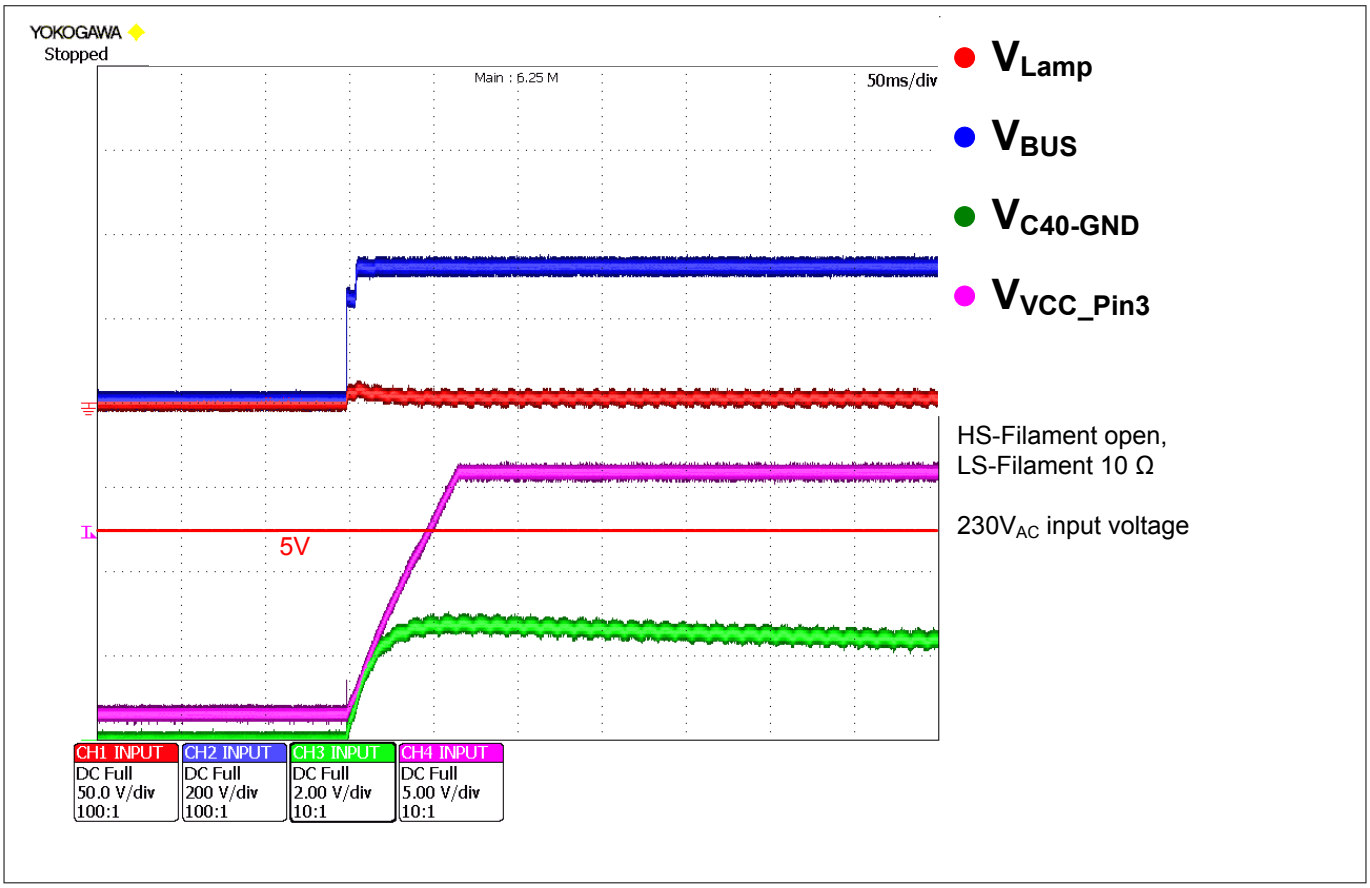



**Figure 13 Startup without High-side Filament**

During run mode there is no high-side filament detection via the LVS pin.

A step-by-step tutorial for dimensioning of the EOL1 and EOL2 thresholds is given in ***Sample Calculation: EOL for 54W T5 Design (Excel)*** of this document.

## 5.2 RES Pin

To deactivate the filament detection for high-side and low-side filaments the RES pin can be connected directly to GND. As explained in ***Filament Detection***, this pin is a current source and detects if the filaments are present via the voltage drop at $R_{36}$. The current out of the RES pin is affected by the LVS status during start-up and the actual voltage at this pin. During run mode, this pin detects the low-side filament. When this filament is broken or removed, the voltage will rise to 5 V. The voltage passes the $V_{RES3}$ threshold for detecting a missing low-side filament.

For current mode preheating designs an additional series resistor to the RES pin (for example 330 Ω) is recommended to avoid destroying the ESD structure if the voltage at the RES pin rises to higher levels. This voltage spike can occur in current mode preheating designs during lamp removal and depends on the resonant circuit and RES pin wiring.

For reliable filament detection during start-up, the voltage $V_{RES}$ has to reach the filament detection level until the chip supply voltage VCC reaches the turn-on threshold of $V_{VCCOn}$ (see also ***Figure 6***).

# 6 Detection of Failures

This chapter provides advice in the event of failures along with examples for evaluating the failure detection functions. Detailed descriptions of the failure conditions can be found in the Data Sheet. Chapters 3 and 4 of the Data Sheet show tables and flow charts indicating which protection feature is active in which operating mode and how the IC will react to each particular failure.

## 6.1 Surge Detection

The ICB2FL03G implements a special detection for surge events. Bus overvoltage followed by inverter overcurrent is detected as a surge, which leads to a restart without latching this failure. Figure 6-1 shows two oscillograms with the signals under surge conditions. For these oscillograms the half-bridge MOSFETs were replaced by 500 V types to provoke an earlier avalanche breakdown in the case of bus overvoltage. In the original mounting with 600 V MOSFETs the surge voltage must be so high that other components can become destroyed before the half-bridge breakdown initiates surge detection.

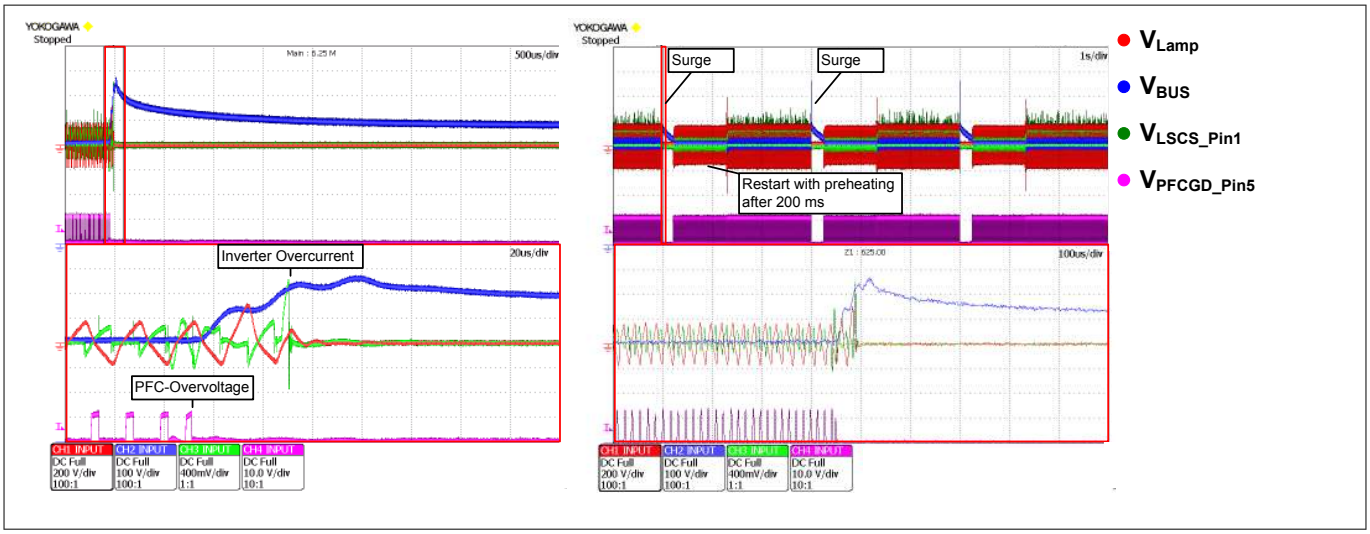



**Figure 14 Surge Detection; Surge Pulse of 1100 V**

The left oscillogram shows one single surge event with a higher resolution and the right one shows three surge events for explanation of the flow diagram. Directly after bus voltage rising due to the surge pulse, the PFC stage detects PFC overvoltage and stops the PFCGD. At a bus voltage of about 620 V the half-bridge MOSFET breaks down due to the avalanche effect. This results in a high current spike at the LSCS pin. The IC detects this overcurrent during overvoltage and stops the inverter gate drives (see Chapter 3.3 in the Data Sheet: “Fault A”). This signal combination does not increment the “Fault Counter” and leads to an IC restart after about 200 ms with preheating. This can be seen in the right oscillogram.

It is important that the time constant of the low-pass filter at this PFCVS pin (generated by the voltage divider and $C_{11}$) is small enough that the voltage can rise fast enough to the 109 % threshold during surge conditions. Otherwise the surge condition cannot be clearly detected.

## 6.2 Inverter Overcurrent Protection

The inverter overcurrent protection via the LSCS pin detects two different thresholds dependent on the actual operation mode. The first threshold of $V_{LSCSOvC2}$ is only active during preheating and run modes. In all other modes the detection threshold of $V_{LSCSOvC1}$ is active for inverter overcurrent protection. Overshooting these thresholds results in a single restart of the IC. After a second detection within 40 s the IC goes into latched fault mode. This means that an input voltage interruption or a lamp removal is necessary for a new start-up of the IC.

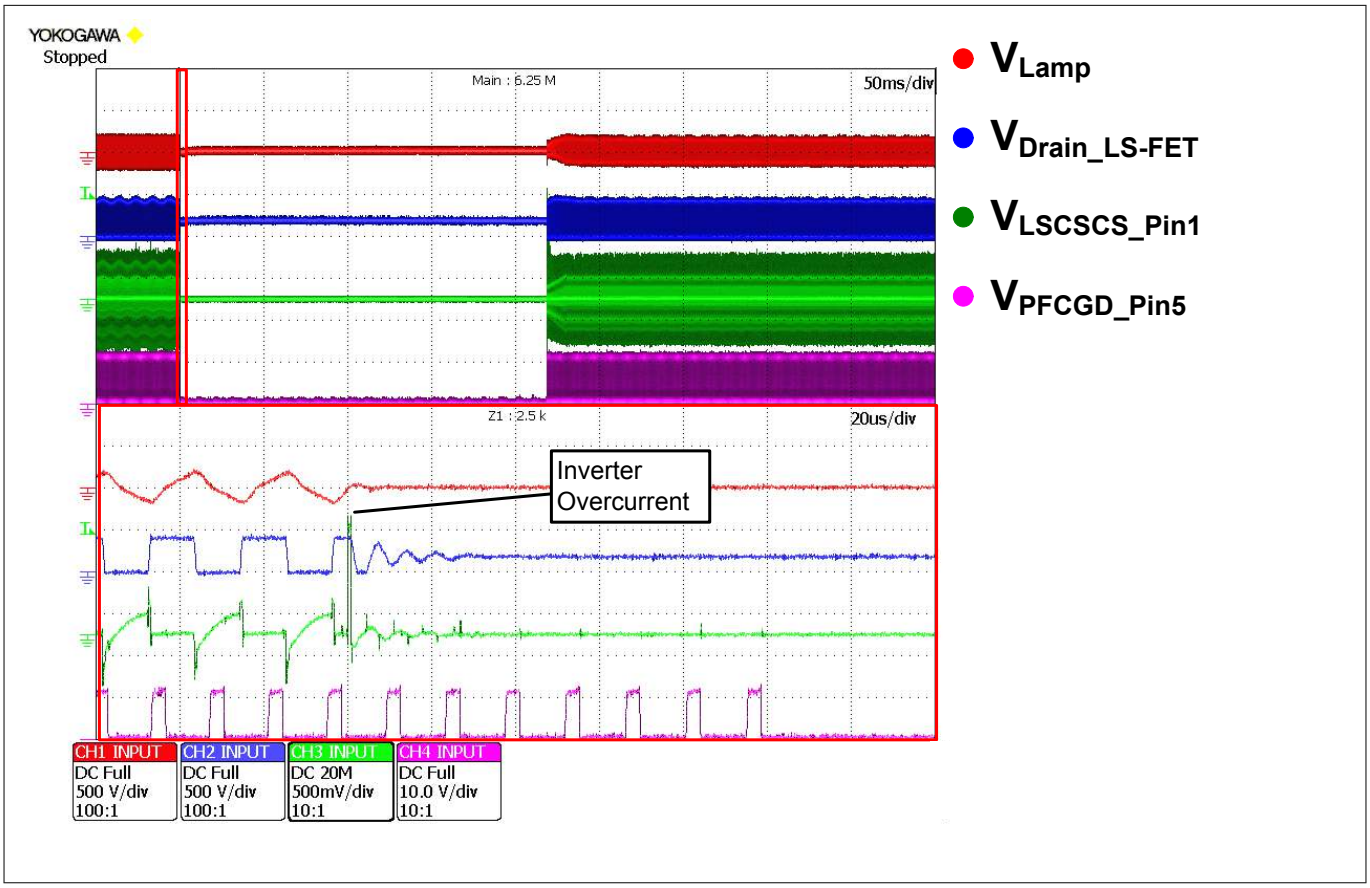



**Figure 15 Inverter Overcurrent**

***Figure 15*** shows an oscillogram with a generated inverter overcurrent. A series resistor of 1 kΩ was inserted in series with the LSCS pin for this measurement. The overcurrent signal is generated by a waveform generator and is overlaid directly at the LSCS pin via a diode.

The half-bridge (blue signal) stops immediately after detecting inverter overcurrent: Fault F. With a short delay of about 100 µs the PFCGD stops working too. This delay is caused by the digital logic. About 200 ms after turning off and incrementing the failure counter, the IC starts another start-up. If a second inverter overcurrent or another Fault F failure occurs within 40 s, the IC goes into latched fault mode.

## 6.3 PFC Overcurrent Protection

*Figure 16* shows an oscillogram of the demo board start-up. The green waveform shows the voltage at the PFCCS pin (across the PFC shunt resistor of 1 Ω). In the beginning, the PFC starts in soft start mode and with a short turn-on time. The turn-on time is increased continuously because the bus voltage is below the nominal value (red area of the oscillogram).

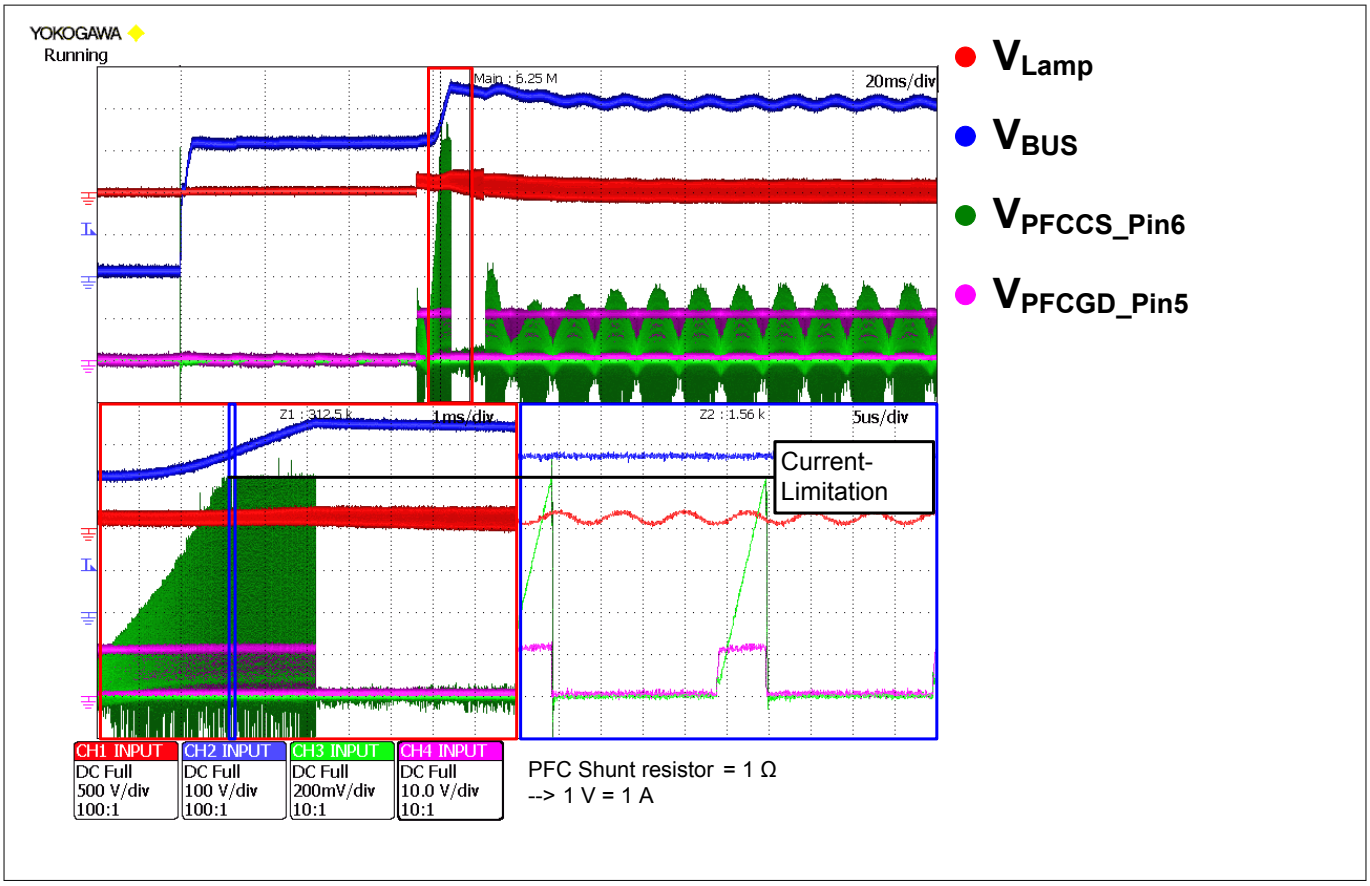



**Figure 16 PFC Overcurrent**

The current through the PFC inductor increases and after reaching the PFC overcurrent threshold of $V_{PFCCSOff}$ the PFCGD turns off cycle by cycle. This working point is shown in the blue area of the oscillogram and is not handled as an operation fault. This feature protects the PFC stage against overload.

## 6.4 Bus Overvoltage Protection 109% – 105% Threshold

Depending on the input voltage, a short bus overvoltage can occur during start-up, which is fully covered by the bus overvoltage protection. ***Figure 17*** shows an oscillogram explaining the functionality of the bus overvoltage protection. Start-up activates the inverter gate drives and the PFC gate drive with a short delay. Then the bus voltage rises and reaches the 109 % threshold. The PFC gate drive stops immediately as long as the bus voltage is above the 105 % threshold and the PFC gate drive is activated again, and the bus voltage goes to the nominal value. If the bus voltage is > 109% for longer than 625 ms, the IC goes into power-down and stops working. The IC restarts automatically without preheating when the bus voltage is below the 105 % threshold.

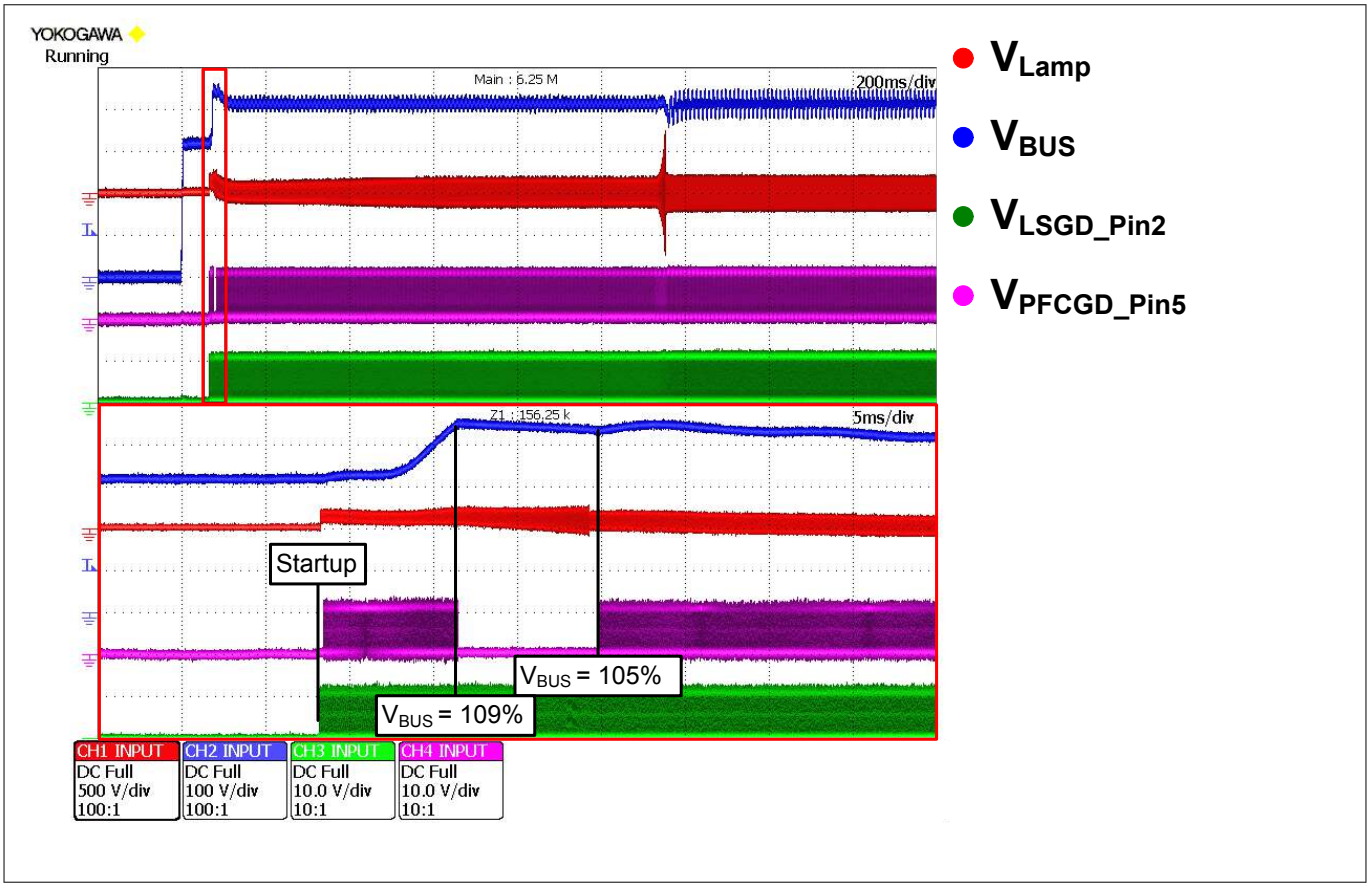



**Figure 17 Bus Overvoltage Hysteresis (Start-up)**

An additional description of the overvoltage detection in run mode can be found in ***Surge Detection***. The surge detection described there is a combined detection of bus overvoltage and inverter overcurrent during pre-run or or run mode.

## 6.5 Bus Undervoltage Protection in Run Mode with 75% Threshold

This failure protection is described in ***Emergency Detection*** because it is used for the emergency lighting feature. Bus undervoltage can also occur in other operation modes. This results in running with lower bus voltage until the IC detects this failure condition after entering run mode.

## 6.6 EOL Detection

This section gives a short introduction on how the EOL (End of Life) tests with high accuracy can be done on our demo board. More information and a description of the normative measurement can be found in EN61347-2-3 (VDE 0712-33). The names EOL1 and EOL2 are defined by Infineon Technologies AG. A lamp

overvoltage/overload is called EOL1 and the rectifier effect according to the standard is called EOL2. The standard contains also circuit descriptions that are necessary for performing the EOL tests on the ballast. An additional description on how this detection works can be found in Section 2.5 of the Data Sheet. The EOL conditions are monitored via the LVS pin. A step-by-step guide with a detailed explanation for basic calculation of the LVS network is given in ***Sample Calculation: EOL for 54W T5 Design (Excel)***. Due to some omissions in the calculations, an experimental adjustment in the circuit may be necessary.

For the following measurements the demo board was supplied with 230 $V_{DC}$ because under DC supply there is no influence of the AC ripple on the measurement. When the tests are done with an AC supply it is important that the measurement field covers at least a full input voltage half-wave and an integer multiple of it. Otherwise, due to the AC ripple, the measurement cannot be reproduced. In this case the resolution of the oscilloscope must be high enough to record all high-frequency waveforms with good accuracy.

### 6.6.1 EOL1 (Overload)

***Figure 15*** shows an oscillogram after EOL1 detection and an example of an EOL2 test setup.

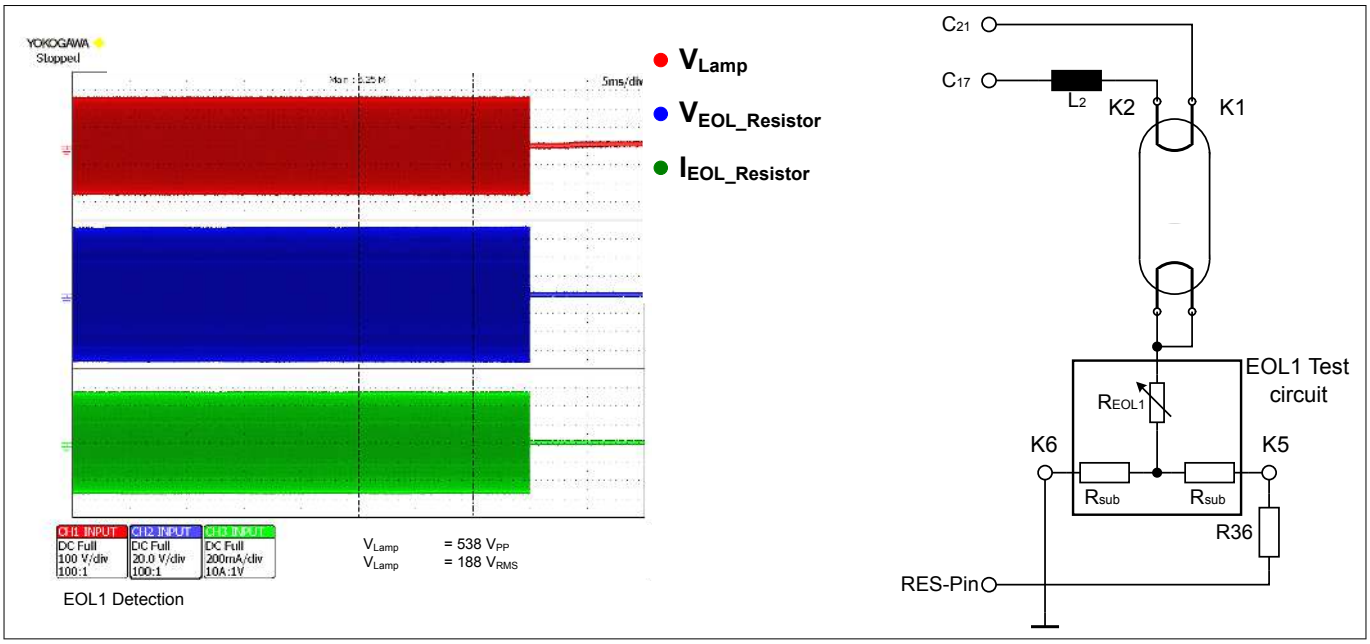



**Figure 18 EOL1 (Overload) Detection; EOL1 Test Setup**

The test was done with a series resistor to the lamp. The resistance of the series resistor was increased until the IC detected the lamp overvoltage and entered the failure analysis flow. The measured EOL1 shutdown voltage was 538 $V_{PP}$. This value matches very well with the calculated value (***Sample Calculation: EOL for 54W T5 Design (Excel)***). There is an internal counter which counts up when the EOL1 event is present and counts down when the EOL1 event is not detected. If the EOL1 threshold is not reached in every cycle, the time to turn off the IC can be longer than 620 µs.

### 6.6.2 EOL2 (Rectifier Effect)

***Figure 19*** shows an example test setup for the EOL2 test. A complete description can be found in the standard EN61347-2-3 (VDE 0712-33). When the current flows via D1, a positive rectifier effect is simulated (EOL2+). Current flowing via D2 simulates a negative rectifier effect (EOL2). The level of the positive or negative superimposed lamp voltage can be adjusted with REOL2. The higher the value of this resistor, the higher the EOL2 voltage because the resonant circuit of the demo board works like a constant current source for the lamp current.

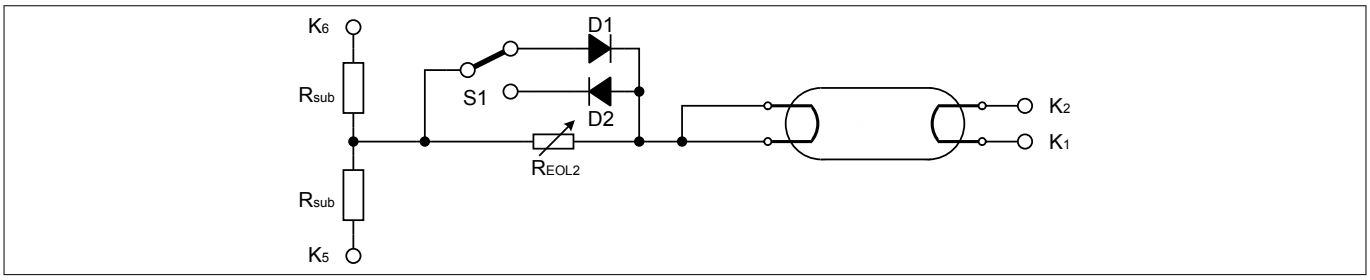



**Figure 19 EOL2 Test Setup**

This failure condition is allowed for a duration of 2.5 s until the IC goes into failure analysis flow. So for the exact measurement of the EOL2 thresholds it is important to increase the value of $R_{EOL2}$ very slowly. The EOL2 power can be calculated by multiplying the RMS values of the current through $R_{EOL2}$ and the voltage over this resistor. ***Figure 20*** shows an example of a measurement for EOL2+ (left) and EOL2 (right) detection.

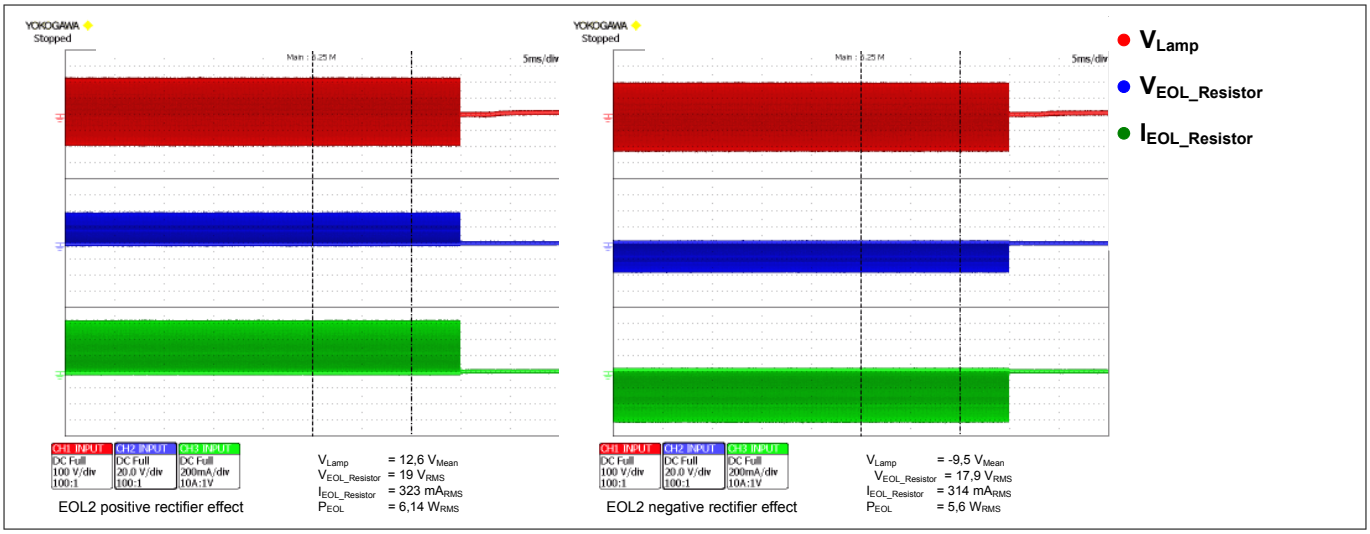



**Figure 20 EOL2 (Rectifier Effect) Detection**

The measured values for EOL2 detection are +6.1 W and -5.6 W. The calculated values from ***Sample Calculation: EOL for 54W T5 Design (Excel)*** are 5.3 W for EOL2+ and 5.3 W for EOL2, a little bit lower than the measured values. This is due to some omissions in the calculations and the influence of the voltage drop of the diode (D1 or D2 of the test circuit), which generates a higher RMS value of the voltage via the EOL2 resistor for the measured values. This means that an experimental adjustment in the circuit may be necessary. Please note that parasitic inductivity of the resistors have to be low.

The difference between the positive and negative thresholds is due to the internal IC design. There is an internal series resistor of about 5 kΩ to an internal voltage source of about 600 mV at the LVS pin (not specified in the Data Sheet). The internal signal processing of the IC generates an internal potential at the LVS pin of about 800 mV at +42 µA and about 400 mV at -42 µA. Due to these differences the positive lamp voltage shift for EOL2 must be higher than the negative to reach the EOL2 turn-off current at the LVS pin. The EOL2 power results from the lamp current multiplied by the EOL2 lamp voltage shift. Consequently, the difference between positive and negative EOL2 rises with the lamp current because the EOL2 lamp voltage shift needed for the same EOL2 power is smaller and the influence of the voltage at the LVS pin becomes higher. Figure 6-14 shows a theoretical example of this effect for a designed EOL2 power rating of 6 W.

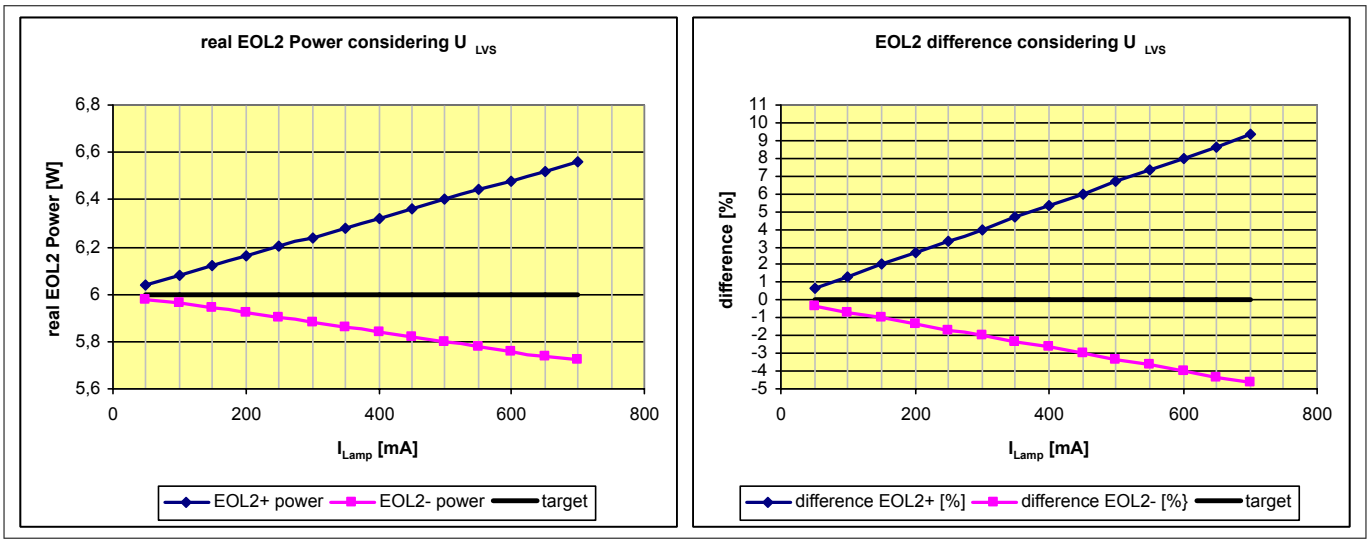



**Figure 21 EOL2 Power Difference**

When the symmetry between the positive and negative EOL2 power must be as good as possible, an additional compensation circuit can feed an additional current into the LVS pin to correct the offset/asymmetry between the positive and negative EOL2 thresholds. ***Figure 22*** shows an example of such a compensation circuit.

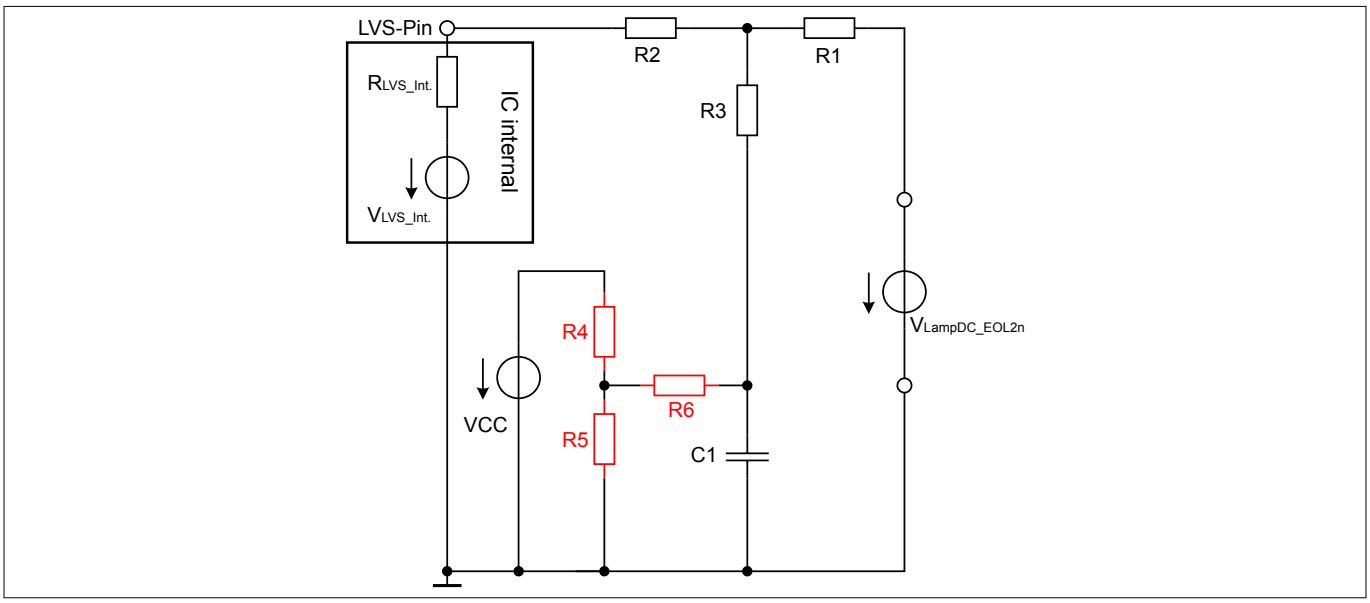



**Figure 22 Compensation Circuit for better EOL2 Symmetry @ High Lamp Currents**

The reference names of $R_1$, $R_2$, $R_3$ and $C_1$ are referenced to the small schematic in ***Figure 35*** and these components are a part of the standard BOM without compensation at the LVS pin. Only three resistors connected to the IC supply voltage are necessary (shown in red) for the compensation circuit. For this design, good matching between the positive and negative EOL2 threshold can be achieved with R4 = 2.2 MΩ, R5 = 680 kΩ and R6 = 470 kΩ. Due to the high-ohmic values of the resistors there are no high losses in this compensation circuit. Please note that this circuit can influence the filament detection via the current into the LVS pin before start-up.

### 6.6.3 Switched Rectifier Effect

***Figure 23*** shows two oscillograms of the IC behavior when the switched rectifier effect (according to EN61347-2-3; VDE 0712-33) occurs during run mode. Applying this test to the ballast leads to an EOL1 detection

because the peak lamp voltage rises to the EOL1 detection limit and the duration to turn off is much shorter than for EOL2 detection. There is an internal counter which counts up when the EOL1 event is present and counts down when the EOL1 event is not detected. If the EOL1 threshold is not reached in every cycle, the time to turn off the IC can be longer than 620 µs (e.g. the amplitude is close to the detection limits). After detecting EOL1 the IC goes into power-down mode with a typical current consumption of $I_{VCCLatch}$. In this mode, the maximum LVS current for the safe operating area is limited to max. 210 µA. Due to this failure condition the voltage at C40 in reference to GND can rise to high values and a voltage limitation at C40 might be necessary to limit the current flowing into the LVS pin.

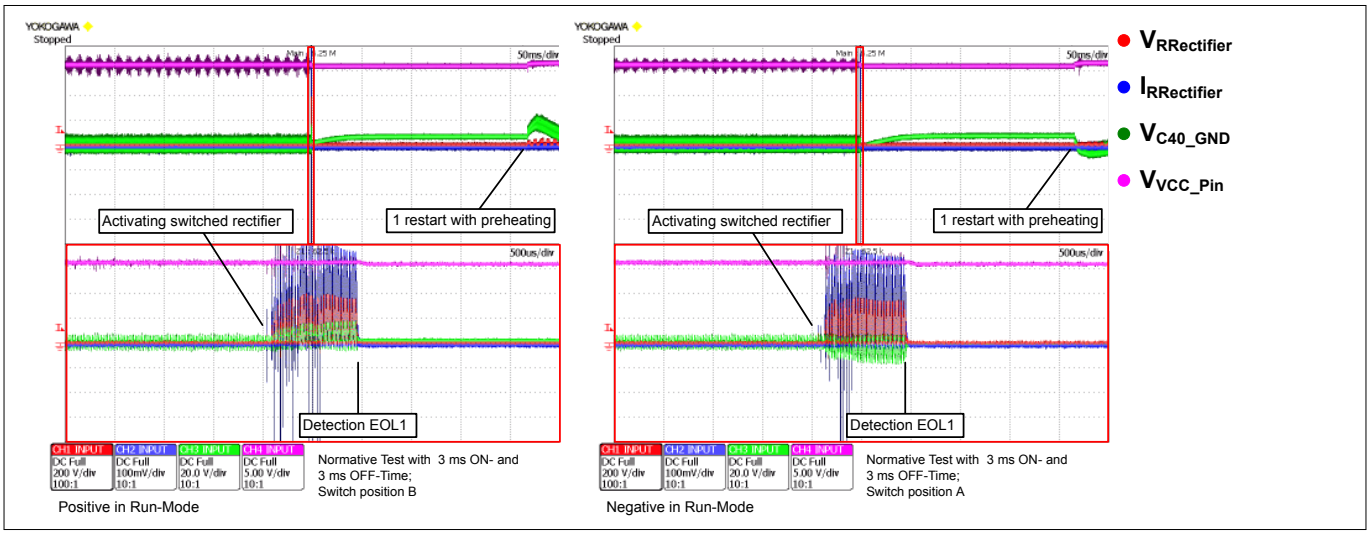



**Figure 23 Switched Rectifier Effect according to EN 61347-2-3 (VDE 0712-33)**

The left oscillogram shows the signals when the switched rectifier effect is applied in the negative direction and the right one shows the behavior for the positively switched rectifier effect.

Result: The requirements of the standard are fulfilled.

### 6.6.4 Hard Rectifier Effect

***Figure 24*** shows two oscillograms with the IC behavior when the hard rectifier effect (according to EN 61347-2-3; VDE 0712-33) occurs during run mode.

Applying this test in run mode leads to EOL1 detection due to the same reasons as explained in ***Switched Rectifier Effect***.

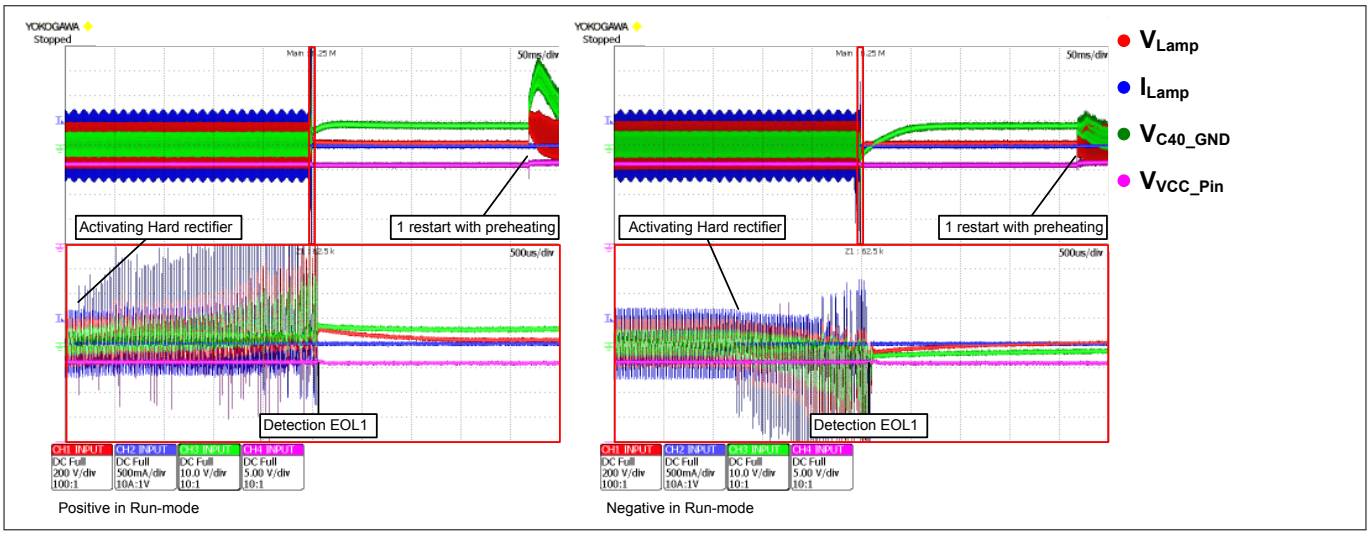



**Figure 24 Hard Rectifier Effect according to EN 61347-2-3 (VDE 0712-33)**

The left oscillogram shows the signals when the hard rectifier effect is applied in the positive direction while the oscillogram on the left side shows the hard rectifier effect when applied in the negative direction.

Result: The requirements of the standard are fulfilled.

## 6.7 Capacitive load (Cap Load)

This section is intended to give an understanding of the effects that take place when the ballast works under capacitive load conditions. To help the explanation, two oscillograms show the signals under cap load 1 and cap load 2. Further information on this can be found in the Data Sheet (Section 2.6).

### 6.7.1 Cap Load 1 (Idling Detection / Current Mode Preheating)

This protection feature is only necessary in current mode preheating topologies, where the half-bridge goes into idling operation when the lamp is disconnected during run mode. In current mode preheating designs, the resonant capacitor ($C_{20}$) is connected “behind” the lamp cathodes, so the cathodes are in series with the resonant capacitor. Removing the lamp and the cathodes results in an open load condition with direct charging and discharging of the snubber $C_{16}$ by the MOSFET, and the half-bridge switches into cap load 1 operation.

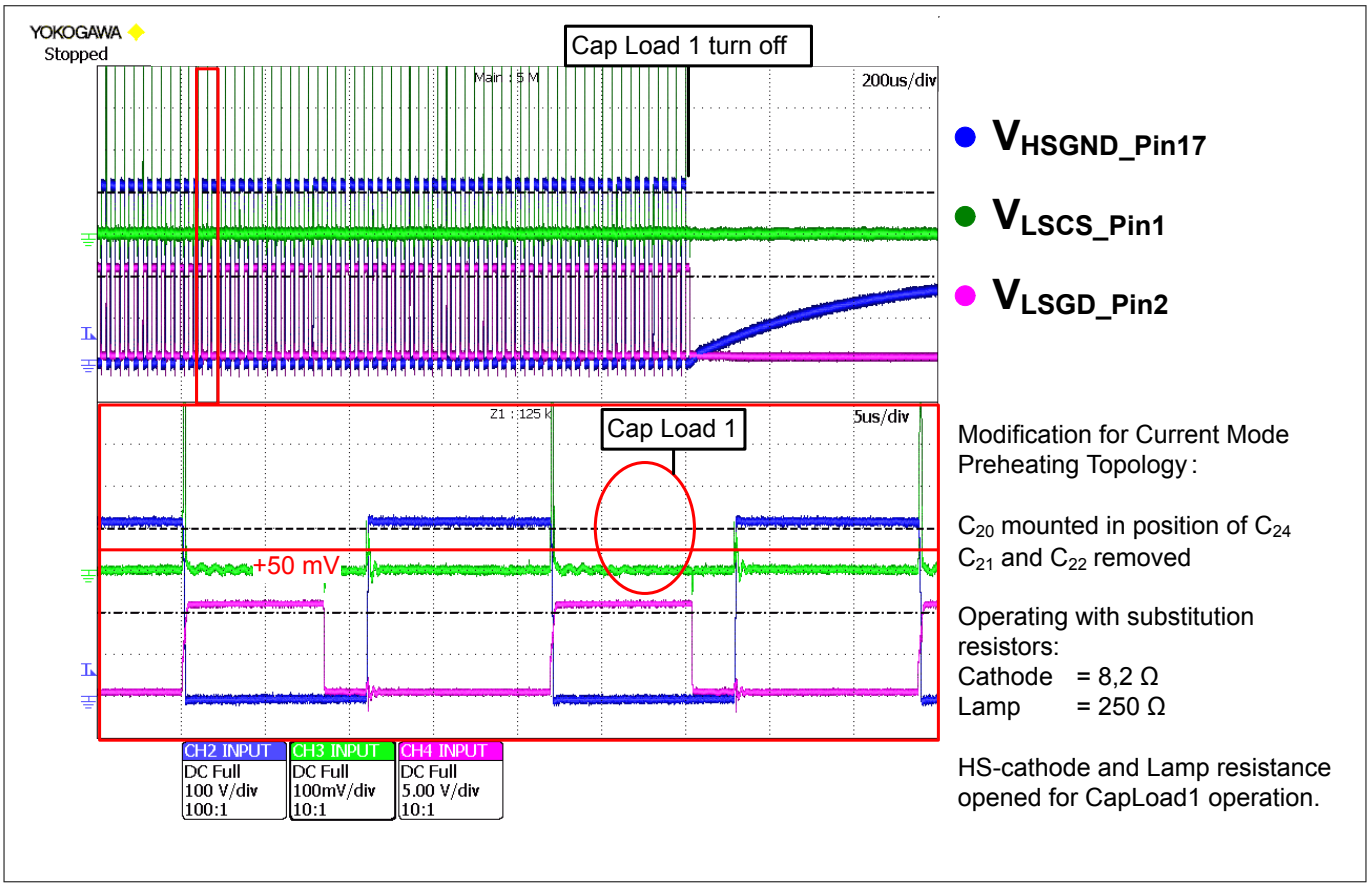



**Figure 25 Cap Load 1 Detection in Designs with Current Mode Preheating**

***Figure 25*** shows an oscillogram in cap load 1 operation with a modified demo board for current mode preheating topologies. The modification to the demo board is described beside the oscillogram. The horizontal red line indicates the $V_{LSCSCap1}$ threshold and the red circle indicates the area where the signal of the LSCS pin should reach this threshold during normal operation. Only a high current spike at the moment of turning on the LS-FET is present in this oscillogram. This leads to “Fault F” detection after about 2500 ms.

In current mode preheating designs there is a higher probability of overload detection during ignition mode. In current mode designs the voltage at the RES pin can increase to very high levels when removing the lamp during ignition and run modes. Please check ***RES Pin*** for information on how the circuit at the RES pin can be modified for this ballast topology.

### 6.7.2 Cap Load 2 (Overcurrent / Operation Below Resonance)

Cap load 2 operation can only occur in designs when the run frequency is below the resonance frequency of the unloaded resonance circuit. Cap load 2 operation is detected if the voltage at the LSCS pin is below $V_{LSCSCap3}$ for longer than $t_{LSCSCap2}$ directly before the HSGD is turned on, or if it exceeds a threshold of $V_{LSCSCap2}$ for longer than $t_{LSCSCap3}$ during on-switching of the HSGD. The duration for detecting this failure is 620 µs.

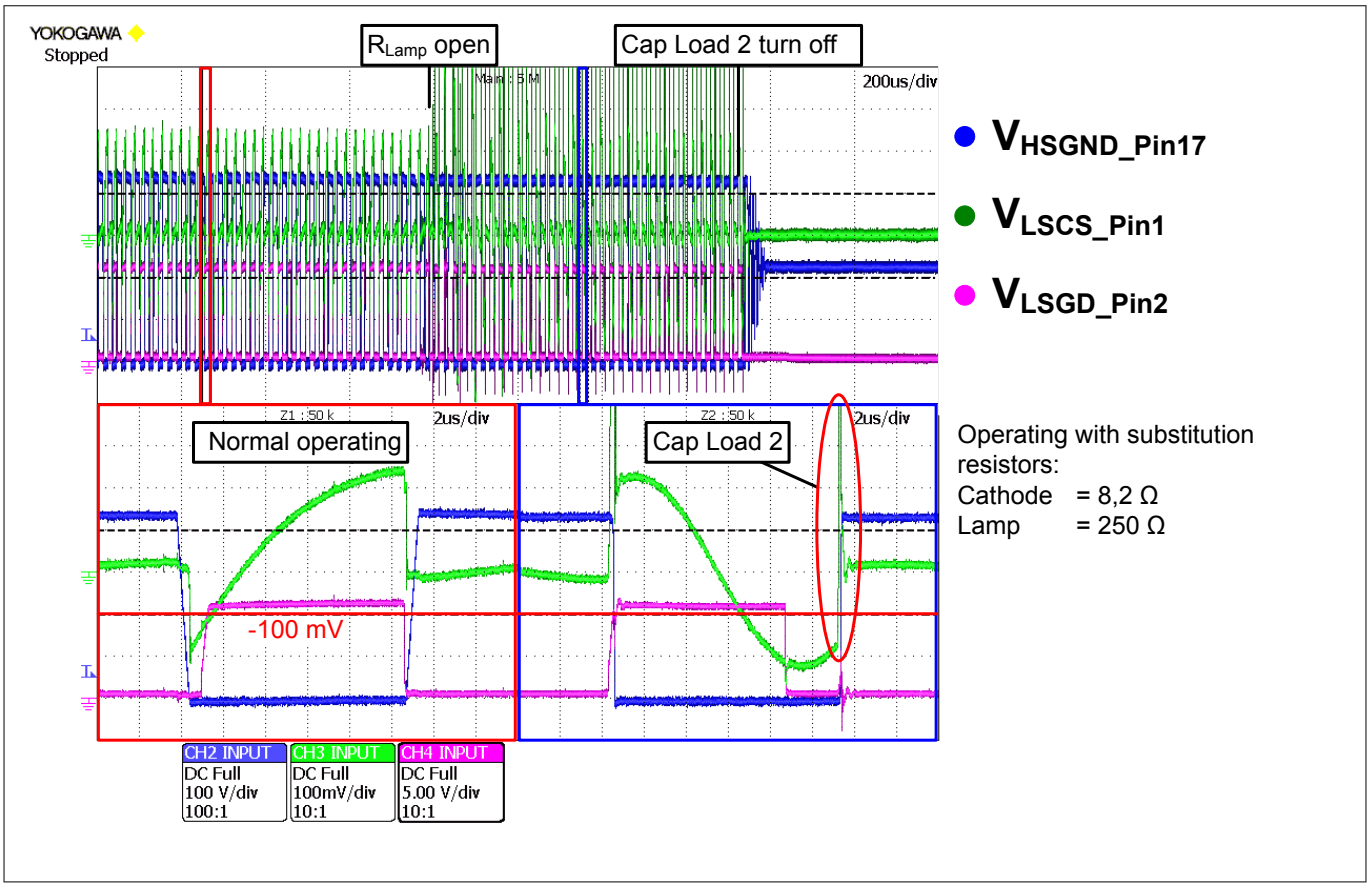



**Figure 26 Cap Load 2 Detection**

***Figure 26*** shows an oscillogram under Cap load 2 operation. The red circle shows the relevant area for detecting cap load 2.

## 6.8 Emergency Detection

The ICB2FL03G supports emergency detection requirements (according to VDE 0108). To fulfill this standard, it is necessary that the illumination returns immediately after short input voltage interruptions. The ICB2FL03G detects short interruptions of the input voltage via the LVS pin together with the value of the bus voltage, and restarts within a specific time frame directly with lamp ignition without a prior preheating phase.

Please check the advice given in ***VCC Chip Supply*** and ***LVS Pin*** on designing the ballast in such a way that correct emergency detection functionality is guaranteed. In the event of an input voltage interruption, the IC supply has to be connected to the bus voltage. ***Figure 27*** shows an oscillogram that demonstrates the functionality of this feature. The oscillogram shows the following sequences: start from connecting the input voltage to run mode followed by input voltage interruption of about 250 ms with direct lamp ignition without preheating and then an input voltage interruption of about 3 s in run mode.

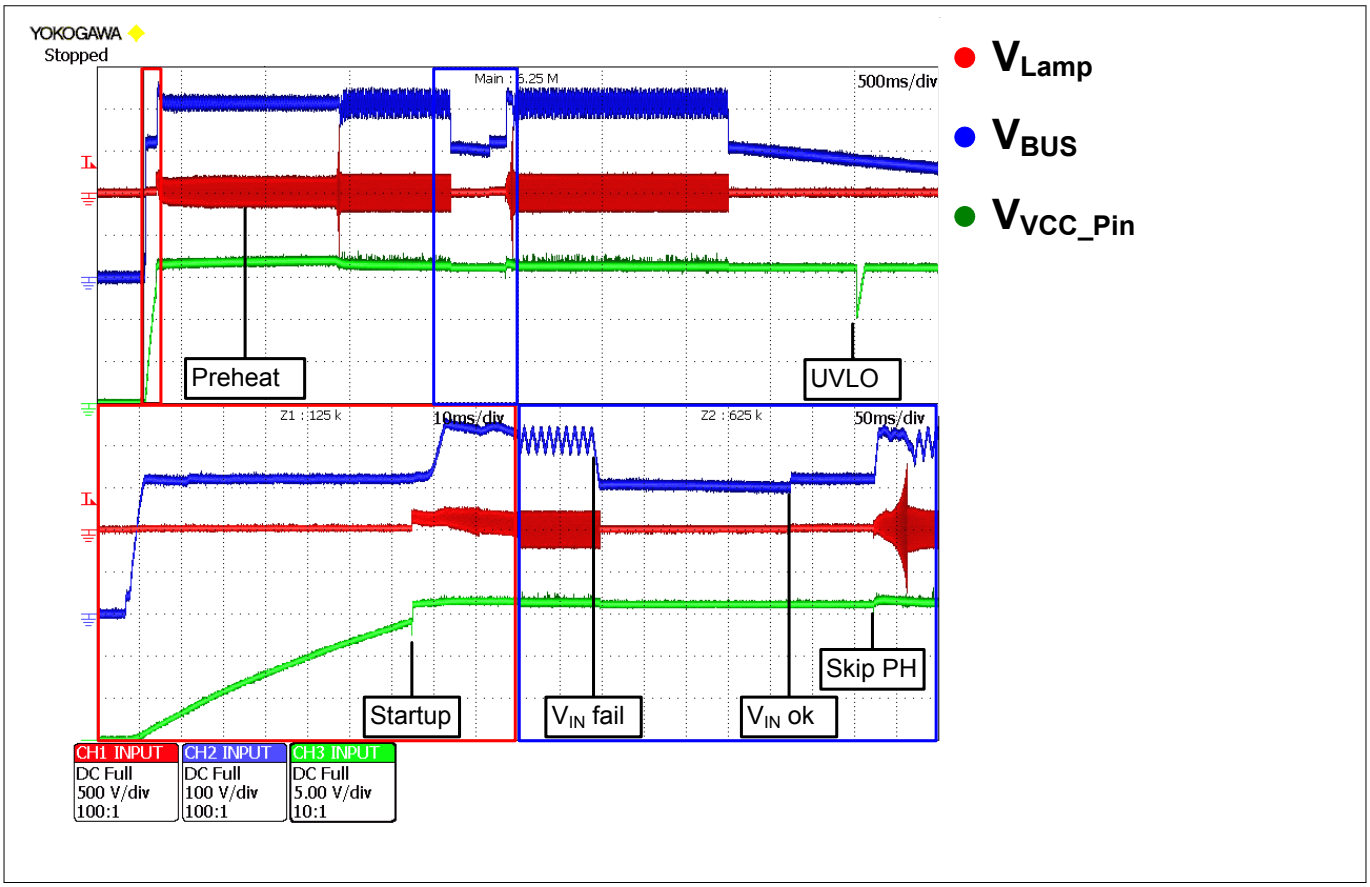



**Figure 27 Emergency Detection**

The bottom left of the oscillogram shows the phase from turning on the input voltage to the preheating phase. The bottom right of the oscillogram shows an input voltage interruption in run mode ($V_{IN}$ fail) for about 250 ms. After reaching 75 % of the rated bus voltage the IC detects bus undervoltage, sets the “skip preheating” flag and stops the inverter. The current consumption falls to a minimum value and the IC checks the presence of the cathodes 7 times in an interval of $t_{TIMER1}$. When the input voltage is present again ($V_{IN}$ ok), checked via the current to the LVS pin, and the counter skip preheating is < 7, the IC restarts without preheating. In the top right of the oscillogram there is a second interruption of the input voltage for longer than 700 ms and the IC goes into a self-generated reset (via UVLO). This resets the “skip preheating” flag and the IC will start with preheating after a new input voltage detection. For an external supply it must be ensured that the IC can perform this UVLO.

# 7 Advice for Design, Layout and Measurements

This section gives some advice on ballast design with the ICB2FL03G. It also provides some additional technical information on the IC function and advice for measurements.

## 7.1 Deactivation of Lamp Section

### 7.1.1 Deactivation of Lamp Section

For evaluation of the PFC stage without the lamp section, the lamp circuit can be easily deactivated. In a first step, the voltage level at the LSCS pin must be higher than $V_{LSCSCap1}$ to prevent detection of cap load 1. A voltage divider from VCC with a level of about 200 mV at the LSCS pin is the easiest way for realizing this. Without the lamp section, the VCC supply cannot be realized via the charge pump, so an external supply is necessary (please note the information in the Data Sheet, Section 3.3, for restrictions at the external supply). The LVS and RES pins can be directly connected to GND to deactivate the lamp protection functions. With these modifications, the pins and assembly around HSGD, HSVCC, HSGND and LSGD can remain unconnected for full PFC functionality without a lamp section.

## 7.2 Deactivation of the PFC Section

For evaluation of the lamp circuit without the PFC stage, the PFC stage can be easily deactivated. To prevent any failure detection of the deactivated PFC section, a voltage level at the PFCVS pin of between $V_{PFCVS95}$ and $V_{PFCVSLOW}$ is necessary. If the voltage at PFCVS is < $V_{PFCVS95}$, the IC restarts 80 ms after activation of the halfbridge and the PFCGD. A level > $V_{PFCVSLOW}$ prevents the IC going into startup and no pulse out of the gate drives is visible. The easiest way is to set this voltage with an external DC supply or a combination of Z-diode, resistor and voltage divider connected to the VCC voltage of the IC. With this modification, the pins and assembly around AUX, PFCZCD PFCGD and PFCCS can remain unconnected for full inverter functionality without a PFC section. If the voltage at PFCCS is between $V_{PFCCSOff}$ and $V_{PFCCS\_max}$ (6 V), the PFCGD is inactive and there is no EMI influence of this gate drive.

## 7.3 RFPH pin (Preheating Frequency)

The resistor at the RFPH pin sets the preheating frequency. This pin is also very helpful for evaluating the device because the voltage level indicates the status of the digital logic during preheating phase. ***Figure 28*** shows an oscillogram for a description of the signals at this pin. The voltage at this pin was filtered by a 16 kHz low-pass filter in the oscilloscope. This can be done because there is no interest in fast signal changes. During the soft start phase the voltage at the RFPH pin rises to 2.5 V in 16 steps and the inverter frequency is reduced from $f_{StartUp}$ down to the adjusted preheating frequency. Reaching a level of 2.5 V indicates entry into the preheating phase. The logic stays in this phase for the time adjusted by the resistance at the RTPH pin. On reaching the end of the preheating time, the logic enters the ignition phase and the voltage at the RFPH pin begins decreasing down to the GND potential in 127 steps within 40 ms while at the same time reducing the inverter frequency down to the run frequency adjusted by the resistance at the RFRUN pin. Decreasing stops when the ignition control becomes active and goes on when the lamp ignites.

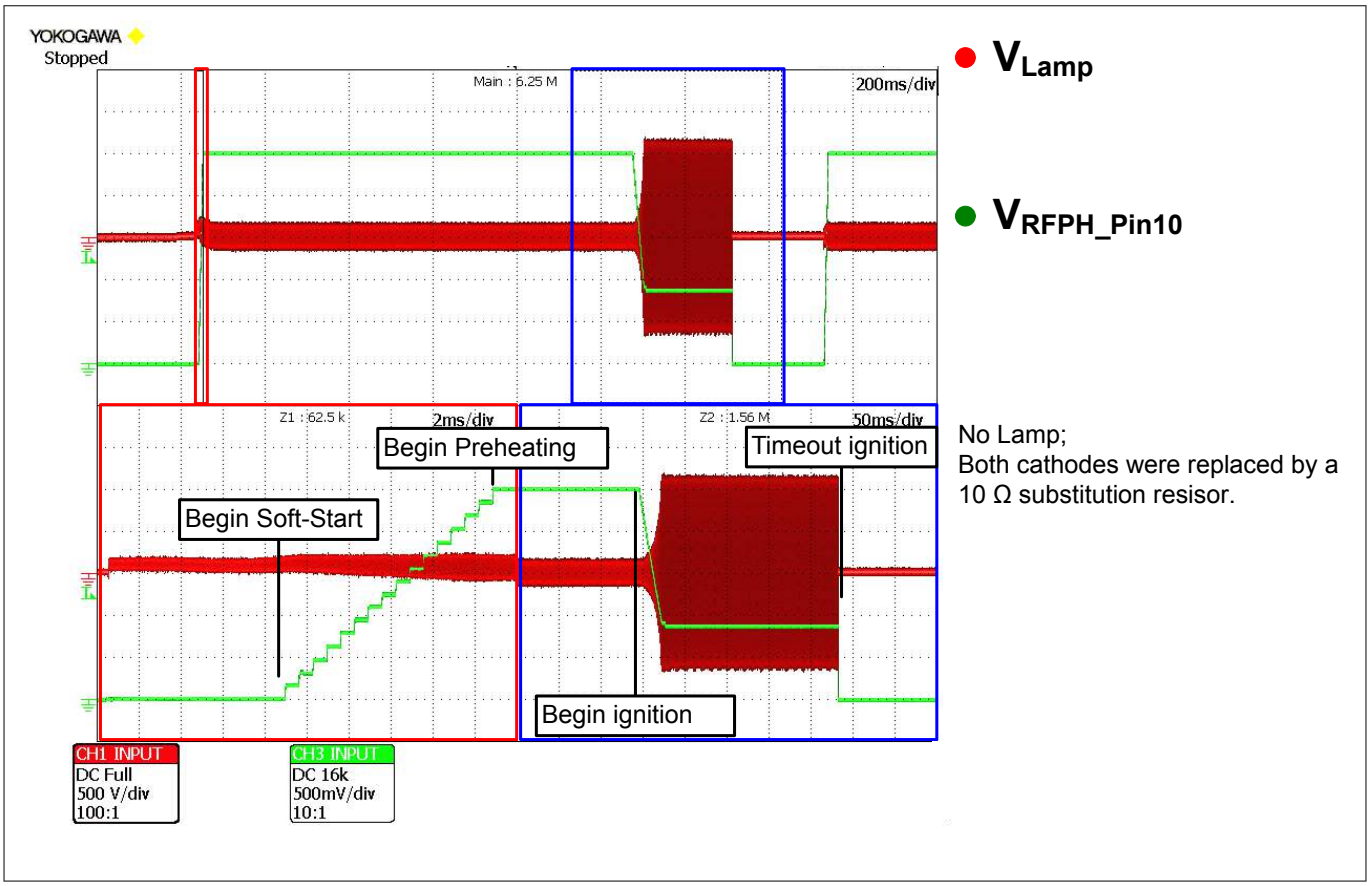



**Figure 28 Status at the RFPH Pin**

This measurement was done only with cathode substitution resistors and no ignition is possible. In this case the logic detects ignition time-out after $t_{NOIgnition}$ and generates a single restart after 200 ms.

## 7.4 RTPH Pin (Preheating Time)

The preheating time can be adjusted with a resistor between 0 Ω and 25 kΩ (equivalent to a preheating time of 0 to 2.5 s) at the RTPH pin. The voltage at this pin is also linear to the resistance at the RTPH pin (0 – 2.5 V). The preheating time $t_{RTPH}$ is divided into 127 counter steps, each with a duration of about 20 ms and an equivalent voltage step at the RTPH pin of about 20 mV. Depending on the voltage at the RTPH pin, the preheating time can fluctuate up to 20 ms when the voltage at this pin is close to these voltage steps.

## 7.5 PFCVS Pin

This pin senses the bus voltage and has protection against open loop protection if the bus voltage falls below 12.5 % of the rated level. This protection function can also be used for switching the IC off and on with a microcontroller. When using this pin for IC shutdown it is important that the voltage drops very quickly below a level of 12.5 % to prevent the PFC regulation from increasing the bus voltage to higher levels for compensation. A level higher than 12.5 % leads to a new IC startup without preheating for a restart time < $t_{TIMER1}$ and with preheating if the turn-off phase is longer than $t_{TIMER1}$.

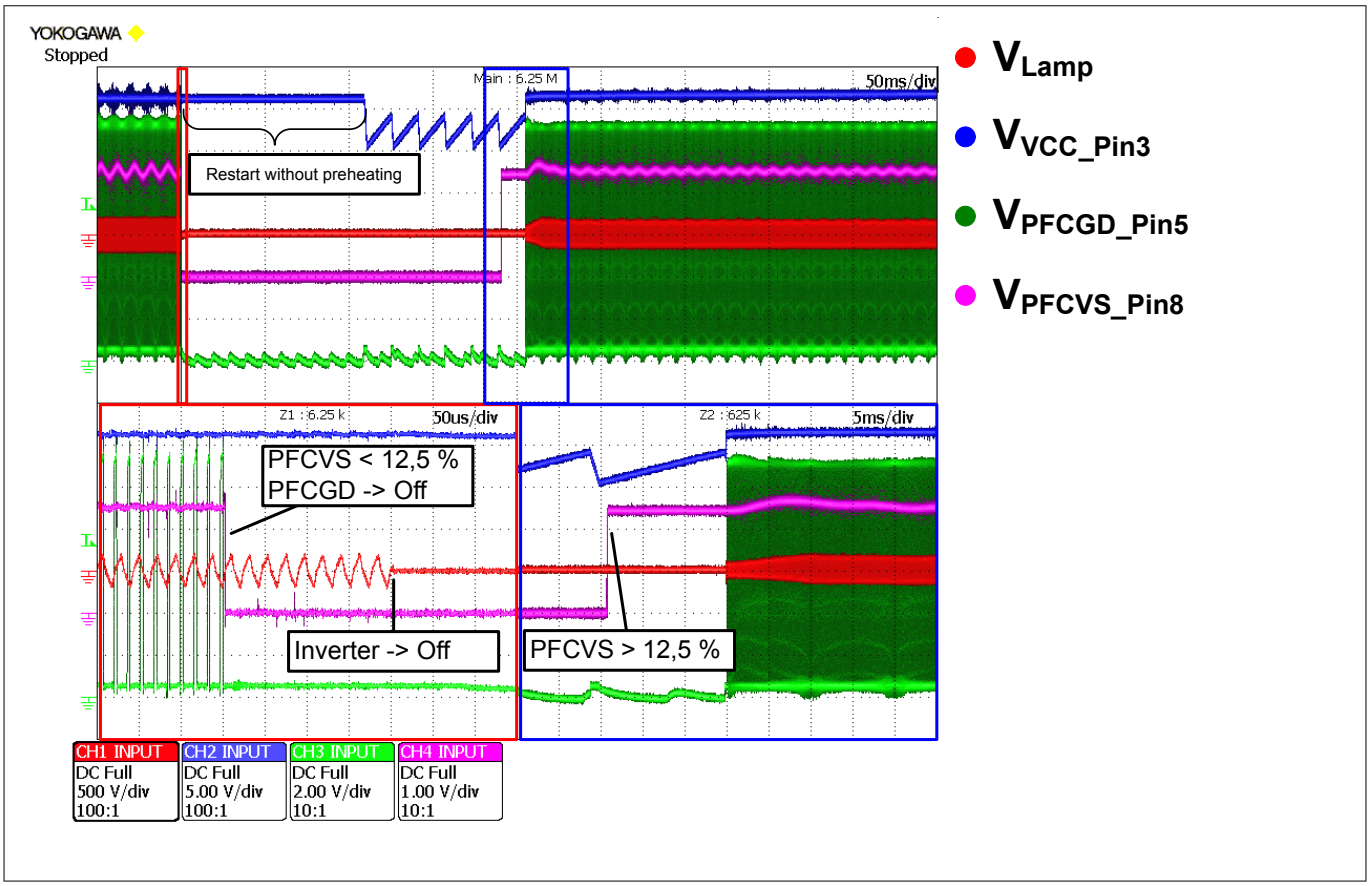



**Figure 29 IC Turn-Off and Turn-On via the PFCVS Pin**

***Figure 29*** shows an example of a measurement to explain the logic flow in the case of turning off the ballast via the PFCVS pin. The PFCGD stops working directly after switching the PFCVS signal to a level < 12.5 %. With a delay of about 200 µs the inverter stops working too because of reaching the 75 % threshold for bus voltage and the IC detects “Fault U – bus undervoltage” (see Section 3.3 of the Data Sheet). Within a time of $t_{TIMER1}$ the IC restarts without preheating when the level at the PFCVS pin is > 12.5 %. After this time the IC goes into power-up because the lamp detection is ok and VCC is > $V_{VCCOn}$. This results in a current consumption of $_{IVCCSupply}$ and, due to the level < 12.5 % at the PFCVS pin, the gate drives remain off. This combination generates a UVLO (resets the whole IC) followed by monitoring and a new power-up. This flow continues until the voltage at the PFCVS pin becomes > 12.5 % again and the IC restarts with preheating.

This method of turning off the IC is only suitable when the IC is in run mode because in other modes the 75 % threshold for the bus voltage is not active. A turn-off signal in phases out of the run mode leads to operation of the IC without a PFC section and to a resulting lower BUS voltage with a higher ripple until the run mode is reached. Then the ballast turns off when activating the 75 % threshold after the pre-run phase.

It is important that the time constant at the PFCVS pin (generated by the voltage divider and $C_{11}$) is small enough that the voltage reaches the 109 % threshold quickly enough during surge conditions, otherwise the surge condition cannot be clearly detected.

## 7.6 RES Pin

This pin is needed for filament detection and can be disabled by setting it to GND. When the voltage at this pin rises higher than $V_{RES3}$ the IC detects an open filament, handled as “Fault F”. This protection function can also be used for switching the IC off and on with a microcontroller. This implementation only works in run mode, and the minimum duration of turn-off should be 400 ms for correct functionality.

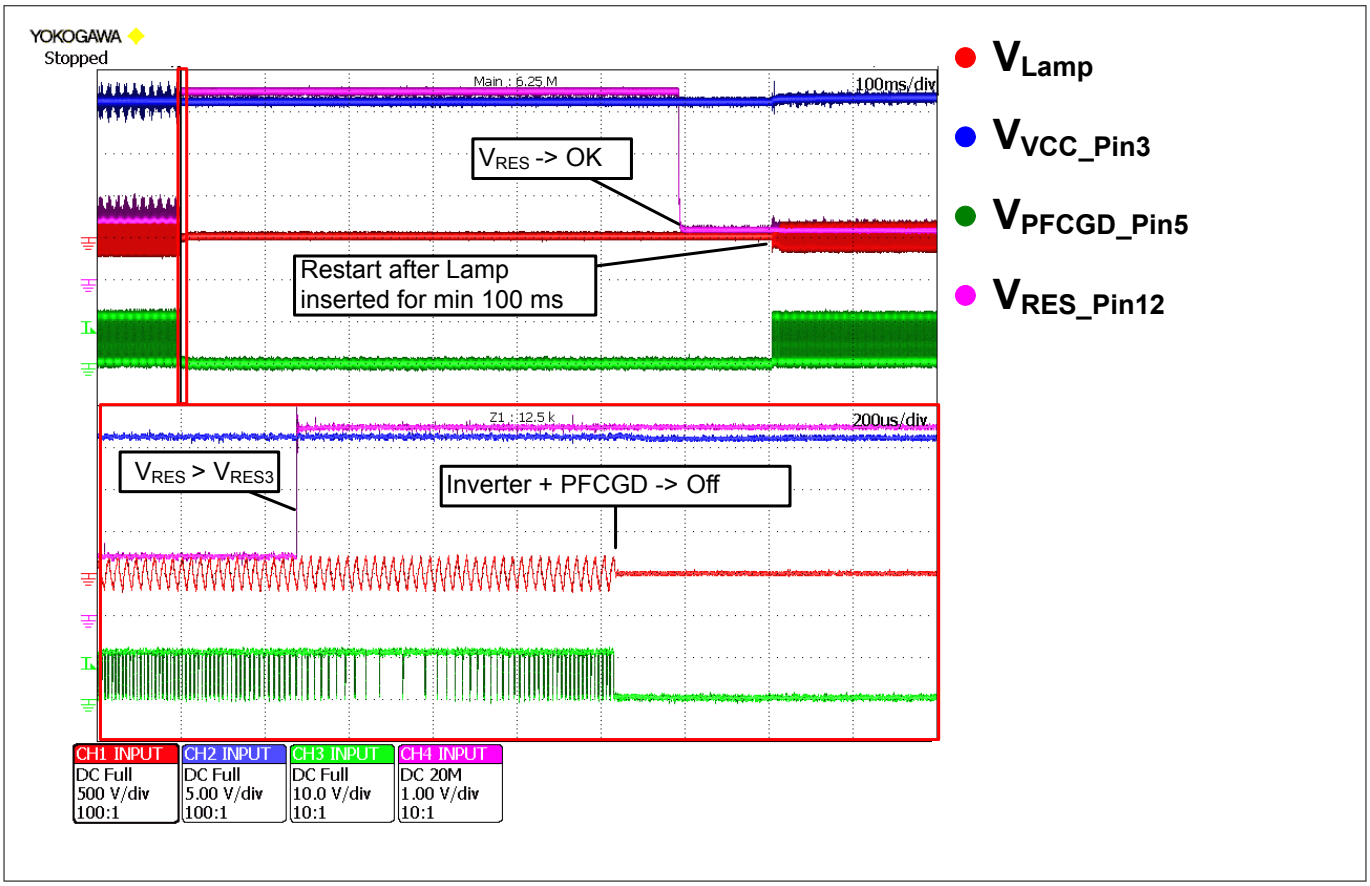



**Figure 30 IC Turn-Off and Turn-On via the RES Pin**

***Figure 30*** shows an example of a measurement to explain the logic flow in the case of turning off the ballast via the RES pin. About 700 µs after reaching a level > $V_{RES3}$ at the RES pin, the IC detects “Fault F” and the inverter and the PFC stop working. The “Fault Counter” increments by 1 and after a first delay of about 200 ms a decision according to the “Fault Counter” has to be taken. This is the reason for the minimal duration of the turn-off time in this solution. If the “Fault Counter” > 2, for example after a second turn of within 40 s, the logic waits for lamp removal ($V_{RES}$ > $V_{RES3}$) of min. 100 ms until a restart can happen. If the voltage at the RES pin falls to a level within the area for correct lamp detection, the IC cannot start because the lamp has not been removed for longer than 100 ms. So an additional turn-off signal with a minimum turn-off time of 100 ms is necessary for restarting the ballast. This can be avoided with the minimum turn-off time of 400 ms mentioned before.

The IC starts with a delay of about 100 ms after reaching the filament detection level at the RES pin.

## 7.7 VCC Pin

The ICB2FL03G is very robust against EMI and shows best functionality also under high EMI influence. A ceramic capacitor with a capacity of several 10 nF (10 nF or 47 nF) is recommended to cover the load jumps for gate driver operation. The signals at this pin are very suitable for evaluating and distinguishing the states in the state diagram (see Data Sheet Sections 3.2 and 3.3).

If there are extremely high spikes at the VCC pin it might be necessary to modify the capacitance at this pin in order to improve EMI stability. EMI problems via VCC can be evaluated very easily. To evaluate this situation, the signal at the VCC pin and a signal of the half-bridge (for example HSGND) are necessary. If the half-bridge stops working and immediately after this the voltage at the VCC pin breaks down to $V_{VCCOff}$ followed by a restart after reaching the $V_{VCCON}$ threshold, an EMI problem at the VCC pin can be the reason. All failures covered by the protection functions of the IC which lead to a restart have a minimum duration of $t_{TIMER1}$ until a new restart can be achieved.

For correct emergency functionality it is necessary that the IC supply via the startup resistors is connected to the bus voltage and is designed in such a way that the supply current in latched fault mode is guaranteed (please see also ***VCC Chip Supply*** in this document for further information).

## 7.8 LVS Pin

The LVS pin is necessary for high-side filament detection before startup and for EOL detection in run mode. This function can be disabled by connecting the LVS pin to GND. This connection should be as short as possible to prevent unintentional reactivation. Reactivation of the deactivated LVS pin is possible when the voltage at the LVS pin reaches a level of $V_{LVSEnable1}$ for a typical duration of 1 µs (not specified in the Data Sheet).

## 7.9 LSCS Pin

For correct working of the adaptive deadtime, the –50 mV threshold must be achieved in all working points (for min. $t_{LSCSCap3}$), otherwise the adaptive deadtime cannot be detected properly and wobbling of the deadtime will be the consequence. Also the +50 mV threshold must be reached in normal operation to prevent cap load 1 detection.

For some dimming applications it can happen that the +50 mV threshold for cap load 1 detection cannot be reached at low dimming levels. Infineon Technologies AG provides a special IC (ICB2FL02G) with deactivated cap load 1 detection to cover all dimming solutions (please contact Infineon Technologies AG for further information or visit ***http://www.infineon.com/smartlighting***).

The maximum voltage level at this pin should not be limited below 1.6 V because half-bridge shootthrough detection and correction is realized at the LSCS pin.

## 7.10 Advice for Board Layout

For greater robustness while evaluating the board, high ohmic resistors (for example 18 kΩ) from the MOSFET gate to FET source are suggested to prevent destruction of the components if there is a broken gate resistor or broken conductor path on the PCB.

***Figure 31*** shows a simplified circuit diagram with the power path shown in bold. This figure helps to differentiate between the signal and power GND. The blue path is the signal GND, to which the resistors for sensing voltages or adjusting IC parameters should be connected. Wires where high current is flowing should be connected to the GND potential shown by the heavy lines. If possible, connect all signal GND lines radiating to the IC GND and all power GND lines radiating to the electrolytic condensator GND.

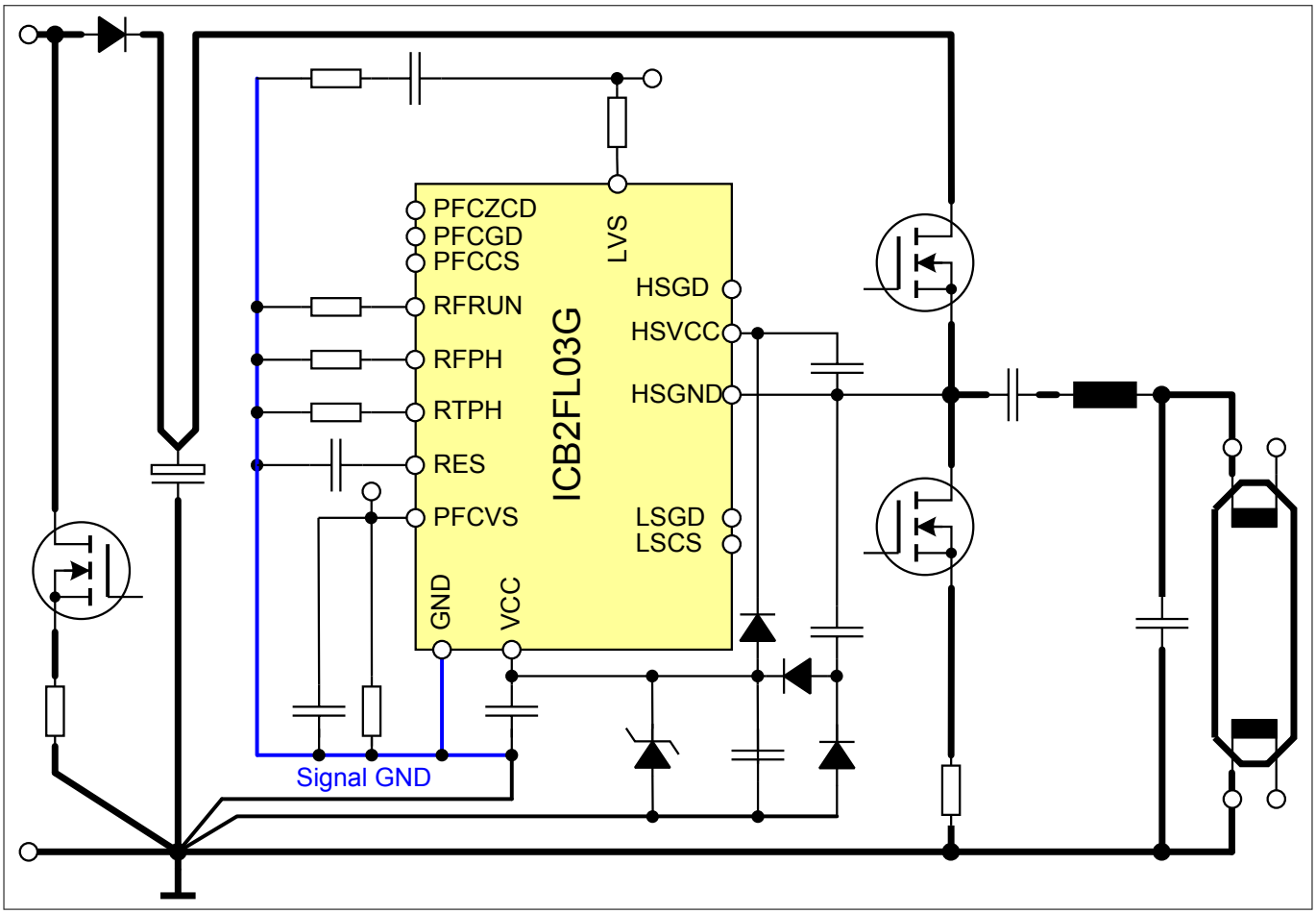



**Figure 31 Simplified Diagram of GND Flow**

The demo board provides a good example of an effective layout for this circuit.

# 8 Annex

## 8.1 Built-In Customer Test Mode

The Built-In Customer Test Mode is implemented to reduce time for the ballast end test dramatically. More information on this test can be found in Chapter 2.8.3 of the Data Sheet. The requested signal levels and the timing diagram for activating the test mode can also be found there. The following three figures show the benefit of testing time with the accelerated clock. The left oscillograms show the normal sequence without acceleration while the right oscillograms show the accelerated sequences. Additional acceleration can be realized by reducing the preheating time via $R_{23}$ temporally for the ballast end test. A UVLO at VCC resets the test mode acceleration.

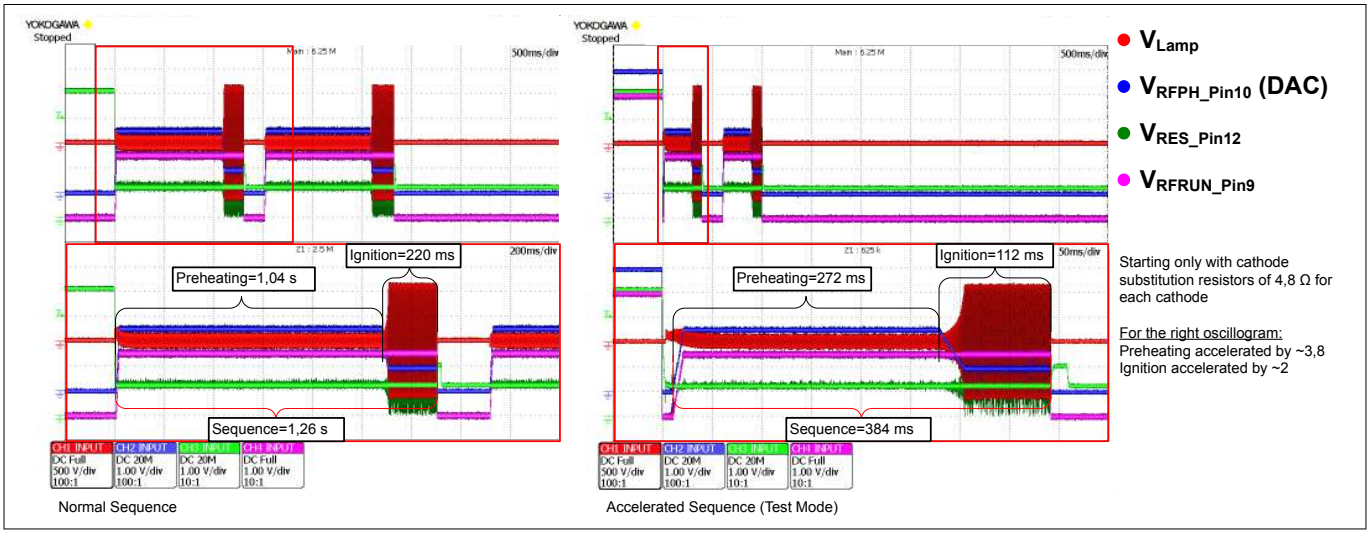



**Figure 32 Built-In Customer Test Mode – Acceleration Preheating & Ignition**

***Figure 32*** shows a comparison between the preheating and ignition phases. Acceleration of about a factor 4 for the preheating phase and of about a factor 2 for the time until time-out ignition can be seen in these oscillograms.

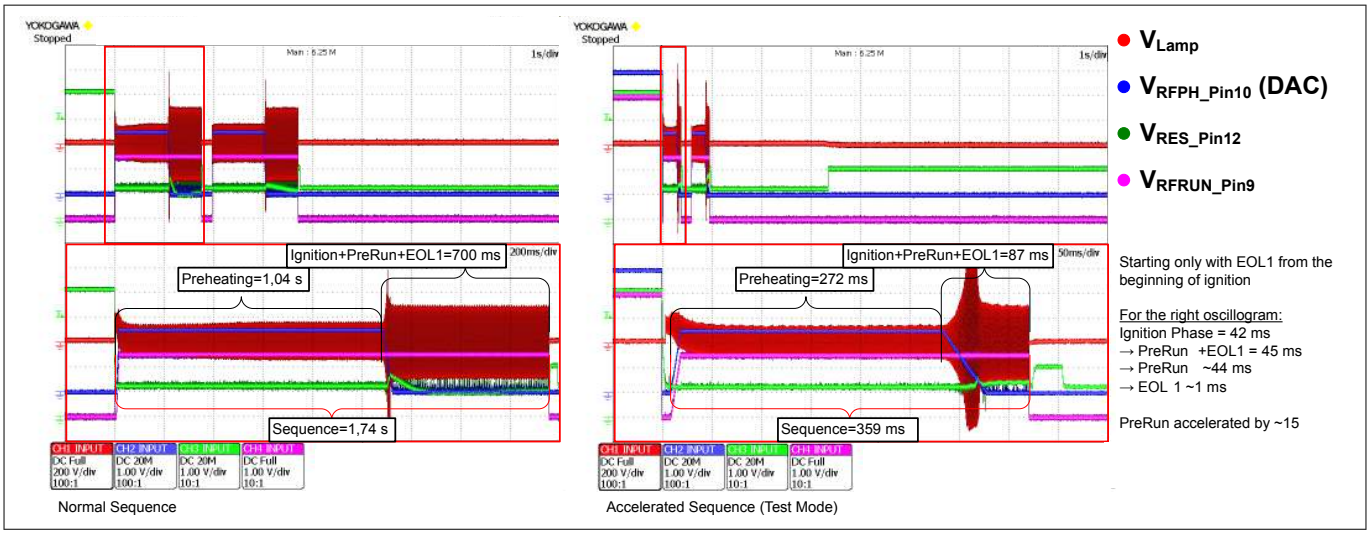



**Figure 33 Built-In Customer Test Mode – Acceleration Pre-Run**

***Figure 33*** shows acceleration of about a factor 15 for the pre-run phase. The minimum duration of the ignition phase is 42 ms for this IC. This time must be subtracted from the time of ignition+pre-run+EOL1 because it is not

affected by the acceleration. EOL1 has a duration of 620 µs and also has to be subtracted before calculating the acceleration of the pre-run phase.

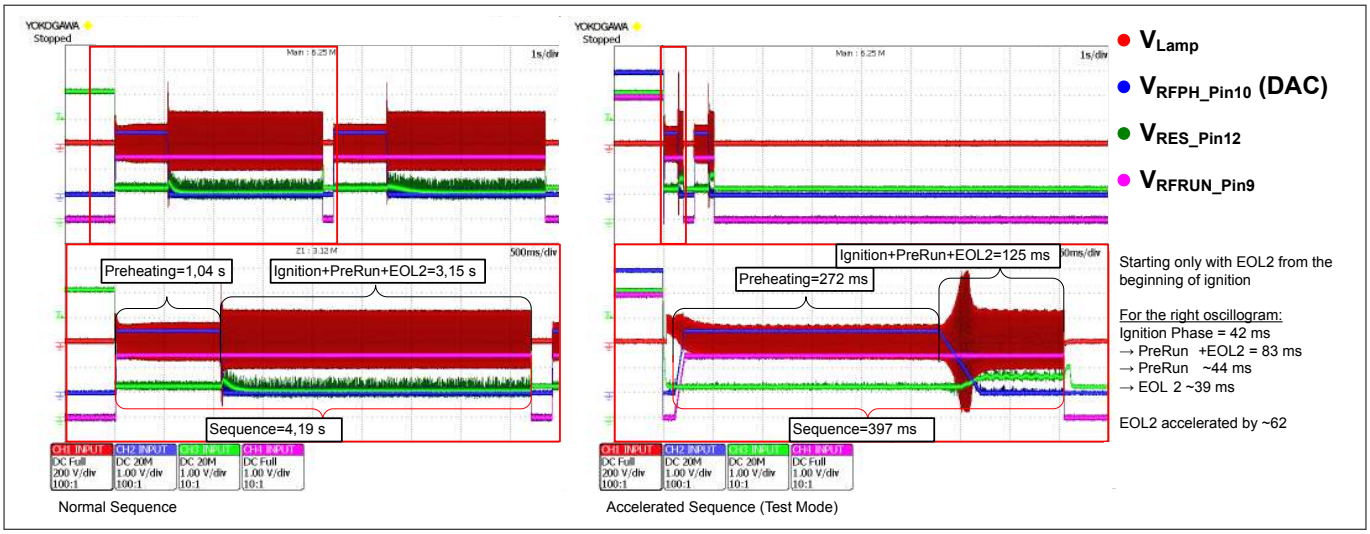



**Figure 34 Built-In Customer Test Mode – Acceleration EOL2**

***Figure 34*** shows the acceleration of about 62 for the time until EOL2 detection. With values of about 700 ms and 86 ms for the ignition and pre-run phases, the measurement in ***Figure 33*** shows that a normal time of 2450 ms for detecting EOL2 can be calculated. The accelerated time for EOL2 detection is about 39 ms.

## 8.2 Calculations

The following section describes some necessary calculations for the demo board design (according to the design used for this Application Note 1 x 54 W T5 with voltage mode preheating).

### 8.2.1 Sample Calculation: EOL for 54W T5 Design (Excel)

***Figure 35*** shows a picture of the “EOL calculation Excel sheet” that supports the design of the EOL network. Contact us at ***http://www.infineon.com/smartlighting*** to obtain the tool.

A step-by-step guide for using this Excel sheet is given in this section. Design-relevant data can be entered in the green fields and the orange-colored fields indicate that the value will be calculated via implemented formulas. Due to some omissions in the calculations an experimental adjustment in the circuit may be necessary.

A description of the planned design data can be entered in the first green field at the top of the page. After this, the nominal values for lamp voltage and lamp current can be entered in the parameter section. Also necessary are the inputs for operation frequency, max. allowed EOL power and the factor for the allowed lamp voltage. After entering these values, the peak-peak lamp voltage for EOL1 and the DC offset of the lamp voltage for EOL2 can be calculated with the currents from the Data Sheet for the EOL1 and EOL2 detection thresholds.

The EOL2 resistors $R_1$ and $R_2$ can be calculated with negligence of the influence of $C_1$ and $R_3$ because $C_1$ blocks the DC current in a steady state (run mode). The ratio between $R_2$ and $R_1$ has an influence on the necessary voltage strength of $C_1$. For major designs a resistance of about 50 kΩ to 70 kΩ for $R_2$ is suitable, so a selection of $R_1$ values regarding this resistance is helpful. It can also be helpful to separate the resistance for $R_1$ into several resistors (in this example 3 x 68 kΩ). This segmenting reduces the voltage drop for each separated resistor of $R_1$. The selected values for $R_1$ and $R_2$ can be entered in the two green fields.

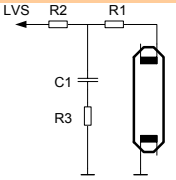
The first field in the EOL1 calculation area calculates the actual max. lamp voltage for EOL1 detection without $C_1$ and $R_3$. This value must be lower than the voltage calculated in the parameter section in the first steps. If this condition is true, $R_3$ and $C_1$ are necessary for reducing the amplitude of the AC current to the LVS pin (indication in the result field). The following calculations are necessary for dimensioning these two components; the

influence of $C_1$ for $R_3$ calculation will be neglected. The voltage across $R_2$ is calculated with the nominal EOL1 detection current ($I_{LVSSourceAC}$) multiplied by the calculated value of $R_2$. The voltage across $R_1$ is the difference between the max. allowed peak-peak lamp voltage ($U_{Lamp\_pp}$) and the voltage across $R_2$ ($U_{R2pp}$). This voltage drop results in a current through $R_1$ ($I_{R1pp}$) that is higher than the threshold for EOL1 detection of $I_{LVSSourceSC}$. This current difference ($I_{R3pp}$) must be fed via $C_1$ and $R_3$ to GND. The field “$R_3$ calculated” shows the calculated value for the needed resistance. If the selected value for $R_3$ is higher, the EOL1 detection reacts earlier and if the selected value for $R_3$ is smaller, the EOL1 detection is triggered at a higher lamp voltage than defined in the parameter section. To reduce the influence of $C_1$ on the EOL1 threshold, the capacitance should be as high as possible and in no case smaller than the calculated value $C_{1\_min}$. After entering the selected value for $C_1$ in the green field, the values for the resistors and the capacitor in the EOL detection network for this design will be summarized at the top of the page.

**For internal use only!**

Date: 18.02.2009
Version: 1.0
FL2-1_Demo_1x54W_T5_VM_180AC-270AC_090223.xls

## EOL: Demoboard 1x54W T5 - VM - 180VAC to 270VAC - ICB2FL03G




This sheet supports designing the EOL circuit with the FL-Controller ICB2FL03G.
Please fill out the green fields top down. The result is listed in the next line.
The design is: R1=204kΩ, R2=68kΩ, R3=6,8kΩ and C1=100nF.
Please note, that it can be necessary to split R1 because of the limited power dissipation.
In this Design the calculated EOL2 Power is about 5,3W+/5,3W- and the calculated EOL1 threshold is about 486Vpp.

| Parameter | short | comment | calculation | unit | Values |
|---|---|---|---|---|---|
| Lamp voltage (Lamp data) | $U_{Lamp}$[RMS] | | | $V_{RMS}$ | 118,00 |
| Lamp current (Lamp data) | $I_{Lamp}$[RMS] | | | $mA_{RMS}$ | 460,00 |
| Operation frequency | $f_{RUN}$ | | | kHz | 45,00 |
| max. allowed EOL Power (DC) | $P_{EOLDC\_max}$ | | | W | 5,00 |
| Factor for allowed Lamp Voltage | $U_{Lamp\_Fact}$ | | | | 1,50 |
| EOL1 threshold (Overvolage) | $I_{LVSSourceAC}$ | >620µs (Datasheet) | | $µA_{pp}$ | 210,00 |
| EOL2 threshold (Rectifier) | $I_{LVSDC}$ | >2500ms (Datasheet) | | $±µA_{RMS}$ | 42,00 |
| Lamp voltage (peak-peak) | $U_{Lamp\_pp}$ | | $U_{Lamp\_pp} = U_{Lamp} \cdot 2 \cdot \sqrt{2} \cdot U_{Lamp\_Fact}$ | $V_{PP}$ | 500,63 |
| Lamp voltage (DC offset) | $U_{Lamp\_DC}$ | | $U_{Lamp\_DC} = \frac{P_{EOLDC\_max}}{I_{Lamp}}$ | $V_{DC}$ | 10,87 |
| **EOL2 calculation (Rectifier Effect)** | | | | | |
| DC voltage across $R_1$ and $R_2$ | | | | $V_{DC}$ | 10,87 |
| $R_1$ and $R_2$ calculated | $R_{1calc}$+$R_{2calc}$ | | $R_{1calc} + R_{2calc} = \frac{U_{Lamp\_DC}}{I_{LVSDC}}$ | kΩ | 258,80 |
| $R_1$ selected | $R_1$ | Select $R_1$ in respect to the voltage strength of $C_1$. $R_1$ >> $R_2$ | | kΩ | 204,00 |
| R2 calculated | $R_{2calc}$ | | $R_2 = R_{1calc} + R_{2calc} - R_1$ | kΩ | 54,80 |
| $R_2$ selected | $R_2$ | | | kΩ | 68,00 |
| $R_1$ and $R_2$ real | $R_1$+$R_2$ | | $R_1 + R_2$ | kΩ | 272,00 |
| EOL Power (DC) calculated | $P_{EOLDC+\_calc}$ | | $P_{EOLDC\_max} = (R_1 + R_2) \cdot I_{LVSDC} \cdot I_{Lamp}$ | W | 5,26 |
| EOL Power (DC) calculated | $P_{EOLDC-\_calc}$ | | $P_{EOLDC\_max} = (R_1 + R_2) \cdot I_{LVSDC} \cdot I_{Lamp}$ | W | 5,26 |
| **EOL1 calculation (Lamp Overvoltage)** | | | | | |
| Actual max voltage | $U_{Lamp\_pp\_EOL1}$ | | $U_{Lamp\_pp\_EOL2} = I_{LVSSourceAC} \cdot (R_1 + R_2)$ | $V_{pp}$ | 57,12 |
| Result | | ULamp_pp_EOL1 too small, R3 and C1 requiered! | | | |
| Voltage across $R_2$ | $U_{R2pp}$ | | $U_{R2pp} = I_{LVSSourceAC} \cdot R_2$ | $V_{pp}$ | 14,28 |
| Voltage across $R_1$ | $U_{R1pp}$ | | $U_{R1pp} = U_{Lamp\_pp} - U_{R2pp}$ | $V_{pp}$ | 486,35 |
| Current through $R_1$ | $I_{R1pp}$ | | $I_{R1pp} = \frac{U_{R1pp}}{R_1}$ | $µA_{pp}$ | 2384,08 |
| Current through $R_3$ | $I_{R3pp}$ | $C_1$ neglected | $I_{R3pp} = I_{R1pp} - I_{LVSSourceAC}$ | $µA_{pp}$ | 2174,08 |
| $R_3$ calculatet | $R_{3calc}$ | | $R_{3calc} = \frac{U_{R2pp}}{I_{R3pp}}$ | kΩ | 6,57 |
| $R_3$ selected | $R_3$ | | | kΩ | 6,80 |
| $C_1$ calculated<br>Select C1 as high as possible in respect of the high side preheating Capacitor! | $C_{1\_min}$ | $C_1$ should affect the current less than 1% | $> \frac{100}{2 \cdot \pi \cdot f_{RUN} \cdot R_3}$ | nF | 52,01 |
| $C_1$ selected | $C_1$ | select $C_1$ as high as possible under consideration of the results of Startup calculation sheet (C40) | | nF | 100,00 |
| EOL1 max voltage calculated | $U_{Lamp\_pp\_EOL1\_calc.}$ | | $U_{Lamp\_pp\_EOL2} = \frac{I_{LVSSourceAC} \cdot (R_2 \cdot R_1 + R_3 \cdot R_1 + R_2 \cdot R_3)}{R_3}$ | $V_{pp}$ | 486 |

**Figure 35 Excel-based EOL Calculation Tool**

Contact us at ***http://www.infineon.com/smartlighting*** to obtain the tool.

### 8.2.2 Sample Calculation – Start-up Network for 54W T5 Design (Excel)

*Figure 36* shows a calculation example for the start-up network to the LVS pin.

**Startup-LVS: Demoboard 1x54W T5 - VM - 180VAC to 270VAC - ICB2FL03G**

This sheet supports designing the LVS-startup-circuit with the FL-Controller ICB2FL03G.
Please fill out the green fields top down. The result is listed in the next line.
The design is: R1=470kΩ, R2=470kΩ, DR12=110kΩ, R34=150kΩ, R35=150kΩ and C40=220nF.

| Parameter | short | comment | calculation | unit | Values |
|---|---|---|---|---|---|
| Minimal Input voltge | $V_{IN\_min}$ | DC-voltage or peak-voltage for AC-supply | | $V_{peak}$ | 176,0 |
| BUS-voltage | $V_{BUS}$ | | | $V_{DC}$ | 410,0 |
| Current for filament detection | $I_{LVSSink}$ | max. value from Datasheet | | µA | 18,0 |
| Internal voltage source LVS | $V_{LVS\_Int}$ | typical value, not tested in End-Test | | $V_{DC}$ | 5,0 |
| $R_{41}$ | $R_{41}$ | $R_2$ (from EOL-calculation) | | kΩ | 68,0 |
| $R_{42}$ | $R_{42}$ | $R_1$ (from EOL-calculation) | | kΩ | 68,0 |
| $R_{43}$ | $R_{43}$ | | | kΩ | 68,0 |
| $R_{44}$ | $R_{44}$ | | | kΩ | 68,0 |
| $R_{45}$ | $R_{45}$ | $R_3$ (from EOL-calculation) | | kΩ | 6,8 |
| **with HS-filament inserted, filament must be detected in the whole input voltage range -** C40 and R45 neglected | | | | | |
| Resistor EOL-DC-Path@Startup | $R_{EOL\_DC}$ | | $R_{EOL\_DC} = R_{41} + R_{42} + R_{43} + R_{44}$ | kΩ | 272,0 |
| Voltage across $R_{EOL\_DC}$ | $V_{REOL\_DC}$ | for lamp detection | $V_{REOL\_DC} = I_{LVSSink} \cdot R_{EOL\_DC}$ | V | 4,9 |
| Voltage Ratio | $n_{voltage}$ | | $n_{voltage} = \frac{V_{BUS}}{V_{IN\_min}}$ | | 2,3 |
| actual $V_{DR12}$ without $R_{34}$+$R_{35}$ | $V_{DR12\_1}$ | | $V_{DR12\_1} = V_{LVS\_Int} + V_{REOL\_DC}$ | V | 9,9 |
| def. $V_{DR12}$ at min. input voltage | $V_{DR12\_min\_def}$ | should be about 6V higher than $V_{DR12\_1}$ | | V | 16,0 |
| $R_{34}$ and $R_{35}$ calculated | $R_{34\_cal}$+$R_{35\_cal}$ | $R_{34\_cal} + R_{35\_cal} = \frac{V_{DR12\_min\_def} - V_{DR12\_1}}{I_{LVSSink}}$ | | kΩ | 339,1 |
| $R_{34}$ selected | $R_{34}$ | | | kΩ | 150,0 |
| $R_{35}$ selected | $R_{35}$ | | | kΩ | 150,0 |
| $R_{34}$ and $R_{35}$ selected | $R_{34}$+$R_{35}$ | must be smaller than calculated value | | kΩ | 300,0 |
| ***worst case, $R_{41}$ to GND instead of LVS-Pin (for calculation of voltage divider $R_1$, $R_2$ and $DR_{12}$ for $V_{DR12\_min}$)*** | | | | | |
| R from $DR_{12}$-to-LVS-DC@Startup | $R_{Startup\_DC}$ | | $R_{Startup\_DC} = R_{34} + R_{35} + R_{EOL\_DC}$ | kΩ | 572,0 |
| Necessary voltage at $DR_{12}$ | $V_{DR12\_min}$ | $V_{DR12\_min} = V_{LVS\_Int} + I_{LVSSink} \cdot R_{Startup\_DC}$ | | V | 15,3 |
| Ratio of $R_{1+2}$ to $DR_{12}$ | $n_{R1+2\_to\_DR12}$ | | $n_{R1+2\_to\_DR12} = \frac{V_{IN\_min}}{V_{DR12\_min}}$ | | 11,5 |
| $DR_{12}$ selected | $DR_{12}$ | take care to $R_1$ and $R_2$ | | kΩ | 110,0 |
| parallel circuit $DR_{12}$, $R_{Startup\_DC}$ | $DR_{12+Startup\_DC}$ | | $DR_{12+Startup\_DC} = \frac{DR_{12} \cdot R_{Startup\_DC}}{DR_{12} + R_{Startup\_DC}}$ | kΩ | 92,3 |
| Resistor $R_1$+$R_2$ | $R_{1\_cal}$+$R_{2\_cal}$ | $R_{1\_cal} + R_{2\_cal} = R_{3+Startup\_DC} \cdot (n_{R1+2\_to\_DR12} - 1)$ | | kΩ | 969,3 |
| $R_1$ selected | $R_1$ | | | kΩ | 470,0 |
| $R_2$ selected | $R_2$ | | | kΩ | 470,0 |
| $R_1$ and $R_2$ selected | $R_1$+$R_2$ | must be smaller than calculated value | | kΩ | 940,0 |
| UDR12 at minimum input votlage | $V_{DR12\_min\_input}$ | $V_{DR12\_min\_input} = \frac{V_{IN\_min} \cdot DR_{12+Startup\_DC}}{R_1 + R_2 + DR_{12+Startup\_DC}}$ | | V | 15,7 |
| UDR12 at maximum input voltage | $V_{DR12\_max\_input}$ | $V_{DR12\_max\_input} = \frac{V_{BUS} \cdot DR_{12+Startup\_DC}}{R_1 + R_2 + DR_{12+Startup\_DC}}$ | | V | 36,6 |
| **without filament, prevent IC startup**<br>worst case, $R_{41}$ open (not connected to LVS-Pin); At maximum input voltage, VC40-to-GND must be < VLVS_Int | | | | | |
| C21 defined | $C_{21}$ | | | nF | 22,0 |
| VDR12_max_input votlage | $V_{DR12\_temp}$ | | | V | 43,0 |
| min. value for $C_{40}$ | $C_{40\_cal}$ | | $C_{40\_cal} = \frac{V_{DR12\_temp} \cdot C_{21}}{V_{LVS\_Int}}$ | nF | 189,0 |
| selected value for C40 | $C_{40}$ | selected value must be higher than calculated value | | nF | 220,0 |

**Figure 36 Excel-based Start-up Network Calculation Tool**

Contact us at http://www.infineon.com/smartlighting to obtain the tool.

### 8.2.3 Inductor L1 of the Boost Converter

The inductivity of the boost inductor is typically designed to operate within a specified voltage range above a minimum frequency in order to obtain easier RFI suppression. It is well known that in critical conduction mode (CritCM) there is a minimum operating frequency at low input voltages and another minimum at maximum input voltage. In state-of-the-art CritCM PFC controllers the lowest value of these two criteria is used.

At minimum AC input voltage:

$$L_A = \frac{(V_{\mathrm{INACmin}} \cdot \sqrt{2})^2 \cdot \left(V_{\mathrm{BUS}} - \left(V_{\mathrm{INACmin}} \cdot \sqrt{2}\right)\right) \cdot n}{4 \cdot f_{\mathrm{min}} \cdot P_{\mathrm{OUTPFC}} \cdot V_{\mathrm{BUS}}}$$

$$L_A = \frac{(180\,V \cdot \sqrt{2})^2 \cdot \left(410\,V - \left(180\,V \cdot \sqrt{2}\right)\right) \cdot 0.95}{4 \cdot 25\,\mathrm{kHz} \cdot 60W \cdot 410\,V} = 3.89\ \mathrm{mH}$$

At maximum AC input voltage:

$$L_B = \frac{\left(V_{\mathrm{INACmax}} \cdot \sqrt{2}\right)^2 \cdot \left(V_{\mathrm{BUS}} - \left(V_{\mathrm{INACmax}} \cdot \sqrt{2}\right)\right) \cdot \eta}{4 \cdot f_{\mathrm{min}} \cdot P_{\mathrm{OUTPFC}} \cdot V_{\mathrm{BUS}}}$$

$$L_B = \frac{\left(270\ V \cdot \sqrt{2}\right)^2 \cdot \left(410\,V - \left(270\,V \cdot \sqrt{2}\right)\right) \cdot 0.95}{4 \cdot 25\,\mathrm{kHz} \cdot 60\,W \cdot 410\,V} = 1.58\ \mathrm{mH}$$

With the new control principle for the PFC preconverter a third criterion that covers the maximum on-time $t_{PFCON\_max}$ is necessary.

At maximum on-time:

$$L_C = \frac{(V_{\mathrm{INACmin}} \cdot \sqrt{2})^2 \cdot T_{\mathrm{ONmax}} \cdot \eta}{4 \cdot P_{\mathrm{OUTPFC}}}$$

$$L_C = \frac{\left(180\ V \cdot \sqrt{2}\right)^2 \cdot 24.0\,\mu\mathrm{s} \cdot \eta}{4 \cdot 60W} = 6.16\ \mathrm{mH}$$

With the assumed conditions the lowest value out of $L_A$, $L_B$, $L_C$ is 1.58 mH.

The selected value is: $L_1$ = 1.58 mH

### 8.2.4 Shunt Resistors for Ignition Voltage $R_{24}$, $R_{25}$

The selected lamp type 54W T5 requires an ignition voltage of $V_{IGN}$ = > 620 $V_{RMS}$. The board is designed for an ignition voltage of $V_{IGN}$ = 800 $V_{RMS}$ (1130 $V_{peak}$). In this application example the resonant inductor is evaluated as $L_2$ = 1.46 mH and the resonant capacitor as $C_{20}$ = 4.7 nF. With these inputs the ignition frequency $f_{IGN}$ can be calculated in a first step:

Calculation of ignition frequency $f_{IGN}$:

$$f_{\mathrm{IGN}} = \sqrt{\frac{1 \pm \frac{V_{\mathrm{BUS}} \cdot 2}{\pi \cdot V_{\mathrm{IGN}}}}{4 \cdot \pi^2 \cdot L_2 \cdot C_{20}}} = \sqrt{\frac{1 \pm \frac{410\ V \cdot 2}{\pi \cdot 1130\,V_{\mathrm{peak}}}}{4 \cdot \pi^2 \cdot 1{,}46\,\mathrm{mH} \cdot 4.7\ \mathrm{nF}}} = 67410\ \mathrm{Hz}$$

The second solution of this equation (with the minus sign) leads to a result of 50163 Hz, which is on the capacitive side of the resonant rise. This value is not a solution because the operating frequency approaches from the higher frequency level.

In the next step, the current through the resonant capacitor $C_{20}$ must be calculated when reaching a voltage level of 800 $V_{peak}$.

Calculation of resonant capacitor current $I_{C20}$:

$$I_{C20} = V_{\text{IGN}} \cdot 2 \cdot \pi \cdot f_{\text{IGN}} \cdot C_{20} = 1130\ V_{\text{peak}} \cdot 2 \cdot \pi \cdot 67410\ \text{Hz} \cdot 4.7\ \text{nF} = 2.25\ A$$

Finally, the resistors $R_{24}$ and $R_{25}$ can be calculated with $I_{C20}$ and the ignition regulating value at the LSCS pin of about 0.8 V.

Calculation of $R_{24}$ and $R_{25}$:

$$\frac{R_{24} \cdot R_{25}}{R_{24} + R_{25}} = \frac{0.8\ V}{I_{C20}} = \frac{0.8\ V}{2.25\ A} = 0.356\ \Omega$$

The selected values are: $R_{24} = R_{25} = 0.68\Omega$ (= 0.34 Ω).

### 8.2.5 Ballast Parameters

The following formulas give advice on calculating relevant ballast parameters.

Calculation of start-up resistors $R_{11}$ and $R_{12}$:

$$R_{11} + R_{12} = \frac{V_{\text{BUS min Input}}}{I_{\text{VCCLatch}} - I_{\text{RESI min}}} = \frac{254\ V}{170\ \mu\text{A} + 54.3\ \mu\text{A}} = 1132\ \text{k}\Omega$$

The selected values are: $R_{11} = R_{12} = 470\ \text{k}\Omega$

Calculation of PFCVS resistor $R_{20}$:

$$R_{20} \le \frac{V_{\text{PFCVSREF}}}{100 \cdot I_{\text{PFCBIAS}}} = \frac{2.5\ V}{100 \cdot 1.0\ \mu\text{A}} = 25\ \text{k}\Omega$$

The selected value is: $R_{20} = 10\ \text{k}\Omega$

Calculation of PFCVS resistors $R_{14}$ and $R_{15}$:

$$R_{14} + R_{15} = \frac{V_{\text{BUS}} - V_{\text{PFCVSREF}}}{V_{\text{PFCVSREF}}} \cdot R_{20} = \frac{410\ V - 2.5\ V}{2.5\ V} \cdot 10\ \text{k}\Omega = 1630\ \text{k}\Omega$$

The selected values are: $R_{14} = R_{15} = 820\ \text{k}\Omega$

Calculation of low pass capacitor $C_{11}$ (corner frequency $f_{C1} = 10$ kHz):

$$C_{11} = \frac{1 \cdot (R_{20} + R_{14} + R_{15})}{2 \cdot \pi \cdot f_{C1} \cdot R_{20} \cdot (R_{14} + R_{15})} = \frac{10\ \text{k}\Omega + 820\ \text{k}\Omega + 820\ \text{k}\Omega}{2 \cdot \pi \cdot 10\ \text{kHz} \cdot 10\ \text{k}\Omega \cdot (820\ \text{k}\Omega + 820\ \text{k}\Omega)} = 1.6\ \text{nF}$$

The selected value is: $C_{11} = 2.2$ nF

Calculation of PFC shunt resistors $R_{18}$ and $R_{19}$:

$$\frac{R_{18} \cdot R_{19}}{R_{18} + R_{19}} = \frac{V_{\text{PFCCSOFF}} \cdot \eta \cdot V_{\text{INACMIN}} \cdot \sqrt{2}}{4 \cdot P_{\text{OUTPFC}}} = \frac{1\ V \cdot 0.95 \cdot 180\ V \cdot \sqrt{2}}{4 \cdot 60\ W} = 1.0\ \Omega$$

The selected values are: $R_{18} = 1\ \Omega$ and $R_{19}$ = not assembled

Calculation of run frequency resistor $R_{21}$ for $f_{\text{RUN}} = 45$ kHz:

$$R_{21} = R_{\text{FRUN}} = \frac{5 \cdot 10^8\ \Omega \cdot \text{Hz}}{f_{\text{RUN}}} = \frac{5 \cdot 10^8\ \Omega \cdot \text{Hz}}{45\ \text{kHz}} = 11.1\ \text{k}\Omega$$

The selected value is: $R_{21} = 11\ \text{k}\Omega$

Calculation of preheating frequency resistor $R_{22}$ for $f_{\text{PH}} = 105$ kHz:

$$R_{22} = R_{\text{FPH}} = \frac{R_{\text{FRUN}}}{\frac{f_{\text{PH}} \cdot R_{\text{FRUN}}}{5 \cdot 10^8 \cdot \Omega \cdot \text{Hz}}} = \frac{11\ \text{k}\Omega}{\frac{105\ \text{kHz} \cdot 11\ \text{k}\Omega}{5 \cdot 10^8 \cdot \Omega \cdot \text{Hz}}} = 8.4\ \text{k}\Omega$$

The selected value is: $R_{22} = 8.2\ \text{k}\Omega$

Calculation of preheating time resistor $R_{23}$ for $t_{\text{PH}} = 1000$ms:

$$R_{23} = R_{\text{TPH}} = \frac{t_{\text{PH}} \cdot \text{k}\Omega}{100\ \text{ms}} = \frac{1000\ \text{ms} \cdot \text{k}\Omega}{100\ \text{ms}} = 10\ \text{k}\Omega$$

The selected value is: $R_{23} = 10\ \text{k}\Omega$

## 8 Annex

The gate drive resistors $R_{16}$, $R_{26}$ and $R_{27}$ are recommended to be equal to or greater than 10 Ω (selected: 10 Ω).

Calculation of bootstrap current limitation resistor $R_{30}$:

$$R_{30} \geq \frac{2 \cdot V_{\mathrm{VCCON}}}{V_{\mathrm{LSCSOVCI}}} \cdot \frac{R_{24} \cdot R_{25}}{R_{24} \cdot R_{25}} = \frac{2 \cdot 14.0 \ \ V}{1.6 \ \ V} \cdot \frac{0.68 \ \ \Omega \cdot 0.68 \ \ \Omega}{0.68 \ \ \Omega \cdot 0.68 \ \ \Omega} = 6 \ \ \Omega$$

The factor of 2 is used in order to keep away from the limit value.

The selected value is: $R_{30}$ = 33 Ω

Calculation of LS filament sense resistor $R_{36}$:

$$R_{36} < \frac{V_{\mathrm{RES1MIN}}}{I_{\mathrm{RES3MIN}}} = \frac{1.55 \ \ V}{26.6 \ \ \mu\mathrm{A}} = 58.3 \ \ \mathrm{k\Omega}$$

$$R_{36} > \frac{V_{\mathrm{RES1MAX}}}{I_{\mathrm{RES1MAX}}} = \frac{1.65 \ \ V}{32.0 \ \ \mu\mathrm{A}} = 51.6 \ \ \mathrm{k\Omega}$$

The selected value is: $R_{36}$ = 56 kΩ

Calculation of low pass capacitor $C_{19}$:

$$C_{19} = \frac{\sqrt{{F_{\mathrm{LP}}}^2 - 1}}{2 \cdot \pi f_{\mathrm{RUN}} \cdot R_{36}} = \frac{\sqrt{300^2 - 1}}{2 \cdot \pi 45 \ \ \mathrm{kHz} \cdot 56 \ \ \mathrm{k\Omega}} = 18.9 \ \ \mathrm{nF}$$

The capacitor $C_{19}$ provides a low pass filter together with resistor R36 in order to suppress AC voltage drops at the LS filament. With an estimation of the AC voltage of about 10 $V_{\mathrm{peak\text{-}to\text{-}peak}}$ at the LS filament during run mode for $f_{\mathrm{RUN}}$ = 45 kHz, suppression by a factor of at least $F_{\mathrm{LP}}$ = 300 is necessary

The selected value is: $C_{19}$ = 22 nF.

*Note: The voltage at the RES pin must reach the filament detection level until VCC reaches the $V_{\mathrm{VCCOn}}$ threshold (see **The IC Starts without a Low-Side FilamentThe IC Starts without a Low-Side Filament**).*

## 8.3 Troubleshooting

This section gives some advice on finding and handling typical start-up problems in designs with the ICB2FL03G. Please check the function in the sequence described in ***Figure 4***. If these checks do not solve the problem, please take a look at ***VCC does not reach 10.5 V ($V_{VCCOff}$) or 14 V ($V_{VCCOn}$)*** to ***The IC Stops about 3 s after Ignition***. If these checks also do not solve the problem, please contact Infineon Technologies AG for further support.

Depending on the voltage at the RES pin, the current consumption of the IC can be higher due to $I_{RES1}$ to $I_{RES4}$

### 8.3.1 VCC does not reach 10.5 V ($V_{VCCOff}$) or 14 V ($V_{VCCOn}$)

If VCC does not reach the $V_{VCCOff}$ threshold (also called the UVLO threshold), the current consumption of the IC is too high or the current through the VCC start-up resistors is too low. The minimum current required, fed across the start-up resistors, is $I_{VCCqu1}$ until $V_{VCCOff}$ is reached and $I_{VCCqu2}$ until $V_{VCCOn}$ is reached. Another powerconsuming device at VCC may be the reason for preventing VCC rising to $V_{VCCOff}$.

- Remove any other consumer at VCC.
- Check the bus voltage and calculate the minimum current across the start-up resistors.
- Check if a wrong Z-diode $D_9$ is mounted that limits the voltage at VCC.

### 8.3.2 VCC Hiccup between 14 V ($V_{VCCOff}$) and 10.5 V ($V_{VCCOn}$)

If VCC reaches the $V_{VCCOn}$ threshold and then goes down to $V_{VCCOff}$ repeatedly (called hiccup operation), the following reasons may apply. There can be a problem in detection of the bus voltage or in the VCC supply via the charge pump.

- Is the bus voltage in the specified range of 12.5 % and 105 % (~0.39 V and 2.57 V at PFCVS pin)?
- Is the voltage divider for bus voltage sensing broken?
- Are the LSGD and HSGD working during VCC breakdown? Otherwise check the next two subcategories.
- Are the diodes of the charge pump correctly mounted ($D_7$ and $D_8$)?
- Check the ratio of $C_{12}$ and $C_{14}$
- Is the charge pump design strong enough? Note: Layout and components have to handle the peak currents.

Calculation of charge pump

$$I_{\mathrm{CHARGE}} = (V_{\mathrm{BUS}} - V_{\mathrm{VCC}}) \cdot f \cdot C_{16}$$

### 8.3.3 No LSGD Pulse

When all start-up conditions are ok, the first pulse out of the IC is normally visible at the LSGD pin. If the VCC is above the $V_{VCCOn}$ threshold and the bus voltage is in the specified range between 12.5 % and 105 %, a filament detection problem can cause this behavior.

- The bus voltage must be smaller than the min. value of $V_{PFCVSLow}$ (105 %) before start-up.
- Set both LVS pins temporarily to GND to disable the high-side filament detection.
- Set the RES pin temporarily to GND to disable the high- and low-side filament detection.

If this solves the problem, a redesign of the LVS path and the resistor R36 is necessary (see ***Calculations***) for correct operation with filament detection.

### 8.3.4 No HSGD Pulse

If there is no HSGD pulse after a number of initial LSGD pulses, a problem with the HSVCC supply may be the reason.

- The bus voltage must be smaller than min. value of $V_{PFCVSLow}$ (105 %) before start-up.
- Check if VCC breaks down to $V_{VCCOff}$ while charging the HSVCC capacitor $C_{14}$ – a higher capacitance at the VCC pin might be helpful.
- Check if the HSVCC reaches a level of min. $V_{HSVCCOn}$ (max. value); does $C_{14}$ have the right value?
- Check if $R_{30}$ and $D_6$ are mounted in the right way.
- Check if the $V_{LSCSOvC1}$ threshold is reached; increasing $R_{30}$ might be helpful.

### 8.3.5 No PFCGD Pulse

If there is no PFCGD pulse after 300 µs of correct inverter working, there can only be a problem in the monitoring of the bus voltage or the connecting tracks to MOSFET.

- The bus voltage must be smaller than the min. value of $V_{PFCVSLow}$ (105 %) before start-up.
- The bus voltage must be smaller than the min. value of $V_{PFCVSRUp}$ (109 %) during run mode.

A bus overvoltage hysteresis is implemented. If the 109 % threshold is reached in run mode, the PFCGD turns off immediately and the bus voltage must undershoot the 105 % threshold for reactivating the PFCGD.

### 8.3.6 The IC Starts without a High-Side Filament

If the IC starts without a high-side filament, a startup current flows into the LVS pin. If a current of min. value of $I_{LVSSINK}$ flows into the LVS pin, the IC interprets this as a present high-side filament. Due to a less than optimum design, this current can flow via other components if no filament is present. If the capacitor in the preheating circuit $C_{21}$ has a high capacitance and $C_{40}$ is relatively low, a transient current flows via $C_{21}$ and $L_{21}$, that is high enough to lead to a high-side filament detection.

- Measure the peak voltage between $C_{40}$ and $R_{41}$ in reference to GND before VCC reaches $V_{VCCOn}$, subtract 5 V[1]) and calculate the current flowing into the LVS pin with the value of $R_{41}$ (further information can be found in ***LVS Pin***)
- Try a capacitor with a higher capacitance for $C_{40}$, this reduces the voltage across $R_{41}$ and leads to a lower transient current into the LVS pin.

Another reason can be that the VCC rise is too fast, and the voltage at the RES pin cannot reach the filament detection level until VCC reaches the $V_{VCCOn}$ threshold. Also check the EOL calculation in ***Sample Calculation: EOL for 54W T5 Design (Excel)***.

### 8.3.7 The IC Starts without a Low-Side FilamentThe IC Starts without a Low-Side Filament

If the IC starts without a low-side filament, a component at this pin leads to a limited voltage at this pin.

- Is the capacitance of $C_{19}$ too high?
- The voltage at the RES pin must be higher than $V_{RES1}$ before VCC reaches the $V_{VCCOn}$ threshold

Another reason can be that the VCC rise is too fast and the voltage at the RES pin cannot reach the filament detection level until VCC reaches the VVCCOn threshold (see also ***Calculations***).

### 8.3.8 The IC Stops within $t_{PRERUN}$ after Ignition

The Protection Function Matrix in Section 4 of the Data Sheet shows in which operating mode special fault detection becomes active. If the IC stops within $t_{PRERUN}$ after ignition, some basic parameters of the circuit

1 The Data Sheet specifies the voltage $V_{LVSClamp}$ = 6.5 V at $I_{LVS}$ =300 µA. An internal comparator threshold of 5 V (see also ***LVS Pin***) can be used for calculation of the start-up current.

will not be in the specified area because in pre-run mode only a few fault detection functions are active. The following list gives an overview of which conditions must be fulfilled for correct IC operation.

- Voltage at VCC must be > $V_{VCCOff}$
- Bus voltage must be > 12.5 %
- Voltage at the PFCCS pin must be < $V_{PFCCSOff}$
- Voltage at the RES pin must be < $V_{RES1}$
- Voltage at the LSCS pin must be < $V_{LSCSOvC1}$

### 8.3.9 The IC Stops about $t_{PRERUN}$ after Ignition

When the IC stops about 625 ms after ignition a failure of a short duration (several µs) can be the reason. The following list gives an overview of what conditions must be fulfilled for correct IC operation.

- Voltage at RES pin < $V_{RES3}$ • • • •
- Bus voltage > 75 %
- EOL1 (overvoltage); set the LVS pin temporarily to GND to verify if this is the problem.
- Cap. load 2; check the waveform at the LSCS pin and compare it with Section 2.6.2 in the Data Sheet.
- Voltage at LSCS pin < $V_{LSCSOvC2}$

### 8.3.10 The IC Stops about 3 s after Ignition

If the IC stops about 3 s after ignitionm a failure of lengthy duration (2500 ms) can be the reason. The following list gives an overview of what conditions must be fulfilled for correct IC operation.

- EOL2 (rectifier effect); set the LVS pin temporarily to GND to verify if this is the problem.
- Cap. load 1; Check the waveform at the LSCS pin and compare it with Section 2.6.1 in the Data Sheet.

## 8.4 BOM Schematic Layout

The documentation of the demo board can be found in this section.

**BOM: Demoboard 1x54W T5 - VM - 180VAC to 270VAC - ICB2FL03G**

ICB2FL03G

Input voltage = 180VAC to 270VAC

VBUS = 410 VRMS

| | | | | Package |
|---|---|---|---|---|
| F1 | Fuse 1A fast | Wickmann | Typ 370 | |
| | | | | |
| K1/1 | AC Input | WAGO 250-203 | | |
| K1/2 | AC Input | | | |
| K1/3 | PE | | | |
| K2/1 | not connected | WAGO 250-203 | | |
| K2/2 | High Side Filament | | | |
| K2/3 | High Side Filament | | | |
| K3/1 | Low Side Filament | WAGO 250-203 | | |
| K3/2 | Low Side Filament | | | |
| K3/3 | not connected | | | |
| IC1 | ICB2FL03G | Infineon | | SO-16 |
| Q1 | IPN60R1K5PFD7S | Infineon | | SOT223 |
| Q2 | IPN60R1K5PFD7S | Infineon | | SOT223 |
| Q3 | IPN60R1K5PFD7S | Infineon | | SOT223 |
| D1…4 | S1M | Fairchild | (1000V/1A/2µs) | DO-214AC |
| D5 | MURS160T3 | ON Semi | (600V/1A/75ns) | SMB |
| D6 | BYG20J | Philips | (600V/1,5A/75ns) | SOD124 |
| D7 | BYG22D | Philips | (200V/1A/25ns) | DO214 |
| D8 | BYG22D | Philips | (200V/1A/25ns) | DO214 |
| D9 | BZV55-C16 | NXP | | SOD-80C |
| DR12 | 110kΩ | | | .1206 |
| D82 | 0Ω | | | .2512 |
| | | | | |
| L101 | 2x68mH/0.6A | Epcos | B82732F2601B001 | |
| L1 PFC | 1.58mH | Epcos | B78326P7373A005 | EFD25/13/9 |
| L 2 | 1.46mH | Epcos | B78326P7374A005 | EFD25/13/9 |
| L 21 | 100µH/760mA | Epcos | B82144B1104J000 | RM5 |
| L 22 | 100µH/760mA | Epcos | B82144B1104J000 | RM5 |
| | | | | |
| C1 | 220nF/X2/305V | Epcos | B32922C3224M000 | RM15 |
| C2 | 33nF/630V/MKT | Epcos | B32521N8333K000 | RM10 |
| C3 | 3,3nF/Y2/300V | Epcos | B32021A3332K000 | RM10 |
| C4 | 220nF/X2/305V | Epcos | B32922C3224M000 | RM15 |
| C10 | 10µF/450V | Epcos | B43888C5106M000 | single ended |
| C11 | 2,2nF/50V | X7R | | .0805 |
| C12 | 100nF/50V | X7R | | .0805 |
| C13 | 1µF/25V | X7R | | .1206 |
| C14 | 68nF/50V | X7R | | .0805 |
| C15 | 22nF/630V/MKT | Epcos | B32621A6223K000 | RM10 |
| C16 | 1nF/630V/MKT | Epcos | B32529C8102K000 | RM5 |
| C17 | 100nF/630V/MKP | Epcos | B32612A6104K008 | RM15 |
| C19 | 22nF/50V | X7R | | .0805 |
| C20 | 4,7nF/1600V/MKP | Epcos | B32612-J1472J008 | RM15 |
| C21 | 22nF/400V/MKP | Epcos | B32620A4223J000 | RM7,5 |
| C22 | 22nF/400V/MKP | Epcos | B32620A4223J000 | RM7,5 |
| C23 | 10nF/50V | X7R | | .0805 |
| C40 | 220nF/50V | X7R | | .0805 |

| | | Package |
|---|---|---|
| R1 | 470kΩ | .1206 |
| R2 | 470kΩ | .1206 |
| R11 | 470kΩ | .1206 |
| R12 | 470kΩ | .1206 |
| R13 | 33kΩ | .1206 |
| R14 | 820kΩ | .1206 |
| R15 | 820kΩ | .1206 |
| R16 | 10Ω | .0805 |
| R18 | 1Ω | .1206 |
| R19 | not assembled | .1206 |
| R20 | 10kΩ | .0805 |
| R21 | 11kΩ | .0805 |
| R22 | 8.2kΩ | .0805 |
| R23 | 10kΩ | .0805 |
| R24 | 0.68Ω | .1206 |
| R25 | 0.68Ω | .1206 |
| R26 | 10Ω | .0805 |
| R27 | 10Ω | .0805 |
| R30 | 33Ω | .1206 |
| R34 | 150kΩ | .1206 |
| R35 | 150kΩ | .1206 |
| R36 | 56kΩ | .1206 |
| R41 | 68kΩ | .0805 |
| R42 | 68kΩ | .1206 |
| R43 | 68kΩ | .1206 |
| R44 | 68kΩ | .1206 |
| R45 | 6,8kΩ | .1206 |
| R61 | 0Ω | .0805 |

**More information:**

http://www.infineon.com/smartlighting

http://www.infineon.com/CoolMOS

http://www.epcos.com Email: wolfgang.dreipelcher@epcos.com

**Figure 37 Bill of Material for Demo Board 1x54W T5 Single Lamp with Voltage Mode Preheating**

## 8 Annex

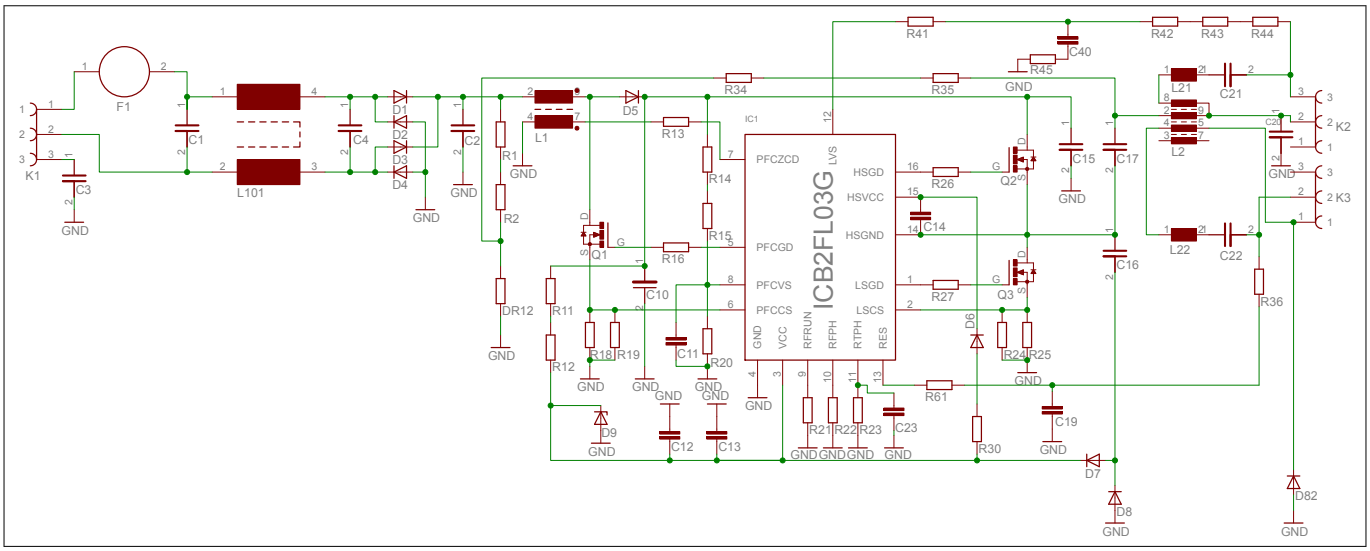



**Figure 38 Schematic**

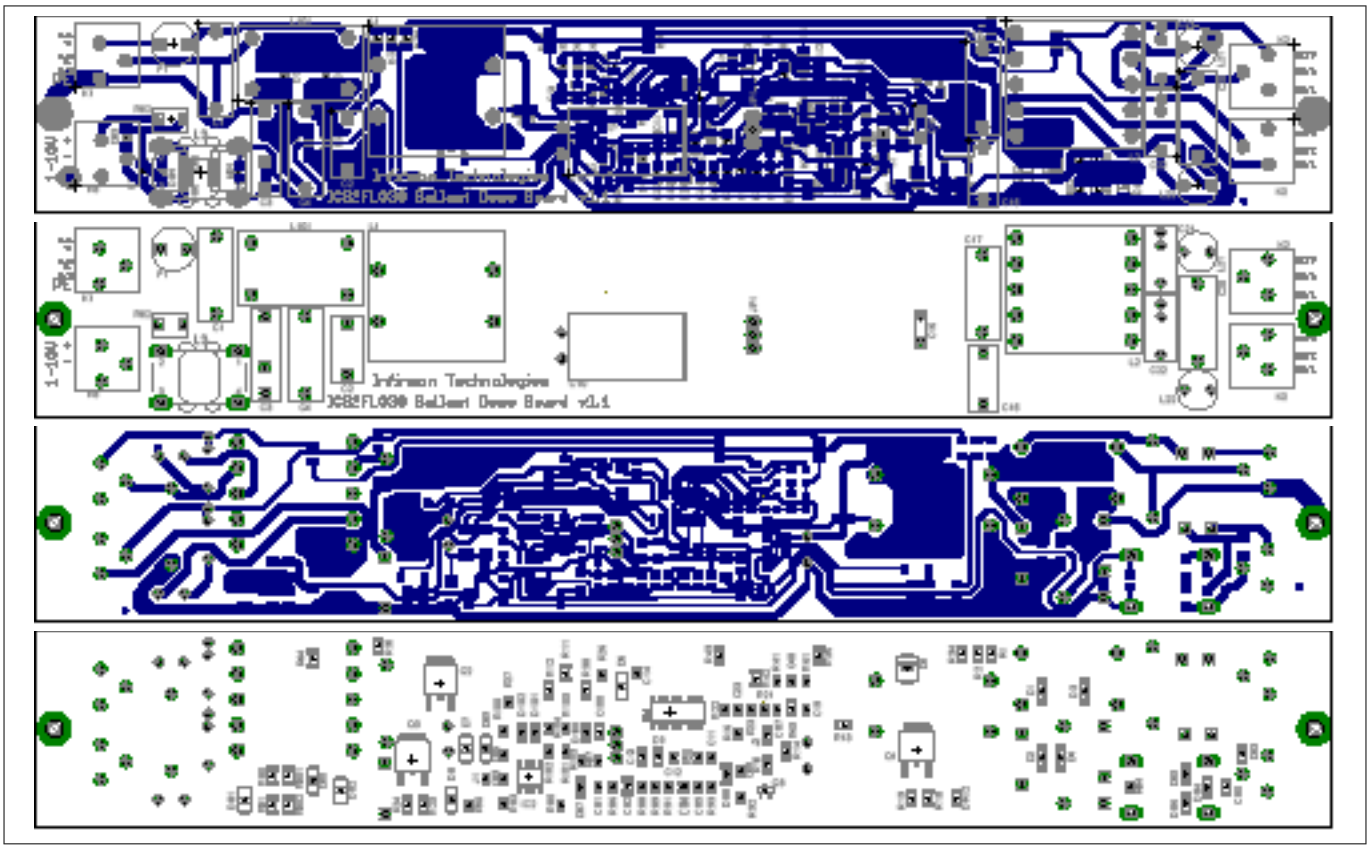



**Figure 39 Layout**

## 8.5 Interference Suppression according to EN 55015

*Figure 40* shows the results of the standard test for interference suppression.

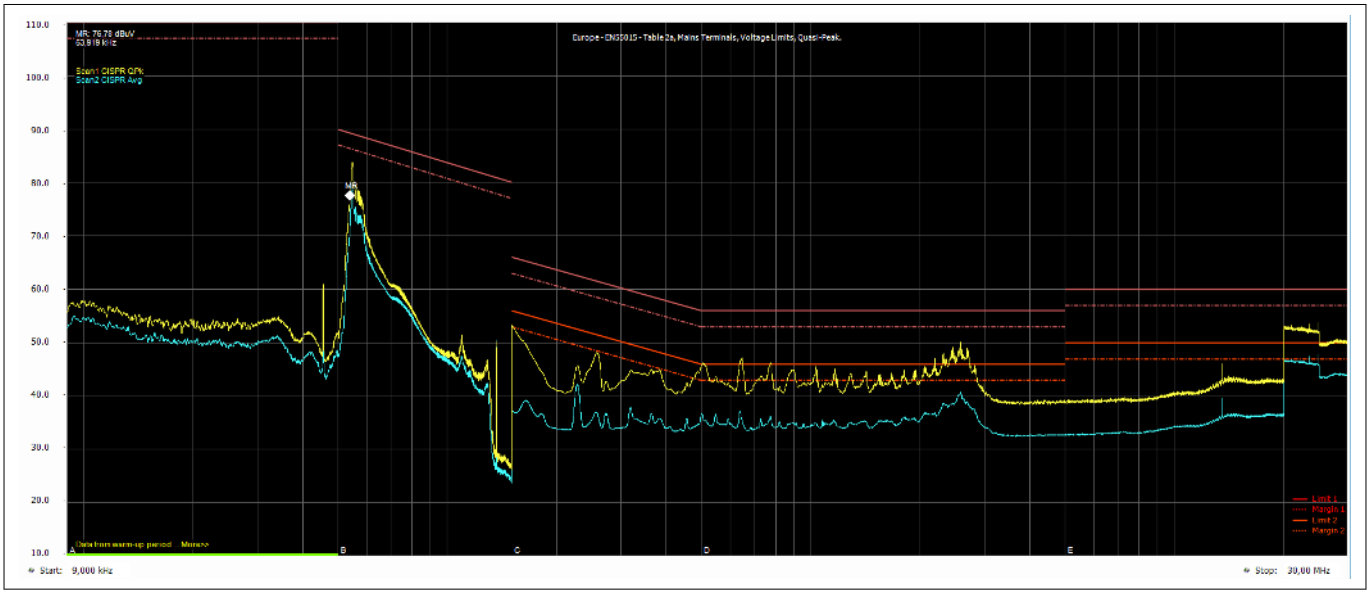



**Figure 40 Interference Suppression according ti EN 55015**

# 9 Terminology

| Acronyms | Explanation |
|---|---|
| $A_{THD}$ | Input current - Total Harmonic Distortion |
| BOM | Bill of material |
| CritCM | Critical Conduction Mode |
| DCM | Discontinuous Conduction Mode |
| EEI | Energy Efficiency Index |
| EOL1 | End of Life 1 (Inverter Overload) |
| EOL2 | End of Life 2 (Rectifier Effect) |
| FL | Fluorescent Lamp |
| $f_{PH}$ | Preheating frequency |
| $F_{RUN}$ | Run frequency |
| HSVCC | IC Supply Voltage (High Side) |
| $I_{Lamp}$ | Lamp current |
| n | efficiency |
| PF | Power factor |
| PFC | Power Factor Correction |
| THD | Total Harmonic Distortion |
| $t_{PH}$ | Preheating time |
| UVLO | Undervoltage Lockout (Restart after VCC hysteresis) |
| $V_{BUS}$ | Electrolytic condensator voltage |
| VCC | IC Supply voltage (Low Side) |
| $V_{IGN}$ | Ignition voltage |
| $V_{IN}$ | Board Input voltage |
| $V_{Lamp}$ | Lamp voltage |

# Revision history

| Revision History | |
|---|---|
| **Page or Item** | **Page or Item** |
| Rev. 1.2, 2020-11-04 | |
| Annex | BOM updated, EMI measurement updated |
| Rev. 1.1, 2012-04-10 | |
| | Reviewed and updated |
| Rev. 1.0, 2010-09-28 | |
| | First edition |

**Trademarks**

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2020-04-11**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**



**Do you have a question about any aspect of this document?**

**Email: erratum@infineon.com**

**Document reference**
**IFX-tul1604305959835**

**IMPORTANT NOTICE**

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

**WARNINGS**

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.