

74HC165; 74HCT165

8-bit parallel-in/serial out shift register

Rev. 03 — 14 March 2008

Product data sheet

1. General description

The 74HC165; 74HCT165 are high-speed Si-gate CMOS devices that comply with JEDEC standard no. 7A. They are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC165; 74HCT165 are 8-bit parallel-load or serial-in shift registers with complementary serial outputs (Q_7 and $\overline{Q_7}$) available from the last stage. When the parallel load (\overline{PL}) input is LOW, parallel data from the D0 to D7 inputs are loaded into the register asynchronously.

When \overline{PL} is HIGH, data enters the register serially at the DS input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the DS input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input \overline{CE} should only take place while CP HIGH for predictable operation. Either the CP or the \overline{CE} should be HIGH before the LOW-to-HIGH transition of \overline{PL} to prevent shifting the data when \overline{PL} is activated.

2. Features

- Asynchronous 8-bit parallel load
- Synchronous serial input
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Applications

- Parallel-to-serial data conversion

4. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74HC165N 74HCT165N | -40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74HC165D 74HCT165D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HC165DB 74HCT165DB | -40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HC165PW 74HCT165PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HC165BQ 74HCT165BQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

5. Functional diagram

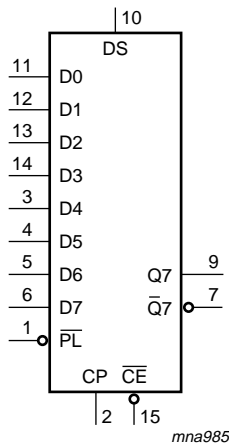


Fig 1. Logic symbol

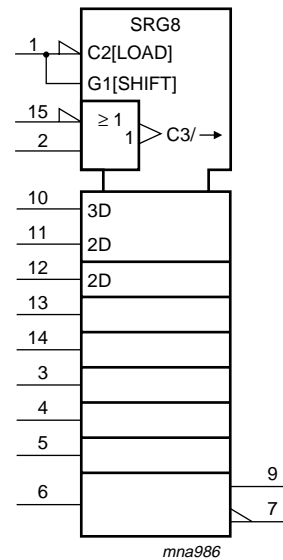


Fig 2. IEC logic symbol

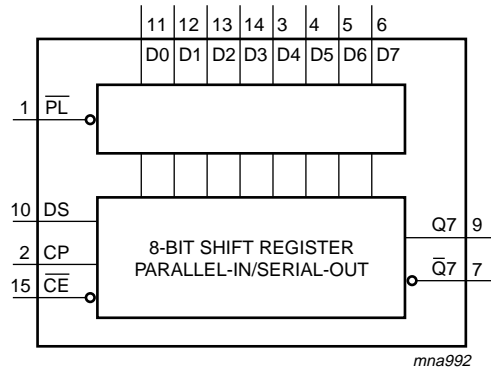


Fig 3. Functional diagram

6. Pinning information

6.1 Pinning

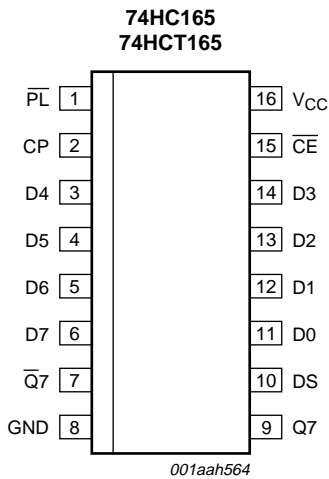
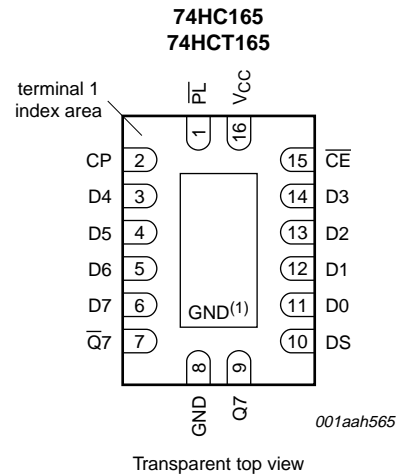


Fig 4. Pin configuration (DIP16, SO16 and (T)SSOP16)



- (1) The die substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input.

Fig 5. Pin configuration (DHVQFN16)

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|------------------------|----------------------------|--|
| $\overline{\text{PL}}$ | 1 | asynchronous parallel load input (active LOW) |
| CP | 2 | clock input (LOW-to-HIGH edge-triggered) |
| $\overline{\text{Q7}}$ | 7 | complementary output from the last stage |
| GND | 8 | ground (0 V) |
| Q7 | 9 | serial output from the last stage |
| DS | 10 | serial data input |
| D0 to D7 | 11, 12, 13, 14, 3, 4, 5, 6 | parallel data inputs (also referred to as D _n) |
| $\overline{\text{CE}}$ | 15 | clock enable input (active LOW) |
| V _{CC} | 16 | positive supply voltage |

7. Functional description

Table 3. Function table^[1]

| Operating modes | Inputs | | | | | Qn registers | | Outputs | |
|-------------------|------------------------|------------------------|----|----|----------|--------------|----------|---------|------------------------|
| | $\overline{\text{PL}}$ | $\overline{\text{CE}}$ | CP | DS | D0 to D7 | Q0 | Q1 to Q6 | Q7 | $\overline{\text{Q7}}$ |
| parallel load | L | X | X | X | L | L | L to L | L | H |
| | L | X | X | X | H | H | H to H | H | L |
| serial shift | H | L | ↑ | l | X | L | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | L | ↑ | h | X | H | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | ↑ | L | l | X | L | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | ↑ | L | h | X | H | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| hold "do nothing" | H | H | X | X | X | q0 | q1 to q6 | q7 | $\overline{\text{q7}}$ |
| | H | X | H | X | X | q0 | q1 to q6 | q7 | $\overline{\text{q7}}$ |

- [1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care;
↑ = LOW-to-HIGH clock transition.

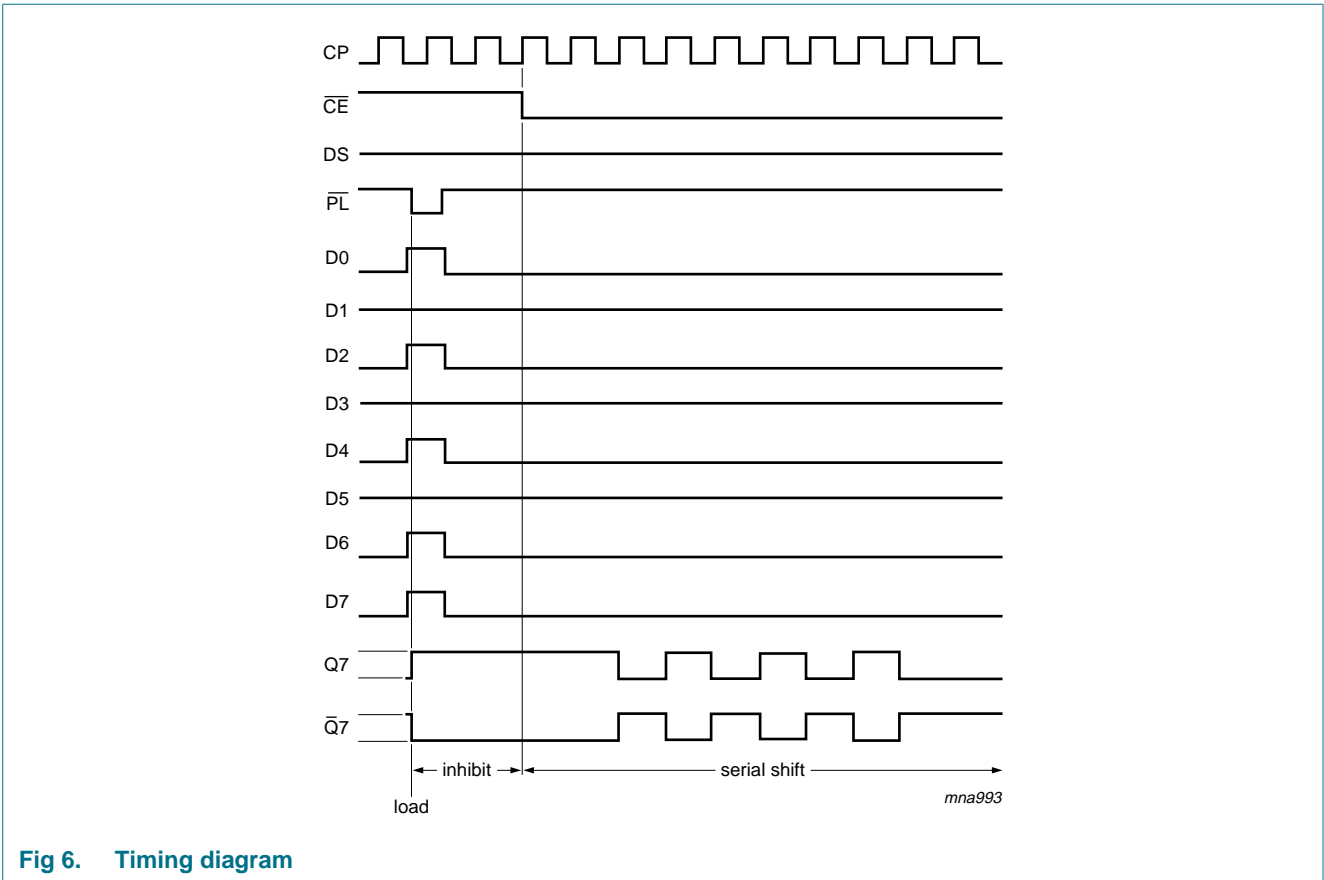


Fig 6. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|-------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | [1] - | ±20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | [1] - | ±20 | mA |
| I_O | output current | $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ | - | ±25 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--------------------------------------|-------|-----|------|
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C | | | |
| | | DIP16 package | [2] - | 750 | mW |
| | | SO16 package | [3] - | 500 | mW |
| | | (T)SSOP16 package | [4] - | 500 | mW |
| | | DHVQFN16 package | [5] - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC165 | | | 74HCT165 | | | Unit |
|------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | - | +125 | -40 | - | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|--------------------------|-------------------------|-------|-----|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC165 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|---|-------|------|------|------------------|-------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | I _O = -5.2 mA; V _{CC} = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| 74HCT165 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | Dn and DS inputs | - | 35 | 126 | - | 157.5 | - | 171.5 | μA |
| | | CP \overline{CE} , and \overline{PL} inputs | - | 65 | 234 | - | 292.5 | - | 318.5 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 12

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-------------------------|-------------------|---|---------------------|---|---------------------|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC165 | | | | | | | | | | |
| t _{pd} | propagation delay | CP or \overline{CE} to Q7, $\overline{Q7}$; see Figure 7 | [1] | | | | | | | |
| | | V _{CC} = 2.0 V | - | 52 | 165 | - | 205 | - | 250 | ns |
| | | V _{CC} = 4.5 V | - | 19 | 33 | - | 41 | - | 50 | ns |
| | | V _{CC} = 6.0 V | - | 15 | 28 | - | 35 | - | 43 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 16 | - | - | - | - | - | ns |
| | | \overline{PL} to Q7, $\overline{Q7}$; see Figure 8 | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 50 | 165 | - | 205 | - | 250 | ns |
| | | V _{CC} = 4.5 V | - | 18 | 33 | - | 41 | - | 50 | ns |
| | | V _{CC} = 6.0 V | - | 14 | 28 | - | 35 | - | 43 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 15 | - | - | - | - | - | ns |
| | | D7 to Q7, $\overline{Q7}$; see Figure 9 | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 36 | 120 | - | 150 | - | 180 | ns |
| | | V _{CC} = 4.5 V | - | 13 | 24 | - | 30 | - | 36 | ns |
| | | V _{CC} = 6.0 V | - | 10 | 20 | - | 26 | - | 31 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 11 | - | - | - | - | - | ns |
| | | t _t | transition time | Q7, $\overline{Q7}$ output; see Figure 7 | [2] | | | | | |
| V _{CC} = 2.0 V | - | | | 19 | 75 | - | 95 | - | 110 | ns |
| V _{CC} = 4.5 V | - | | | 7 | 15 | - | 19 | - | 22 | ns |
| V _{CC} = 6.0 V | - | | | 6 | 13 | - | 16 | - | 19 | ns |
| t _w | pulse width | CP input HIGH or LOW; see Figure 7 | | | | | | | | |
| | | V _{CC} = 2.0 V | 80 | 17 | - | 100 | - | 120 | - | ns |
| | | V _{CC} = 4.5 V | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | V _{CC} = 6.0 V | 14 | 5 | - | 17 | - | 20 | - | ns |
| | | \overline{PL} input LOW; see Figure 8 | | | | | | | | |
| | | V _{CC} = 2.0 V | 80 | 14 | - | 100 | - | 120 | - | ns |
| | | V _{CC} = 4.5 V | 16 | 5 | - | 20 | - | 24 | - | ns |
| | | V _{CC} = 6.0 V | 14 | 4 | - | 17 | - | 20 | - | ns |
| | | t _{rec} | recovery time | \overline{PL} to CP, \overline{CE} ; see Figure 8 | | | | | | |
| V _{CC} = 2.0 V | 100 | | | 22 | - | 125 | - | 150 | - | ns |
| V _{CC} = 4.5 V | 20 | | | 8 | - | 25 | - | 30 | - | ns |
| V _{CC} = 6.0 V | 17 | | | 6 | - | 21 | - | 26 | - | ns |

Table 7. Dynamic characteristics ...continued
 GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 12](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit | |
|-----------|-------------------------------|--|--|-----|-----|------------------|-----|-------------------|-----|------|----|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| t_{su} | set-up time | DS to CP, \overline{CE} ; see Figure 10 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 11 | - | 100 | - | 120 | - | ns | |
| | | $V_{CC} = 4.5$ V | 16 | 4 | - | 20 | - | 24 | - | ns | |
| | | | $V_{CC} = 6.0$ V | 14 | 3 | - | 17 | - | 20 | - | ns |
| | | | \overline{CE} to CP and CP to \overline{CE} ; see Figure 10 | | | | | | | | |
| | | | $V_{CC} = 2.0$ V | 80 | 17 | - | 100 | - | 120 | - | ns |
| | | | $V_{CC} = 4.5$ V | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | | $V_{CC} = 6.0$ V | 14 | 5 | - | 17 | - | 20 | - | ns |
| | | | Dn to \overline{PL} ; see Figure 11 | | | | | | | | |
| | | | $V_{CC} = 2.0$ V | 80 | 22 | - | 100 | - | 120 | - | ns |
| | | | $V_{CC} = 4.5$ V | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | | $V_{CC} = 6.0$ V | 14 | 6 | - | 17 | - | 20 | - | ns |
| t_h | hold time | DS to CP, \overline{CE} and Dn to \overline{PL} ; see Figure 10 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 5 | 6 | - | 5 | - | 5 | - | ns | |
| | | $V_{CC} = 4.5$ V | 5 | 2 | - | 5 | - | 5 | - | ns | |
| | | | $V_{CC} = 6.0$ V | 5 | 2 | - | 5 | - | 5 | - | ns |
| | | | \overline{CE} to CP and CP to \overline{CE} ; see Figure 10 | | | | | | | | |
| | | | $V_{CC} = 2.0$ V | 5 | -17 | - | 5 | - | 5 | - | ns |
| | | | $V_{CC} = 4.5$ V | 5 | -6 | - | 5 | - | 5 | - | ns |
| | | $V_{CC} = 6.0$ V | 5 | -5 | - | 5 | - | 5 | - | ns | |
| f_{max} | maximum frequency | CP input; see Figure 7 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 6 | 17 | - | 5 | - | 4 | - | MHz | |
| | | $V_{CC} = 4.5$ V | 30 | 51 | - | 24 | - | 20 | - | MHz | |
| | | $V_{CC} = 6.0$ V | 35 | 61 | - | 28 | - | 24 | - | MHz | |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 56 | - | - | - | - | - | MHz | |
| C_{PD} | power dissipation capacitance | per package; $V_I = \text{GND to } V_{CC}$ | [3] | - | 35 | - | - | - | - | pF | |

Table 7. Dynamic characteristics ...continued
 GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 12](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---------------------------------|-------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HCT165 | | | | | | | | | | |
| t_{pd} | propagation delay | \overline{CE} , CP to Q7, $\overline{Q7}$; see Figure 7 [1] | - | 17 | 34 | - | 43 | - | 51 | ns |
| | | $V_{CC} = 4.5$ V | - | 17 | 34 | - | 43 | - | 51 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 14 | - | - | - | - | - | ns |
| | | \overline{PL} to Q7, $\overline{Q7}$; see Figure 8 | - | 20 | 40 | - | 50 | - | 60 | ns |
| | | $V_{CC} = 4.5$ V | - | 20 | 40 | - | 50 | - | 60 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 17 | - | - | - | - | - | ns |
| | | D7 to Q7, $\overline{Q7}$; see Figure 9 | - | 14 | 28 | - | 35 | - | 42 | ns |
| $V_{CC} = 4.5$ V | - | 14 | 28 | - | 35 | - | 42 | ns | | |
| $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 11 | - | - | - | - | - | ns | | |
| t_t | transition time | Q7, $\overline{Q7}$ output; see Figure 7 [2] | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC} = 4.5$ V | - | 7 | 15 | - | 19 | - | 22 | ns |
| t_W | pulse width | CP input; see Figure 7 | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | $V_{CC} = 4.5$ V | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | \overline{PL} input; see Figure 8 | 20 | 9 | - | 25 | - | 30 | - | ns |
| $V_{CC} = 4.5$ V | 20 | 9 | - | 25 | - | 30 | - | ns | | |
| t_{rec} | recovery time | \overline{PL} to CP, \overline{CE} ; see Figure 8 | 20 | 8 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 4.5$ V | 20 | 8 | - | 25 | - | 30 | - | ns |
| t_{su} | set-up time | DS to CP, \overline{CE} ; see Figure 10 | 20 | 2 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 4.5$ V | 20 | 2 | - | 25 | - | 30 | - | ns |
| | | \overline{CE} to CP and CP to \overline{CE} ; see Figure 10 | 20 | 7 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 4.5$ V | 20 | 7 | - | 25 | - | 30 | - | ns |
| | | Dn to \overline{PL} ; see Figure 11 | 20 | 10 | - | 25 | - | 30 | - | ns |
| $V_{CC} = 4.5$ V | 20 | 10 | - | 25 | - | 30 | - | ns | | |
| t_h | hold time | DS to CP, \overline{CE} and Dn to \overline{PL} ; see Figure 10 | 7 | -1 | - | 9 | - | 11 | - | ns |
| | | $V_{CC} = 4.5$ V | 7 | -1 | - | 9 | - | 11 | - | ns |
| | | \overline{CE} to CP and CP to \overline{CE} ; see Figure 10 | 0 | -7 | - | 0 | - | 0 | - | ns |
| $V_{CC} = 4.5$ V | 0 | -7 | - | 0 | - | 0 | - | ns | | |
| f_{max} | maximum frequency | CP input; see Figure 7 | 26 | 44 | - | 21 | - | 17 | - | MHz |
| | | $V_{CC} = 4.5$ V | 26 | 44 | - | 21 | - | 17 | - | MHz |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 48 | - | - | - | - | - | MHz |

Table 7. Dynamic characteristics ...continued

GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 12](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| C_{PD} | power dissipation capacitance | per package; $V_I = GND$ to $V_{CC} - 1.5$ V | [3] | - | 35 | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

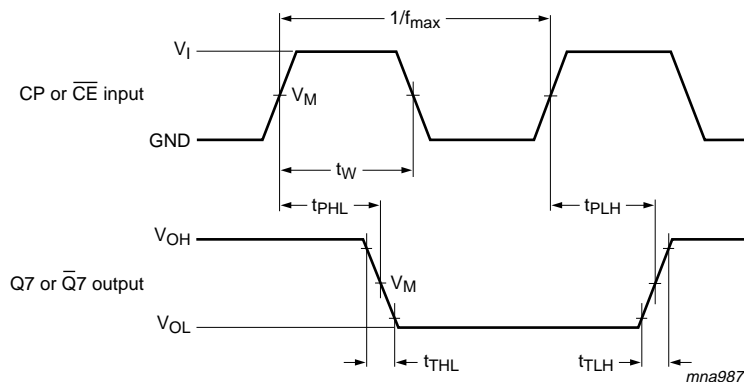
f_o = output frequency in MHz;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

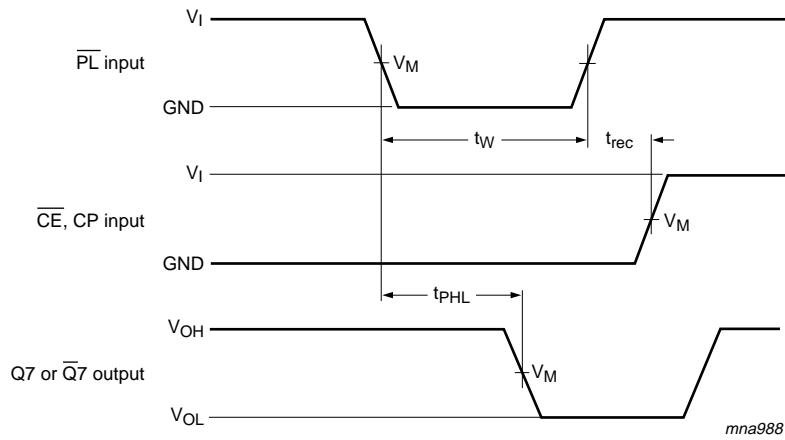
12. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

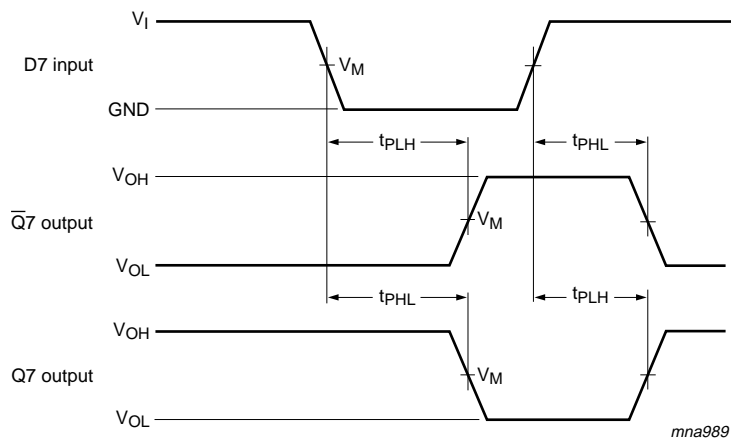
Fig 7. The clock (CP) or clock enable (\overline{CE}) to output (Q_7 or $\overline{Q_7}$) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

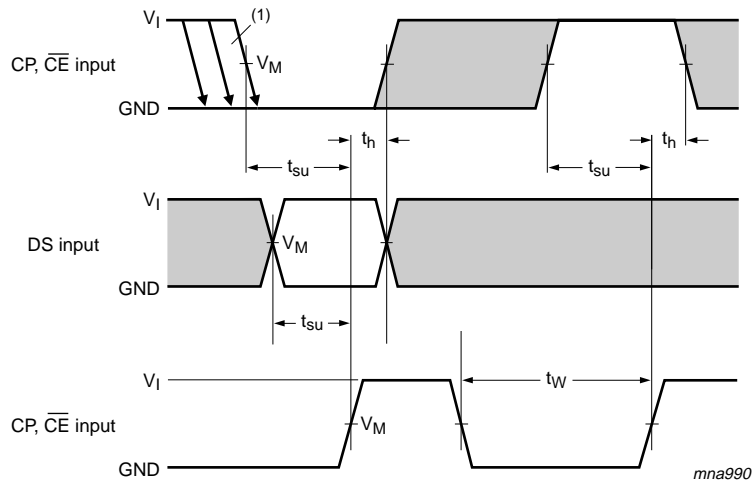
Fig 8. The parallel load ($\overline{\text{PL}}$) pulse width, the parallel load to output (Q7 or $\overline{\text{Q7}}$) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{\text{CE}}$) recovery time



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. The data input (D7) to output (Q7 or $\overline{\text{Q7}}$) propagation delays when $\overline{\text{PL}}$ is LOW

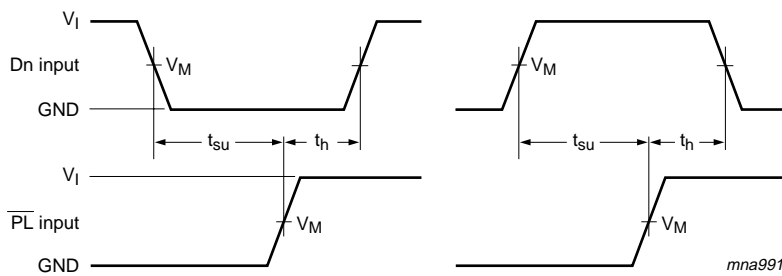


The shaded areas indicate when the input is permitted to change for predictable output performance. Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

- (1) \overline{CE} may change only from HIGH-to-LOW while CP is LOW, see [Section 1](#).

Fig 10. The set-up and hold times from the serial data input (DS) to the clock (CP) and clock enable (\overline{CE}) inputs, from the clock enable input (\overline{CE}) to the clock input (CP) and from the clock input (CP) to the clock enable input (\overline{CE})



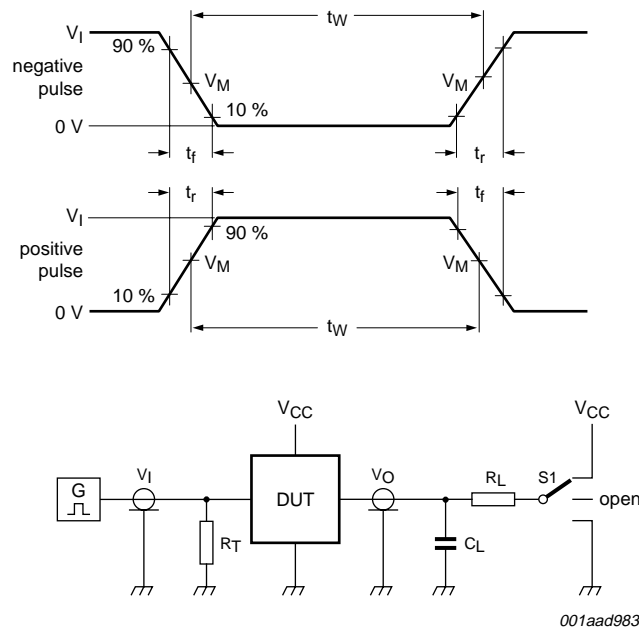
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 11. The set-up and hold times from the data inputs (Dn) to the parallel load input (\overline{PL})

Table 8. Measurement points

| Type | Input | | Output |
|----------|----------|-------------|-------------|
| | V_I | V_M | V_M |
| 74HC165 | V_{CC} | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT165 | 3 V | 1.3 V | 1.3 V |



Test data is given in [Table 9](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch

Fig 12. Test circuit for measuring switching times

Table 9. Test data

| Type | Input | | Load | | | S1 position |
|----------|----------|------------|--------------|--------------|--------------------|-------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | |
| 74HC165 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open | |
| 74HCT165 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open | |

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

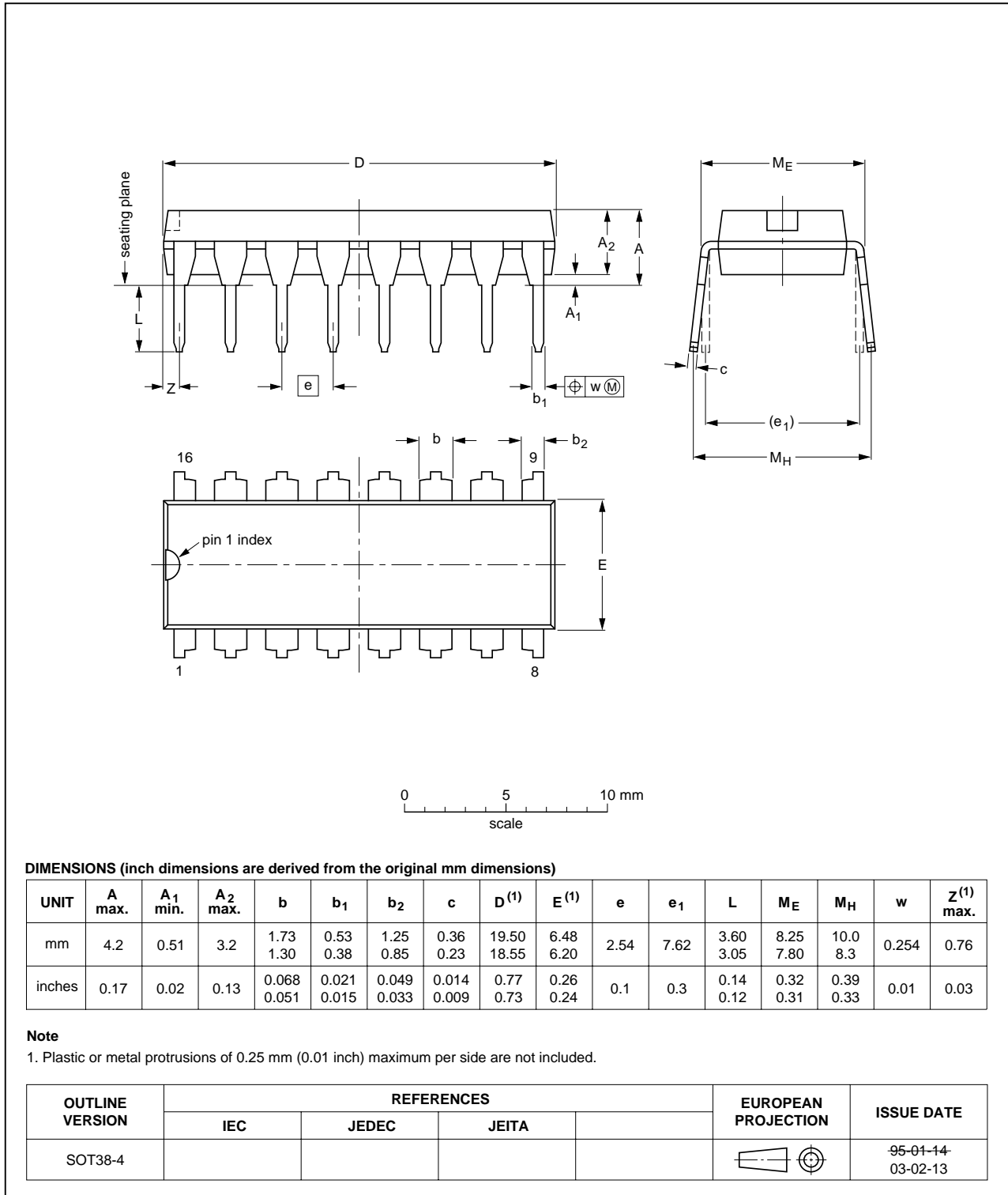


Fig 13. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

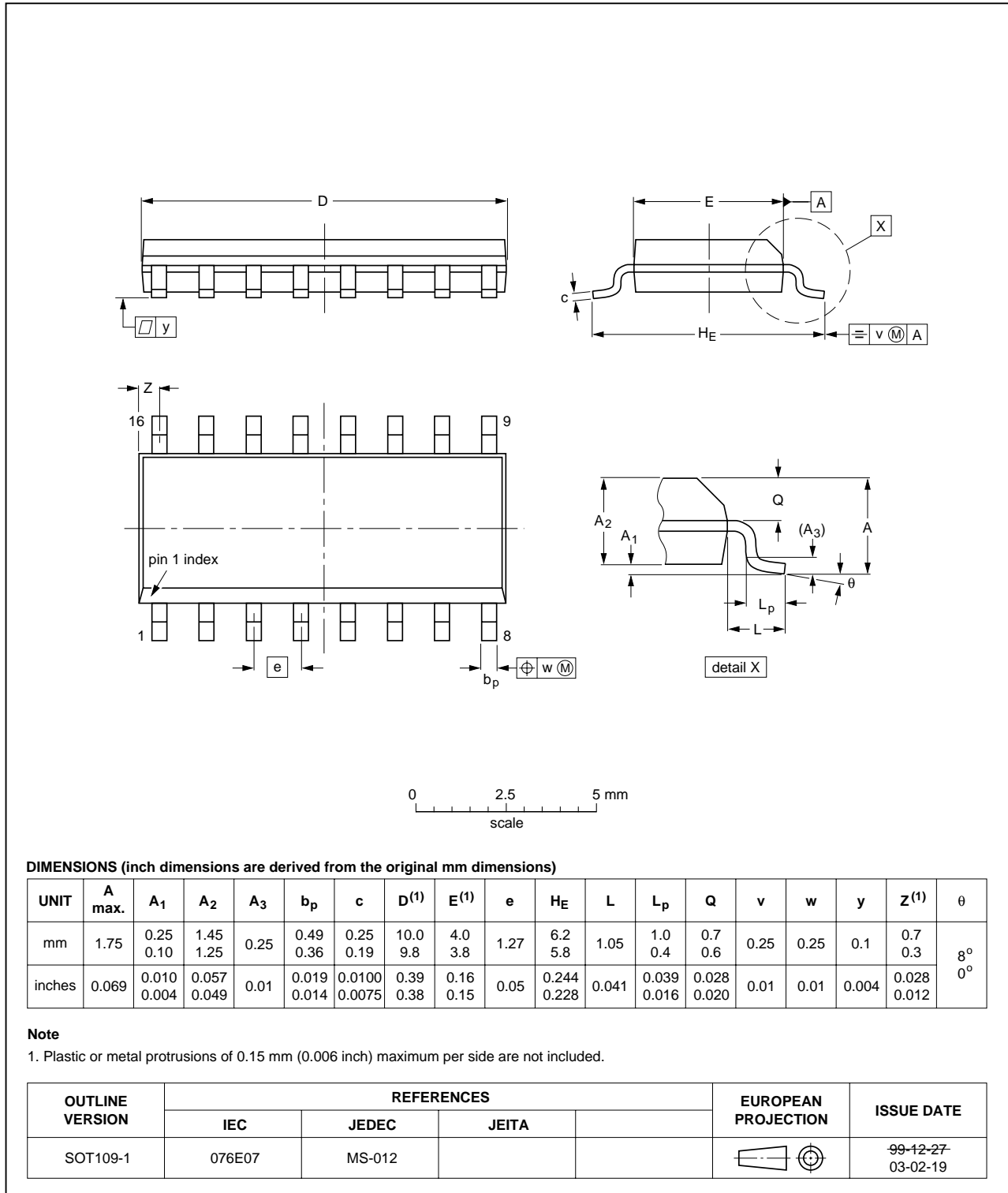


Fig 14. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

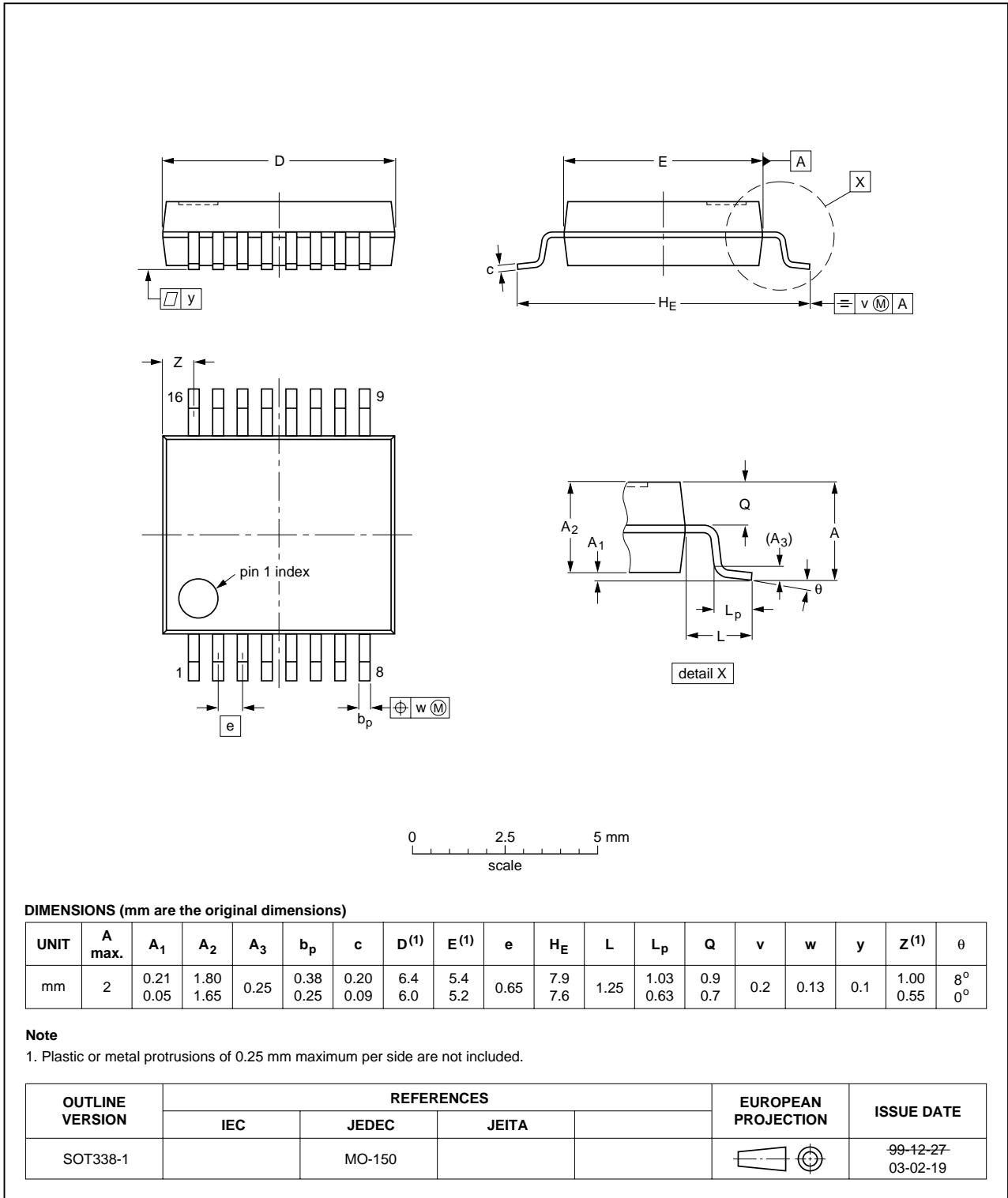


Fig 15. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

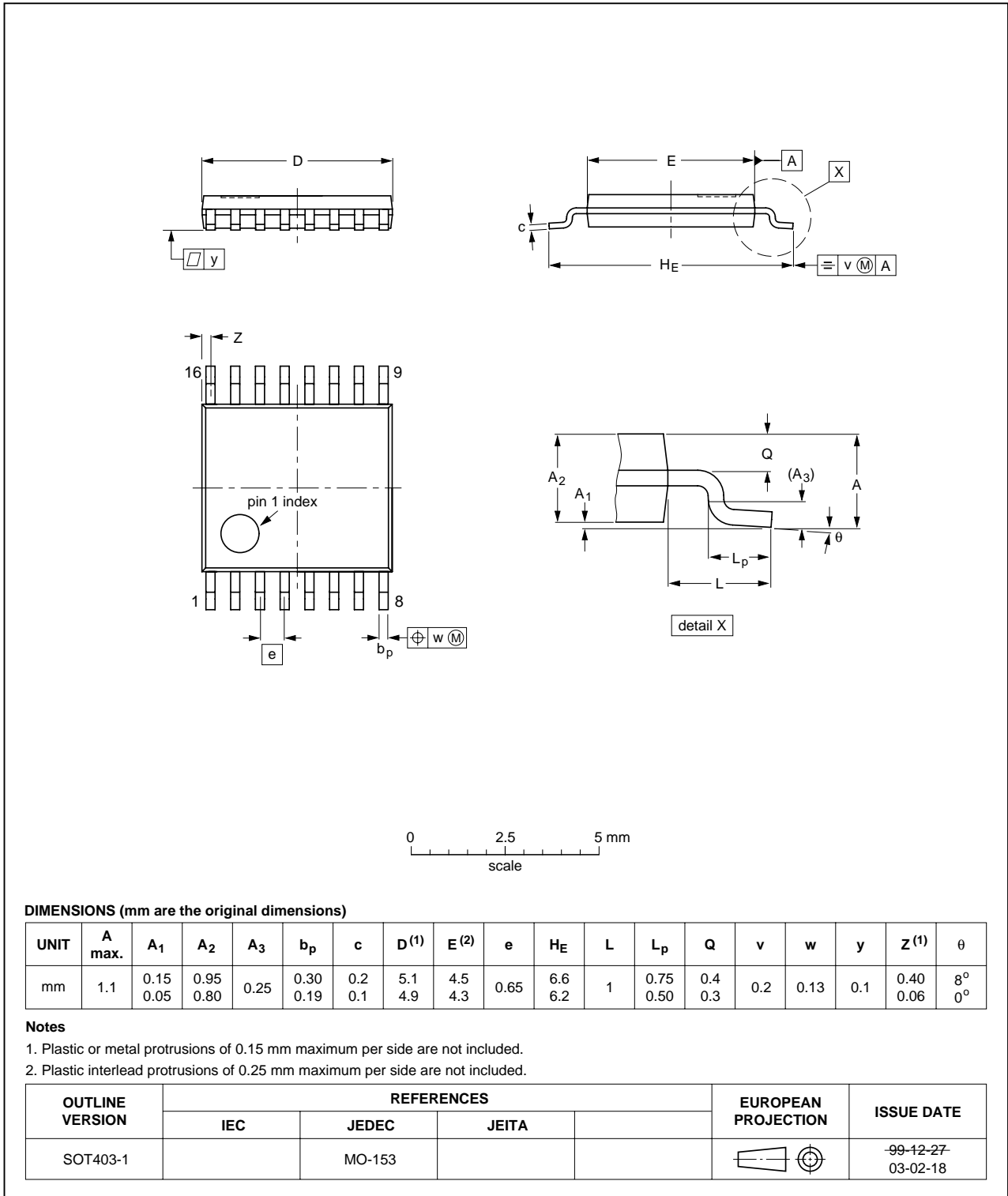


Fig 16. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

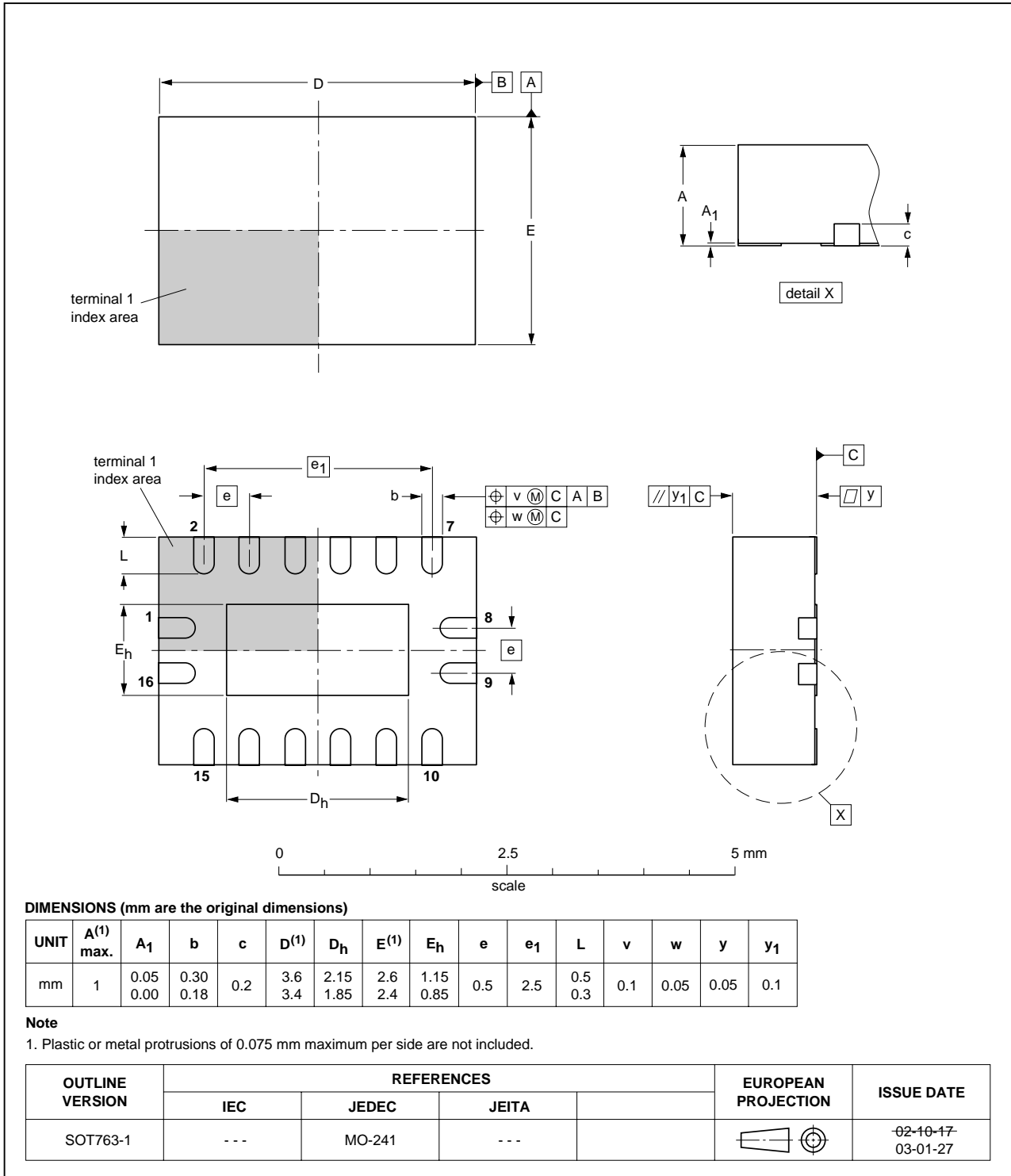


Fig 17. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

15. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--|-----------------------|---------------|-------------------|
| 74HC_HCT165_3 | 20080314 | Product data sheet | - | 74HC_HCT165_CNV_2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Package SOT763-1 (DHVQFN16) added to Section 4 “Ordering information” and Section 13 “Package outline”. Family data added, see Section 10 “Static characteristics” | | | |
| 74HC_HCT165_CNV_2 | December 1990 | Product specification | - | - |

16. Legal information

16.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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