



ELECTRONICS, INC.  
 44 FARRAND STREET  
 BLOOMFIELD, NJ 07003  
 (973) 748-5089  
<http://www.nteinc.com>

## NTE74LS85 Integrated Circuit TTL – 4–Bit Magnitude Comparator

**Description:**

The NTE74LS85 is a 4-bit magnitude comparator in a 16-Lead plastic DIP type package that performs comparison of straight binary and straight BCD (8–4–2–1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. This device is fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have low-level voltages applied to the A > B and A < B inputs. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words.

**Absolute Maximum Ratings:** (Note 1)

Supply Voltage,  $V_{CC}$  ..... 7V  
 Input Voltage,  $V_{IN}$  ..... 7V  
 Operating Temperature Range,  $T_A$  ..... 0°C to +70°C  
 Storage Temperature Range,  $T_{stg}$  ..... –65°C to +150°C

Note 1. Voltage values are with respect to network ground terminal.

**Recommended Operating Conditions:**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.75	5.0	5.25	V
High-Level Output Current	$I_{OH}$	–	–	–400	$\mu A$
Low-Level Output Current	$I_{OL}$	–	–	8	mA
Operating Temperature Range	$T_A$	0	–	+70	°C

### Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
High Level Input Voltage	$V_{IH}$		2	–	–	V	
Low Level Input Voltage	$V_{IL}$		–	–	0.7	V	
Input Clamp Voltage	$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$	–	–	-1.5	V	
High Level Output Voltage	$V_{OH}$	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = \text{MAX}, I_{OH} = -400\mu\text{A}$	2.7	3.4	–	V	
Low Level Output Voltage	$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = \text{MAX}$	$I_{OL} = 4\text{mA}$	–	0.25	0.4	V
			$I_{OL} = 8\text{mA}$	–	0.35	0.5	V
Input Current A < B, A > B Inputs	$I_I$	$V_{CC} = \text{MAX}, V_I = 7\text{V}$	–	–	0.1	mA	
			–	–	0.3	mA	
High Level Input Current A < B, A > B Inputs	$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$	–	–	20	$\mu\text{A}$	
			–	–	60	$\mu\text{A}$	
Low Level Input Current A < B, A > B Inputs	$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	–	–	-0.4	mA	
			–	–	-1.2	mA	
Short-Circuit Output Current	$I_{OS}$	$V_{CC} = \text{MAX}, \text{Note 4}$	-20	–	-100	mA	
Supply Current	$I_{CC}$	$V_{CC} = \text{MAX}, \text{Note 5}$	–	10.4	20	mA	

Note 2. For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at  $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ .

Note 4. Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

Note 5.  $I_{CC}$  is measured with outputs open, A = B grounded, and all other inputs at 4.5V.

### Switching Characteristics: ( $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	From Input	To Output	Number of Gate Levels	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time	$t_{PLH}$	Any A or B Data Input	A < B, A > B	1	$R_L = 2\text{k}\Omega,$ $C_L = 15\text{pF}$	–	14	–	ns
				2		–	19	–	ns
			3	–		24	36	ns	
			4	–		27	45	ns	
Propagation Delay Time	$t_{PHL}$	Any A or B Data Input	A < B, A > B	1		–	11	–	ns
				2		–	15	–	ns
			3	–		20	30	ns	
			4	–		22	45	ns	
Propagation Delay Time	$t_{PLH}$	A < B or A = B	A > B	1	–	14	22	ns	
Propagation Delay Time	$t_{PHL}$	A < B or A = B	A > B	1	–	11	17	ns	
Propagation Delay Time	$t_{PLH}$	A = B	A = B	2	–	13	20	ns	
Propagation Delay Time	$t_{PHL}$	A = B	A = B	2	–	13	26	ns	
Propagation Delay Time	$t_{PLH}$	A > B or A = B	A < B	1	–	14	22	ns	
Propagation Delay Time	$t_{PHL}$	A > B or A = B	A < B	1	–	11	17	ns	

**Function Table:**

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A2 < B2	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A2 = B2	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A2 = B2	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A2 = B2	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A2 = B2	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A2 = B2	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A2 = B2	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A2 = B2	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A2 = B2	A0 = B0	L	L	L	H	H	L

H = HIGH Level

L = LOW Level

X = Irrelevant

**Pin Connection Diagram**



