TEXAS INSTRUMENTS

ADS8528, ADS8548, ADS8568

SBAS543C – AUGUST 2011 – REVISED FEBRUARY 2016

ADS85x8 12-, 14-, and 16-Bit, 8-Channel, Simultaneous Sampling ADCs

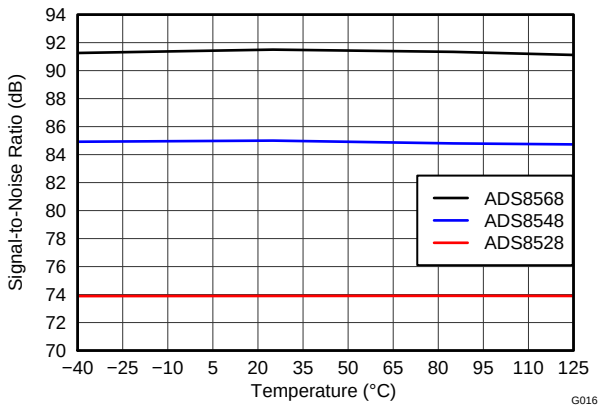
1 Features

- Family of 12-, 14-, and 16-Bit, Pin- and Software-Compatible ADCs
- Maximum Data Rate per Channel:
  - ADS8528: 650 kSPS (PAR) or 480 kSPS (SER)
  - ADS8548: 600 kSPS (PAR) or 450 kSPS (SER)
  - ADS8568: 510 kSPS (PAR) or 400 kSPS (SER)
- Excellent AC Performance:
  - Signal-to-Noise Ratio: ADS8528: 73.9 dB, ADS8548: 85 dB, ADS8568: 91.5 dB
  - Total Harmonic Distortion: ADS8528: –89 dB, ADS8548: –91 dB, ADS8568: –94 dB
- Programmable, Buffered Internal Reference: 0.5 V–2.5 V or 0.5 V–3.0 V Supports Input Voltage Ranges up to ±12 V
- Selectable Parallel or Serial Interface
- Scalable Low-Power Operation Using Auto-Sleep Mode: Only 32 mW at 10 kSPS
- Fully Specified Over Extended Industrial Temperature Range

2 Applications

- Protection Relays
- Power Quality Measurement
- Multi-Axis Motor Controls
- Programmable Logic Controllers
- Industrial Data Acquisition

SNR vs Temperature



3 Description

The ADS85x8 contain eight low-power, 12-, 14-, or 16-bit, successive approximation register (SAR)-based analog-to-digital converters (ADCs) with true bipolar inputs. These channels are grouped in four pairs, thus allowing simultaneous high-speed signal acquisition of up to 650 kSPS.

The devices support selectable parallel or serial interface with daisy-chain capability. The programmable reference allows handling of analog input signals with amplitudes up to ±12 V.

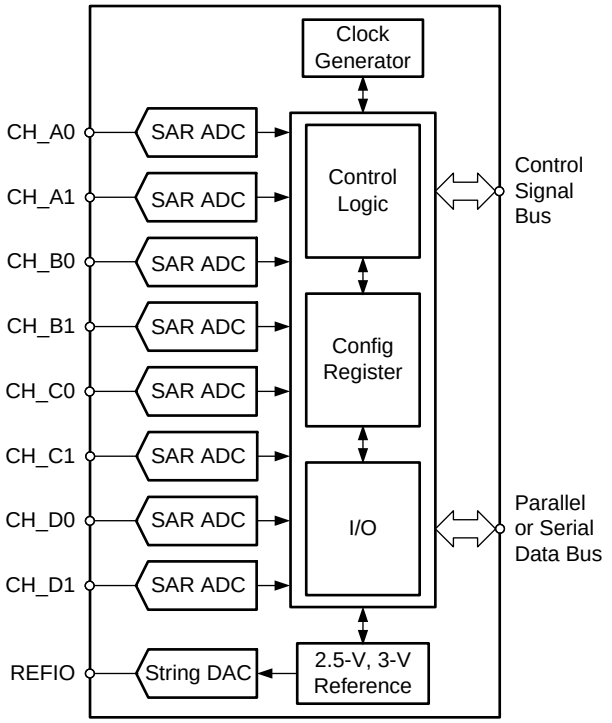
The ADS85x8 family supports an auto-sleep mode for minimum power dissipation and is available in both 64-pin VQFN and LQFP packages. The entire family is specified over a temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS85x8	VQFN (64)	9.00 mm × 9.00 mm
	LQFP (64)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2015) to Revision C — **Page**

- Changed Figure 45: changed capacitor values from 820 nF to 820 pF ... 42

Changes from Revision A (October 2011) to Revision B — **Page**

- Added *ESD Ratings* table, *Recommended Operating Conditions* table, *Feature Description* section, *Device Functional Modes* section, *Register Maps* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed title of *Device Comparison Table*, deleted footnote 1 ... 4
- Added *Storage temperature* parameter to *Absolute Maximum Ratings* table ... 9
- Changed *Clock cycles per conversion* to be a single parameter instead of part of t_{CONV} parameter in *Serial Interface Timing Requirements* table ... 16
- Changed t_{BUFS} parameter in *Serial Interface Timing Requirements* table ... 16
- Added footnote 3 to *Serial Interface Timing Requirements* table ... 16
- Changed *Clock cycles per conversion* to be a single parameter instead of part of t_{CONV} parameter in *Parallel Interface Timing Requirements (Read Access)* table ... 17
- Changed t_{BUCS} parameter in *Parallel Interface Timing Requirements (Read Access)* table ... 17
- Added footnote 3 to *Parallel Interface Timing Requirements (Read Access)* table ... 17
- Changed *Data Readout and BUSY/INT Signal* section ... 30
- Added *Sequential Operation* section ... 31
- Changed description of initiating a new conversion in *Reset and Power-Down Modes* section ... 38

Changes from Original (August 2011) to Revision A **Page**

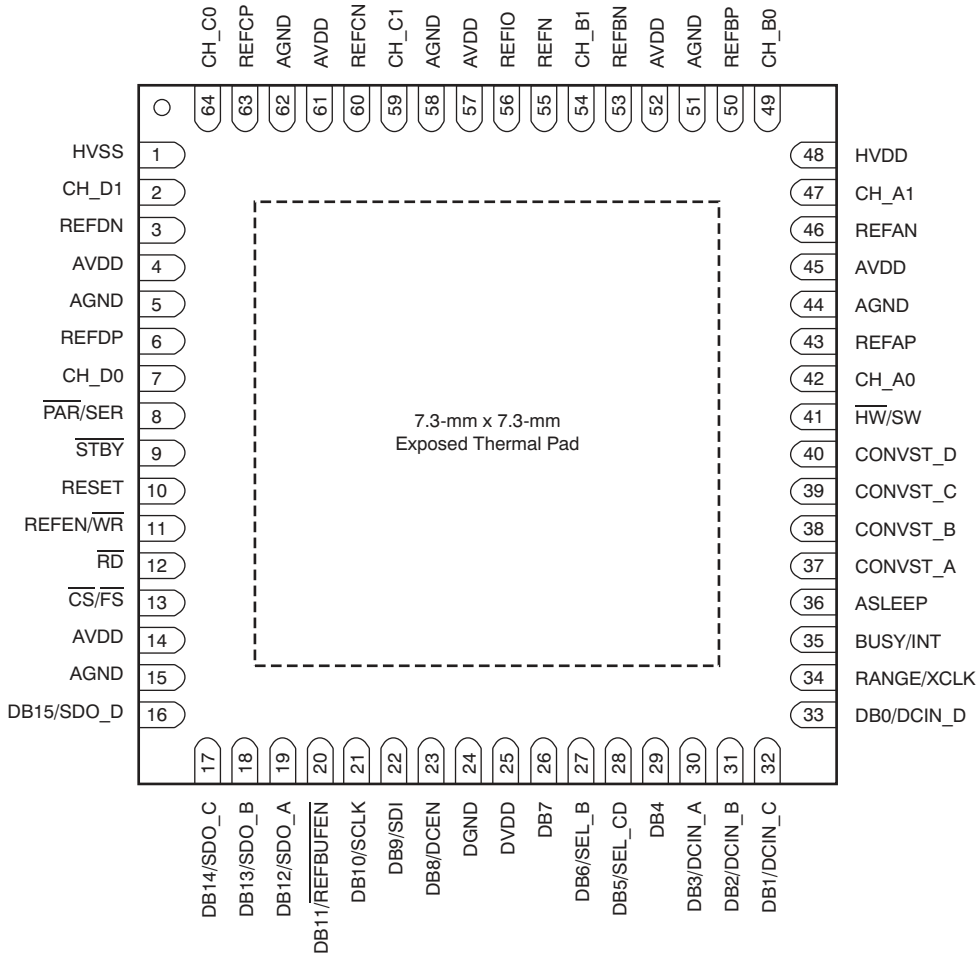
- Deleted INL column from Family/Ordering Information table 4
- Changed DC Accuracy, *INL* parameter in ADS8568 Electical Chatacteristics table..... 15

5 Device Comparison Table

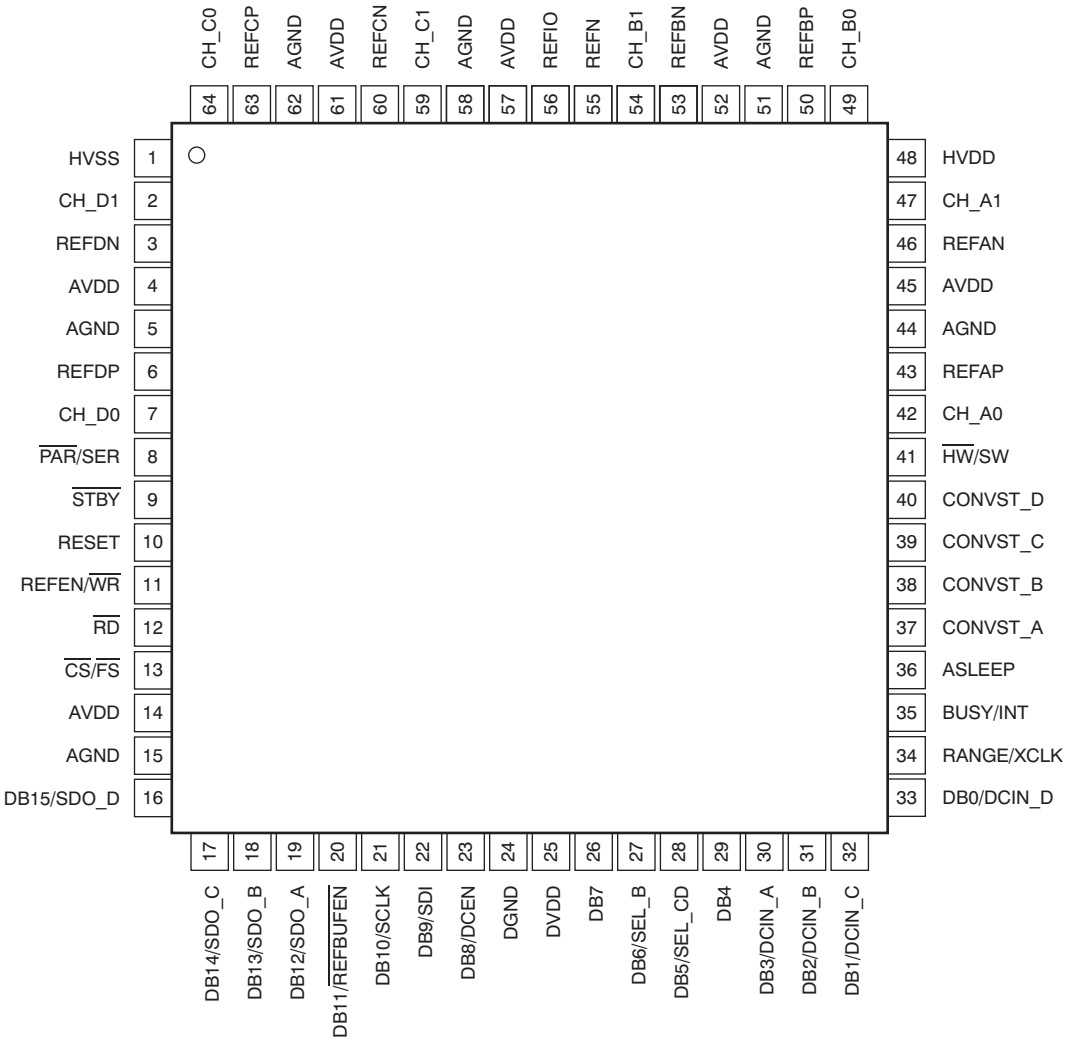
PRODUCT	RESOLUTION (Bits)	MAXIMUM DATA RATE: PAR, SER (kSPS per Channel)	SNR (dB, Typ)	THD (dB, Typ)
ADS8528	12	650, 480	73.9	–89
ADS8548	14	600, 450	85	–91
ADS8568	16	510, 400	91.5	–94

6 Pin Configuration and Functions

RGC Package
64-Pin VQFN
Top View



PM Package
64-Pin LQFP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION	
NAME	NO.		PARALLEL INTERFACE ($\overline{PAR}$/SER = 0)	SERIAL INTERFACE ($\overline{PAR}$/SER = 1)
AGND	5, 15, 44, 51, 58, 62	P	Analog ground; connect to the analog ground plane.	
ASLEEP	36	DI	Auto-sleep enable input. When low, the device operates in normal mode. When high, the device functions in auto-sleep mode where the hold mode and the actual conversion is activated six conversion clock (t_{CCLK}) cycles after issuing a conversion start using a CONVST_x. This mode is recommended to save power if the device runs at a lower data rate; see the *Reset and Power-Down Modes* section for more details.	
AVDD	4, 14, 45, 52, 57, 61	P	Analog power supply. Decouple according to the *Power Supply Recommendations* section.	
BUSY/INT	35	DO	When CONFIG bit C27 = 0 (BUSY/INT), this pin is a converter busy status output. This pin transitions high when a conversion is started and transitions low for a single conversion clock cycle (t_{CCLK}) whenever a channel pair conversion is completed and stays low when the conversion of the last channel pair completes. When bit C27 = 1 (BUSY/INT in CONFIG), this pin is an interrupt output. This pin transitions high after a conversion completes and remains high until the next read access. This mode can only be used if all eight channels are sampled simultaneously (all CONVST_x tied together). The polarity of the BUSY/INT output can be changed using the C26 bit (BUSY L/H) in the Configuration register.	
CH_A0	42	AI	Analog input of channel A0; channel A is the master channel pair that is always active. The input voltage range is controlled by the RANGE pin in hardware mode or by Configuration register (CONFIG) bit C24 (RANGE_A) in software mode. In cases where channel pairs of the device are used at different data rates, channel pair A must always run at the highest data rate.	
CH_A1	47	AI	Analog input of channel A1; channel A is the master channel pair that is always active. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C24 (RANGE_A) in software mode. In cases where channel pairs of the device are used at different data rates, channel pair A must always run at the highest data rate.	
CH_B0	49	AI	Analog input of channel B0. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C23 (RANGE_B) in software mode.	
CH_B1	54	AI	Analog input of channel B1. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C23 (RANGE_B) in software mode.	
CH_C0	64	AI	Analog input of channel C0. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C21 (RANGE_C) in software mode.	
CH_C1	59	AI	Analog input of channel C1. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C21 (RANGE_C) in software mode.	
CH_D0	7	AI	Analog input of channel D0.The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C19 (RANGE_D) in software mode. This pin can be powered down using CONFIG bit C18 (PD_D) in software mode.	
CH_D1	2	AI	Analog input of channel D1.The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C19 (RANGE_D) in software mode. This pin can be powered down using CONFIG bit C18 (PD_D) in software mode.	
CONVST_A	37	DI	Conversion start of channel pair A. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_A[1:0]. This signal resets the internal channel state machine that causes the data output to start with conversion results of channel A0 with the next read access.	
CONVST_B	38	DI	Conversion start of channel pair B. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_B[1:0].	
CONVST_C	39	DI	Conversion start of channel pair C. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_C[1:0].	
CONVST_D	40	DI	Conversion start of channel pair D. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_D[1:0].	
$\overline{CS}$/$\overline{FS}$	13	DI, DI	Chip-select input. When low, the parallel interface is enabled. When high, the interface is disabled.	Frame synchronization. The $\overline{FS}$ falling edge controls the frame transfer.
DB0/DCIN_D	33	DIO, DI	Data bit 0 (LSB) input/output	When DCEN = 1 and SEL_CD = 1, this pin is the daisy-chain data input for SDO_D of the previous device in the chain. When DCEN = 0, connect to DGND.
DB1/DCIN_C	32	DIO, DI	Data bit 1 input/output	When DCEN = 1 and SEL_CD = 1, this pin is the daisy-chain data input for SDO_C of the previous device in the chain. When DCEN = 0, connect to DGND.
DB2/DCIN_B	31	DIO, DI	Data bit 2 input/output	When DCEN = 1 and SEL_B = 1, this pin is the daisy-chain data input for SDO_B of the previous device in the chain. When DCEN = 0, connect to DGND.
DB3/DCIN_A	30	DIO, DI	Data bit 3 input/output	When DCEN = 1, this pin is the daisy-chain data input for SDO_A of the previous device in the chain. When DCEN = 0, connect to DGND.

(1) AI = analog input; AIO = analog input/output; DI = digital input; DIO = digital input/output; DO = digital output; and P = power supply.

Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION	
NAME	NO.		PARALLEL INTERFACE ($\overline{PAR}$/SER = 0)	SERIAL INTERFACE ($\overline{PAR}$/SER = 1)
DB4	29	DIO	Data bit 4 input/output	Connect to DGND
DB5/SEL_CD	28	DIO, DI	Data bit 5 input/output	Select SDO_C and SDO_D input. When high, data from channel pair C are available on SDO_C and data from channel pair D are available on SDO_D. When low and SEL_B = 1, data from channel pairs A and C are available on SDO_A and data from channel pairs B and D are available on SDO_B. When low and SEL_B = 0, data from all eight channels are available on SDO_A.
DB6/SEL_B	27	DIO, DI	Data bit 6 input/output	Select SDO_B input. When low, SDO_B is disabled and data from all eight channels are only available through SDO_A. When high and SEL_CD = 0, data from channel pairs B and D are available on SDO_B. When SEL_CD = 1, data from channel pair B are available on SDO_B.
DB7	26	DIO	Data bit 7 input/output	Must be connected to DGND
DB8/DCEN	23	DIO, DI	Data bit 8 input/output	Daisy-chain enable input. When high, DB[3:0] serve as daisy-chain inputs DCIN_[A:D]. If daisy-chain mode is not used, connect to DGND.
DB9/SDI	22	DIO, DI	Data bit 9 input/output	Hardware mode ($\overline{HW}$/SW = 0): connect to DGND. Software mode ($\overline{HW}$/SW = 1): serial data input.
DB10/SCLK	21	DIO, DI	Data bit 10 input/output	Serial interface clock input.
DB11/$\overline{REFBUFEN}$	20	DIO, DI	Data bit 11 input/output. Output is MSB for the ADS8528.	Hardware mode ($\overline{HW}$/SW = 0): reference buffer enable input. When low, all internal reference buffers are enabled (mandatory if internal reference is used). When high, all reference buffers are disabled. Software mode ($\overline{HW}$/SW = 1): connect to DGND or DVDD. The internal reference buffers are controlled by CONFIG bit C14 ($\overline{REFBUFEN}$).
DB12/SDO_A	19	DIO, DO	Data bit 12 input/output. Output is sign extension for the ADS8528.	Data output for channel pair A. When SEL_CD = 0, data from channel pair C are also available on this output. When SEL_CD = 0 and SEL_B = 0, SDO_A functions as single data output for all eight channels.
DB13/SDO_B	18	DIO, DO	Data bit 13 input/output. Output is sign extension for the ADS8528 and MSB for the ADS8548.	When SEL_B = 1, this pin is the data output for channel pair B. When SEL_B = 0, tie this pin to DGND. When SEL_CD = 0, data from channel pair D are also available on this output.
DB14/SDO_C	17	DIO, DO	Data bit 14 input/output. Output is sign extension for the ADS8528 and ADS8548.	When SEL_CD = 1, this pin is the data output for channel pair C. When SEL_CD = 0, tie this pin to DGND.
DB15/SDO_D	16	DIO, DO	Data bit 15 (MSB) input/output. Output is sign extension for the ADS8528 and ADS8548.	When SEL_CD = 1, this pin is the data output for channel pair D. When SEL_CD = 0, tie this pin to DGND.
DGND	24	P	Buffer I/O ground, connect to digital ground plane	
DVDD	25	P	Buffer I/O supply, connect to digital supply. Decouple according to the *Power Supply Recommendations* section.	
HVDD	48	P	Positive supply voltage for the analog inputs. Decouple according to the *Power Supply Recommendations* section.	
HVSS	1	P	Negative supply voltage for the analog inputs. Decouple according to the *Power Supply Recommendations* section.	
$\overline{HW}$/SW	41	DI	Mode selection input. When low, hardware mode is selected and the device functions according to the settings of the external pins. When high, software mode is selected and the device is configured by writing to the Configuration register (CONFIG).	
$\overline{PAR}$/SER	8	DI	Interface mode selection input. When low, the parallel interface is selected. When high, the serial interface is enabled.	
RANGE/XCLK	34	DI/DI/DO	Hardware mode ($\overline{HW}$/SW = 0): analog input voltage range select input. When low, the analog input voltage range is ±4 VREF. When high, the analog input voltage range is ±2 VREF. Software mode ($\overline{HW}$/SW = 1): this pin is an external conversion clock input if CONFIG bit C29 = 1 (CLKSEL); or an internal conversion clock output if CONFIG bit C28 = 1 (CLKOUT_EN). If this pin is not used, connect to DGND.	
$\overline{RD}$	12	DI/DI	Read data input. When low, the parallel data output is enabled (if $\overline{CS}$ = 0). When high, the data output is disabled.	Must be connected to DGND.

Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION	
NAME	NO.		PARALLEL INTERFACE ($\overline{PAR}$/SER = 0)	SERIAL INTERFACE ($\overline{PAR}$/SER = 1)
REFAN	46	AI	Decoupling capacitor input for reference of channel pair A. Connect to the decoupling capacitor and AGND according to the *Power Supply Recommendations* section.	
REFAP	43	AI	Decoupling capacitor input for reference of channel pair A. Connect to the decoupling capacitor according to the *Power Supply Recommendations* section.	
REFBN	53	AI	Decoupling capacitor input for reference of channel pair B. Connect to the decoupling capacitor and AGND according to the *Power Supply Recommendations* section.	
REFBP	50	AI	Decoupling capacitor input for reference of channel pair B. Connect to the decoupling capacitor according to the *Power Supply Recommendations* section.	
REFCN	60	AI	Decoupling capacitor input for reference of channel pair C. Connect to the decoupling capacitor and AGND according to the *Power Supply Recommendations* section.	
REFCP	63	AI	Decoupling capacitor input for reference of channel pair C. Connect to the decoupling capacitor according to the *Power Supply Recommendations* section.	
REFDN	3	AI	Decoupling capacitor input for reference of channel pair D. Connect to the decoupling capacitor and AGND according to the *Power Supply Recommendations* section.	
REFDP	6	AI	Decoupling capacitor input for the channel pair D reference. Connect to the decoupling capacitor according to the *Power Supply Recommendations* section.	
REFEN/$\overline{WR}$	11	DI/DI	Hardware mode ($\overline{HW}$/SW = 0): internal reference enable input. When high, the internal reference is enabled (the reference buffers are also enabled). When low, the internal reference is disabled and an external reference is applied at REFIO. Software mode ($\overline{HW}$/SW = 1): write input. The parallel data input is enabled when $\overline{CS}$ and $\overline{WR}$ are low. The internal reference is enabled by CONFIG bit C15 (REFEN).	Hardware mode ($\overline{HW}$/SW = 0): internal reference enable input. When high, the internal reference is enabled (the reference buffers are also enabled). When low, the internal reference is disabled and an external reference is applied at REFIO. Software mode ($\overline{HW}$/SW = 1): connect to DGND or DVDD. The internal reference is enabled by CONFIG bit C15 (REFEN).
REFIO	56	AIO	Reference voltage input/output. The internal reference is enabled by the REFEN/$\overline{WR}$ pin in hardware mode or by CONFIG bit C15 (REFEN) in software mode. The output value is controlled by the internal digital-to-analog converter (DAC), CONFIG bits C[9:0]. Connect to a decoupling capacitor according to the *Power Supply Recommendations* section.	
REFN	55	AI	Negative reference input/output pin. Connect to a decoupling capacitor and AGND according to the *Power Supply Recommendations* section.	
RESET	10	DI	Reset input, active high. This pin aborts any ongoing conversions and resets the internal Configuration register (CONFIG) to 000003FFh. A valid reset pulse must be at least 50 ns long.	
$\overline{STBY}$	9	DI	Hardware mode ($\overline{HW}$/SW = 0): standby mode input. When low, the entire device is powered down (including the internal conversion clock source and reference). When high, the device operates in normal mode. Software mode ($\overline{HW}$/SW = 1): connect to DGND or DVDD. The standby mode can be activated using CONFIG bit C25 ($\overline{STBY}$).	

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	HVDD to AGND	–0.3	18	V
	HVSS to AGND	–18	0.3	
	AVDD to AGND	–0.3	6	
	DVDD to DGND	–0.3	6	
Analog input voltage		HVSS – 0.3	HVDD + 0.3	V
Reference input voltage with respect to AGND		AGND – 0.3	AVDD + 0.3	V
Digital input voltage with respect to DGND		DGND – 0.3	DVDD + 0.3	V
Ground voltage difference AGND to DGND			±0.3	V
Input current to all pins except supply			±10	mA
Maximum virtual junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage	4.5	5.0	5.5	V
DVDD	Buffer I/O supply voltage	2.7	3.3	5.5	V
HVDD	Input positive supply voltage	5.0	15.0	16.5	V
HVSS	Input negative supply voltage	–16.5	–15.0	–5.0	V
T_A	Operating ambient temperature range	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		ADS85x8		UNIT
		RGC (VQFN)	PM (LQFP)	
		64 PINS	64 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22	48.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.0	9.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	21.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.9	21.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: General

All minimum and maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
CHXX	Bipolar full-scale range	RANGE pin, RANGE bit = 0	–4 VREF		4 VREF	V
		RANGE pin, RANGE bit = 1	–2 VREF		2 VREF	
	Input capacitance	Input range = ±4 VREF		10		pF
		Input range = ±2 VREF		20		
	Input leakage current	No ongoing conversion	–1		1	µA
	Aperture delay			5		ns
	Aperture delay matching	Common CONVST for all channels		100		ps
	Aperture jitter			50		ps
PSRR	Power-supply rejection ratio	At output code FFFFh, related to HVDD and HVSS		–78		dB
REFERENCE VOLTAGE OUTPUT (REF_{OUT})						
VREF	Reference voltage	2.5-V operation, REFDAC = 3FFh	2.485	2.5	2.515	V
		2.5-V operation, REFDAC = 3FFh at 25°C	2.496	2.5	2.504	
		3.0-V operation, REFDAC = 3FFh	2.985	3.0	3.015	
		3.0-V operation, REFDAC = 3FFh at 25°C	2.995	3.0	3.005	
dVREF/dT	Reference voltage drift			±10		ppm/°C
PSRR	Power-supply rejection ratio	At output code FFFFh, related to AVDD		–77		dB
$IREF_{OUT}$	Output current	At dc current	–2		2	mA
I_{REFSC}	Short-circuit current(1)			50		mA
t_{REFON}	Turn-on settling time			10		ms
	External load capacitance	At REF_xP, REF_xN pins	4.7	10		µF
		At REFIO pin	100	470		nF
REFDAC	Tuning range	Internal reference output voltage range	0.2 VREF		VREF	V
	REFDAC resolution		10			Bits
DNL_{DAC}	REFDAC differential nonlinearity		–1	±0.1	1	LSB
INL_{DAC}	REFDAC integral nonlinearity		–2	±0.1	2	LSB
V_{OSDAC}	REFDAC offset error	VREF = 0.5 V (DAC = 0CDh)	–4	±0.65	4	LSB
REFERENCE VOLTAGE INPUT (REF_{IN})						
$VREF_{IN}$	Reference input voltage		0.5	2.5	3.025	V
	Input resistance			100		MΩ
	Input capacitance			5		pF
	Reference input current				1	µA
DIGITAL INPUTS(2) (CMOS with Schmitt-Trigger Logic Family)						
	High-level input voltage		0.7 DVDD		DVDD + 0.3	V
	Low-level input voltage		DGND – 0.3		0.3 DVDD	V
	Input current	V_I = DVDD to DGND	–50		50	nA
	Input capacitance			5		pF
DIGITAL OUTPUTS(2)						
	Output capacitance			5		pF
	Load capacitance				30	pF
	High-impedance-state output current		–50		50	nA
	Logic family			CMOS		
V_{OH}	High-level output voltage	I_{OH} = 100 µA	DVDD – 0.6			V
V_{OL}	Low-level output voltage	I_{OH} = –100 µA			DGND + 0.4	V

(1) Reference output current is not limited internally.
(2) Specified by design.

Electrical Characteristics: General (continued)

All minimum and maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog supply voltage		4.5	5.0	5.5	V
DVDD	Buffer I/O supply voltage		2.7	3.3	5.5	V
HVDD	Input positive supply voltage		5.0	15.0	16.5	V
HVSS	Input negative supply voltage		–16.5	–15.0	–5.0	V
IAVDD	Analog supply current	ADS8528, f_{DATA} = maximum		37.9	50.1	mA
		ADS8548, f_{DATA} = maximum		37.3	49.3	
		ADS8568, f_{DATA} = maximum		36.6	48.4	
		f_{DATA} = 250 kSPS, auto-sleep mode		20.3	30.0	
		f_{DATA} = 200 kSPS, auto-sleep mode		17		
		f_{DATA} = 10 kSPS, normal operation		30		
		f_{DATA} = 10 kSPS, auto-sleep mode		4.6		
		Auto-sleep mode, no ongoing conversion, internal conversion clock			7.0	
		Power-down mode			0.03	
IDVDD	Buffer I/O supply current	f_{DATA} = maximum		0.5	2.0	mA
		f_{DATA} = 250 kSPS		0.5	1.4	
		f_{DATA} = 200 kSPS		0.5		
		f_{DATA} = 10 kSPS		0.4		
		Auto-sleep mode, no ongoing conversion, internal conversion clock			0.35	
		Power-down mode			0.01	
IHVDD	Input positive supply current	ADS8528, f_{DATA} = maximum		3.0	4.2	mA
		ADS8548, f_{DATA} = maximum		2.8	3.9	
		ADS8568, f_{DATA} = maximum		2.3	3.2	
		f_{DATA} = 250 kSPS		1.8	2.4	
		f_{DATA} = 200 kSPS		1.5		
		f_{DATA} = 10 kSPS		0.4		
		Auto-sleep mode, no ongoing conversion, internal conversion clock			0.45	
		Power-down mode			0.01	

Electrical Characteristics: General (continued)

All minimum and maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS (continued)						
IHVSS	Input negative supply current	ADS8528, f_{DATA} = maximum		3.4	4.5	mA
		ADS8548, f_{DATA} = maximum		3.3	4.4	
		ADS8568, f_{DATA} = maximum		2.7	3.6	
		f_{DATA} = 250 kSPS		2.1	2.6	
		f_{DATA} = 200 kSPS		1.7		
		f_{DATA} = 10 kSPS		0.4		
		Auto-sleep mode, no ongoing conversion, internal conversion clock			0.35	
		Power-down mode			0.01	
	Power dissipation(3)	ADS8528, f_{DATA} = maximum		287.1	430.1	mW
		ADS8548, f_{DATA} = maximum		279.7	419.1	
		ADS8568, f_{DATA} = maximum		259.7	389.4	
		f_{DATA} = 250 kSPS, auto-sleep mode		161.7	255.2	
		f_{DATA} = 200 kSPS, auto-sleep mode		151.2		
		f_{DATA} = 10 kSPS, normal operation		163.3		
		f_{DATA} = 10 kSPS, auto-sleep mode		36.3		
		Auto-sleep mode, no ongoing conversion, internal conversion clock			53.6	
		Power-down mode			0.6	

(3) Maximum power dissipation values are specified with HVDD = 15 V and HVSS = –15 V.

7.6 Electrical Characteristics: ADS8528

All minimum and maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLING DYNAMICS						
	Conversion time	Internal conversion clock			1.33	µs
f_{DATA}	Throughput rate	Serial interface, all four SDOx active			480	kSPS
		Parallel interface			650	
DC ACCURACY						
	Resolution			12		Bits
	No missing codes		12			Bits
INL	Integral linearity error(1)		–0.75	±0.2	0.75	LSB
DNL	Differential linearity error		–0.5	±0.2	0.5	LSB
	Offset error		–1.5	±0.5	1.5	mV
	Offset error matching		–0.65		0.65	mV
	Offset error drift			±3.5		µV/°C
	Gain error	Referenced to voltage at REFIO	–0.5%	±0.25%	0.5%	
	Gain error matching	Between channels of any pair	–0.2%		0.2%	
		Between any two channels	–0.4%		0.4%	
	Gain error drift	Referenced to voltage at REFIO		±6		ppm/°C
AC ACCURACY						
SNR	Signal-to-noise ratio	At f_{IN} = 10 kHz	73	73.9		dB
SINAD	Signal-to-noise ratio + distortion	At f_{IN} = 10 kHz	73	73.8		dB
THD	Total harmonic distortion(2)	At f_{IN} = 10 kHz		–89	–84	dB
SFDR	Spurious-free dynamic range	At f_{IN} = 10 kHz	84	92		dB
	Channel-to-channel isolation	At f_{IN} = 10 kHz		120		dB
BW	–3-dB small-signal bandwidth	In 4-VREF mode		48		MHz
		In 2-VREF mode		24		

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as the number of LSBs or percentage of the specified full-scale range.
(2) Calculated on the first nine harmonics of the input frequency.

7.7 Electrical Characteristics: ADS8548

All minimum and maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLING DYNAMICS						
	Conversion time	Internal conversion clock			1.45	µs
f_{DATA}	Throughput rate	Serial interface, all four SDOx active			450	kSPS
		Parallel interface			600	
DC ACCURACY						
	Resolution			14		Bits
	No missing codes		14			Bits
INL	Integral linearity error(1)		–1	±0.5	1	LSB
DNL	Differential linearity error		–1	±0.25	1	LSB
	Offset error		–1.5	±0.5	1.5	mV
	Offset error matching		–0.65		0.65	mV
	Offset error drift			±3.5		µV/°C
	Gain error	Referenced to voltage at REFIO	–0.5%	±0.25%	0.5%	
	Gain error matching	Between channels of any pair	–0.2%		0.2%	
		Between any two channels	–0.4%		0.4%	
	Gain error drift	Referenced to voltage at REFIO		±6		ppm/°C
AC ACCURACY						
SNR	Signal-to-noise ratio	At f_{IN} = 10 kHz	84	85		dB
SINAD	Signal-to-noise ratio + distortion	At f_{IN} = 10 kHz	83	84		dB
THD	Total harmonic distortion(2)	At f_{IN} = 10 kHz		–91	–86	dB
SFDR	Spurious-free dynamic range	At f_{IN} = 10 kHz	86	92		dB
	Channel-to-channel isolation	At f_{IN} = 10 kHz		120		dB
BW	–3-dB small-signal bandwidth	In 4-VREF mode		48		MHz
		In 2-VREF mode		24		

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as the number of LSBs or percentage of the specified full-scale range.
(2) Calculated on the first nine harmonics of the input frequency.

7.8 Electrical Characteristics: ADS8568

All minimum and maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLING DYNAMICS						
	Conversion time	Internal conversion clock			1.7	µs
f_{DATA}	Throughput rate	Serial interface, all four SDOx active			400	kSPS
		Parallel interface			510	
DC ACCURACY						
	Resolution			16		Bits
	No missing codes		16			Bits
INL	Integral linearity error(1)	At T_A = –40°C to +85°C, VQFN package (RGC)	–3	±1.5	3	LSB
		At T_A = –40°C to +125°C, VQFN package (RGC)	–4	±1.5	4	
		At T_A = –40°C to +85°C, LQFP package (PM)	–4	±1.5	4	
		At T_A = –40°C to +125°C, LQFP package (PM)	–4.5	±1.5	4.5	
DNL	Differential linearity error	At T_A = –40°C to +85°C	–1	±0.75	1.75	LSB
		At T_A = –40°C to +125°C	–1	±0.75	2	
	Offset error		–1.5	±0.5	1.5	mV
	Offset error matching		–0.65		0.65	mV
	Offset error drift			±3.5		µV/°C
	Gain error	Referenced to voltage at REFIO	–0.5%	±0.25%	0.5%	
	Gain error matching	Between channels of any pair	–0.2%		0.2%	
		Between any two channels	–0.4%		0.4%	
	Gain error drift	Referenced to voltage at REFIO		±6		ppm/°C
AC ACCURACY						
SNR	Signal-to-noise ratio	At f_{IN} = 10 kHz, T_A = –40°C to +85°C	90	91.5		dB
		At f_{IN} = 10 kHz, T_A = –40°C to +125°C	89	91.5		
SINAD	Signal-to-noise ratio + distortion	At f_{IN} = 10 kHz, T_A = –40°C to +85°C	87	90		dB
		At f_{IN} = 10 kHz, T_A = –40°C to +125°C	86.5	90		
THD	Total harmonic distortion(2)	At f_{IN} = 10 kHz, T_A = –40°C to +85°C		–94	–90	dB
		At f_{IN} = 10 kHz, T_A = –40°C to +125°C		–94	–89.5	
SFDR	Spurious-free dynamic range	At f_{IN} = 10 kHz, T_A = –40°C to +85°C	90	95		dB
		At f_{IN} = 10 kHz, T_A = –40°C to +125°C	89.5	95		
	Channel-to-channel isolation	At f_{IN} = 10 kHz		120		dB
BW	–3-dB small-signal bandwidth	In 4-VREF mode		48		MHz
		In 2-VREF mode		24		

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as the number of LSBs or percentage of the specified full-scale range.
(2) Calculated on the first nine harmonics of the input frequency.

7.9 Serial Interface Timing Requirements

over recommended operating free-air temperature range (T_A), AVDD = 5 V, and DVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
t_{SCVX}	CONVST_x high to XCLK rising edge setup time (CLKSEL = 1)		6			ns
t_{XCLK}	External conversion clock period	ADS8528	66.67			ns
		ADS8548	72.46			
		ADS8568	85.11			
	External conversion clock frequency	ADS8528	1		15.0	MHz
		ADS8548	1		13.8	
		ADS8568	1		11.75	
	External conversion clock duty cycle		40%		60%	
t_{CVL}	CONVST_x low time		20			ns
t_{ACQ}	Acquisition time		280			ns
	Clock cycles per conversion	ADS85x8, t_{CCLK} or t_{XCLK}	19		20	Cycles
t_{CONV}	Conversion time	ADS8528, CLKSEL = 0			1.33	µs
		ADS8548, CLKSEL = 0			1.45	
		ADS8568, CLKSEL = 0			1.7	
t_{DCVB}	CONVST_x high to BUSY high delay				25	ns
t_{BUFS}	BUSY low to $\overline{FS}$ low time	ADS85x8, CLKSEL = 1	0			ns
		ADS8528, CLKSEL = 0(2)	67			
		ADS8548, CLKSEL = 0(2)	73			
		ADS8568, CLKSEL = 0(2)	86			
t_{FSCV}	Bus access finished to next conversion start time	ADS8528	0			ns
		ADS8548	20			
		ADS8568	40			
t_{SCLK}	Serial clock period		0.022		10	µs
	Serial clock frequency		0.1		45	MHz
	Serial clock duty cycle		40%		60%	
t_{DMSB}	$\overline{FS}$ low to MSB valid delay				12	ns
t_{HDO}	Output data to SCLK falling edge hold time		5			ns
t_{PDDO}	SCLK falling edge to new data valid propagation delay				17	ns
t_{DTRI}	$\overline{FS}$ high to SDO_x three-state delay				10	ns
t_{SUDI}	Input data to SCLK falling edge setup time		3			ns
t_{HDI}	Input data to SCLK falling edge hold time		5			ns

(1) All input signals are specified with $t_R = t_F = 1.5$ ns (10% to 90% of DVDD) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$.
(2) The device runs with an internal conversion clock. Data can be retrieved after the maximum conversion time $t_{CONV(max)}$, independently from the BUSY signal. When referring the data readout to the falling edge of the BUSY signal, $t_{BUFS(min)}$ must be taken into account (see the *Data Readout and BUSY/INT Signal* section).

7.10 Parallel Interface Timing Requirements (Read Access)

over recommended operating free-air temperature range (T_A), AVDD = 5 V, and DVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
t_{CVL}	CONVST_x low time		20			ns
t_{ACQ}	Acquisition time		280			ns
	Clock cycles per conversion	ADS85x8, t_{CCLK} or t_{XCLK}	19		20	Cycles
t_{CONV}	Conversion time	ADS8528, CLKSEL = 0			1.33	µs
		ADS8548, CLKSEL = 0			1.45	
		ADS8568, CLKSEL = 0			1.7	
t_{DCVB}	CONVST_x high to BUSY high delay				25	ns
t_{BUCS}	BUSY low to $\overline{CS}$ low time	ADS85x8, CLKSEL = 1	0			ns
		ADS8528, CLKSEL = 0(2)	67			
		ADS8548, CLKSEL = 0(2)	73			
		ADS8568, CLKSEL = 0(2)	86			
t_{CSCV}	Bus access finished to next conversion start time(3)	ADS8528	0			ns
		ADS8548	20			
		ADS8568	40			
t_{CSRD}	$\overline{CS}$ low to $\overline{RD}$ low time		0			ns
t_{RDCS}	$\overline{RD}$ high to $\overline{CS}$ high time		0			ns
t_{RDL}	$\overline{RD}$ pulse duration		20			ns
t_{RDH}	Minimum time between two read accesses		2			ns
t_{PDDO}	$\overline{RD}$ or $\overline{CS}$ falling edge to data valid propagation delay				15	ns
t_{HDO}	Output data to $\overline{RD}$ or $\overline{CS}$ rising edge hold time		5			ns
t_{DTRI}	$\overline{CS}$ high to DB[15:0] three-state delay				10	ns

(1) All input signals are specified with $t_R = t_F$ = 1.5 ns (10% to 90% of DVDD) and timed from a voltage level of (V_{IL} + V_{IH}) / 2.
(2) The device runs with an internal conversion clock. Data can be retrieved after the maximum conversion time $t_{CONV(max)}$, independently from the BUSY signal. When referring the data readout to the falling edge of the BUSY signal, $t_{BUCS(min)}$ must be taken into account (see the *Data Readout and BUSY/INT Signal* section).
(3) See the $\overline{CS}$ signal or $\overline{RD}$, whichever occurs first.

7.11 Parallel Interface Timing Requirements (Write Access)

over recommended ambient temperature range (T_A), AVDD = 5 V, and DVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
t_{CSWR}	$\overline{CS}$ low to $\overline{WR}$ low time	0			ns
t_{WRL}	$\overline{WR}$ low pulse duration	15			ns
t_{WRH}	Minimum time between two write accesses	10			ns
t_{WRCS}	$\overline{WR}$ high to $\overline{CS}$ high time	0			ns
t_{SUDI}	Output data to $\overline{WR}$ rising edge setup time	5			ns
t_{HDI}	Data output to $\overline{WR}$ rising edge hold time	5			ns

(1) All input signals are specified with $t_R = t_F$ = 1.5 ns (10% to 90% of DVDD) and timed from a voltage level of (V_{IL} + V_{IH}) / 2.

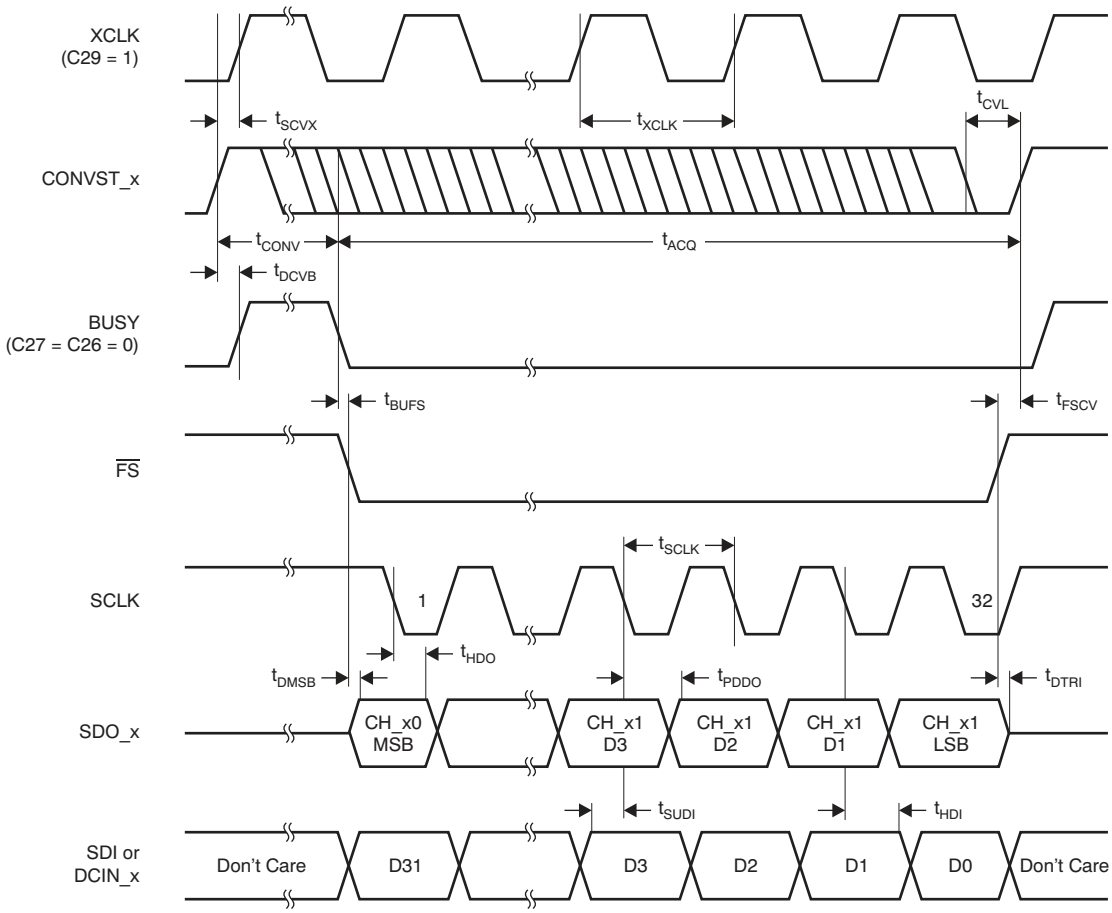


Figure 1. Serial Operation Timing Diagram (All Four SDO_x Active)

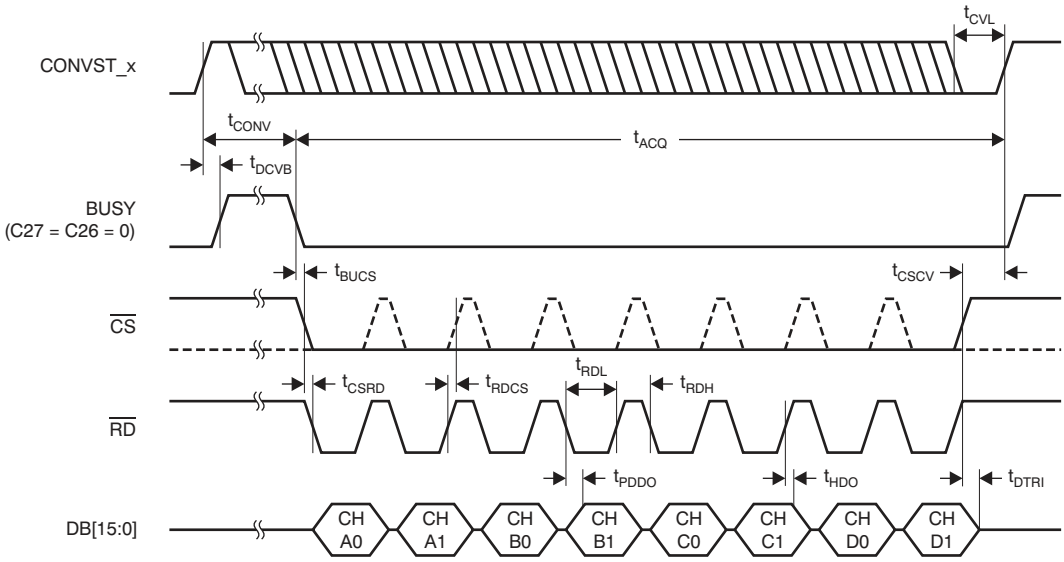


Figure 2. Parallel Read Access Timing Diagram

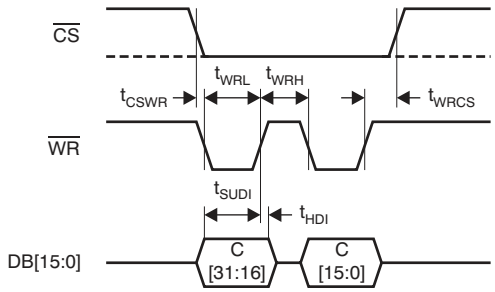


Figure 3. Parallel Write Access Timing Diagram

7.12 Typical Characteristics

graphs are valid for all devices of the family, at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = maximum (unless otherwise noted)

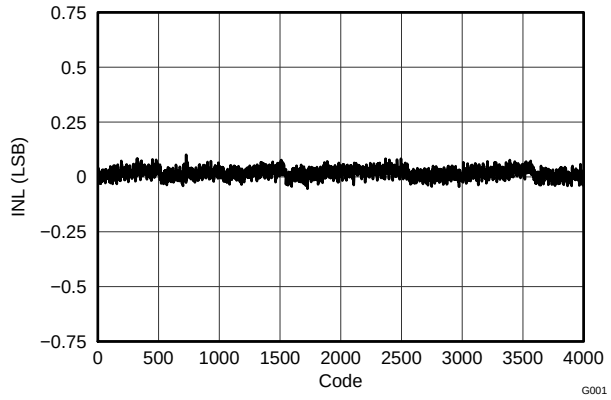


Figure 4. Integral Nonlinearity vs Code (ADS8528)

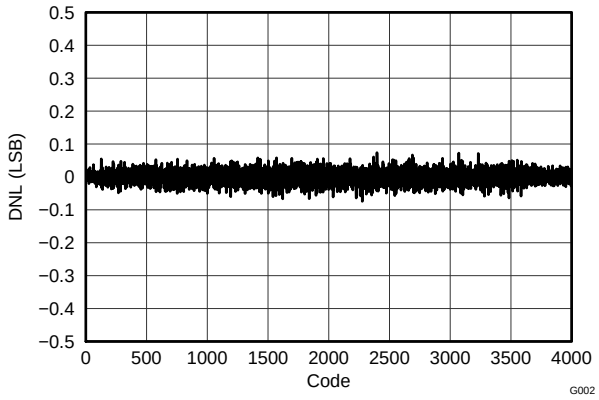


Figure 5. Differential Nonlinearity vs Code (ADS8528)

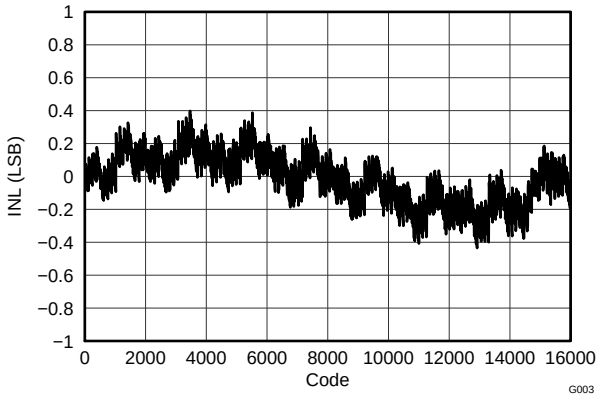


Figure 6. Integral Nonlinearity vs Code (ADS8548 ±10-V_{IN} Range)

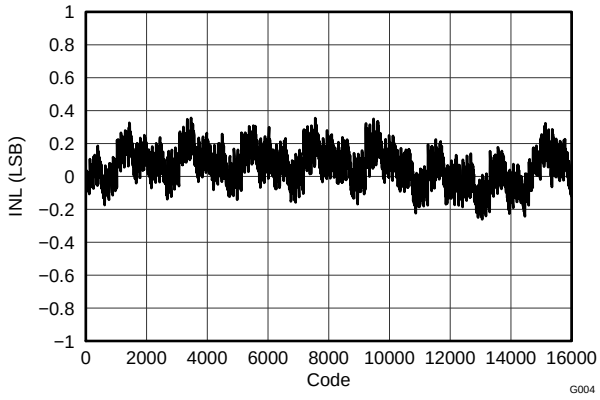


Figure 7. Integral Nonlinearity vs Code (ADS8548 ±5-V_{IN} Range)

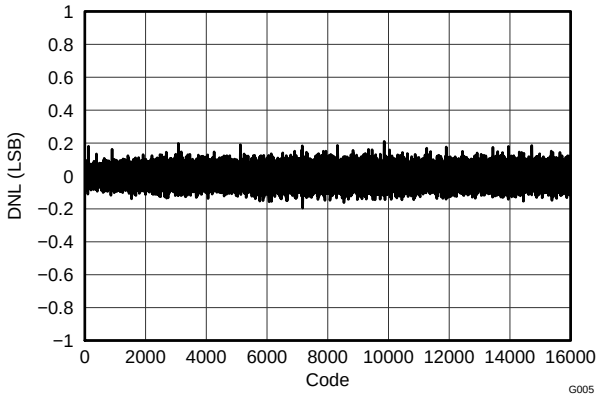


Figure 8. Differential Nonlinearity vs Code (ADS8548 ±10-V_{IN} Range)

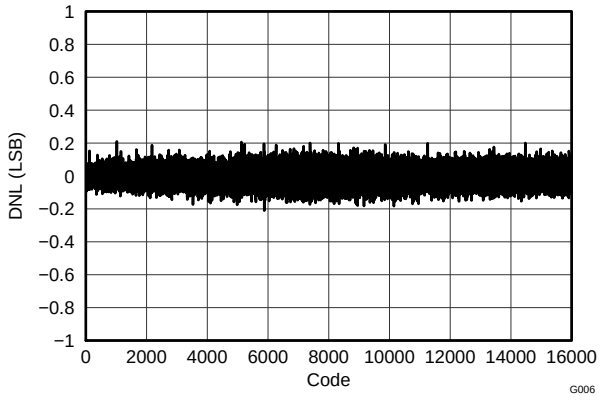


Figure 9. Differential Nonlinearity vs Code (ADS8548 ±5-V_{IN} Range)

Typical Characteristics (continued)

graphs are valid for all devices of the family, at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = maximum (unless otherwise noted)

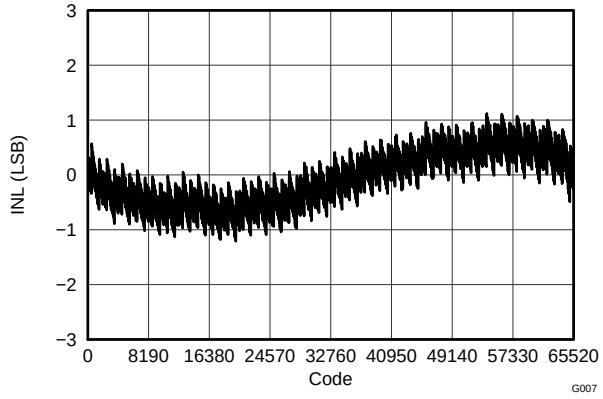


Figure 10. Integral Nonlinearity vs Code (ADS8568 ±10-V_{IN} Range)

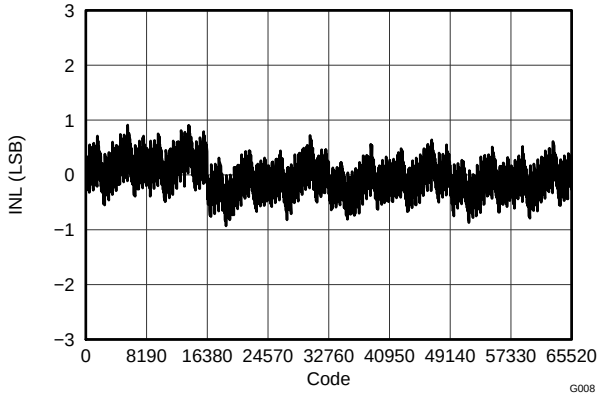


Figure 11. Integral Nonlinearity vs Code (ADS8568 ±5-V_{IN} Range)

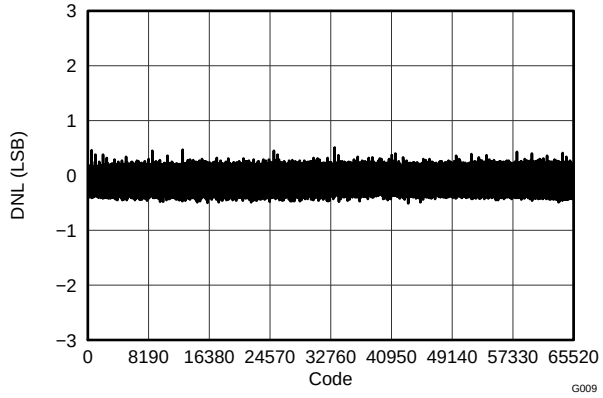


Figure 12. Differential Nonlinearity vs Code (ADS8568 ±10-V_{IN} Range)

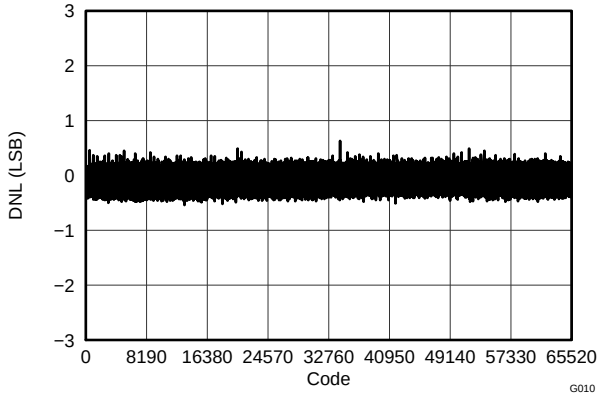


Figure 13. Differential Nonlinearity vs Code (ADS8568 ±5-V_{IN} Range)

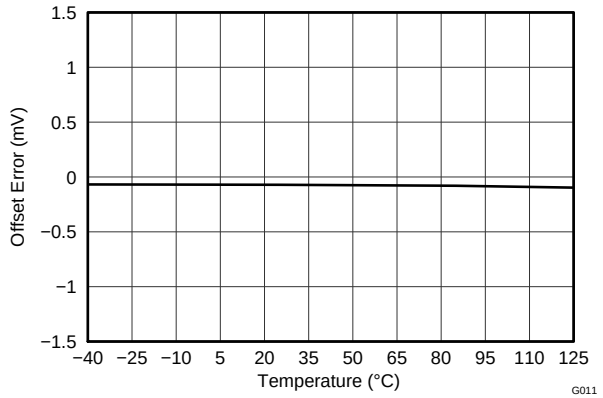


Figure 14. Offset Error vs Temperature

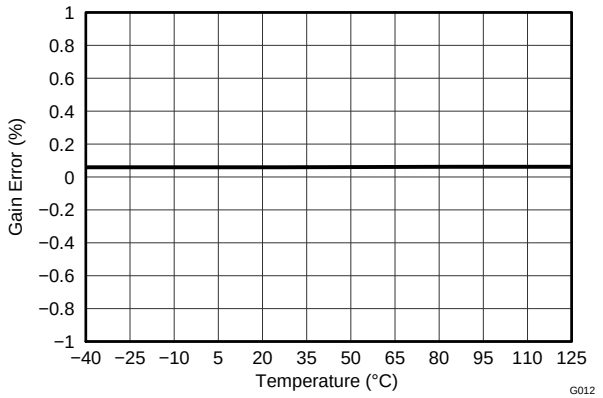


Figure 15. Gain Error vs Temperature

Typical Characteristics (continued)

graphs are valid for all devices of the family, at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = maximum (unless otherwise noted)

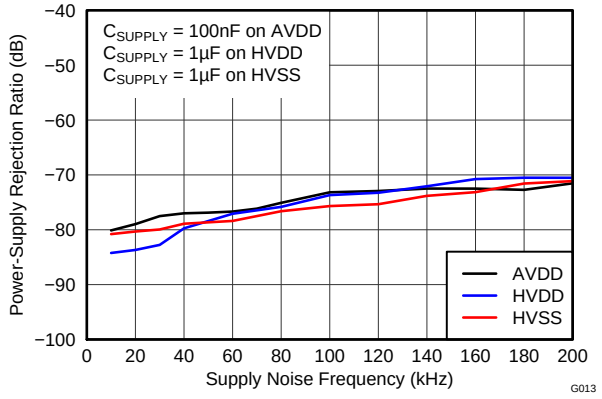


Figure 16. PSRR vs Supply Noise Frequency

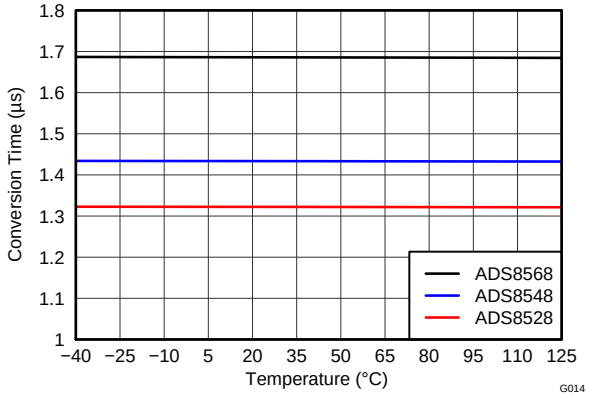


Figure 17. Conversion Time vs Temperature

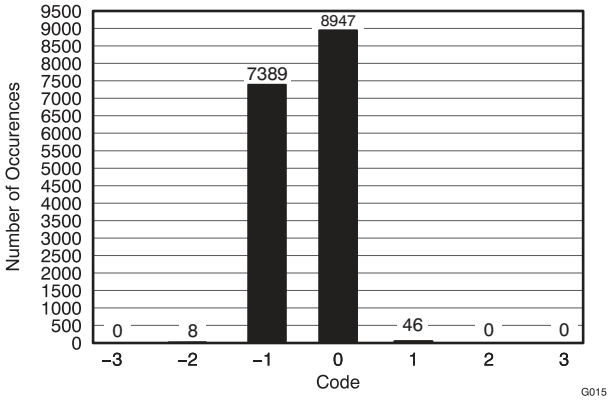


Figure 18. Code Histogram (ADS8568, 16390 Hits)

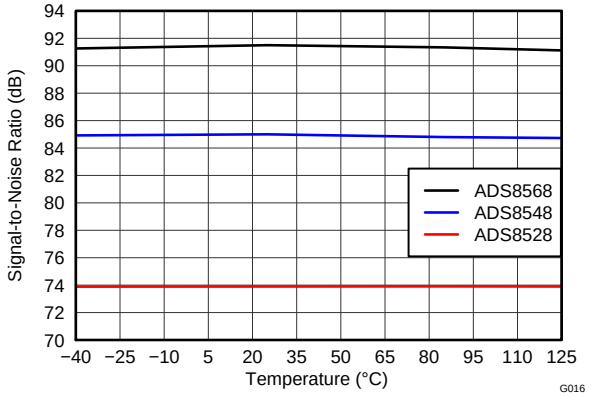


Figure 19. SNR vs Temperature

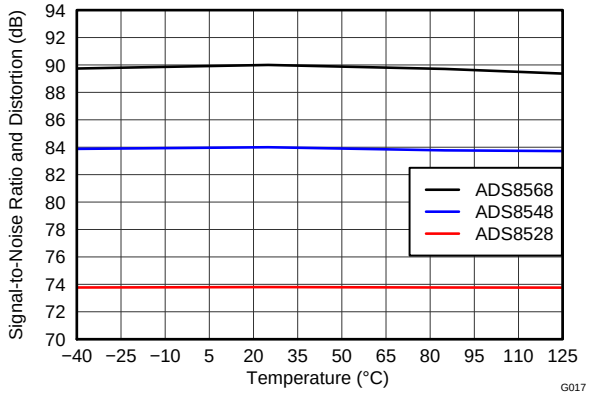


Figure 20. SINAD vs Temperature

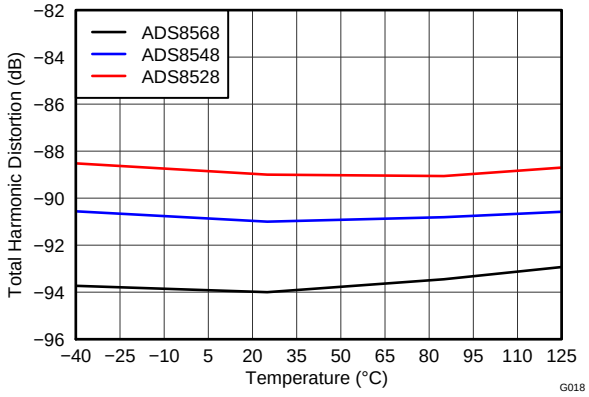


Figure 21. THD vs Temperature

Typical Characteristics (continued)

graphs are valid for all devices of the family, at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = maximum (unless otherwise noted)

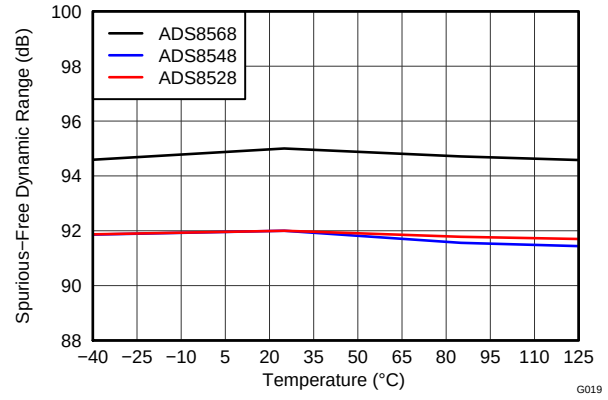


Figure 22. SFDR vs Temperature

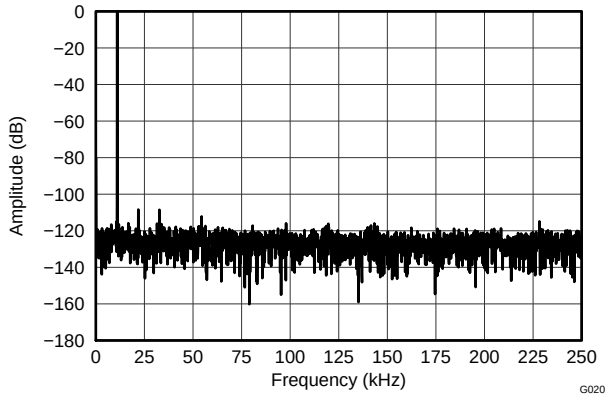


Figure 23. Frequency Spectrum (ADS8568, 2048-Point FFT, f_{IN} = 10 kHz, ±10-V_{IN} Range)

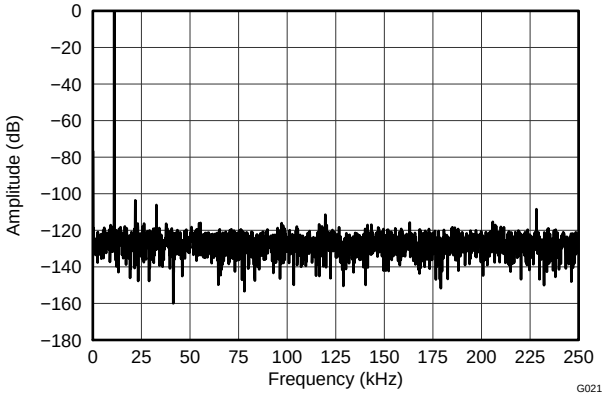


Figure 24. Frequency Spectrum (ADS8568, 2048-Point FFT, f_{IN} = 10 kHz, ±5-V_{IN} Range)

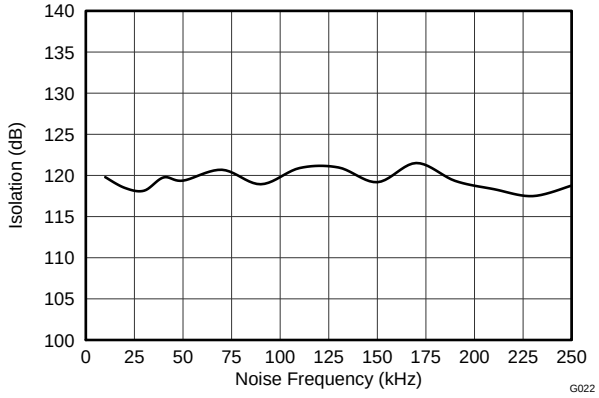


Figure 25. Channel-to-Channel Isolation vs Input Noise Frequency

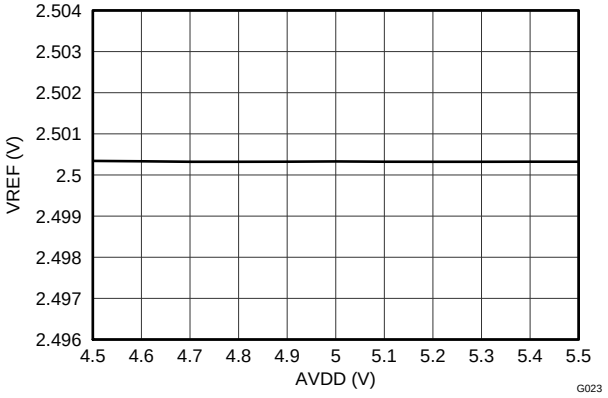


Figure 26. Internal Reference Voltage vs Analog Supply Voltage (2.5-V Mode)

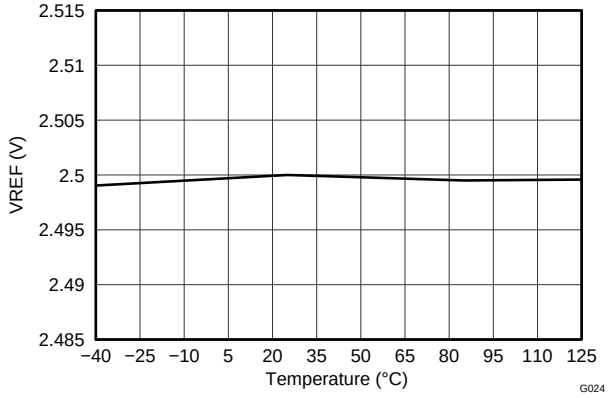


Figure 27. Internal Reference Voltage vs Temperature (2.5-V Mode)

Typical Characteristics (continued)

graphs are valid for all devices of the family, at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = maximum (unless otherwise noted)

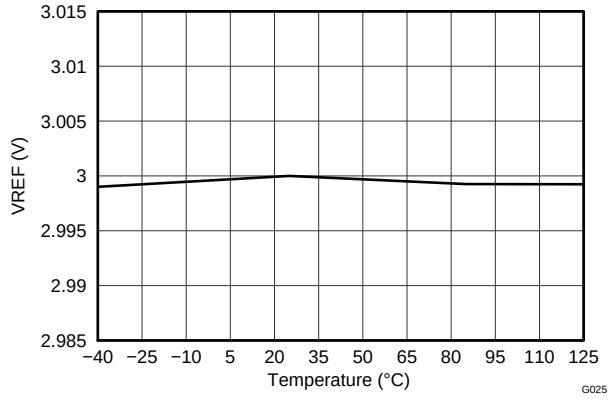


Figure 28. Internal Reference Voltage vs Temperature (3.0-V Mode)

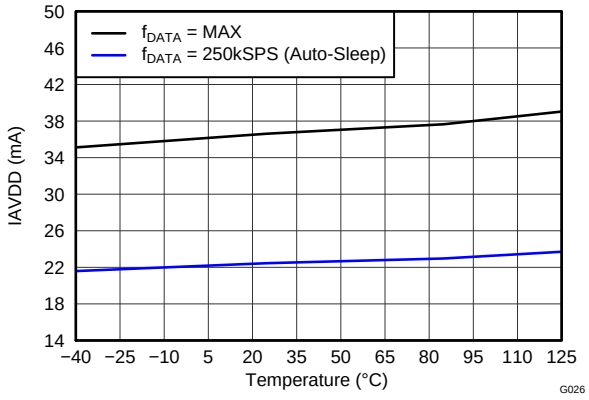


Figure 29. ADS8568 Analog Supply Current vs Temperature

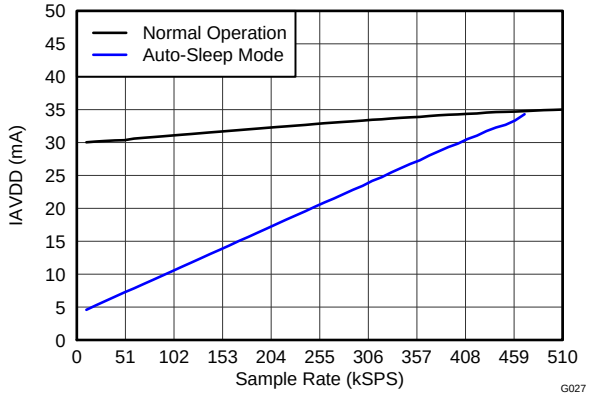


Figure 30. ADS8568 Analog Supply Current vs Data Rate

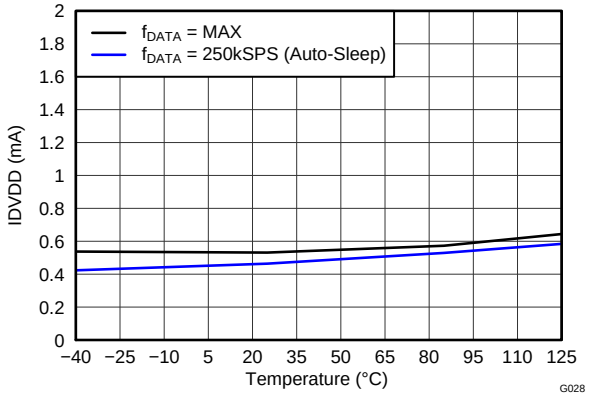


Figure 31. Buffer I/O Supply Current vs Temperature

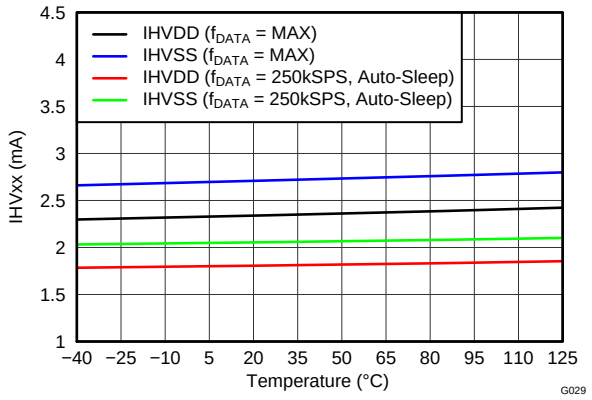


Figure 32. ADS8568 Input Supply Current vs Temperature

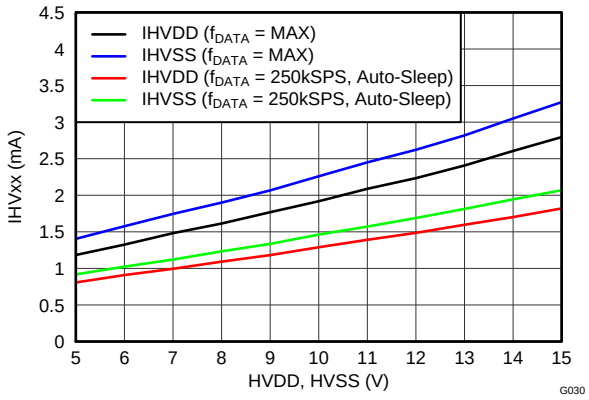


Figure 33. ADS8568 Input Supply Current vs Input Supply Voltage

Typical Characteristics (continued)

graphs are valid for all devices of the family, at T_A = 25°C, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), V_{IN} = ±10 V, and f_{DATA} = maximum (unless otherwise noted)

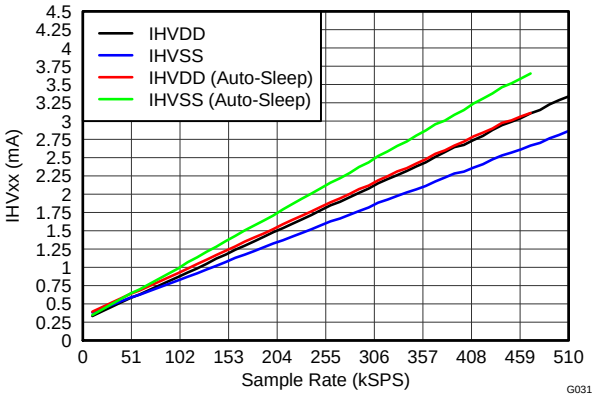


Figure 34. ADS8568 Input Supply Current vs Data Rate

8 Parameter Measurement information

8.1 Equivalent Circuits

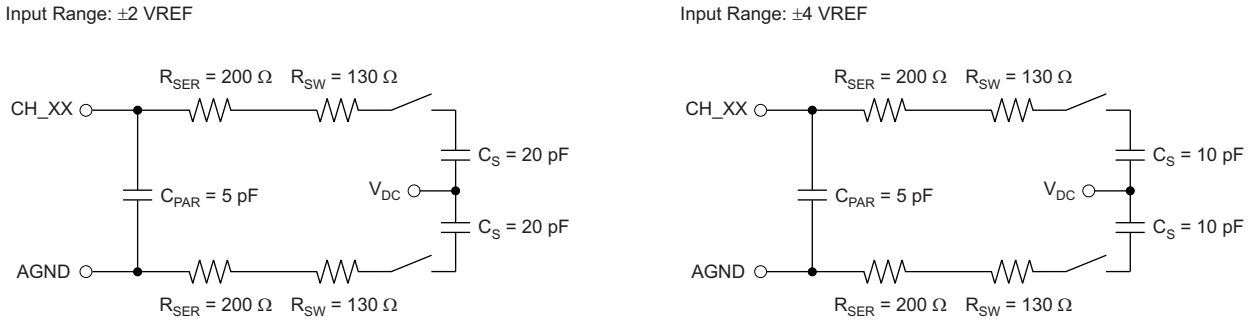


Figure 35. Equivalent Input Circuits

9 Detailed Description

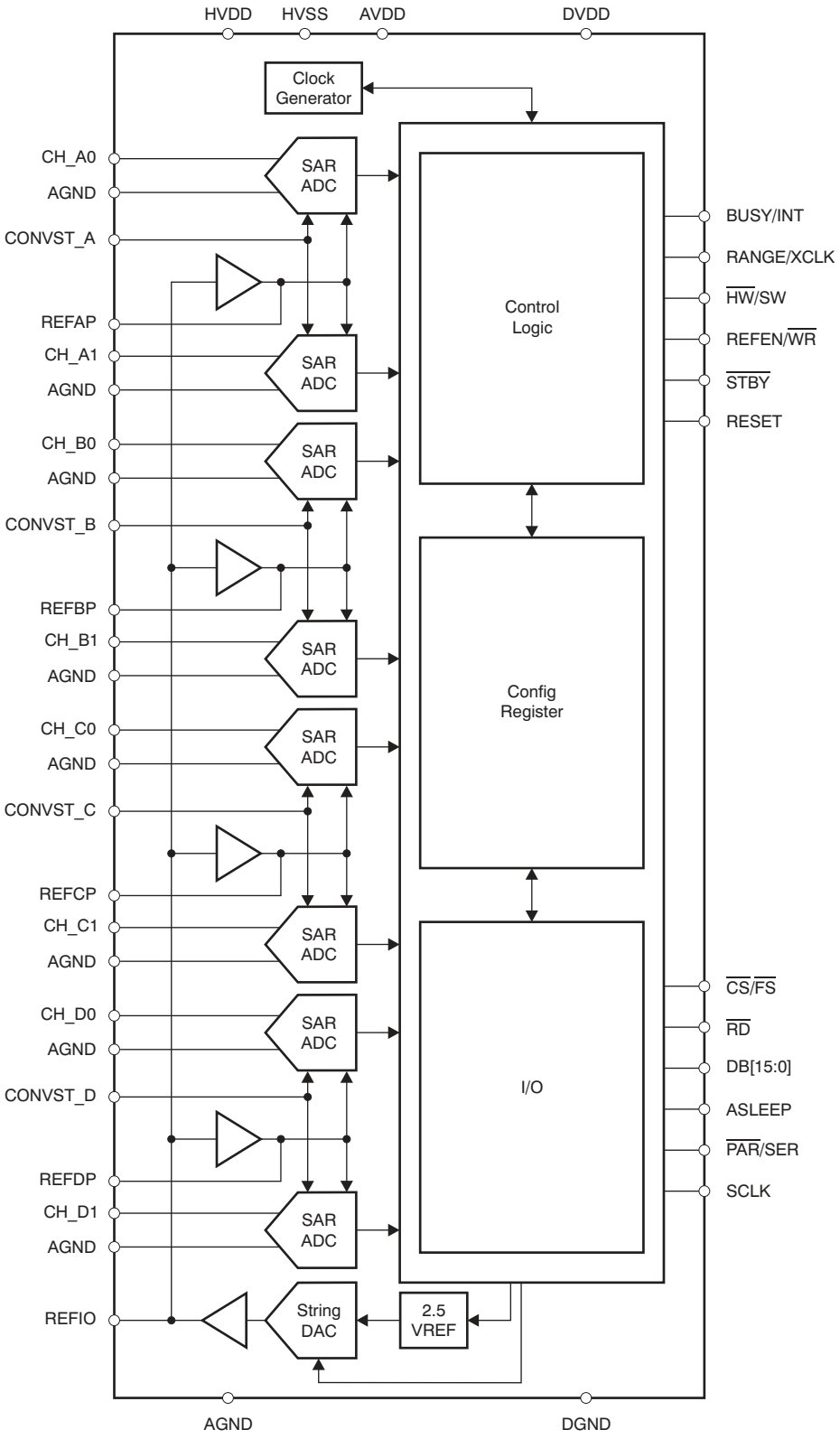
9.1 Overview

The ADS85x8 series includes eight 12-, 14-, and 16-bit analog-to-digital converters (ADCs) that operate based on the successive approximation register (SAR) architecture. This architecture is designed on the charge redistribution principle that inherently includes a sample-and-hold function. The eight analog inputs are grouped into four channel pairs. These channel pairs can be sampled and converted simultaneously, preserving the relative phase information of the signals of each pair. Separate conversion start signals allow simultaneous sampling on each channel pair of four, six, or eight channels. These devices accept single-ended, bipolar analog input signals in the selectable ranges of ±4 VREF or ±2 VREF with an absolute value of up to ±12 V; see the *Analog Inputs* section.

The devices offer an internal 2.5-V or 3-V reference source followed by a 10-bit digital-to-analog converter (DAC) that allows the reference voltage VREF to be adjusted in 2.44-mV or 2.93-mV steps, respectively.

The ADS85x8 also offer a selectable parallel or serial interface that can be used in hardware or software mode; see the *Device Configuration* section for details. The *Analog* and *Digital* sections describe the functionality and control of the device in detail.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Analog

This section addresses the analog input circuit, the ADCs and control signals, and the reference design of the device.

9.3.1.1 Analog Inputs

The inputs and the converters are of single-ended bipolar type. The absolute voltage range can be selected using the RANGE pin (in hardware mode) or RANGE_x bits (in software mode) in the Configuration (CONFIG) register to either ±4 VREF or ±2 VREF. With the internal reference set to 2.5 V (VREF bit C13 = 0 in the CONFIG register), the input voltage range can be ±10 V or ±5 V. With the internal reference source set to 3 V (CONFIG bit C13 = 1), an input voltage range of ±12 V or ±6 V can be configured. The logic state of the RANGE pin is latched with the falling edge of BUSY (if CONFIG bit C26 = 0).

The input current on the analog inputs depends on the actual sample rate, input voltage, and signal source impedance. Essentially, the current into the analog inputs charges the internal capacitor array only during the sampling period (t_{ACQ}). The source of the analog input voltage must be able to charge the input capacitance of 10 pF in ±4-VREF mode or of 20 pF in ±2-VREF mode to a 12-, 14-, or 16-bit accuracy level within the acquisition time; see Figure 35. During the conversion period, there is no further input current flow and the input impedance is greater than 1 MΩ. To ensure a defined start condition, the sampling capacitors of the ADS85x8 are pre-charged to a fixed internal voltage before switching into sampling mode.

To maintain the linearity of the converter, the inputs must always remain within the specified range defined in the *Electrical Characteristics* table. The minimum –3-dB bandwidth of the driving operational amplifier can be calculated using Equation 1:

$$f_{3dB} = \frac{\ln(2)(n + 1)}{2\pi t_{ACQ}} \quad (1)$$

where

- n = 12, 14, or 16; *n* is the resolution of the ADS85x8

With a minimum acquisition time of t_{ACQ} = 280 ns, the required minimum bandwidth of the driving amplifier is 5.2 MHz for the ADS8528, 6.0 MHz for the ADS8548, or 6.7 MHz for the ADS8568. The required bandwidth can be lower if the application allows a longer acquisition time. A gain error occurs if a given application does not fulfill the bandwidth requirement shown in Equation 1.

A driving operational amplifier may not be required if the impedance of the signal source (R_{SOURCE}) fulfills the requirement of Equation 2:

$$R_{SOURCE} < \frac{t_{ACQ}}{C_S \ln(2)(n + 1)} - (R_{SER} + R_{SW}) \quad (2)$$

where

- n = 12, 14, or 16; *n* is the resolution of the ADC
- C_S = 10 pF is the sample capacitor value in V_{IN} = ±4-VREF mode
- R_{SER} = 200 Ω is the input resistor value
- and R_{SW} = 130 Ω is the switch resistance value

With a minimum acquisition time of t_{ACQ} = 280 ns, the maximum source impedance must be less than 2.7 kΩ for the ADS8528, 2.3 kΩ for the ADS8548, and 2.0 kΩ for the ADS8568 in ±4V-REF mode, or less than 1.2 kΩ for the ADS8528, 1.0 kΩ for the ADS8548, and 0.8 kΩ for the ADS8568 in ±2-VREF mode. The source impedance can be higher if the application allows a longer acquisition time.

9.3.1.2 Analog-to-Digital Converter (ADC)

The device includes eight ADCs that operate with either an internal or an external conversion clock.

Feature Description (continued)

9.3.1.3 Conversion Clock

The device uses either an internally-generated (CCLK) or an external (XCLK) conversion clock signal (in software mode only). In default mode, the device generates an internal clock. In this case, a complete conversion including the pre-charging of the sample capacitors takes 19 to 20 clock cycles, depending on the setup time of the incoming CONVST_x signal with relation to the CCLK rising edge.

When the CLKSEL bit is set high (CONFIG bit C29), an external conversion clock can be applied on pin 34. A complete conversion process requires 19 clock cycles in this case if the t_{SCVX} timing requirement is fulfilled. The external clock can remain low between conversions.

If the application requires lowest power dissipation at low data rates, using the auto-sleep mode activated with pin 36 (ASLEEP) is recommended. In this case, a conversion cycle takes up to 26 clock cycles (see the *Reset and Power-Down Modes* section for more details).

9.3.1.4 CONVST_x

The analog inputs of each channel pair (CH_x0, CH_x1) are held with the rising edge of the corresponding CONVST_x signal. The conversion automatically starts with the next rising edge of the conversion clock. CONVST_A is a master conversion start that resets the internal state machine and causes the data output to start with the result of channel A0. In cases where channel pairs of the device are used at different data rates, CONVST_A must always be the one used at the highest frequency.

A conversion start must not be issued during an ongoing conversion on the corresponding channel pair. However, conversions are allowed to be initiated on other input pairs; see the *Sequential Operation* section for more details.

If a parallel interface is used, the content of the output port depends on which CONVST_x signals are issued. Figure 36 shows examples of different scenarios with all channel pairs active.

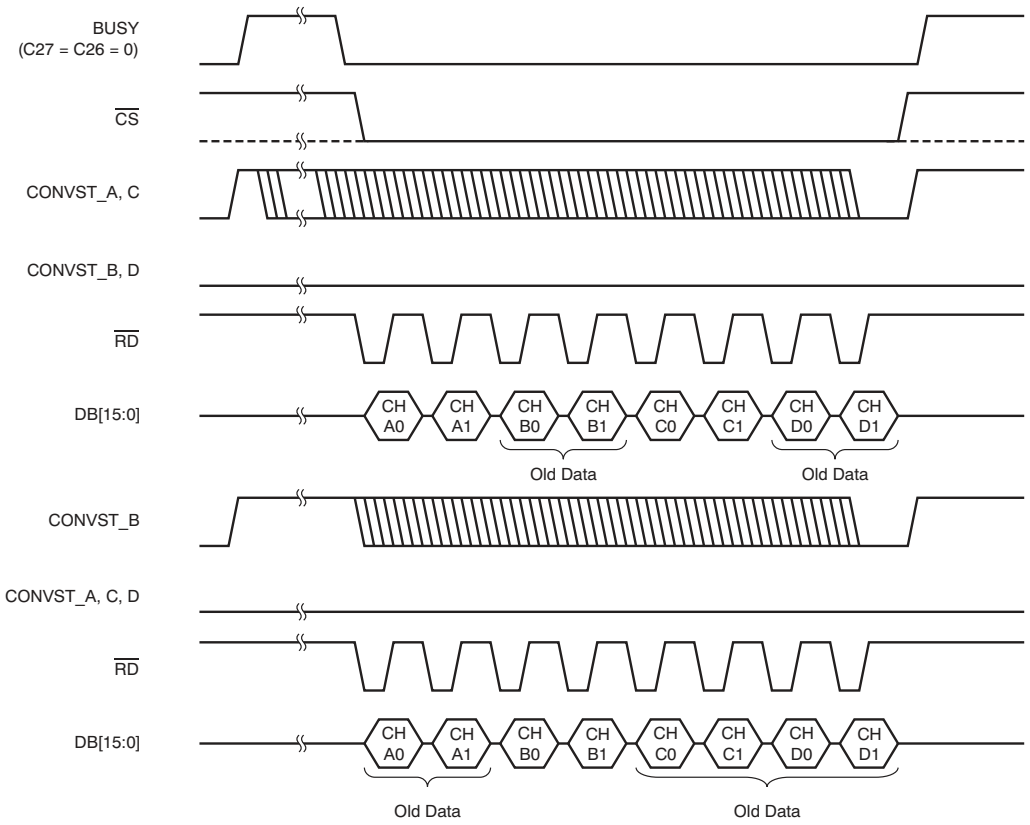


Figure 36. Data Output versus CONVST_x (All Channels Active)

Feature Description (continued)

9.3.1.5 Data Readout and BUSY/INT Signal

The BUSY signal indicates if a conversion is in progress. The BUSY signal goes high with a rising edge of any CONVST_x signal and returns low again when the last channel pair completes the conversion cycle.

When operating the device with an external clock (CONFIG bit 29, CLKSEL = 1), data readout can be initiated immediately after the falling edge of the BUSY signal or after 19 complete conversion clock cycles (XCLK), respectively.

When using the device with an internal conversion clock (CONFIG bit 29, CLKSEL = 0), data can be retrieved after $t_{CONV(max)}$ independently from the BUSY signal. In case the data readout is referred to the falling edge of the BUSY signal, the readout sequence cannot start before $t_{BUFS/BUCS}$ after the falling edge, corresponding to 1 CCLK cycle (for example, 86 ns for the ADS8568).

In contrast, the INT signal goes high when a new conversion result is loaded in the output register (which occurs when the conversion completes) and remains high until the next read access, as shown in Figure 37.

The polarity of the BUSY/INT signal can be changed using CONFIG bit C26. The mode of pin 35 can be controlled using CONFIG bit C27.

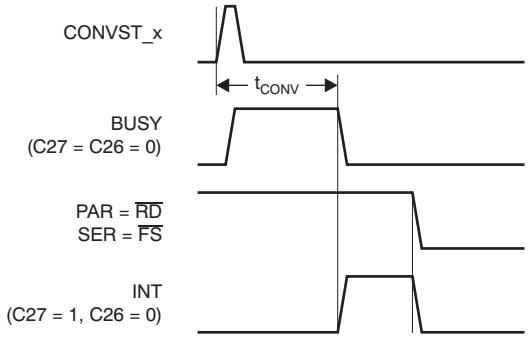
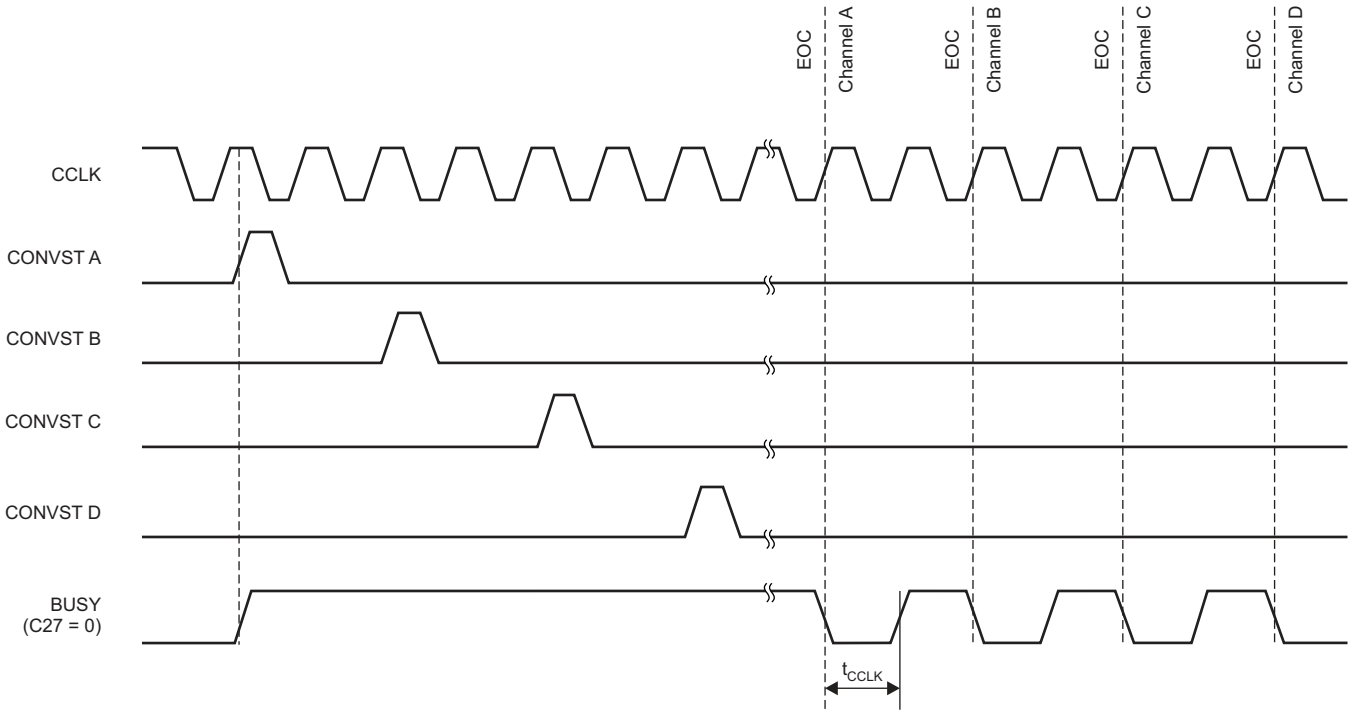


Figure 37. BUSY versus INT Behavior of Pin 35

Feature Description (continued)

9.3.1.6 Sequential Operation

The four channel pairs of the ADS8528, ADS8548, and ADS8568 can run in sequential mode, with the corresponding CONVST_x signals interleaved. In this case, the BUSY output transitions low for a single conversion clock cycle (t_{CCLK}) whenever a channel pair completes a conversion. BUSY finally remains low when the conversion of the last channel pair completes. Figure 38 shows the behavior of the BUSY output in this mode.



NOTE: EOC = end of conversion (internal signal).

Figure 38. Sequential Operation Timing Diagram

For best performance, operation with an external clock is recommended (CONFIG bit 29, CLKSEL = 1). Initiate each conversion start during the high phase of the external clock; see Figure 40.

The time between two CONVST_x pulses must be at least one conversion clock cycle. In case the skew of the CONVST_x signals is less than one conversion clock cycle, the data readout cannot be started before t_{CCLK} after the falling edge of the BUSY signal.

9.3.1.7 Reference

The ADS85x8 provides an internal, low-drift, 2.5-V reference source. To increase the input voltage range, the reference voltage can be switched to 3-V mode using the VREF bit (CONFIG bit C13). The reference feeds a 10-bit string-DAC controlled by the REFDAC[9:0] bits in the Configuration (CONFIG) register. The buffered DAC output is connected to the REFIO pin. In this way, the voltage at this pin is programmable in 2.44-mV steps (2.92 mV in 3-V mode) and adjustable to the applications needs without additional external components. The actual output voltage can be calculated using Equation 3:

$$V_{REF} = \frac{\text{Range} \times (\text{Code} + 1)}{1024} \quad (3)$$

where

- Range = the chosen maximum reference voltage output range (2.5 V or 3 V)
- Code = the decimal value of the DAC register content

Feature Description (continued)

Table 1 lists some examples of internal reference DAC settings with a reference range set to 2.5 V. However, to ensure proper performance, the DAC output voltage must not be programmed below 0.5 V.

Decouple the buffered output of the DAC with a 100-nF capacitor (minimum); for best performance, a 470-nF capacitor is recommended. If the internal reference is placed into power-down (default), an external reference voltage can drive the REFIO pin.

Table 1. DAC Settings Examples (2.5-V Operation)

VREFOUT	DECIMAL CODE	BINARY CODE	HEXADECIMAL CODE
0.5 V	204	00 1100 1100	CCh
1.25 V	511	01 1111 1111	1FFh
2.5 V	1023	11 1111 1111	3FFh

The voltage at the REFIO pin is buffered with four internal amplifiers, one for each ADC pair. The output of each buffer must be decoupled with a 10-µF capacitor between the pin pairs of 3 and 6, 43 and 46, 50 and 53, and 60 and 63. The 10-µF capacitors are available as ceramic 0805-SMD components and in X5R quality.

The internal reference buffers can be powered down to decrease the power dissipation of the device. In this case, external reference drivers can be connected to the REFAP, REFBP, REFCP, and REFDP pins. With 10-µF decoupling capacitors, the minimum required bandwidth can be calculated using Equation 4:

$$f_{3dB} = \frac{\ln(2)}{2\pi t_{CONV}} \quad (4)$$

With the minimum t_{CONV} of 1.33 µs, the external reference buffers require a minimum bandwidth of 83 kHz.

9.3.2 Digital

This section describes the digital control and the timing of the device in detail.

9.3.2.1 Device Configuration

Depending on the desired mode of operation, the ADS85x8 can be configured using the external pins or the Configuration register (CONFIG), as shown in Table 2.

Table 2. ADS85x8 Configuration Settings

INTERFACE MODE	HARDWARE MODE ($\overline{HW}$/SW = 0)	SOFTWARE MODE ($\overline{HW}$/SW = 1)
Parallel ($\overline{PAR}$/SER = 0)	Configuration using pins and (optionally) Configuration register bits C30, C29, C[27:26], C22, C20, C18, C14, C13, and C[9:0]	Configuration using Configuration register bits C[31:0] only; status of pins 9, 11, 20, and 34 are disregarded (if C29 = C28 = 0)
Serial ($\overline{PAR}$/SER = 1)	Configuration using pins and (optionally) Configuration register bits C30, C29, C[27:26], C22, C20, C18, C13, and C[9:0]	Configuration using Configuration register bits C[31:0] only; status of pins 9, 11, 20, and 34 are disregarded (if C29 = C28 = 0)

9.3.2.2 Parallel Interface

To use the device with the parallel interface, hold the $\overline{\text{PAR}}$/SER pin low. The maximum achievable data throughput rate is 650 kSPS for the ADS8528, 600 kSPS for the ADS8548, and 510 kSPS for the ADS8568 in this case.

Access to the ADS85x8 is controlled as illustrated in Figure 2 and Figure 3.

9.3.2.3 Serial Interface

The serial interface mode is selected by setting the $\overline{\text{PAR}}$/SER pin high. In this case, each data transfer starts with the falling edge of the frame synchronization input ($\overline{\text{FS}}$). The conversion results are presented on the serial data output pins SDO_A (always active), SDO_B, SDO_C, and SDO_D, depending on the selections made using the SEL_xx pins. Starting with the most significant bit (MSB), the output data are changed with the SCLK falling edge. The ADS8528 and ADS8548 output data maintain the LSB-aligned, 16-bit format with leading bits containing the extended sign (see Table 3). Serial data input SDI are latched with the SCLK falling edge.

The serial interface can be used with one, two, or four output ports. Port SDO_B can be enabled using pin 27 (SEL_B) and ports SDO_C and SDO_D are enabled using pin 28 (SEL_CD). If all four serial data output ports are selected, data can be read with either two 16-bit data transfers or with a single 32-bit data transfer. The data of channels CH_x0 are available first, followed by data from channels CH_x1. The maximum achievable data throughput rate is 480 kSPS for the ADS8528, 450 kSPS for the ADS8548, and 400 kSPS for the ADS8568 in this case.

If the application allows a data transfer using two ports only, the SDO_A and SDO_B outputs are used. The device outputs data from channel CH_A0 followed by CH_A1, CH_C0, and CH_C1 on SDO_A; data from channel CH_B0 followed by CH_B1, CH_D0, and CH_D1 occur on SDO_B. In this case, a data transfer of four 16-bit words, two 32-bit words, or one continuous 64-bit word is supported. The maximum achievable data throughput rate is 360 kSPS for the ADS8528, 345 kSPS for the ADS8548, and 315 kSPS for the ADS8568 in this case.

The output SDO_A is always active and exclusively used if only one serial data port is used in the application. Data are available in the following order: CH_A0, CH_A1, CH_B0, CH_B1, CH_C0, CH_C1, CH_D0, and CH_D1. Data can be read using eight 16-bit transfers, four 32-bit transfers, two 64-bit transfers, or a single 128-bit transfer. The maximum achievable data throughput rate is 235 kSPS for the ADS8528, 230 kSPS for the ADS8548 and 215 kSPS for the ADS8568 in this case. Figure 1 and Figure 39 illustrate all possible scenarios in more detail.

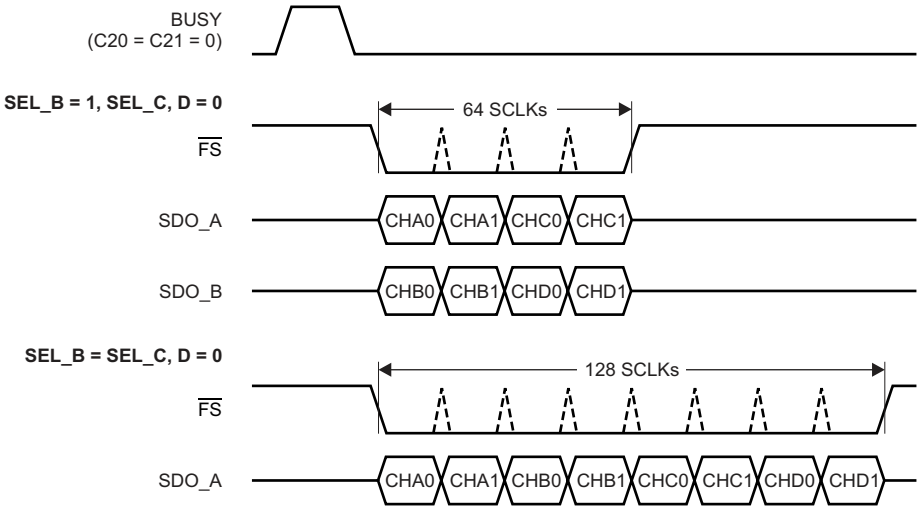


Figure 39. Data Output with One or Two Active SDOs (All Input Channels Active and Converted)

9.3.2.4 Output Data Format

The data output format of the ADS85x8 is binary twos complement, as shown in Table 3. For the ADS8528 and ADS8548 (that deliver 12-bit or 14-bit conversion results, respectively), the leading bits of either the 16-bit frame (serial interface) or the output pins (DB[15:12] for the ADS8528 or DB[15:14] for the ADS8548 in parallel mode) deliver a sign extension.

Table 3. Output Data Format

DESCRIPTION	INPUT VOLTAGE VALUE	BINARY CODE HEXADECIMAL CODE		
		ADS8528	ADSS8548	ADS8568
Positive full-scale	4 VREF or 2 VREF	0000 0111 1111 1111 07FFh	0001 1111 1111 1111 1FFFh	0111 1111 1111 1111 7FFFh
Midscale 0.5 LSB	VREF / (2 × resolution)	0000 0000 0000 0000 0000h	0000 0000 0000 0000 0000h	0000 0000 0000 0000 0000h
Midscale –0.5 LSB	–VREF / (2 × resolution)	1111 1111 1111 1111 FFFFh	1111 1111 1111 1111 FFFFh	1111 1111 1111 1111 FFFFh
Negative full-scale	–4 VREF or –2 VREF	1111 1000 0000 0000 F800h	1110 0000 0000 0000 E000h	1000 0000 0000 0000 8000h

9.4 Device Functional Modes

9.4.1 Hardware Mode

With the $\overline{\text{HW}}$/SW input (pin 41) set low, the device functions are controlled via the pins and, optionally, Configuration register bits C30, C29, C[27:26], C22, C20, C18, C14 (in parallel interface mode only), C13, and C[9:0].

The device can generally be used in hardware mode but can be switched to software mode to initialize or adjust the Configuration register settings (for example, the internal reference DAC) and back to hardware mode thereafter.

9.4.2 Software Mode

When the $\overline{\text{HW}}$/SW input is set high, the device operates in software mode with functionality set only by the Configuration register bits (corresponding pin settings are ignored).

If the parallel interface is used, an update of all Configuration register settings is performed by issuing two 16-bit write accesses on pins DB[15:0] (to avoid losing data, the entire sequence must be finished before starting a new conversion). Do not hold $\overline{\text{CS}}$ low during these two accesses. To enable the actual update of the register settings, the first bit (C31) must be set to 1 during the access.

If the serial interface is used, the update of the register contents can be performed continuously (combined read/write access). Optionally, to reduce the data transfer on the SDI line and the electromagnetic interference (EMI) of the system, the SDI input can be pulled low when a register update is not required. Figure 40 illustrates the different Configuration register update options.

Device Functional Modes (continued)

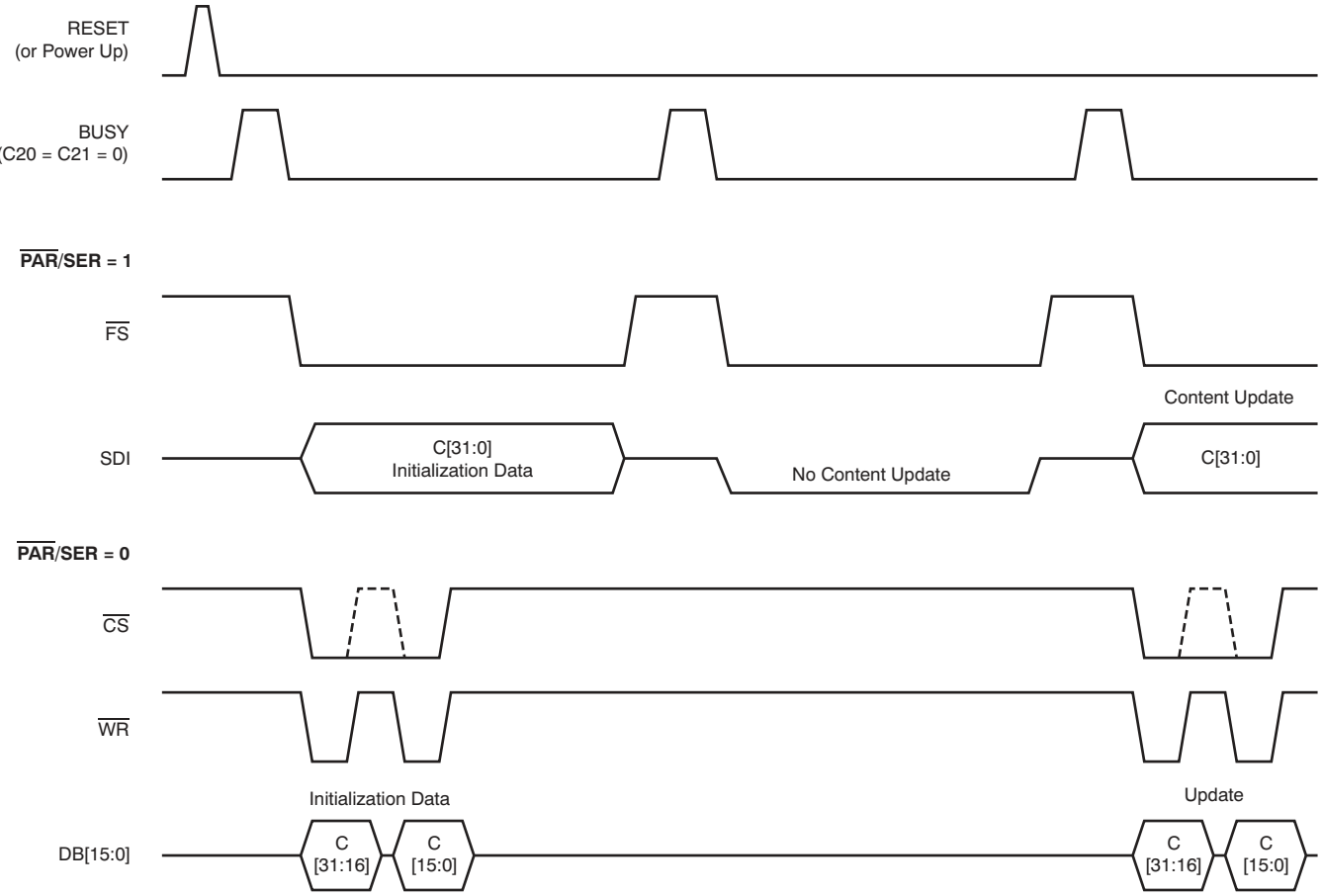


Figure 40. Configuration Register Update Options

Device Functional Modes (continued)

9.4.3 Daisy-Chain Mode

The serial interface of the ADS85x8 supports a daisy-chain feature that allows cascading of multiple devices to minimize the board space requirements and simplify routing of the data and control lines. In this case, the DB3/DCIN_A, DB2/DCIN_B, DB1/DCIN_C, and DB0/DCIN_D pins are used as serial data inputs for channels A, B, C, and D, respectively. Figure 41 shows an example of a daisy-chain connection of three devices sharing a common CONVST line to allow simultaneous sampling of 24 analog channels along with the corresponding timing diagram.

To activate the daisy-chain mode, the DCEN pin must be pulled high. However, the DCEN of the first device in the chain must remain low.

In applications where not all channel pairs are used, declaring the device with disabled channel pairs to be the first in the daisy-chain is recommended.

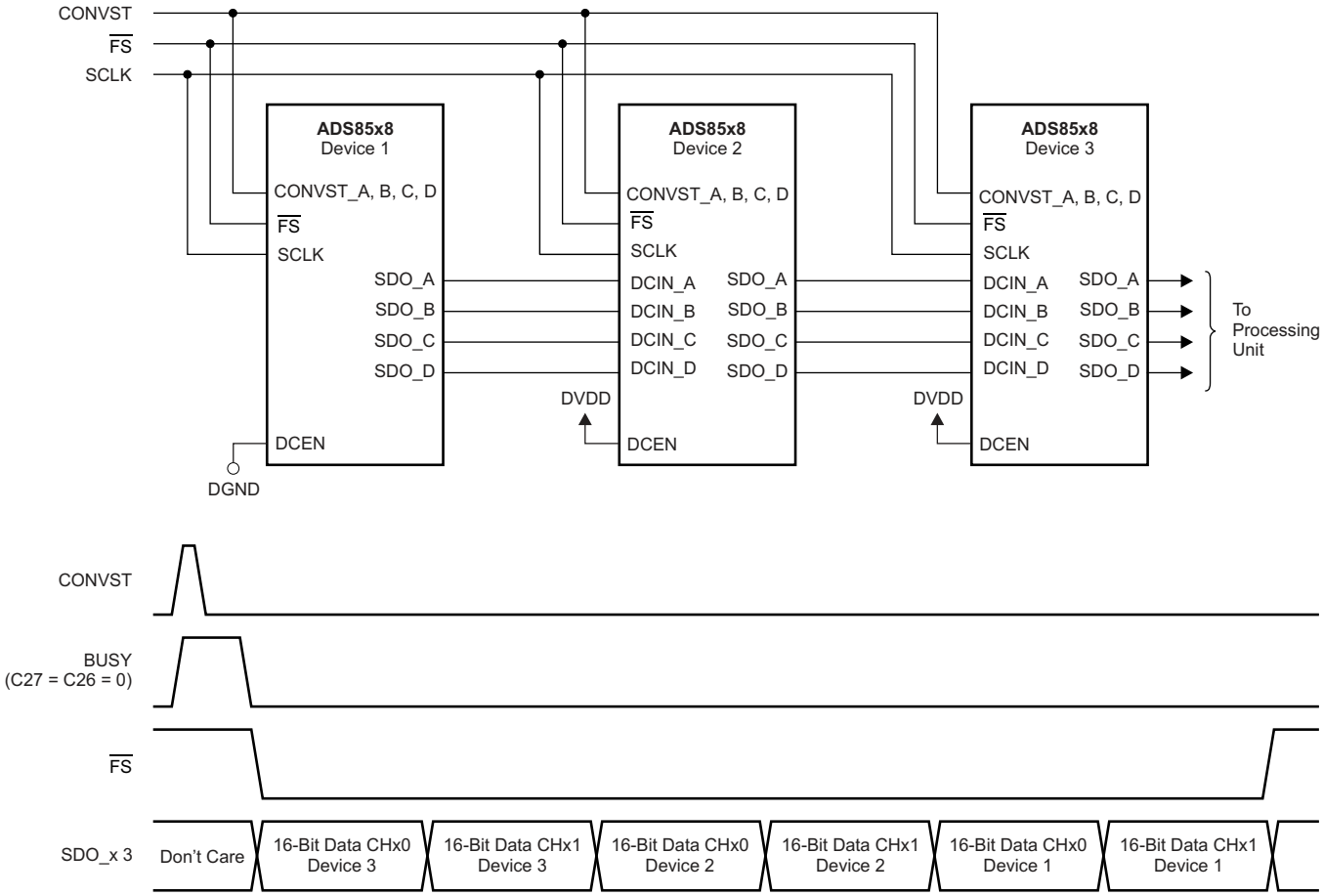


Figure 41. Example of Daisy-Chaining Three Devices

9.4.4 Reset and Power-Down Modes

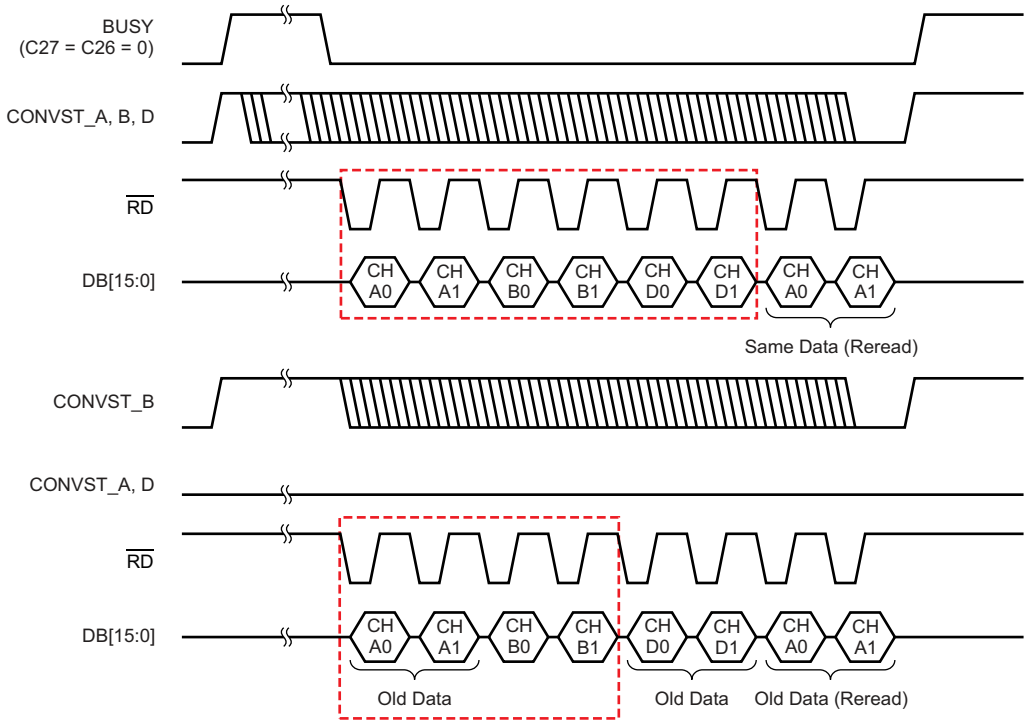
The device supports two reset mechanisms: a power-on reset (POR) and a pin-controlled reset (RESET) that can be issued using pin 10. Both the POR and RESET function as a master reset that causes any ongoing conversion to be interrupted, the Configuration register content to be set to the default value, and all channels to be switched into sample mode.

When the device is powered up, POR sets the device in default mode when AVDD reaches 1.2 V. In normal operation, glitches on the AVDD supply below this threshold trigger a device reset.

Device Functional Modes (continued)

The entire device, except for the digital interface, can be powered down by pulling the $\overline{\text{STBY}}$ pin low (pin 9). Data can be retrieved when in standby mode because the digital interface section remains active. To power the device on again, the $\overline{\text{STBY}}$ pin must be brought high. The device is ready to start a new conversion after the 10 ms required to activate and settle the internal circuitry. This user-controlled approach can be used in applications that require lower data throughput rates at lowest power dissipation. The content of CONFIG is not changed during standby mode and is not required to perform a reset after returning to normal operation.

Although standby mode affects the entire device, each device channel pair (except channel pair A, which is the master channel pair and is always active) can also be individually switched off by setting the Configuration register bits C22, C20, and C18 (PD_x). If a certain channel pair is powered-down in this manner, the output register is disabled as shown in Figure 42. When reactivated, the relevant channel pair requires 10 ms to fully settle before starting a new conversion.



(1) Channel pair C disabled (PD_C = 1), $\overline{\text{CS}}$ = 0.

NOTE: Boxed areas indicate the minimum required frame to acquire all new conversion results. The read access can be interrupted, thereafter.

Figure 42. Example of Data Output Order With Channel Pair C Powered Down(1)

Device Functional Modes (continued)

Auto-sleep mode is enabled by pulling pin 36 (ASLEEP) high. If auto-sleep mode is enabled, the ADS85x8 automatically reduce the current requirement to 7 mA (IAVDD) after finishing a conversion; thus, the end of conversion actually activates this power-down mode. Triggering a new conversion by applying a positive CONVST_x edge starts the wake-up sequence to put the device back into normal operation. At the beginning, all required building blocks power-up and the sampling switches close again. This sequence takes six to seven conversion clock cycles of either the internal or external clock. During this time, the sampling capacitance must be recharged to the input signal with the required 12-bit, 14-bit, or 16-bit accuracy level. The bandwidth requirements of the driving operational amplifier described in the *Analog Inputs* section must be fulfilled. At the end of the sequence, the new sample is taken and the conversion starts automatically, as shown in Figure 43. Therefore, a complete conversion process takes 25 to 26 conversion clock cycles; thus, the maximum throughput rate in auto-sleep mode is reduced to a maximum of 400 kSPS for the ADS8528, 375 kSPS for the ADS8548, and 330 kSPS for the ADS8568 in serial interface mode. In parallel mode, the maximum data rates are 510 kSPS for the ADS8528, 470 kSPS for the ADS8548, and 400 kSPS for the ADS8568. If enabled, the internal reference remains active during auto-sleep mode. Table 4 compares the analog current requirements of the device in different modes.

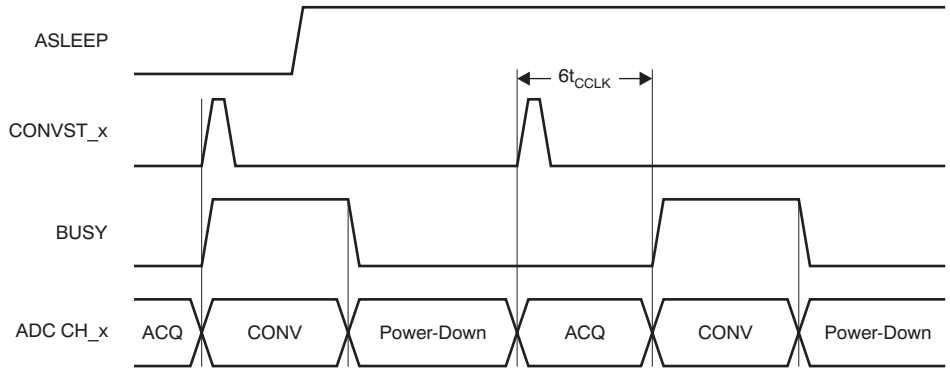


Figure 43. Auto-Sleep Power-Down Mode

Table 4. Maximum Analog Current (IAVDD) Demand of the ADS85x8

OPERATIONAL MODE	ANALOG CURRENT (IAVDD)	ENABLED, DISABLED BY	ACTIVATED BY	NORMAL OPERATION TO POWER-DOWN DELAY	RESUMED BY	POWER-UP TO NORMAL OPERATION DELAY	POWER-UP TO NEXT CONVERSION START TIME
Normal operation	12.5 mA/ch pair at maximum data rate	Power on Power off	CONVST_x	—	—	—	—
Auto-sleep	1.75 mA/ch pair	ASLEEP = 1 ASLEEP = 0	Each end of conversion	At BUSY falling edge	CONVST_x	Immediate	7 × t_{CCLK} max
Power-down of channel pair X	16 µA (channel pair X)	$\overline{HW}$/SW = 1 $\overline{HW}$/SW = 0	PD_x = 1 (CONFIG bit)	Immediate	PD_x = 0 (CONFIG bit)	Immediate after completing CONFIG update	10 ms
Power-down (entire device)	30 µA	Power on Power off	$\overline{STBY}$ = 0	Immediate	$\overline{STBY}$ = 1	Immediate	10 ms

9.5 Register Maps

9.5.1 Configuration (CONFIG) Register

The Configuration register settings can only be changed in software mode and are not affected when switching to hardware mode thereafter. The register values are independent from input pin settings. Changes are active with the second $\overline{WR}$ rising edge in parallel interface mode or with the 32nd SCLK falling edge of the access where the register content is updated in serial mode. The CONFIG content is defined in CONFIG: Configuration Register (default = 000003FFh).

9.5.1.1 CONFIG: Configuration Register (default = 000003FFh)

Figure 44. CONFIG Register

31	30	29	28	27	26	25	24
WRITE_EN	READ_EN	CLKSEL	CLKOUT	BUSY/INT	BUSY POL	STBY	RANGE_A
23	22	21	20	19	18	17	16
RANGE_B	PD_B	RANGE_C	PD_C	RANGE_D	PD_D	Don't care	Don't care
15	14	13	12	11	10	9	8
REFEN	REFBUF	VREF	Don't care	Don't care	Don't care	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit 31 **WRITE_EN: Register update enable**

This bit is not active in hardware mode.
0 = Register content update disabled (default)
1 = Register content update enabled

Bit 30 **READ_EN: Register read-out access enable**

This bit is not active in hardware mode.
0 = Normal operation (conversion results available on SDO_A)
1 = Configuration register contents output on SDO_A with next two accesses (READ_EN automatically resets to 0 thereafter)

Bit 29 **CLKSEL: Conversion clock selector**

This bit is active in hardware mode.
0 = Normal operation with internal conversion clock; mandatory in hardware mode (default)
1 = External conversion clock applied through pin 34 (XCLK) is used (conversion takes 19 clock cycles)

Bit 28 **CLKOUT: Internal conversion clock output enable**

This bit is not active in hardware mode.
0 = Normal operation (default)
1 = Internal conversion clock is available at pin 34

Bit 27 **BUSY/INT: Busy/interrupt selector**

This bit is active in hardware mode.
0 = BUSY/INT pin is in BUSY mode (default)
1 = BUSY/INT pin is in interrupt mode (INT); can only be used if all eight channels are sampled simultaneously (all CONVST_x tied together)

Bit 26 **BUSY POL: BUSY/INT polarity selector**

This bit is active in hardware mode.
0 = BUSY/INT active high (default)
1 = BUSY/INT active low

Bit 25 **$\overline{\text{STBY}}$: Power-down enable**

This bit is not active in hardware mode.
0 = Normal operation (default)
1 = Entire device is powered down (including the internal clock and reference)

Bit 24 **RANGE_A: Input voltage range selector for channel pair A**

This bit is not active in hardware mode.
0 = Input voltage range: 4 VREF (default)
1 = Input voltage range: 2 VREF

Bit 23 **RANGE_B: Input voltage range selector for channel pair B**

This bit is not active in hardware mode.
0 = Input voltage range: 4 VREF (default)
1 = Input voltage range: 2 VREF

Bit 22 **PD_B: Power-down enable for channel pair B**

This bit is active in hardware mode.
0 = Normal operation (default)
1 = Channel pair B is powered down

Bit 21 **RANGE_C: Input voltage range selector for channel pair C**

This bit is not active in hardware mode.
0 = Input voltage range: 4 VREF (default)
1 = Input voltage range: 2 VREF

Bit 20 **PD_C: Power-down enable for channel pair C**

This bit is active in hardware mode.
0 = Normal operation (default)
1 = Channel pair C is powered down

Bit 19 **RANGE_D: Input voltage range selector for channel pair D**

This bit is not active in hardware mode.
0 = Input voltage range: 4 VREF (default)
1 = Input voltage range: 2 VREF

Bit 18 **PD_D: Power-down enable for channel pair D**

This bit is active in hardware mode.
0 = Normal operation (default)
1 = Channel pair D is powered down

Bits 17-16 **Not used (default = 0)**

Bit 15 **REF_EN: Internal reference enable**

This bit is not active in hardware mode.
0 = Internal reference source disabled (default)
1 = Internal reference source enabled

Bit 14 **REFBUF: Internal reference buffers disable**

This bit is active in hardware mode if the parallel interface is used.
0 = Internal reference buffers enabled (default)
1 = Internal reference buffers disabled

Bit 13 **VREF: Internal reference voltage selector**

This bit is active in hardware mode.
0 = Internal reference voltage set to 2.5 V (default)
1 = Internal reference voltage set to 3.0 V

Bits 12-10 **Not used (default = 0)**

Bits 9-0 **D[9:0]: REFDAC setting bits**

These bits are active in hardware mode.
These bits correspond to the settings of the internal reference DACs (compare to the *Reference* section). Bit 9 is the MSB of the DAC. Default value is 3FFh (2.5 V, typ).

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ADS85x8 enables high-precision measurement of up to eight analog signals simultaneously. The *Typical Application* section summarizes some of the typical use cases for the ADS85x8 and the main steps and components used around the analog-to-digital converter (ADC).

10.2 Typical Application

The accurate measurement of electrical variables in a power grid is extremely critical because this measurement helps determine the operating status and running quality of the grid. Such accurate measurements also help diagnose problems with the power network, thereby enabling prompt solutions and minimizing down time. The key electrical variables measured in 3-phase power systems are the three line voltages, the neutral voltage at the load, the three line currents, and the neutral return current; see Figure 45. These variables enable metrology and power automation systems to determine the amplitude, frequency, and phase information in order to perform harmonic analysis, power factor calculations, and power quality assessment, among others.

Typical Application (continued)

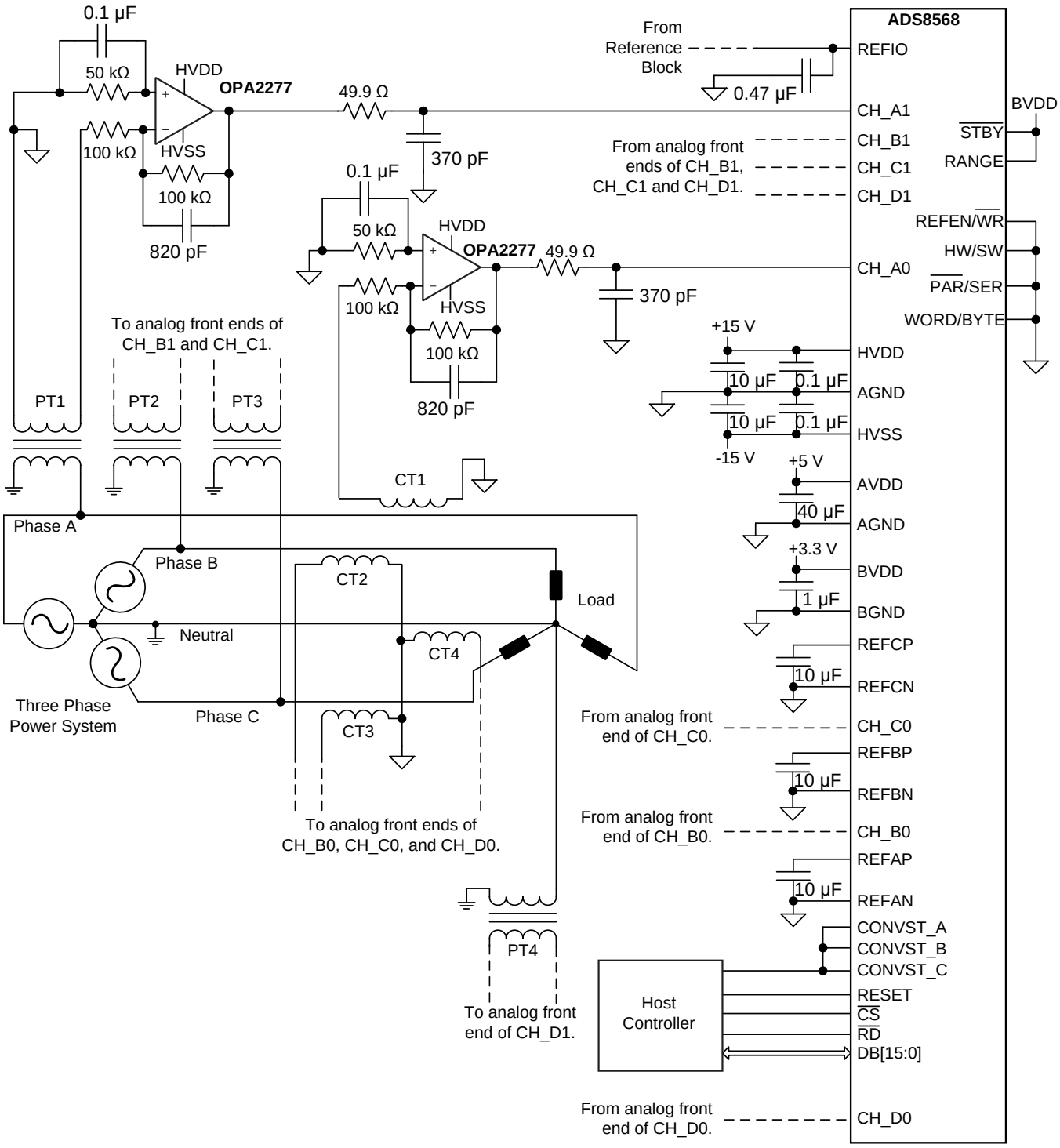


Figure 45. Simultaneous Acquisition of Voltage and Current in a 3-Phase Power System

Typical Application (continued)

10.2.1 Design Requirements

To begin the design process, a few parameters must be decided upon. The designer must know the following:

- Output range of the potential transformers (elements labeled PT1, PT2, and PT3 in Figure 45)
- Output range of the current transformers (elements labeled CT1, CT2, and CT3 in Figure 45)
- Input impedance required from the analog front-end for each channel
- Fundamental frequency of the power system
- Number of harmonics that must be acquired, and
- Type of signal conditioning required from the analog front-end for each channel

10.2.2 Detailed Design Procedure

Figure 46 shows the topology chosen to meet the design requirements.

NOTE

A feedback capacitor C_F is included in order to provide a low-pass filter characteristic and attenuate signals outside the band of interest.

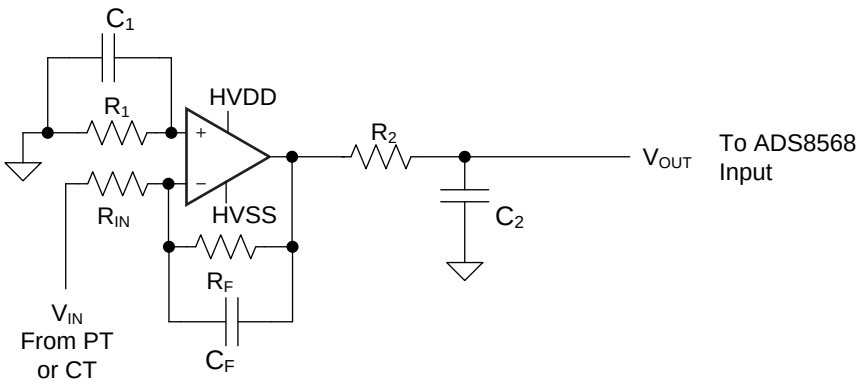


Figure 46. Op Amp in an Inverting Configuration

The potential transformers and current transformers used in the system depicted in Figure 45 provide the eight inputs required. These transformers have a ±10-V output range. Although the PT and CT elements provide isolation from the power system, the value of R_{IN} is selected as 100 kΩ in order to provide an additional, high-impedance safety element in the current path leading up to the input of the ADC. Moreover, selecting a low-frequency gain of –1 V/V (as shown in Equation 5) provides a ±10-V output that can be fed into the ADS8568; therefore, the value of R_F is selected as 100 kΩ too.

$$V_{out}\big|_{Low\ f} = -\frac{R_F}{R_{IN}}V_{in} = -\frac{100\ k\Omega}{100\ k\Omega}V_{in} = -V_{in} \tag{5}$$

The primary goal of the acquisition system depicted in Figure 45 is to measure up to 20 harmonics in a 60-Hz power network. With this goal in mind, the analog front-end must have sufficient bandwidth to measure signals up to 1260 Hz as shown in Equation 6.

$$f_{MAX} = (20+1)60\,Hz = 1260\,Hz \tag{6}$$

Based on the bandwidth from in Equation 6, the ADS8568 is set to simultaneously sample all six channels at 15.36 kSPS, thus providing enough samples to clearly resolve even the highest harmonic required.

The passband of the configuration shown in Figure 46 is determined by the –3-dB frequency according to Equation 7. The value of C_F is selected as 820 pF because C_F is a standard capacitance value available in 0603 size (surface-mount component) and such values, combined with that of R_F, result in sufficient bandwidth to accommodate the required 20 harmonics (at 60 Hz).

Typical Application (continued)

$$f_{-3dB} = \frac{1}{2\pi R_F C_F} = \frac{1}{2\pi (100\ k\Omega)(820\ pF)} = 1940\ Hz \quad (7)$$

The value of R_1 is selected as the parallel combination of R_{IN} and R_F to prevent the input bias current of the operational amplifier from generating an offset error.

The value of component C_1 is chosen as 0.1 µF to provide a low-impedance path for noise signals that can be picked up by R_1, thus improving the EMI robustness and noise performance of the system.

The OPA2277 is chosen for its low input offset voltage, low drift, bipolar swing, sufficient gain-bandwidth product, and low quiescent current. For additional information on the procedure to select SAR ADC input drivers, see the TIPD151 verified design guide, *16-Bit 100-KSPS 4-Channel Multiplexed Data Acquisition System Design Guide*.

The charge injection damping circuit is composed by R_2 (49.9 Ω) and C_2 (370 pF); these components reject high-frequency noise and meet the settling requirements of the ADS8568 input.

Figure 47 shows the reference block used in this design.

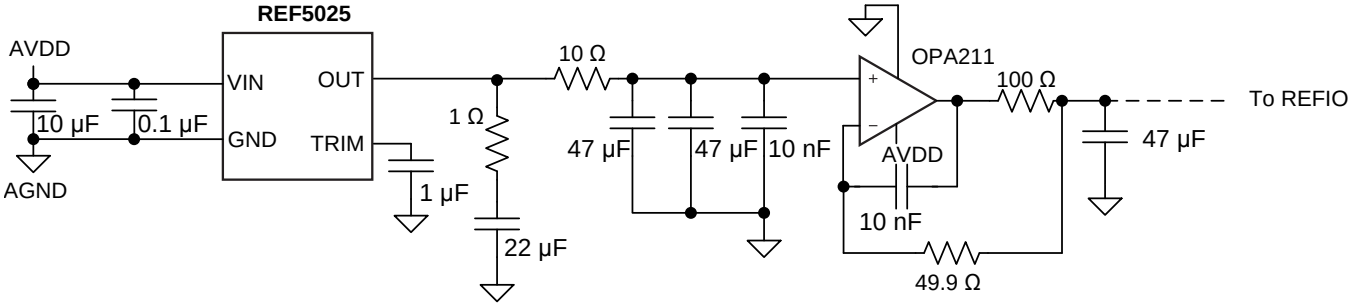


Figure 47. Reference Block

For more information on the design of charge injection damping circuits and reference driving circuits for SAR ADCs, see the TIPD149 verified design reference guide, *Power-Optimized 16-Bit 1-MSPS Data Acquisition Block for Lowest Distortion and Noise*.

Typical Application (continued)

10.2.3 Application Curve

Figure 48 shows the frequency spectrum of the data acquired by the ADS8568 for a sinusoidal, 20-V_{PP} input at 60 Hz.

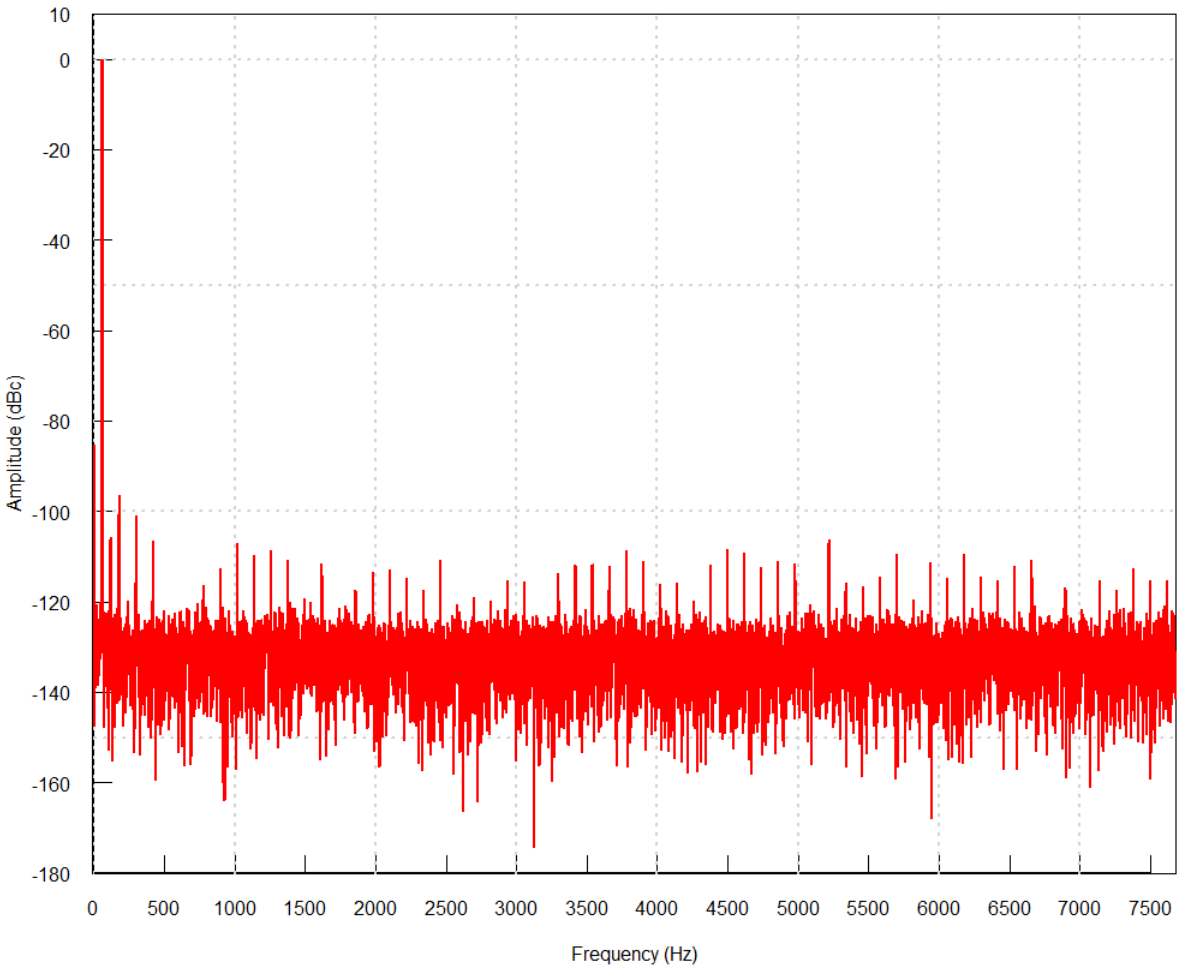


Figure 48. Frequency Spectrum for a Sinusoidal 20-V_{PP} Signal at 60 Hz

The ac performance parameters are:

- SNR: 91.16 dB
- THD: –94.34 dB
- SNDR: 89.45 dB
- SFDR: 96.56 dB

11 Power Supply Recommendations

The ADS85x8 require four separate supplies: an analog supply for the ADC (AVDD), the buffer I/O supply for the digital interface (DVDD), and the two high-voltage supplies driving the analog input circuitry (HVDD and HVSS). Generally, there are no specific requirements with regard to the power sequencing of the device. However, when HVDD is supplied before AVDD, the internal electrostatic discharge (ESD) structure conducts, increasing the IHVDD beyond the specified value until AVDD is applied.

The AVDD supply provides power to the internal circuitry of the ADC. If run at maximum data rate, the IAVDD is too high to allow use of a passive filter between the digital board supply of the application and the AVDD pins. A linear regulator is recommended to generate the analog supply voltage. Decouple each AVDD pin to AGND with a 100-nF ceramic capacitor. In addition, place a single 10-µF capacitor close to the device but without compromising the placement of the smaller capacitors. Optionally, each supply pin can be decoupled using a 1-µF ceramic capacitor without the requirement of the additional 10-µF capacitor.

The DVDD supply is only used to drive the digital I/O buffers and allows seamless interface with most state-of-the-art processors and controllers. Resulting from the low IDVDD value, a 10-Ω series resistor can be used on the DVDD pin to reduce the noise energy from the external digital circuitry influencing the performance of the device. Place a 1-µF bypass ceramic capacitor (or alternatively, a pair of 100-nF and 10-µF capacitors) between pins 24 and 25.

The high-voltage supplies (HVSS and HVDD) are connected to the analog inputs. These supplies are not required to be of symmetrical nature with regard to AGND. Noise and glitches on these supplies directly couple into the input signals. Place a 100-nF ceramic decoupling capacitor, located as close to the device as possible, between pins 1, 48, and AGND. An additional 10-µF capacitor is used that must be placed close to the device but without compromising the placement of the smaller capacitors.

12 Layout

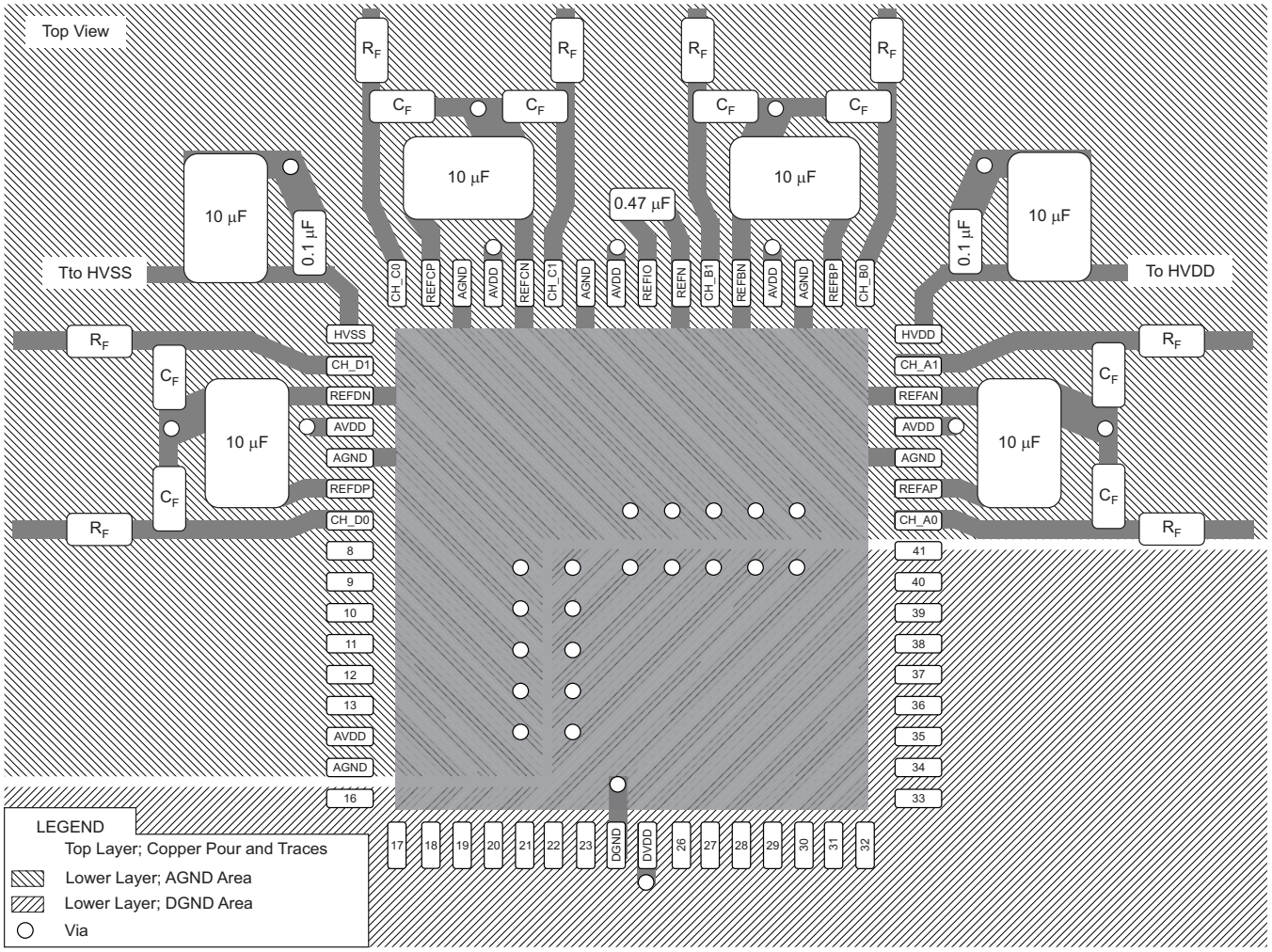
12.1 Layout Guidelines

All ground pins must be connected to a clean ground reference. Keep this connection as short as possible to minimize the inductance of these paths. Using vias is recommended to connect the pads directly to the corresponding ground plane. In designs without ground planes, keep the ground trace as wide and as short as possible to reduce inductance. Avoid connections that are too close to the grounding point of a microcontroller or digital signal processor.

Depending on the circuit density on the board, placement of the analog and digital components, and the related current loops, a single solid ground plane for the entire printed circuit board (PCB) or dedicated analog and digital ground areas can be used. In case of separated ground areas, ensure that a low-impedance connection is between the analog and digital ground of the ADC by placing a bridge underneath (or next to) the ADC. Otherwise, even short undershoots on the digital interface with a value less than –300 mV lead to the conduction of ESD diodes, causing current to flow through the substrate and either degrading the analog performance or even damaging the device. Using a common ground plane underneath the device is recommended as a local ground reference for all xGND pins; see Figure 49. During PCB layout, care must be taken to avoid any return currents crossing sensitive analog areas or signals.

12.2 Layout Example

Figure 49 shows a layout recommendation for the ADS85x8 along with the proper decoupling and reference capacitors placement and connections. The layout recommendation takes into account the actual size of the components used.



(1) All AVDD and DVDD decoupling capacitors are placed on the bottom layer underneath the device power-supply pins and are connected by vias. All 100-nF ceramic capacitors are placed as close as possible to the device and the 10-µF capacitors are also placed close but without compromising the placement of the smaller capacitors.

Figure 49. Layout Recommendation

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- OPA2277 Data Sheet, SBOS079
- REF5025 Data Sheet, SBOS410
- TIPD151 Verified Design Guide, *16-Bit 100-KSPS 4-Channel Multiplexed Data Acquisition System Design Guide*
- TIPD149 Verified Design Reference Guide, *Power-Optimized 16-Bit 1-MSPS Data Acquisition Block for Lowest Distortion and Noise*

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS8528	Click here	Click here	Click here	Click here	Click here
ADS8548	Click here	Click here	Click here	Click here	Click here
ADS8568	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8528SPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8528	Samples
ADS8528SPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8528	Samples
ADS8528SRGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8528	Samples
ADS8528SRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8528	Samples
ADS8548SPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8548	Samples
ADS8548SPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8548	Samples
ADS8548SRGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8548	Samples
ADS8548SRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8548	Samples
ADS8568SPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8568	Samples
ADS8568SPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8568	Samples
ADS8568SRGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8568	Samples
ADS8568SRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8568	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

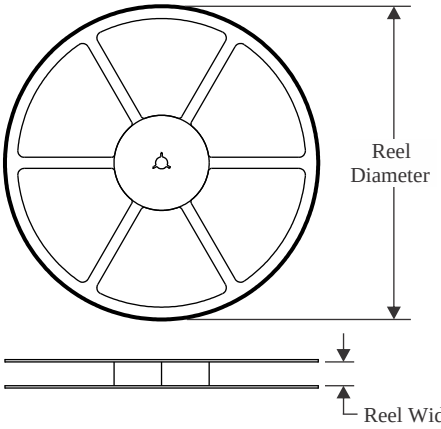
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

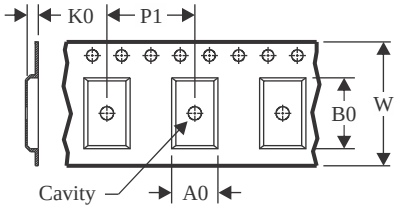
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

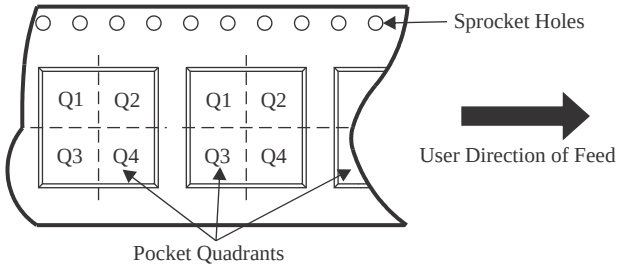


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

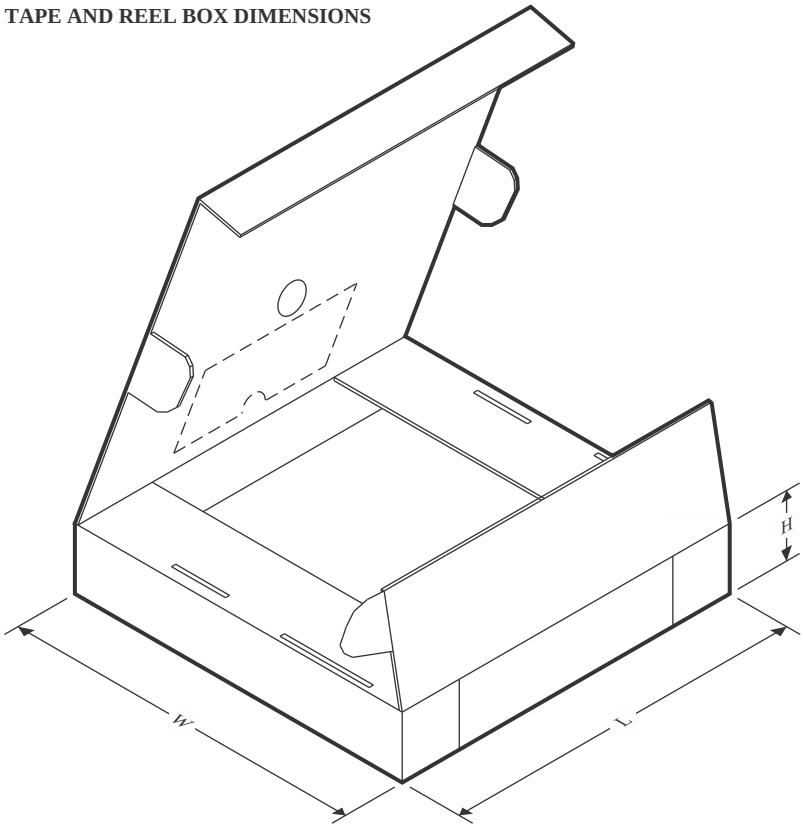
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8528SPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
ADS8528SRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
ADS8528SRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
ADS8548SPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
ADS8548SRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
ADS8548SRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
ADS8568SPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
ADS8568SRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
ADS8568SRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

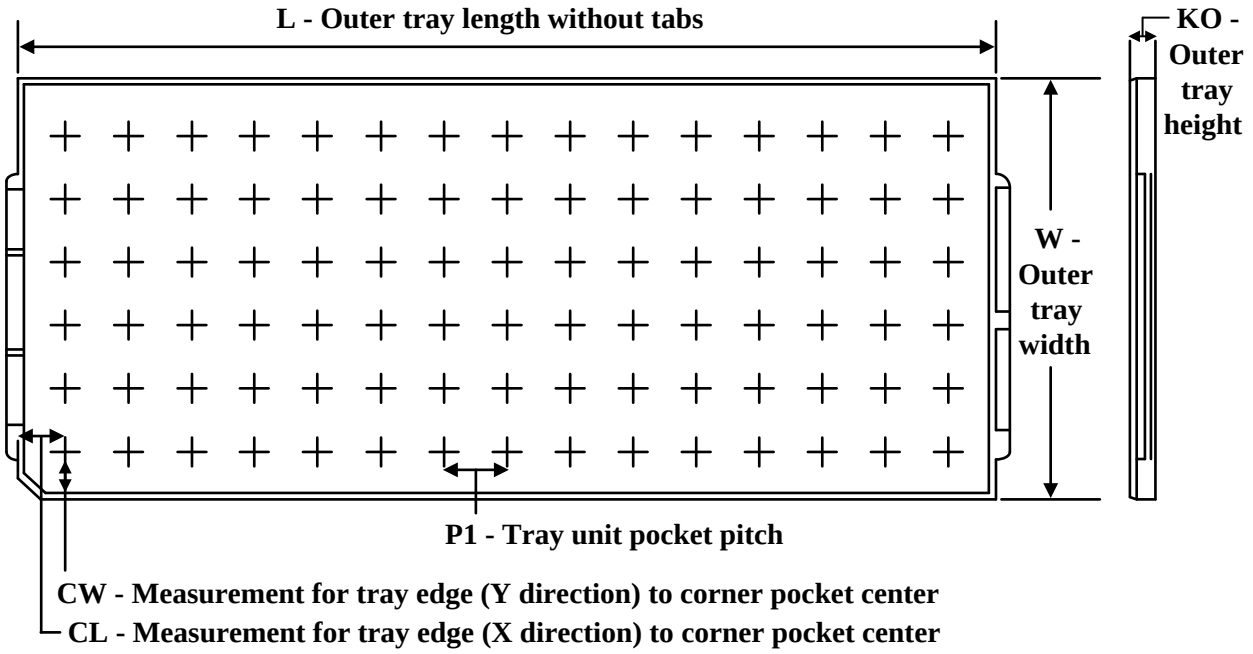
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8528SPMR	LQFP	PM	64	1000	350.0	350.0	43.0
ADS8528SRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
ADS8528SRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
ADS8548SPMR	LQFP	PM	64	1000	350.0	350.0	43.0
ADS8548SRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
ADS8548SRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
ADS8568SPMR	LQFP	PM	64	1000	350.0	350.0	43.0
ADS8568SRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
ADS8568SRGCT	VQFN	RGC	64	250	210.0	185.0	35.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

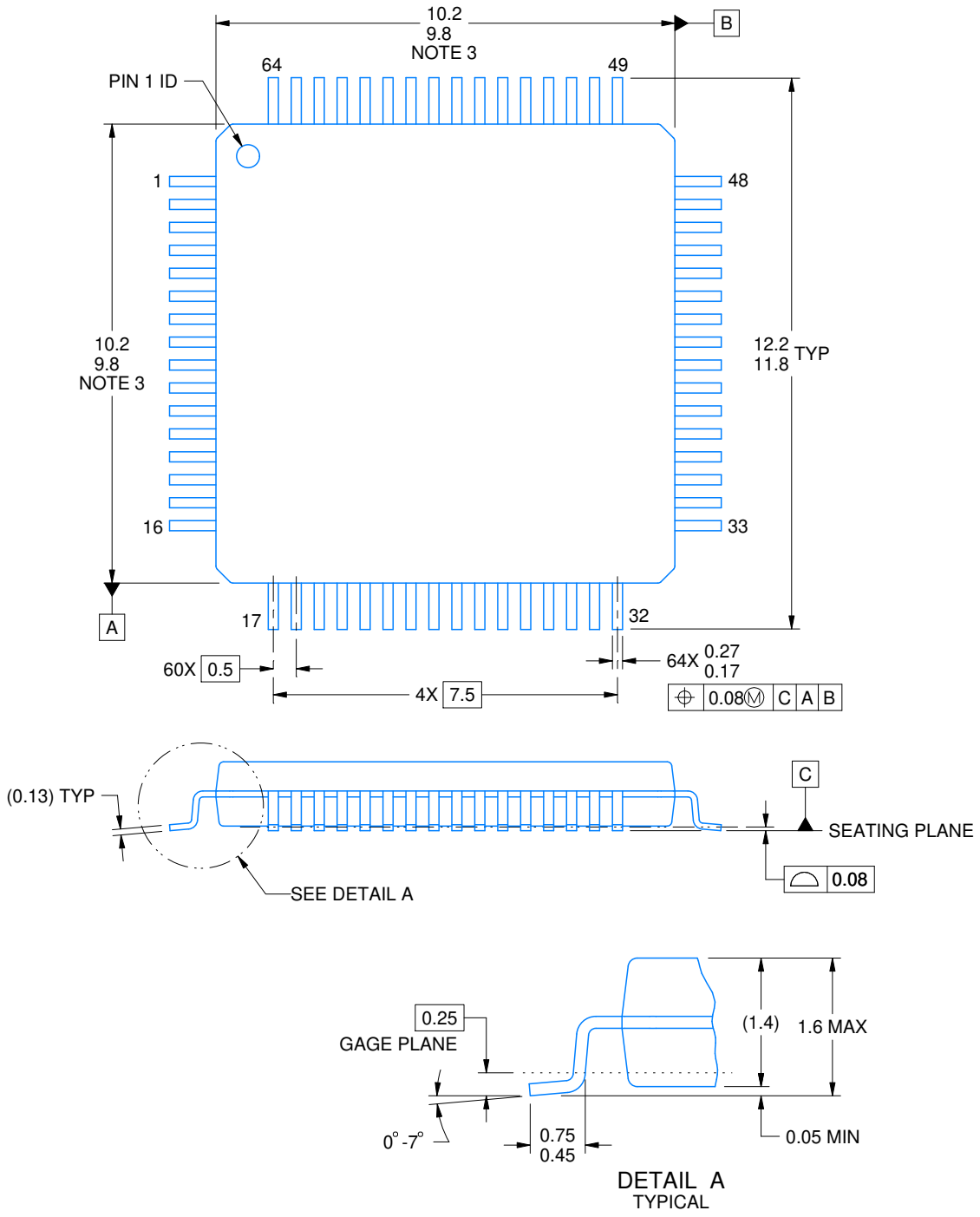
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS8528SPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
ADS8548SPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
ADS8568SPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13

PACKAGE OUTLINE

PM0064A

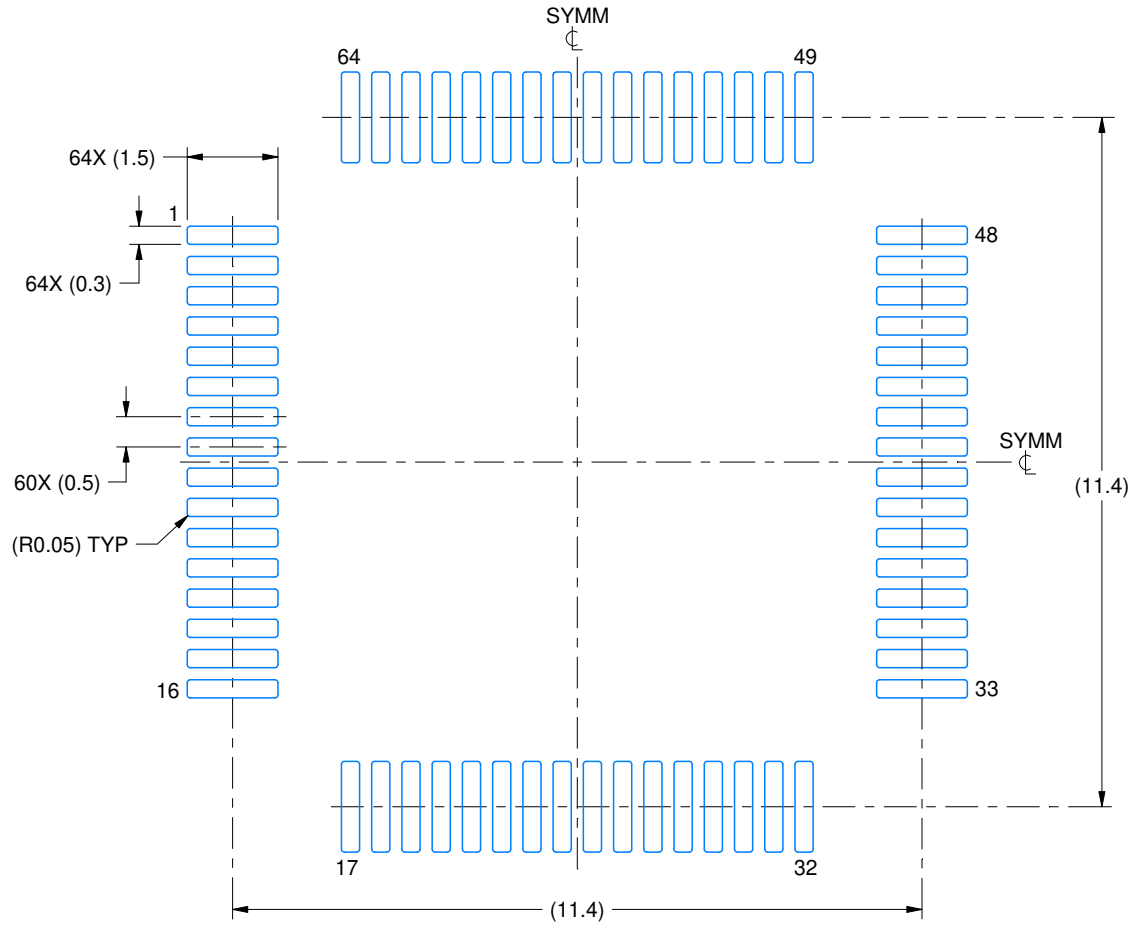
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

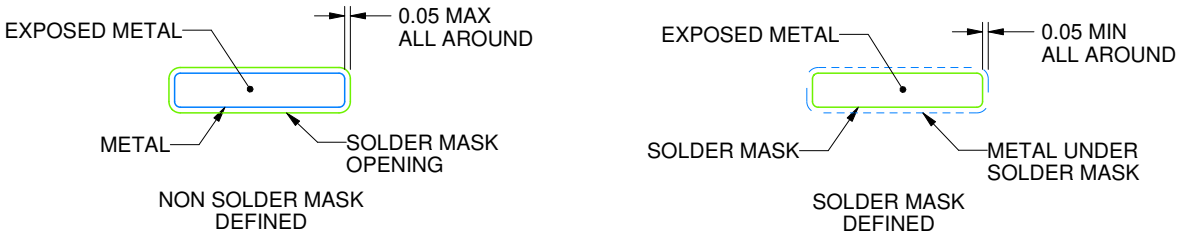


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

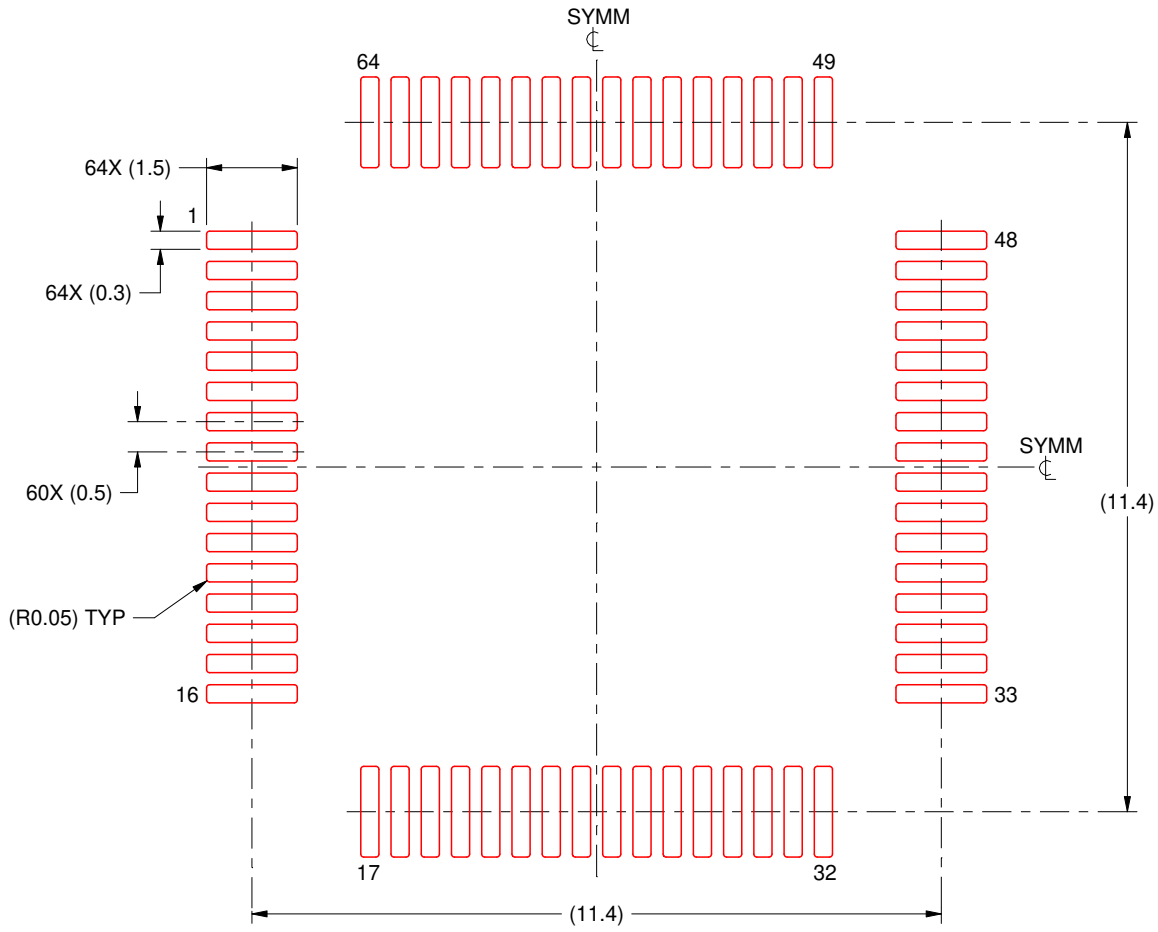


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

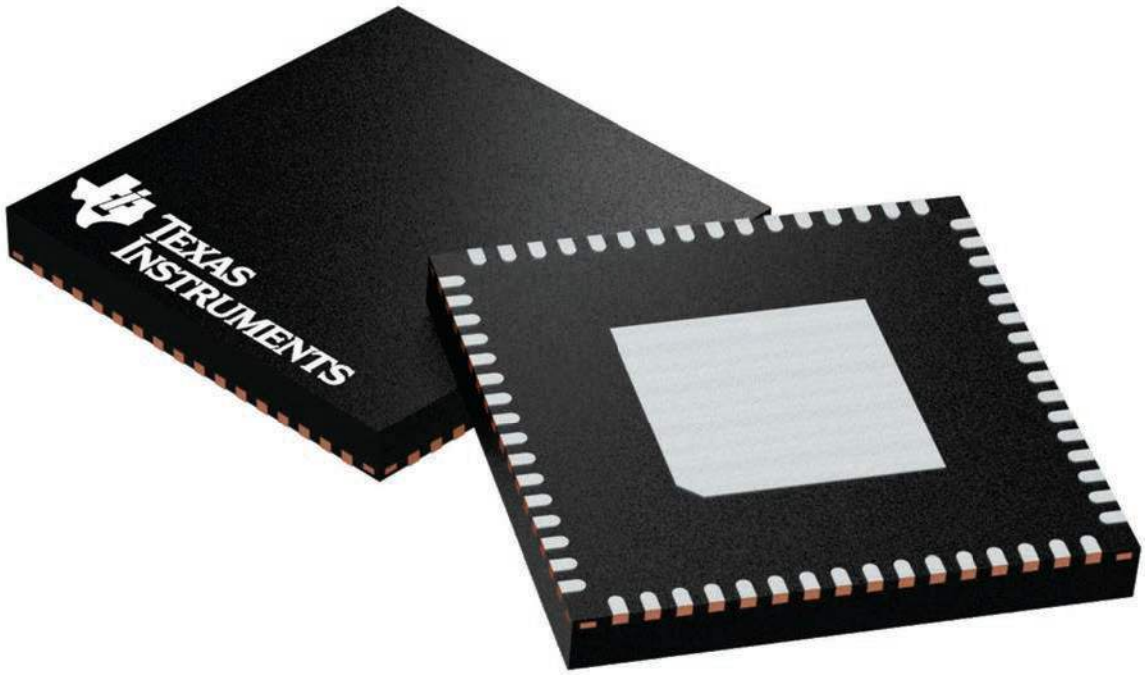
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

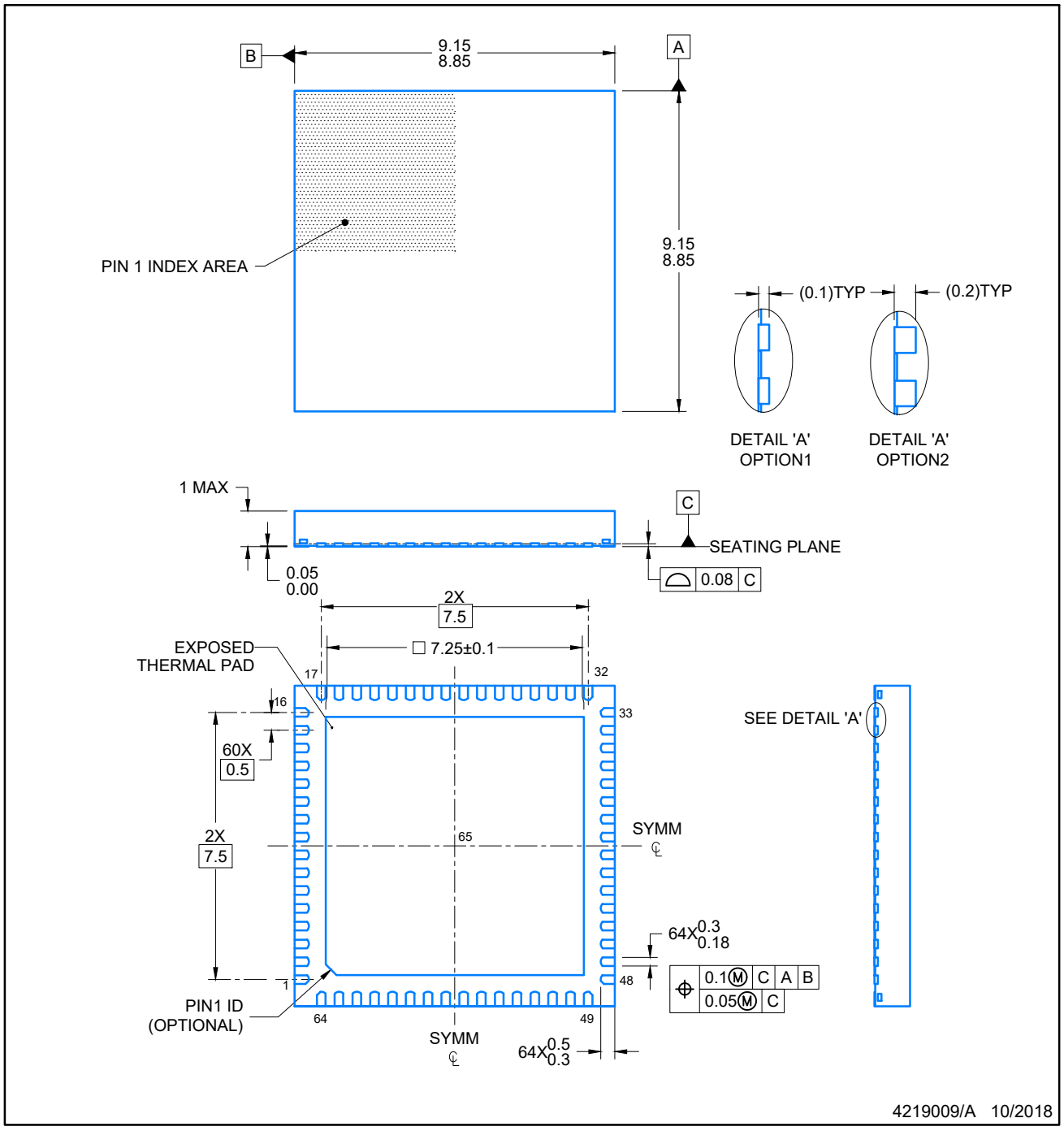
4224597/A

PACKAGE OUTLINE

RGC0064A

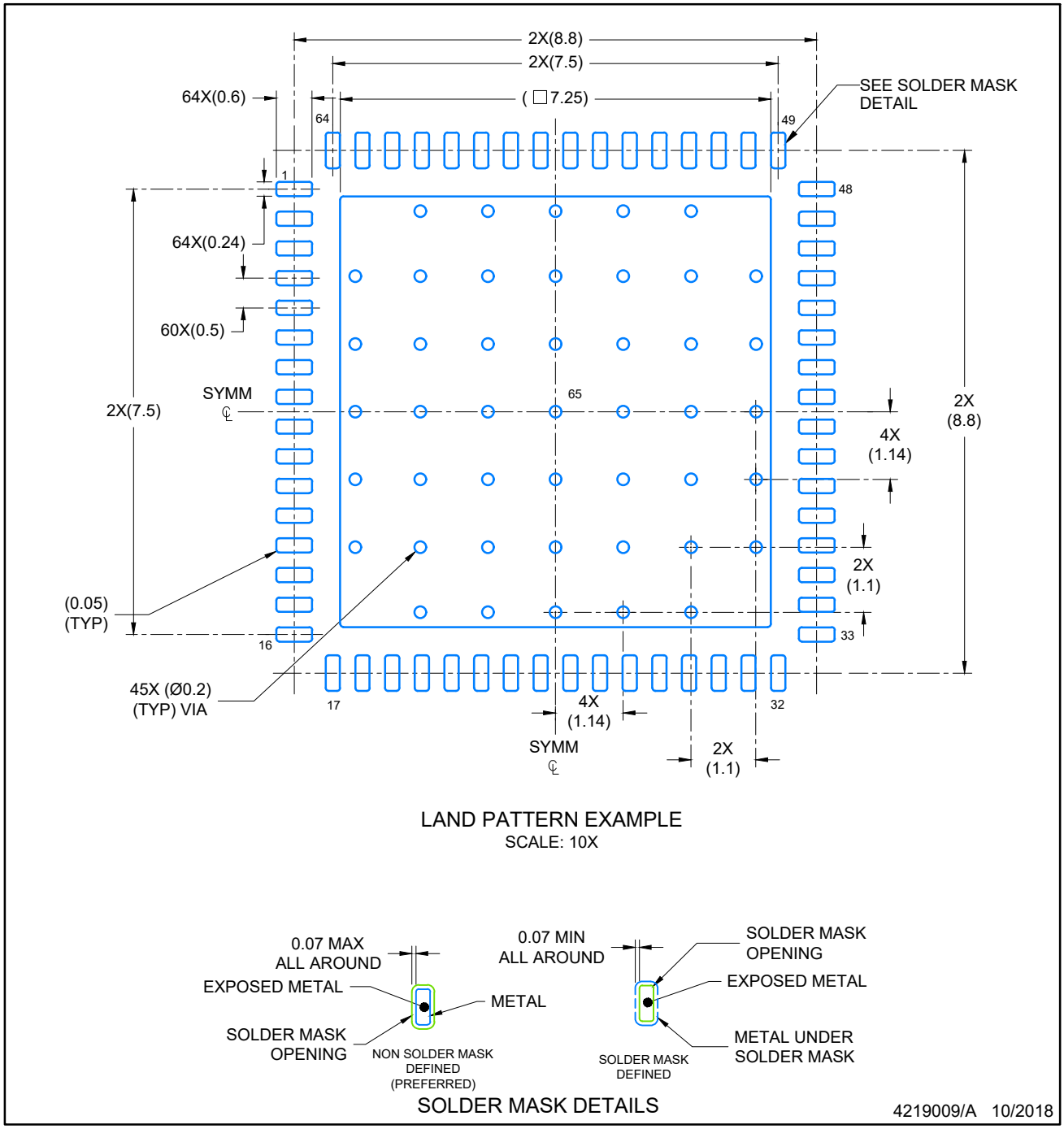
VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

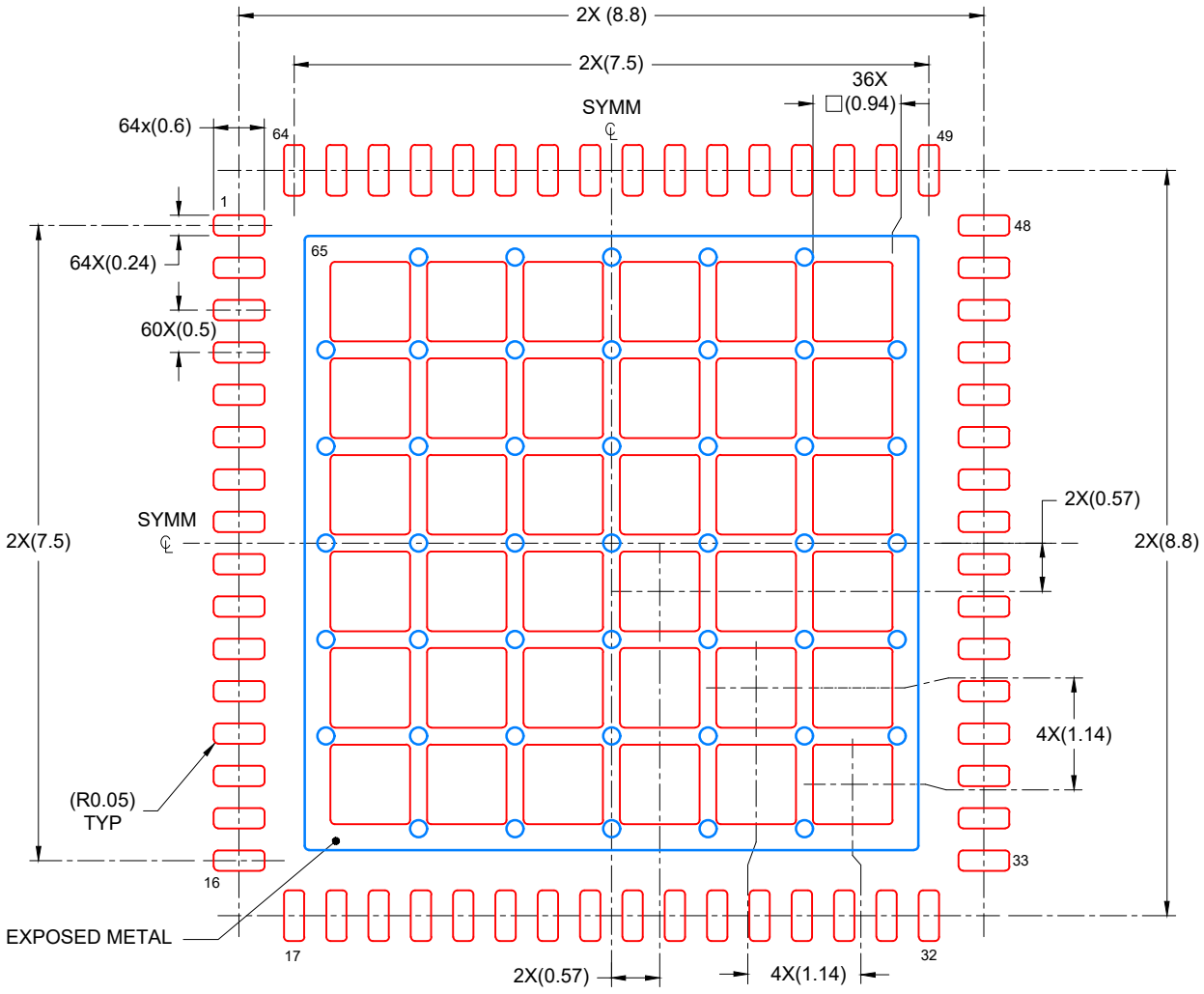
SCALE: 10X

SOLDER MASK DETAILS

4219009/A 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED COVERAGE BY AREA
SCALE: 12X

4219009/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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