TC4626/TC4627

Power CMOS Drivers With Voltage Tripler

Features:

- Power Driver With On-Board Voltage Booster
- Low I_{DD}: < 4 mA
- Small Package: 8-Pin PDIP
- Undervoltage Circuitry
- Fast Rise/Fall Time: <40 ns @1000 pF
- Below-Rail Input Protection

Applications:

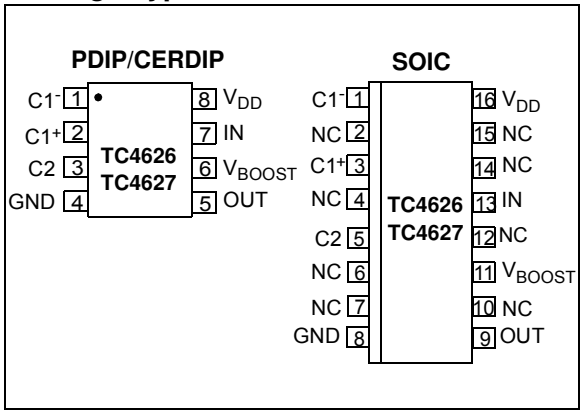
- Raises 5V to drive higher – Vgs (ON) MOSFETs
- Eliminates one system power supply

General Description:

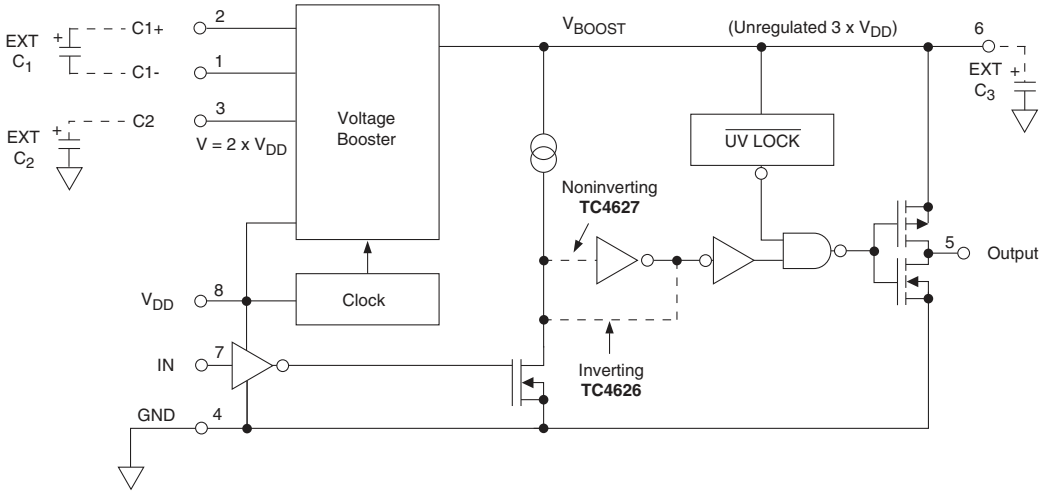
The TC4626/TC4627 are single CMOS high-speed drivers with an on-board voltage boost circuit. These parts work with an input supply voltage from 4 to 6 volts. The internal voltage booster will produce a V_{BOOST} potential up to 12 volts above V_{IN}. This V_{BOOST} is not regulated, so its voltage is dependent on the input V_{DD} voltage and output drive loading requirements. An internal undervoltage lockout circuit keeps the output in a low state when V_{BOOST} drops below 7.8 volts. Output is enabled when V_{BOOST} is above 11.3 volts.

Note: Check the Microchip web site for available package types and package information.

Package Type



Functional Block Diagram



NOTE: Pin numbers correspond to 8-pin package.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage 6.2V
Input Voltage, Any Terminal
..... V_S + 0.3V to GND – 0.3V
Package Power Dissipation ($T_A \leq 70°C$)
PDIP ..... 730 mW
CERDIP ..... 800 mW
SOIC ..... 760 mW
Derating Factor PDIP .....5.6 mW/°C Above 36°C
CERDIP ..... 6.0 mW/°C
Operating Temperature Range (Ambient)
C Version ..... 0°C to +70°C
E Version ..... -40°C to +85°C
M Version ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC4626/TC4627 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: T_A = +25°C, V_{DD} = 5V, $C_1 = C_2 = C_3$ 10µF unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-1	—	+1	µA	$0V \leq V_{IN} \leq V_{DRIVE}$
Output						
High Output Voltage	V_{OH}	V_{BOOST} – 0.025	—	—	V	
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance, High	R_O	—	10	15	Ω	I_{OUT} = 10 mA, V_{DD} = 5V
Output Resistance, Low	R_O	—	8	10	Ω	I_{OUT} = 10 mA, V_{DD} = 5V
Peak Output Current	I_{PK}	—	1.5	—	A	
Switching Time						
Rise Time	t_R	—	33	40	ns	Figure 3-1, Figure 3-2
Fall Time	t_F	—	27	35	ns	Figure 3-1, Figure 3-2
Delay Time	t_{D1}	—	35	45	ns	Figure 3-1, Figure 3-2
Delay Time	t_{D2}	—	45	55	ns	Figure 3-1, Figure 3-2
Maximum Switching Frequency	F_{MAX}	1.0	—	—	MHz	V_{DD} = 5V, V_{BOOST} > 8.5V, Figure 3-1
Voltage Booster						
Voltage Tripler Output Source Resistance	R_3	—	300	400	Ω	I_L = 10mA, V_{DD} = 5V
Voltage Doubler Output Source Resistance	R_2	—	120	200	Ω	
Oscillator Frequency	F_{OSC}	12	—	28	kHz	
Oscillator Amplitude Measured at C1-	V_{OSC}	4.5	—	10	V	R_{LOAD} = 10 kΩ
Undervoltage Threshold	UV @V_{BOOST}	7.0	7.8	8.5	V	
Start-Up Voltage	V_{START} @V_{BOOST}	10.5	11.3	12	V	

TC4626/TC4627 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: T_A = +25°C, V_{DD} = 5V, C_1 = C_2 = C_3 10µF unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
@V_{DD} = 5V	V_{BOOST}	14.6	—	—	V	No Load
Power Supply						
Power Supply Current	I_{DD}	—	—	2.5	mA	V_{IN} = Low or High
Supply Voltage	V_{DD}	4.0	—	6.0	V	
Input						
Logic 1, High Input Voltage	V_{IH}	2.4	—	—	V	
Logic 0, Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-10	—	1	µA	$0V \le V_{IN} \le V_{BOOST}$
Output						
High Output Voltage	V_{OH}	V_{DRIVE} – 0.025	—	—	V	
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance, High	R_O	—	 15 15	 20 25	Ω	I_{OUT} = 10 mA, V_{DD} = 5V C & E Version (T_A = +70°C or +85°C) M Version (T_A = +125°C)
Output Resistance, Low	R_O	—	 10 10	 13 15	Ω	I_{OUT} = 10 mA, V_{DD} = 5V C & E Version (T_A = +70°C or +85°C) M Version (T_A = +125°C)
Peak Output Current	I_{PK}	—	1.5	—	A	
Switching Time						
Rise Time	t_R	—	—	55	ns	Figure 3-1, Figure 3-2
Fall Time	t_F	—	—	50	ns	Figure 3-1, Figure 3-2
Delay Time	t_{D1}	—	—	60	ns	Figure 3-1, Figure 3-2
Delay Time	t_{D2}	—	—	70	ns	Figure 3-1, Figure 3-2
Maximum Switching Frequency	F_{MAX}	750	—	—	kHz	V_{DD} = 5V, V_{BOOST} > 8.5V, Figure 3-1
Voltage Booster						
Voltage Boost Output Source Resistance	R_3	—	400	500	Ω	I_L = 10 mA, V_{DD} = 5V
Voltage Doubler Output Source Resistance	R_2	—	170	300	Ω	
Oscillator Frequency	F_{OSC}	5	—	50	kHz	
Oscillator Amplitude Measured at C1-	V_{OSC}	4.5	—	10	V	R_{LOAD} = 10 kΩ
Undervoltage Threshold	UV @V_{BOOST}	7.0	7.8	8.5	V	
Start-Up Voltage	V_{START} @V_{BOOST}	10.5	11.3	12	V	
@V_{DD} = 5V	V_{BOOST}	14.6	—	—	V	No Load
Power Supply						
Power Supply Current	I_{DD}	—	—	4	mA	V_{IN} = Low or High
Supply Voltage	V_{DD}	4.0	—	6.0	V	

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, CERDIP)	Pin No. (16-Pin SOIC Wide)	Symbol	Description
1	1	C1-	See **Section 3.1 "Booster Function"** for description
2	3	C1+	See **Section 3.1 "Booster Function"** for description
3	5	C2	See **Section 3.1 "Booster Function"** for description
4	8	GND	Ground.
5	9	OUT	Output
6	11	V_{BOOST}	See **Section 3.1 "Booster Function"** for description
7	13	IN	Control Input
8	16	V_{DD}	Supply Input
—	2, 4, 6, 7, 10, 12, 14, 15	NC	Not connected.

3.0 APPLICATIONS INFORMATION

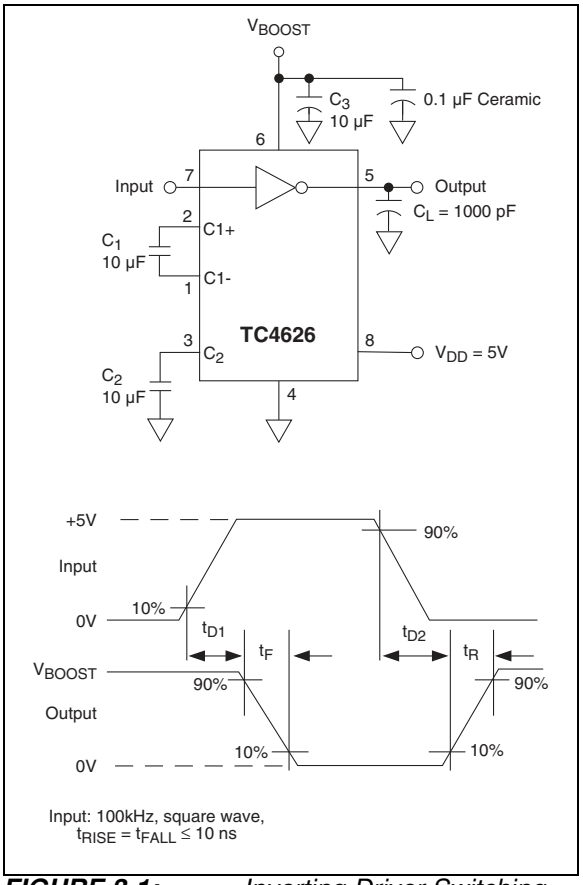


FIGURE 3-1: *Inverting Driver Switching Time.*

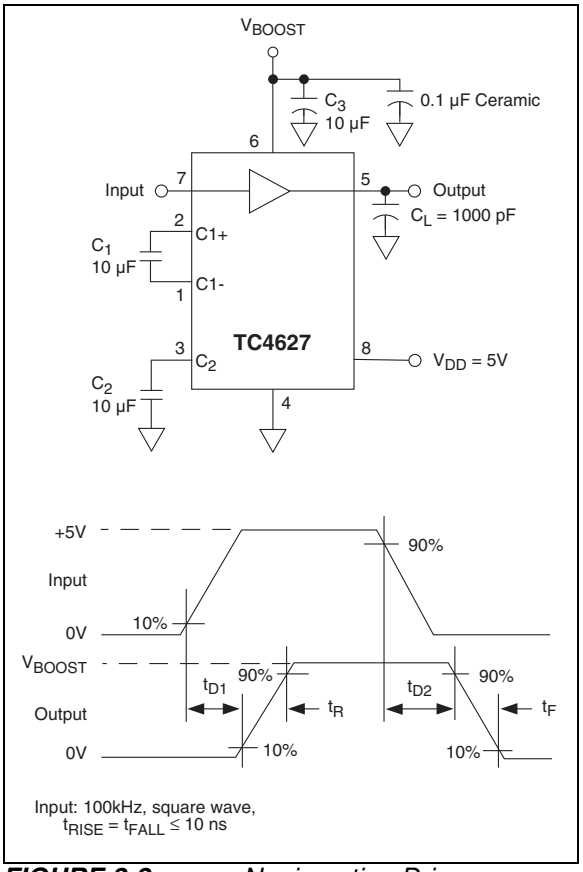


FIGURE 3-2: *Noninverting Driver Switching Time.*

3.1 BOOSTER FUNCTION

The voltage booster is an unregulated voltage tripler circuit. The tripler consists of three sets of internal switches and three external capacitors. S1a and S1b charge capacitor C1 to V_{DD} potential. S2a and S2b add C1 potential to V_{DD} input to charge C2 to 2 x V_{DD}. S3a and S3b add C1 potential to C2 to charge C3 to 3 x V_{DD}. The position of the switches is controlled by the internal four-phase clock.

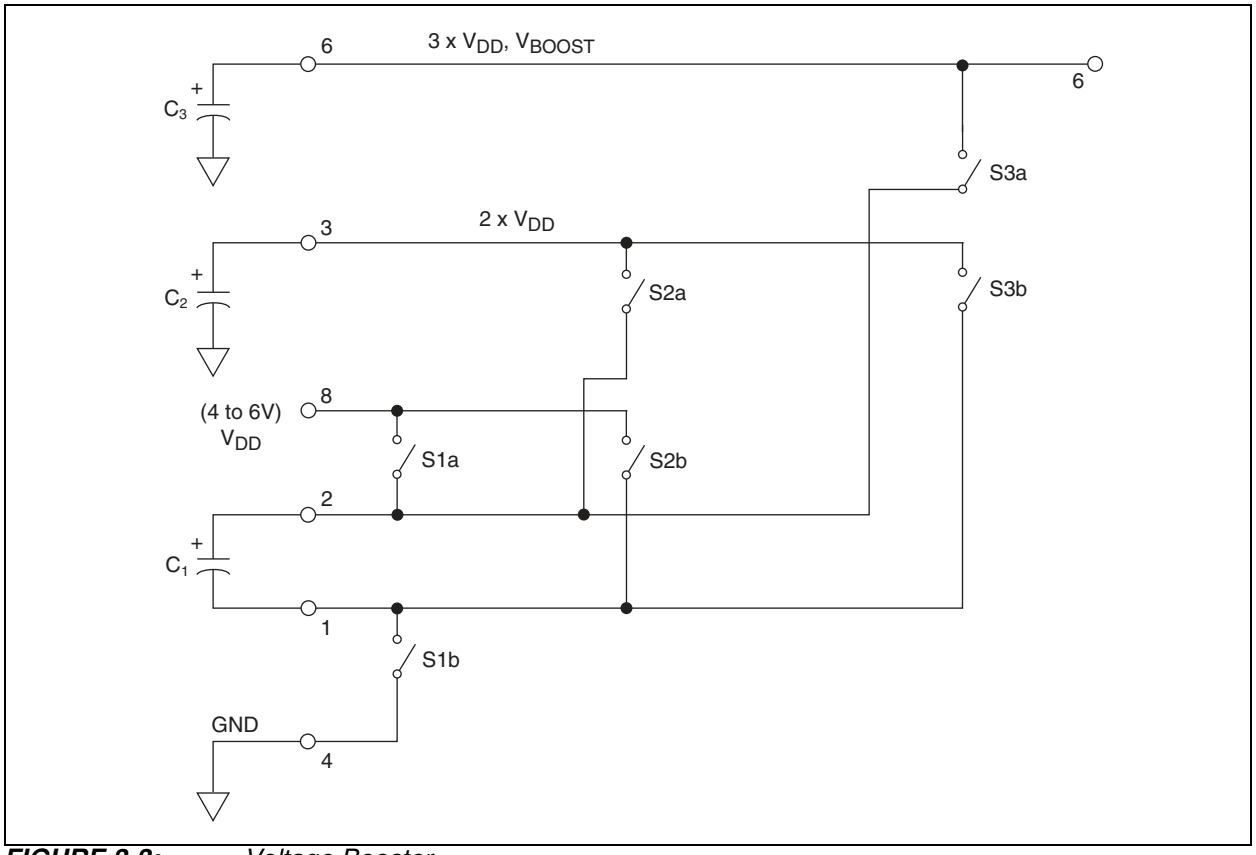


FIGURE 3-3: *Voltage Booster.*

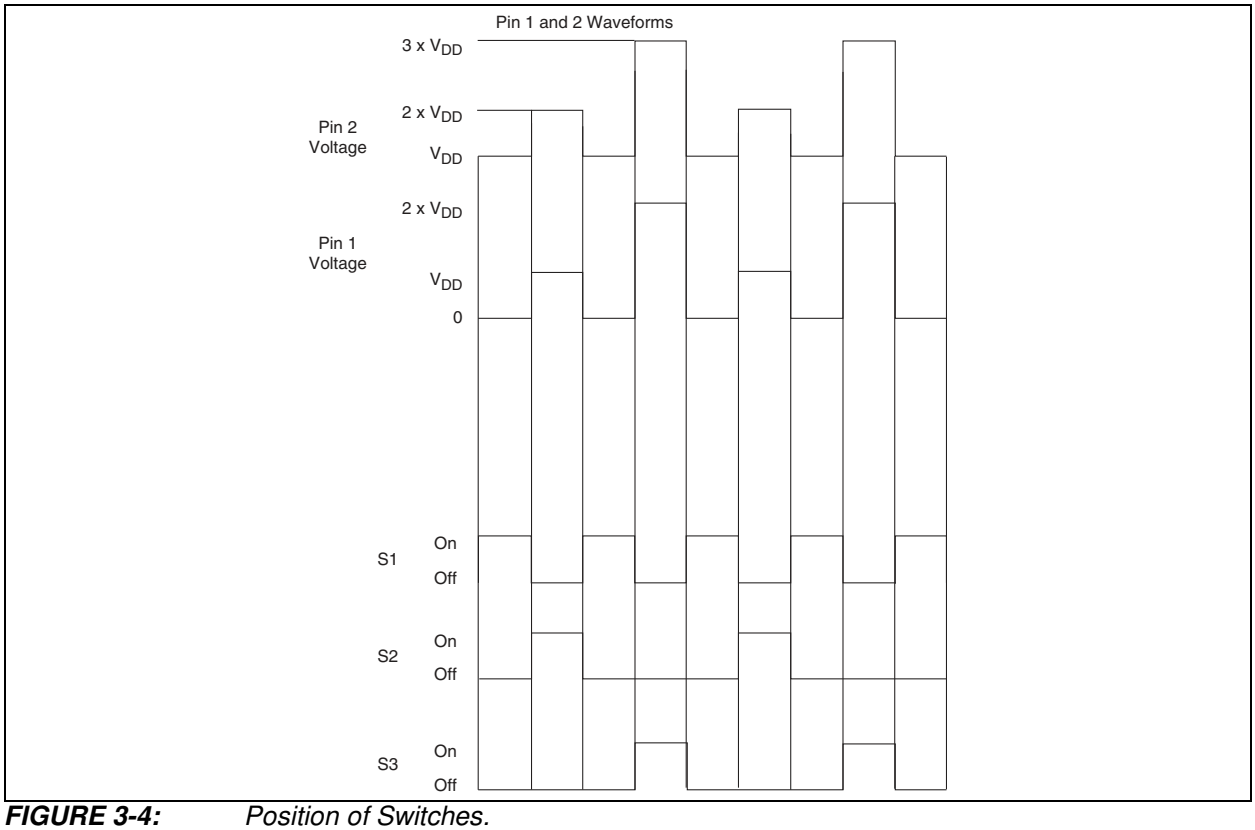
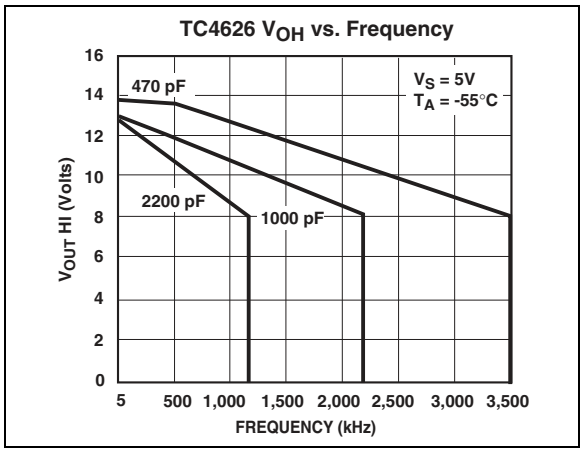
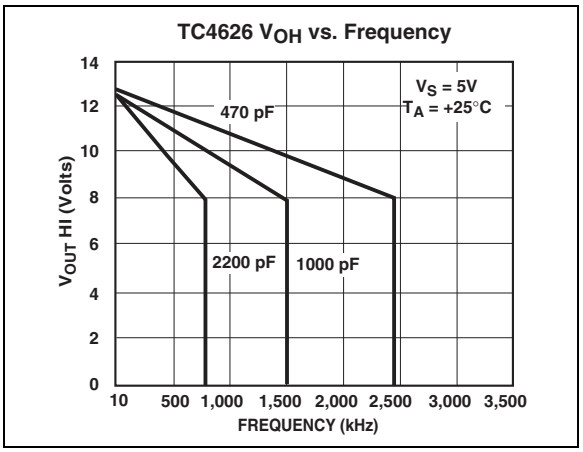


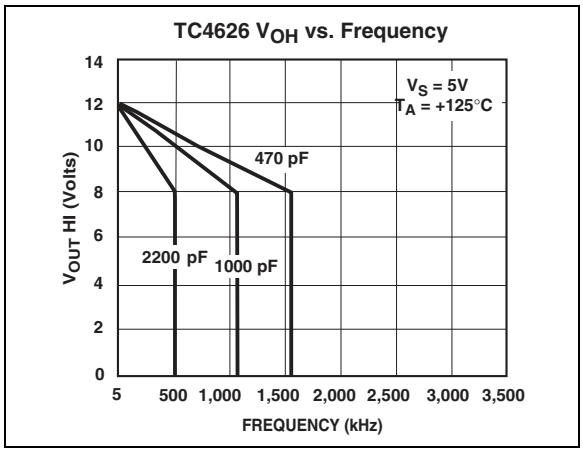
FIGURE 3-4: *Position of Switches.*

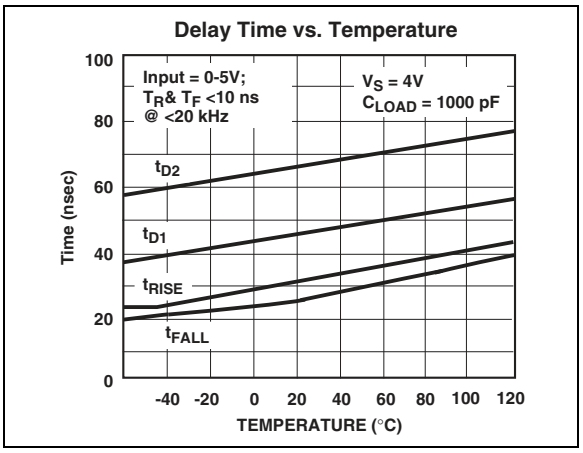
4.0 TYPICAL CHARACTERISTICS

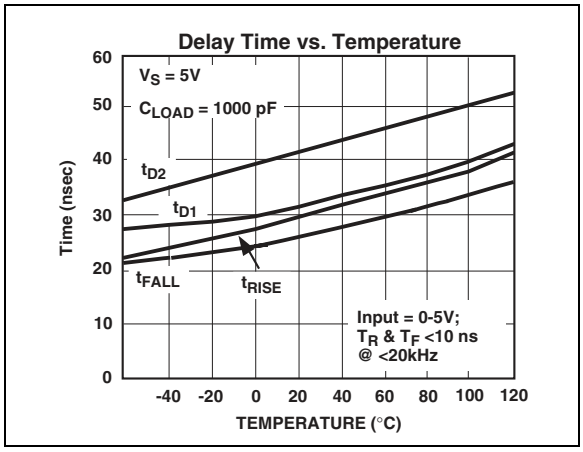
Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

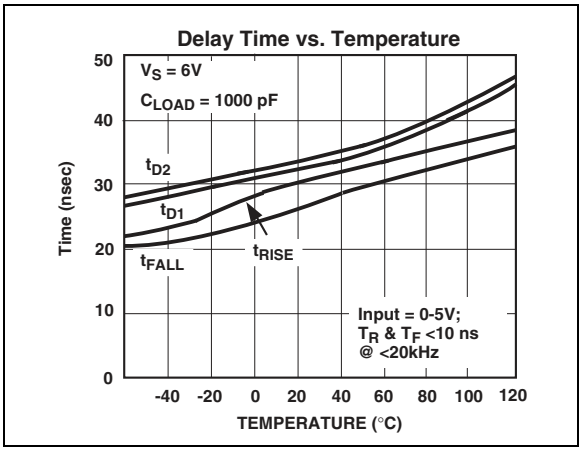


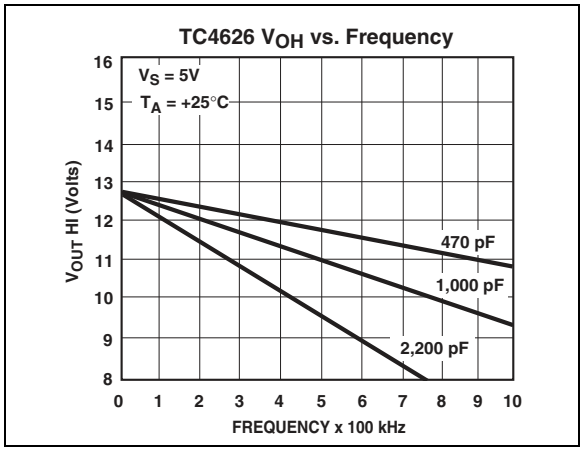


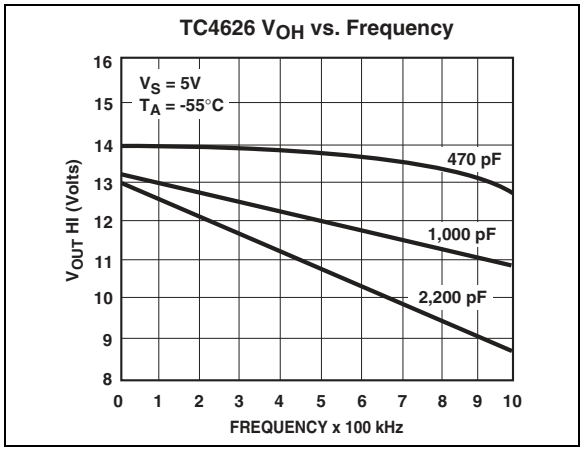


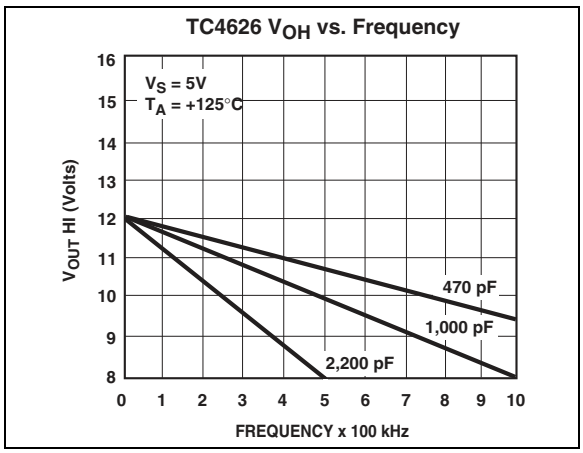







TC4626 V_{OH} vs. Frequency
V_S = 5V
T_A = +25°C
470 pF
1,000 pF
2,200 pF
V_{OUT} HI (Volts)
FREQUENCY x 100 kHz

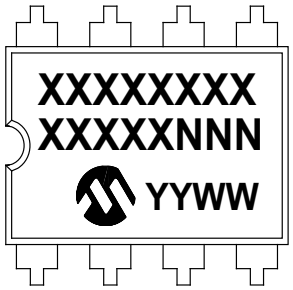

TC4626 V_{OH} vs. Frequency
V_S = 5V
T_A = -55°C
470 pF
1,000 pF
2,200 pF
V_{OUT} HI (Volts)
FREQUENCY x 100 kHz


TC4626 V_{OH} vs. Frequency
V_S = 5V
T_A = +125°C
470 pF
1,000 pF
2,200 pF
V_{OUT} HI (Volts)
FREQUENCY x 100 kHz

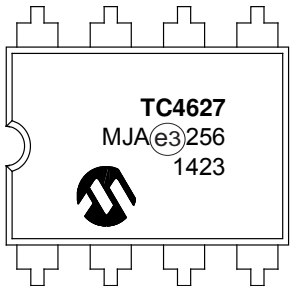
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

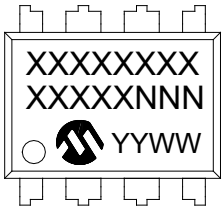
8-Lead CERDIP (.300") **(TC4627 Only)**



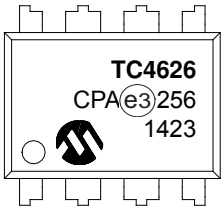
Example



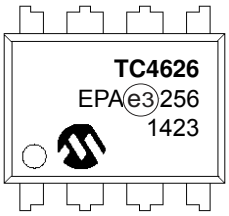
8-Lead PDIP (300 mil)



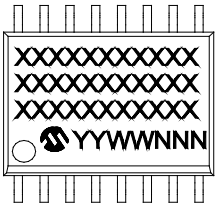
Example



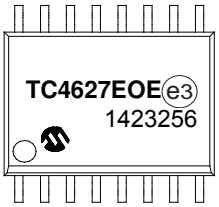
OR



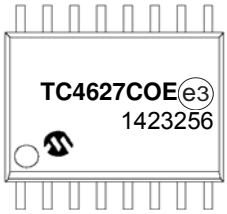
16-Lead SOIC (7.50 mm)



Example



OR

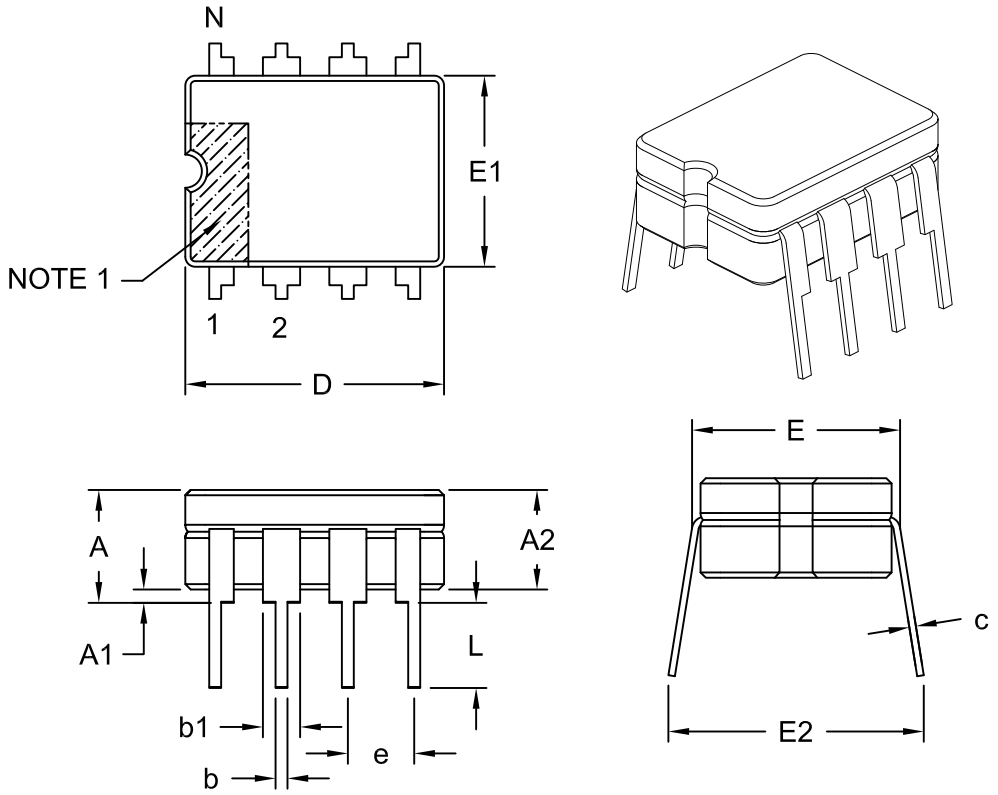


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Ceramic Dual In-Line (JA) ~ .300" Body [CERDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.200
Base to Seating Plane §	A1	.015	-	-
Ceramic Package Height	A2	.140	-	.175
Shoulder to Shoulder Width	E	.290	-	.320
Ceramic Pkg. Width	E1	.230	.248	.300
Overall Length	D	.370	.380	.400
Tip to Seating Plane	L	.125	-	.200
Lead Thickness	c	.008	-	.015
Upper Lead Width	b1	.045	-	.065
Lower Lead Width	b	.015	-	.023
Overall Row Spacing	E2	.314	-	.410

Notes:

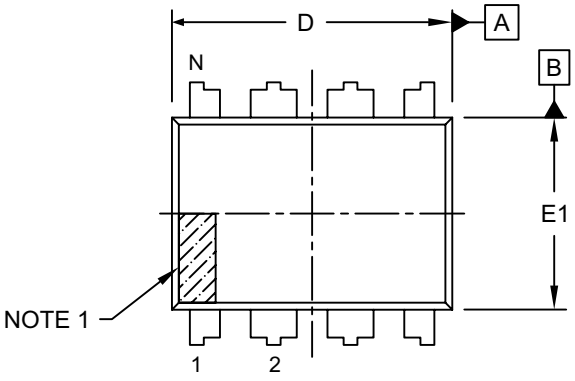
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

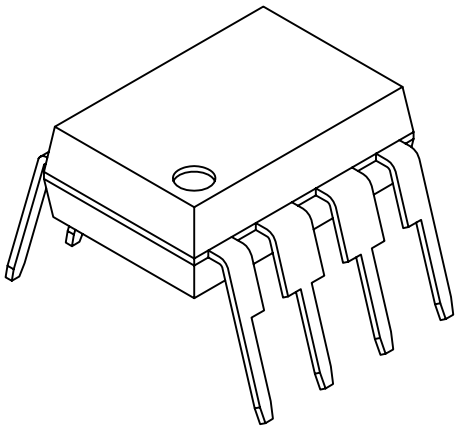
Microchip Technology Drawing No. C04-001C

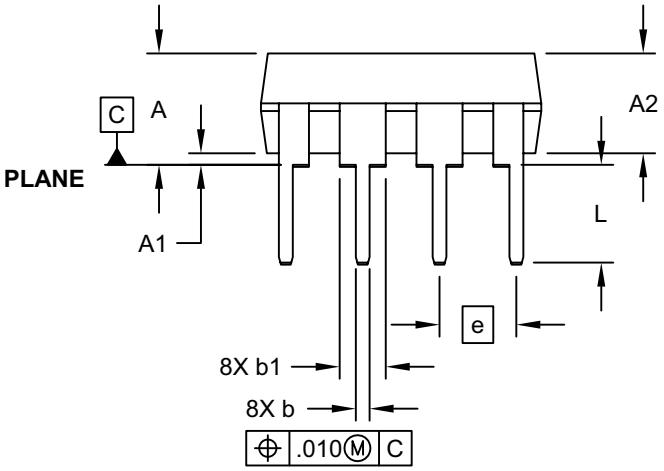
8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

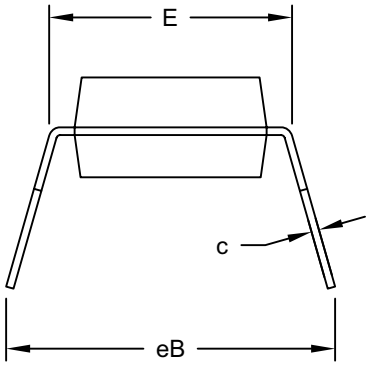


TOP VIEW





SIDE VIEW

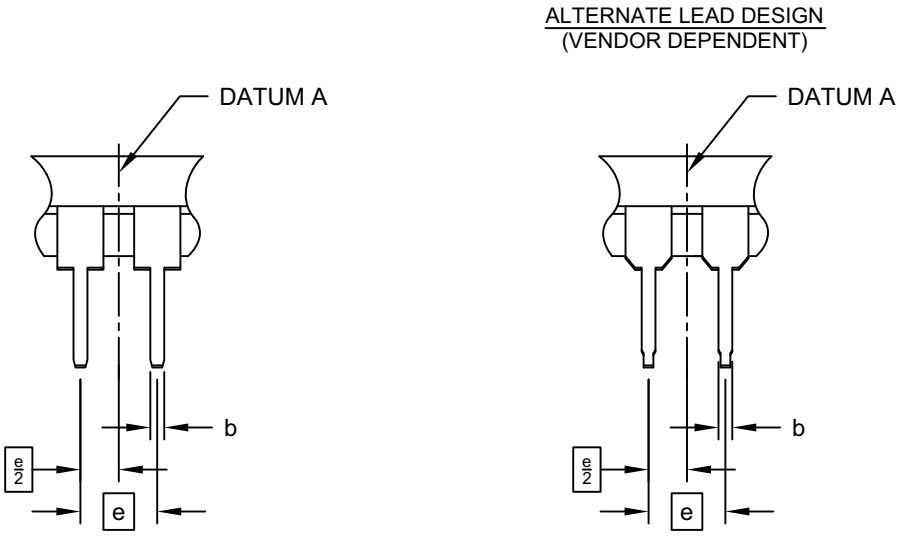


END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

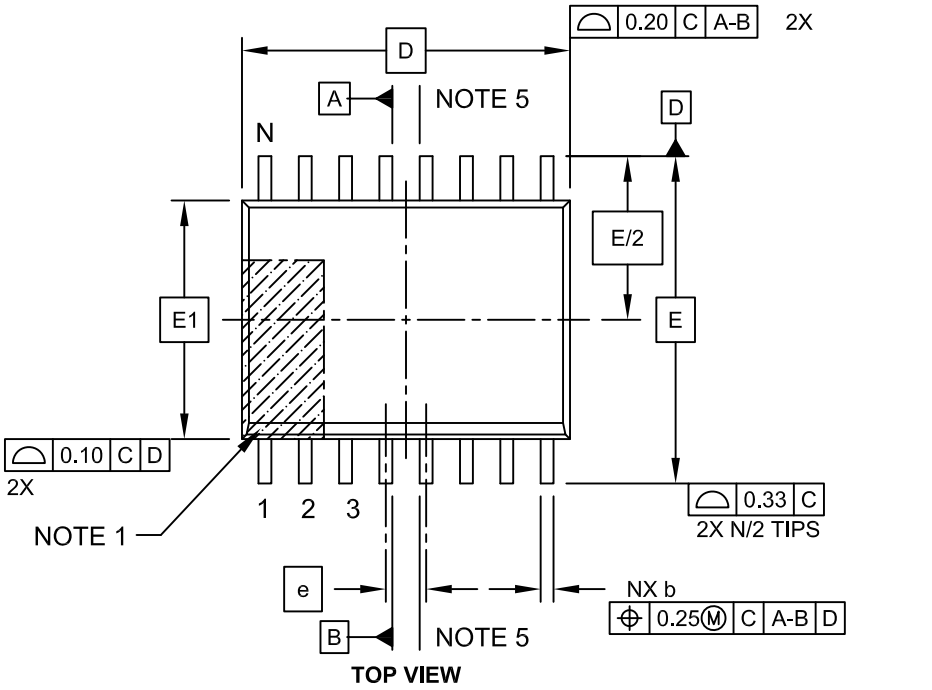
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

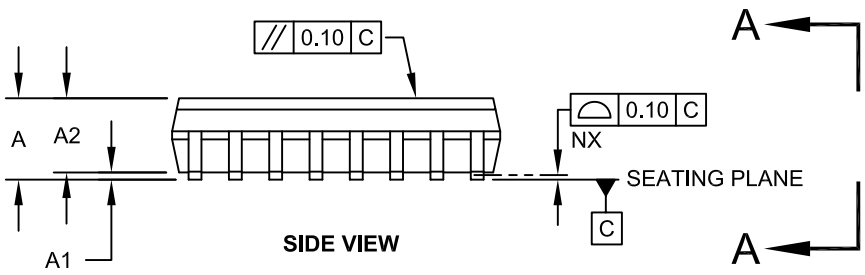
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

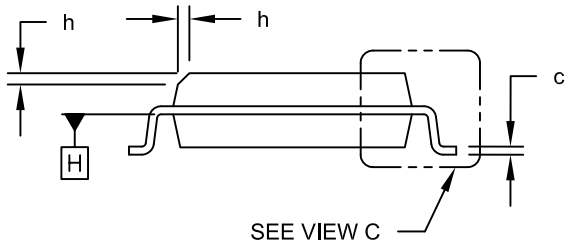
Microchip Technology Drawing No. C04-018D Sheet 2 of 2

16-Lead Plastic Small Outline (OE) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





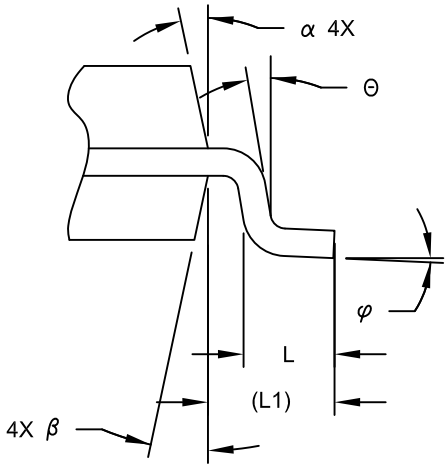


VIEW A-A

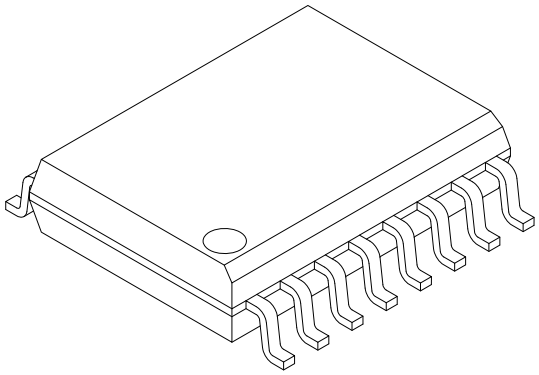
Microchip Technology Drawing C04-102C Sheet 1 of 2

16-Lead Plastic Small Outline (OE) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		10.30 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

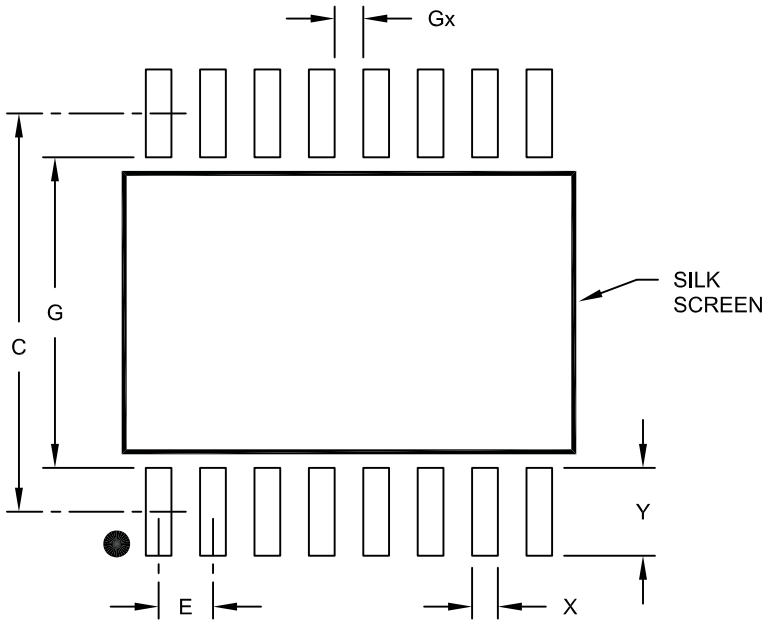
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-102C Sheet 2 of 2

16-Lead Plastic Small Outline (OE) – Wide, 7.50 mm Body [SOIC] Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.30	
Contact Pad Width	X			0.60
Contact Pad Length	Y			2.05
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2102A

APPENDIX A: REVISION HISTORY

Revision D (July 2014)

The following is the list of modifications:

- Restructured **Table 2-1** for readability purposes.
- Updated package specification drawings in **Section 5.0, Packaging Information** to match all views available.
- Added new **Product Identification System**.

Revision C (December 2012)

Added a note to each package outline drawing.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–	X	/XX
Device		Temperature Range	Package

Device: TC4626: Single CMOS High-Speed Driver, Inverting
TC4627: Single CMOS High-Speed Driver, Non-Inverting

Temperature Range: C = 0°C to +70°C
E = -40°C to +85°C

Package: JA = 8-Lead Ceramic Dual In-Line, 300" Body (CERDIP) (TC4627 only)
OE = 16-Lead Plastic Small Outline, Wide, 7.50 mm Body (SOIC)
PA = 8-Lead Plastic Dual In-Line, 300 mil Body (PDIP)

Examples:

a) TC4626CPA: High-Speed Inverting Single CMOS Driver, 0°C to +70°C.

b) TC4626EPA: High-Speed Inverting Single CMOS Driver, -40°C to +85°C.

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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