



STL75N3LLZH5

N-channel 30 V, 0.0055 Ω , 19 A PowerFLAT™ (5x6)
STripFET™ V Power MOSFET

Preliminary data

Features

Type	V _{DSS}	R _{DS(on) max}	I _D
STL75N3LLZH5	30 V	<0.0061 Ω	19 A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses
- Built in G-S Zener diodes

Application

- Switching applications

Description

The STL75N3LLZH5 is an N-channel STripFET™V Power MOSFET which has been designed to achieve very low on-state resistance providing also one of the best-in-class figure of merit (FOM).

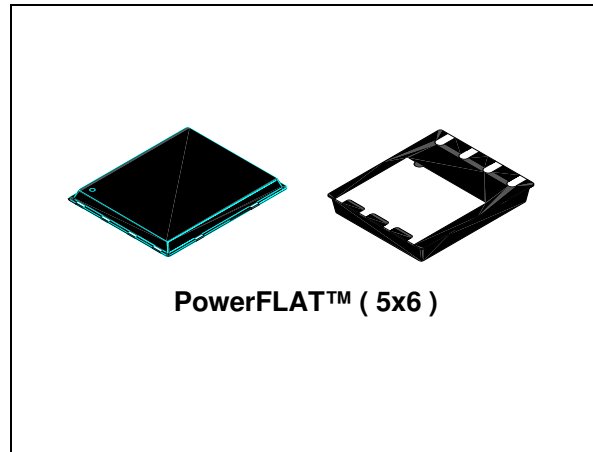


Figure 1. Internal schematic diagram

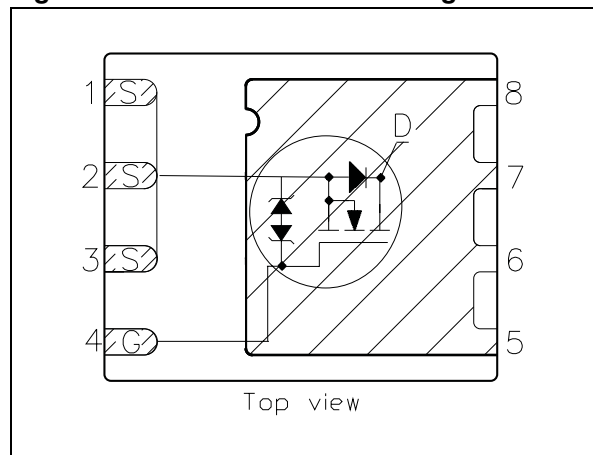


Table 1. Device summary

Order code	Marking	Package	Packaging
STL75N3LLZH5	75N3LLZH5	PowerFLAT™ (5x6)	Tape and reel

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	± 18	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	75	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	47	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	19	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	11.8	A
$I_{DM}^{(3)}$	Drain current (pulsed)	76	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25^\circ\text{C}$	4	W
	Derating factor	0.03	W/ $^\circ\text{C}$
T_J	Operating junction temperature	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature		

1. The value is rated according R_{thj-c} .
2. The value is rated according $R_{thj-pcb}$.
3. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (Drain) (steady state)	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10$ sec

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating @ } 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 18\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 9.5\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 9.5\text{ A}$		0.0055 0.0066	0.0061 0.0078	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1510	-	μF
C_{oss}	Output capacitance			287		
C_{rss}	Reverse transfer capacitance			40		
Q_g	Total gate charge	$V_{DD} = 15\text{ V}$, $I_D = 19\text{ A}$	-	11.8	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\text{ V}$		4		
Q_{gd}	Gate-drain charge	Figure 3		6		

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 9.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ Figure 2	-	9.2	-	ns
t_r	Rise time			11		
$t_{d(off)}$	Turn-off delay time			55		
t_f	Fall time			20		

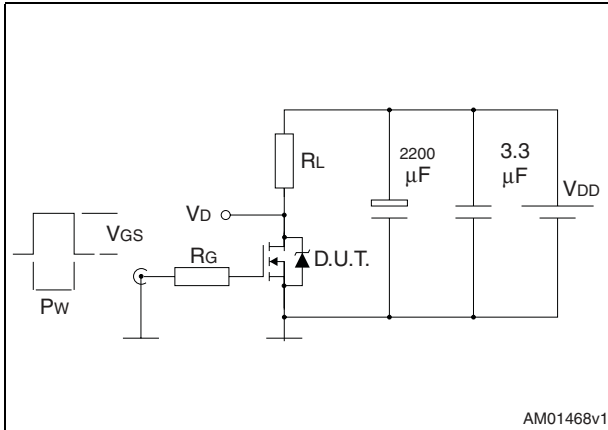
Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		19	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		76	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 19 \text{ A}, V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 19 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 25 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$	-	24		ns
Q_{rr}	Reverse recovery charge			17		nC
I_{RRM}	Reverse recovery current			1.4		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration= 300 μs , duty cycle 1.5%.

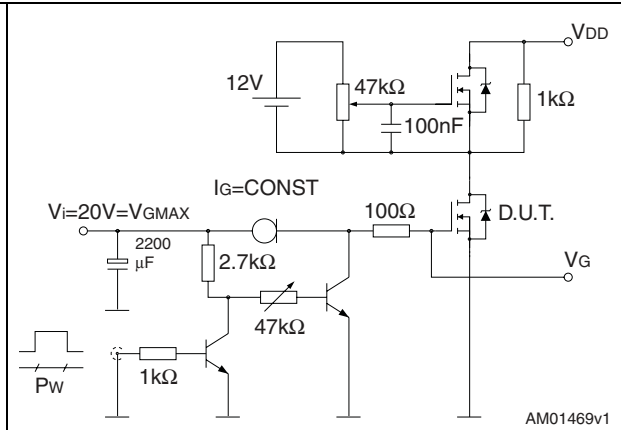
3 Test circuits

Figure 2. Switching times test circuit for resistive load



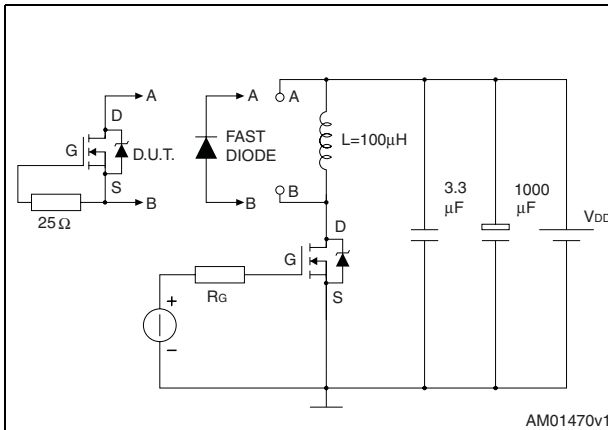
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Figure 3. Gate charge test circuit



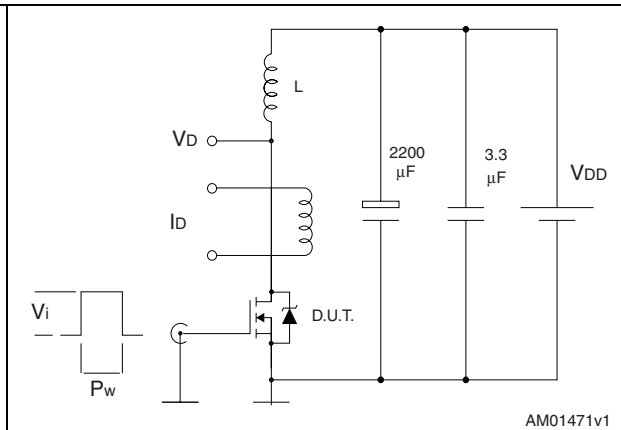
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Figure 4. Test circuit for inductive load switching and diode recovery times



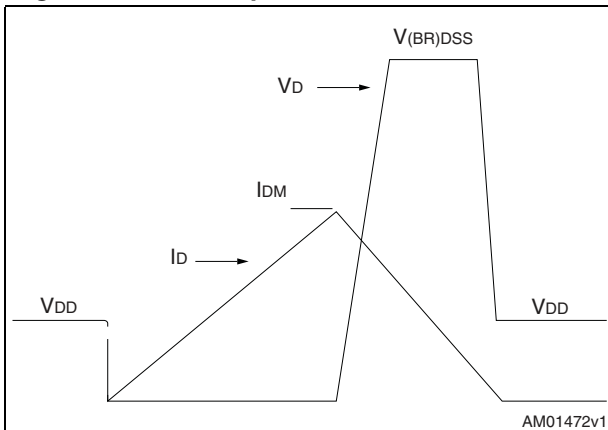
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Figure 5. Unclamped inductive load test circuit



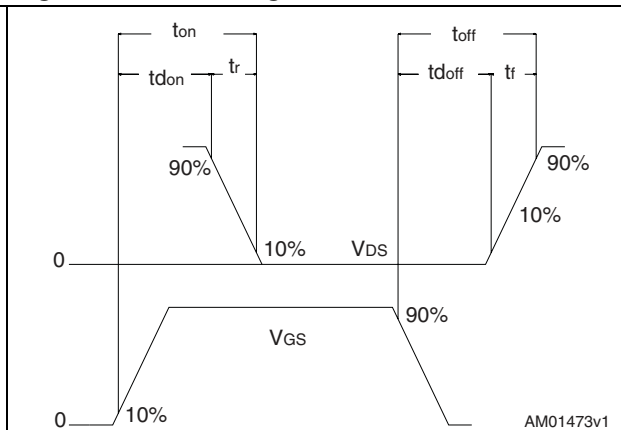
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Figure 6. Unclamped inductive waveform



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Figure 7. Switching time waveform



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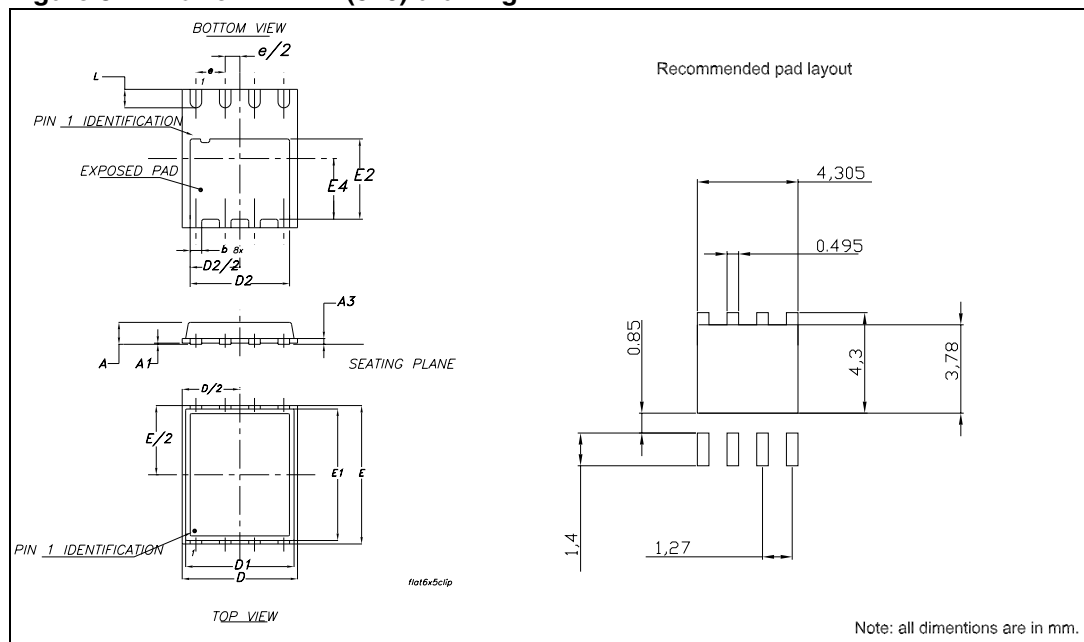
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. Power FLAT™ (5x6) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.83	0.93	0.031	0.32	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035

Figure 8. Power FLAT™ (5x6) drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
22-Jun-2010	1	First release.
08-Jul-2010	2	Modified V_{GS} in Table 2: Absolute maximum ratings and Table 4: On/off states .

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