

## Features

- Very high speed: 45 ns
- Temperature ranges:
  - Industrial: -40 °C to +85 °C
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62128DV30
- Ultra low standby power
  - Typical standby current: 1 μA
  - Maximum standby current: 4 μA
- Ultra low active power
  - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 32-pin small outline integrated circuit (SOIC), 32-pin thin small outline package (TSOP) Type I, and 32-pin shrunk thin small outline package (STSOP) packages

## Functional Description

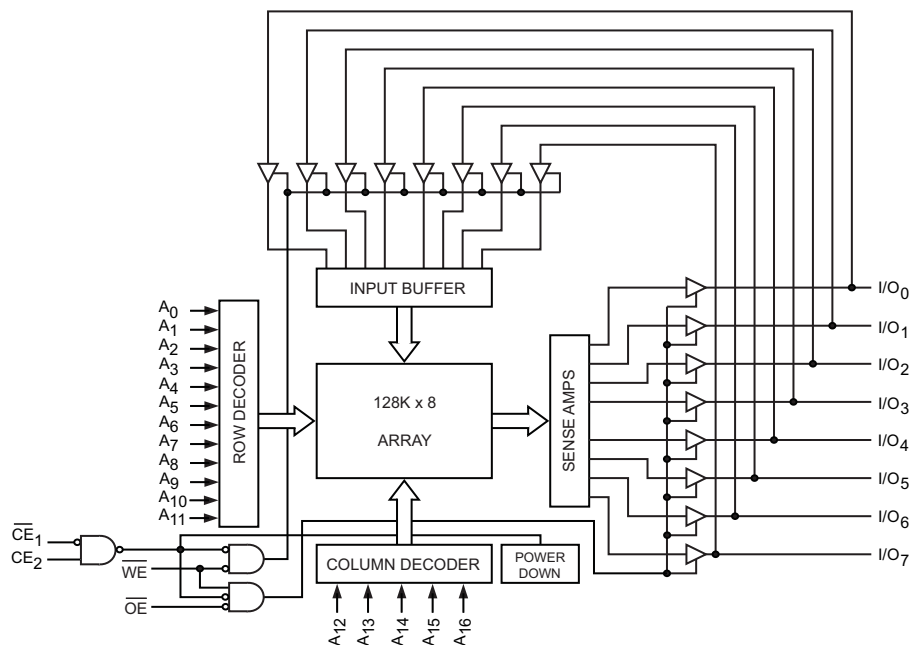
The CY62128EV30 is a high performance CMOS static RAM module organized as 128K words by 8-bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW). The eight input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress ( $CE_1$  LOW and  $CE_2$  HIGH and  $WE$  LOW).

To write to the device, take chip enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and write enable ( $WE$ ) inputs LOW. Data on the eight I/O pins is then written into the location specified on the address pin ( $A_0$  through  $A_{16}$ ).

To read from the device, take chip enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and output enable ( $\overline{OE}$ ) LOW while forcing write enable ( $WE$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related resources, [click here](#).

## Logic Block Diagram



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## Pin Configuration

Figure 1. 32-pin STSOP pinout [1]

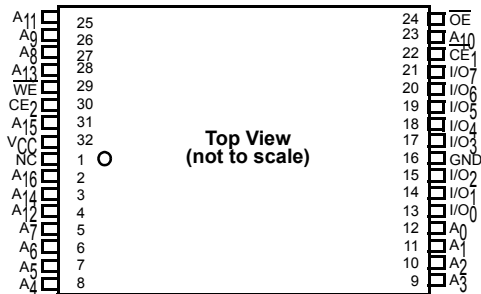


Figure 2. 32-pin TSOP I pinout [1]

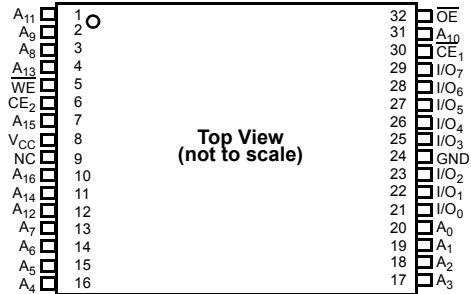
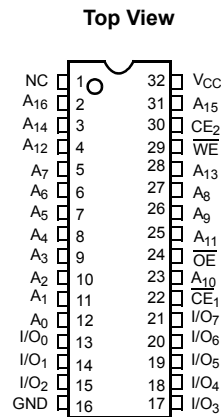


Figure 3. 32-pin SOIC pinout [1]



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (µA)	
						f = 1 MHz		f = f <sub>max</sub>			
Min	Typ [2]	Max	Typ [2]	Max	Typ [2]	Max	Typ [2]	Max			
CY62128EV30LL	Industrial	2.2	3.0	3.6	45	1.3	2.0	11	16	1	4

### Notes

- NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	..... -65 °C to +150 °C
Ambient temperature with power applied	..... -55 °C to +125 °C
Supply voltage to ground potential [3, 4]	..... -0.3 V to $V_{CC(max)}$ + 0.3 V
DC voltage applied to outputs in high Z State [3, 4]	..... -0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [3, 4]	..... -0.3 V to $V_{CC(max)}$ + 0.3 V
Output current into outputs (LOW)	..... 20 mA
Static discharge voltage (MIL-STD-883, method 3015)	..... > 2001 V
Latch-up current	..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ [5]
CY62128EV30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Industrial)			Unit
			Min	Typ [6]	Max	
$V_{OH}$	Output HIGH voltage	$I_{OH} = -0.1$ mA	2.0	–	–	V
		$I_{OH} = -1.0$ mA, $V_{CC} \geq 2.70$ V	2.4	–	–	V
$V_{OL}$	Output LOW voltage	$I_{OL} = 0.1$ mA	–	–	0.4	V
		$I_{OL} = 2.1$ mA, $V_{CC} \geq 2.70$ V	–	–	0.4	V
$V_{IH}$	Input HIGH voltage	$V_{CC} = 2.2$ V to 2.7 V	1.8	–	$V_{CC} + 0.3$ V	V
		$V_{CC} = 2.7$ V to 3.6 V	2.2	–	$V_{CC} + 0.3$ V	V
$V_{IL}$	Input LOW voltage	$V_{CC} = 2.2$ V to 2.7 V	-0.3	–	0.6	V
		$V_{CC} = 2.7$ V to 3.6 V	-0.3	–	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	–	+1	µA
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , output disabled	-1	–	+1	µA
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{max} = 1/t_{RC}$	–	11	16	mA
		$f = 1$ MHz	–	1.3	2.0	mA
$I_{SB1}$ [7]	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 < 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} < 0.2$ V $f = f_{max}$ (address and data only), $f = 0$ ( $\overline{OE}$ and $\overline{WE}$ ), $V_{CC} = 3.60$ V	–	1	4	µA
$I_{SB2}$ [7]	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 < 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} < 0.2$ V, $f = 0$ , $V_{CC} = 3.60$ V	–	1	4	µA

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 µs ramp time from 0 to  $V_{CC(min)}$  and 200 µs wait time after  $V_{CC}$  stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.
- Chip enables ( $CE_1$  and  $CE_2$ ) must be at CMOS level to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.

### Capacitance

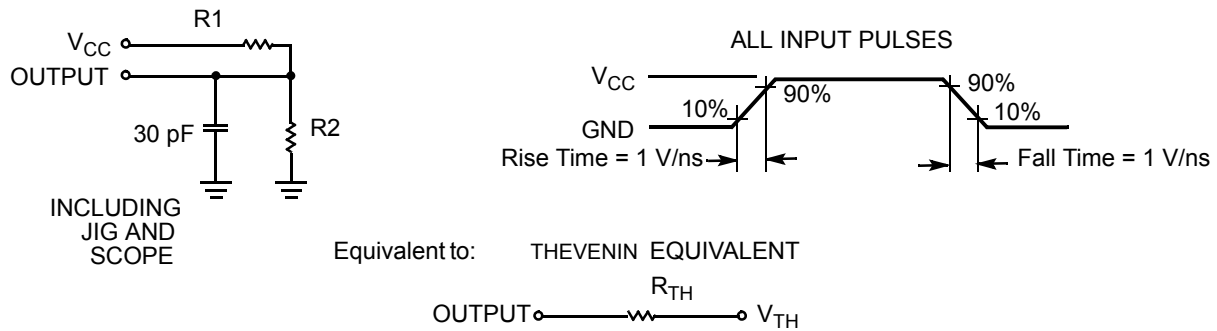
Parameter <sup>[8]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

### Thermal Resistance

Parameter <sup>[8]</sup>	Description	Test Conditions	32-pin TSOP I	32-pin SOIC	32-pin STSOP	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	56.90	79.34	69.47	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		14.81	18.49	13.39	°C/W

### AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

**Note**

8. Tested initially and after any design or process changes that may affect these parameters.

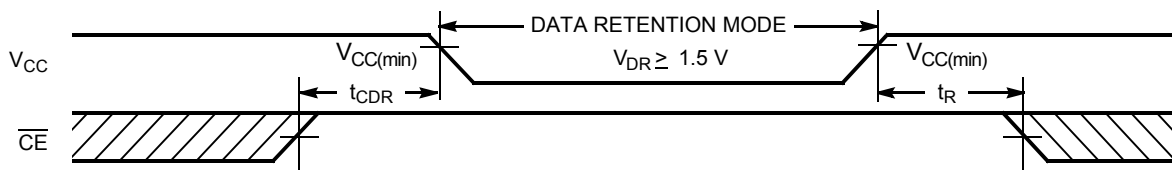
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[9]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.5	–	–	V
$I_{CCDR}$ <sup>[10]</sup>	Data retention current	$V_{CC} = 1.5\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	3	$\mu\text{A}$
$t_{CDR}$ <sup>[11]</sup>	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[12]</sup>	Operation recovery time		45	–	–	ns

## Data Retention Waveform

Figure 5. Data Retention Waveform<sup>[13]</sup>



### Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
10. Chip enables ( $CE_1$  and  $CE_2$ ) must be at CMOS level to meet the  $I_{SB1} / I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
13.  $\overline{CE}$  is the logical combination of  $CE_1$  and  $CE_2$ . When  $CE_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $CE_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

## Switching Characteristics

Over the Operating Range

Parameter <sup>[14, 15]</sup>	Description	45 ns (Industrial)		Unit
		Min	Max	
<b>Read Cycle</b>				
t <sub>RC</sub>	Read cycle time	45	–	ns
t <sub>AA</sub>	Address to data valid	–	45	ns
t <sub>OHA</sub>	Data hold from address change	10	–	ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to data valid	–	45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	22	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to low Z <sup>[16]</sup>	5	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to high Z <sup>[16, 17]</sup>	–	18	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to low Z <sup>[16]</sup>	10	–	ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to high Z <sup>[16, 17]</sup>	–	18	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to power-up	0	–	ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to power-down	–	45	ns
<b>Write Cycle <sup>[18, 19]</sup></b>				
t <sub>WC</sub>	Write cycle time	45	–	ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to write end	35	–	ns
t <sub>AW</sub>	Address setup to write end	35	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	35	–	ns
t <sub>SD</sub>	Data setup to write end	25	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to high Z <sup>[16, 17]</sup>	–	18	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to low Z <sup>[16]</sup>	10	–	ns

### Notes

14.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
15. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 4 on page 5](#).
16. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
17.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the output enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. The minimum write pulse width for WRITE Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

Figure 6. Read Cycle 1 (Address Transition Controlled) [21, 22]

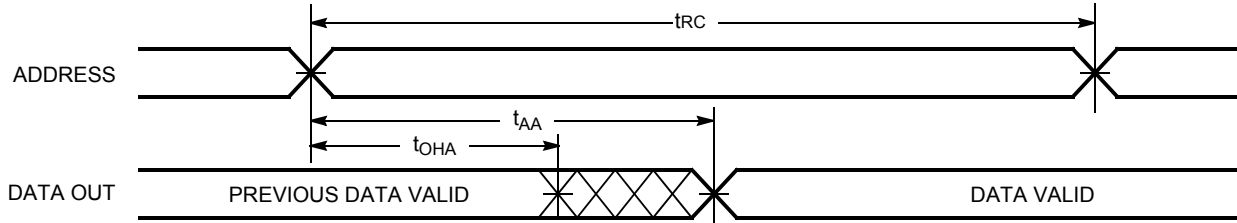
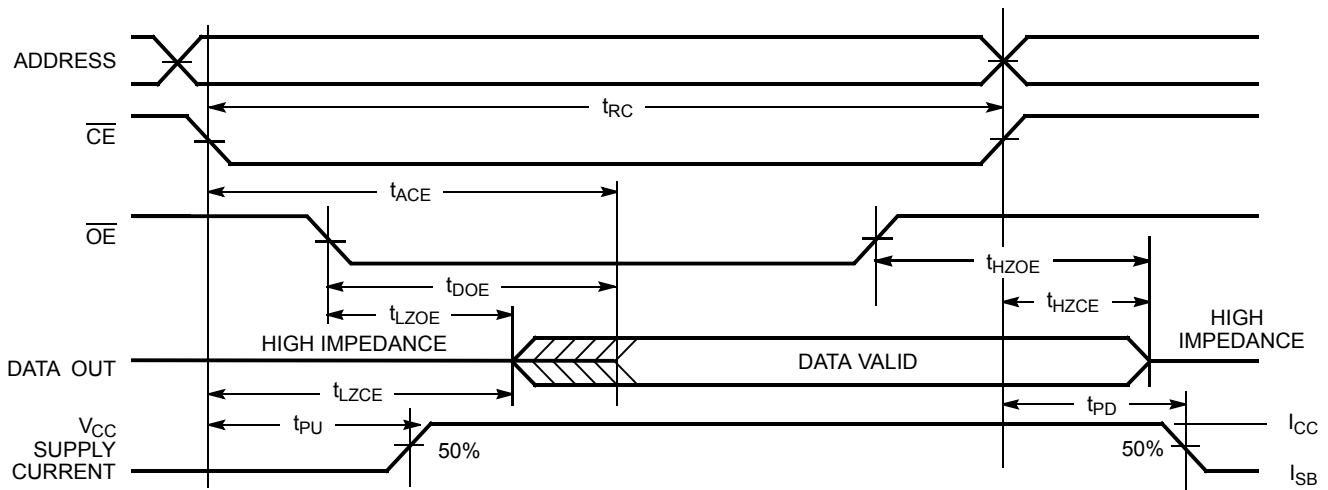


Figure 7. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [22, 23, 24]



### Notes

20. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

21. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{CE}_2 = V_{IH}$ .

22.  $\overline{WE}$  is HIGH for read cycle.

23.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$ . When  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW,  $\overline{CE}$  is HIGH.

24. Address valid before or similar to  $\overline{CE}_1$  transition LOW and  $\overline{CE}_2$  transition HIGH.



Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ( $\overline{WE}$  Controlled) [25, 26, 27, 28]

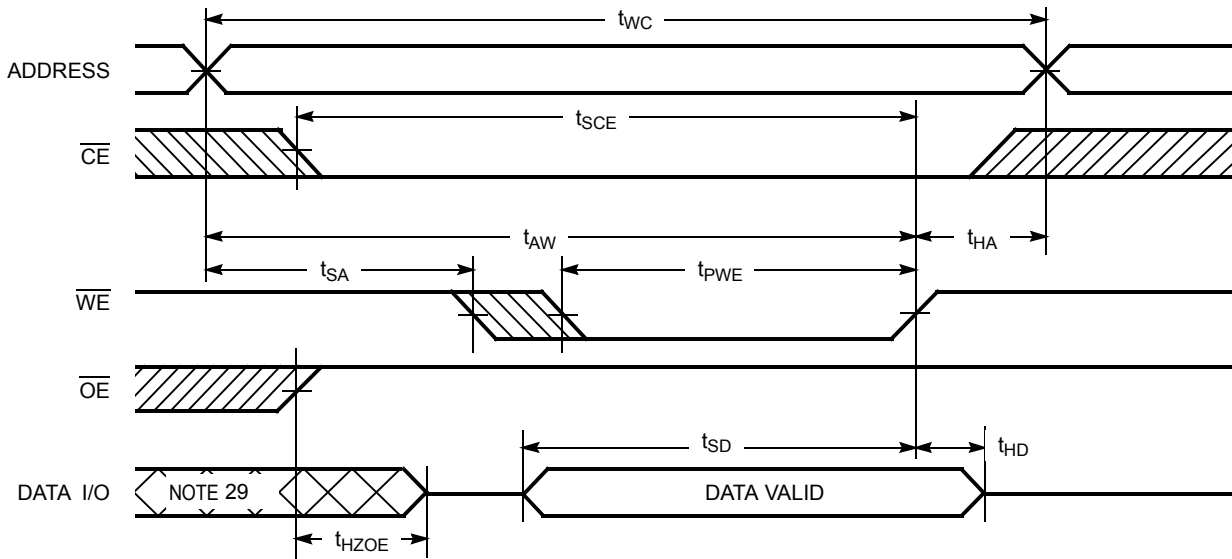
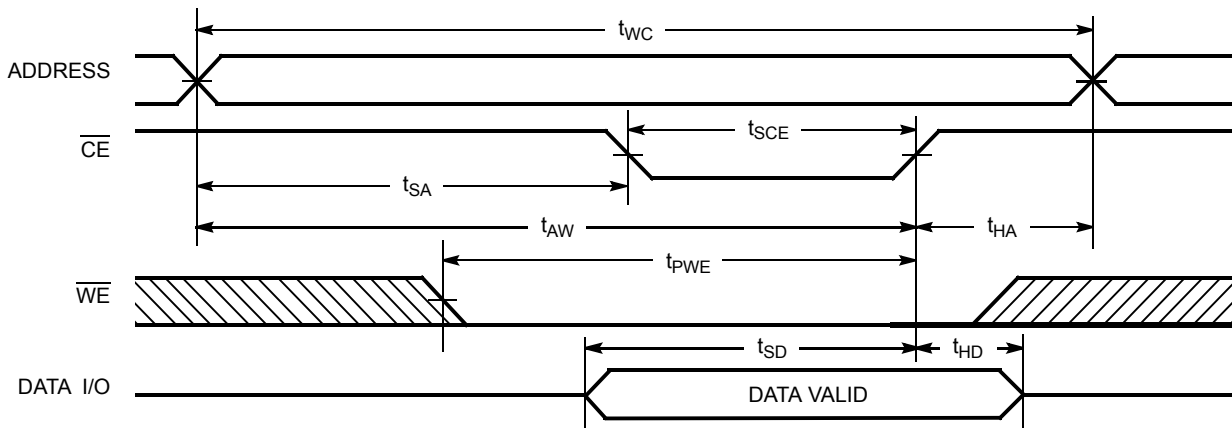


Figure 9. Write Cycle No. 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled) [25, 26, 27, 28]

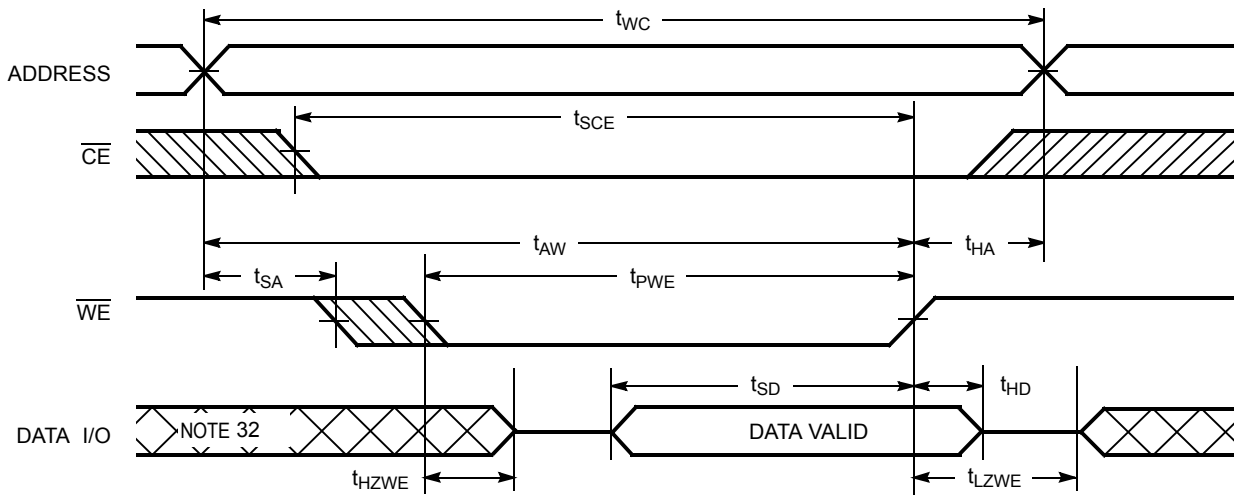


Notes

- 25. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 26.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 27. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 28. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 29. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [30, 31, 33]



Notes

30.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
31. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
32. During this period, the I/Os are in output state. Do not apply input signals.
33. The minimum write pulse width for WRITE Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X <sup>[34]</sup>	X	X	High Z	Deselect/power-down	Standby ( $I_{SB}$ )
X <sup>[34]</sup>	L	X	X	High Z	Deselect/power-down	Standby ( $I_{SB}$ )
L	H	H	L	Data out	Read	Active ( $I_{CC}$ )
L	H	L	X	Data in	Write	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, outputs disabled	Active ( $I_{CC}$ )

**Note**

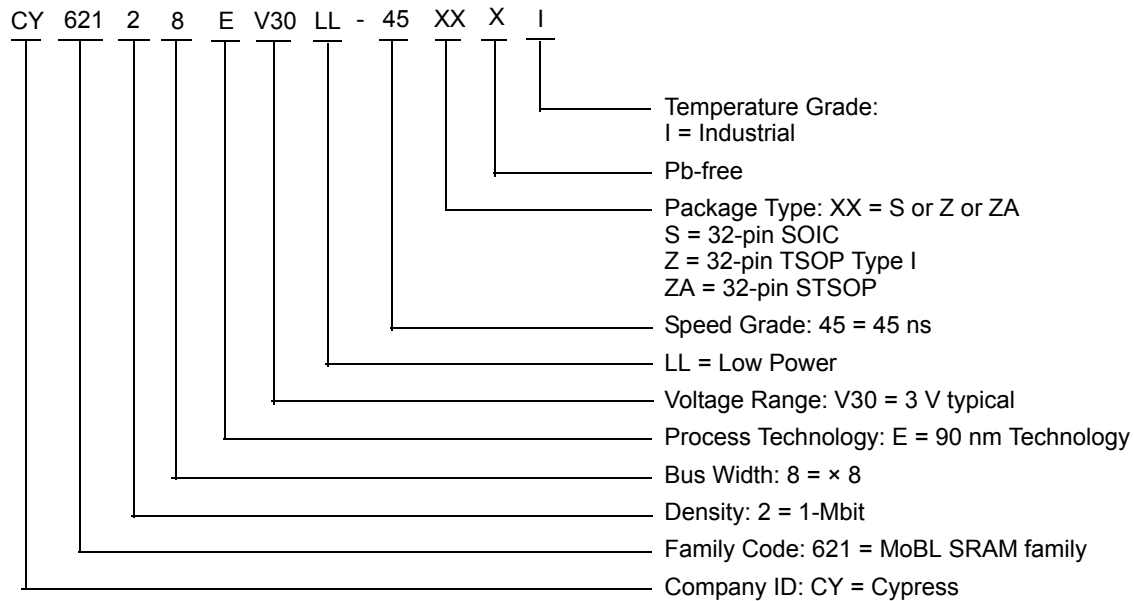
34. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62128EV30LL-45SXI	51-85081	32-pin 450-Mil SOIC (Pb-free)	Industrial
	CY62128EV30LL-45ZXI	51-85056	32-pin TSOP Type I (Pb-free)	
	CY62128EV30LL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	

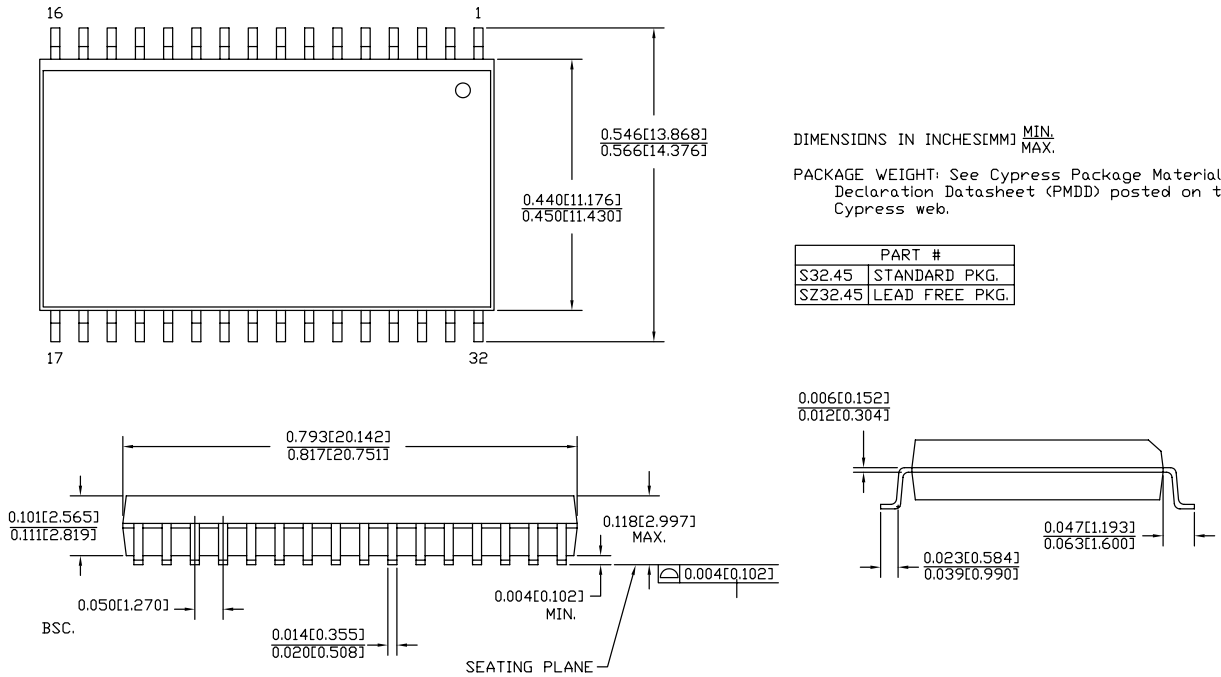
Contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions



**Package Diagrams**

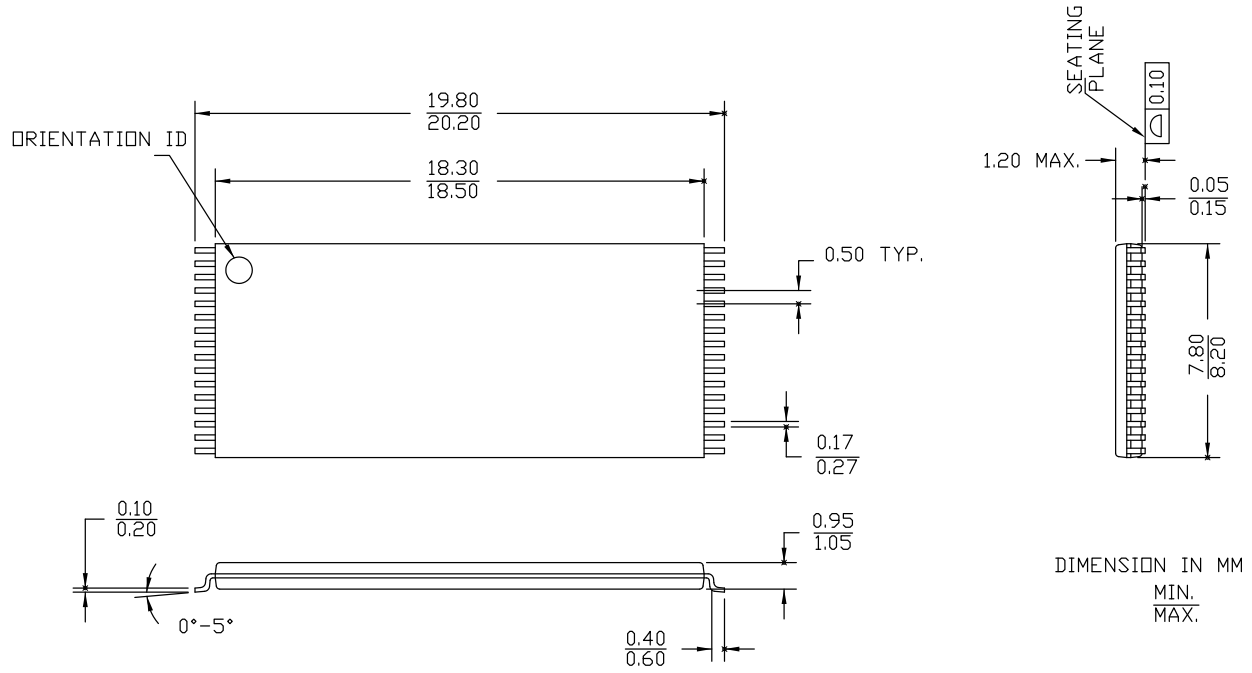
**Figure 11. 32-pin Molded SOIC (450 Mil) S32.45/SZ32.45, 51-85081**



51-85081 \*E

**Package Diagrams** (continued)

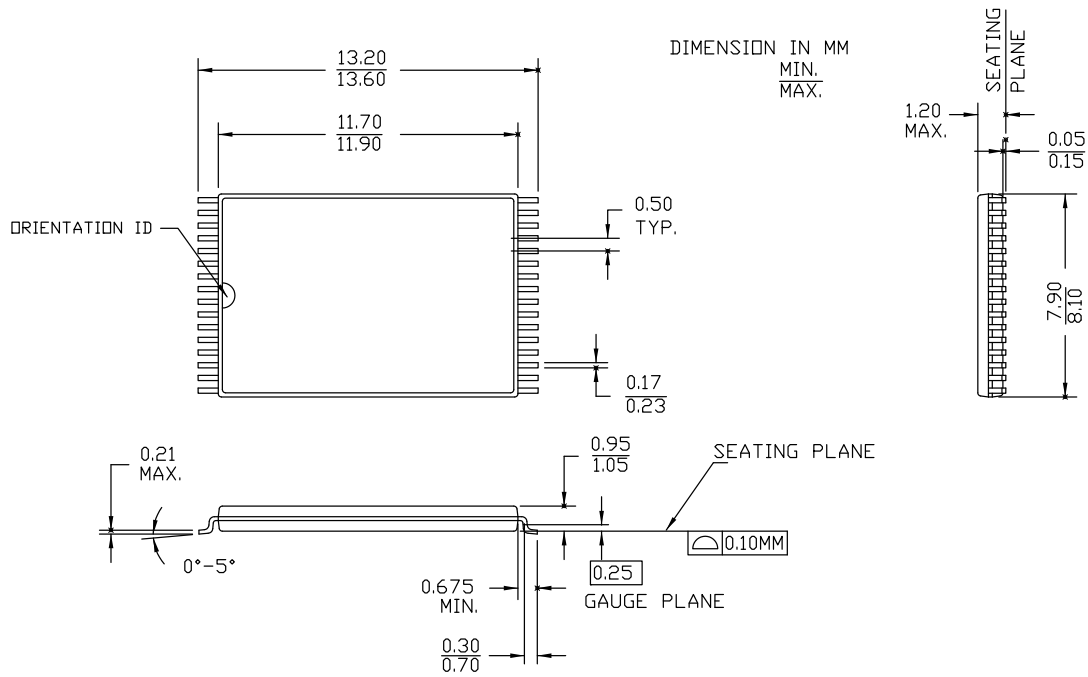
**Figure 12. 32-pin TSOP I (8 × 20 × 1.0 mm) Z32, 51-85056**



51-85056 \*G

Package Diagrams (continued)

Figure 13. 32-pin Small TSOP (8 × 13.4 × 1.2 mm) ZA32, 51-85094



51-85094 \*G

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
STSOP	Shrunk Thin Small Outline Package
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



## Document History Page

Document Title: CY62128EV30 MoBL®, 1-Mbit (128K × 8) Static RAM				
Document Number: 38-05579				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	285473	See ECN	PCI	New data sheet.
*A	461631	See ECN	NXR	<p>Changed status from Preliminary to Final.</p> <p>Removed 35 ns speed bin related information in all instances across the document.</p> <p>Removed “L” version of CY62128EV30 related information in all instances across the document.</p> <p>Removed Reverse TSOP I package related information in all instances across the document.</p> <p>Updated <a href="#">Electrical Characteristics</a>:</p> <p>Changed typical value of I<sub>CC</sub> parameter from 8 mA to 11 mA corresponding to Test Condition “f = f<sub>max</sub>”.</p> <p>Changed maximum value of I<sub>CC</sub> parameter from 12 mA to 16 mA corresponding to Test Condition “f = f<sub>max</sub>”.</p> <p>Changed maximum value of I<sub>CC</sub> parameter from 1.5 mA to 2.0 mA corresponding to Test Condition “f = 1 MHz”.</p> <p>Changed typical value of I<sub>SB2</sub> parameter from 0.5 μA to 1 μA.</p> <p>Changed maximum value of I<sub>SB2</sub> parameter from 1 μA to 4 μA.</p> <p>Updated <a href="#">AC Test Loads and Waveforms</a>:</p> <p>Updated <a href="#">Figure 4</a>:</p> <p>Changed value of AC Test load Capacitance from 50 pF to 30 pF.</p> <p>Updated <a href="#">Data Retention Characteristics</a>:</p> <p>Changed maximum value of I<sub>CCDR</sub> parameter from 1 μA to 3 μA corresponding to Test Condition “LL”.</p> <p>Updated <a href="#">Switching Characteristics</a>:</p> <p>Changed minimum value of t<sub>LZOE</sub> parameter from 3 ns to 5 ns for 45 ns speed bin.</p> <p>Changed minimum value of t<sub>LZCE</sub> parameter from 6 ns to 10 ns for 45 ns speed bin.</p> <p>Changed maximum value of t<sub>HZCE</sub> parameter from 22 ns to 18 ns for 45 ns speed bin.</p> <p>Changed minimum value of t<sub>PWE</sub> parameter from 30 ns to 35 ns for 45 ns speed bin.</p> <p>Changed minimum value of t<sub>SD</sub> parameter from 22 ns to 25 ns for 45 ns speed bin.</p> <p>Changed minimum value of t<sub>LZWE</sub> parameter from 6 ns to 10 ns for 45 ns speed bin.</p> <p>Updated <a href="#">Ordering Information</a>.</p>
*B	464721	See ECN	NXR	Updated <a href="#">Logic Block Diagram</a> .
*C	1024520	See ECN	VKN	<p>Added final Automotive-A and Automotive-E information in all instances across the document.</p> <p>Updated <a href="#">Electrical Characteristics</a>:</p> <p>Added Note 7 and referred the same note in I<sub>SB2</sub> parameter.</p> <p>Updated <a href="#">Data Retention Characteristics</a>:</p> <p>Added Note 10 and referred the same note in I<sub>CCDR</sub> parameter.</p> <p>Updated <a href="#">Ordering Information</a>.</p>
*D	2257446	See ECN	NXR	<p>Updated <a href="#">Maximum Ratings</a>:</p> <p>Changed the Maximum rating of “Ambient Temperature with Power Applied” from 55 °C to +125 °C to –55 °C to +125 °C.</p>
*E	2702841	05/06/2009	VKN / PYRS	<p>Updated <a href="#">Switching Characteristics</a>:</p> <p>Updated description of t<sub>PD</sub> parameter.</p> <p>Updated <a href="#">Ordering Information</a> (Added -45SXA part).</p>
*F	2781490	10/08/2009	VKN	Updated <a href="#">Ordering Information</a> (Included “CY62128EV30LL-45ZAXA” part).

**Document History Page** (continued)

Document Title: CY62128EV30 MoBL®, 1-Mbit (128K × 8) Static RAM				
Document Number: 38-05579				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
*G	2934428	06/03/10	VKN	Updated <a href="#">Truth Table</a> : Added Note 34 and referred the same note in 'X' in " $\overline{CE}_1$ " and " $CE_2$ " columns. Updated <a href="#">Package Diagrams</a> . Updated to new template.
*H	3026548	09/12/2010	AJU	Updated <a href="#">Pin Configuration</a> . Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Minor edits.
*I	3115909	01/06/2011	RAME	Separated Automotive and Industrial parts from this data sheet. Removed Automotive related information in all instances across the document.
*J	3292906	06/25/2011	AJU	Updated <a href="#">Functional Description</a> : Removed the Note "For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at <a href="http://www.cypress.com">http://www.cypress.com</a> website." and its reference. Updated <a href="#">Package Diagrams</a> . Updated to new template.
*K	4499499	09/11/2014	MEMJ	Updated <a href="#">Switching Characteristics</a> : Added Note 19 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added Note 33 and referred the same note in <a href="#">Figure 10</a> . Updated <a href="#">Package Diagrams</a> : spec 51-85081 – Changed revision from *C to *E. spec 51-85056 – Changed revision from *F to *G. spec 51-85094 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.
*L	4581542	11/27/2014	VINI	Updated <a href="#">Functional Description</a> : Added "For a complete list of related resources, <a href="#">click here</a> ." at the end. Updated <a href="#">Maximum Ratings</a> : Referred Notes 3, 4 in "Supply voltage to ground potential".
*M	4920942	09/15/2015	VINI	Updated to new template. Completing Sunset Review.
*N	5445076	09/22/2016	VINI	Updated <a href="#">Thermal Resistance</a> : Replaced "two-layer" with "four-layer" in "Test Conditions" column. Updated all values of $\Theta_{JA}$ and $\Theta_{JC}$ parameters. Updated to new template. Completing Sunset Review.

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