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Team Nexperia

PMR280UN

N-channel TrenchMOS ultra low level FET

Rev. 2 — 3 February 2012 Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in ultra small Surface-Mounted Device (SMD) plastic package using TrenchMOS technology.

1.2 Features and benefits

- Surface mounted package
- Low on-state resistance
- Footprint 63% smaller than SOT23
- Low threshold voltage

1.3 Applications

- Driver circuits
- Switching in portable appliances

1.4 Quick reference data

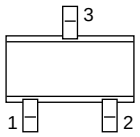
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	20	V
I_D	drain current	$T_{sp} = 25$ °C; $V_{GS} = 4.5$ V	-	-	0.98	A
V_{GS}	gate-source voltage		-8	-	8	V
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 0.2$ A; $T_j = 25$ °C	-	280	340	mΩ

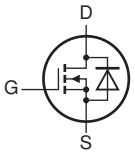
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	D	drain		



SOT416 (SC-75)



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3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMR280UN	SC-75	plastic surface-mounted package; 3 leads	SOT416

4. Marking

Table 4. Marking codes

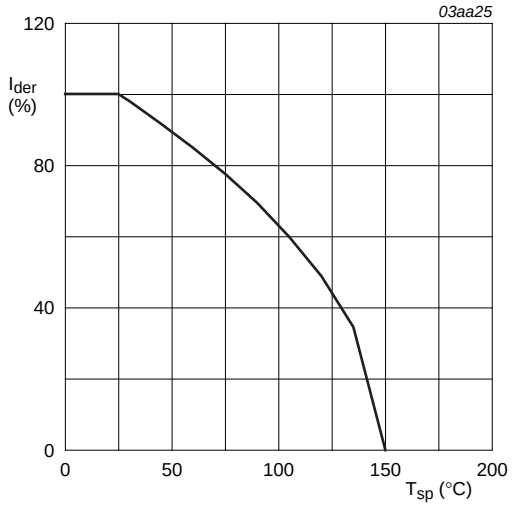
Type number	Marking code
PMR280UN	R5

5. Limiting values

Table 5. Limiting values

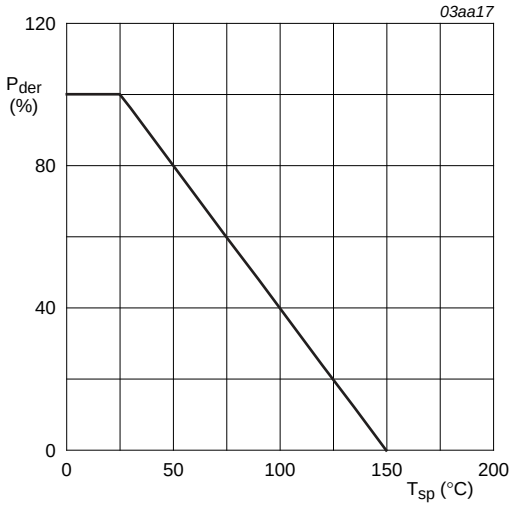
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	20	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; $R_{GS} = 20$ kΩ	-	20	V
V_{GS}	gate-source voltage		-8	8	V
I_D	drain current	$T_{sp} = 25$ °C; $V_{GS} = 4.5$ V	-	0.98	A
		$T_{sp} = 100$ °C; $V_{GS} = 4.5$ V	-	0.62	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ µs	-	1.97	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C	-	0.53	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25$ °C	-	0.44	A
I_{SM}	peak source current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ µs	-	0.88	A



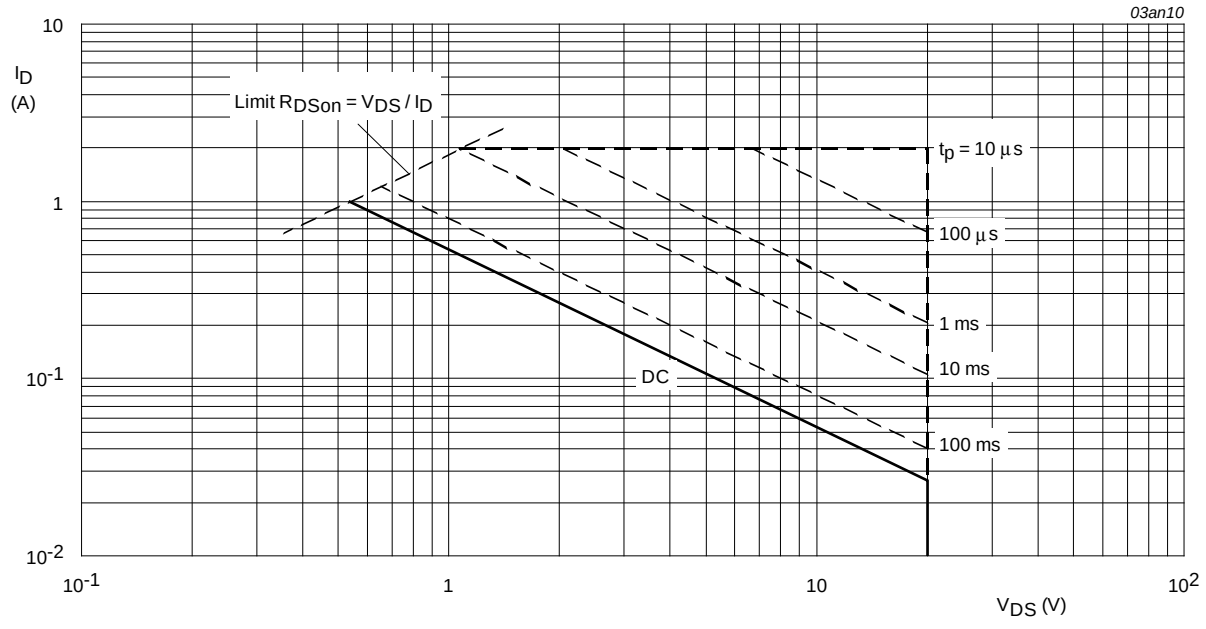
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$$T_{sp} = 25°C; I_{DM} \text{is single pulse}; V_{GS} = 4.5V$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}sp)}$	thermal resistance from junction to solder point		-	-	235	K/W

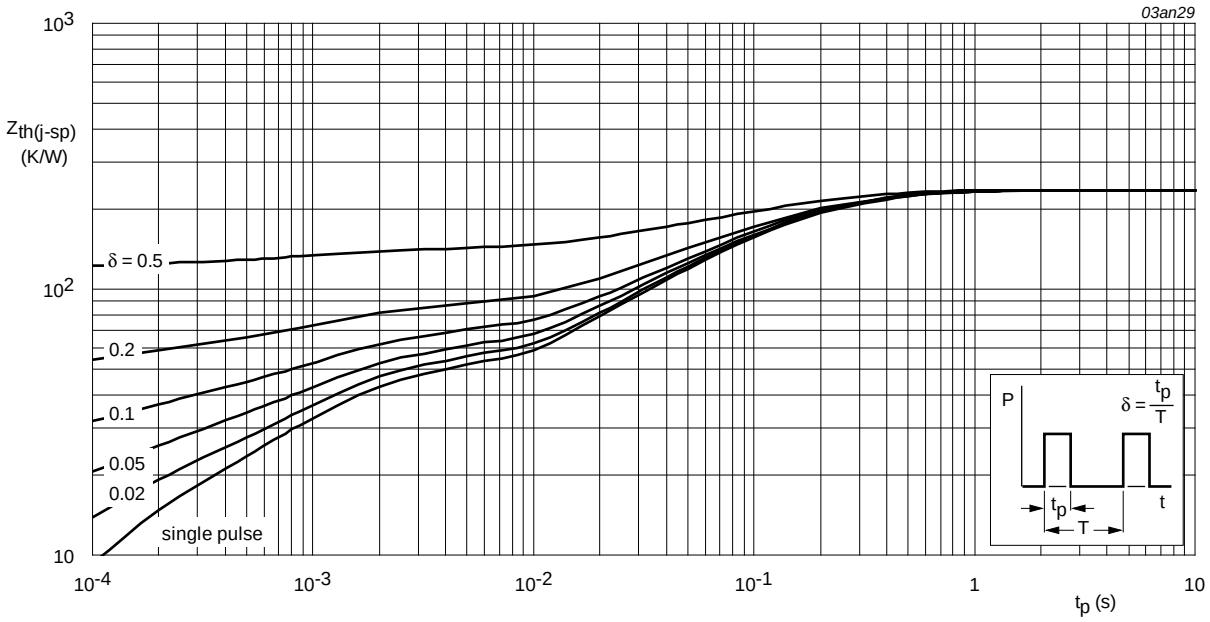
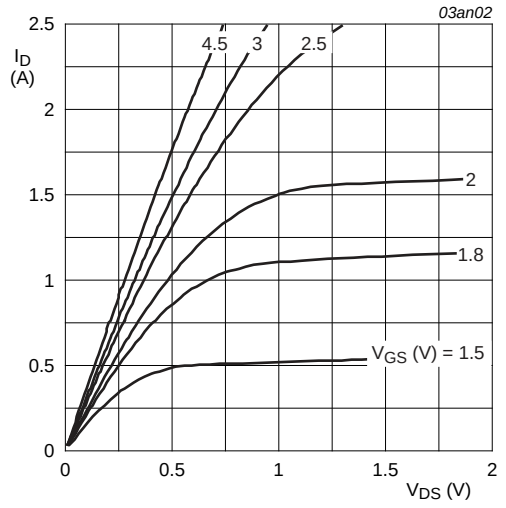


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

7. Characteristics

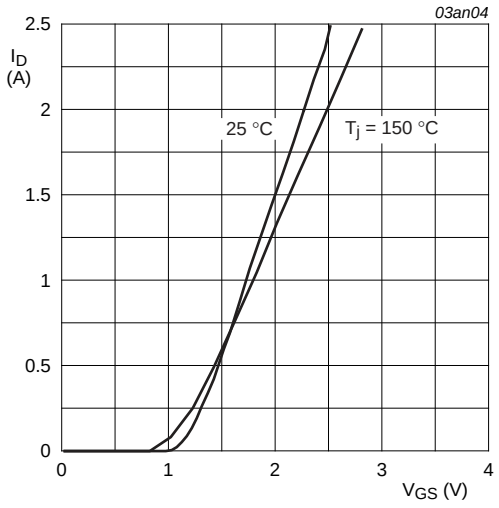
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 1 µA; V_{GS} = 0 V; T_j = 25 °C	20	-	-	V
		I_D = 1 µA; V_{GS} = 0 V; T_j = -55 °C	18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 0.25 mA; V_{DS} = V_{GS}; T_j = 25 °C	0.45	0.7	1	V
		I_D = 0.25 mA; V_{DS} = V_{GS}; T_j = 150 °C	0.25	-	-	V
		I_D = 0.25 mA; V_{DS} = V_{GS}; T_j = -55 °C	-	-	1.2	V
I_{DSS}	drain leakage current	V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 20 V; V_{GS} = 0 V; T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.2 A; T_j = 25 °C	-	280	340	mΩ
		V_{GS} = 4.5 V; I_D = 0.2 A; T_j = 150 °C	-	448	544	mΩ
		V_{GS} = 2.5 V; I_D = 0.1 A; T_j = 25 °C	-	360	430	mΩ
		V_{GS} = 1.8 V; I_D = 0.075 A; T_j = 25 °C	-	460	660	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 1 A; V_{DS} = 10 V; V_{GS} = 4.5 V; T_j = 25 °C	-	0.89	-	nC
Q_{GS}	gate-source charge		-	0.13	-	nC
Q_{GD}	gate-drain charge		-	0.18	-	nC
C_{iss}	input capacitance	V_{DS} = 20 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	45	-	pF
C_{oss}	output capacitance		-	11	-	pF
C_{rss}	reverse transfer capacitance		-	7	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 10 V; R_L = 10 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	4.5	-	ns
t_r	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	18.5	-	ns
t_f	fall time		-	5	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 0.3 A; V_{GS} = 0 V; T_j = 25 °C	-	0.83	1.2	V



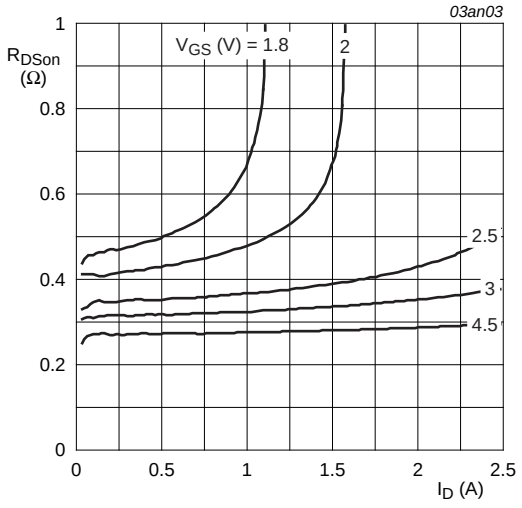
$T_j = 25°C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



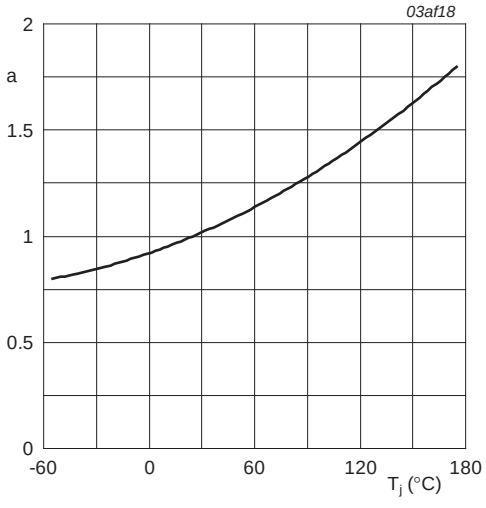
$T_j = 25°C \text{ and } 150°C; V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



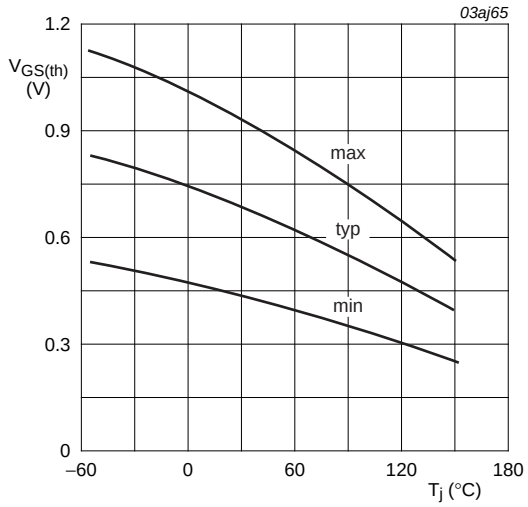
$T_j = 25°C$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



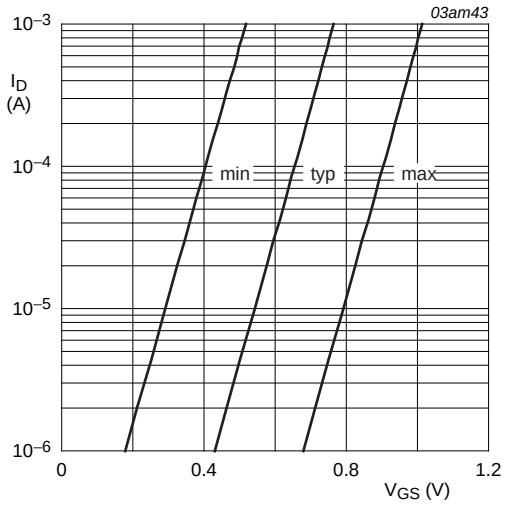
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



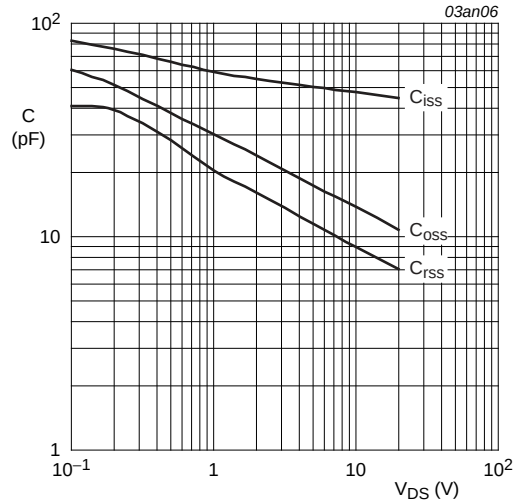
I_D = 0.25 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature



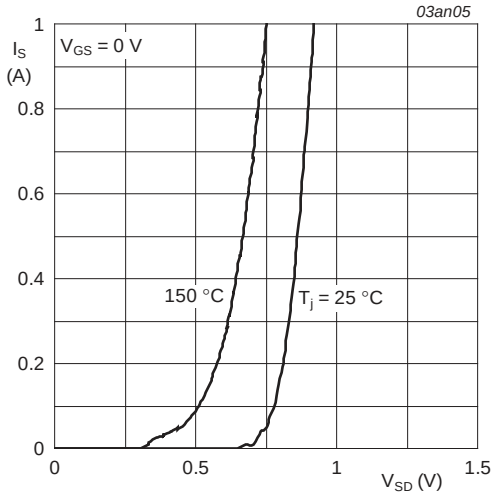
$T_j = 25°C; V_{DS} = 5V$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$V_{GS} = 0V; f = 1MHz$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25°C$ and $150°C; V_{GS} = 0V$

Fig 12. Source current as a function of source-drain voltage; typical values

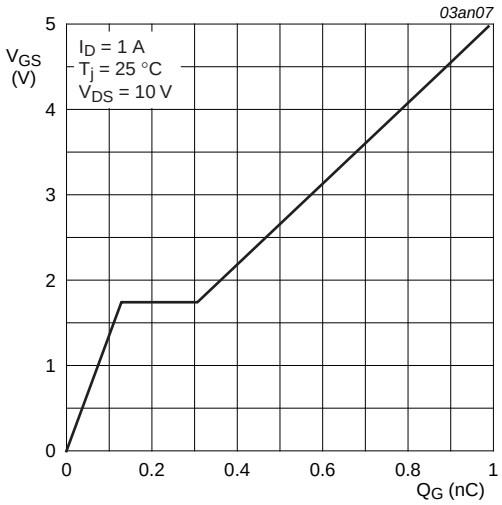


Fig 13. Gate-source voltage as a function of gate charge; typical values

8. Package outline

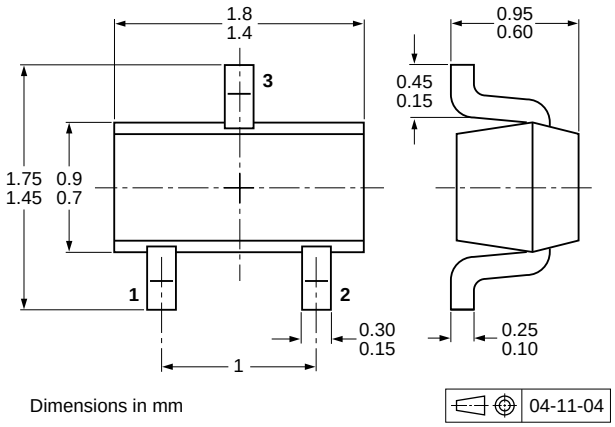


Fig 14. Package outline SOT416 (SC-75)

9. Soldering

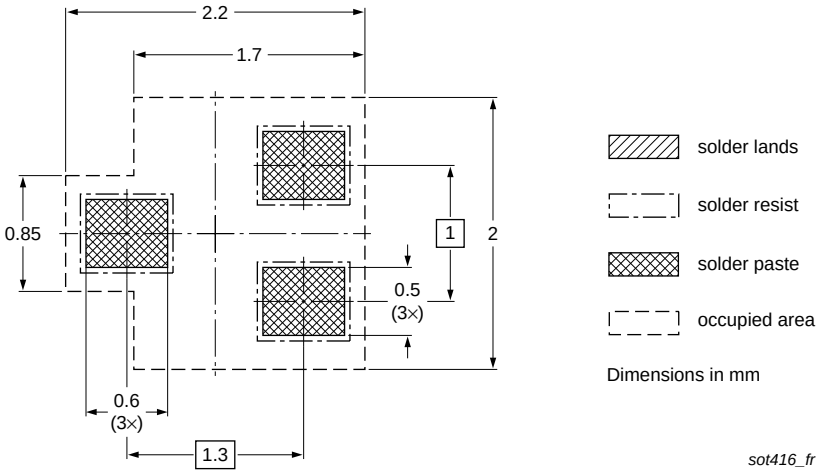


Fig 15. Reflow soldering footprint for SOT416 (SC-75)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMR280UN v.2	20120203	Product data sheet	-	PMR280UN v.1
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
PMR280UN v.1	20040305	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contents

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