PERICOM®

PI3VDP1431
PI3VDP1413A

Low Power Dual-mode DisplayPort 3.4Gb/s Level Shifter/Redriver

Features

- Dual-mode DisplayPort level shifter/Redriver
- Operation up to 3.4 Gbps per lane (340MHz pixel clock)
- 4K Ultra HD, 3D video formats (1080p, 1080i, 720p), 48-bit per pixel Deep Color support
- Low standby current with DDC passive Switch or Buffer mode
- Flexible 3 steps equalization control steps: 2.5, 5, 7.5 dB
- Pre-emphasis control 3 steps: 0, 1.5, 2.5 dB
- Automatic output squelch and HPD function for power saving states management at no input signal condition
- Convert low-swing DC or AC coupled differential input
- Integrated DDC level shifter or DDC Buffer (A version)
- Signal Input channels with pull-down termination resistor
- 3.3V single power supply
- Pin-to-Pin compatible with PI3HDMI511/PI3HDX511A
- Integrated ESD protection on I/O pins. +4k/-8kV contact
- 32-pin TQFN(ZLS32) 3x6mm package

Description

PI3VDP1431 is a low power dual-mode DisplayPort Level Shifter with intergrated 3.4Gbps redriver to improve jitter performance. Input channels has as pull-down termination resistors(RT), optimized for displayport level shifter application.

For mobile platforms, extended battery hours have been one of the most demanding features. This product supports output squelch and/or HPD detection for smart power management to extend battery life with < 1mA stand-by current.

The device converts AC and DC coupled input signals to the compliant signals in the HDMI or dual-mode DisplayPort source systems. Programmable TMDS input signal equalization helps to solve the compliance jitter issues, creating in the non-standard HDMI source system with robust ESD/EOS protection.

Application

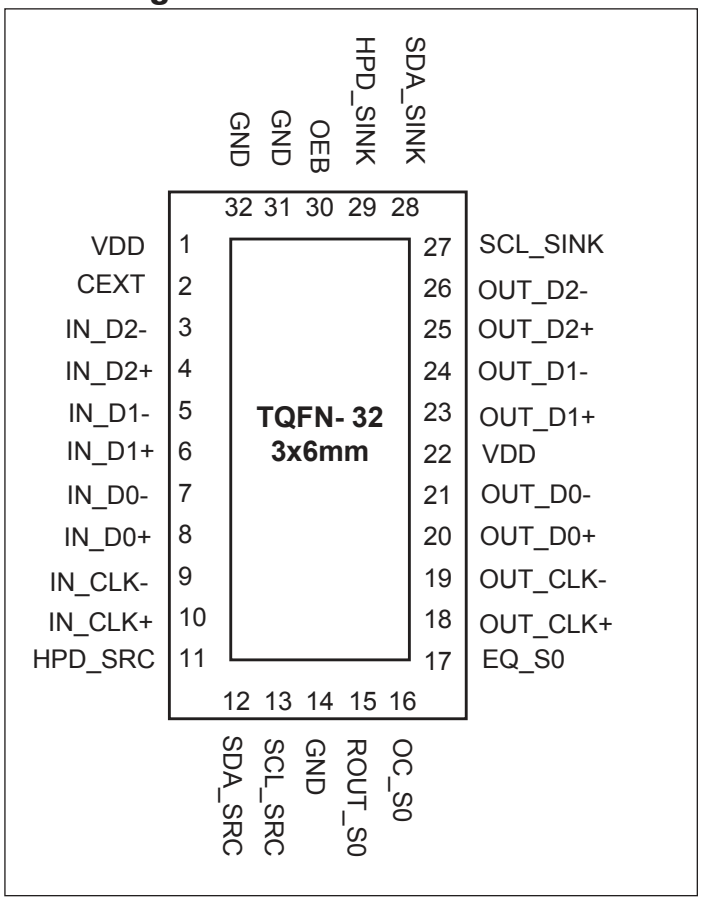
- Notebook and Desktop computers

Device Information

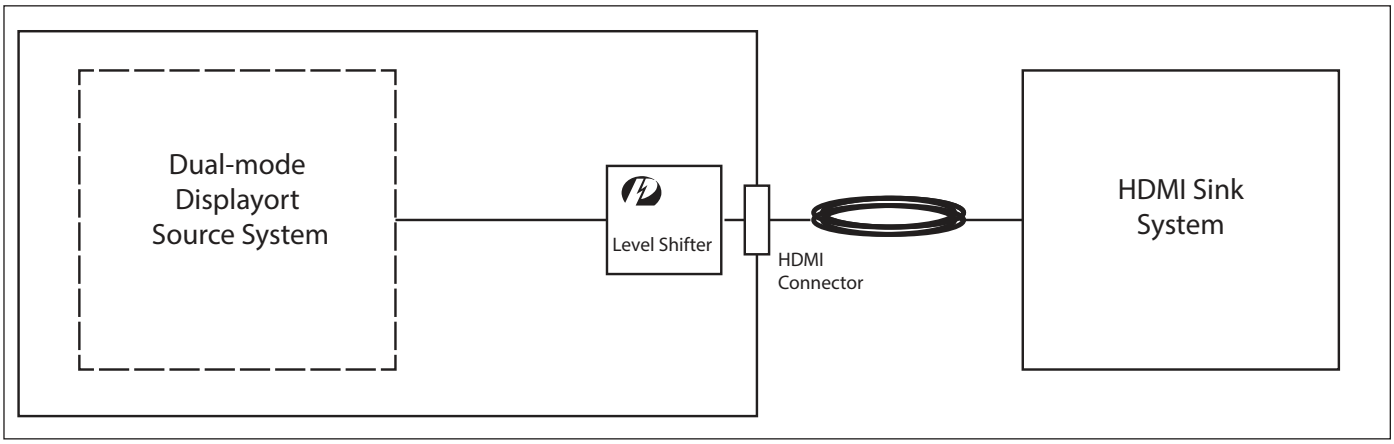
Part Number	Package/Body Size	Description
PI3VDP1431	TQFN(32) 3x6mm	DDC Switch
PI3VDP1431A	TQFN(32) 3x6mm	DDC Buffer

Note: Please refer ordering addendum at the end of the datasheet

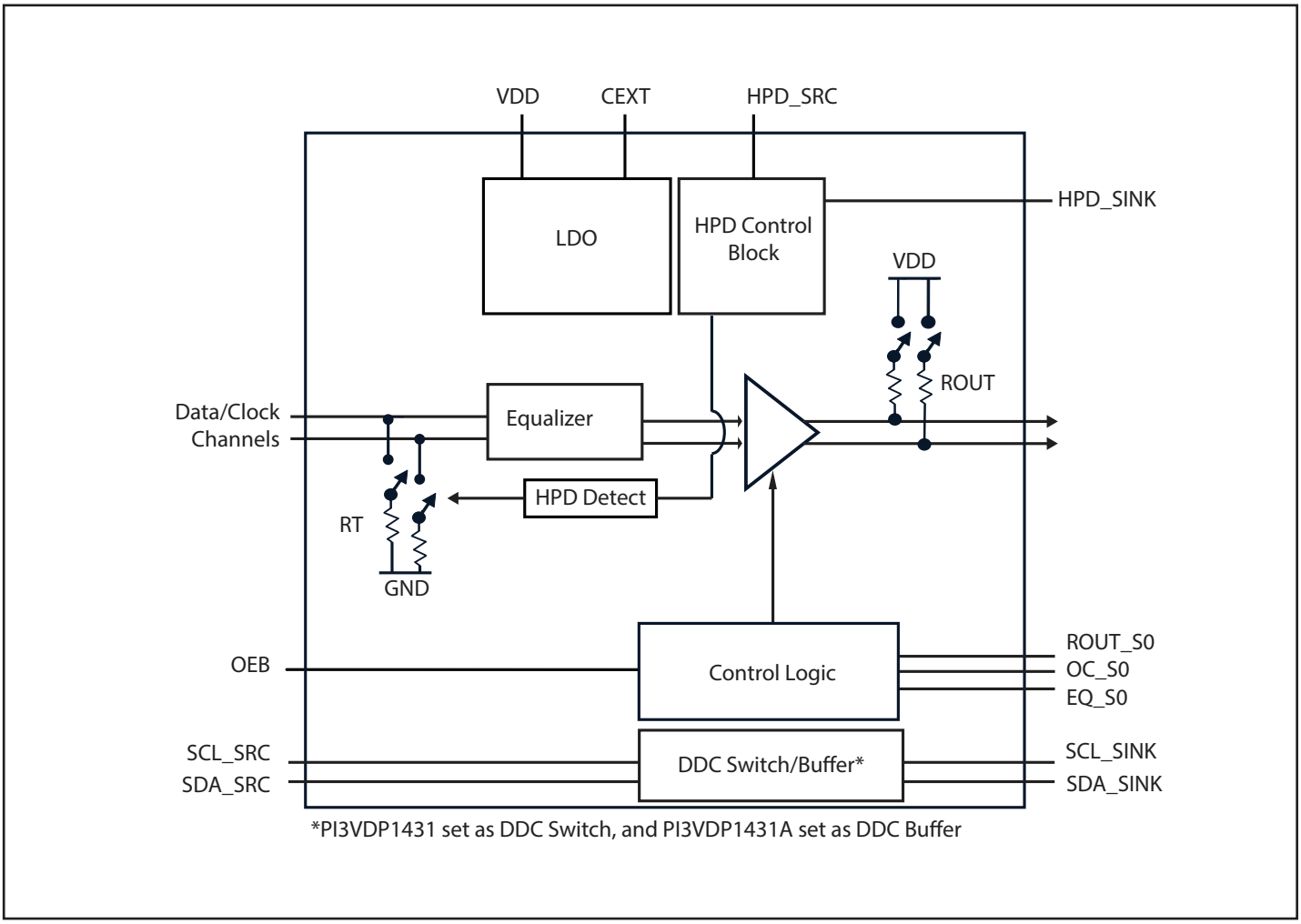
Pin Configuration



Application diagram



Block diagram



Pin Description

Pin #	Pin Name	Type	Description
1,22	VDD	PWR	3.3V power supply. Add external 0.1uF capacitor to GND
2	CEXT	PWR	LDO output for internal core supplier. Add external capacitor (2.2uF-4.7uF) to GND
14,31,32	GND	GND	Ground connection
29	HPD_SINK	I	Sink side hot plug detector input; internal pull-down at 120 Kohm.
11	HPD_SRC	O	HPD output to source side
3 4 5 6 7 8 9 10	IN_D2- IN_D2+ IN_D1- IN_D1+ IN_D0- IN_D0+ IN_CLK- In_CLK+	I	TMDS inputs. RT=50Ohm
26 25 24 23 21 20 19 18	OUT_D2- OUT_D2+ OUT_D1- OUT_D1+ OUT_D0- OUT_D0+ OUT_CLK- OUT_CLK+	O	TMDS outputs. ROUT=50Ohm is active when ROUT_S0 = "1"
13	SCL_SRC	IO	Source side DDC Clock
12	SDA_SRC	IO	Source side DDC Data
27	SCL_SINK	IO	Sink side DDC Clock for connector
28	SDA_SINK	IO	Sink side DDC Data for connector
16	OC_S0	I	TMDS output three-level pre-emphasis selection. See OC_S0 truth table. GND=0dB, NC=1.5dB, VDD=2.5dB;
17	EQ_S0	I	TMDS input three-level equalization selection. See EQ_S0 truth table. GND=2.5dB, NC=5dB, VDD=7.5dB;
30	OEB	I	Output Enable control. Active low. Internal pull-down at 100 Kohm.
15	ROUT_S0	I	TMDS output double termination selection. Internally pull-up to VDD.

Functional Description

Squelch Function:

Automatic output squelch function disables TMDS output when no Input signal presents. Output Disable (Squelch) Mode uses TMDS Clock channel signal detection. When low voltage levels on the TMDS input clock signals are detected, Squelch state enables and TMDS output port signals shall disable; when the TMDS clock input signal levels are above a pre-determined threshold voltage, output ports shall return to the normal voltage swing levels.

HPD_SINK Shut Down

When HPD_SINK pin is floating or tie to GND, TMDS outputs shall shut down to sleep mode; HPD_SINK does not control DDC channel.

Pre-emphasis Control OC_S0 Truth Table

Output pre-emphasis setting		Functional Description		Notes
ROUT_S0	OC_S0	Single-end Vswing	Pre-emphasis	
"0"	"0"	500 mV	0 dB	Open drain output.
	"NC" or VDD/2	500 mV	1.5 dB	Open drain output: default
	"1"	500 mV	2.5 dB	Open drain output
"1"	"0"	500 mV	0 dB	Double termination
	"NC" or VDD/2	500 mV	1.5 dB	Double termination: default
	"1"	500 mV	2.5 dB	Double termination

Input Equalization EQ _S0Truth Table

EQ_S0	Functional Description	Note
"0"	2.5 dB	TMDS Clock(CLK) channel EQ is always fixed as 3dB without pre-emphasis.
"NC" or VDD/2	5 dB	
"1"	7.5 dB	

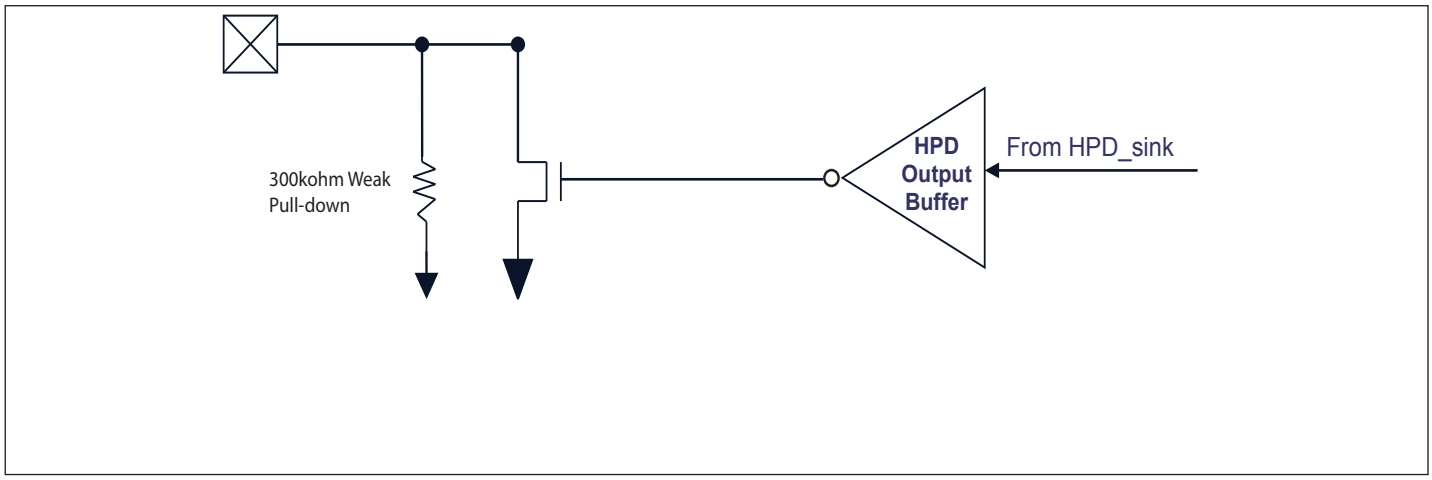
Output Signal Enable OEB Truth Table

OEB	Functional Description
"0"	Normal mode
"1"	Disable output signal for power saving mode

Sink side Hot Plug Detect HPD_SINK Truth Table

HPD_SINK	Functional Description
"1"	Normal mode
"0"	Disable output signal for power saving mode

Source side HPD_SRC Block Diagram



Note:
*1: Open drain buffer is recommended with external pull-up resistor to <4.5V power supply.

Absolute Maximum Ratings

Item	Absolute Rating*1
Supply Voltage to Ground Potential	4.5V
All Inputs and Outputs	-0.5V to 4.5V
5V Tolerance I/O (SDA_SINK,SCL_SINK,HPD_SINK)	-0.5V to 5.5V
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Note *1) Stress beyond those lists under "Absolute Maximum Ratings" may cause permanent damage to the device

Recommended Operation Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
TA	Ambient Operating Temperature	-20	25	85	°C
VDD	Power Supply Voltage	2.89	3.3	3.6	V

DC Specification (VDD = 3.3V ±10%)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
IDD	VDD Supply Current	Open drain, 500mV single-end, Pre-emphasis 0dB		80	100	mA
ISTB	Stand-by mode	VDD=3.6V, DDC passive switch, HPD_SINK="0", OEB="1"		40	50	uA
ISQLH	Squelch mode current	VDD=3.6V, DDC passive switch, HPD_SINK=3.6V		2.7	4	mA

HPD_SRC pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VOL	Open Drain Output Low Voltage	IOL = 4 mA	0		0.4	V
IOFF	Off leakage current	VDD=0, VIN=3.6V			25	µA
IOZ	Open drain Output leakage current	VDD=3.6, VIN=3.6V			25	

HPD_SINK

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IIH	High level digital input current(1)	VIH =5.5V	-10		80	µA
IIL	Low level digital input current(1)	VIL = GND	-10		10	µA
VIH	High level digital input voltage	VDD=3.3V	2.0			V
VIL	Low level digital input voltage	VDD=3.3V	0		0.8	V

Control pin (OEB with 100k pull to gnd)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IIH	High level digital input current	VIH =3.3V	-10		40	µA
IIL	Low level digital input current	VIL = GND	-10		10	µA
VIH	High level digital input voltage		2.0			V
VIL	Low level digital input voltage		0		0.8	V

Control pin (EQ_S0, OC_S0 with 100k pull high and 100k pull down when TMDS active)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IIH	High level digital input current	VIH =3.3V	-10		40	µA
IIL	Low level digital input current	VIL = GND, VDD=3.3V	-40		10	µA

Control pin (ROUT_S0)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IIH	High level digital input current	VIH =VDD	-10		10	µA
IIL	Low level digital input current	VIL = GND	-20		10	µA
VIH	High level digital input voltage		2.0			V
VIL	Low level digital input voltage		0		0.8	V

DDC Channel switch (P/N: PI3VDP1431)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ILK	Input leakage current	DDC switch is OFF, VIN=5.5V	-10		30	µA
CIO	Input/Output capacitance when passive switch on	VIpp(peak-peak) = 1V, 100 kHz		10		pF
RON	Passive Switch resistance	IO = 3mA, VO = 0.4V		30	50	Ω
VPASS	Switch Output voltage	VI=3.3V, II=100uA, VDD=3.3V	1.5	2.0	2.5	V

DDC Channel Buffer (P/N: PI3VDP1431A)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIH_SRC	Source Side DDC Buffer Input High Voltage		0.6			V
VIL_SRC	Source Side DDC Buffer Input Low Voltage				0.4	V
VOL_SRC	Source Side DDC Buffer Output Low Voltage	External pull-up to VDD from 1.5kΩ to 10kΩ	0.47	0.52	0.6	V
VOL_SINK	Sink Side DDC Buffer Output Low Voltage				0.2	V
VIH_SINK	Sink Side DDC Buffer Input High Voltage		2.0			V
VIL_SINK	Sink Side DDC Buffer Input Low Voltage				0.8	V
CI_SRC	Source side DDC capacitance when active switch is on, or passive switch off	VIpp(peak-peak)=1V, 100 KHz		5		pF
CI_SINK	Sink side DDC capacitance when active switch is on, or passive switch off			5		pF

TMDS differential pins

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VOH	Single-ended high level output voltage	VDD = 3.3V, ROUT=50Ω	VDD-10		VDD+10	mV
VOL	Single-ended low level output voltage		VDD-600		VDD–400	mV
VSWING	Single-ended output swing voltage		400		600	mV
VOD(O)*1	Overshoot of output differential voltage				180*1	mV
VOD(U)*2	Undershoot of output differential voltage				200*2	mV
VOC(SS)	Change in steady-state common- mode output voltage between logic states				5	mV
IOS	Short Circuit output current at open drain mode	Short to VDD	-12		12	mA
	Short Circuit output current at double termination mode	Short to VDD	-24		24	mA
VI(open)	Single-ended input voltage under high impedance input or open input	II = 10uA	VDD-10		VDD+10	mV
RT	Input termination resistance	VIN = 2.9V	45	50	55	Ω
IOZ	Leakage current with Hi-Z I/O	VDD = 3.6V,			30	µA

Note:

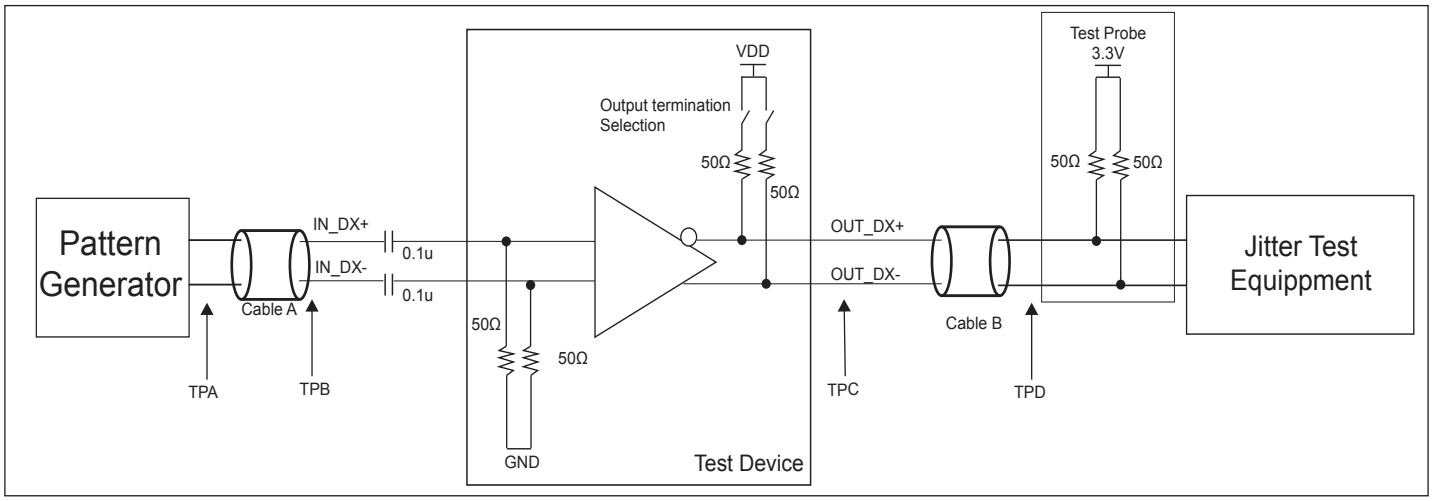
*1) Overshoot of output differential voltage VOD(O) = (VSWING(MAX) * 2) * 15%

*2) Undershoot of output differential voltage VOD(O) = (VSWING(MIN) * 2) * 25%

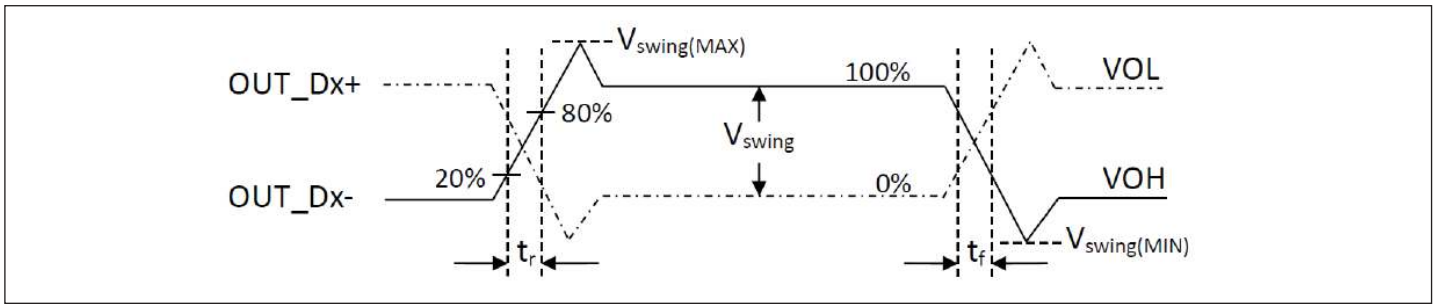
AC Characteristics (Over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
TMDS differential pins						
tPD	Propagation delay	VDD = 3.3V ROUT = 50Ω			2000	ps
tR/tF	Differential output signal rise/fall time(20% - 80%), open drain, 0dB pre-emphasis			120		
	Differential output signal rise/fall time (20% - 80%), open drain, 2.5dB pre-emphasis			100		
tSK(P)	Pulse skew			10	50	
tSK(D)	Intra-pair differential skew			23	50	
tSK(O)	Inter-pair differential skew				100	
tJIT(PP)	Peak-to-peak output Clock residual jitter	Data Input = 3.4 Gbps HDMI data patterns		30	60	
tJIT(PP)	Peak-to-peak output DATA Residual Jitter			40	70	
tEN	Enable time				50	µs
tDIS	Disable time				0.01	
DDC I/O pins (passive switch)						
tPD(DDC)	Propagation delay : SCL_SINK/SDA_SINK to SCL/SDA or SCL/ SDA to SCL_SINK/SDA_ SINK in passive SW	CL = 10pF			5	ns
Control and Status Pins (HPD_SINK, HPD)						
tPD(HPD)	Propagation delay : From HPD_SINK to the active port of HPD, high to low	CL = 10pF, Pull high resistor=1kΩ Open drain		10		ns

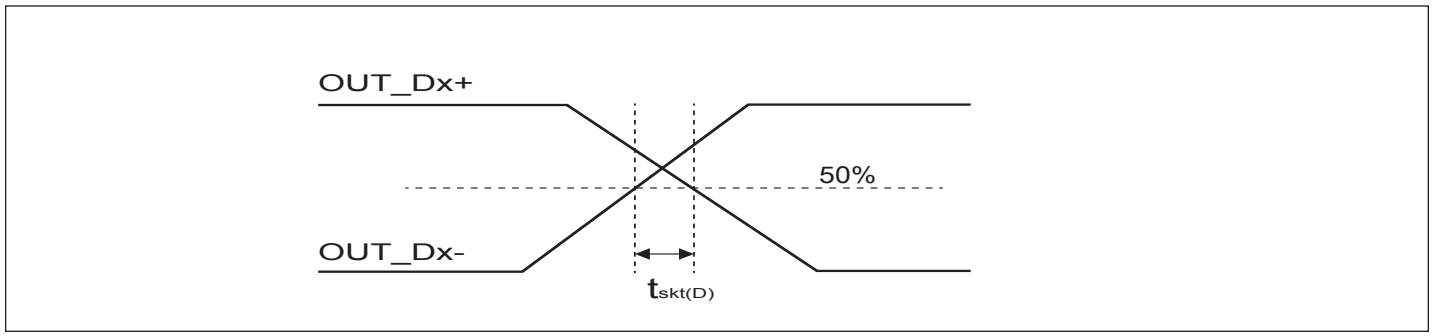
Input Measurement Test Setup



Rise/Fall Time and Single-ended Swing Voltage

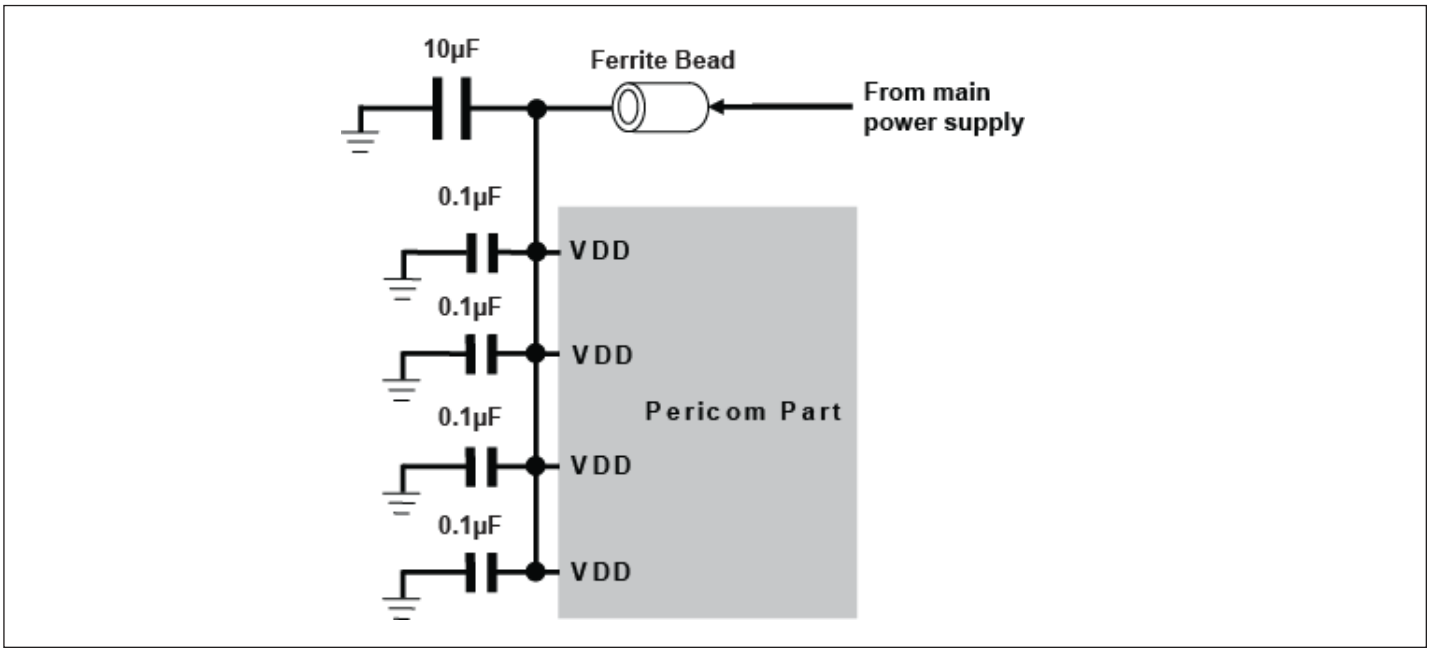


Intra-pair Skew Definition



Power Supply Decoupling Circuit

It is recommended to put 0.1 µF decoupling capacitors on each VDD pins of our part, there are four 0.1 µF decoupling capacitors are put in Figure 1 with an assumption of only four VDD pins on our part, if there is more or less VDD pins on our Pericm parts, the number of 0.1 µF decoupling capacitors should be adjusted according to the actual number of VDD pins. On top of 0.1 µF decoupling capacitors on each VDD pins, it is recommended to put a 10 µF decoupling capacitor near our part's VDD, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.



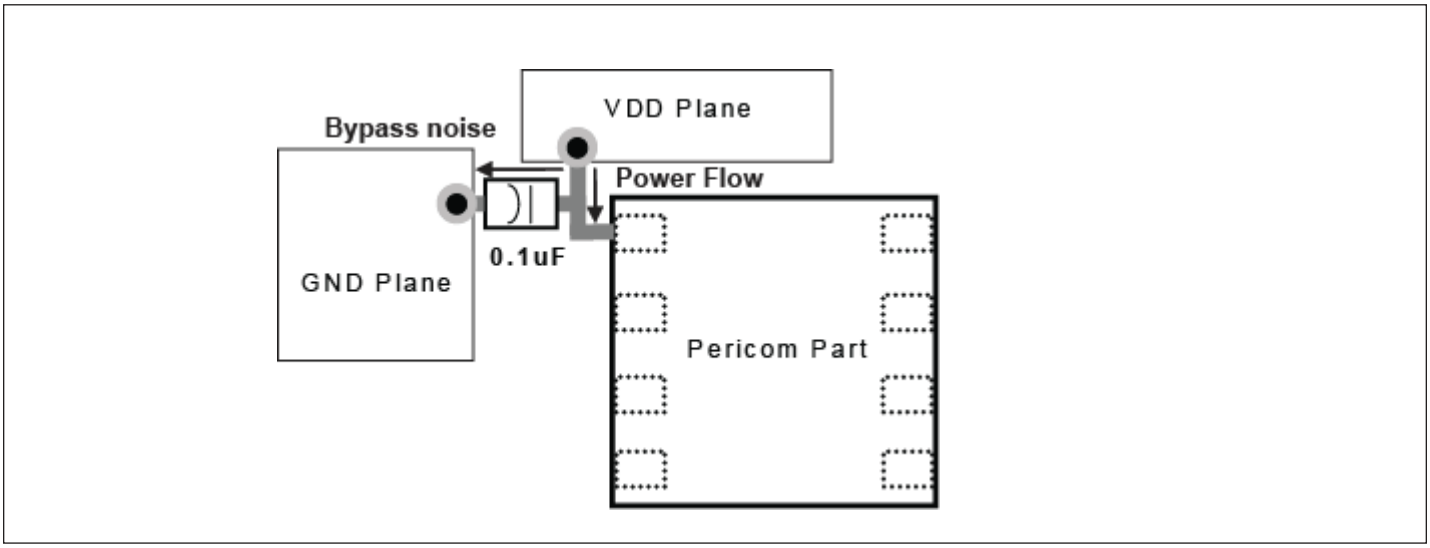
Recommended Power Supply Decoupling Capacitor Diagram

De-coupling Capacitors Requirements

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

Layout Placement Consideration

- ➔ Each 0.1 µF decoupling capacitor should be placed as close as possible to each VDD pin.
- ➔ VDD and GND planes should be used to provide a low impedance path for power and ground.
- ➔ Via holes should be placed to connect to VDD and GND planes directly.
- ➔ Trace should be as wide as possible
- ➔ Trace should be as short as possible.
- ➔ The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- ➔ 10 µF Capacitor should also be placed closed to our part and should be placed in the middle location of 0.1 µF capacitors.
- ➔ Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes. Since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.

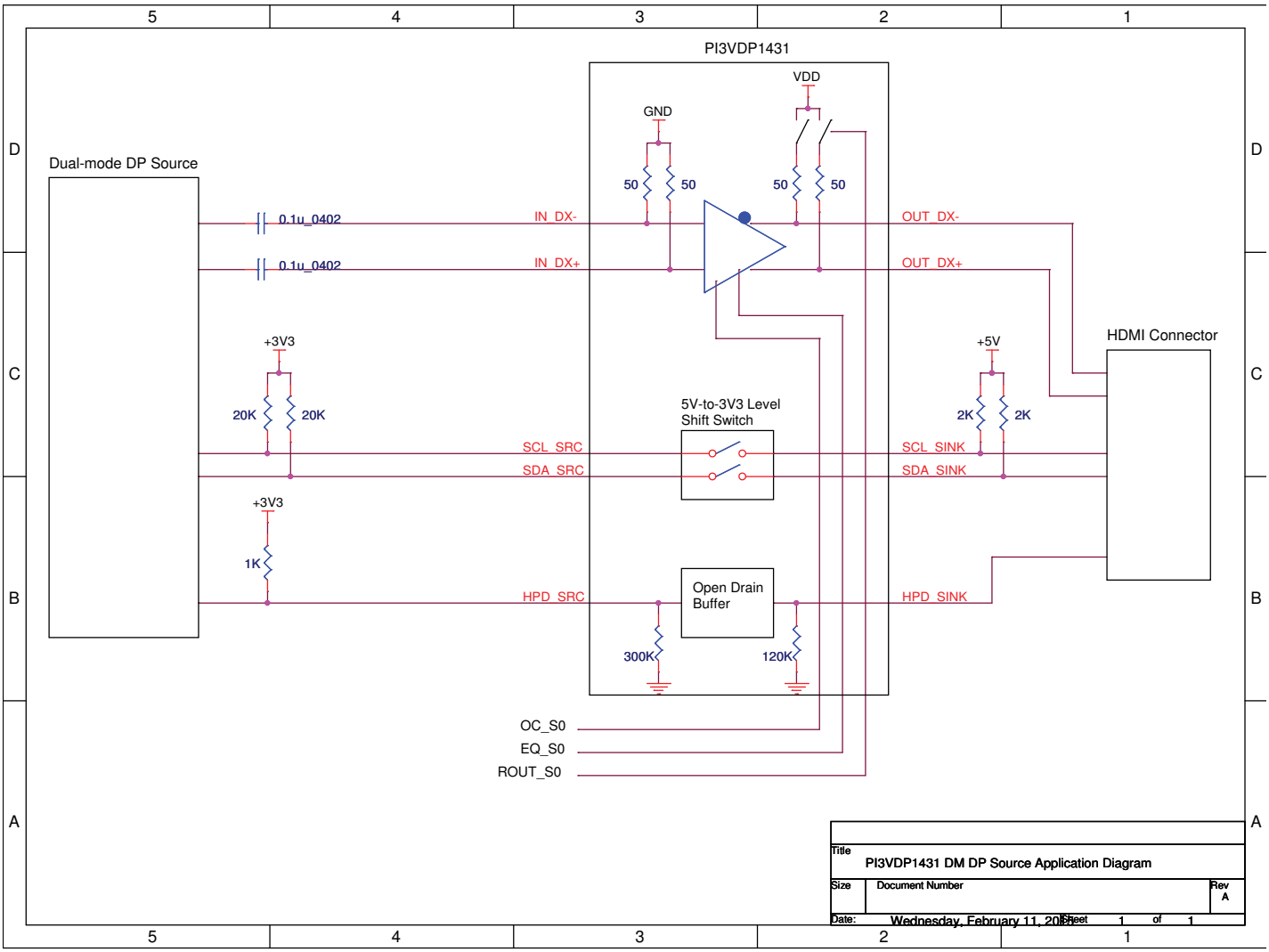


Decoupling Capacitor Placement Diagram

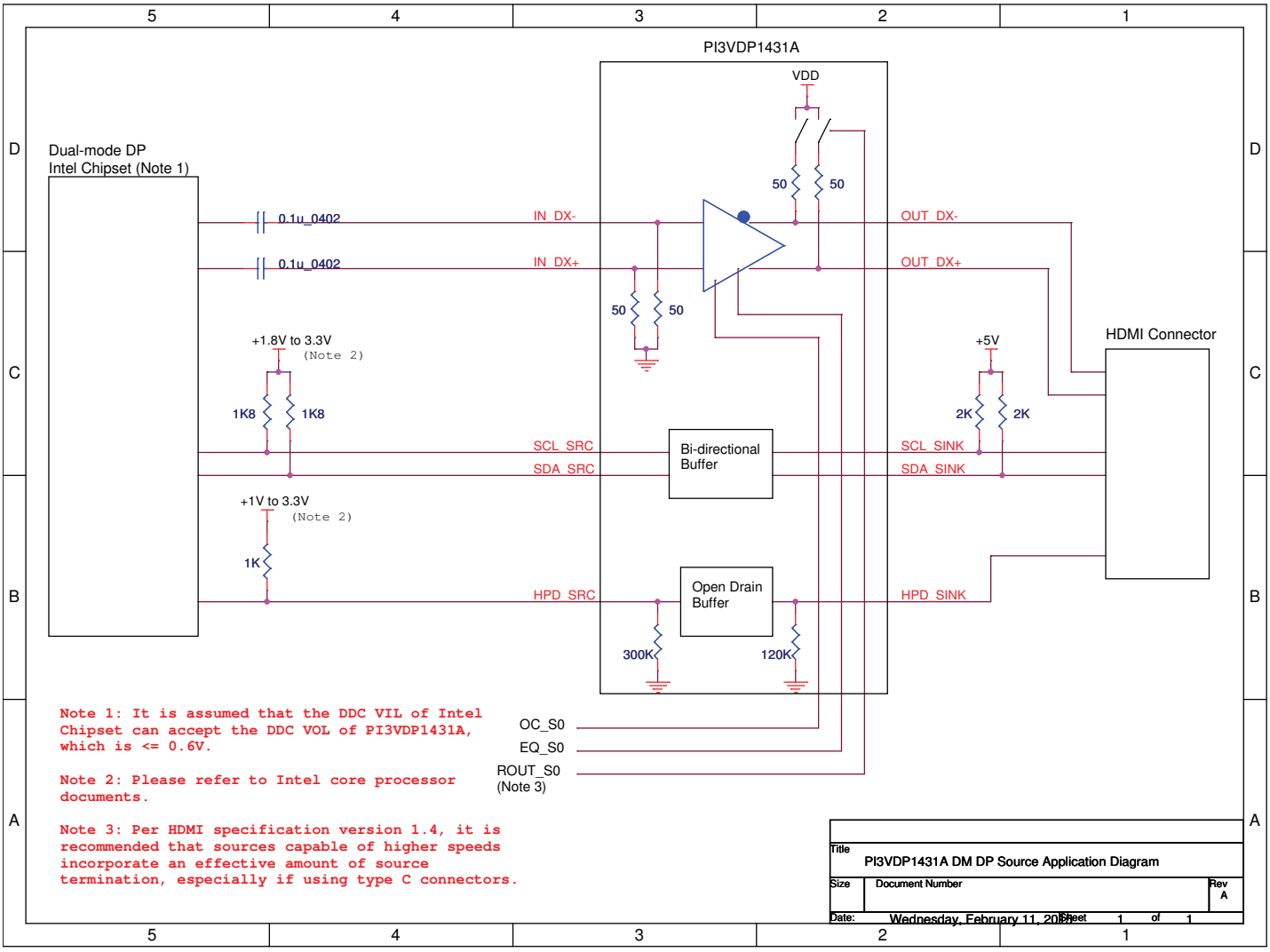
PI3VDP1431, PI3VDP1431A

Low Power Dual-mode DisplayPort 3.4Gb/s Level Shifter/Redriver

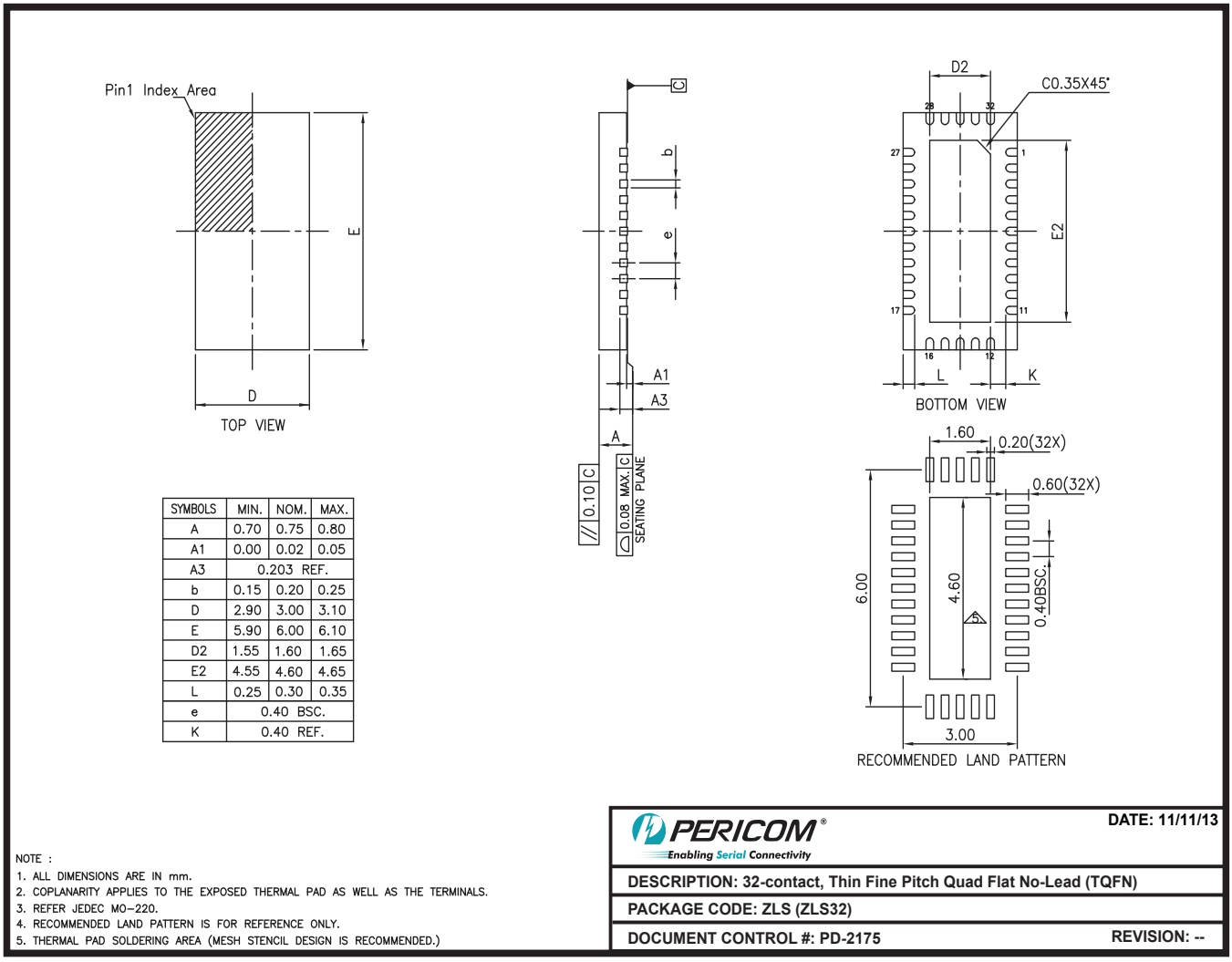
PI3VDP1431 Application Schematic



PI3VDP1431A Application Schematic



Packaging Mechanical: 32-Contact TQFN (ZLS)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	5.90	6.00	6.10
D2	1.55	1.60	1.65
E2	4.55	4.60	4.65
L	0.25	0.30	0.35
e		0.40 BSC.	
K		0.40 REF.	

NOTE :
1. ALL DIMENSIONS ARE IN mm.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED.)

PERICOM Enabling Serial Connectivity

DATE: 11/11/13

DESCRIPTION: 32-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZLS (ZLS32)

DOCUMENT CONTROL #: PD-2175 REVISION: --

Please check for the latest package information on the Pericom web site at www.pericom.com/support/packaging.

Ordering Information

Ordering Number	Package Code	Package Description
PI3VDP1431ZLSEX	ZLS	32-Contact, Thin Fine Pitch Quad Flat No Lead Package (TQFN) with DDC Switch
PI3VDP1431AZLSEX	ZLS	32-Contact, Thin Fine Pitch Quad Flat No Lead Package (TQFN) with DDC Buffer

Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

- E = Pb-free and Green
- X suffix = Tape/Reel

Related Products

Part Number	Product Description
PI3WVR12612	Wide Voltage Range DisplayPort™ & HDMI Video Switch
PI3HDX1204-B	HDMI2.0 Redriver and Displayport Level Shifter for 6Gbps Application
PI3EQXDP1201	Displayport 1.2 redriver with built-in auto test mode
PI3HDX414	1:4 Active 3.4Gbps HDMI1.4b Splitter/DeMux with Signal Conditioning
PI3HDX412BD	1:2 Active 3.4Gbps HDMI1.4b Splitter/DeMux with Signal Conditioning
PI3HDX621	2:1 Active 3.4Gbps HDMI 1.4b Switch
PI3HDMI336	3:1 Active 2.5Gbps HDMI Switch with I2C control and ARC Transmitter

Reference Information

Document	Description
HDMI1.4b	High-Definition Multimedia Interface Specification Version 1.4b, HDMI Licensing, LLC