User's Manual

16

78K0R/Kx3-L

User's Manual: Hardware

16-Bit Single-Chip Microcontrollers

Renesas Electronics
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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

Readers

This manual is intended for user engineers who wish to understand the functions of the 78K0R/Kx3-L and design and develop application systems and programs for these devices.
The target products are as follows.

- 78K0R/KC3-L: μPD78F1000, 78F1001, 78F1002, 78F1003
- 78K0R/KD3-L: μPD78F1004, 78F1005, 78F1006
- 78K0R/KE3-L: μPD78F1007, 78F1008, 78F1009
- 78K0R/KF3-L: μPD78F1010, 78F1011, 78F1012, 78F1027, 78F1028
- 78K0R/KG3-L: μPD78F1013, 78F1014, 78F1029, 78F1030

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The 78K0R/Kx3-L manual is separated into two parts: this manual and the instructions edition (common to the 78K0R Microcontroller).

78K0R/Kx3-L User's Manual (This Manual)	**78K0R Microcontroller User's Manual Instructions**
• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.
- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the RA78K0R, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0R.
- To know details of the 78K0R Microcontroller instructions:
  → Refer to the separate document **78K0R Microcontroller Instructions User's Manual (U17792E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
78K0R/Kx3-L User's Manual	This manual
78K0R Microcontroller Instructions User's Manual	U17792E
78K0R Microcontroller Self Programming Library Type02 User's Manual[Note]	U19193E

Note This document is classified under engineering management. Contact an Renesas Electronics sales representative.

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
CC78K0R Ver. 2.00 C Compiler	Operation	U18549E
	Language	U18548E
RA78K0R Ver. 1.20 Assembler Package	Operation	U18547E
	Language	U18546E
SM+ System Simulator	Operation	U18010E
PM+ Ver. 6.30		U18416E
ID78K0R-QB Ver. 3.20 Integrated Debugger	Operation	U17839E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
QB-MINI2 On-Chip Debug Emulator with Programming Function	U18371E
QB-78K0RIX3 In-Circuit Emulator (compatible with 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L)	U19228E
QB-78K0RKX3C In-Circuit Emulator (compatible with 78K0R/KF3-L and 78K0R/KG3-L (μPD78F1010, 78F1011, 78F1012, 78F1013, and 78F1014))	U19324E
QB-78F1030 In-Circuit Emulator (compatible with 78K0R/KF3-L and 78K0R/KG3-L (μPD78F1027, 78F1028, 78F1029, and 78F1030))	Under development

Documents Related to Flash Memory Programming

Document Name	Document No.
PG-FP5 Flash Memory Programmer User's Manual	R02UT0008E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Other Documents

Document Name	Document No.
RENESAS MICROCOMPUTER GENERAL CATALOG	R01CS0001E
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the “Semiconductor Device Mount Manual” website (http://www.renesas.com/prod/package/manual/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

CONTENTS

CHAPTER 1 OUTLINE

1.1 Features

- Minimum instruction execution time can be changed from high speed (0.05 μs: @ 20 MHz operation with high-speed system clock) to ultra low-speed (61 μs: @ 32.768 kHz operation with subsystem clock)
- General-purpose register: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM, RAM capacities

Flash ROM	RAM	78K0R/KC3-L			78K0R/KD3-L	78K0R/KE3-L	78K0R/KF3-L	78K0R/KG3-L
		40 pins	44 pins	48 pins	52 pins	64 pins	80 pins	100 pins
256 KB	12 KB[Note 1]	–			–	–	μPD78F1028	μPD78F1030
192 KB	10 KB	–			–	–	μPD78F1027	μPD78F1029
128 KB	8 KB[Note 2]	–			–	–	μPD78F1012	μPD78F1014
96 KB	6 KB	–			–	–	μPD78F1011	μPD78F1013
64 KB	4 KB	–			–	–	μPD78F1010	–
	3 KB[Note 3]	μPD78F1003			μPD78F1006	μPD78F1009	–	–
48 KB	2 KB	μPD78F1002			μPD78F1005	μPD78F1008	–	–
32 KB	1.5 KB	μPD78F1001			μPD78F1004	μPD78F1007	–	–
16 KB	1 KB	μPD78F1000		–	–	–	–	–

Notes 1. This is 11 KB when the self-programming function is used.
2. This is 7 KB when the self-programming function is used.
3. This is 2 KB when the self-programming function is used.

- On-chip internal high-speed oscillation clocks
  - 20 MHz Internal high-speed oscillation clock: 20 MHz (TYP.)
  - 8 MHz Internal high-speed oscillation clock: 8 MHz (TYP.)
  - 1 MHz Internal high-speed oscillation clock: 1 MHz (TYP.)
- On-chip single-power-supply flash memory (with prohibition of chip erase/block erase/writing function)
- Self-programming (with boot swap function/flash shield window function)
- On-chip debug function
- On-chip power-on-clear (POC) circuit and low-voltage detector (LVI)
- On-chip watchdog timer (operable with the dedicated internal low-speed oscillation clock)
- On-chip multiplier/divider (16 bits × 16 bits, 32 bits ÷ 32 bits)
- On-chip key interrupt function
- On-chip clock output/buzzer output controller[Note 1]
- On-chip BCD adjustment
- I/O ports: 33 to 89 (N-ch open drain: 2/4[Note 1])
- Timer: 10/14 channels
  - 16-bit timer: 8/12 channels
  - Watchdog timer: 1 channel
  - Real-time counter: 1 channel[Note 2]

Notes1. Those are not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.
2. This is not mounted onto 40-pin product of the 78K0R/KC3-L.

- On-chip comparator/programmable gain amplifier function [Note 1]
- Serial interface
  - CSI
  - UART/UART (LIN-bus supported)
  - I^2C [Note 2]/simplified I^2C
- 10-bit resolution A/D converter (AV_{REF} = 1.8 to 5.5 V): 10 to 16 channels
- Power supply voltage: V_{DD} = 1.8 to 5.5 V
- Operating ambient temperature: T_A = –40 to +85°C

Notes 1. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only.

2. This is not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L

Remark The pins mounted depend on the product. See **1.6 Block Diagram** and **1.7 Outline of Functions**.

1.2 Applications

- Audio visual equipment
- Home appliances
- Industrial equipment

1.3 Ordering Information

- **Flash memory version (lead-free product)**

78K0R/Kx3-L Microcontroller	Package	Part Number
78K0R/KC3-L	40-pin plastic WQFN (6 × 6)	μPD78F1000K8-4B4-AX[Note 1], 78F1001K8-4B4-AX[Note 1], 78F1002K8-4B4-AX[Note 1], 78F1003K8-4B4-AX[Note 1]
	44-pin plastic LQFP (10 × 10)	μPD78F1000GB-GAF-AX, 78F1001GB-GAF-AX, 78F1002GB-GAF-AX, 78F1003GB-GAF-AX
	48-pin plastic TQFP (fine pitch) (7 × 7)	μPD78F1001GA-HAA-AX, 78F1002GA-HAA-AX, 78F1003GA-HAA-AX
	48-pin plastic WQFN (7 × 7)	μPD78F1001K8-5B4-AX[Note 1], 78F1002K8-5B4-AX[Note 1], 78F1003K8-5B4-AX[Note 1]
78K0R/KD3-L	52-pin plastic LQFP (10 × 10)	μPD78F1004GB-GAG-AX, 78F1005GB-GAG-AX, 78F1006GB-GAG-AX
78K0R/KE3-L	64-pin plastic LQFP (12 × 12)	μPD78F1007GK-GAJ-AX, 78F1008GK-GAJ-AX, 78F1009GK-GAJ-AX
	64-pin plastic LQFP (fine pitch) (10 × 10)	μPD78F1007GB-GAH-AX, 78F1008GB-GAH-AX, 78F1009GB-GAH-AX
	64-pin plastic TQFP (fine pitch) (7 × 7)	μPD78F1007GA-HAB-AX, 78F1008GA-HAB-AX, 78F1009GA-HAB-AX
	64-pin plastic FBGA (5 × 5)	μPD78F1007F1-AN1-A, 78F1008F1-AN1-A, 78F1009F1-AN1-A
	64-pin plastic FBGA (4 × 4)	μPD78F1007F1-AA2-A, 78F1008F1- AA2-A, 78F1009F1- AA2-A
	64-pin plastic WQFN (9 × 9)	μPD78F1007K8-6B4-AX[Note 2], 78F1008K8- 6B4-AX[Note 2], 78F1009K8- 6B4-AX[Note 2]
78K0R/KF3-L	80-pin plastic LQFP (14 × 14)	μPD78F1010GC-GAD-AX, 78F1011GC-GAD-AX, 78F1012GC-GAD-AX, 78F1027GC-GAD-AX, 78F1028GC-GAD-AX
	80-pin plastic LQFP (fine pitch) (12 × 12)	μPD78F1010GK-GAK-AX, 78F1011GK-GAK-AX, 78F1012GK-GAK-AX, 78F1027GK-GAK-AX, 78F1028GK-GAK-AX
78K0R/KG3-L	100-pin plastic LQFP (14 × 20)	μPD78F1013GF-GAS-AX, 78F1014GF-GAS-AX, 78F1029GF-GAS-AX, 78F1030GF-GAS-AX
	100-pin plastic LQFP (fine pitch) (14 × 14)	μPD78F1013GC-UEU-AX, 78F1014GC-UEU-AX, 78F1029GC-UEU-AX, 78F1030GC-UEU-AX
	100-pin plastic FBGA (6 × 6)[Note 3]	μPD78F1013F1-BAK-A, 78F1014F1- BAK-A

Notes 1. Under development

2. Development cancellation

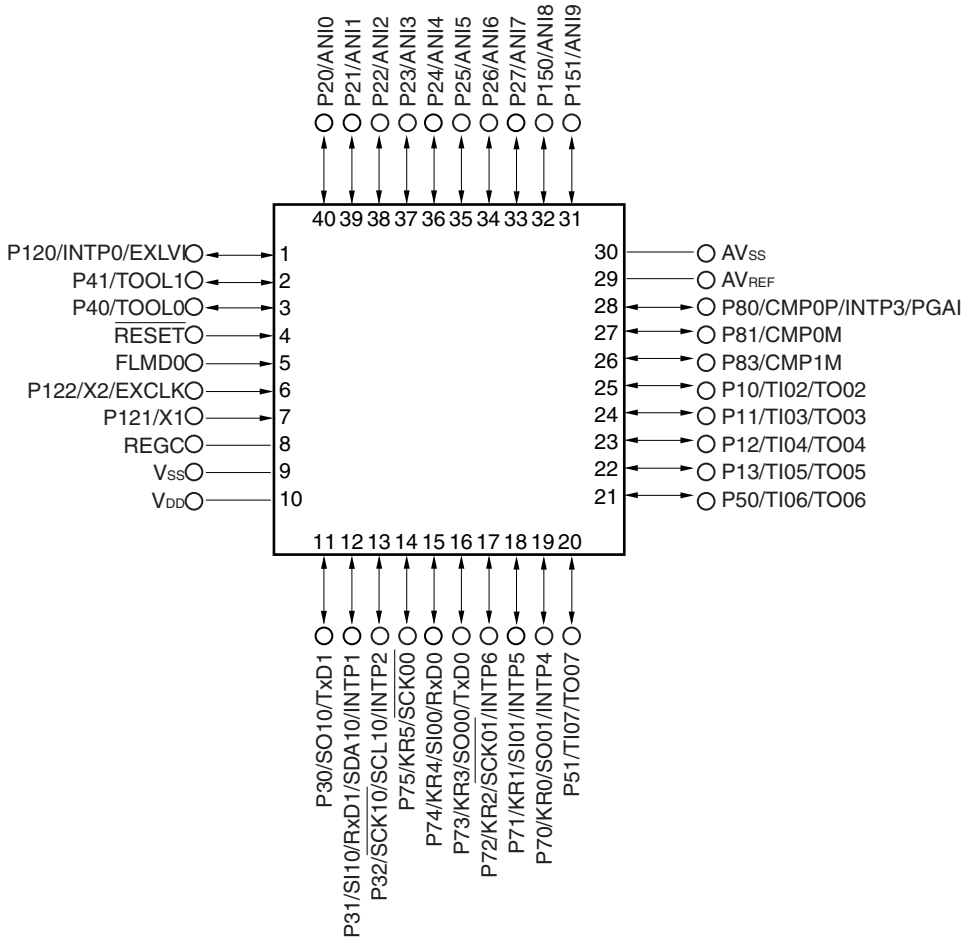
2. The μPD78F1029 and μPD78F1030 don't have the FBGA package.

Caution The 78K0R/Kx3-L has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

1.4 Pin Configuration (Top View)

1.4.1 78K0R/KC3-L

- 40-pin plastic WQFN (6 × 6) (Under development)



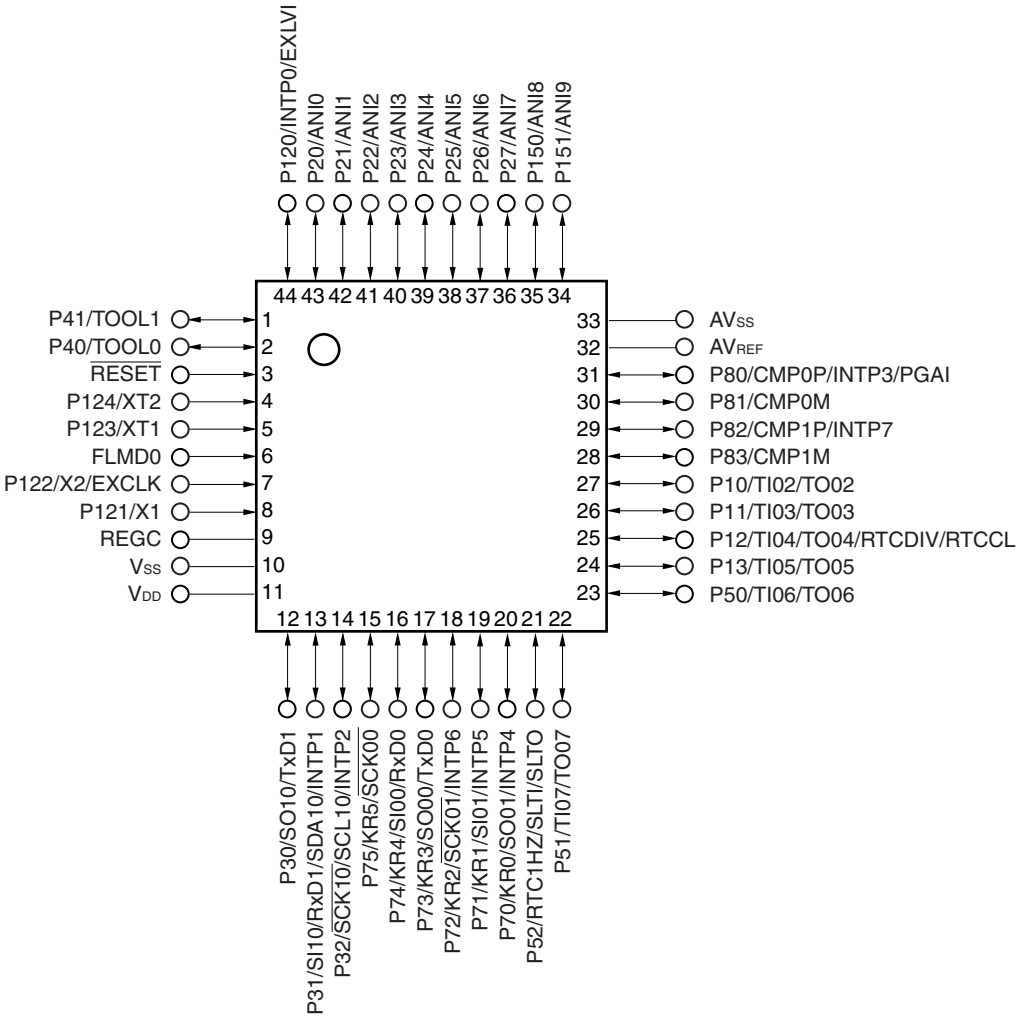
Cautions 1. Make AVSS the same potential as VSS.

2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

3. P20/ANI0 to P27/ANI7 and P151/ANI9 are set as analog inputs in the order of P151/ANI9, …, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P151/ANI9 as analog inputs, start designing from P151/ANI9 (see 13.3 (6) A/D port configuration register (ADPC) for details).

Remark For pin identification, see **1.5 Pin Identification**.

- 44-pin plastic LQFP (10 × 10)



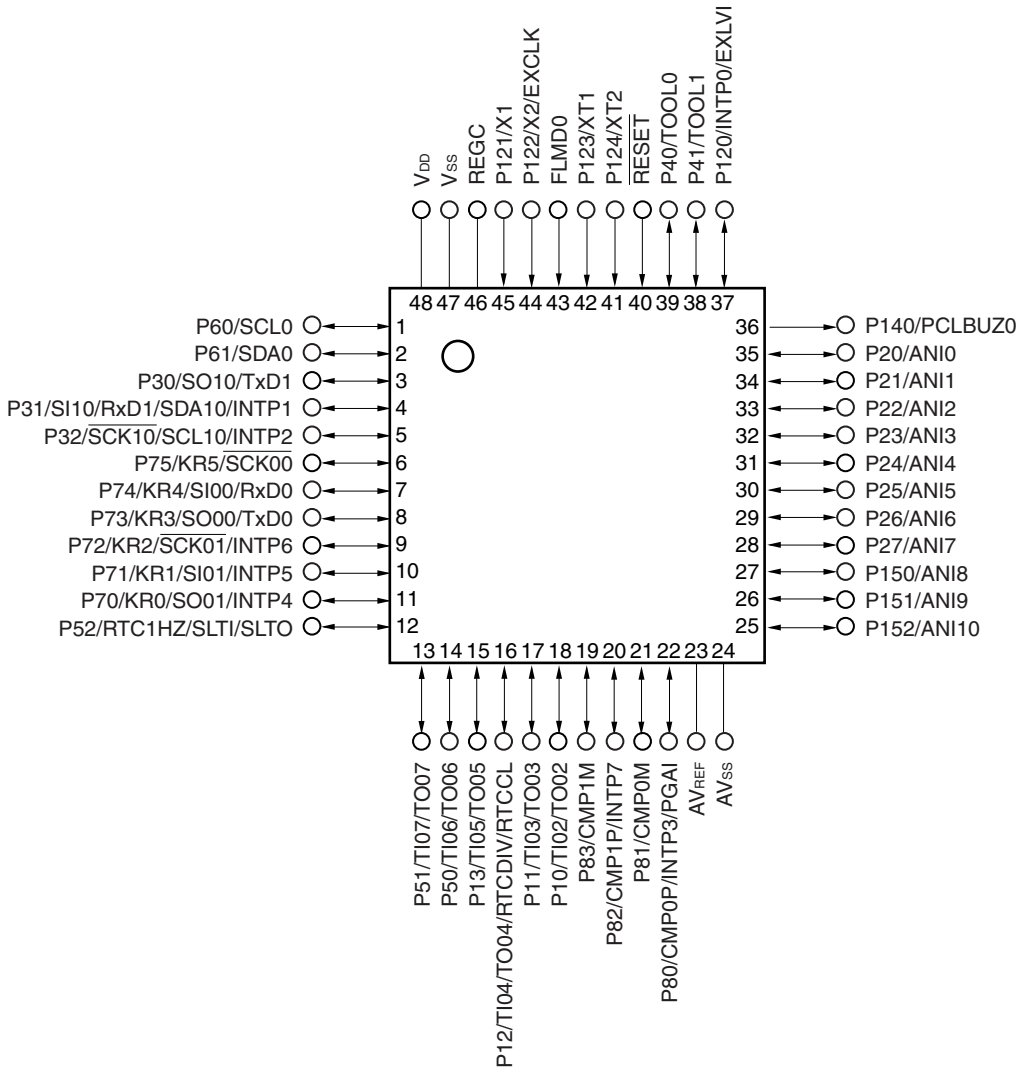
Cautions 1. Make AVSS the same potential as VSS.

2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

3. P20/ANI0 to P27/ANI7 and P151/ANI9 are set as analog inputs in the order of P151/ANI9, …, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P151/ANI9 as analog inputs, start designing from P151/ANI9 (see 13.3 (6) A/D port configuration register (ADPC) for details).

Remark For pin identification, see **1.5 Pin Identification**.

- 48-pin plastic TQFP (fine pitch) (7 × 7)
- 48-pin plastic WQFN (7 × 7) (Under development)



Cautions 1. Make AVSS the same potential as VSS.

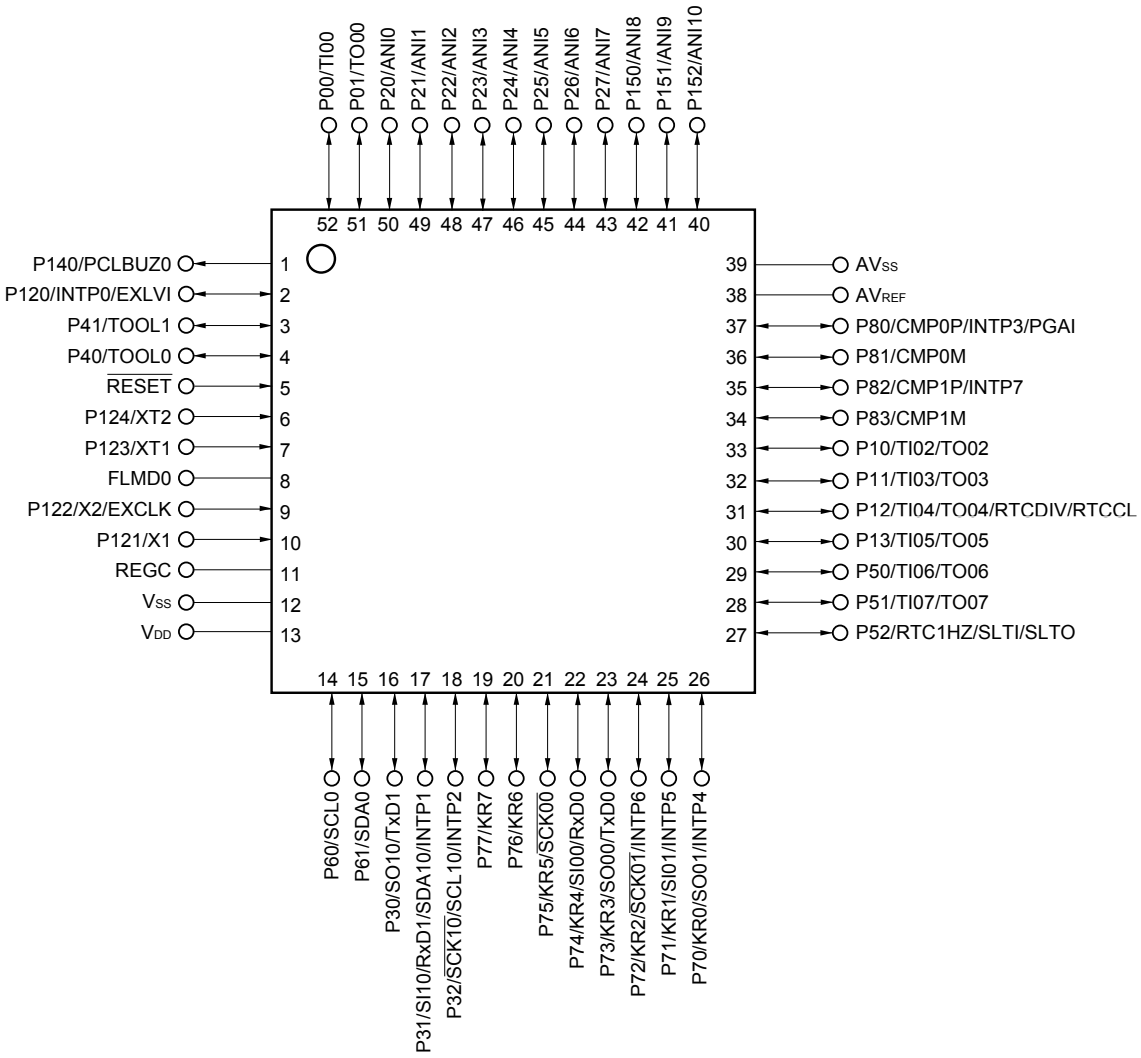
2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

3. P20/ANI0 to P27/ANI7 and P150/ANI8 to P152/ANI10 are set as analog inputs in the order of P152/ANI10, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P152/ANI10 as analog inputs, start designing from P152/ANI10 (see 13.3 (6) A/D port configuration register (ADPC) for details).

Remark For pin identification, see **1.5 Pin Identification**.

1.4.2 78K0R/KD3-L

- 52-pin plastic LQFP (10 × 10)



Cautions 1. Make AVSS the same potential as VSS.

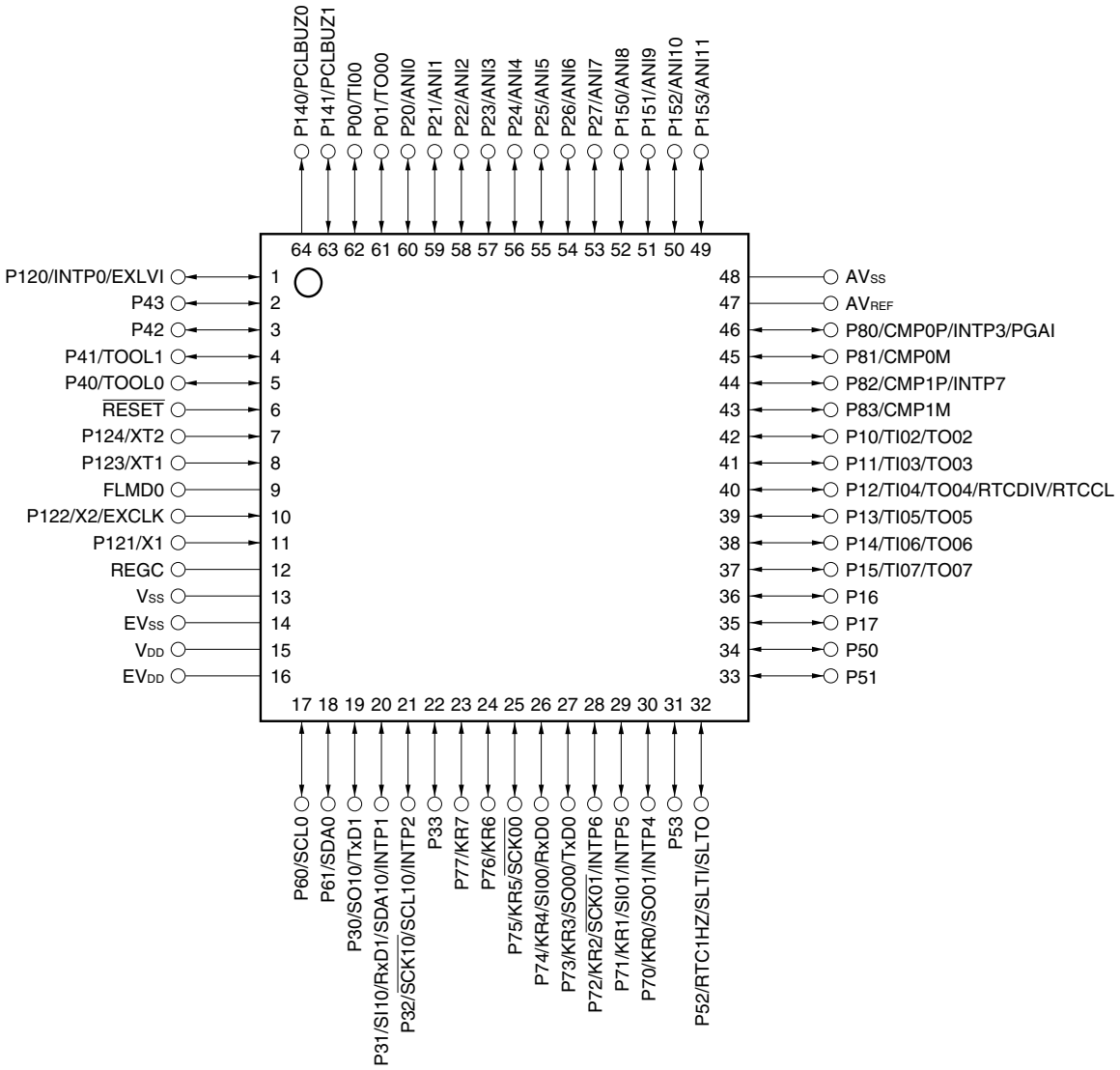
2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

3. P20/ANI0 to P27/ANI7 and P150/ANI8 to P152/ANI10 are set as analog inputs in the order of P152/ANI10, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P152/ANI10 as analog inputs, start designing from P152/ANI10 (see 13.3 (6) A/D port configuration register (ADPC) for details).

Remark For pin identification, see **1.5 Pin Identification**.

1.4.3 78K0R/KE3-L

- 64-pin plastic LQFP (12 × 12)
- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic TQFP (fine pitch) (7 × 7)



Cautions 1. Make AVSS and EVSS the same potential as VSS.

2. Make EVDD the same potential as VDD.

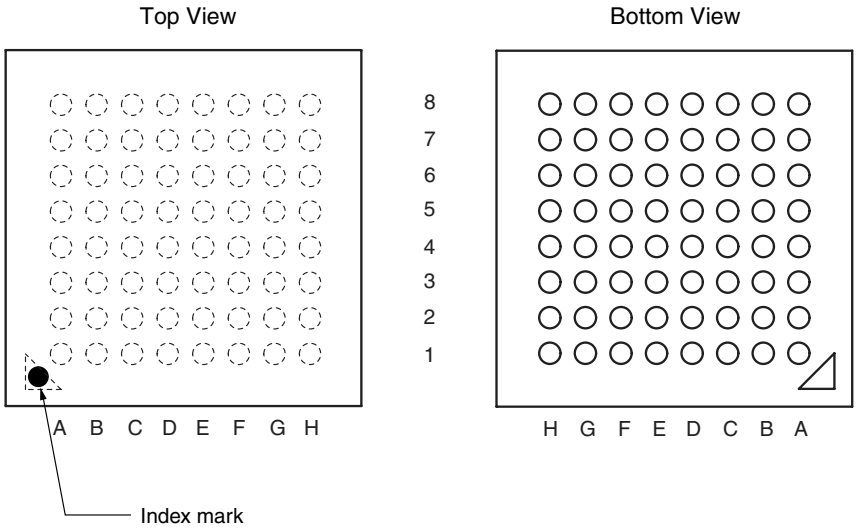
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

4. P20/ANI0 to P27/ANI7 and P150/ANI8 to P153/ANI11 are set as analog inputs in the order of P153/ANI11, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P153/ANI11 as analog inputs, start designing from P153/ANI11 (see 13.3 (6) A/D port configuration register (ADPC) for details).

Remarks 1. For pin identification, see **1.5 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD pins and connect the VSS and EVSS pins to separate ground lines.

- 64-pin plastic FBGA (5 × 5)
- 64-pin plastic FBGA (4 × 4)



Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P53	C1	P50	E1	P83/CMP1M	G1	AV_{REF}
A2	P52/RTC1HZ/SLTI /SLTO	C2	P71/KR1/SI01/INTP5	E2	P12/TI04/TO04 /RTCDIV/RTCCL	G2	P151/ANI9
A3	P72/KR2/$\overline{SCK01}$ /INTP6	C3	P74/KR4/SI00/RxD0	E3	P11/TI03/TO03	G3	P150/ANI8
A4	P75/KR5/$\overline{SCK00}$	C4	P17	E4	P10/TI02/TO02	G4	P26/ANI6
A5	P77/KR7	C5	P33	E5	P21/ANI1	G5	P23/ANI3
A6	P61/SDA0	C6	P31/SI10/RxD1 /SDA10/INTP1	E6	P41/TOOL1	G6	P20/ANI0
A7	P60/SCL0	C7	V_{SS}	E7	$\overline{RESET}$	G7	P00/TI00
A8	EV_{DD}	C8	P121/X1	E8	FLMD0	G8	P124/XT2
B1	P51	D1	P15/TI07/TO07	F1	P80/CMP0P /INTP3/PGAI	H1	AV_{SS}
B2	P70/KR0/SO01 /INTP4	D2	P14/TI06/TO06	F2	P81/CMP0M	H2	P153/ANI11
B3	P73/KR3/SO00/TxD0	D3	P13/TI05/TO05	F3	P82/CMP1P/INTP7	H3	P152/ANI10
B4	P76/KR6	D4	P16	F4	P25/ANI5	H4	P27/ANI7
B5	P32/$\overline{SCK10}$/SCL10 /INTP2	D5	P42	F5	P22/ANI2	H5	P24/ANI4
B6	P30/SO10/TxD1	D6	P40/TOOL0	F6	P43	H6	P141/PCLBUZ1
B7	V_{DD}	D7	REGC	F7	P01/TO00	H7	P140/PCLBUZ0
B8	EV_{SS}	D8	P122/X2/EXCLK	F8	P123/XT1	H8	P120/INTP0/EXLVI

Cautions 1. Make AV_{SS} and EV_{SS} the same potential as V_{SS}.

2. Make EV_{DD} the same potential as V_{DD}.

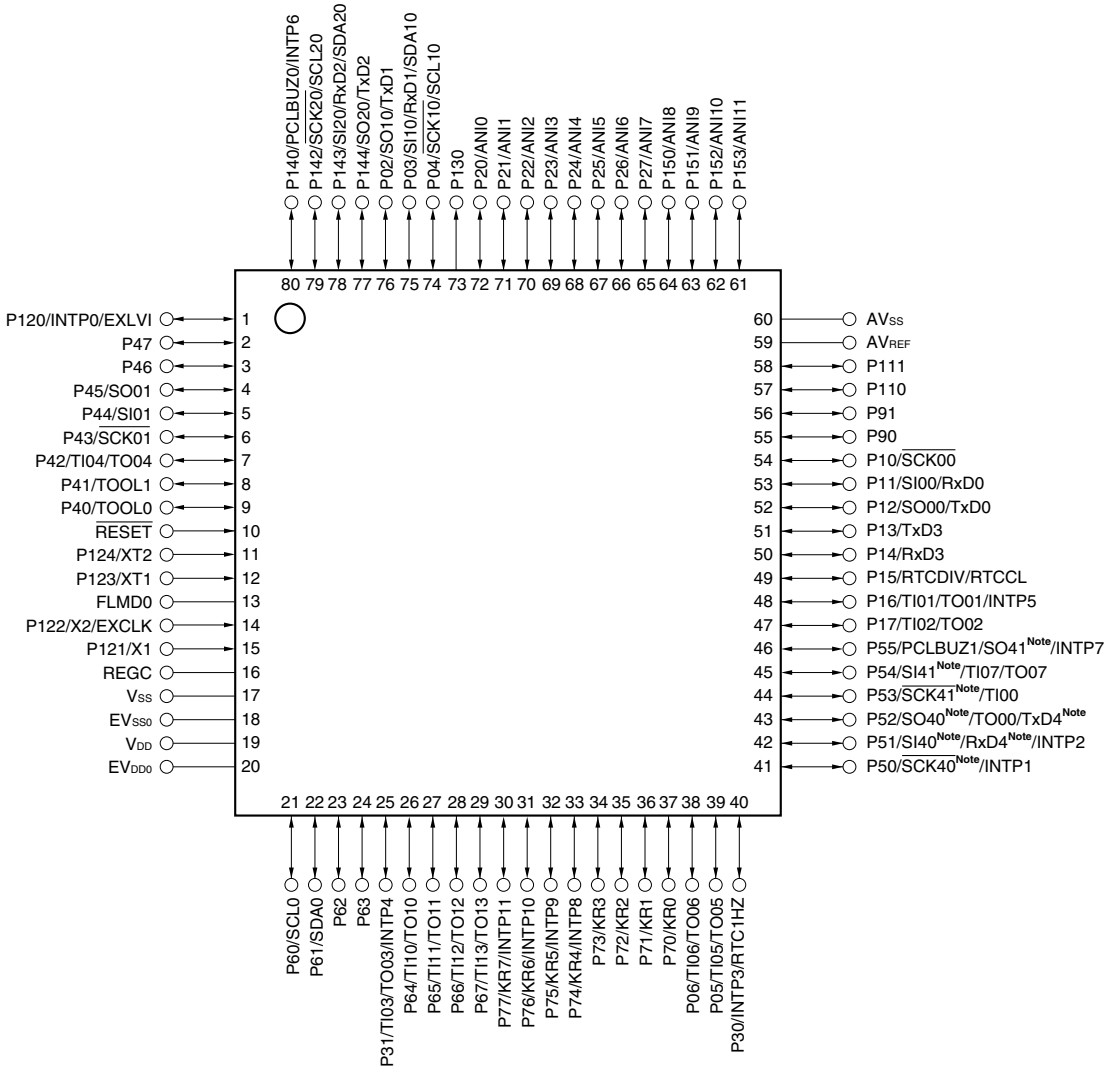
3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.5 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{SS} and EV_{SS} pins to separate ground lines.

1.4.4 78K0R/KF3-L

- 80-pin plastic LQFP (14 × 14)
- 80-pin plastic LQFP (fine pitch) (12 × 12)



Note $\overline{\text{SCK40}}$, $\overline{\text{SCK41}}$, SI40, SI41, SO40, SO41, TxD4, RxD4 pins are only mounted in the μPD78F1027 and 78F1028.

Cautions 1. Make AV_{SS} and EV_{SS0} the same potential as V_{SS}.

2. Make EV_{DD0} the same potential as V_{DD}.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF: target).

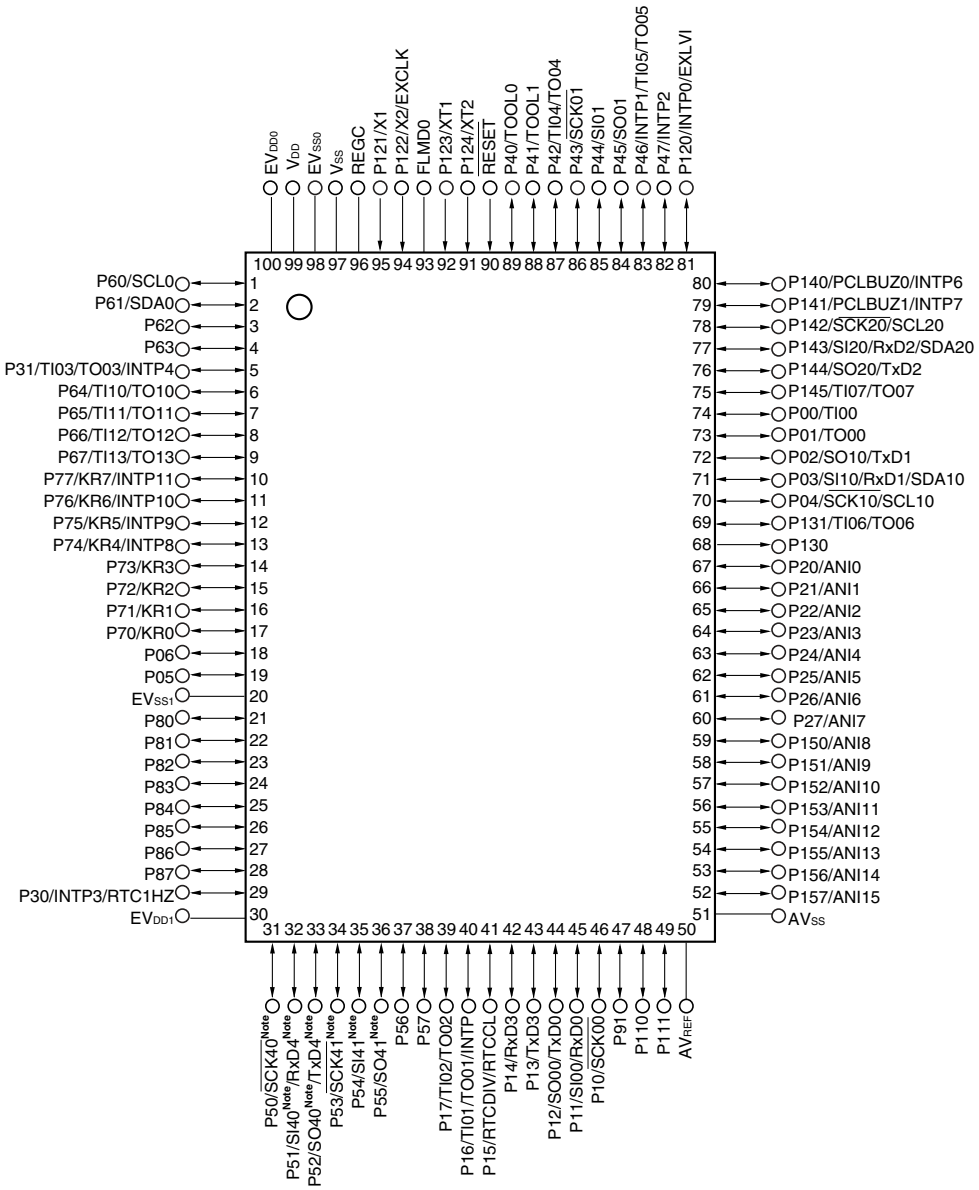
4. P20/ANI0 to P27/ANI7 and P150/ANI8 to P153/ANI11 are set as analog inputs in the order of P153/ANI11, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P153/ANI11 as analog inputs, start designing from P153/ANI11 (see 13.3 (6) A/D port configuration register (ADPC) for details).

Remarks 1. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

2. For pin identification, see **1.5 Pin Identification.**

1.4.5 78K0R/KG3-L

- 100-pin plastic LQFP (14 × 20)

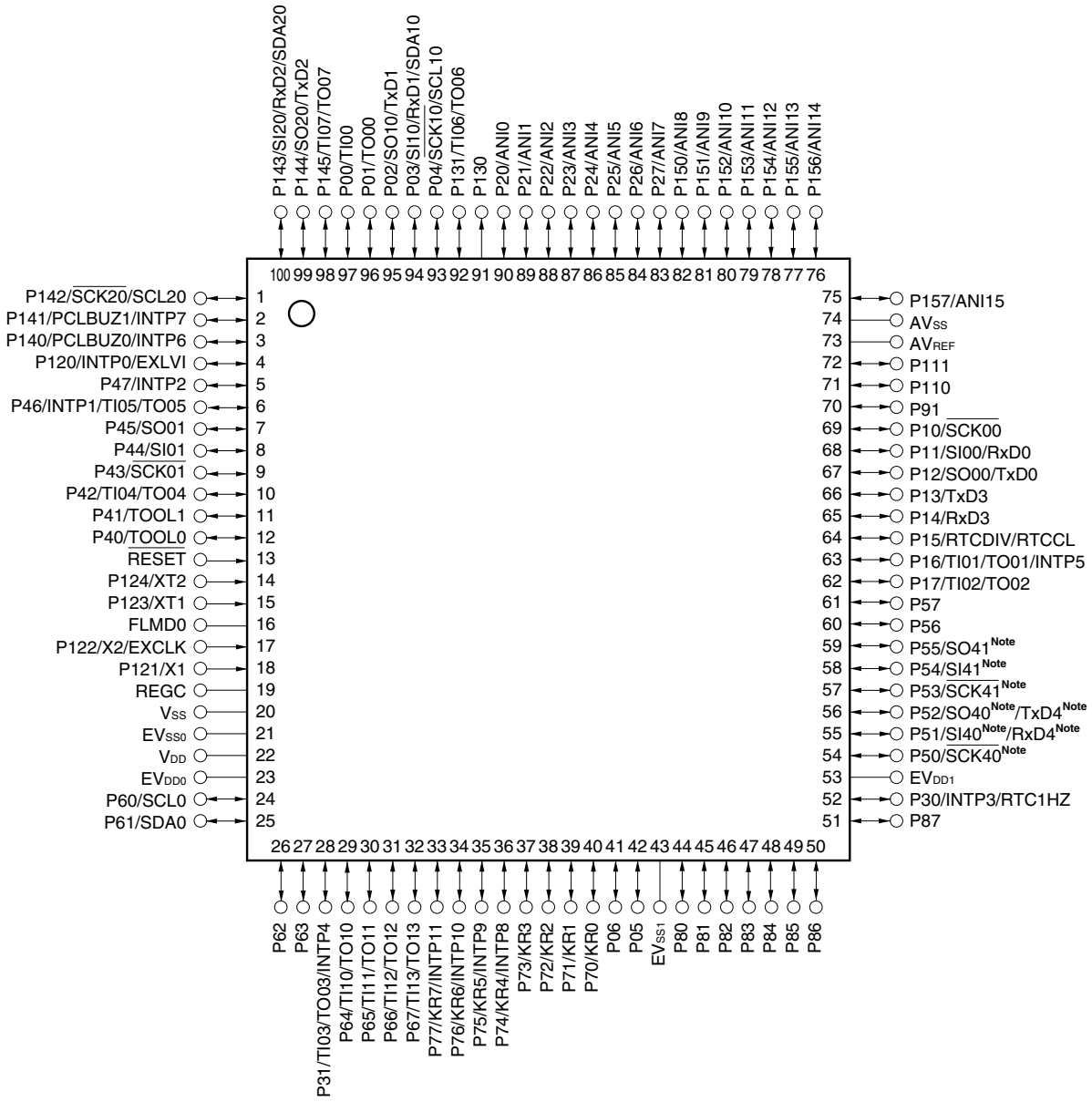


Note SCK40, SCK41, SI40, SI41, SO40, SO41, TxD4, RxD4 pins are only mounted in the μ PD78F1029 and 78F1030.

Cautions 1. Make AVSS, EVSS0, and EVSS1 the same potential as VSS.
2. Make EVDD0 and EVDD1 the same potential as VDD.
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF: target).
4. P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 are set as analog inputs in the order of P157/ANI15, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 as analog inputs, start designing from P157/ANI15 (see 13.3 (6) A/D port configuration register (ADPC) for details).

Remarks 1. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and two EVDD pins and connect the VSS and two EVSS pins to separate ground lines.
2. For pin identification, see **1.5 Pin Identification.**

- 100-pin plastic LQFP (fine pitch) (14 × 14)



Note SCK40, SCK41, SI40, SI41, SO40, SO41, TxD4, RxD4 pins are only mounted in the 48-pin products of the μPD78F1029 and 78F1030.

Cautions 1. Make AVSS, EVSS0, and EVSS1 the same potential as VSS.

2. Make EVDD0 and EVDD1 the same potential as VDD.

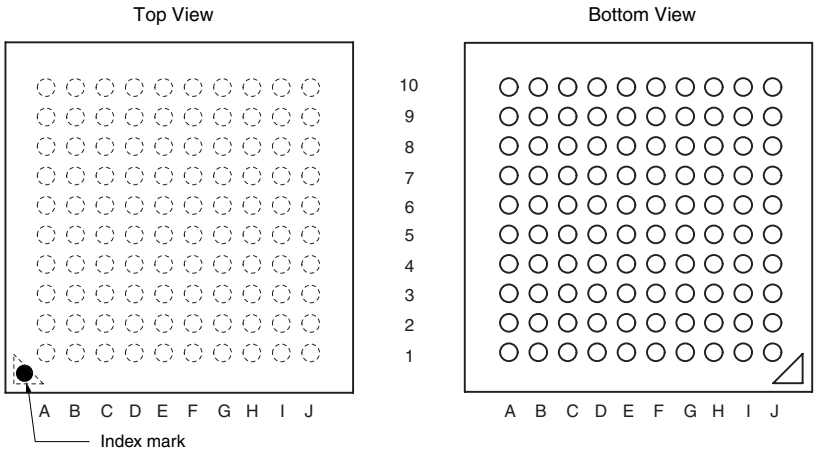
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF: target).

4. P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 are set as analog inputs in the order of P157/ANI15, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 as analog inputs, start designing from P157/ANI15 (see 13.3 (6) A/D port configuration register (ADPC) for details).

Remarks 1. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and two EVDD pins and connect the VSS and two EVSS pins to separate ground lines.

2. For pin identification, see **1.5 Pin Identification.**

- 100-pin plastic FBGA (6 × 6) [Note]



Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P86	C6	P72/KR2	F1	P15/RTCDIV/RTCCL	H6	P20/ANI0
A2	P84	C7	P75/KR5/INTP9	F2	P14/RxD3	H7	P00/TI00
A3	EV_{SS1}	C8	P77/KR7/INTP11	F3	P13/TxD3	H8	P142/$\overline{SCK20}$/SCL20
A4	P05	C9	V_{DD}	F4	P12/SO00/TxD0	H9	P42/TI04/TO04
A5	P63	C10	EV_{DD0}	F5	P11/SI00/RxD0	H10	P124/XT2
A6	P62	D1	P50	F6	P04/$\overline{SCK10}$/SCL10	J1	P156/ANI14
A7	P61/SDA0	D2	P51	F7	P44/SI01	J2	P157/ANI15
A8	P60/SCL0	D3	P52	F8	P45/SO01	J3	P152/ANI10
A9	P65/TI11/TO11	D4	P53	F9	FLMD0	J4	P27/ANI7
A10	P64/TI10/TO10	D5	P54	F10	V_{SS}	J5	P24/ANI4
B1	P87	D6	P73/KR3	G1	P130	J6	P21/ANI1
B2	P85	D7	P76/KR6/INTP10	G2	P91	J7	P01/TO00
B3	P83	D8	P40/TOOL0	G3	P110	J8	P144/SO20/TxD2
B4	P81	D9	EV_{SS0}	G4	P111	J9	P47/INTP2
B5	P06	D10	P121/X1	G5	P10/$\overline{SCK00}$	J10	P120/INTP0/EXLVI
B6	P71/KR1	E1	P55	G6	P03/SI10/RxD1/SDA10	K1	P155/ANI13
B7	P74/KR4/INTP8	E2	P56	G7	P02/SO10/TxD1	K2	P154/ANI12
B8	P67/TI13/TO13	E3	P57	G8	P46/TI05/TO05/INTP1	K3	P153/ANI11
B9	P66/TI12/TO12	E4	P17/TI02/TO02	G9	$\overline{RESET}$	K4	P150/ANI8
B10	P31/TI03/TO03/INTP4	E5	P16/TI01/TO01/INTP5	G10	P123/XT1	K5	P25/ANI5
C1	EV_{DD1}	E6	P13/TI06/TO06	H1	AV_{REF}	K6	P22/ANI2
C2	P30/RTC1HZ/INTP3	E7	P41/TOOL1	H2	AV_{SS}	K7	P145/TI07/TO07
C3	P82	E8	P43/$\overline{SCK01}$	H3	P151/ANI9	K8	P143/SI20/RxD2/SDA20
C4	P80	E9	REGC	H4	P26/ANI6	K9	P141/PCLBUZ1/INTP7
C5	P70/KR0	E10	P122/X2/EXCLK	H5	P23/ANI3	K10	P140/PCLBUZ0/INTP6

Note μPD78F1013 and μPD78F1014 only

Cautions 1. Make AV_{SS}, EV_{SS0}, and EV_{SS1} the same potential as V_{SS}.

2. Make EV_{DD0} and EV_{DD1} the same potential as V_{DD}.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF: target).

Remarks 1. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and two EV_{DD} pins and connect the V_{SS} and two EV_{SS} pins to separate ground lines.

2. For pin identification, see **1.5 Pin Identification.**

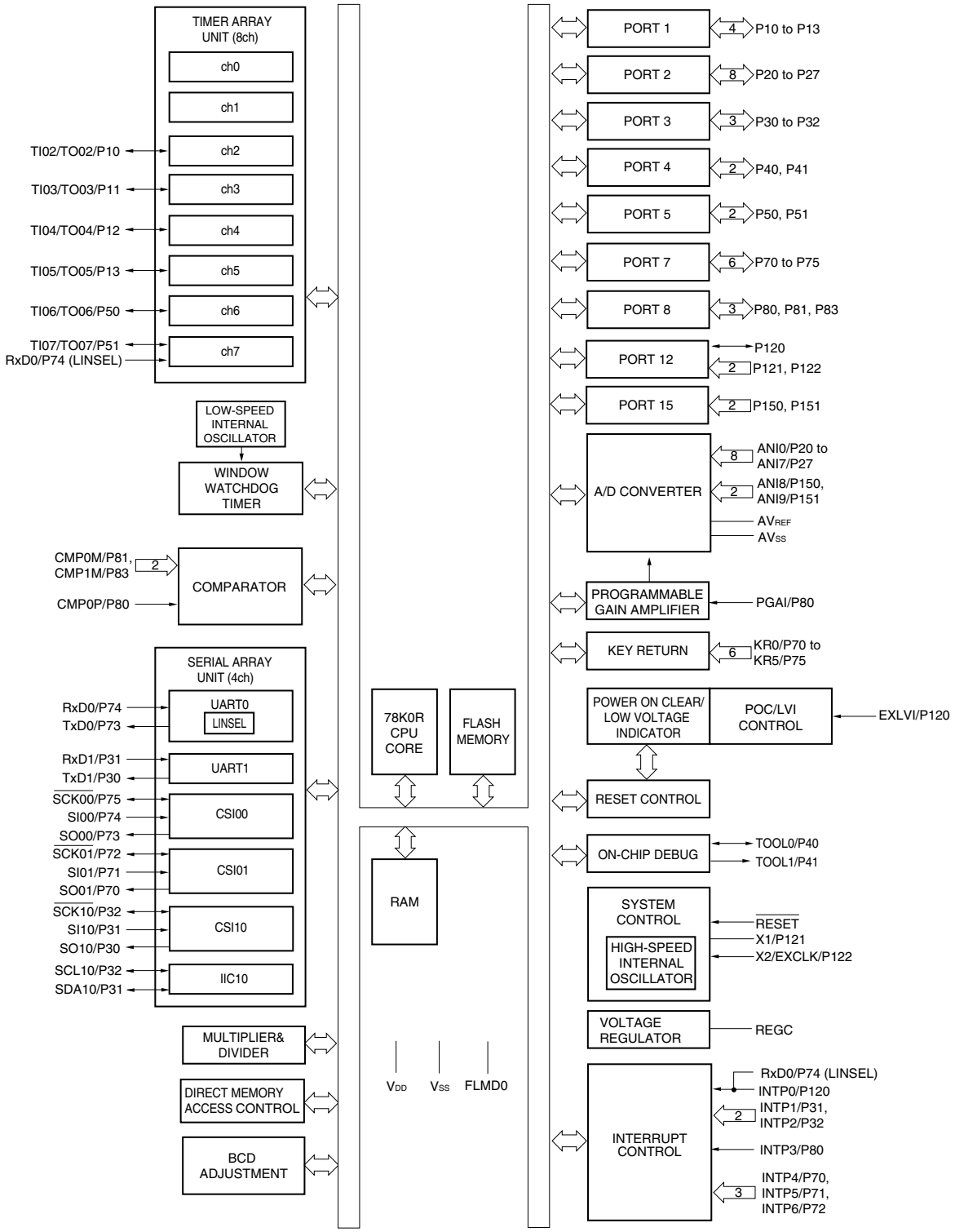
1.5 Pin Identification

ANI0-ANI15: Analog Input
AV_{REF}: Analog Reference Voltage
AV_{SS} : Analog Ground
CMP0M, CMP1M: Comparator Input (Minus)
CMP0P, CMP1P: Comparator Input (Plus)
EV_{DD}, EV_{DD0}, EV_{DD1}: Power Supply for Port
EV_{SS}, EV_{SS0}, EV_{SS1}: Ground for Port
EXCLK: External Clock Input (Main System Clock)
EXLVI: External Potential Input for Low-voltage Detector
FLMD0: Flash Programming Mode
INTP0 to INTP11: External Interrupt Input
KR0 to KR7: Key Return
P00 to P06: Port 0
P10 to P17: Port 1
P20 to P27: Port 2
P30 to P33: Port 3
P40 to P47: Port 4
P50 to P57: Port 5
P60 to P67: Port 6
P70 to P77: Port 7
P80 to P87: Port 8
P90, P91: Port 9
P110, P111: Port 11
P120 to P124: Port 12
P130, P131: Port 13
P140 to P145: Port 14
P150 to P157: Port 15
PCLBUZ0, PCLBUZ1: Programmable Clock Output/ Buzzer Output
PGAI: Programmable Gain Amplifier Input
REGC: Regulator Capacitance
$\overline{\text{RESET}}$: Reset
RTC1HZ: Real-time Counter Correction Clock (1 Hz) Output
RTCCL: Real-time Counter Clock (32 kHz Original Oscillation) Output
RTCDIV: Real-time Counter Clock (32 kHz Divided Frequency) Output
RxD0 to RxD4: Receive Data
$\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK10}}$, $\overline{\text{SCK20}}$, $\overline{\text{SCK40}}$, $\overline{\text{SCK41}}$: Serial Clock Input/Output
SCL0, SCL10, SCL20: Serial Clock Input/Output
SDA0, SDA10, SDA20: Serial Data Input/Output
SI00, SI01, SI10, SI20, SI40, SI41: Serial Data Input
SLTI: Selectable Timer Input
SLTO: Selectable Timer Output
SO00, SO01, SO10, SO20, SO40, SO41: Serial Data Output
TI00 to TI07, TI10 to TI13: Timer Input
TO00 to TO07, TO10 to TO13: Timer Output
TOOL0: Data Input/Output for Tool
TOOL1: Clock Output for Tool
TxD0 to TxD4: Transmit Data
V_{DD}: Power Supply
V_{SS}: Ground
X1, X2: Crystal Oscillator (Main System Clock)
XT1, XT2: Crystal Oscillator (Subsystem Clock)

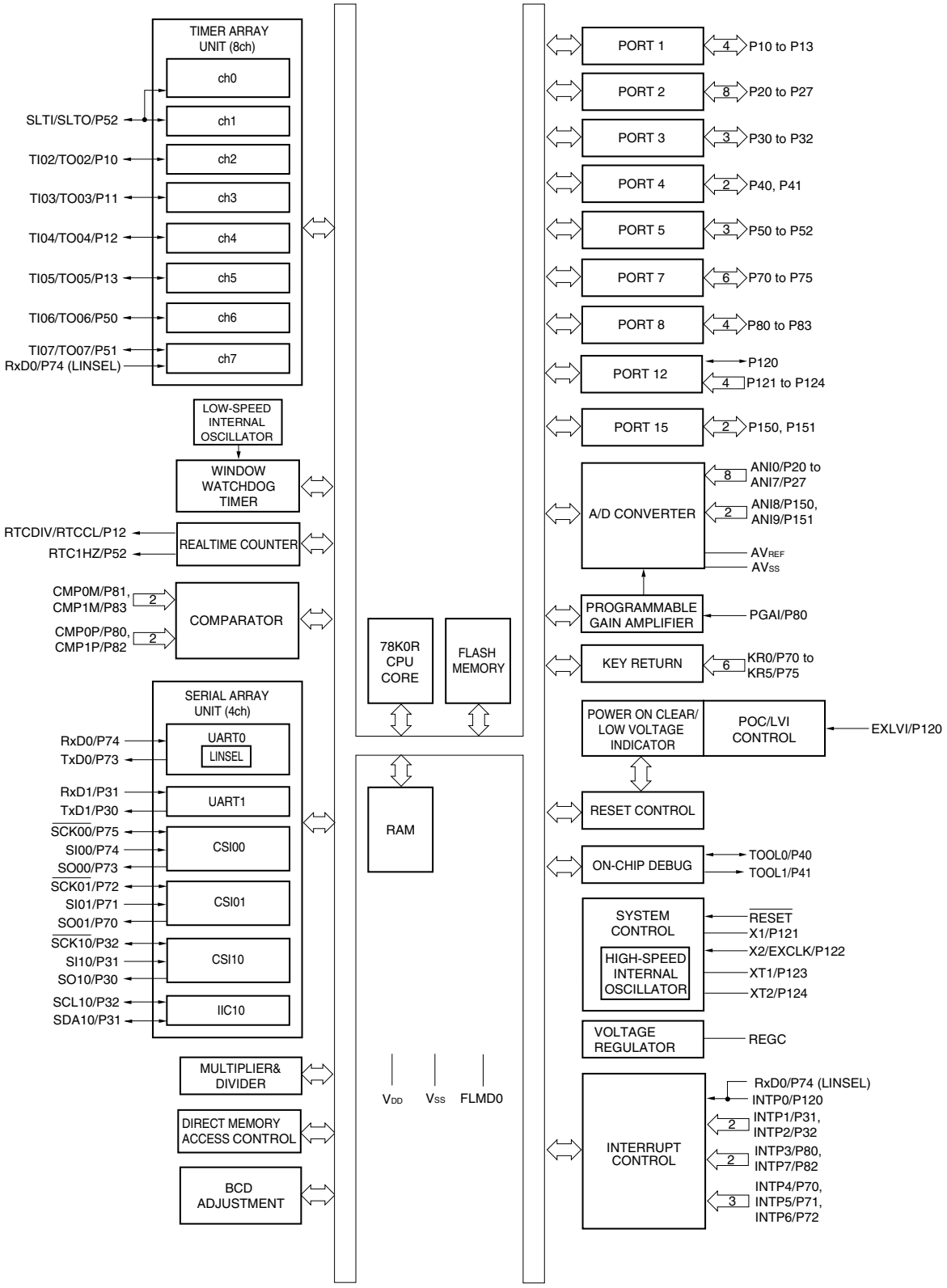
1.6 Block Diagram

1.6.1 78K0R/KC3-L

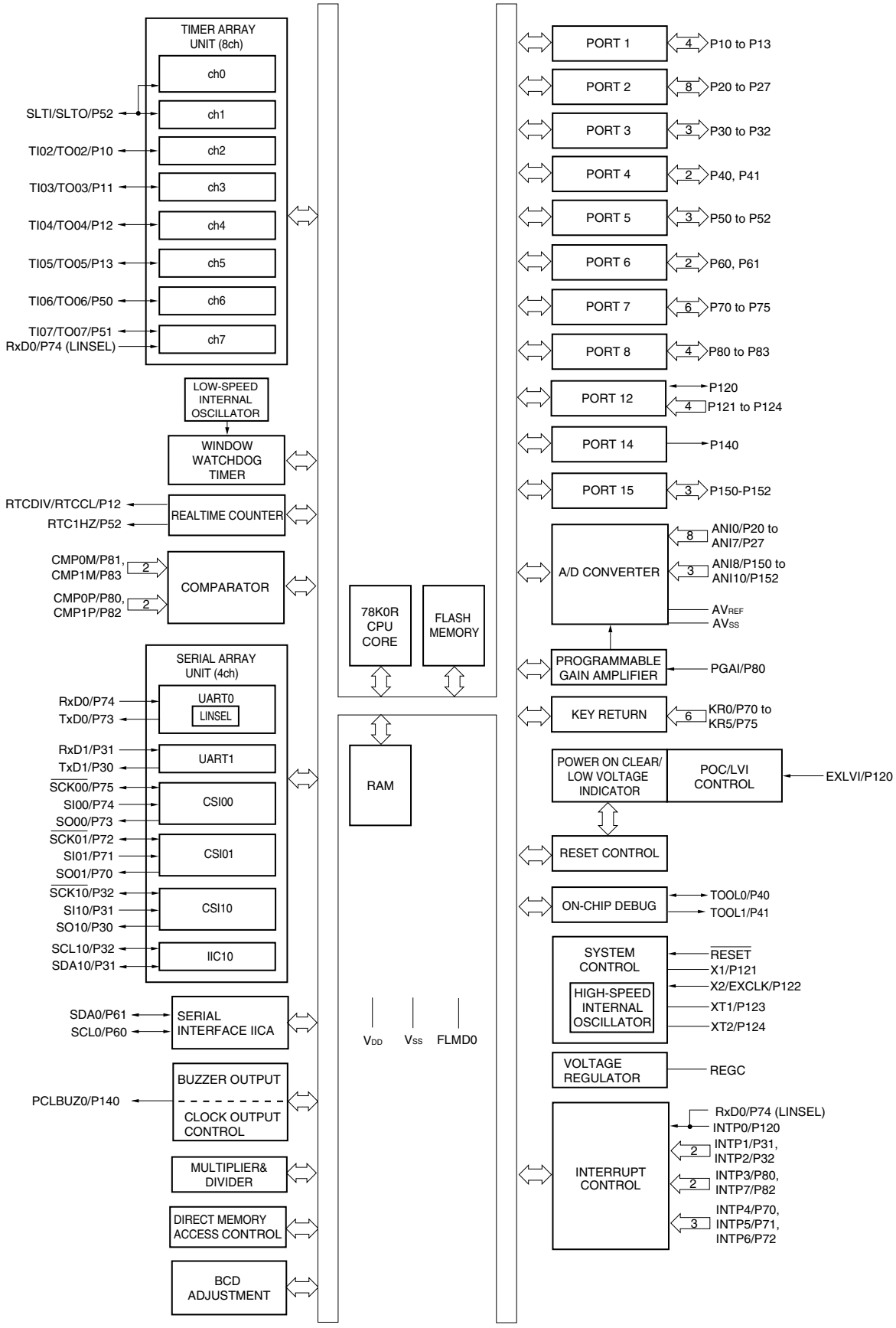
- 40-pin products



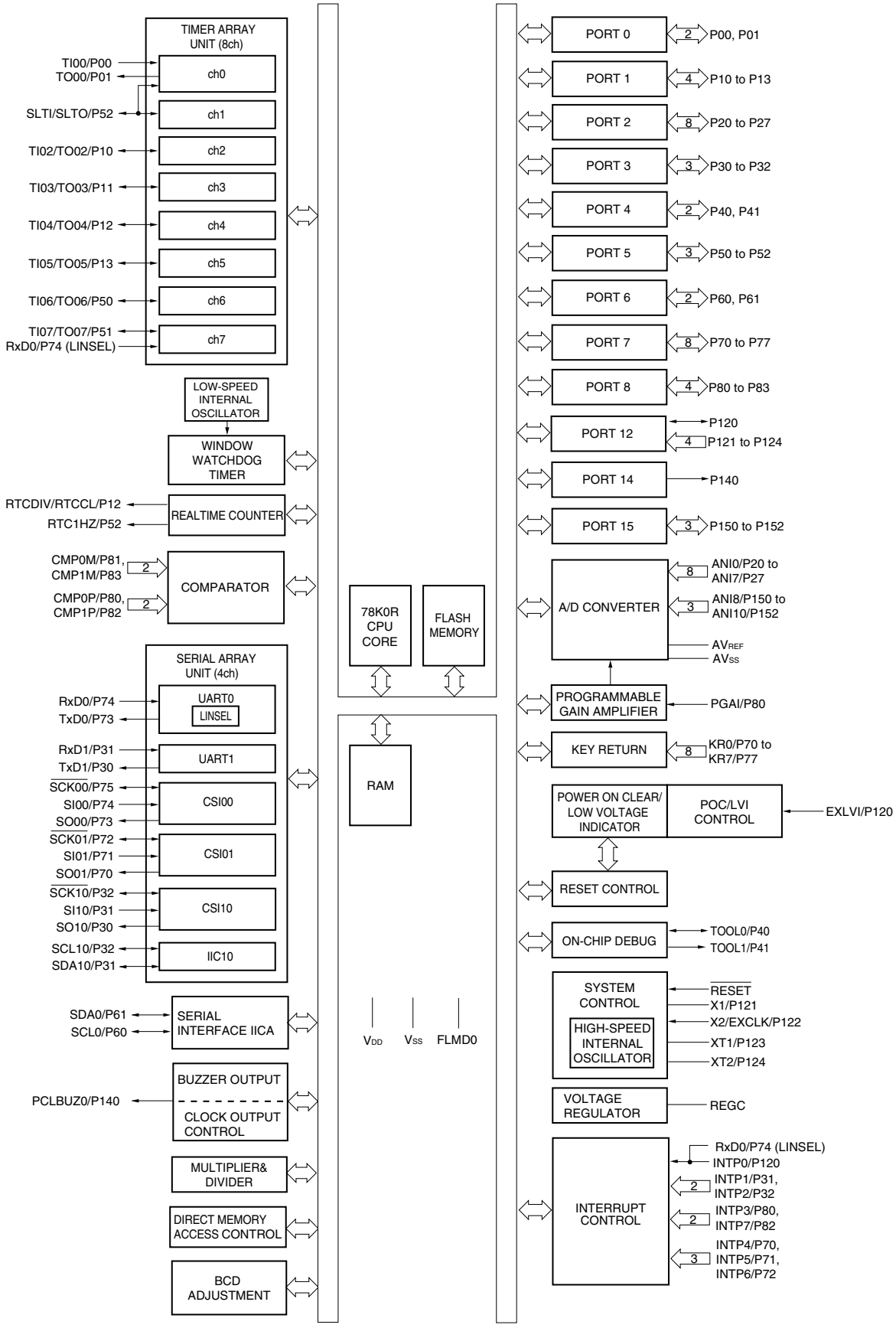
- 44-pin products



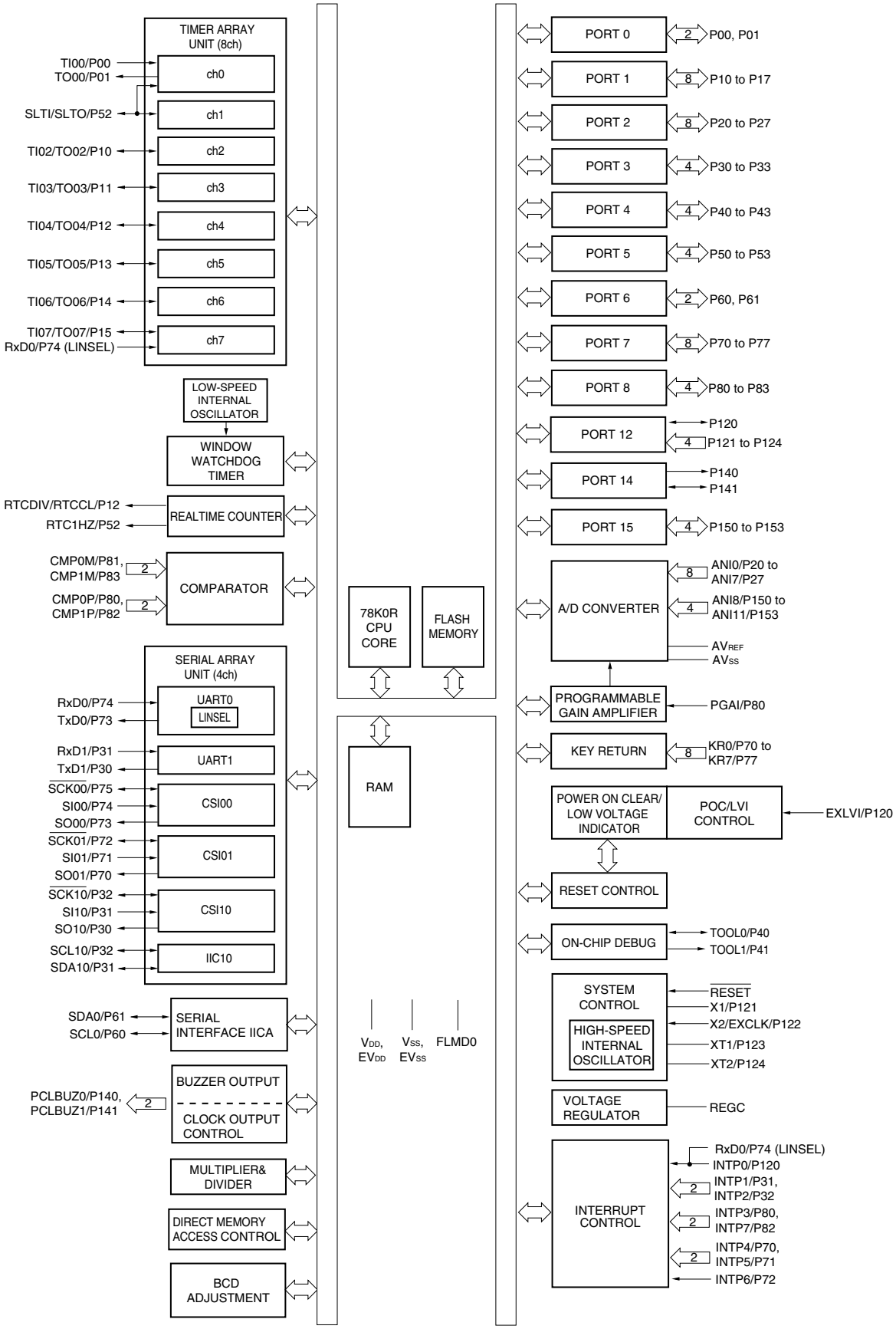
- 48-pin products



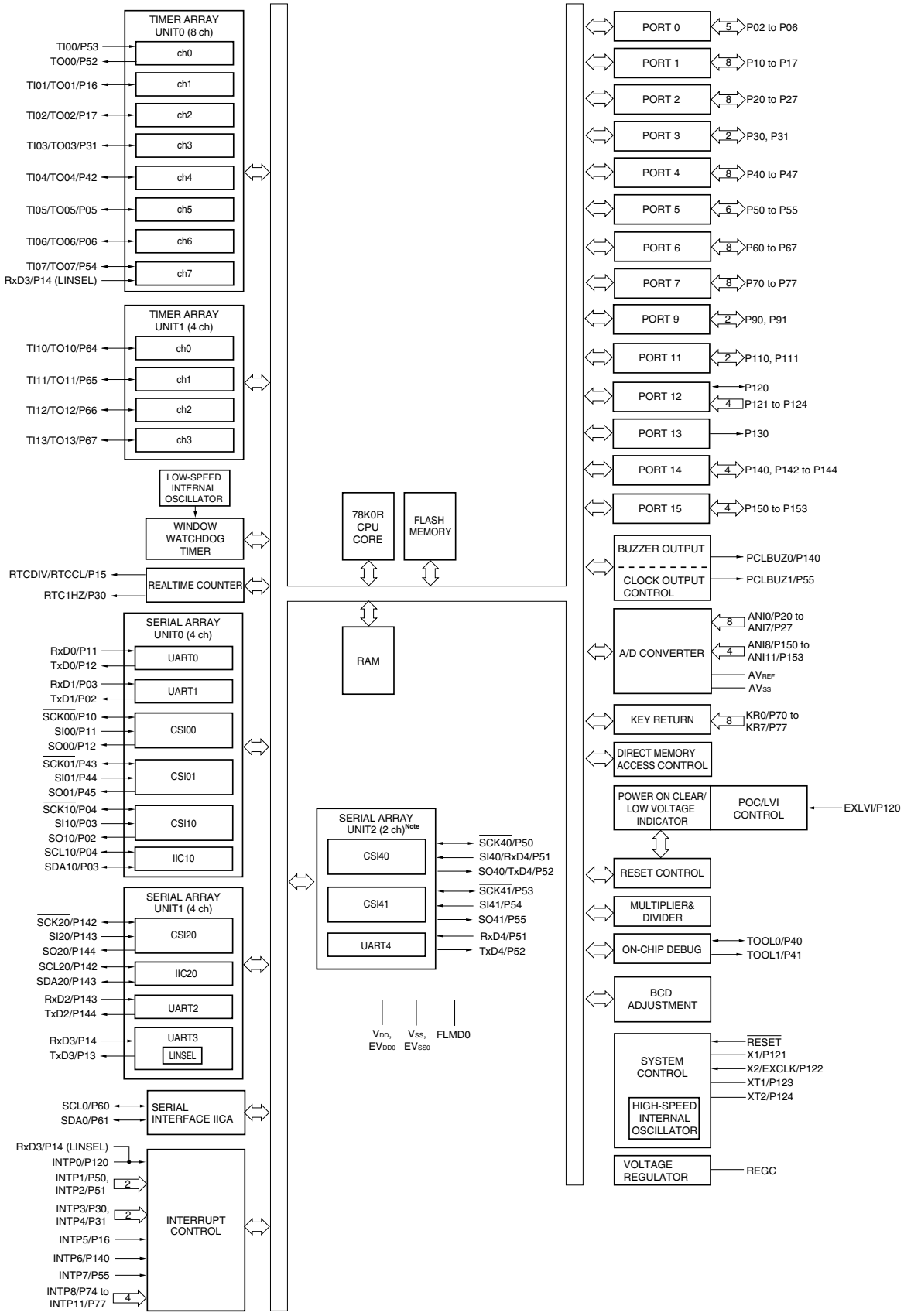
1.6.2 78K0R/KD3-L



1.6.3 78K0R/KE3-L

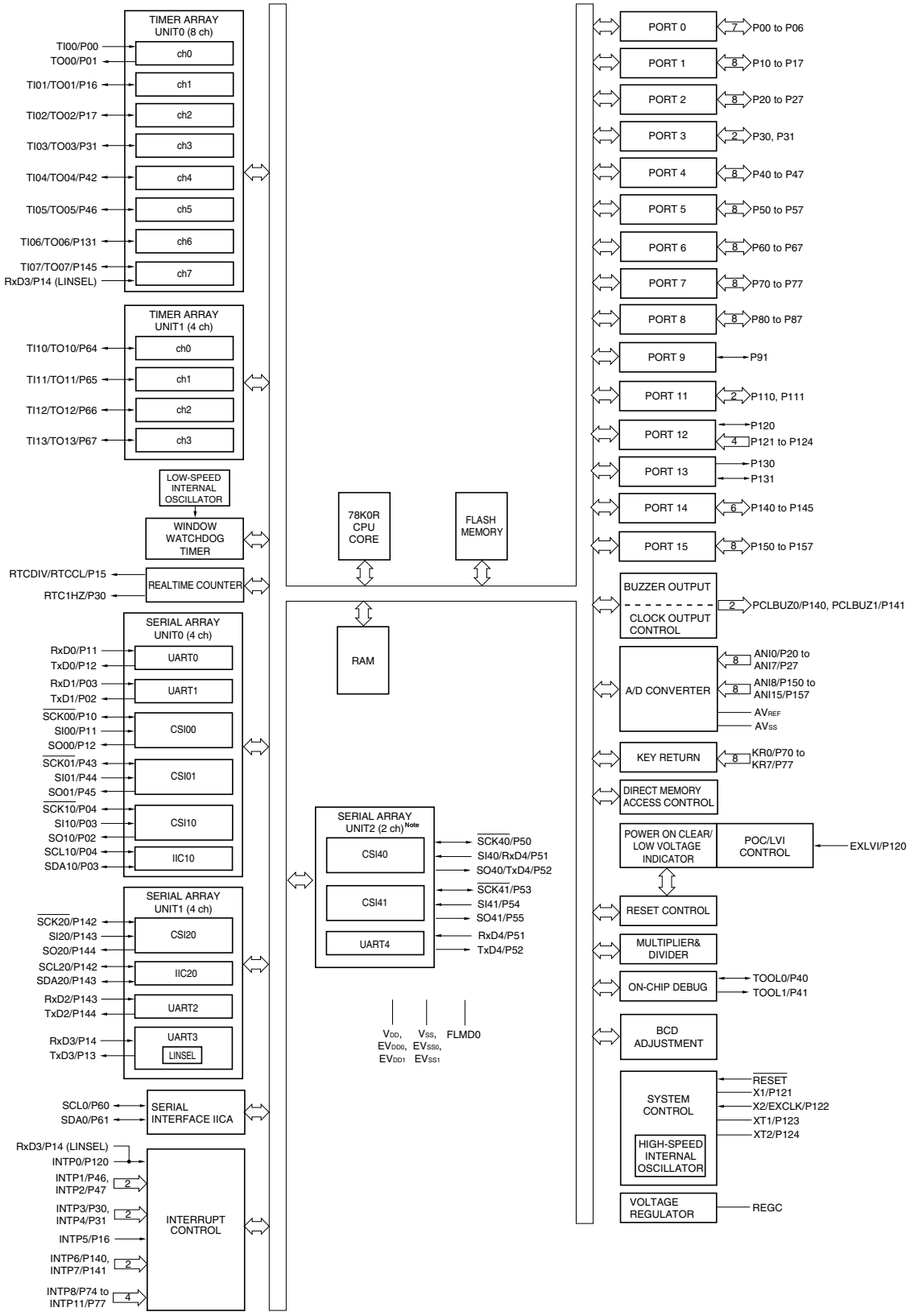


1.6.4 78K0R/KF3-L



Note Serial array unit 2 is only mounted in the μPD78F1027 and 78F1028.

1.6.5 78K0R/KG3-L



Note Serial array unit 2 is only mounted in the μPD78F1029 and 78F1030.

1.7 Outline of Functions

1. 7. 1 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L

(1/2)

Item		78K0R/KC3-L											78K0R/KD3-L			78K0R/KE3-L		
		40-pin				44-pin				48-pin								
		μPD78F1000	μPD78F1001	μPD78F1002	μPD78F1003	μPD78F1000	μPD78F1001	μPD78F1002	μPD78F1003	μPD78F1001	μPD78F1002	μPD78F1003	μPD78F1004	μPD78F1005	μPD78F1006	μPD78F1007	μPD78F1008	μPD78F1009
Internal memory	Flash memory (KB)	16	32	48	64	16	32	48	64	32	48	64	32	48	64	32	48	64
	RAM (KB)	1	1.5	2	3/2 Note 1	1	1.5	2	3/2 Note 1	1.5	2	3/2 Note 1	1.5	2	3/2 Note 1	1.5	2	3/2 Note 1
Memory space		1 MB																
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 2 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 2 to 5 MHz: V_{DD} = 1.8 to 5.5 V																
	Internal high-speed oscillation clock	Internal oscillation 1 MHz (TYP.), 8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V																
	20 MHz internal high-speed oscillation clock	Internal oscillation 20 MHz (TYP.): V_{DD} = 2.7 to 5.5 V																
Subsystem clock		–				XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V												
Internal low-speed oscillation clock (dedicated to WDT)		Internal oscillation 30 kHz (TYP.): V_{DD} = 1.8 to 5.5 V																
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)																
Minimum instruction execution time		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)																
		–				61 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)												
Instruction set		• 8-bit operation, 16-bit operation • Multiplication (8 bits × 8 bits) • Bit manipulation (Set, reset, test, and Boolean operation), etc.																
I/O port	Total	33				37				41			45			55		
	CMOS I/O	31				33				34			38			48		
	CMOS input	2				4				4			4			4		
	CMOS output	–				–				1			1			1		
	N-ch open-drain I/O (6 V tolerance)	–				–				2			2			2		
Timer	16-bit timer	8 channels																
	Watchdog timer	1 channel																
	Real-time counter (RTC)	–				1 channel												
	Timer output	6 (PWM outputs: 6 Note 2)				8 (PWM outputs: 7 Note 2)												
	RTC output	–				2 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz) • 512 Hz, 16.384 kHz, or 32.768 kHz (subsystem clock: f_{SUB} = 32.768 kHz)													

Notes 1. This is 2 KB when the self-programming function is used.

2. The number of outputs varies, depending on the setting.

(2/2)

Item	78K0R/KC3-L											78K0R/KD3-L			78K0R/KE3-L		
	40-pin				44-pin				48-pin								
	μPD78F1000	μPD78F1001	μPD78F1002	μPD78F1003	μPD78F1000	μPD78F1001	μPD78F1002	μPD78F1003	μPD78F1001	μPD78F1002	μPD78F1003	μPD78F1004	μPD78F1005	μPD78F1006	μPD78F1007	μPD78F1008	μPD78F1009
Clock output/buzzer output	–								1			1			2		
									• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (peripheral hardware clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)								
10-bit resolution A/D converter (AV_{REF} = 1.8 to 5.5 V)	10 channels								11 channels			11 channels			12 channels		
Comparators	2 channels (reference voltage: 12 combinations)																
Programmable gain amplifiers	1 channel (5 amplification factors)																
Serial interface	• CSI: 2 channels/UART (LIN-bus supported): 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel																
I^2C bus	–								1 channel			1 channel			1 channel		
Multiplier/divider	• 16 bits × 16 bits = 32 bits (multiplication) • 32 bits ÷ 32 bits = 32 bits (division)																
DMA controller	2 channels																
Vectored interrupt sources: Internal	22				24				25			25			25		
Vectored interrupt sources: External	8				9												
Key interrupt	6 channels (KR0 to KR5)								8 channels (KR0 to KR7)								
Reset	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by a reset processing check error																
Power-on-clear circuit	• Power-on-reset: 1.61 ±0.09 V • Power-down-reset: 1.59 ±0.09 V																
Low-voltage detector	1.91 V to 4.22 V (16 stages)																
On-chip debug function	Provided																
Power supply voltage	V_{DD} = 1.8 to 5.5 V																
Operating ambient temperature	T_A = –40 to +85 °C																

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

1. 7. 2 78K0R/KF3-L, 78K0R/KG3-L

(1/2)

Item		78K0R/KF3-L					78K0R/KG3-L			
		μPD78F1010	μPD78F1011	μPD78F1012	μPD78F1027	μPD78F1028	μPD78F1013	μPD78F1014	μPD78F1029 Note 4	μPD78F1030 Note 4
Internal memory	Flash memory (KB)	64	96	128	192	256	96	128	192	256
	RAM (KB)	4	6	8/7 Note 1	10	12/11 Note 2	6	8/7 Note 1	10	12/11 Note 2
Memory space		1 MB								
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 2 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 2 to 5 MHz: V_{DD} = 1.8 to 5.5 V								
	Internal high-speed oscillation clock	Internal oscillation 1 MHz (TYP.), 8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V								
	20 MHz internal high-speed oscillation clock	Internal oscillation 20 MHz (TYP.): V_{DD} = 2.7 to 5.5 V								
Subsystem clock		XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V								
Internal low-speed oscillation clock (dedicated to WDT)		Internal oscillation 30 kHz (TYP.): V_{DD} = 1.8 to 5.5 V								
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)								
Minimum instruction execution time		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)								
		61 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)								
Instruction set		• 8-bit operation, 16-bit operation • Multiplication (8 bits × 8 bits) • Bit manipulation (Set, reset, test, and Boolean operation), etc.								
I/O port	Total	71					89			
	CMOS I/O	62					80			
	CMOS input	4					4			
	CMOS output	1					1			
	N-ch open-drain I/O (6 V tolerance)	4					4			
Timer	16-bit timer	12 channels (unit 0: 8 channels, unit 1: 4 channels)								
	Watchdog timer	1 channel								
	Real-time counter (RTC)	1 channel								
	Timer output	12 channels (PWM outputs unit 0: 7, unit 1: 3 Note 3)								
	RTC output	2 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz) • 512 Hz, 16.384 kHz, or 32.768 kHz (subsystem clock: f_{SUB} = 32.768 kHz)								

Notes 1. This is 7 KB when the self-programming function is used.

2. This is 11 KB when the self-programming function is used.

3. The number of outputs varies, depending on the setting.

4. The μPD78F1029 and μPD78F1030 don't have the FBGA package.

(2/2)

Item		78K0R/KF3-L					78K0R/KG3-L			
		μPD78F1010	μPD78F1011	μPD78F1012	μPD78F1027	μPD78F1028	μPD78F1013	μPD78F1014	μPD78F1029 Note 1	μPD78F1030 Note 1
Clock output/buzzer output		2								
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (peripheral hardware clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)								
10-bit resolution A/D converter (AV_{REF} = 1.8 to 5.5 V)		12 channels					16 channels			
Comparators		–								
Programmable gain amplifiers		–								
Serial interface		• CSI: 2 channels/UART: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • UART supporting LIN-bus: 1 channel • CSI: 2 channels/UART: 1 channel (μPD78F1027, 78F1028, 78F1029, 78F1030)								
	I^2C bus	1 channel								
Multiplier/divider		• 16 bits × 16 bits = 32 bits (multiplication) • 32 bits ÷ 32 bits = 32 bits (division)								
DMA controller		2 channels								
Vectored interrupt sources	Internal	33			35		33			35
	External	13								
Key interrupt		8 channels (KR0 to KR7)								
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by a reset processing check error								
Power-on-clear circuit		• Power-on-reset: 1.61 ±0.09 V • Power-down-reset: 1.59 ±0.09 V								
Low-voltage detector		1.91 V to 4.22 V (16 stages)								
On-chip debug function		Provided								
Power supply voltage		V_{DD} = 1.8 to 5.5 V								
Operating ambient temperature		T_A = −40 to +85 °C								

Notes 1. The μPD78F1029 and μPD78F1030 don't have the FBGA package.

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

CHAPTER 2 PIN FUNCTIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

Caution For the functions of the pins in the 78K0R/KF3-L and 78K0R/KG3-L, see CHAPTER 3 PIN FUNCTIONS (78K0R/KF3-L and 78K0R/KG3-L).

2.1 Pin Function List

Pin I/O buffer power supplies depend on the product. The relationship between these power supplies and the pins is shown below.

Table 2-1. Pin I/O Buffer Power Supplies (AV_{REF}, V_{DD})

- 78K0R/KC3-L: 40-pin plastic WQFN (6x6) Note 1
  44-pin plastic LQFP (10x10)
  48-pin plastic TQFP (fine pitch) (7x7)
  48-pin plastic WQFN (7x7) Note 1
- 78K0R/KD3-L: 52-pin plastic LQFP (10x10)

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27, P150 to P152 Note 2, P80 to P83 Note 3
EV_{DD}	• Port pins other than P20 to P27, P150 to P152 Note 2, P80 to P83 Note 3 • Pins other than port pins

Notes 1. Under development
2. 40-pin and 44-pin products of the 78K0R/KC3-L do not have a P152 pin.
3. 40-pin product of the 78K0R/KC3-L does not have a P82 pin.

Table 2-2. Pin I/O Buffer Power Supplies (AV_{REF}, EV_{DD}, V_{DD})

- 78K0R/KE3-L: 64-pin plastic FBGA (5x5)
  64-pin plastic FBGA (4x4)
  64-pin plastic TQFP (fine pitch) (7x7)
  64-pin plastic LQFP (fine pitch) (10x10)
  64-pin plastic LQFP (12x12)

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27, P150 to P153, P80 to P83
EV_{DD}	• Port pins other than P20 to P27, P150 to P153, P80 to P83, and P121 to P124 • $\overline{\text{RESET}}$ pin and FLMD0 pin
V_{DD}	• P121 to P124 • Pins other than port pins (other than $\overline{\text{RESET}}$ pin and FLMD0 pin)

2.1.1 78K0R/KC3-L (40-pin products)

(1) Port functions (1/2): 78K0R/KC3-L (40-pin)

Function Name	I/O	Function	After Reset	Alternate Function
P10	I/O	Port 1. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI02/TO02
P11				TI03/TO03
P12				TI04/TO04
P13				TI05/TO05
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
P30	I/O	Port 3. 3-bit I/O port. Input of P31 and P32 can be set to TTL buffer. Output of P30 to P32 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SO10/TxD1
P31				SI10/RxD1/SDA10/INTP1
P32				$\overline{\text{SCK10}}$/SCL10/INTP2
P40[Note]	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P50	I/O	Port 5. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI06/TO06
P51				TI07/TO07
P70	I/O	Port 7. 6-bit I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
P71				KR1/SI01/INTP5
P72				KR2/$\overline{\text{SCK01}}$/INTP6
P73				KR3/SO00/TxD0
P74				KR4/SI00/RxD0
P75				KR5/$\overline{\text{SCK00}}$

Note If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally.

(1) Port functions (2/2): 78K0R/KC3-L (40-pin)

Function Name	I/O	Function	After Reset	Alternate Function
P80	I/O	Port 8. 3-bit I/O port. Inputs/output can be specified in 1-bit units. Inputs of P80, P81, and P83 can be set as comparator inputs or programmable gain amplifier inputs.	Analog input	CMP0P/INTP3/ PGAI
P81				CMP0M
P83				CMP1M
P120	I/O	Port 12. 1-bit I/O port and 2-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P150, P151	I/O	Port 15. 2-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8, ANI9

(2) Non-port functions (1/2): 78K0R/KC3-L (40-pin)

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANI8, ANI9	Input	A/D converter analog input	Digital input port	P150, P151
CMP0M	Input	Input voltage on the (–) side of comparator 0	Analog input	P81
CMP0P	Input	Input voltage on the (+) side of comparator 0		P80/INTP3/PGAI
CMP1M	Input	Input voltage on the (–) side of comparator 1		P83
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P31/SI10/RxD1/SDA10
INTP2				P32/$\overline{\text{SCK10}}$/SCL10
INTP3			Analog input	P80/CMP0P/PGAI
INTP4			Input port	P70/KR0/SO01
INTP5				P71/KR1/SI01
INTP6				P72/KR2/$\overline{\text{SCK01}}$
KR0	Input	Key interrupt input	Input port	P70/SO01/INTP4
KR1				P71/SI01/INTP5
KR2				P72/$\overline{\text{SCK01}}$/INTP6
KR3				P73/SO00/TxD0
KR4				P74/SI00/RxD0
KR5				P75/$\overline{\text{SCK00}}$
PGAI	Input	Programmable gain amplifier input	Analog input	P80/CMP0P/INTP3
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	–	–
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P74/KR4/SI00
RxD1		Serial data input to UART1		P31/SI10/SDA10/INTP1
$\overline{\text{SCK00}}$	I/O	Clock input/output for CSI00	Input port	P75/KR5
$\overline{\text{SCK01}}$		Clock input/output for CSI01		P72/KR2/INTP6
$\overline{\text{SCK10}}$		Clock input/output for CSI10		P32/SCL10/INTP2

(2) Non-port functions (2/2): 78K0R/KC3-L (40-pin)

Function Name	I/O	Function	After Reset	Alternate Function
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P32/$\overline{SCK10}$/INTP2
SDA10	I/O	Serial data I/O for simplified I^2C	Input port	P31/SI10/RxD1/ INTP1
SI00	Input	Serial data input to CSI00	Input port	P74/KR4/RxD0
SI01		Serial data input to CSI01		P71/KR1/INTP5
SI10		Serial data input to CSI10		P31/RxD1/SDA10/ INTP1
SO00	Output	Serial data output from CSI00	Input port	P73/KR3/TxD0
SO01		Serial data output from CSI01		P70/KR0/INTP4
SO10		Serial data output from CSI10		P30/TxD1
TI02	Input	External count clock input to 16-bit timer 02	Input port	P10/TO02
TI03		External count clock input to 16-bit timer 03		P11/TO03
TI04		External count clock input to 16-bit timer 04		P12/TO04
TI05		External count clock input to 16-bit timer 05		P13/TO05
TI06		External count clock input to 16-bit timer 06		P50/TO06
TI07		External count clock input to 16-bit timer 07		P51/TO07
TO02	Output	16-bit timer 02 output	Input port	P10/TI02
TO03		16-bit timer 03 output		P11/TI03
TO04		16-bit timer 04 output		P12/TI04
TO05		16-bit timer 05 output		P13/TI05
TO06		16-bit timer 06 output		P50/TI06
TO07		16-bit timer 07 output		P51/TI07
TxD0	Output	Serial data output from UART0	Input port	P73/KR3/SO00
TxD1		Serial data output from UART1		P30/SO10
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
EXCLK	Input	External clock input for main system clock	Input port	P122/X2
V_{DD}	–	Positive power supply (Port pins other than P20 to P27, P80, P81, P83, P150, P151, and other than ports)	–	–
AV_{REF}	–	• A/D converter and comparator reference voltage input • Positive power supply for P20 to P27, P80, P81, P83, P150, P151, A/D converter, programmable gain amplifier, and comparator	–	–
V_{SS}	–	Ground potential (Port pins other than P20 to P27, P80, P81, P83, P150, P151, and other than ports)	–	–
AV_{SS}	–	Ground potential for A/D converter, programmable gain amplifier, comparator, P20 to P27, P80, P81, P83, P150, P151	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

2.1.2 78K0R/KC3-L (44-pin and 48-pin products)

(1) Port functions (1/2): 78K0R/KC3-L (44-pin and 48-pin products)

Function Name	I/O	Function	After Reset	Alternate Function
P10	I/O	Port 1. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI02/TO02
P11				TI03/TO03
P12				TI04/TO04/ RTCDIV/RTCCL
P13				TI05/TO05
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
P30	I/O	Port 3. 3-bit I/O port. Input of P31 and P32 can be set to TTL buffer. Output of P30 to P32 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SO10/TxD1
P31				SI10/RxD1/SDA10/ INTP1
P32				$\overline{\text{SCK10}}$/SCL10/ INTP2
P40 Note 1	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P50	I/O	Port 5. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI06/TO06
P51				TI07/TO07
P52				RTC1HZ/SLTI/ SLTO
P60 Note 2	I/O	Port 6. 2-bit I/O port. Output of P60 and P61 is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0 Note 2
P61 Note 2				SDA0 Note 2
P70	I/O	Port 7. 6-bit I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
P71				KR1/SI01/INTP5
P72				KR2/$\overline{\text{SCK01}}$/INTP6
P73				KR3/SO00/TxD0
P74				KR4/SI00/RxD0
P75				KR5/$\overline{\text{SCK00}}$

Notes 1. If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally.

2. 48-pin products only.

(1) Port functions (2/2): 78K0R/KC3-L (44-pin and 48-pin products)

Function Name	I/O	Function	After Reset	Alternate Function
P80	I/O	Port 8. 4-bit I/O port. Inputs/output can be specified in 1-bit units. Inputs of P80 to P83 can be set as comparator inputs or programmable gain amplifier inputs.	Analog input	CMP0P/INTP3/ PGAI
P81				CMP0M
P82				CMP1P/INTP7
P83				CMP1M
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P140 Note	Output	Port 14. 1-bit output port.	Output port	PCLBUZ0 Note
P150, P151, P152 Note	I/O	Port 15. 3-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8, ANI9, ANI10 Note

Note 48-pin products only.

(2) Non-port functions (1/3): 78K0R/KC3-L (44-pin and 48-pin products)

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANI8, ANI9, ANI10 Note	Input			P150, P151, P152 Note
CMP0M	Input	Input voltage on the (–) side of comparator 0	Analog input	P81
CMP0P	Input	Input voltage on the (+) side of comparator 0		P80/INTP3/PGAI
CMP1M	Input	Input voltage on the (–) side of comparator 1		P83
CMP1P	Input	Input voltage on the (+) side of comparator 1		P82/INTP7
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P31/SI10/RxD1/SDA10
INTP2				P32/$\overline{\text{SCK10}}$/SCL10
INTP3			Analog input	P80/CMP0P/PGAI
INTP4			Input port	P70/KR0/SO01
INTP5				P71/KR1/SI01
INTP6				P72/KR2/$\overline{\text{SCK01}}$
INTP7			Analog input	P82/CMP1P
KR0	Input	Key interrupt input	Input port	P70/SO01/INTP4
KR1				P71/SI01/INTP5
KR2				P72/$\overline{\text{SCK01}}$/INTP6
KR3				P73/SO00/TxD0
KR4				P74/SI00/RxD0
KR5				P75/$\overline{\text{SCK00}}$
PCLBUZ0 Note	Output	Clock output/buzzer output	Output port	P140 Note
PGAI	Input	Programmable gain amplifier input	Analog input	P80/CMP0P/INTP3
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz division) output	Input port	P12/TI04/TO04/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P12/TI04/TO04/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P52/SLTI/SLTO
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P74/KR4/SI00
RxD1		Serial data input to UART1		P31/SI10/SDA10/INTP1
$\overline{\text{SCK00}}$	I/O	Clock input/output for CSI00	Input port	P75/KR5
$\overline{\text{SCK01}}$		Clock input/output for CSI01		P72/KR2/INTP6
$\overline{\text{SCK10}}$		Clock input/output for CSI10		P32/SCL10/INTP2

Note 48-pin products only.

(2) Non-port functions (2/3): 78K0R/KC3-L (44-pin and 48-pin products)

Function Name	I/O	Function	After Reset	Alternate Function
SCL0 Note	I/O	Clock input/output for I^2C	Input port	P60 Note
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P32/$\overline{SCK10}$/INTP2
SDA0 Note	I/O	Serial data I/O for I^2C	Input port	P61 Note
SDA10	I/O	Serial data I/O for simplified I^2C	Input port	P31/SI10/RxD1/ INTP1
SI00	Input	Serial data input to CSI00	Input port	P74/KR4/RxD0
SI01		Serial data input to CSI01		P71/KR1/INTP5
SI10		Serial data input to CSI10		P31/RxD1/SDA10/ INTP1
SLTI	Input	16-bit timer 00, 01 input	Input port	P52/RTC1HZ/SLTO
SLTO	Output	16-bit timer 00, 01 output	Input port	P52/RTC1HZ/SLTI
SO00	Output	Serial data output from CSI00	Input port	P73/KR3/TxD0
SO01		Serial data output from CSI01		P70/KR0/INTP4
SO10		Serial data output from CSI10		P30/TxD1
TI02	Input	External count clock input to 16-bit timer 02	Input port	P10/TO02
TI03		External count clock input to 16-bit timer 03		P11/TO03
TI04		External count clock input to 16-bit timer 04		P12/TO04/ RTCDIV/RTCCL
TI05		External count clock input to 16-bit timer 05		P13/TO05
TI06		External count clock input to 16-bit timer 06		P50/TO06
TI07		External count clock input to 16-bit timer 07		P51/TO07
TO02	Output	16-bit timer 02 output	Input port	P10/TI02
TO03		16-bit timer 03 output		P11/TI03
TO04		16-bit timer 04 output		P12/TI04/ RTCDIV/RTCCL
TO05		16-bit timer 05 output		P13/TI05
TO06		16-bit timer 06 output		P50/TI06
TO07		16-bit timer 07 output		P51/TI07
TxD0	Output	Serial data output from UART0	Input port	P73/KR3/SO00
TxD1		Serial data output from UART1		P30/SO10
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124
EXCLK	Input	External clock input for main system clock	Input port	P122/X2
V_{DD}	–	Positive power supply (Port pins other than P20 to P27, P80 to P83, P150, P151, P152 Note, and other than ports)	–	–
AV_{REF}	–	• A/D converter and comparator reference voltage input • Positive power supply for P20 to P27, P150, P151, P152 Note, P80 to P83, A/D converter, programmable gain amplifier, and comparator	–	–
V_{SS}	–	Ground potential (Port pins other than P20 to P27, P80 to P83, P150, P151, P152 Note, and other than ports)	–	–

Note 48-pin products only.

(2) Non-port functions (3/3): 78K0R/KC3-L (44-pin and 48-pin products)

Function Name	I/O	Function	After Reset	Alternate Function
AV_{SS}	–	Ground potential for A/D converter, programmable gain amplifier, comparator, P20 to P27, P150, P151, P152 Note and P80 to P83	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

Note 48-pin products only.

2.1.3 78K0R/KD3-L

(1) Port functions (1/2): 78K0R/KD3-L

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI00
P01				TO00
P10	I/O	Port 1. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI02/TO02
P11				TI03/TO03
P12				TI04/TO04/ RTCDIV/RTCCL
P13				TI05/TO05
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
P30	I/O	Port 3. 3-bit I/O port. Input of P31 and P32 can be set to TTL buffer. Output of P30 to P32 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SO10/TxD1
P31				SI10/RxD1/SDA10/ INTP1
P32				$\overline{\text{SCK10}}$/SCL10/ INTP2
P40[Note]	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P50	I/O	Port 5. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI06/TO06
P51				TI07/TO07
P52				RTC1HZ/SLTI/ SLTO
P60	I/O	Port 6. 2-bit I/O port. Output of P60 and P61 is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0

Note If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally.

(1) Port functions (2/2): 78K0R/KD3-L

Function Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7. 8-bit I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
P71				KR1/SI01/INTP5
P72				KR2/$\overline{\text{SCK01}}$/INTP6
P73				KR3/SO00/TxD0
P74				KR4/SI00/RxD0
P75				KR5/$\overline{\text{SCK00}}$
P76				KR6
P77				KR7
P80	I/O	Port 8. 4-bit I/O port. Inputs/output can be specified in 1-bit units. Inputs of P80 to P83 can be set as comparator inputs or programmable gain amplifier inputs.	Analog input	CMP0P/INTP3/ PGAI
P81				CMP0M
P82				CMP1P/INTP7
P83				CMP1M
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P140	Output	Port 14. 1-bit output port.	Output port	PCLBUZ0
P150 to P152	I/O	Port 15. 3-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8 to ANI10

(2) Non-port functions (1/3): 78K0R/KD3-L

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANI8 to ANI10	Input			P150 to P152
CMP0M	Input	Input voltage on the (–) side of comparator 0	Analog input	P81
CMP0P	Input	Input voltage on the (+) side of comparator 0		P80/INTP3/PGAI
CMP1M	Input	Input voltage on the (–) side of comparator 1		P83
CMP1P	Input	Input voltage on the (+) side of comparator 1		P82/INTP7
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P31/SI10/RxD1/SDA10
INTP2				P32/$\overline{\text{SCK10}}$/SCL10
INTP3			Analog input	P80/CMP0P/PGAI
INTP4			Input port	P70/KR0/SO01
INTP5				P71/KR1/SI01
INTP6				P72/KR2/$\overline{\text{SCK01}}$
INTP7			Analog input	P82/CMP1P
KR0	Input	Key interrupt input	Input port	P70/SO01/INTP4
KR1				P71/SI01/INTP5
KR2				P72/$\overline{\text{SCK01}}$/INTP6
KR3				P73/SO00/TxD0
KR4				P74/SI00/RxD0
KR5				P75/$\overline{\text{SCK00}}$
KR6				P76
KR7				P77
PCLBUZ0	Output	Clock output/buzzer output	Output port	P140
PGAI	Input	Programmable gain amplifier input	Analog input	P80/CMP0P/INTP3
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz division) output	Input port	P12/TI04/TO04/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P12/TI04/TO04/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P52/SLTI/SLTO
$\overline{\text{RESET}}$	Input	System reset input	–	–

(2) Non-port functions (2/3): 78K0R/KD3-L

Function Name	I/O	Function	After Reset	Alternate Function
RxD0	Input	Serial data input to UART0	Input port	P74/KR4/SI00
RxD1		Serial data input to UART1		P31/SI10/SDA10/INTP1
$\overline{SCK00}$	I/O	Clock input/output for CSI00	Input port	P75/KR5
$\overline{SCK01}$		Clock input/output for CSI01		P72/KR2/INTP6
$\overline{SCK10}$		Clock input/output for CSI10		P32/SCL10/INTP2
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P32/$\overline{SCK10}$/INTP2
SDA0	I/O	Serial data I/O for I^2C	Input port	P61
SDA10	I/O	Serial data I/O for simplified I^2C	Input port	P31/SI10/RxD1/INTP1
SI00	Input	Serial data input to CSI00	Input port	P74/KR4/RxD0
SI01		Serial data input to CSI01		P71/KR1/INTP5
SI10		Serial data input to CSI10		P31/RxD1/SDA10/INTP1
SLTI	Input	16-bit timer 00, 01 input	Input port	P52/RTC1HZ/SLTO
SLTO	Output	16-bit timer 00, 01 output	Input port	P52/RTC1HZ/SLTI
SO00	Output	Serial data output from CSI00	Input port	P73/KR3/TxD0
SO01		Serial data output from CSI01		P70/KR0/INTP4
SO10		Serial data output from CSI10		P30/TxD1
TI00	Input	External count clock input to 16-bit timer 00	Input port	P00
TI02		External count clock input to 16-bit timer 02		P10/TO02
TI03		External count clock input to 16-bit timer 03		P11/TO03
TI04		External count clock input to 16-bit timer 04		P12/TO04/RTCDIV/RTCCL
TI05		External count clock input to 16-bit timer 05		P13/TO05
TI06		External count clock input to 16-bit timer 06		P50/TO06
TI07		External count clock input to 16-bit timer 07		P51/TO07
TO00	Output	16-bit timer 00 output	Input port	P01
TO02		16-bit timer 02 output		P10/TI02
TO03		16-bit timer 03 output		P11/TI03
TO04		16-bit timer 04 output		P12/TI04/RTCDIV/RTCCL
TO05		16-bit timer 05 output		P13/TI05
TO06		16-bit timer 06 output		P50/TI06
TO07		16-bit timer 07 output		P51/TI07
TxD0	Output	Serial data output from UART0	Input port	P73/KR3/SO00
TxD1		Serial data output from UART1		P30/SO10
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124
EXCLK	Input	External clock input for main system clock	Input port	P122/X2

(2) Non-port functions (3/3): 78K0R/KD3-L

Function Name	I/O	Function	After Reset	Alternate Function
V_{DD}	–	Positive power supply (Port pins other than P20 to P27, P80 to P83, P150 to P152, and other than ports)	–	–
AV_{REF}	–	• A/D converter and comparator reference voltage input • Positive power supply for P20 to P27, P150 to P152, P80 to P83, A/D converter, programmable gain amplifier, and comparator	–	–
V_{SS}	–	Ground potential (Port pins other than P20 to P27, P80 to P83, P150 to P152, and other than ports)	–	–
AV_{SS}	–	Ground potential for A/D converter, programmable gain amplifier, comparator, P20 to P27, P150 to P152 and P80 to P83	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

2.1.4 78K0R/KE3-L

(1) Port functions (1/2): 78K0R/KE3-L

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI00
P01				TO00
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI02/TO02
P11				TI03/TO03
P12				TI04/TO04/ RTCDIV/RTCCL
P13				TI05/TO05
P14				TI06/TO06
P15				TI07/TO07
P16				–
P17				–
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
P30	I/O	Port 3. 4-bit I/O port. Input of P31 and P32 can be set to TTL buffer. Output of P30 to P32 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SO10/TxD1
P31				SI10/RxD1/SDA10/ INTP1
P32				$\overline{\text{SCK10}}$/SCL10/ INTP2
P33				–
P40[Note]	I/O	Port 4. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P42				–
P43				–
P50	I/O	Port 5. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P51				–
P52				RTC1HZ/SLTI/ SLTO
P53				–
P60	I/O	Port 6. 2-bit I/O port. Output of P60 and P61 is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0

Note If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally.

(1) Port functions (2/2): 78K0R/KE3-L

Function Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7. 8-bit I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
P71				KR1/SI01/INTP5
P72				KR2/$\overline{\text{SCK01}}$/INTP6
P73				KR3/SO00/TxD0
P74				KR4/SI00/RxD0
P75				KR5/$\overline{\text{SCK00}}$
P76				KR6
P77				KR7
P80	I/O	Port 8. 4-bit I/O port. Inputs/output can be specified in 1-bit units. Inputs of P80 to P83 can be set as comparator inputs or programmable gain amplifier inputs.	Analog input	CMP0P/INTP3/ PGAI
P81				CMP0M
P82				CMP1P/INTP7
P83				CMP1M
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P140	Output	Port 14. 1-bit output port and 1-bit I/O port. For only P141, input/output can be specified. For only P141, use of an on-chip pull-up resistor can be specified by a software setting.	Output port	PCLBUZ0
P141	I/O		Input port	PCLBUZ1
P150 to P153	I/O	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8 to ANI11

(2) Non-port functions (1/3): 78K0R/KE3-L

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANI8 to ANI11	Input			P150 to P153
CMP0M	Input	Input voltage on the (–) side of comparator 0	Analog input	P81
CMP0P	Input	Input voltage on the (+) side of comparator 0		P80/INTP3/PGAI
CMP1M	Input	Input voltage on the (–) side of comparator 1		P83
CMP1P	Input	Input voltage on the (+) side of comparator 1		P82/INTP7
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P31/SI10/RxD1/SDA10
INTP2				P32/$\overline{\text{SCK10}}$/SCL10
INTP3			Analog input	P80/CMP0P/PGAI
INTP4			Input port	P70/KR0/SO01
INTP5				P71/KR1/SI01
INTP6				P72/KR2/$\overline{\text{SCK01}}$
INTP7			Analog input	P82/CMP1P
KR0	Input	Key interrupt input	Input port	P70/SO01/INTP4
KR1				P71/SI01/INTP5
KR2				P72/$\overline{\text{SCK01}}$/INTP6
KR3				P73/SO00/TxD0
KR4				P74/SI00/RxD0
KR5				P75/$\overline{\text{SCK00}}$
KR6				P76
KR7				P77
PCLBUZ0	Output	Clock output/buzzer output	Output port	P140
PCLBUZ1			Input port	P141
PGAI	Input	Programmable gain amplifier input	Analog input	P80/CMP0P/INTP3
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz division) output	Input port	P12/TI04/TO04/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P12/TI04/TO04/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P52/SLTI/SLTO
$\overline{\text{RESET}}$	Input	System reset input	–	–

(2) Non-port functions (2/3): 78K0R/KE3-L

Function Name	I/O	Function	After Reset	Alternate Function
RxD0	Input	Serial data input to UART0	Input port	P74/KR4/SI00
RxD1		Serial data input to UART1		P31/SI10/SDA10/INTP1
$\overline{SCK00}$	I/O	Clock input/output for CSI00	Input port	P75/KR5
$\overline{SCK01}$		Clock input/output for CSI01		P72/KR2/INTP6
$\overline{SCK10}$		Clock input/output for CSI10		P32/SCL10/INTP2
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P32/$\overline{SCK10}$/INTP2
SDA0	I/O	Serial data I/O for I^2C	Input port	P61
SDA10	I/O	Serial data I/O for simplified I^2C	Input port	P31/SI10/RxD1/INTP1
SI00	Input	Serial data input to CSI00	Input port	P74/KR4/RxD0
SI01		Serial data input to CSI01		P71/KR1/INTP5
SI10		Serial data input to CSI10		P31/RxD1/SDA10/INTP1
SLTI	Input	16-bit timer 00, 01 input	Input port	P52/RTC1HZ/SLTO
SLTO	Output	16-bit timer 00, 01 output	Input port	P52/RTC1HZ/SLTI
SO00	Output	Serial data output from CSI00	Input port	P73/KR3/TxD0
SO01		Serial data output from CSI01		P70/KR0/INTP4
SO10		Serial data output from CSI10		P30/TxD1
TI00	Input	External count clock input to 16-bit timer 00	Input port	P00
TI02		External count clock input to 16-bit timer 02		P10/TO02
TI03		External count clock input to 16-bit timer 03		P11/TO03
TI04		External count clock input to 16-bit timer 04		P12/TO04/RTCDIV/RTCCL
TI05		External count clock input to 16-bit timer 05		P13/TO05
TI06		External count clock input to 16-bit timer 06		P14/TO06
TI07		External count clock input to 16-bit timer 07		P15/TO07
TO00	Output	16-bit timer 00 output	Input port	P01
TO02		16-bit timer 02 output		P10/TI02
TO03		16-bit timer 03 output		P11/TI03
TO04		16-bit timer 04 output		P12/TI04/RTCDIV/RTCCL
TO05		16-bit timer 05 output		P13/TI05
TO06		16-bit timer 06 output		P14/TI06
TO07		16-bit timer 07 output		P15/TI07
TxD0	Output	Serial data output from UART0	Input port	P73/KR3/SO00
TxD1		Serial data output from UART1		P30/SO10
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124
EXCLK	Input	External clock input for main system clock	Input port	P122/X2

(2) Non-port functions (3/3): 78K0R/KE3-L

Function Name	I/O	Function	After Reset	Alternate Function
V_{DD}	–	Positive power supply (P121 to P124 and other than ports (other than $\overline{\text{RESET}}$ pin and FLMD0 pin))	–	–
EV_{DD}	–	Positive power supply for ports (other than P20 to P27, P150 to P153, P80 to P83, and P121 to P124), and $\overline{\text{RESET}}$ and FLMD0 pin	–	–
AV_{REF}	–	• A/D converter and comparator reference voltage input • Positive power supply for P20 to P27, P150 to P153, P80 to P83, A/D converter, programmable gain amplifier, and comparator	–	–
V_{SS}	–	Ground potential (P121 to P124 and other than ports (other than $\overline{\text{RESET}}$ pin and FLMD0 pin))	–	–
EV_{SS}	–	Ground potential for ports (other than P20 to P27, P150 to P153, and P121 to P124), and $\overline{\text{RESET}}$ and FLMD0 pin	–	–
AV_{SS}	–	Ground potential for A/D converter, programmable gain amplifier, comparator, P20 to P27, P150 to P153 and P80 to P83	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

2.2 Description of Pin Functions

Remark The pins mounted depend on the product. See **1.4 Pin Configuration (Top View)** and **2.1 Pin Function List**.

2.2.1 P00, P01 (port 0)

P00 and P01 function as an I/O port. These pins also function as timer I/O.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P00/ TI00	–		–	√	√
P11/TO00	–		–	√	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P00 and P01 function as an I/O port. P00 and P01 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00 and P01 function as timer I/O.

(a) TI00

This is the pin for inputting an external count clock/capture trigger to 16-bit timer 00.

(b) TO00

This is the timer output pin of 16-bit timer 00.

2.2.2 P10 to P17 (port 1)

P10 to P17 function as an I/O port. These pins also function as timer I/O and real-time counter clock output.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P10/TI02/TO02	√		√	√	√
P11/TO00/TI03/ TO03	√		√	√	√
P12/TI04/TO04/ RTCDIV/RTCCL	P12/TI04/ TO04[Note 1]	√	√	√	√
P13/TI05/TO05	√		√	√	√
P14/TI06/TO06	–[Note 2]		–[Note 2]	–[Note 2]	√
P15/TI07/TO07	–[Note 2]		–[Note 2]	–[Note 2]	√
P16	–		–	–	√
P17	–		–	–	√

Notes 1. 40-pin product of the 78K0R/KC3-L does not have a RTCDIV/RTCCL pin.

2. TI06/TO06 and TI07/TO07 are shared with P50 and P51, respectively, in products other than the 78K0R/KE3-L.

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P10 to P17 function as an I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

(2) Control mode

P10 to P17 function as timer I/O and real-time counter clock output.

(a) TI02 to TI07

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 02 to 07.

(b) TO02 to TO07

These are the timer output pins of 16-bit timers 02 to 07.

(c) RTCDIV

This is the real-time counter clock (32 kHz division) output pin.

(d) RTCCL

This is the real-time counter clock (32 kHz original oscillation) output pin.

2.2.3 P20 to P27 (port 2)

P20 to P27 function as an I/O port. These pins also function as A/D converter analog input.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P20/ANI0	√		√	√	√
P21/ANI1	√		√	√	√
P22/ANI2	√		√	√	√
P23/ANI3	√		√	√	√
P24/ANI4	√		√	√	√
P25/ANI5	√		√	√	√
P26/ANI6	√		√	√	√
P27/ANI7	√		√	√	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P27 function as an I/O port. P20 to P27 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P27 function as the A/D converter analog input pins (ANI0 to ANI7). When using these pins as the analog input pins, see **13.6 (5) ANI0/P20 to ANI7/P27, ANI8/P150 to ANI15/P157**.

Caution ANI0/P20 to ANI7/P27 are set in the digital input (general-purpose port) mode after release of reset.

2.2.4 P30 to P33 (port 3)

P30 to P33 function as an I/O port. These pins also function as serial interface data I/O, clock I/O, and external interrupt request input.

Input to the P30 and P31 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units, using port input mode register 3 (PIM3).

Output from the P30 to P32 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units, using port output mode register 3 (POM3).

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P30/SO10/TxD1	√		√	√	√
P31/SI10/RxD1/ SDA10/INTP1	√		√	√	√
P32/$\overline{\text{SCK10}}$/ SCL10/INTP2	√		√	√	√
P33	–		–	–	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P33 function as an I/O port. P30 to P33 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 to P33 function as serial interface data I/O, clock I/O, and external interrupt request input.

(a) SI10

This is a serial data input pin of serial interface CSI10.

(b) SO10

This is a serial data output pin of serial interface CSI10.

(c) $\overline{\text{SCK10}}$

This is a serial clock I/O pin of serial interface CSI10.

(d) TxD1

This is a serial data output pin of serial interface UART1.

(e) RxD1

This is a serial data input pin of serial interface UART1.

(f) SDA10

This is a serial data I/O pin of serial interface for simplified I^2C.

(g) SCL10

This is a serial clock I/O pin of serial interface for simplified I^2C.

(h) INTP1, INTP2

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

Caution To use P30/SO10/TxD1 and P32/$\overline{\text{SCK10}}$/SCL10/INTP2 as general-purpose ports, set serial communication operation setting register 02 (SCR02) to the default status (0087H). In addition, clear port output mode register 3 (POM3) to 00H.

2.2.5 P40 to P43 (port 4)

P40 to P43 function as an I/O port. These pins also function as data I/O for a flash memory programmer/debugger and clock output.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P40/TOOL0	√		√	√	√
P41/TOOL1	√		√	√	√
P42	–		–	–	√
P43	–		–	–	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P40 to P43 function as an I/O port. P40 to P43 can be set to input or output port in 1-bit units using port mode register 4 (PM4). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 4 (PU4).

Be sure to connect an external pull-up resistor to P40 when on-chip debugging is enabled (by using an option byte).

(2) Control mode

P40 to P43 function as data I/O for a flash memory programmer/debugger and clock output.

(a) TOOL0

This is a data I/O pin for a flash memory programmer/debugger.

Be sure to pull up this pin externally when on-chip debugging is enabled (pulling it down is prohibited).

(b) TOOL1

This is a clock output pin for a debugger.

When the on-chip debug function is used, the P41/TOOL1 pin can be used as follows by the mode setting on the debugger.

1-line mode: can be used as a port (P41).

2-line mode: used as a TOOL1 pin and cannot be used as a port (P41).

Caution The function of the P40/TOOL0 pin varies as described in (a) to (c) below.
In the case of (b) or (c), make the specified connection.

(a) In normal operation mode and when on-chip debugging is disabled (OCDENSET = 0) by an option byte (000C3H)
=> Use this pin as a port pin (P40).

(b) In normal operation mode and when on-chip debugging is enabled (OCDENSET = 1) by an option byte (000C3H)
=> Connect this pin to V_{DD} via an external resistor, and always input a high level to the pin before reset release.

(c) When on-chip debug function is used, or in write mode of flash memory programmer
=> Use this pin as TOOL0.
Directly connect this pin to the on-chip debug emulator or a flash memory programmer, or pull it up by connecting it to V_{DD} via an external resistor.

2.2.6 P50 to P53 (port 5)

P50 to P53 function as an I/O port. These pins also function as real-time counter correction clock output and timer I/O.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P50/TI06/TO06	√		√	√	P50[Note]
P51/TI07/TO07	√		√	√	P51[Note]
P52/RTC1HZ/ SLTI/SLTO	–	√	√	√	√
P53	–		–	–	√

Note TI06/TO06 and TI07/TO07 are shared only in the 78K0R/KC3-L and 78K0R/KD3-L. The 78K0R/KE3-L does not have a sharing function.

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P50 to P53 function as an I/O port. P50 to P53 can be set to input or output port in 1-bit units using port mode register 5 (PM5). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 5 (PU5).

(2) Control mode

P50 to P53 function as real-time counter correction clock output and timer I/O.

(a) RTC1HZ

This is the real-time counter correction clock (1 Hz) output pin.

(b) SLTI

This is used as a pin for inputting an external count clock or a capture trigger to 16-bit timers 00 and 01, by setting the input switching control register (ISC).

(c) SLTO

This is used as a timer output pin of 16-bit timers 00 and 01, by setting the input switching control register (ISC).

(d) TI06, TI07

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 06 and 07.

(e) TO06, TO07

These are the timer output pins of 16-bit timers 06 and 07.

2.2.7 P60 and P61 (port 6)

P60 and P61 function as an I/O port. These pins also function as serial interface IICA data I/O and clock I/O.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P60/SCL0	–		√	√	√
P61/SDA0	–		√	√	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P60 and P61 function as an I/O port. P60 and P61 can be set to input port or output port in 1-bit units using port mode register 6 (PM6).

Output of P60 and P61 is N-ch open-drain output (6 V tolerance).

(2) Control mode

P60 and P61 function as serial interface IICA data I/O and clock I/O.

(a) SDA0

This is a serial data I/O pin of serial interface IICA.

(b) SCL0

This is a serial clock I/O pin of serial interface IICA.

2.2.8 P70 to P77 (port 7)

P70 to P77 function as an I/O port. These pins also function as key interrupt input, serial interface data I/O, clock I/O, and external interrupt request input.

Input to the P71, P72, P74, and P75 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units, using port input mode register 7 (PIM7).

Output from the P70, P72, P73, and P75 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units, using port output mode register 7 (POM7).

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P70/KR0/SO01/INTP4	√		√	√	√
P71/KR1/SI01/INTP5	√		√	√	√
P72/KR2/$\overline{\text{SCK01}}$/INTP6	√		√	√	√
P73/KR3/SO00/TxD0	√		√	√	√
P74/KR4/SI00/RxD0	√		√	√	√
P75/KR5/$\overline{\text{SCK00}}$	√		√	√	√
P76/KR6	–		–	√	√
P77/KR7	–		–	√	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P70 to P77 function as an I/O port. P70 to P77 can be set to input or output port in 1-bit units using port mode register 7 (PM7). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 7 (PU7).

(2) Control mode

P70 to P77 function as key interrupt input, serial interface data I/O, clock I/O, and external interrupt request input.

(a) KR0 to KR7

These are the key interrupt input pins.

(b) SI00, SI01

These are the serial data input pin of serial interface CSI00 and CSI01.

(c) SO00, SO01

These are the serial data output pin of serial interface CSI00 and CSI01.

(d) $\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$

These are the serial clock I/O pins of serial interface CSI00 and CSI01.

(e) RxD0

This is a serial data input pin of serial interface UART0.

(f) TxD0

This is a serial data output pin of serial interface UART0.

(g) INTP4 to INTP6

These are the external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

Caution To use P70/KR0/SO01/INTP4, P72/KR2/$\overline{\text{SCK01}}$/INTP6, P73/KR3/SO00/TxD0, and P75/KR5/$\overline{\text{SCK00}}$ as general-purpose ports, set serial communication operation setting registers 00 and 01 (SCR00 and SCR01) to the default status (0087H). In addition, clear port output mode register 7 (POM7) to 00H.

2.2.9 P80 to P83 (port 8)

P80 to P83 function as an I/O port. These pins also function as input voltages on the (+) side of comparators 0 and 1, input voltages on the (–) side of comparators 0 and 1, external interrupt request inputs, and programmable gain amplifier inputs.

Inputs to the P80 to P83 pins must be enabled or disabled in 1-bit units using port input mode register 8 (PIM8).

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P80/CMP0P/ INTP3/PGAI	√		√	√	√
P81/CMP0M	√		√	√	√
P82/CMP1P/ INTP7	–	√	√	√	√
P83/CMP1M	√		√	√	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P80 to P83 function as an I/O port. P80 to P83 can be set to input port or output port in 1-bit units using port mode register 8 (PM8).

(2) Control mode

P80 to P83 function as input voltages on the (+) side of comparators 0 and 1, input voltages on the (–) side of comparators 0 and 1, external interrupt request inputs, and programmable gain amplifier inputs.

(a) CMP0P, CMP1P

These are the input voltage pins on the (+) sides of comparators 0 and 1.

(b) CMP0M, CMP1M

These are the input voltage pins on the (–) sides of comparators 0 and 1.

(c) INTP3, INTP7

These are the external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(d) PGAI

This is a programmable gain amplifier input pin.

2.2.10 P120 to P124 (port 12)

P120 functions as an I/O port. P121 to P124 function as ant input port. These pins also function as external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, and external clock input for main system clock.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P120/INTP0/ EXLVI	√		√	√	√
P121/X1	√		√	√	√
P122/X2/ EXCLK	√		√	√	√
P123/XT1	–	√	√	√	√
P124/XT2	–	√	√	√	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P120 functions as an I/O port. P120 can be set to input or output port using port mode register 12 (PM12). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P124 function as an input port.

(2) Control mode

P120 to P124 function as external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, and external clock input for main system clock.

(a) INTP0

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) EXLVI

This is a potential input pin for external low-voltage detection.

(c) X1, X2

These are the pins for connecting a resonator for main system clock.

(d) EXCLK

This is an external clock input pin for main system clock.

(e) XT1, XT2

These are the pins for connecting a resonator for subsystem clock.

2.2.11 P140, P141 (port 14)

P140 functions as a 1-bit output port. P141 functions as a 1-bit I/O port. These pins also function as clock/buzzer output.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P140/PCLBUZ0	–		√	√	√
P141/PCLBUZ1	–		–	–	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P140 functions as a 1-bit output port.

P141 functions as a 1-bit I/O port. P141 can be set to input or output port in 1-bit units using port mode register 14 (PM14). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 14 (PU14).

(2) Control mode

P140 and P141 function as clock/buzzer output.

(a) PCLBUZ0, PCLBUZ1

These are the clock/buzzer output pins.

2.2.12 P150 to P153 (port 15)

P150 to P153 function as an I/O port. These pins also function as A/D converter analog input.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P150/ANI8	√		√	√	√
P151/ANI9	√		√	√	√
P152/ANI10	–		√	√	√
P153/ANI11	–		–	–	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P150 to P153 function as an I/O port. P150 to P153 can be set to input or output port in 1-bit units using port mode register 15 (PM15).

(2) Control mode

P150 to P153 function as the A/D converter analog input pins (ANI8 to ANI11). When using these pins as the analog input pins, see **13.6 (5) ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI15/P157**.

Caution ANI8/P150 to ANI11/P153 are set in the digital input (general-purpose port) mode after release of reset.

2.2.13 AV_{REF}, AV_{SS}, V_{DD}, EV_{DD}, V_{SS}, EV_{SS}

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
AV_{REF}	√		√	√	√
AV_{SS}	√		√	√	√
V_{DD}	√		√	√	√
EV_{DD}	–		–	–	√
V_{SS}	√		√	√	√
EV_{SS}	–		–	–	√

(1) AV_{REF}

This is the A/D converter and comparator reference voltage input pin and the positive power supply pin of P20 to P27, P150 to P153, P80 to P83, A/D converter, programmable gain amplifier, and comparator.

When all pins of port 2, port 15, and port 8 are used as the analog port pins, make the potential of AV_{REF} be such that $1.8\ V \leq AV_{REF} \leq V_{DD}$. When one or more of the pins of port 2, port 15, and port 8 are used as the digital port pins or when the A/D converter, programmable gain amplifier, and comparator are not used, make AV_{REF} the same potential as EV_{DD} or V_{DD}.

(2) AV_{SS}

This is the ground potential pin of A/D converter, programmable gain amplifier, comparator, P20 to P27, P150 to P153, and P80 to P83. Even when the A/D converter, programmable gain amplifier, and comparator are not used, always use this pin with the same potential as EV_{SS} or V_{SS}.

(3) V_{DD}, EV_{DD}

V_{DD} is the positive power supply pin for P121 to P124 and other than ports (other than the $\overline{\text{RESET}}$ pin and FLMD0 pin) Note.

EV_{DD} is the positive power supply pin for ports other than those of P20 to P27, P150 to P153, P80 to P83, and P121 to P124, as well as for the $\overline{\text{RESET}}$ pin and FLMD0 pin.

Note With products not provided with an EV_{DD} pin, use V_{DD} as the positive power supply pin for port pins other than P20 to P27, P150 to P153, and P80 to P83, as well as for pins other than those of ports.

(4) V_{SS}, EV_{SS}

V_{SS} is the ground potential pin for P121 to P124 and other than ports (other than the $\overline{\text{RESET}}$ pin and FLMD0 pin) Note.

EV_{SS} is the ground potential pin for ports other than those of P20 to P27, P150 to P153, P80 to P83, and P121 to P124, as well as for the $\overline{\text{RESET}}$ pin and FLMD0 pin.

Note With products not provided with an EV_{SS} pin, use V_{SS} as the ground potential pin for port pins other than P20 to P27, P150 to P153, P80 to P83, as well as for pins other than those of ports.

2.2.14 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

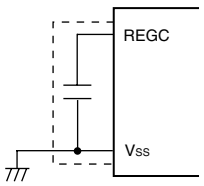
When the external reset pin is not used, connect this pin directly to EV_{DD} or via a resistor.

When the external reset pin is used, design the circuit based on V_{DD}.

2.2.15 REGC

This is the pin for connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF).

Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

2.2.16 FLMD0

This is a pin for setting flash memory programming mode.

Perform either of the following processing.

(a) In normal operation mode

It is recommended to leave this pin open during normal operation.

The FLMD0 pin must always be kept at the V_{SS} level before reset release but does not have to be pulled down externally because it is internally pulled down by reset. However, pulling it down must be kept selected (i.e., FLMDPUP = "0", default value) by using bit 7 (FLMDPUP) of the background event control register (BECTL) (see **26.5 (1) Back ground event control register**). To pull it down externally, use a resistor of 200 kΩ or smaller.

Self programming and the rewriting of flash memory with the programmer can be prohibited using hardware, by directly connecting this pin to the V_{SS} pin.

(b) In self programming mode

It is recommended to leave this pin open when using the self programming function. To pull it down externally, use a resistor of 100 kΩ to 200 kΩ.

In the self programming mode, the setting is switched to pull up in the self programming library.

(c) In flash memory programming mode

Directly connect this pin to a flash memory programmer when data is written by the flash memory programmer. This supplies a writing voltage of the V_{DD} level to the FLMD0 pin.

The FLMD0 pin does not have to be pulled down externally because it is internally pulled down by reset. To pull it down externally, use a resistor of 1 kΩ to 200 kΩ.

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-3 shows the types of pin I/O circuits and the recommended connections of unused pins.

Table 2-3. Connection of Unused Pins (1/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI00	8-R	I/O	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P01/TO00	5-AG		
P10/TI02/TO02	8-R		
P11/TI03/TO03			
P12/TI04/TO04/RTCDIV/RTCCL			
P13/TI05/TO05			
P14/TI06/TO06 Note 1			
P15/TI07/TO07 Note 1			
P16			
P17			
P20/ANI0 to P27/ANI7 Note 2	11-G		Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open.
P30/SO10/TxD1	5-AG		Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P31/SI10/RxD1/SDA10/INTP1	5-AN		<When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P32/$\overline{SCK10}$/SCL10/INTP2			
P33	5-AG		Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P40/TOOL0	8-R		<When on-chip debugging is enabled> Pull this pin up (pulling it down is prohibited). <When on-chip debugging is disabled> Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P41/TOOL1			Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P42	5-AG		
P43			
P50/TI06/TO06 Note 3	8-R		
P51/TI07/TO07 Note 3			
P52/RTC1HZ/SLTI/SLTO			
P53	5-AG		

Notes 1. TI06/TO06 and TI07/TO07 are shared with P50 and P51, respectively, in products other than the 78K0R/KE3-L.

2. P20/ANI0 to P27/ANI7 are set in the digital input port mode after release of reset.

3. TI06/TO06 and TI07/TO07 are shared with P14 and P15, respectively, in the 78K0R/KE3-L.

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Table 2-3. Connection of Unused Pins (2/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P60/SCL0	13-R	I/O	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor, or connect directly to EV_{SS}. Output: Set the port output latch to 0 and leave open with low level out put.
P61/SDA0			
P70/KR0/SO01/INTP4	8-R		Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P71/KR1/SI01/INTP5	5-AN		Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P72/KR2/$\overline{SCK01}$/INTP6			Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P73/KR3/SO00/TxD0	8-R		
P74/KR4/SI00/RxD0	5-AN		Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P75/KR5/$\overline{SCK00}$			Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P76/KR6	8-R		Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P77/KR7			
P80/CMP0P/INTP3/PGAI	11-J		Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open.
P81/CMP0M	11-H		
P82/CMP1P/INTP7	11-I		
P83/CMP1M	11-H		
P120/INTP0/EXLVI	8-R		Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Table 2-2. Connection of Unused Pins (3/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P121/X1[Note 1]	37-C	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P122/X2/EXCLK[Note 1]			
P123/XT1[Note 1]	37-B		
P124/XT2[Note 1]			
P140/PCLBUZ0	3-C	Output	Leave open.
P141/PCLBUZ1	5-AG	I/O	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P150/ANI8 to P153/ANI11[Note 2]	11-G		Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open.
AV_{REF}	–	–	<When one or more of P20 to P27, P150 to P153, or P80 to P83 are set as a digital port> Make this pin the same potential as EV_{DD} or V_{DD}. <When all of P20 to P27, P150 to P153, and P80 to P83 are set as analog ports> Make this pin to have a potential where 1.8 V ≤ AV_{REF} ≤ V_{DD}.
AV_{SS}	–	–	Make this pin the same potential as EV_{SS} or V_{SS}.
FLMD0	2-W	–	Leave open or connect to V_{SS} via a resistor of 100 kΩ or more.
$\overline{\text{RESET}}$	2	Input	Connect directly to EV_{DD} or via a resistor.
REGC	–	–	Connect to V_{SS} via capacitor (0.47 to 1 μF).

Notes 1. Use recommended connection above in input port mode (see **Figure 7-3 Format of Clock Operation Mode Control Register (CMC)**) when these pins are not used.

2. P150/ANI8 to P153/ANI11 are set in the digital input port mode after release of reset.

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 2-1. Pin I/O Circuit List (1/3)

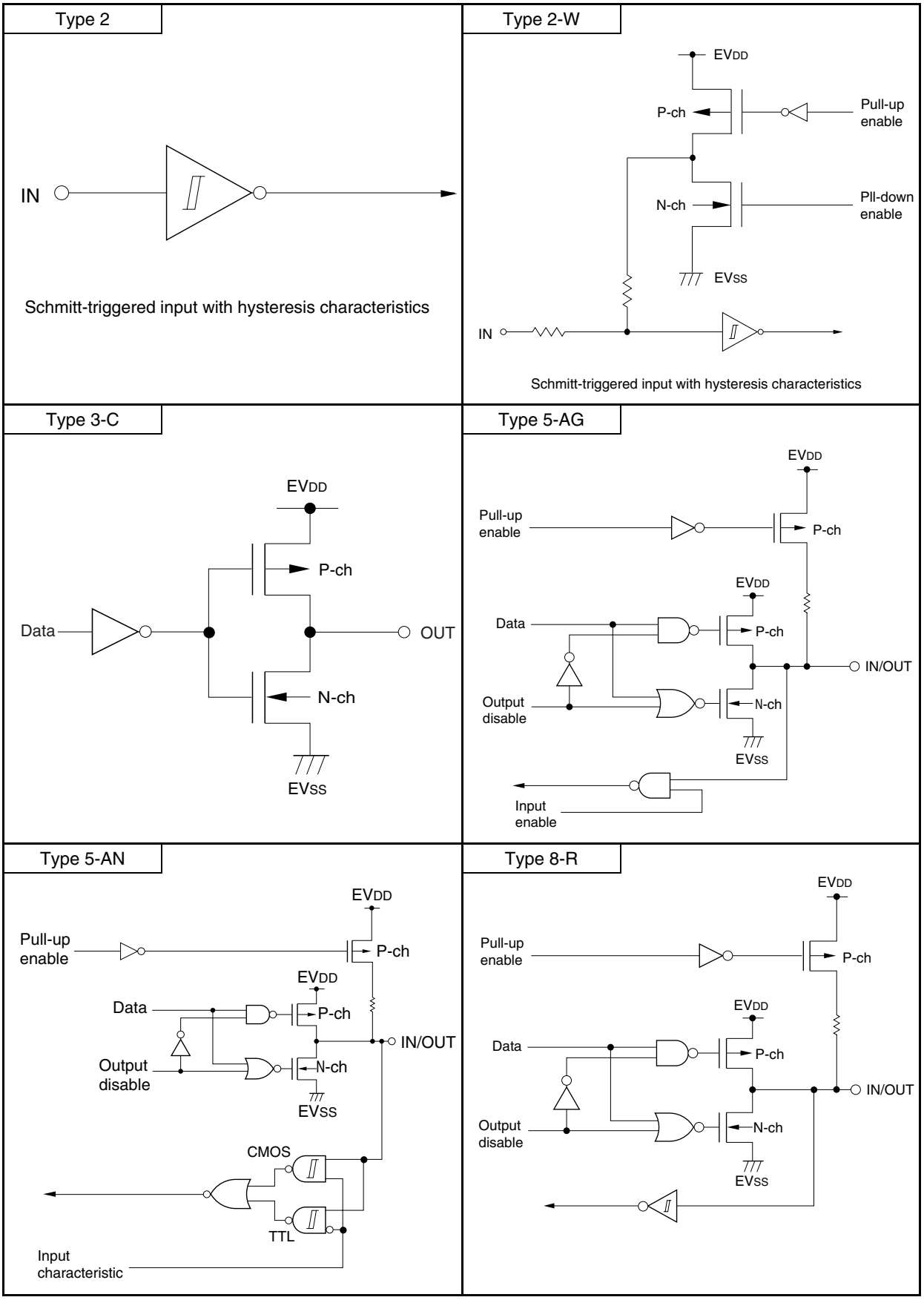


Figure 2-1. Pin I/O Circuit List (2/3)

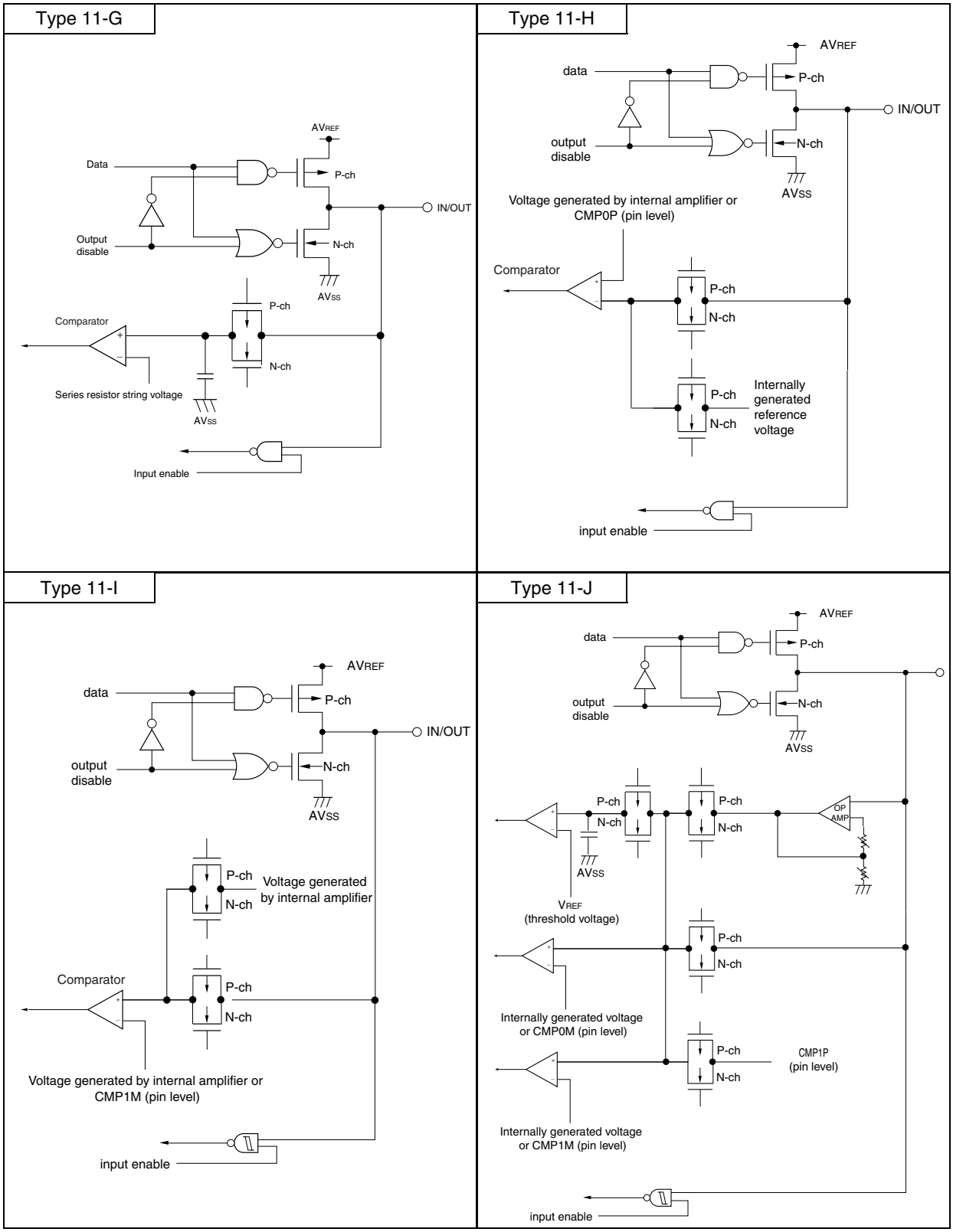
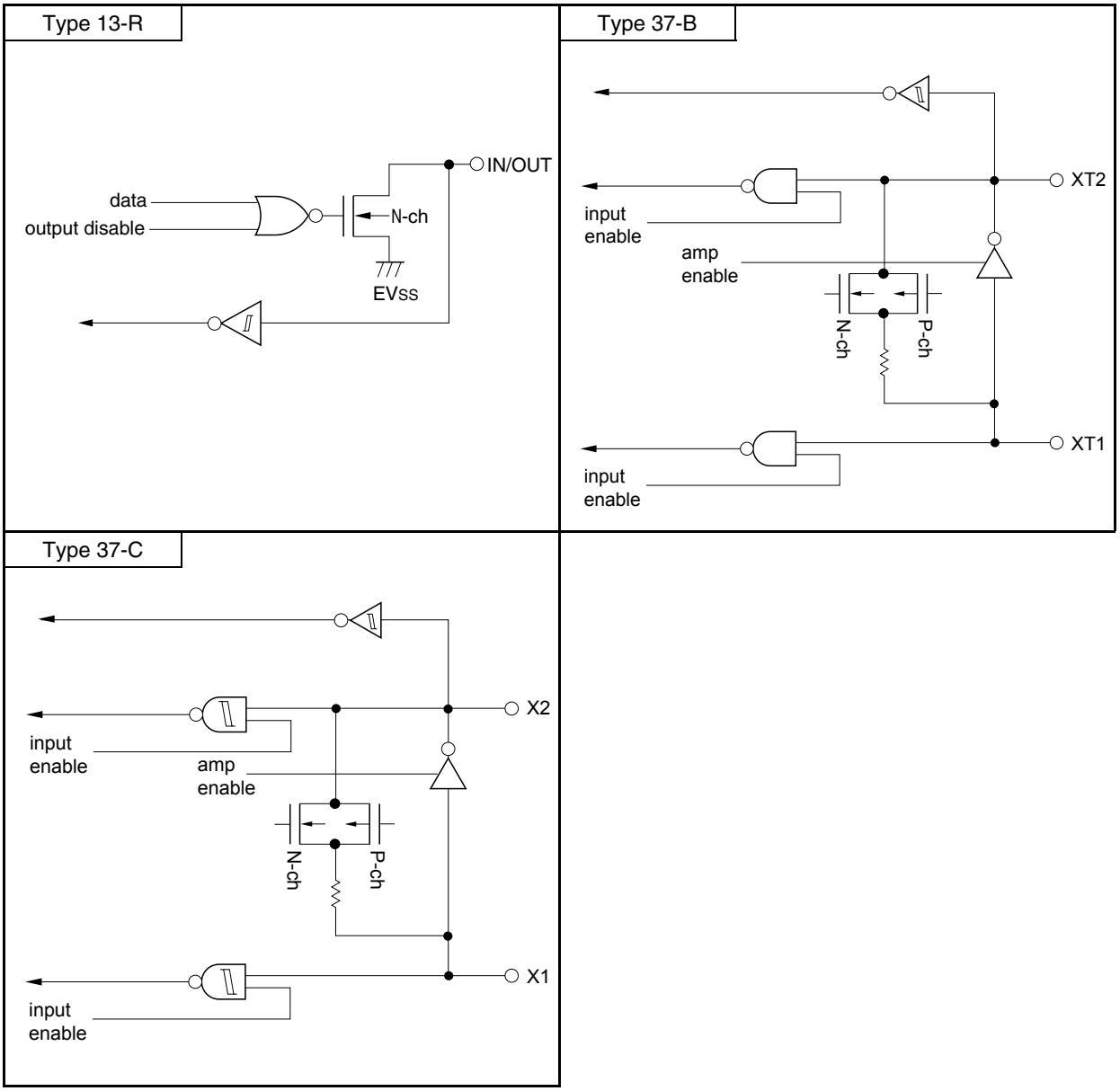


Figure 2-1. Pin I/O Circuit List (3/3)



CHAPTER 3 PIN FUNCTIONS (78K0R/KF3-L, 78K0R/KG3-L)

Caution For the functions of the pins in the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L, see CHAPTER 2 PIN FUNCTIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L).

3.1 Pin Function List

Pin I/O buffer power supplies depend on the product. The relationship between these power supplies and the pins is shown below.

Table 3-1. Pin I/O Buffer Power Supplies (AV_{REF}, EV_{DD0}, V_{DD})

- 78K0R/KF3-L: 80-pin plastic LQFP (14x14)
  80-pin plastic LQFP (fine pitch) (12x12)

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27, P150 to P153
EV_{DD0}	• Port pins other than P20 to P27, P121 to P124, and P150 to P153 • $\overline{\text{RESET}}$ and FLMD0 pins
V_{DD}	• P121 to P124 • Pins other than port pins (excluding $\overline{\text{RESET}}$ and FLMD0 pins)

Table 3-2. Pin I/O Buffer Power Supplies (AV_{REF}, EV_{DD0}, EV_{DD1}, V_{DD})

- 78K0R/KG3-L: 100-pin plastic LQFP (14x20)
  100-pin plastic LQFP (fine pitch) (14x14)
  100-pin plastic FBGA (6x6)[Note]

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27, P150 to P157
EV_{DD0}, EV_{DD1}	• Port pins other than P20 to P27, P121 to P124, and P150 to P157 • $\overline{\text{RESET}}$ and FLMD0 pins
V_{DD}	• P121 to P124 • Pins other than port pins (excluding $\overline{\text{RESET}}$ and FLMD0 pins)

Note μPD78F1013 and μPD78F1014 only

3.1.1 78K0R/KF3-L

(1) Port functions (1/2): 78K0R/KF3-L

Function Name	I/O	Function	After Reset	Alternate Function
P02	I/O	Port 0. 5-bit I/O port. Input of P03 and P04 can be set to TTL input buffer. Output of P02 to P04 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SO10/TxD1
P03				SI10/RxD1/SDA10
P04				$\overline{\text{SCK10}}$/SCL10
P05				TI05/TO05
P06				TI06/TO06
P10	I/O	Port 1. 8-bit I/O port. Input of P10 and P11 can be set to TTL input buffer. Output of P10 and P12 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK00}}$
P11				SI00/RxD0
P12				SO00/TxD0
P13				TxD3
P14				RxD3
P15				RTCDIV/RTCCL
P16				TI01/TO01/INTP5
P17				TI02/TO02
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
P30	I/O	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	RTC1HZ/INTP3
P31				TI03/TO03/INTP4
P40[Note 1]	I/O	Port 4. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P42				TI04/TO04
P43				$\overline{\text{SCK01}}$
P44				SI01
P45				SO01
P46, P47				–
P50	I/O	Port 5. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1/$\overline{\text{SCK40}}$[Note 2]
P51				INTP2/SI40/RxD4[Note 2]
P52				TO00/SO40/TxD4[Note 2]
P53				TI00/$\overline{\text{SCK41}}$[Note 2]
P54				TI07/TO07/SI41[Note 2]
P55				PCLBUZ1/INTP7/SO41[Note 2]

Notes 1. If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally (see **Caution** in **3.2.5 P40 to P47 (port 4)**).

2. SCK40, SCK41, SI40, SI41, SO40, SO41, TxD4, RxD4 are only mounted in the μPD78F1027 and 78F1028.

(1) Port functions (2/2): 78K0R/KF3-L

Function Name	I/O	Function	After Reset	Alternate Function
P60	I/O	Port 6. 8-bit I/O port. Output of P60 to P63 can be set to N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units. For only P64 to P67, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCL0
P61				SDA0
P62, P63				–
P64 to P67				TI10/TO10 to TI13/TO13
P70 to P73	I/O	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0 to KR3
P74 to P77				KR4/INTP8 to KR7/INTP11
P90, P91	I/O	Port 9. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P110, P111	I/O	Port 11. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P130	Output	Port 13. 1-bit output port.	Output port	–
P140	I/O	Port 14. 4-bit I/O port. Input of P142 and P143 can be set to TTL input buffer. Output of P142 to P144 can be set to the N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0/INTP6
P142				$\overline{SCK20}$/SCL20
P143				SI20/RxD2/SDA20
P144				SO20/TxD2
P150 to P153	I/O	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8 to ANI11

(2) Non-port functions (1/3): 78K0R/KF3-L

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANI8 to ANI11				P150 to P153
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P50/$\overline{\text{SCK40}}$[Note]
INTP2				P51/SI40[Note]/RxD4[Note]
INTP3				P30/RTC1HZ
INTP4				P31/TI03/TO03
INTP5				P16/TI01/TO01
INTP6				P140/PCLBUZ0
INTP7				P55/PCLBUZ1/SO41[Note]
INTP8 to INTP11				P74/KR4 to P77/KR7
KR0 to KR3	Input	Key interrupt input	Input port	P70 to P73
KR4 to KR7				P74/INTP8 to P77/INTP11
PCLBUZ0	Output	Clock output/buzzer output	Input port	P140/INTP6
PCLBUZ1				P55/INTP7
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF: target).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz divided frequency) output	Input port	P15/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P15/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P30/INTP3
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P11/SI00
RxD1	Input	Serial data input to UART1	Input port	P03/SI10/SDA10
RxD2	Input	Serial data input to UART2	Input port	P143/SI20/SDA20
RxD3	Input	Serial data input to UART3	Input port	P14
RxD4[Note]	Input	Serial data input to UART4	Input port	P51/INTP2/SI40[Note]
$\overline{\text{SCK00}}$	I/O	Clock input/output for CSI00, CSI01, CSI10, CSI20, CSI40, and CSI41	Input port	P10
$\overline{\text{SCK01}}$				P43
$\overline{\text{SCK10}}$				P04/SCL10
$\overline{\text{SCK20}}$				P142/SCL20
$\overline{\text{SCK40}}$				P50/INTP1
$\overline{\text{SCK41}}$				P53/TI00
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P04/$\overline{\text{SCK10}}$
SCL20				P142/$\overline{\text{SCK20}}$

Note $\overline{\text{SCK40}}$, $\overline{\text{SCK41}}$, SI40, SI41, SO40, SO41, TxD4, RxD4 are only mounted in the μPD78F1027 and 78F1028.

(2) Non-port functions (2/3): 78K0R/KF3-L

Function Name	I/O	Function	After Reset	Alternate Function
SDA0	I/O	Serial data I/O for I^2C	Input port	P61
SDA10	I/O	Serial data I/O for simplified I^2C	Input port	P03/SI10/RxD1
SDA20				P143/SI20/RxD2
SI00	Input	Serial data input to CSI00, CSI01, CSI10, CSI20, CSI40, and CSi41	Input port	P11/RxD0
SI01				P44
SI10				P03/RxD1/SDA10
SI20				P143/RxD2/SDA20
SI40Note				P51/RxD4Note/INTP2
SI41Note				P54/TI07/TO07
SO00	Output	Serial data output from CSI00, CSI01, CSI10, CSI20, CSI40, and CSI41	Input port	P12/TxD0
SO01				P45
SO10				P02/TxD1
SO20				P144/TxD2
SO40				P52/TO00/TxD4Note
SO41				P55/PCLBUZ1/INTP7
TI00	Input	External count clock input to 16-bit timer 00	Input port	P53/$\overline{SCK41}$Note
TI01		External count clock input to 16-bit timer 01		P16/TO01/INTP5
TI02		External count clock input to 16-bit timer 02		P17/TO02
TI03		External count clock input to 16-bit timer 03		P31/TO03/INTP4
TI04		External count clock input to 16-bit timer 04		P42/TO04
TI05		External count clock input to 16-bit timer 05		P05/TO05
TI06		External count clock input to 16-bit timer 06		P06/TO06
TI07		External count clock input to 16-bit timer 07		P54/TO07/SI41Note
TI10		External count clock input to 16-bit timer 10		P64/TO10
TI11		External count clock input to 16-bit timer 11		P65/TO11
TI12		External count clock input to 16-bit timer 12		P66/TO12
TI13		External count clock input to 16-bit timer 13		P67/TO13
TO00	Output	16-bit timer 00 output	Input port	P52/SO40Note/TxD4Note
TO01		16-bit timer 01 output		P16/TI01/INTP5
TO02		16-bit timer 02 output		P17/TI02
TO03		16-bit timer 03 output		P31/TI03/INTP4
TO04		16-bit timer 04 output		P42/TI04
TO05		16-bit timer 05 output		P05/TI05
TO06		16-bit timer 06 output		P06/TI06
TO07		16-bit timer 07 output		P54/TI07/SI41Note
TO10		16-bit timer 10 output		P64/TI10
TO11		16-bit timer 11 output		P65/TI11
TO12		16-bit timer 12 output		P66/TI12
TO13		16-bit timer 13 output		P67/TI13

Note $\overline{SCK41}$, SI40, SI41, SO40, SO41, TxD4, and RxD4 are only mounted in the μPD78F1027 and 78F1028.

(2) Non-port functions (3/3) : 78K0R/KF3-L

Function Name	I/O	Function	After Reset	Alternate Function
TxD0	Output	Serial data output from UART0	Input port	P12/SO00
TxD1		Serial data output from UART1		P02/SO10
TxD2		Serial data output from UART2		P144/SO20
TxD3		Serial data output from UART3		P13
TxD4[Note]		Serial data output from UART4		P52/SO40[Note]/TO00
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
EXCLK	Input	External clock input for main system clock	Input port	P122/X2
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124
V_{DD}	–	Positive power supply (P121 to P124 and other than ports (excluding $\overline{\text{RESET}}$ and FLMD0 pins))	–	–
EV_{DD0}	–	Positive power supply for ports (other than P20 to P27, P121 to P124, P150 to P153), and $\overline{\text{RESET}}$ and FLMD0 pins	–	–
AV_{REF}	–	• A/D converter reference voltage input • Positive power supply for P20 to P27, P150 to P153, and A/D converter	–	–
V_{SS}	–	Ground potential (P121 to P124 and other than ports (excluding $\overline{\text{RESET}}$ and FLMD0 pins))	–	–
EV_{SS0}	–	Ground potential for ports (other than P20 to P27, P121 to P124, and P150 to P153), and $\overline{\text{RESET}}$ and FLMD0 pins	–	–
AV_{SS}	–	Ground potential for A/D converter, P20 to P27, and P150 to P153. Use this pin with the same potential as EV_{SS0} and V_{SS}.	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

Note SO40 and RxD4 are only mounted in the μPD78F1027 and 78F1028.

3.1.2 78K0R/KG3-L

(1) Port functions (1/3): 78K0R/KG3-L

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 7-bit I/O port. Input of P03 and P04 can be set to TTL input buffer. Output of P02 to P04 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI00
P01				TO00
P02				SO10/TxD1
P03				SI10/RxD1/SDA10
P04				$\overline{SCK10}$/SCL10
P05, P06				–
P10	I/O	Port 1. 8-bit I/O port. Input of P10 and P11 can be set to TTL input buffer. Output of P10 and P12 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK00}$
P11				SI00/RxD0
P12				SO00/TxD0
P13				TxD3
P14				RxD3
P15				RTCDIV/RTCCL
P16				TI01/TO01/INTP5
P17				TI02/TO02
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
P30	I/O	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	RTC1HZ/INTP3
P31				TI03/TO03/INTP4
P40[Note]	I/O	Port 4. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P42				TI04/TO04
P43				$\overline{SCK01}$
P44				SI01
P45				SO01
P46				INTP1/TI05/TO05
P47				INTP2

Note If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally (see **Caution** in **3.2.5 P40 to P47 (port 4)**).

(1) Port functions (2/3): 78K0R/KG3-L

Function Name	I/O	Function	After Reset	Alternate Function
P50	I/O	Port 5. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK40}$ Note
P51				SI40/RxD4 Note
P52				SO40/TxD4 Note
P53				$\overline{SCK41}$ Note
P54				SI41 Note
P55				SO41 Note
P56				–
P57				–
P60	I/O	Port 6. 8-bit I/O port. Output of P60 to P63 can be set to N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units. For only P64 to P67, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCL0
P61				SDA0
P62, P63				–
P64 to P67				TI10/TO10 to TI13/TO13
P70 to P73	I/O	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0 to KR3
P74 to P77				KR4/INTP8 to KR7/INTP11
P80 to P87	I/O	Port 8. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P91	I/O	Port 9. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P110, P111	I/O	Port 11. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P130	Output	Port 13. 1-bit output port and 1-bit I/O port. For only P131, use of an on-chip pull-up resistor can be specified by a software setting.	Output port	–
P131	I/O		Input port	TI06/TO06

Note $\overline{SCK40}$, $\overline{SCK41}$, SI40, SI41, SO40, SO41, TxD4, RxD4 are only mounted in the μPD78F1027 and 78F1028.

(1) Port functions (3/3): 78K0R/KG3-L

Function Name	I/O	Function	After Reset	Alternate Function
P140	I/O	Port 14. 6-bit I/O port. Input of P142 and P143 can be set to TTL input buffer. Output of P142 to P144 can be set to the N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0/INTP6
P141				PCLBUZ1/INTP7
P142				$\overline{SCK20}$/SCL20
P143				SI20/RxD2/SDA20
P144				SO20/TxD2
P145				TI07/TO07
P150 to P157	I/O	Port 15. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8 to ANI15

(2) Non-port functions (1/3): 78K0R/KG3-L

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANI8 to ANI15				P150 to P157
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P46/TI05/TO05
INTP2				P47
INTP3				P30/RTC1HZ
INTP4				P31/TI03/TO03
INTP5				P16/TI01/TO01
INTP6				P140/PCLBUZ0
INTP7				P141/PCLBUZ1
INTP8 to INTP11				P74/KR4 to P77/KR7
KR0 to KR3	Input	Key interrupt input	Input port	P70 to P73
KR4 to KR7				P74/INTP8 to P77/INTP11
PCLBUZ0	Output	Clock output/buzzer output	Input port	P140/INTP6
PCLBUZ1				P141/INTP7
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF: target).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz divided frequency) output	Input port	P15/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P15/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P30/INTP3
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P11/SI00
RxD1	Input	Serial data input to UART1	Input port	P03/SI10/SDA10
RxD2	Input	Serial data input to UART2	Input port	P143/SI20/SDA20
RxD3	Input	Serial data input to UART3	Input port	P14
RxD4Note	Input	Serial data input to UART4	Input port	P51/SI40Note
$\overline{\text{SCK00}}$	I/O	Clock input/output for CSI00, CSI01, CSI10, CSI20, CSI40, and CSI41	Input port	P10
$\overline{\text{SCK01}}$				P43
$\overline{\text{SCK10}}$				P04/SCL10
$\overline{\text{SCK20}}$				P142/SCL20
$\overline{\text{SCK40}}$Note				P50
$\overline{\text{SCK41}}$Note				P53
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P04/$\overline{\text{SCK10}}$
SCL20	I/O	Clock input/output for simplified I^2C	Input port	P142/$\overline{\text{SCK20}}$

Note $\overline{\text{SCK40}}$, $\overline{\text{SCK41}}$, SI40, RxD4 are only mounted in the μ PD78F1029 and 78F1030.

(2) Non-port functions (2/3): 78K0R/KG3-L

Function Name	I/O	Function	After Reset	Alternate Function
SDA0	I/O	Serial data I/O for I^2C	Input port	P61
SDA10	I/O	Serial data I/O for simplified I^2C	Input port	P03/SI10/RxD1
SDA20	I/O	Serial data I/O for simplified I^2C	Input port	P143/SI20/RxD2
SI00	Input	Serial data input to CSI00, CSI01, CSI10, CSI20, CSI40, and CSI41	Input port	P11/RxD0
SI01				P44
SI10				P03/RxD1/SDA10
SI20				P143/RxD2/SDA20
SI40Note				P51/RxD4Note
SI41Note				P54
SO00	Output	Serial data output from CSI00, CSI01, CSI10, CSI20, CSI40, and CSI41	Input port	P12/TxD0
SO01				P45
SO10				P02/TxD1
SO20				P144/TxD2
SO40Note				P52/TxD4Note
SO41Note				P55
TI00	Input	External count clock input to 16-bit timer 00	Input port	P00
TI01		External count clock input to 16-bit timer 01		P16/TO01/INTP5
TI02		External count clock input to 16-bit timer 02		P17/TO02
TI03		External count clock input to 16-bit timer 03		P31/TO03/INTP4
TI04		External count clock input to 16-bit timer 04		P42/TO04
TI05		External count clock input to 16-bit timer 05		P46/INTP1/TO05
TI06		External count clock input to 16-bit timer 06		P131/TO06
TI07		External count clock input to 16-bit timer 07		P145/TO07
TI10		External count clock input to 16-bit timer 10		P64/TO10
TI11		External count clock input to 16-bit timer 11		P65/TO11
TI12		External count clock input to 16-bit timer 12		P66/TO12
TI13		External count clock input to 16-bit timer 13		P67/TO13
TO00	Output	16-bit timer 00 output	Input port	P01
TO01		16-bit timer 01 output		P16/TI01/INTP5
TO02		16-bit timer 02 output		P17/TI02
TO03		16-bit timer 03 output		P31/TI03/INTP4
TO04		16-bit timer 04 output		P42/TI04
TO05		16-bit timer 05 output		P46/INTP1/TI05
TO06		16-bit timer 06 output		P131/TI06
TO07		16-bit timer 07 output		P145/TI07
TO10		16-bit timer 10 output		P64/TI10
TO11		16-bit timer 11 output		P65/TI11
TO12		16-bit timer 12 output		P66/TI12
TO13		16-bit timer 13 output		P67/TI13

Note SI40, SI41, SO40, SO41, TxD4, and RxD4 are only mounted in the μPD78F1029 and 78F1030.

(2) Non-port functions (3/3): 78K0R/KG3-L

Function Name	I/O	Function	After Reset	Alternate Function
TxD0	Output	Serial data output from UART0	Input port	P12/SO00
TxD1		Serial data output from UART1		P02/SO10
TxD2		Serial data output from UART2		P144/SO20
TxD3		Serial data output from UART3		P13
TxD4[Note]		Serial data output from UART4		P52/SO40[Note]
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
EXCLK	Input	External clock input for main system clock	Input port	P122/X2
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124
V_{DD}	–	Positive power supply (P121 to P124 and other than ports (excluding $\overline{RESET}$ and FLMD0 pins))	–	–
EV_{DD0}, EV_{DD1}	–	Positive power supply for ports (other than P20 to P27, P121 to P124, P150 to P157), and $\overline{RESET}$ and FLMD0 pins	–	–
AV_{REF}	–	• A/D converter reference voltage input • Positive power supply for P20 to P27, P150 to P157, and A/D converter	–	–
V_{SS}	–	Ground potential (P121 to P124 and other than ports (excluding $\overline{RESET}$ and FLMD0 pins))	–	–
EV_{SS0}, EV_{SS1}	–	Ground potential for ports (other than P20 to P27, P121 to P124, and P150 to P157), and $\overline{RESET}$ and FLMD0 pins	–	–
AV_{SS}	–	Ground potential for A/D converter, P20 to P27, and P150 to P157. Use this pin with the same potential as EV_{SS0}, EV_{SS1}, and V_{SS}.	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

Note SO40 and TxD4 are only mounted in the μPD78F1029 and 78F1030.

3.2 Description of Pin Functions

Remark The pins mounted depend on the product. See **1.4 Pin Configuration (Top View)** and **3.1 Pin Function List**.

3.2.1 P00 to P06 (port 0)

P00 to P06 function as an I/O port. These pins also function as timer I/O, serial interface data I/O, and clock I/O.

Input to the P03 and P04 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units, using port input mode register 0 (PIM0).

Output from the P02 to P04 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units, using port output mode register 0 (POM0).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P00/TI00	–[Note 1]	√
P01/TO00	–[Note 1]	√
P02/SO10/TxD1	√	√
P03/SI10/RxD1/SDA10	√	√
P04/$\overline{SCK10}$/SCL10	√	√
P05/TI05/TO05	√	P05[Note 2]
P06/TI06/TO06	√	P06[Note 2]

Notes 1. TI00 and TO00 are shared with P53 and P52, respectively, in the 78K0R/KF3-L.

2. TI05/TO05 and TI06/TO06 are shared with P46 and P131, respectively, in the 78K0R/KG3-L.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P00 to P06 function as an I/O port. P00 to P06 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00 to P04 function as timer I/O, serial interface data I/O, and clock I/O.

(a) TI00, TI05, and TI06

There are the pins for inputting an external count clock/capture trigger to 16-bit timers 00, 05, and 06.

(b) TO00, TO05, and TO06

These are the timer output pins of 16-bit timers 00, 05, and 06.

(c) SI10

This is a serial data input pin of serial interface CSI10.

(d) SO10

This is a serial data output pin of serial interface CSI10.

(e) $\overline{\text{SCK10}}$

This is a serial clock I/O pin of serial interface CSI10.

(f) TxD1

This is a serial data output pin of serial interface UART1.

(g) RxD1

This is a serial data input pin of serial interface UART1.

(h) SDA10

This is a serial data I/O pin of serial interface for simplified I^2C.

(i) SCL10

This is a serial clock I/O pin of serial interface for simplified I^2C.

Caution To use P02/SO10/TxD1 and P04/$\overline{\text{SCK10}}$/SCL10 as general-purpose ports, set serial communication operation setting register 02 (SCR02) to the default status (0087H). In addition, clear port output mode register 0 (POM0) to 00H.

3.2.2 P10 to P17 (port 1)

P10 to P17 function as an I/O port. These pins also function as external interrupt request input, serial interface data I/O, clock I/O, timer I/O, and real-time counter clock output.

Input to the P10 and P11 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units, using port input mode register 1 (PIM1).

Output from the P10 and P12 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units, using port output mode register 1 (POM1).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P10/$\overline{\text{SCK00}}$	√	√
P11/SI00/RxD0	√	√
P12/SO00/TxD0	√	√
P13/TxD3	√	√
P14/RxD3	√	√
P15/RTCDIV/RTCCL	√	√
P16/TI01/TO01/INTP5	√	√
P17/TI02/TO02	√	√

The following operation modes can be specified in 1-bit units.

(1) Port mode

P10 to P17 function as an I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

(2) Control mode

P10 to P17 function as external interrupt request input, serial interface data I/O, clock I/O, timer I/O, and real-time counter clock output.

(a) SI00

This is a serial data input pin of serial interface CSI00.

(b) SO00

This is a serial data output pin of serial interface CSI00.

(c) $\overline{\text{SCK00}}$

This is a serial clock I/O pin of serial interface CSI00.

(d) RxD0, RxD3

These are the serial data input pins of serial interface UART0 and UART3.

(e) TxD0, TxD3

These are the serial data output pins of serial interface UART0 and UART3.

(f) TI01, TI02

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 01 and 02.

(g) TO01, TO02

These are the timer output pins of 16-bit timers 01 and 02.

(h) INTP5

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(i) RTCDIV

This is a real-time counter clock (32 kHz, divided) output pin.

(j) RTCCL

This is a real-time counter clock (32 kHz, original oscillation) output pin.

Cautions 1. To use P10/$\overline{\text{SCK00}}$ and P12/SO00/TxD0 as general-purpose ports, set serial communication operation setting register 00 (SCR00) to the default status (0087H).

2. Do not enable outputting RTCCL and RTCDIV at the same time.

3.2.3 P20 to P27 (port 2)

P20 to P27 function as an I/O port. These pins also function as A/D converter analog input.

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P20/ANI0	√	√
P21/ANI1	√	√
P22/ANI2	√	√
P23/ANI3	√	√
P24/ANI4	√	√
P25/ANI5	√	√
P26/ANI6	√	√
P27/ANI7	√	√

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P27 function as an I/O port. P20 to P27 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P27 function as the A/D converter analog input pins (ANI0 to ANI7). When using these pins as the analog input pins, see **13.6 (5) ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI15/P157**.

Caution ANI0/P20 to ANI7/P27 are set in the digital input (general-purpose port) mode after release of reset.

3.2.4 P30, P31 (port 3)

P30 and P31 function as an I/O port. These pins also function as external interrupt request input, timer I/O, and real-time counter correction clock output.

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P30/RTC1HZ/INTP3	√	√
P31/TI03/TO03/INTP4	√	√

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 and P31 function as an I/O port. P30 and P31 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 and P31 function as external interrupt request input, timer I/O, and real-time counter correction clock output.

(a) INTP3, INTP4

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TI03

This is a pin for inputting an external count clock/capture trigger to 16-bit timer 03.

(c) TO03

This is a timer output pin from 16-bit timer 03.

(d) RTC1HZ

This is a real-time counter correction clock (1 Hz) output pin.

3.2.5 P40 to P47 (port 4)

P40 to P47 function as an I/O port. These pins also function as external interrupt request input, serial interface data I/O, clock I/O, data I/O for a flash memory programmer/debugger, clock output, and timer I/O.

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P40/TOOL0	√	√
P41/TOOL1	√	√
P42/TI04/TO04	√	√
P43/$\overline{\text{SCK01}}$	√	√
P44/SI01	√	√
P45/SO01	√	√
P46/INTP1/TI05/TO05	P46 Note 1	√
P47/INTP2	P47 Note 2	√

Notes 1. INTP1 and TI05/TO05 are shared with P50 and P05, respectively, in the 78K0R/KF3-L.

2. INTP2 is shared with P51, in the 78K0R/KF3-L.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P40 to P47 function as an I/O port. P40 to P47 can be set to input or output port in 1-bit units using port mode register 4 (PM4). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 4 (PU4).

Be sure to connect an external pull-up resistor to P40 when on-chip debugging is enabled (by using an option byte).

(2) Control mode

P40 to P47 function as serial interface data I/O, clock I/O, external interrupt request input, data I/O for a flash memory programmer/debugger, clock output, and timer I/O.

(a) INTP1, INTP2

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TOOL0

This is a data I/O pin for a flash memory programmer/debugger.

Be sure to pull up this pin externally when on-chip debugging is enabled (pulling it down is prohibited).

(c) TOOL1

This is a clock output pin for a debugger.

When the on-chip debug function is used, the P41/TOOL1 pin can be used as follows by the mode setting on the debugger.

1-line mode: can be used as a port (P41).

2-line mode: used as a TOOL1 pin and cannot be used as a port (P41).

(d) TI04, TI05

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 04 and 05.

(e) TO04, TO05

These are the timer output pins from 16-bit timers 04 and 05.

(f) $\overline{\text{SCK01}}$

This is a serial clock I/O pin of serial interface CSI01.

(g) SI01

This is a serial data input pin of serial interface CSI01.

(h) SO01

This is a serial data output pin of serial interface CSI01.

Caution The function of the P40/TOOL0 pin varies as described in (a) to (c) below.
In the case of (b) or (c), make the specified connection.

(a) In normal operation mode and when on-chip debugging is disabled (OCDENSET = 0) by an option byte (000C3H)
=> Use this pin as a port pin (P40).

(b) In normal operation mode and when on-chip debugging is enabled (OCDENSET = 1) by an option byte (000C3H)
=> Connect this pin to EV_{DD0} or EV_{DD1} via an external resistor, and always input a high level to the pin before reset release.

(c) When on-chip debug function is used, or in write mode of flash memory programmer
=> Use this pin as TOOL0.
Directly connect this pin to the on-chip debug emulator or a flash memory programmer, or pull it up by connecting it to EV_{DD0} or EV_{DD1} via an external resistor.

3.2.6 P50 to P57 (port 5)

P50 to P57 function as an I/O port. These pins also function as serial interface data I/O, clock I/O, external interrupt request input, timer I/O, and clock/buzzer output.

<In case of the μPD78F1010, 78F1011, 78F1012, 78F1013, 78F1014>

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14)
P50/INTP1	√	P50 Note
P51/INTP2	√	P51 Note
P52/TO00	√	P52 Note
P53/TI00	√	P53 Note
P54/TI07/TO07	√	P54 Note
P55/PCLBUZ1/INTP7	√	P55 Note
P56	–	√
P57	–	√

Note The following pins are shared in the 78K0R/KG3-L.

- P46/INTP1
- P47/INTP2
- P01/TO00
- P00/TI00
- P145/TI07/TO07
- P141/PCLBUZ1/INTP7

<In case of the μPD78F1027, 78F1028, 78F1029, 78F1030>

	78K0R/KF3-L (μPD78F10xx: xx = 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 29, 30)
P50/$\overline{\text{SCK40}}$/INTP1	√	P50/$\overline{\text{SCK40}}$ Note
P51/SI40/RxD4/INTP2	√	P51/SI40/RxD4 Note
P52/SO40/TO00/TxD4	√	P52/SO40/TxD4 Note
P53/$\overline{\text{SCK41}}$/TI00	√	P53/$\overline{\text{SCK41}}$ Note
P54/SI41/TI07/TO07	√	P54/SI41 Note
P55/PCLBUZ1/SO41/ INTP7	√	P55/SO41 Note
P56	–	√
P57	–	√

Note The following pins are shared in the 78K0R/KG3-L.

- P46/INTP1
- P47/INTP2
- P01/TO00
- P00/TI00
- P145/TI07/TO07
- P141/PCLBUZ1/INTP7

The following operation modes can be specified in 1-bit units.

(1) Port mode

P50 to P57 function as an I/O port. P50 to P57 can be set to input or output port in 1-bit units using port mode register 5 (PM5). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 5 (PU5).

(2) Control mode

P50 to P57 function as serial interface data I/O, clock I/O, external interrupt request input, timer I/O, and clock/buzzer output.

(a) INTP1, INTP2, INTP7

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TI00, TI07

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 00 and 07.

(c) TO00, TO07

These are the timer output pins of 16-bit timers 00 and 07.

(d) PCLBUZ1

This is a clock/buzzer output pin.

(e) SI40, SI41

These are the serial data input pins of serial interface CSI40 and CSI41.

(f) SO40, SO41

These are the serial data output pin of serial interface CSI40 and CSI41.

(g) $\overline{\text{SCK40}}$, $\overline{\text{SCK41}}$

These are the serial clock I/O pins of serial interface CSI40 and CSI41.

(h) RxD4

This is a serial data input pin of serial interface UART4.

(i) TxD4

This is a serial data output pins of serial interface UART4.

3.2.7 P60 to P67 (port 6)

P60 to P67 function as an I/O port. These pins also function as serial interface data I/O, clock I/O, and timer I/O.

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P60/SCL0	√	√
P61/SDA0	√	√
P62	√	√
P63	√	√
P64/TI10/TO10	√	√
P65/TI11/TO11	√	√
P66/TI12/TO12	√	√
P67/TI13/TO13	√	√

The following operation modes can be specified in 1-bit units.

(1) Port mode

P60 to P67 function as an I/O port. P60 to P67 can be set to input port or output port in 1-bit units using port mode register 6 (PM6). Only for P64 to P67, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 6 (PU6).

Output of P60 to P63 is N-ch open-drain output (6 V tolerance).

(2) Control mode

P60 and P61 and P64 to P67 function as serial interface data I/O, clock I/O, and timer I/O.

(a) SDA0

This is a serial data I/O pin of serial interface IICA.

(b) SCL0

This is a serial clock I/O pin of serial interface IICA.

(c) TI10 to TI13

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 10 to 13.

(d) TO10 to TO13

These are the timer output pins of 16-bit timers 10 to 13.

3.2.8 P70 to P77 (port 7)

P70 to P77 function as an I/O port. These pins also function as key interrupt input and external interrupt request input.

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P70/KR0	√	√
P71/KR1	√	√
P72/KR2	√	√
P73/KR3	√	√
P74/KR4/INTP8	√	√
P75/KR5/INTP9	√	√
P76/KR6/INTP10	√	√
P77/KR7/INTP11	√	√

The following operation modes can be specified in 1-bit units.

(1) Port mode

P70 to P77 function as an I/O port. P70 to P77 can be set to input or output port in 1-bit units using port mode register 7 (PM7). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 7 (PU7).

(2) Control mode

P70 to P77 function as key interrupt input, and external interrupt request input.

(a) KR0 to KR7

These are the key interrupt input pins.

(b) INTP8 to INTP11

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

3.2.9 P80 to P87 (port 8)

P80 to P87 function as an I/O port.

P80 to P87 can be set to input or output port in 1-bit units using port mode register 8 (PM8). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 8 (PU8).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P80	–	√
P81	–	√
P82	–	√
P83	–	√
P84	–	√
P85	–	√
P86	–	√
P87	–	√

3.2.10 P90, P91 (port 9)

P90 and P91 function as an I/O port.

P90 and P91 can be set to input or output port in 1-bit units using port mode register 9 (PM9). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 9 (PU9).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P90	√	–
P91	√	√

3.2.11 P110, P111 (port 11)

P110 and P111 function as an I/O port.

P110 and P111 can be set to input or output port in 1-bit units using port mode register 11 (PM11). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 11 (PU11).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P110	√	√
P111	√	√

3.2.12 P120 to P124 (port 12)

P120 function as a 1-bit I/O port. P121 to P124 functions as a 4-bit input port. These pins also function as external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, and external clock input for main system clock.

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P120/INTP0/EXLVI	√	√
P121/X1	√	√
P122/X2/EXCLK	√	√
P123/XT1	√	√
P124/XT2	√	√

The following operation modes can be specified in 1-bit units.

(1) Port mode

P120 functions as a 1-bit I/O port. P120 can be set to input or output port using port mode register 12 (PM12). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P124 functions as a 4-bit input port.

(2) Control mode

P120 to P124 function as external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, and external clock input for main system clock.

(a) INTP0

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) EXLVI

This is a potential input pin for external low-voltage detection.

(c) X1, X2

These are the pins for connecting a resonator for main system clock.

(d) EXCLK

This is an external clock input pin for main system clock.

(e) XT1, XT2

These are the pins for connecting a resonator for subsystem clock.

3.2.13 P130, P131 (port 13)

P130 functions as a 1-bit output port. P131 functions as a 1-bit I/O port. These pins also function as timer I/O.

Remark When the device is reset, P130 outputs a low level. Therefore, to output a high level from P130 before the device is reset, the output signal of P130 can be used as a pseudo reset signal of the CPU (see the figure for **Remark** in **6.2.13 Port 13**).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P130/INTP1	√	√
P131/TI06/TO06	–[Note]	√

Note TI06/TO06 is shared with P06, in the 78K0R/KF3-L.

(1) Port mode

P130 functions as a 1-bit output port.

P131 functions as a 1-bit I/O port. P131 can be set to input or output port using port mode register 13 (PM13). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 13 (PU13).

(2) Control mode

P131 functions as timer I/O.

(a) TI06

This is a pin for inputting an external count clock/capture trigger to 16-bit timer 06.

(b) TO06

This is a timer output pin from 16-bit timer 06.

3.2.14 P140 to P145 (port 14)

P140 to P145 function as an I/O port. These pins also function as timer I/O, external interrupt request input, clock/buzzer output, serial interface data I/O, and clock I/O.

Input to the P142 and P143 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 14 (PIM14).

Output from the P142 to P144 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 14 (POM14).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P140/PCLBUZ0/INTP6	√	√
P141/PCLBUZ1/INTP7	–Note 1	√
P142/$\overline{\text{SCK20}}$/SCL20	√	√
P143/SI20/RxD2/SDA20	√	√
P144/SO20/TxD2	√	√
P145/TI07/TO07	–Note 2	√

Notes 1. PCLBUZ/INTP7 is shared with P55, in the 78K0R/KF3-L.

2. TI07/TO07 is shared with P54, in the 78K0R/KF3-L.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P140 to P145 function as an I/O port. P140 to P145 can be set to input or output port in 1-bit units using port mode register 14 (PM14). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 14 (PU14).

(2) Control mode

P140 to P145 function as timer I/O, external interrupt request input, clock/buzzer output, serial interface data I/O, and clock I/O.

(a) INTP6, INTP7

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) PCLBUZ0, PCLBUZ1

These are the clock/buzzer output pins.

(c) TI07

This is a pin for inputting an external count clock/capture trigger to 16-bit timer 07.

(d) TO07

This is a timer output pin of 16-bit timer 07.

(e) SI20

This is a serial data input pin of serial interface CSI20.

(f) SO20

This is a serial data output pin of serial interface CSI20.

(g) $\overline{\text{SCK20}}$

This is a serial clock I/O pin of serial interface CSI20.

(h) TxD2

This is a serial data output pin of serial interface UART2.

(i) RxD2

This is a serial data input pin of serial interface UART2.

(j) SDA20

This is a serial data I/O pin of serial interface for simplified I^2C.

(k) SCL20

This is a serial clock I/O pin of serial interface for simplified I^2C.

3.2.15 P150 to P157 (port 15)

P150 to P157 function as an I/O port. These pins also function as A/D converter analog input.

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P150/ANI8	√	√
P151/ANI9	√	√
P152/ANI10	√	√
P153/ANI11	√	√
P154/ANI12	–	√
P155/ANI13	–	√
P156/ANI14	–	√
P157/ANI15	–	√

The following operation modes can be specified in 1-bit units.

(1) Port mode

P150 to P157 function as an I/O port. P150 to P157 can be set to input or output port in 1-bit units using port mode register 15 (PM15).

(2) Control mode

P150 to P157 function as the A/D converter analog input pins (ANI8 to ANI15). When using these pins as the analog input pins, see **13.6 (5) ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI15/P157**.

Caution ANI8/P150 to ANI15/P157 are set in the digital input (general-purpose port) mode after release of reset.

3.2.16 AV_{REF}, AV_{SS}, V_{DD}, EV_{DD0}, EV_{DD1}, V_{SS}, EV_{SS0}, EV_{SS1}

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
AV_{REF}	√	√
AV_{SS}	√	√
V_{DD}	√	√
EV_{DD0}	√	√
EV_{DD1}	–	√
V_{SS}	√	√
EV_{SS0}	√	√
EV_{SS1}	–	√

(1) AV_{REF}

This is the A/D converter reference voltage input pin and the positive power supply pin of P20 to P27, P150 to P157, and A/D converter.

When all pins of ports 2 and 15 are used as the analog port pins, make the potential of AV_{REF} be such that 1.8 V ≤ AV_{REF} ≤ V_{DD}. When one or more of the pins of ports 2 and 15 are used as the digital port pins or when the A/D converter is not used, make AV_{REF} the same potential as EV_{DD0}, EV_{DD1}, and V_{DD}.

(2) AV_{SS}

This is the ground potential pin of A/D converter, P20 to P27, and P150 to P157. Even when the A/D converter is not used, always use this pin with the same potential as EV_{SS0}, EV_{SS1}, and V_{SS}.

(3) V_{DD}, EV_{DD0}, EV_{DD1}

V_{DD} is the positive power supply pin for P121 to P124 and pins other than ports (excluding the $\overline{\text{RESET}}$ and FLMD0 pins).

EV_{DD0} and EV_{DD1} are the positive power supply pins for ports other than P20 to P27, P121 to P124, and P150 to P157 as well as for the $\overline{\text{RESET}}$ and FLMD0 pins.

(4) V_{SS}, EV_{SS0}, EV_{SS1}

V_{SS} is the ground potential pin for P121 to P124 and pins other than ports (excluding the $\overline{\text{RESET}}$ and FLMD0 pins).

EV_{SS0} and EV_{SS1} are the ground potential pins for ports other than P20 to P27, P121 to P124, and P150 to P157 as well as for the $\overline{\text{RESET}}$ and FLMD0 pins.

3.2.17 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

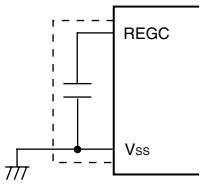
When the external reset pin is not used, connect this pin directly or via a resistor to EV_{DD0} or EV_{DD1}.

When the external reset pin is used, design the circuit based on V_{DD}.

3.2.18 REGC

This is the pin for connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF: target).

Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

3.2.19 FLMD0

This is a pin for setting flash memory programming mode.

Perform either of the following processing.

(a) In normal operation mode

It is recommended to leave this pin open during normal operation.

The FLMD0 pin must always be kept at the V_{SS} level before reset release but does not have to be pulled down externally because it is internally pulled down by reset. However, pulling it down must be kept selected (i.e., FLMDPUP = “0”, default value) by using bit 7 (FLMDPUP) of the background event control register (BECTL) (see **26.5 (1) Back ground event control register**). To pull it down externally, use a resistor of 200 kΩ or smaller.

Self programming and the rewriting of flash memory with the programmer can be prohibited using hardware, by directly connecting this pin to the V_{SS} pin.

(b) In self programming mode

It is recommended to leave this pin open when using the self programming function. To pull it down externally, use a resistor of 100 kΩ to 200 kΩ.

In the self programming mode, the setting is switched to pull up in the self programming library.

(c) In flash memory programming mode

Directly connect this pin to a flash memory programmer when data is written by the flash memory programmer. This supplies a writing voltage of the V_{DD} level to the FLMD0 pin.

The FLMD0 pin does not have to be pulled down externally because it is internally pulled down by reset. To pull it down externally, use a resistor of 1 kΩ to 200 kΩ.

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

3.3.1 78K0R/KF3-L

Table 3-3 shows the types of pin I/O circuits and the recommended connections of unused pins. For I/O Circuit Type, see **Figure 3-1. Pin I/O Circuit List**.

Table 3-3. Connection of Unused Pins (1/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P02/SO10/TxD1	5-AG	I/O	Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P03/SI10/RxD1/SDA10	5-AN		
P04/$\overline{SCK10}$/SCL10			
P05/TI05/TO05	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P06/TI06/TO06			
P10/$\overline{SCK00}$	5-AN		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P11/SI00/RxD0			Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P12/SO00/TxD0	5-AG		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P13/TxD3			Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P14/RxD3	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P15/RTCDIV/RTCCL	5-AG		
P16/TI01/TO01/INTP5	8-R		
P17/TI02/TO02			
P20/ANI0 to P27/ANI7[Note]	11-G		Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open.
P30/RTC1HZ/INTP3	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P31/TI03/TO03/INTP4			
P40/TOOL0			<When on-chip debugging is enabled> Pull this pin up (pulling it down is prohibited). <When on-chip debugging is disabled> Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.

Note P20/ANI0 to P27/ANI7 are set in the digital input port mode after release of reset.

Table 3-3. Connection of Unused Pins (2/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P41/TOOL1	5-AG	I/O	Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P42/TI04/TO04	8-R		
P43/$\overline{SCK01}$			
P44/SI01			
P45/SO01	5-AG		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P46, P47	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P50/$\overline{SCK40}$/INTP1			
P51/SI40/RxD4/INTP2			
P52/SO40/TO00/TxD4	5-AG		
P53/$\overline{SCK41}$/TI00	8-R		
P54/SI41/TI07/TO07			
P55/PCLBUZ1/SO41/INTP7			
P60/SCL0	13-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor, or connect directly to EV_{SS0}. Output: Set the port output latch to 0 and leave open with low level out put.
P61/SDA0			
P62			
P63	13-P		
P64/TI10/TO10	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P65/TI11/TO11			
P66/TI12/TO12			
P67/TI13/TO13			
P70/KR0 to P73//KR3			
P74/KR4/INTP8 to P77/KR7/INTP11			
P90, P91	5-AG		
P110	8-R		
P111	5-AG		
P120/INTP0/EXLVI	8-R		

Table 3-3. Connection of Unused Pins (3/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P121/X1[Note 1]	37-C	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P122/X2/EXCLK[Note 1]			
P123/XT1[Note 1]	37-B		
P124/XT2[Note 1]			
P130	3-C	Output	Leave open.
P140/PCLBUZ0/ITNP6	8-R	I/O	Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P142/$\overline{SCK20}$/SCL20	5-AN		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P143/SI20/RxD2/SDA20			
P144/SO20/TxD2	5-AG		<When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P150/ANI8 to P153/ANI11 [Note 2]	11-G		Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open.
AV_{REF}	–	–	<When one or more of P20 to P27 and P150 to P153 are set as a digital port> Make this pin the same potential as EV_{DD0} or V_{DD}. <When all of P20 to P27 and P150 to P153 are set as analog ports> Make this pin to have a potential where 1.8 V ≤ AV_{REF} ≤ V_{DD}.
AV_{SS}	–	–	Make this pin the same potential as EV_{SS0} or V_{SS}.
FLMD0	2-W	–	Leave open or connect to V_{SS} via a resistor of 100 kΩ or more.
$\overline{RESET}$	2	Input	Connect directly or via a resistor to EV_{DD0}.
REGC	–	–	Connect to V_{SS} via capacitor (0.47 to 1 μF).

Notes 1. Use recommended connection above in input port mode (see **Figure 7-3 Format of Clock Operation Mode Control Register (CMC)**) when these pins are not used.

2. P150/ANI8 to P153/ANI11 are set in the digital input port mode after release of reset.

3.3.2 78K0R/KG3-L

Table 3-4 shows the types of pin I/O circuits and the recommended connections of unused pins. For I/O Circuit Type, see **Figure 3-1. Pin I/O Circuit List**.

Table 3-4. Connection of Unused Pins (1/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI00	8-R	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P01/TO00	5-AG		
P02/SO10/TxD1			Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P03/SI10/RxD1/SDA10	5-AN		
P04/$\overline{SCK10}$/SCL10			<When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P05	8-R		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P06			
P10/$\overline{SCK00}$	5-AN		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P11/SI00/RxD0			Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P12/SO00/TxD0	5-AG		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P13/TxD3			Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P14/RxD3	8-R		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P15/RTCDIV/RTCCL	5-AG		
P16/TI01/TO01/INTP5	8-R		
P17/TI02/TO02			
P20/ANI0 to P27/ANI7[Note]	11-G		Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open.
P30/RTC1HZ/INTP3	8-R		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P31/TI03/TO03/INTP4			

Note P20/ANI0 to P27/ANI7 are set in the digital input port mode after release of reset.

Table 3-4. Connection of Unused Pins (2/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P40/TOOL0	8-R	I/O	<When on-chip debugging is enabled> Pull this pin up (pulling it down is prohibited). <When on-chip debugging is disabled> Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P41/TOOL1	5-AG		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P42/TI04/TO04	8-R		
P43/$\overline{SCK01}$			
P44/SI01			
P45/SO01	5-AG		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P46/TI05/TO05/INTP1	8-R		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P47/INTP2			
P50, P51, P53 to P55			
P50/$\overline{SCK40}$			
P51/SI40/RxD4			
P52/SO40/TxD4	5-AG		
P53/$\overline{SCK41}$	8-R		
P54/SI41			
P55/SO41			
P56	5-AG		
P57			
P60/SCL0	13-R		Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor, or connect directly to EV_{SS0}, EV_{SS1}. Output: Set the port output latch to 0 and leave open with low level out put.
P61/SDA0			
P62			
P63	13-P		
P64/TI10/TO10	8-R		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P65/TI11/TO11			
P66/TI12/TO12			
P67/TI13/TO13			
P70/KR0 to P73//KR3			
P74/KR4/INTP8 to P77/KR7/INTP11			

Table 3-4. Connection of Unused Pins (3/3)

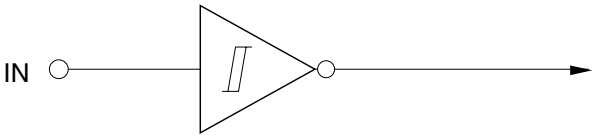
Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P80 to P87	5-AG	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P91			
P110	8-R		
P111	5-AG		
P120/INTP0/EXLVI	8-R		
P121/X1[Note 1]	37-C	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P122/X2/EXCLK[Note 1]			
P123/XT1[Note 1]	37-B		
P124/XT2[Note 1]			
P130	3-C	Output	Leave open.
P131/TI06/TO06	8-R	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P140/PCLBUZ0/ITNP6			
P141/PCLBUZ1/INTP7			
P142/$\overline{SCK20}$/SCL20	5-AN		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P143/SI20/RxD2/SDA20			
P144/SO20/TxD2	5-AG		<When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P145/TI07/TO07	8-R		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P150/ANI8 to P157/ANI15[Note 2]	11-G		Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open.
AV_{REF}	–	–	<When one or more of P20 to P27 and P150 to P157 are set as a digital port> Make this pin the same potential as EV_{DD0}, EV_{DD1}, or V_{DD}. <When all of P20 to P27 and P150 to P157 are set as analog ports> Make this pin to have a potential where 1.8 V ≤ AV_{REF} ≤ V_{DD}.
AV_{SS}	–	–	Make this pin the same potential as EV_{SS0}, EV_{SS1}, or V_{SS}.
FLMD0	2-W	–	Leave open or connect to V_{SS} via a resistor of 100 kΩ or more.
$\overline{RESET}$	2	Input	Connect directly or via a resistor to EV_{DD0} or EV_{DD1}.
REGC	–	–	Connect to V_{SS} via capacitor (0.47 to 1 μF: target).

Notes 1. Use recommended connection above in input port mode (see **Figure 7-3 Format of Clock Operation Mode Control Register (CMC)**) when these pins are not used.

2. P150/ANI8 to P157/ANI15 are set in the digital input port mode after release of reset.

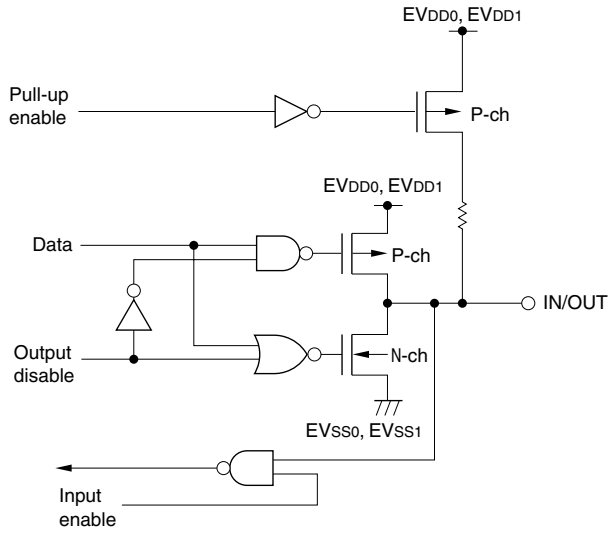
Figure 3-1. Pin I/O Circuit List (1/2)

Type 2

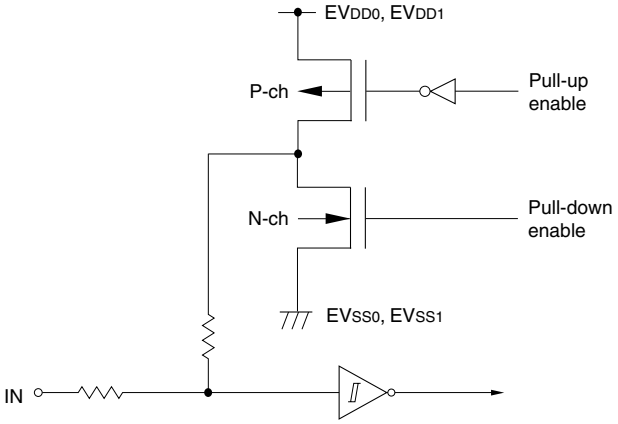


Schmitt-triggered input with hysteresis characteristics

Type 5-AG

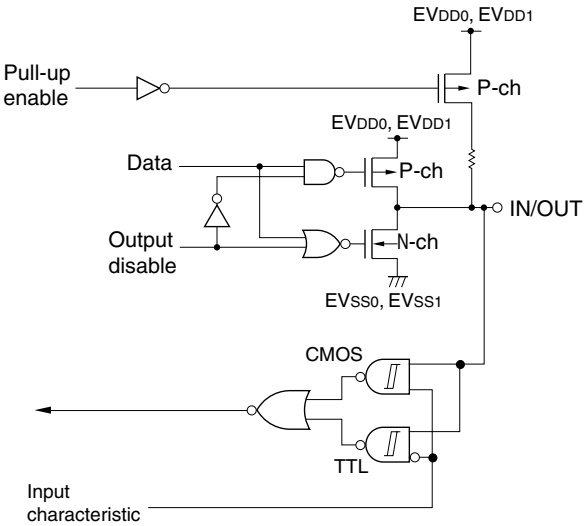


Type 2-W

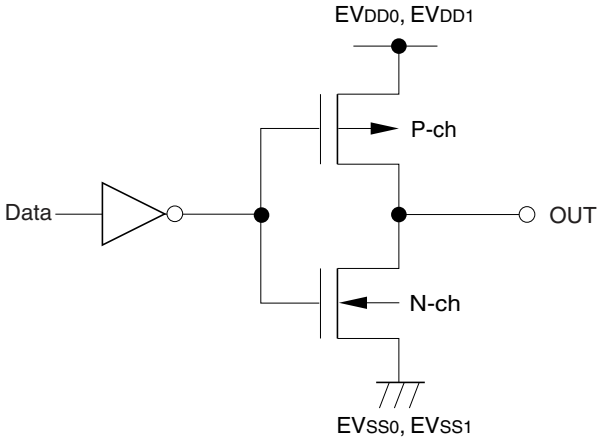


Schmitt-triggered input with hysteresis characteristics

Type 5-AN



Type 3-C



Type 8-R

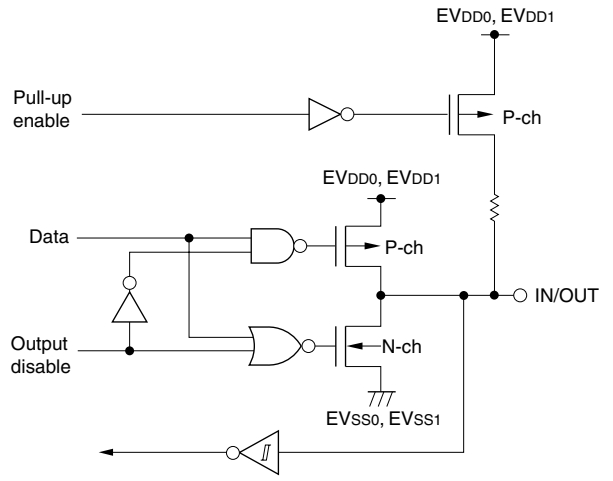
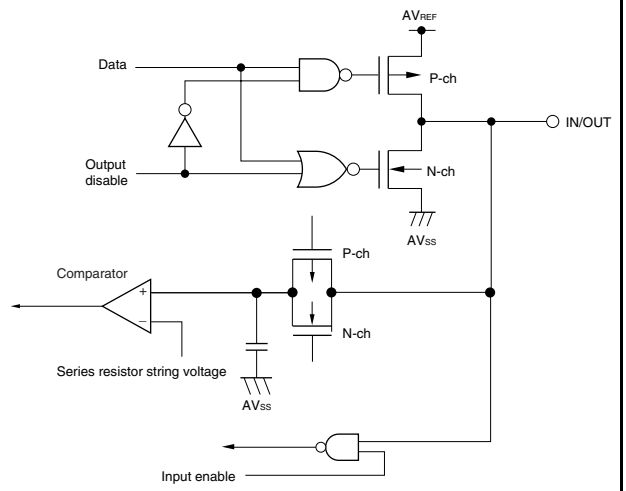
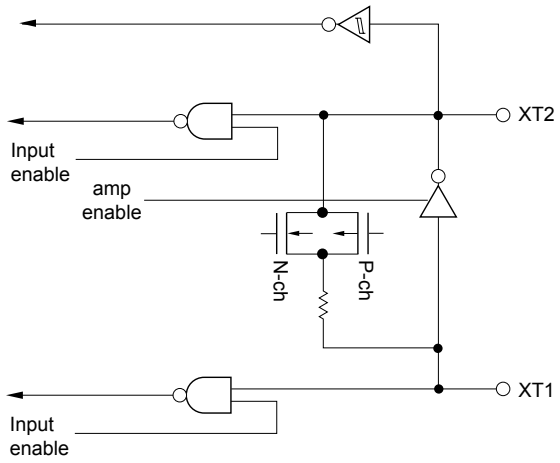


Figure 3-1. Pin I/O Circuit List (2/2)

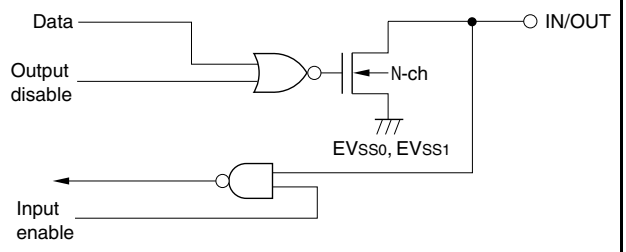
Type 11-G



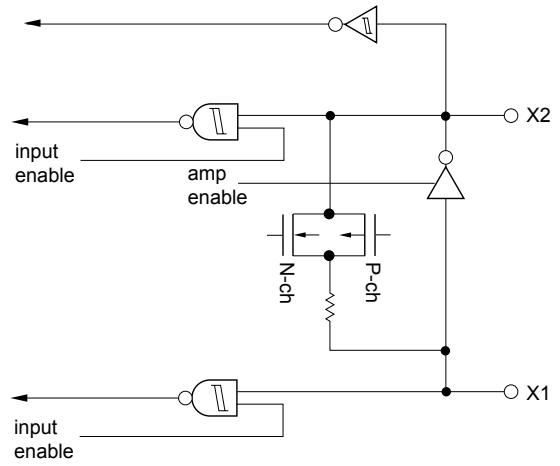
Type 37-B



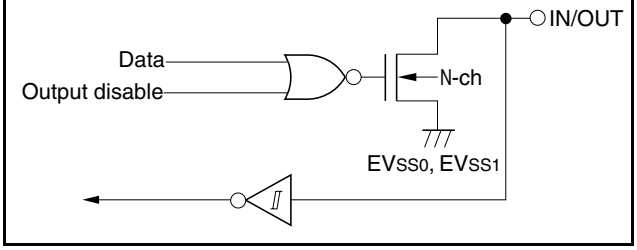
Type 13-P



Type 37-C



Type 13-R

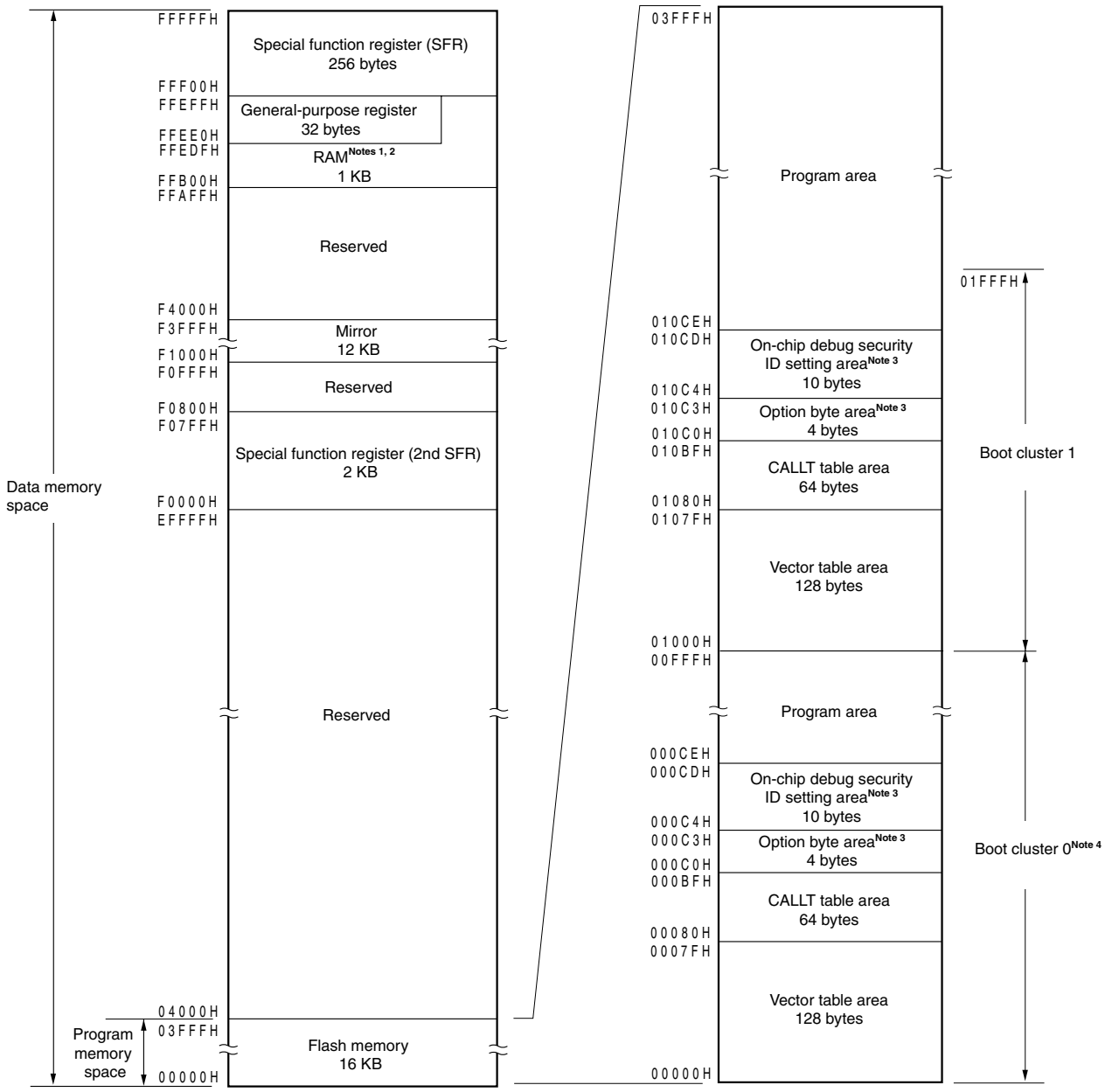


CHAPTER 4 CPU ARCHITECTURE

4.1 Memory Space

Products in the 78K0R/Kx3-L can access a 1 MB memory space. Figures 4-1 to 4-9 show the memory maps.

Figure 4-1. Memory Map (μPD78F1000)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

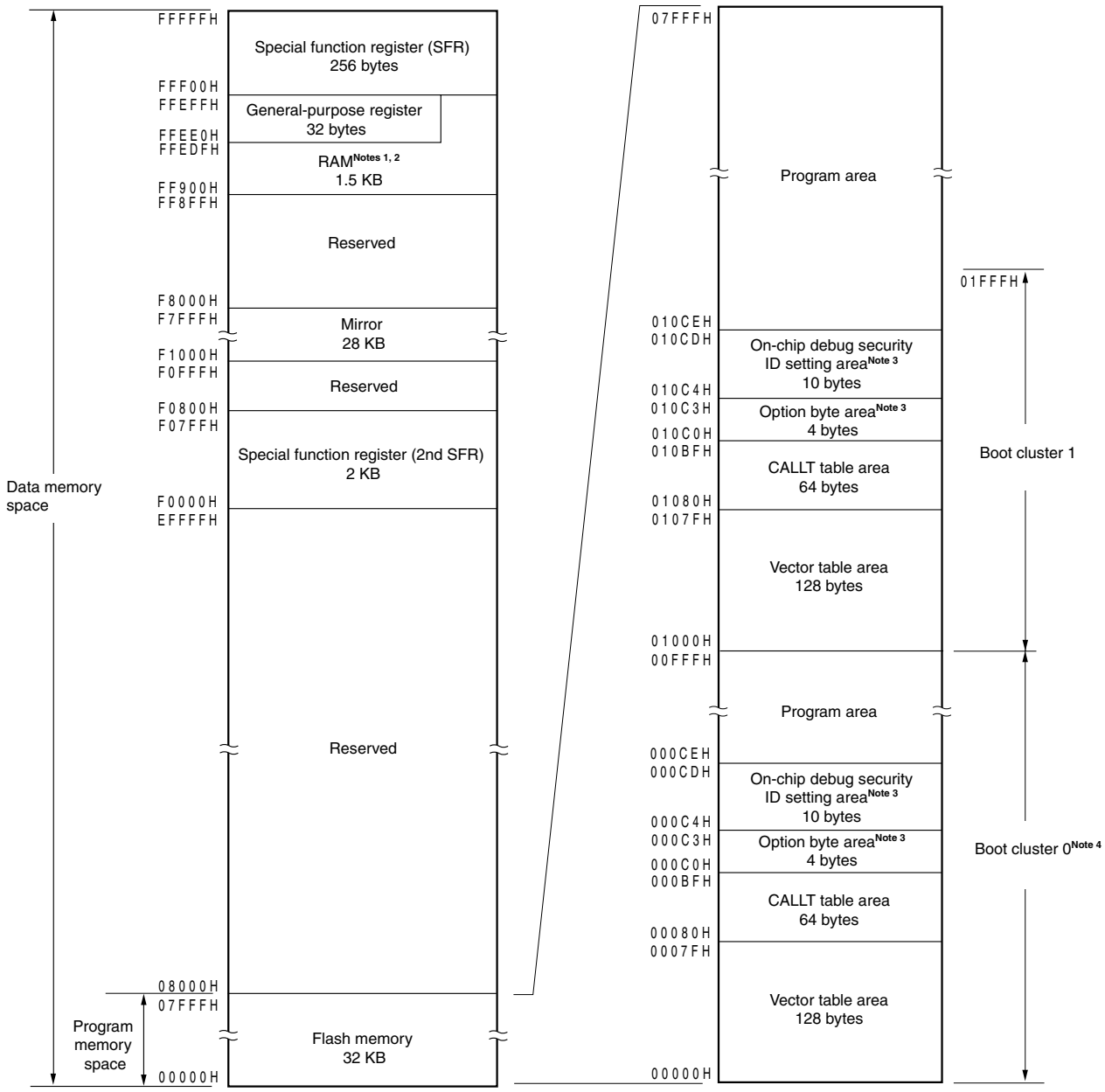
2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Figure 4-2. Memory Map (μPD78F1001, 78F1004, 78F1007)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

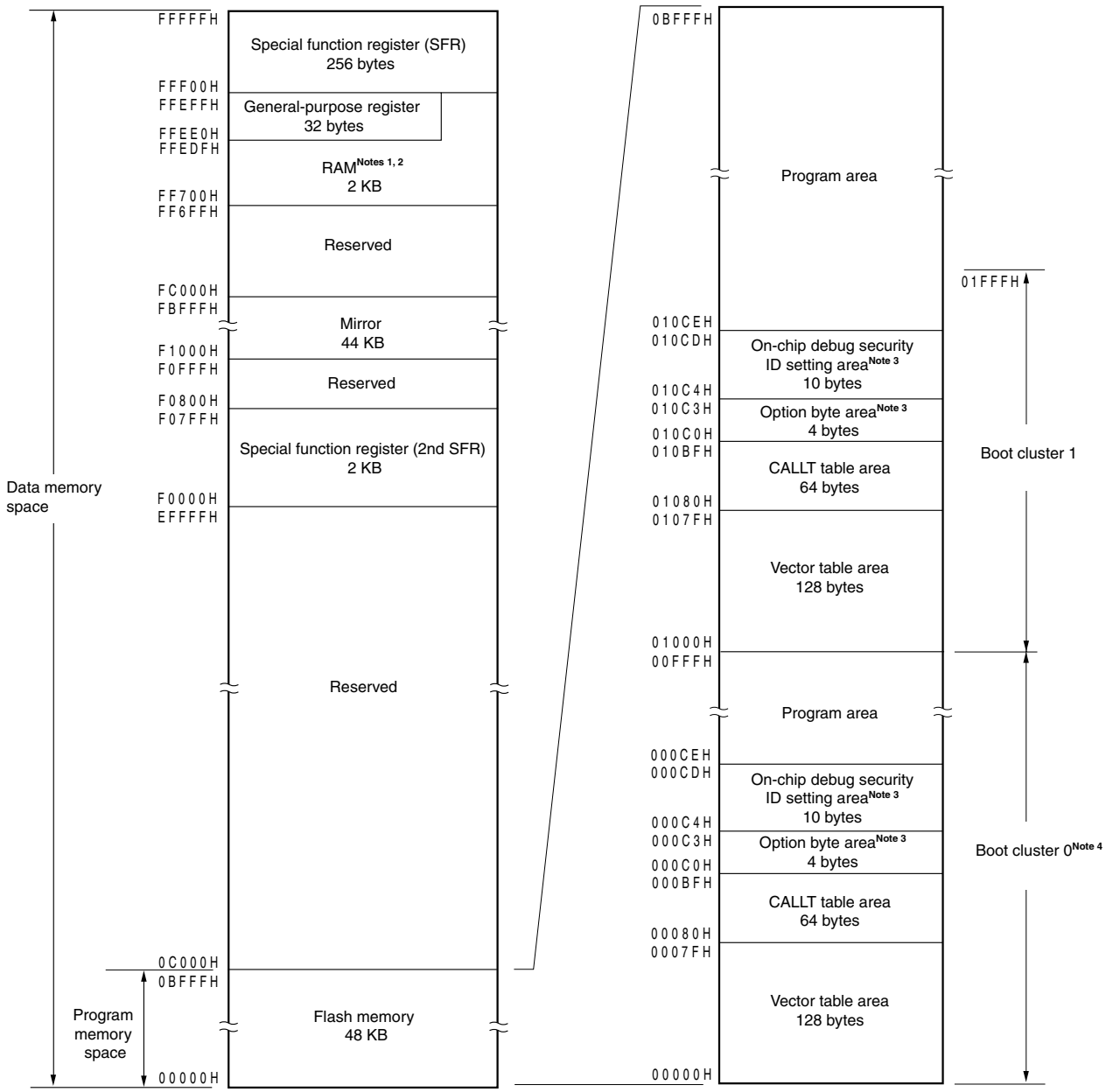
2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Figure 4-3. Memory Map (μPD78F1002, 78F1005, 78F1008)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

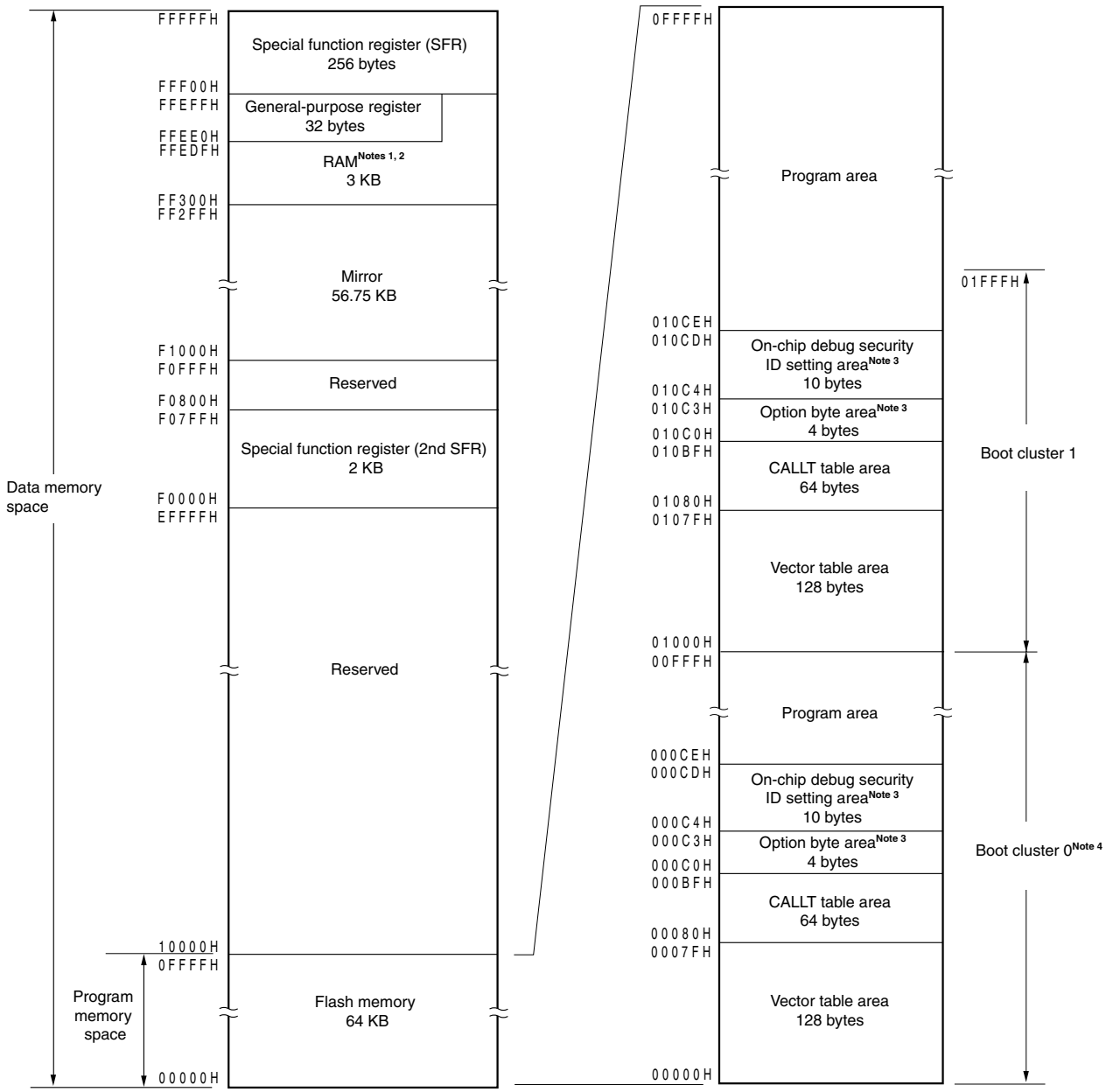
2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Figure 4-4. Memory Map (μPD78F1003, 78F1006, 78F1009)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FF300H to FF6FFH also cannot be used with the μPD78F1003, 78F1006 and 78F1009.

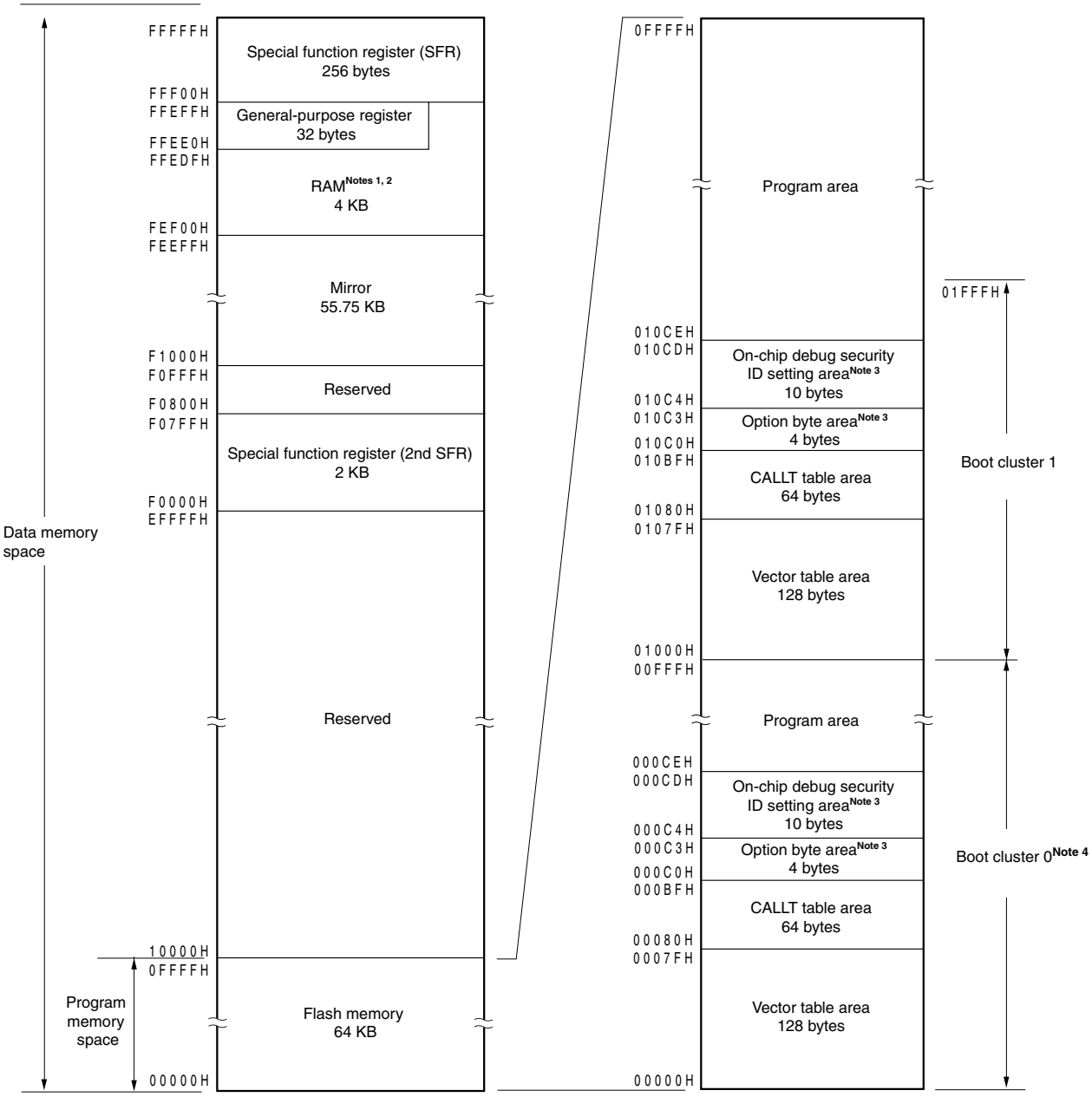
2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Figure 4-5. Memory Map (μPD78F1010)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

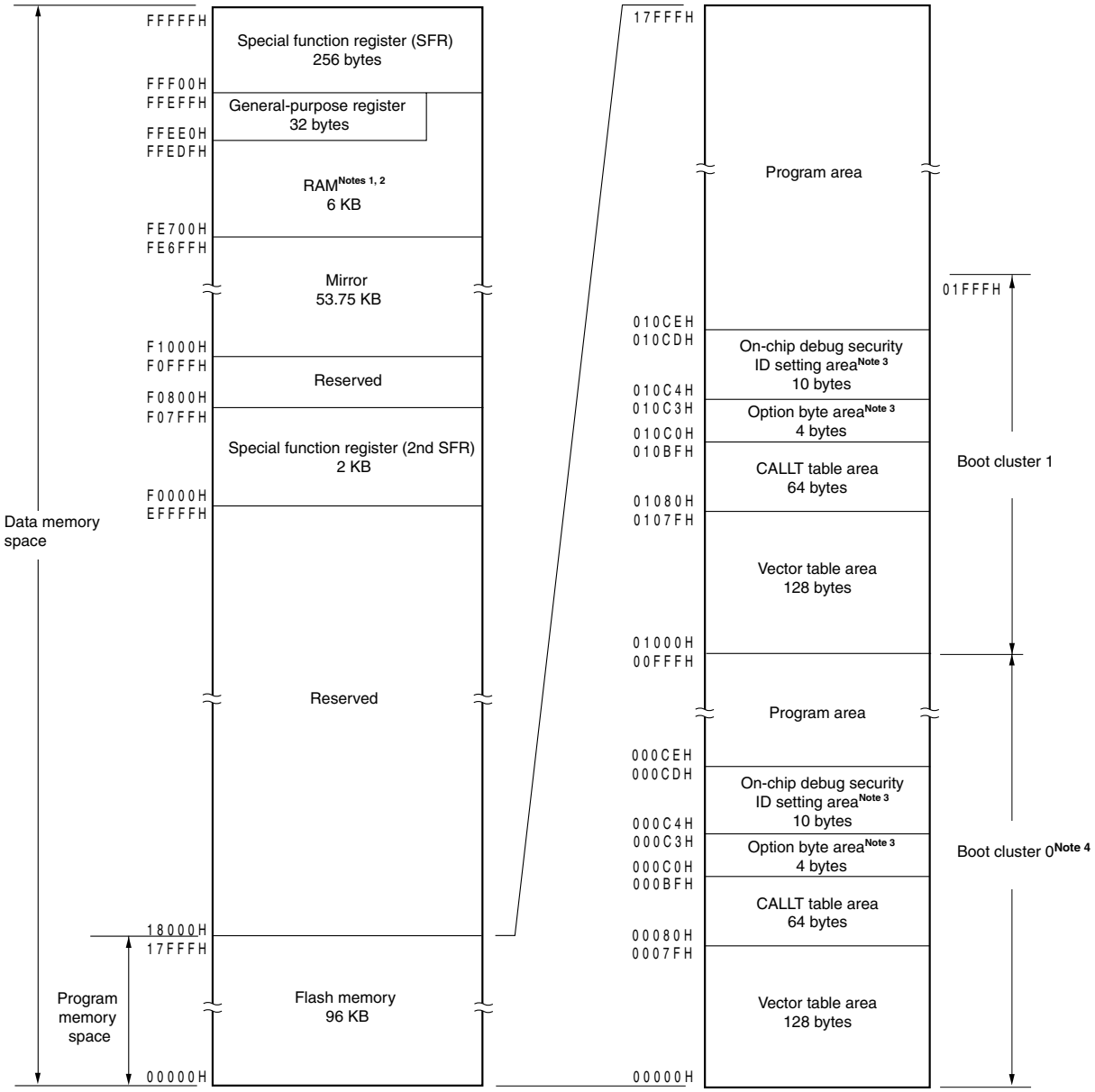
2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Figure 4-6. Memory Map (μPD78F1011, 78F1013)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

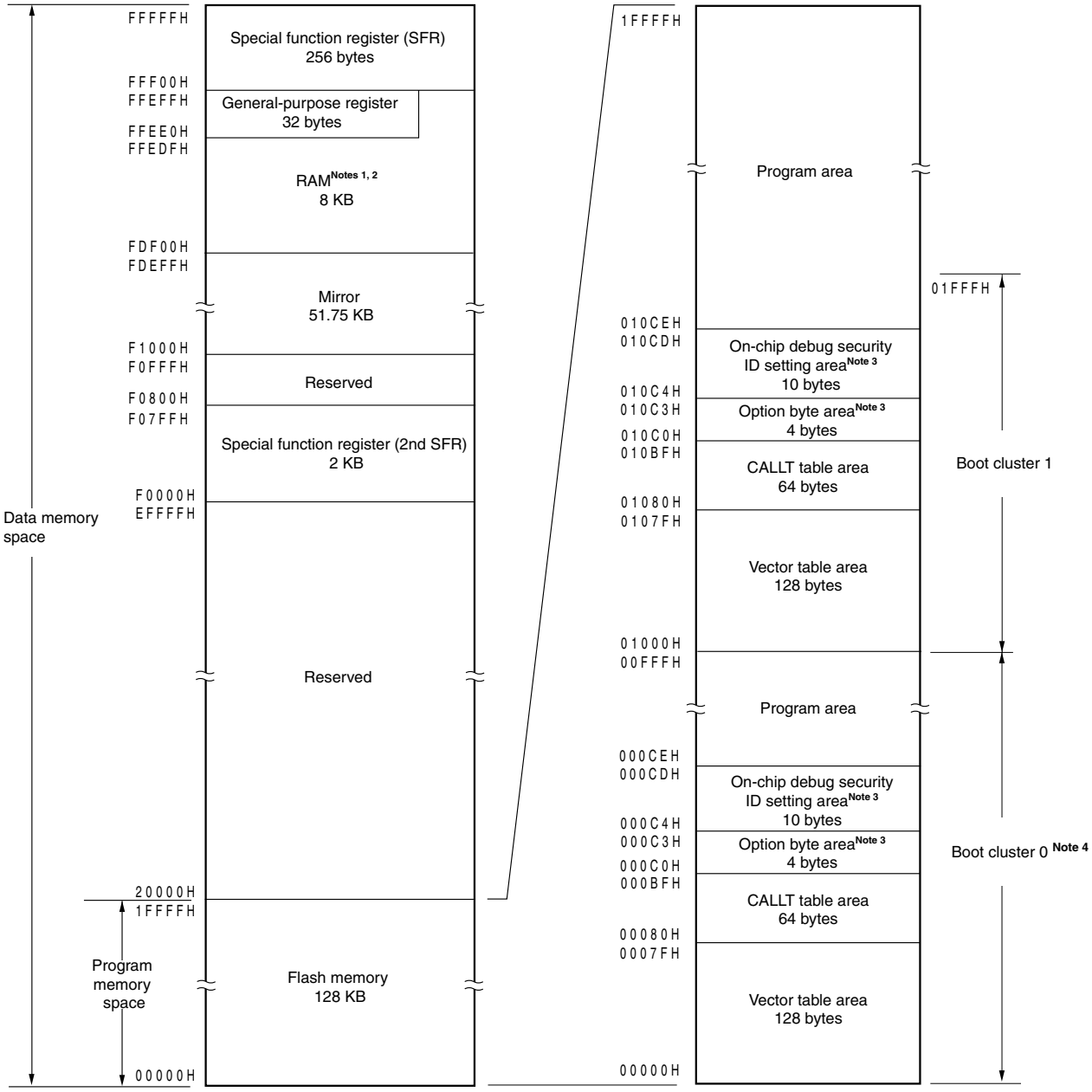
2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Figure 4-7. Memory Map (μPD78F1012, 78F1014)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FDF00H to FE2FFH also cannot be used with the μPD78F1012 and 78F1014.

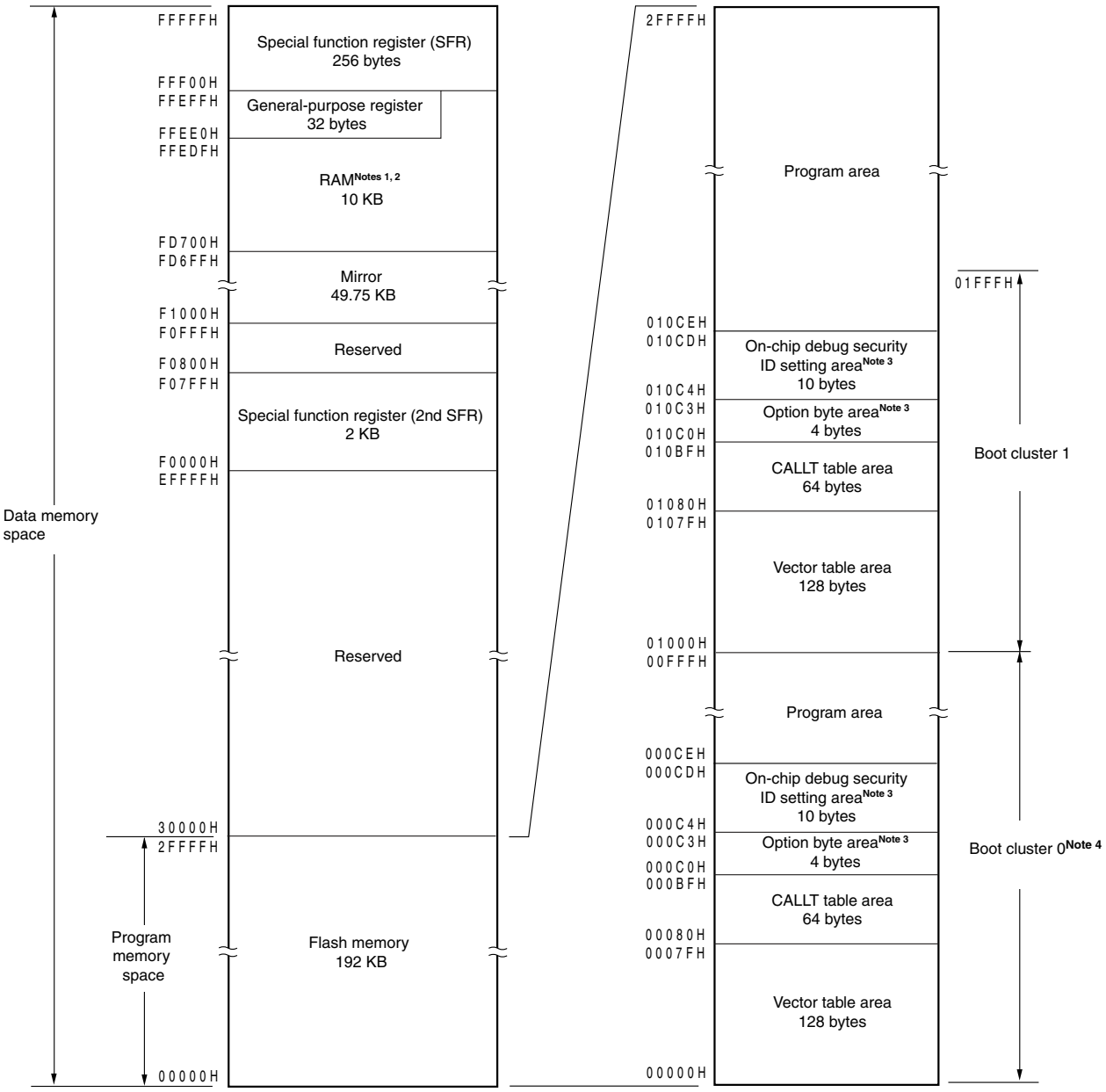
2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Figure 4-8. Memory Map (μPD78F1027, 78F1029)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

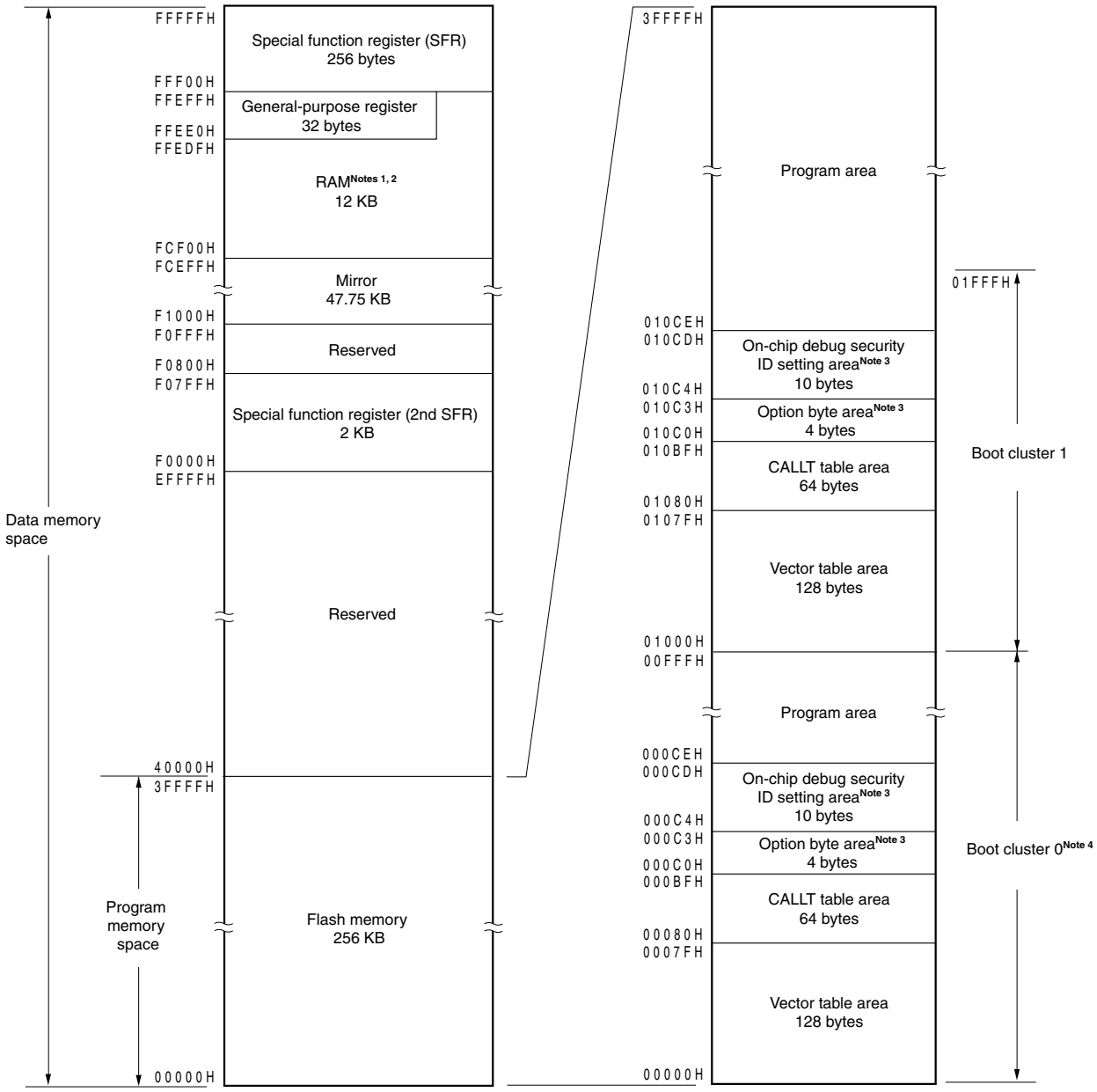
2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Figure 4-9. Memory Map (μPD78F1028, 78F1030)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FCF00H to FD2FFH also cannot be used with the μPD78F1029 and 78F1030.

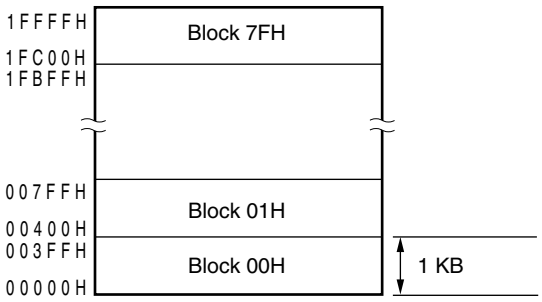
2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 4-1 Correspondence Between Address Values and Block Numbers in Flash Memory**.



(μPD78F1012, 78F1014)

Correspondence between the address values and block numbers in the flash memory are shown below.

Table 4-1. Correspondence Between Address Values and Block Numbers in Flash Memory (1/2)

Address Value	Block Number	Address Value	Block Number	Address Value	Block Number	Address Value	Block Number
00000H to 003FFH	00H	08000H to 083FFH	20H	10000H to 103FFH	40H	18000H to 183FFH	60H
00400H to 007FFH	01H	08400H to 087FFH	21H	10400H to 107FFH	41H	18400H to 187FFH	61H
00800H to 00BFFH	02H	08800H to 08BFFH	22H	10800H to 10BFFH	42H	18800H to 18BFFH	62H
00C00H to 00FFFH	03H	08C00H to 08FFFH	23H	10C00H to 10FFFH	43H	18C00H to 18FFFH	63H
01000H to 013FFH	04H	09000H to 093FFH	24H	11000H to 113FFH	44H	19000H to 193FFH	64H
01400H to 017FFH	05H	09400H to 097FFH	25H	11400H to 117FFH	45H	19400H to 197FFH	65H
01800H to 01BFFH	06H	09800H to 09BFFH	26H	11800H to 11BFFH	46H	19800H to 19BFFH	66H
01C00H to 01FFFH	07H	09C00H to 09FFFH	27H	11C00H to 11FFFH	47H	19C00H to 19FFFH	67H
02000H to 023FFH	08H	0A000H to 0A3FFH	28H	12000H to 123FFH	48H	1A000H to 1A3FFH	68H
02400H to 027FFH	09H	0A400H to 0A7FFH	29H	12400H to 127FFH	49H	1A400H to 1A7FFH	69H
02800H to 02BFFH	0AH	0A800H to 0ABFFH	2AH	12800H to 12BFFH	4AH	1A800H to 1ABFFH	6AH
02C00H to 02FFFH	0BH	0AC00H to 0AFFFH	2BH	12C00H to 12FFFH	4BH	1AC00H to 1AFFFH	6BH
03000H to 033FFH	0CH	0B000H to 0B3FFH	2CH	13000H to 133FFH	4CH	1B000H to 1B3FFH	6CH
03400H to 037FFH	0DH	0B400H to 0B7FFH	2DH	13400H to 137FFH	4DH	1B400H to 1B7FFH	6DH
03800H to 03BFFH	0EH	0B800H to 0BBFFH	2EH	13800H to 13BFFH	4EH	1B800H to 1BBFFH	6EH
03C00H to 03FFFH	0FH	0BC00H to 0BFFFH	2FH	13C00H to 13FFFH	4FH	1BC00H to 1BFFFH	6FH
04000H to 043FFH	10H	0C000H to 0C3FFH	30H	14000H to 143FFH	50H	1C000H to 1C3FFH	70H
04400H to 047FFH	11H	0C400H to 0C7FFH	31H	14400H to 147FFH	51H	1C400H to 1C7FFH	71H
04800H to 04BFFH	12H	0C800H to 0CBFFH	32H	14800H to 14BFFH	52H	1C800H to 1CBFFH	72H
04C00H to 04FFFH	13H	0CC00H to 0CFFFH	33H	14C00H to 14FFFH	53H	1CC00H to 1CFFFH	73H
05000H to 053FFH	14H	0D000H to 0D3FFH	34H	15000H to 153FFH	54H	1D000H to 1D3FFH	74H
05400H to 057FFH	15H	0D400H to 0D7FFH	35H	15400H to 157FFH	55H	1D400H to 1D7FFH	75H
05800H to 05BFFH	16H	0D800H to 0DBFFH	36H	15800H to 15BFFH	56H	1D800H to 1DBFFH	76H
05C00H to 05FFFH	17H	0DC00H to 0DFFFH	37H	15C00H to 15FFFH	57H	1DC00H to 1DFFFH	77H
06000H to 063FFH	18H	0E000H to 0E3FFH	38H	16000H to 163FFH	58H	1E000H to 1E3FFH	78H
06400H to 067FFH	19H	0E400H to 0E7FFH	39H	16400H to 167FFH	59H	1E400H to 1E7FFH	79H
06800H to 06BFFH	1AH	0E800H to 0EBFFH	3AH	16800H to 16BFFH	5AH	1E800H to 1EBFFH	7AH
06C00H to 06FFFH	1BH	0EC00H to 0EFFFH	3BH	16C00H to 16FFFH	5BH	1EC00H to 1EFFFH	7BH
07000H to 073FFH	1CH	0F000H to 0F3FFH	3CH	17000H to 173FFH	5CH	1F000H to 1F3FFH	7CH
07400H to 077FFH	1DH	0F400H to 0F7FFH	3DH	17400H to 177FFH	5DH	1F400H to 1F7FFH	7DH
07800H to 07BFFH	1EH	0F800H to 0FBFFH	3EH	17800H to 17BFFH	5EH	1F800H to 1FBFFH	7EH
07C00H to 07FFFH	1FH	0FC00H to 0FFFFH	3FH	17C00H to 17FFFH	5FH	1FC00H to 1FFFFH	7FH

Remark μPD78F1000: Block numbers 00H to 0FH
μPD78F1001, 78F1004, 78F1007: Block numbers 00H to 1FH
μPD78F1002, 78F1005, 78F1008: Block numbers 00H to 2FH
μPD78F1003, 78F1006, 78F1009, 78F1010: Block numbers 00H to 3FH
μPD78F1011, 78F1013: Block numbers 00H to 5FH
μPD78F1012, 78F1014: Block numbers 00H to 7FH

Table 4-1. Correspondence Between Address Values and Block Numbers in Flash Memory (2/2)

Address Value	Block Number	Address Value	Block Number	Address Value	Block Number	Address Value	Block Number
20000H to 203FFH	80H	28000H to 283FFH	A0H	30000H to 303FFH	C0H	38000H to 383FFH	E0H
20400H to 207FFH	81H	28400H to 287FFH	A1H	30400H to 307FFH	C1H	38400H to 387FFH	E1H
20800H to 20BFFH	82H	28800H to 28BFFH	A2H	30800H to 30BFFH	C2H	38800H to 38BFFH	E2H
20C00H to 20FFFH	83H	28C00H to 28FFFH	A3H	30C00H to 30FFFH	C3H	38C00H to 38FFFH	E3H
21000H to 213FFH	84H	29000H to 293FFH	A4H	31000H to 313FFH	C4H	39000H to 393FFH	E4H
21400H to 217FFH	85H	29400H to 297FFH	A5H	31400H to 317FFH	C5H	39400H to 397FFH	E5H
21800H to 21BFFH	86H	29800H to 29BFFH	A6H	31800H to 31BFFH	C6H	39800H to 39BFFH	E6H
21C00H to 21FFFH	87H	29C00H to 29FFFH	A7H	31C00H to 31FFFH	C7H	39C00H to 39FFFH	E7H
22000H to 223FFH	88H	2A000H to 2A3FFH	A8H	32000H to 323FFH	C8H	3A000H to 3A3FFH	E8H
22400H to 227FFH	89H	2A400H to 2A7FFH	A9H	32400H to 327FFH	C9H	3A400H to 3A7FFH	E9H
22800H to 22BFFH	8AH	2A800H to 2ABFFH	AAH	32800H to 32BFFH	CAH	3A800H to 3ABFFH	EAH
22C00H to 22FFFH	8BH	2AC00H to 2AFFFH	ABH	32C00H to 32FFFH	CBH	3AC00H to 3AFFFH	EBH
23000H to 233FFH	8CH	2B000H to 2B3FFH	ACH	33000H to 333FFH	CCH	3B000H to 3B3FFH	ECH
23400H to 237FFH	8DH	2B400H to 2B7FFH	ADH	33400H to 337FFH	CDH	3B400H to 3B7FFH	EDH
23800H to 23BFFH	8EH	2B800H to 2BBFFH	AEH	33800H to 33BFFH	CEH	3B800H to 3BBFFH	EEH
23C00H to 23FFFH	8FH	2BC00H to 2BFFFH	AFH	33C00H to 33FFFH	CFH	3BC00H to 3BFFFH	EFH
24000H to 243FFH	90H	2C000H to 2C3FFH	B0H	34000H to 343FFH	D0H	3C000H to 3C3FFH	F0H
24400H to 247FFH	91H	2C400H to 2C7FFH	B1H	34400H to 347FFH	D1H	3C400H to 3C7FFH	F1H
24800H to 24BFFH	92H	2C800H to 2CBFFH	B2H	34800H to 34BFFH	D2H	3C800H to 3CBFFH	F2H
24C00H to 24FFFH	93H	2CC00H to 2CFFFH	B3H	34C00H to 34FFFH	D3H	3CC00H to 3CFFFH	F3H
25000H to 253FFH	94H	2D000H to 2D3FFH	B4H	35000H to 353FFH	D4H	3D000H to 3D3FFH	F4H
25400H to 257FFH	95H	2D400H to 2D7FFH	B5H	35400H to 357FFH	D5H	3D400H to 3D7FFH	F5H
25800H to 25BFFH	96H	2D800H to 2DBFFH	B6H	35800H to 35BFFH	D6H	3D800H to 3DBFFH	F6H
25C00H to 25FFFH	97H	2DC00H to 2DFFFH	B7H	35C00H to 35FFFH	D7H	3DC00H to 3DFFFH	77H
26000H to 263FFH	98H	2E000H to 2E3FFH	B8H	36000H to 363FFH	D8H	3E000H to 3E3FFH	F8H
26400H to 267FFH	99H	2E400H to 2E7FFH	B9H	36400H to 367FFH	D9H	3E400H to 3E7FFH	F9H
26800H to 26BFFH	9AH	2E800H to 2EBFFH	BAH	36800H to 36BFFH	DAH	3E800H to 3EBFFH	FAH
26C00H to 26FFFH	9BH	2EC00H to 2EFFFH	BBH	36C00H to 36FFFH	DBH	3EC00H to 3EFFFH	FBH
27000H to 273FFH	9CH	2F000H to 2F3FFH	BCH	37000H to 373FFH	DCH	3F000H to 3F3FFH	FCH
27400H to 277FFH	9DH	2F400H to 2F7FFH	BDH	37400H to 377FFH	DDH	3F400H to 3F7FFH	FDH
27800H to 27BFFH	9EH	2F800H to 2FBFFH	BEH	37800H to 37BFFH	DEH	3F800H to 3FBFFH	FEH
27C00H to 27FFFH	9FH	2FC00H to 2FFFFH	BFH	37C00H to 37FFFH	DFH	3FC00H to 3FFFFH	FFH

Remark μPD78F1027, 78F1029: Block numbers 00H to BFH
μPD78F1028, 78F1030: Block numbers 00H to FFH

4.1.1 Internal program memory space

The internal program memory space stores the program and table data.

The 78K0R/Kx3-L products incorporate internal ROM (flash memory), as shown below.

Table 4-2. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
μPD78F1000	Flash memory	16384 × 8 bits (00000H to 03FFFH)
μPD78F1001, 78F1004, 78F1007		32768 × 8 bits (00000H to 07FFFH)
μPD78F1002, 78F1005, 78F1008		49152 × 8 bits (00000H to 0BFFFH)
μPD78F1003, 78F1006, 78F1009, 78F1010		65536 × 8 bits (00000H to 0FFFFH)
μPD78F1011, 78F1013		98304 × 8 bits (00000H to 17FFFH)
μPD78F1012, 78F1014		131072 × 8 bits (00000H to 1FFFFH)
μPD78F1027, 78F1029		196608 × 8 bits (00000H to 2FFFFH)
μPD78F1028, 78F1030		262144 × 8 bits (00000H to 3FFFFH)

The internal program memory space is divided into the following areas.

(1) Vector table area

The 128-byte area 00000H to 0007FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area. Furthermore, the interrupt jump address is a 64 K address of 00000H to 0FFFFH, because the vector code is assumed to be 2 bytes.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

Table 4-3. Vector Table (1/2)

Vector Table Address	Interrupt Source	KC3-L (40pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
00000H	$\overline{\text{RESET}}$ input, POC, LVI, WDT, TRAP	√	√	√	√	√	√	√
00004H	INTWDTI	√	√	√	√	√	√	√
00006H	INTLVI	√	√	√	√	√	√	√
00008H	INTP0	√	√	√	√	√	√	√
0000AH	INTP1	√	√	√	√	√	√	√
0000CH	INTP2	√	√	√	√	√	√	√
0000EH	INTP3	√	√	√	√	√	√	√
00010H	INTP4	√	√	√	√	√	√	√
00012H	INTP5	√	√	√	√	√	√	√
00014H	INTST3	–	–	–	–	–	√	√
00016H	INTSR3	–	–	–	–	–	√	√
	INTCMP0	√	√	√	√	√	–	–
00018H	INTSRE3	–	–	–	–	–	√	√
	INTCMP1	√	√	√	√	√	–	–
0001AH	INTDMA0	√	√	√	√	√	√	√
0001CH	INTDMA1	√	√	√	√	√	√	√
0001EH	INTST0/INTCSI00	√	√	√	√	√	√	√
00020H	INTSR0/INTCSI01	√	√	√	√	√	√	√
00022H	INTSRE0	√	√	√	√	√	√	√
00024H	INTST1/INTCSI10/INTIIC10	√	√	√	√	√	√	√
00026H	INTSR1	√	√	√	√	√	√	√
00028H	INTSRE1	√	√	√	√	√	√	√
0002AH	INTIICA	–	–	√	√	√	√	√
0002CH	INTTM00	√	√	√	√	√	√	√
0002EH	INTTM01	√	√	√	√	√	√	√
00030H	INTTM02	√	√	√	√	√	√	√
00032H	INTTM03	√	√	√	√	√	√	√

Table 4-3. Vector Table (2/2)

Vector Table Address	Interrupt Source	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
00034H	INTAD	√	√	√	√	√	√	√
00036H	INTRTC	–	√	√	√	√	√	√
00038H	INTRTCI	–	√	√	√	√	√	√
0003AH	INTKR	√	√	√	√	√	√	√
0003CH	INTST2/INTCSI20/INTIIC20	–	–	–	–	–	√	√
0003EH	INTP6	–	–	–	–	–	√	√
00040H	INTTM13	–	–	–	–	–	√	√
	INTMD	√	√	√	√	√	–	–
00042H	INTTM04	√	√	√	√	√	√	√
00044H	INTTM05	√	√	√	√	√	√	√
00046H	INTTM06	√	√	√	√	√	√	√
00048H	INTTM07	√	√	√	√	√	√	√
0004AH	INTSR2	–	–	–	–	–	√	√
	INTP6	√	√	√	√	√	–	–
0004CH	INTP7	–	√	√	√	√	√	√
0004EH	INTP8	–	–	–	–	–	√	√
00050H	INTP9	–	–	–	–	–	√	√
00052H	INTP10	–	–	–	–	–	√	√
00054H	INTP11	–	–	–	–	–	√	√
	INTSRE4	–	–	–	–	–	Note	Note
00056H	INTTM10	–	–	–	–	–	√	√
00058H	INTTM11	–	–	–	–	–	√	√
0005AH	INTTM12	–	–	–	–	–	√	√
0005CH	INTSRE2	–	–	–	–	–	√	√
0005EH	INTMD	–	–	–	–	–	√	√
00060H	INTST4	–	–	–	–	–	Note	Note
	INTCSI40	–	–	–	–	–	Note	Note
00062H	INTSR4	–	–	–	–	–	Note	Note
	INTCSI41	–	–	–	–	–	Note	Note
0007EH	BRK	√	√	√	√	√	√	√

Note Those are only mounted in the 78K0R/KF3-L (μ PD78F1027 and 78F1028) and the 78K0R/KG3-L (μ PD78F1029 and 78F1030).

(2) CALLT instruction table area

The 64-byte area 00080H to 000BFH can store the subroutine entry address of a 2-byte call instruction (CALLT). Set the subroutine entry address to a value in a range of 00000H to 0FFFFH (because an address code is of 2 bytes).

To use the boot swap function, set a CALLT instruction table also at 01080H to 010BFH.

(3) Option byte area

A 4-byte area of 000C0H to 000C3H can be used as an option byte area. Set the option byte at 010C0H to 010C3H when the boot swap is used. For details, see **CHAPTER 25 OPTION BYTE**.

(4) On-chip debug security ID setting area

A 10-byte area of 000C4H to 000CDH and 010C4H to 010CDH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 000C4H to 000CDH when the boot swap is not used and at 000C4H to 000CDH and 010C4H to 010CDH when the boot swap is used. For details, see **CHAPTER 27 ON-CHIP DEBUG FUNCTION**.

4.1.2 Mirror area

The 78K0R/Kx3-L mirrors the data flash area of 00000H to 0FFFFH, to F0000H to FFFFFH. The μPD78F1011 to 78F1014, 78F1027, 78F1028, 78F1029, and 78F1030 mirror the data flash area of 00000H to 0FFFFH or 10000H to 1FFFFH, to F0000H to FFFFFH (the data flash area to be mirrored is set by the processor mode control register (PMC)).

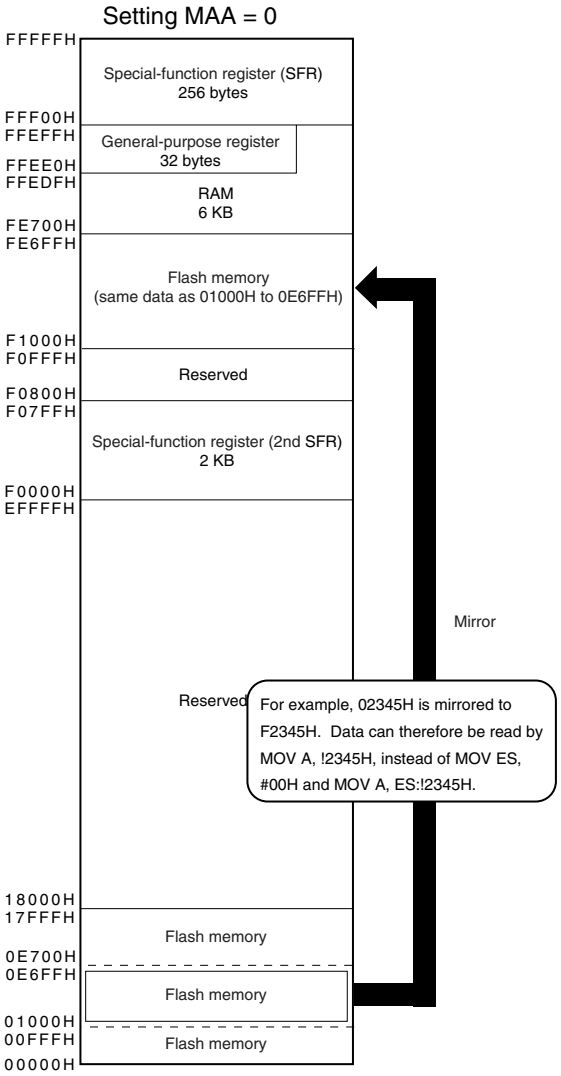
By reading data from F0000H to FFFFFH, an instruction that does not have the ES register as an operand can be used, and thus the contents of the data flash can be read with the shorter code. However, the data flash area is not mirrored to the SFR, extended SFR, RAM, and use prohibited areas.

See **4.1 Memory Space** for the mirror area of each product.

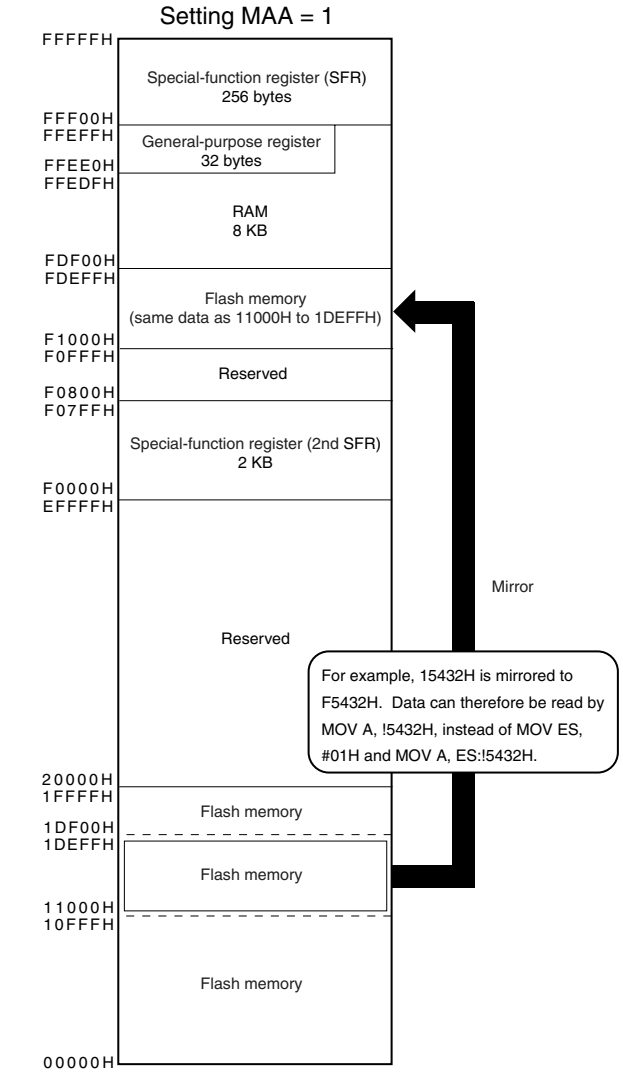
The mirror area can only be read and no instruction can be fetched from this area.

The following show examples.

Example 1 μPD8F1011, 78F1013
(Flash memory: 96 KB, RAM: 6 KB)



Example 2 μPD78F1012, 78F1014
(Flash memory: 128 KB, RAM: 8 KB)



Remark MAA: Bit 0 of the processor mode control register (PMC)

The PMC register is described below.

- **Processor mode control register (PMC)**

This register sets the flash memory space for mirroring to area from F0000H to FFFFFH.

The PMC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 4-10. Format of Configuration of Processor Mode Control Register (PMC)

Address: FFFFEH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
PMC	0	0	0	0	0	0	0	MAA

MAA	Selection of flash memory space for mirroring to area from F0000H to FFFFFH
0	00000H to 0FFFFH is mirrored to F0000H to FFFFFH
1	10000H to 1FFFFH is mirrored to F0000H to FFFFFH Note

Note This setting is prohibited in products other than the μPD78F1011 to 78F1014, 78F1027, 78F1028, 78F1029, and 78F1030.

Cautions 1. In products other than the μPD78F1011 to 78F1014, 78F1027, 78F1028, 78F1029, and 78F1030, be sure to set bit 0 (MAA) to 0 (default value).

2. Set the PMC register only once during the initial settings prior to operating the DMA controller. Rewriting the PMC register other than during the initial settings is prohibited.

3. After setting the PMC register, wait for at least one instruction and access the mirror area.

4.1.3 Internal data memory space

The 78K0R/Kx3-L products incorporate the following RAMs.

Table 4-4. Internal RAM Capacity

Part Number	Internal RAM
μPD78F1000	1024 × 8 bits (FFB00H to FFEFFH)
μPD78F1001, 78F1004, 78F1007	1536 × 8 bits (FF900H to FFEFFH)
μPD78F1002, 78F1005, 78F1008	2048 × 8 bits (FF700H to FFEFFH)
μPD78F1003, 78F1006, 78F1009	3072 × 8 bits (FF300H to FFEFFH)
μPD78F1010	4096 × 8 bits (FEF00H to FFEFFH)
μPD78F1011, 78F1013	6144 × 8 bits (FE700H to FFEFFH)
μPD78F1012, 78F1014	8192 × 8 bits (FDF00H to FFEFFH)
μPD78F1027, 78F1029	10240 × 8 bits (FD700H to FFEFFH)
μPD78F1028, 78F1030	12288 × 8 bits (FCF00H to FFEFFH)

The internal RAM can be used as a data area and a program area where instructions are written and executed. Four general-purpose register banks consisting of eight 8-bit registers per bank are assigned to the 32-byte area of FFEE0H to FFEFFH of the internal RAM area. However, instructions cannot be executed by using the general-purpose registers.

The internal RAM is used as a stack memory.

Cautions 1. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.

2. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FF300H to FF6FFH and FDF00H to FE2FFH also cannot be used with the μPD78F1003, 78F1006 and 78F1009, and μPD78F1011 to 78F1014, 78F1027, 78F1028, 78F1029, and 78F1030, respectively.

4.1.4 Special function register (SFR) area

On-chip peripheral hardware special function registers (SFRs) are allocated in the area FFF00H to FFFFFH (see **Table 4-5** in **4.2.4 Special function registers (SFRs)**).

Caution Do not access addresses to which SFRs are not assigned.

4.1.5 Extended special function register (2nd SFR: 2nd Special Function Register) area

On-chip peripheral hardware special function registers (2nd SFRs) are allocated in the area F0000H to F07FFH (see **Table 4-6** in **4.2.5 Extended Special function registers (2nd SFRs: 2nd Special Function Registers)**).

SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

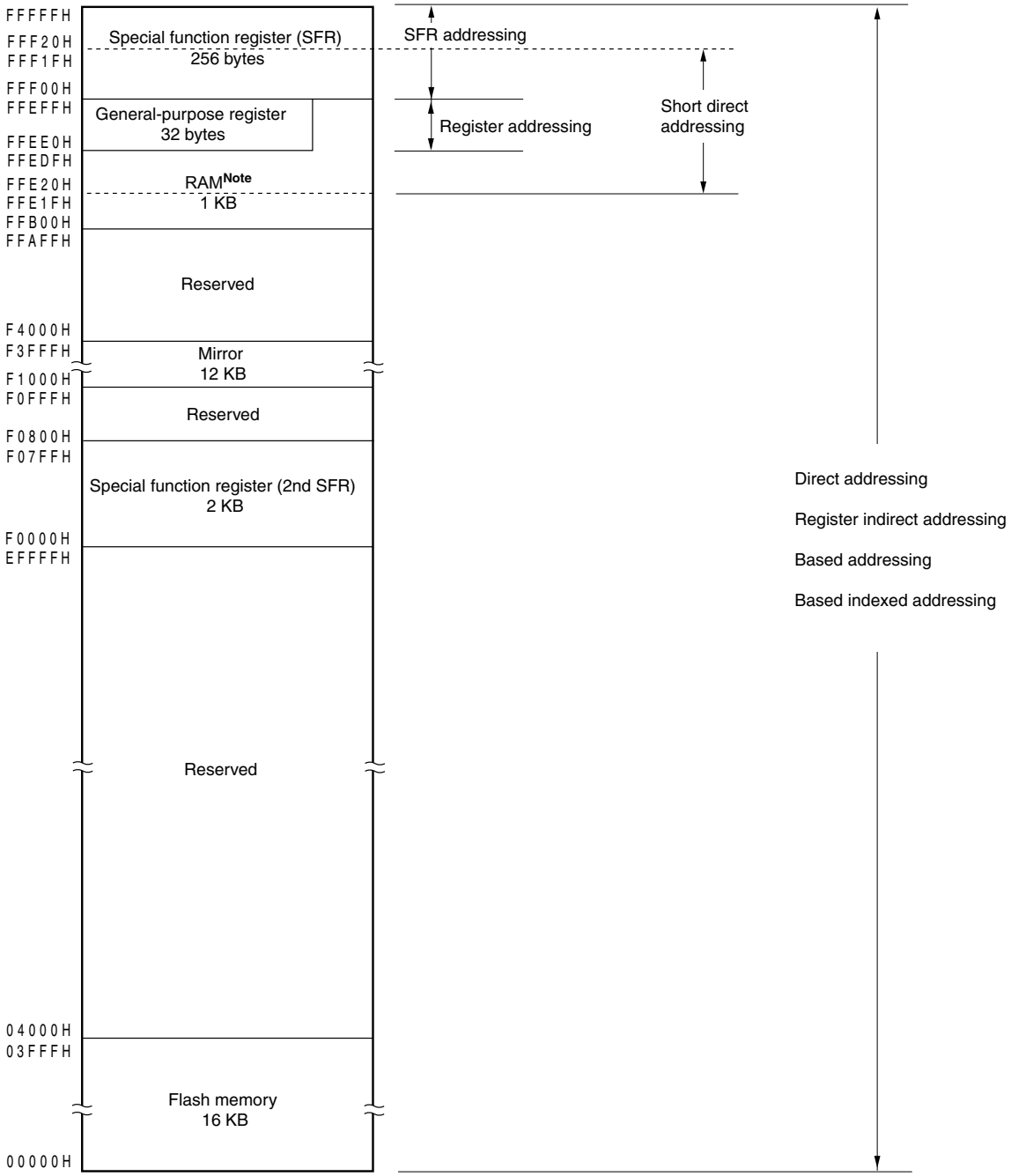
Caution Do not access addresses to which extended SFRs are not assigned.

4.1.6 Data memory addressing

Addressing refers to the method of specifying the address of the instruction to be executed next or the address of the register or memory relevant to the execution of instructions.

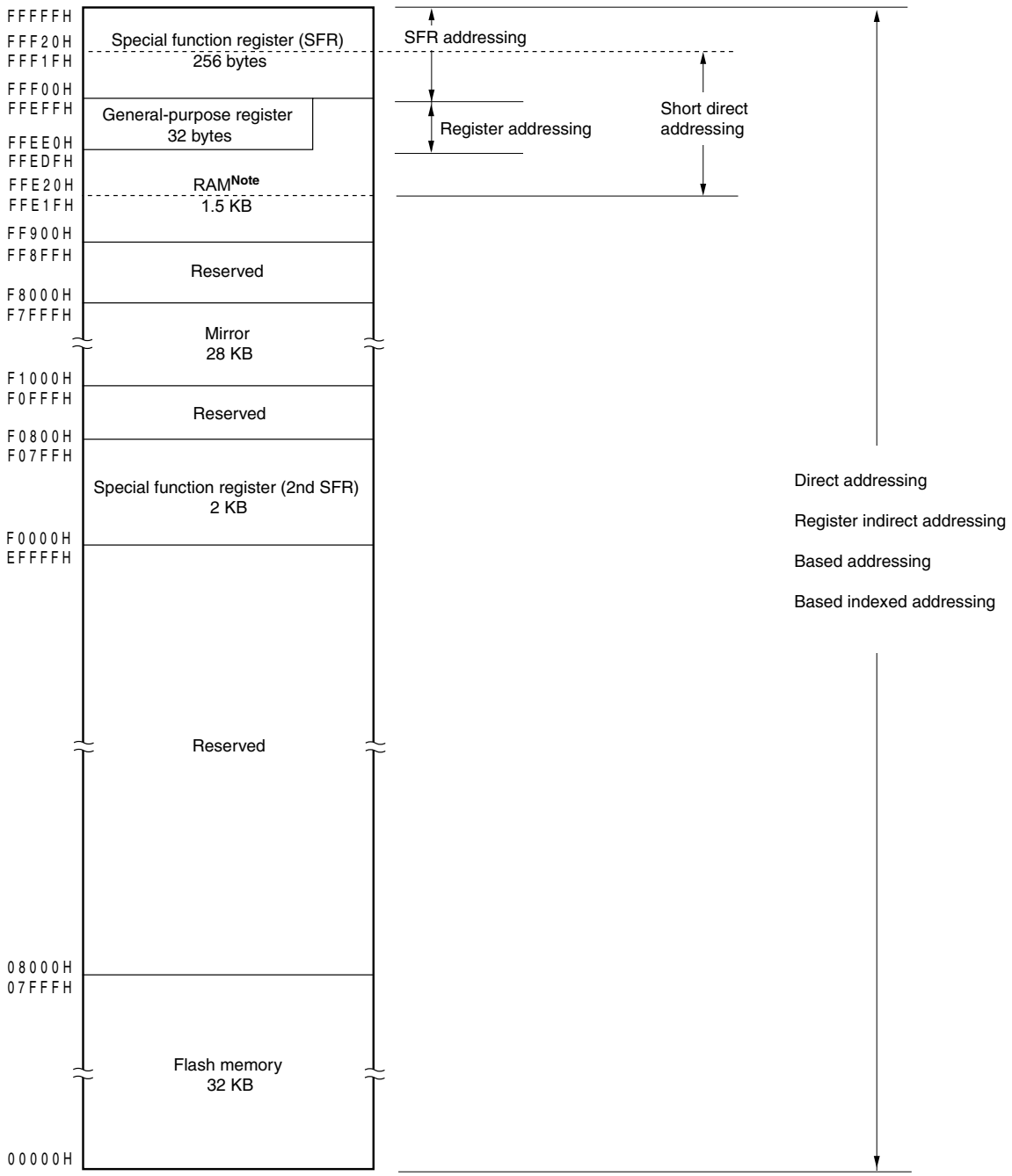
Several addressing modes are provided for addressing the memory relevant to the execution of instructions for the 78K0R/Kx3-L, based on operability and other considerations. For areas containing data memory in particular, special addressing methods designed for the functions of the special function registers (SFR) and general-purpose registers are available for use. Figures 4-11 to 4-19 show correspondence between data memory and addressing.

Figure 4-11. Correspondence Between Data Memory and Addressing (μPD78F1000)



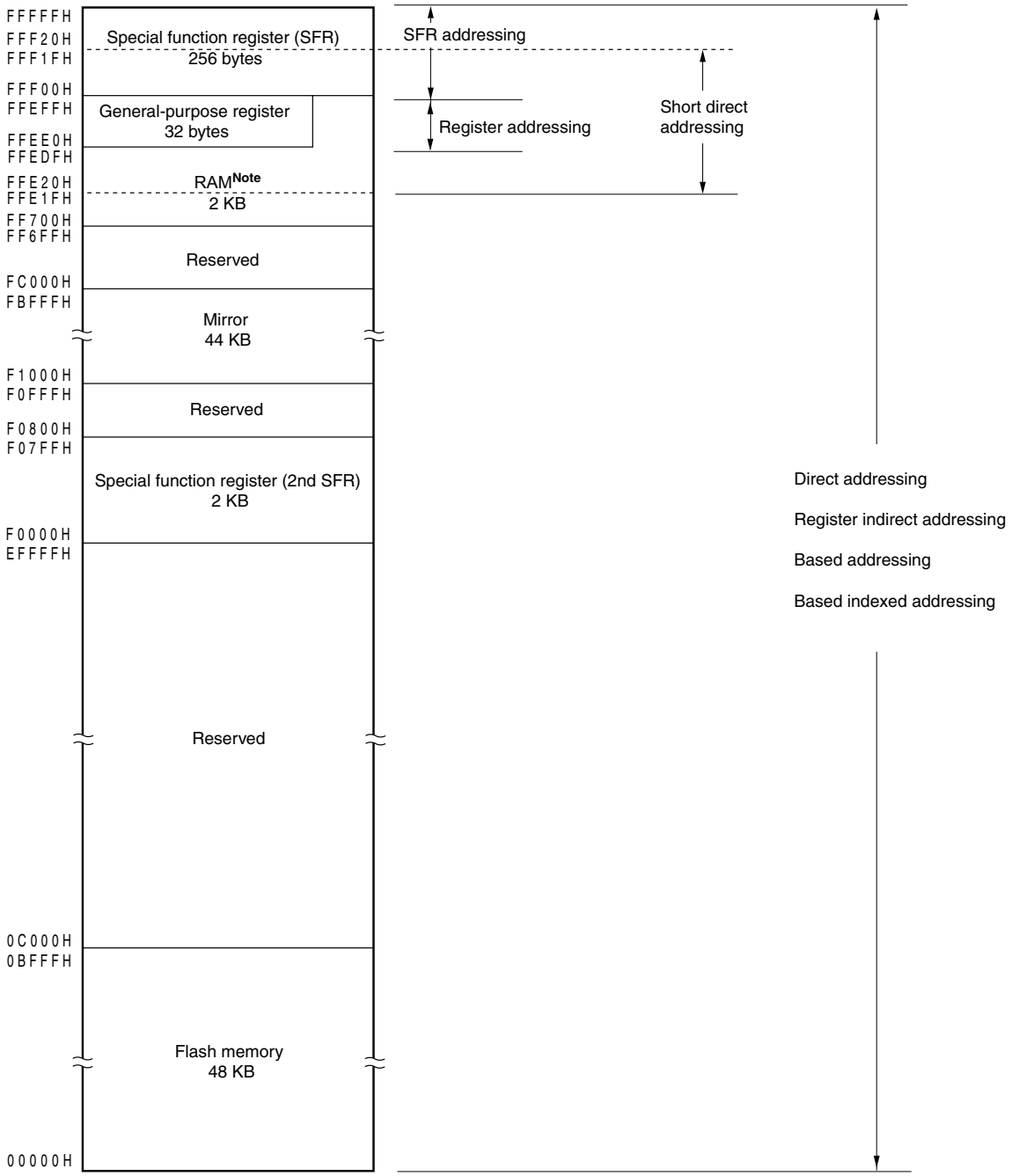
Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

Figure 4-12. Correspondence Between Data Memory and Addressing (μPD78F1001, 78F1004, 78F1007)



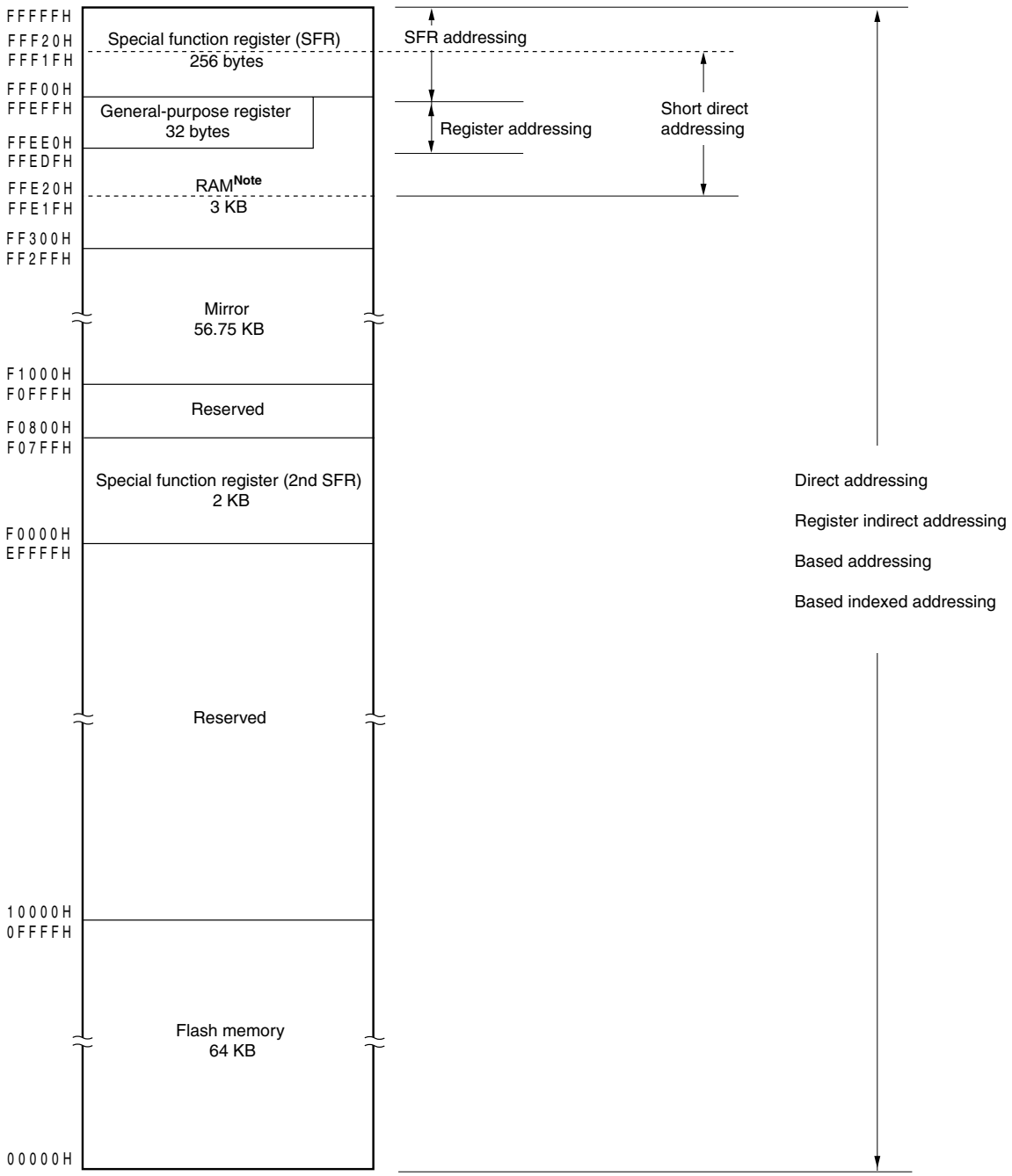
Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

Figure 4-13. Correspondence Between Data Memory and Addressing (μPD78F1002, 78F1005, 78F1008)



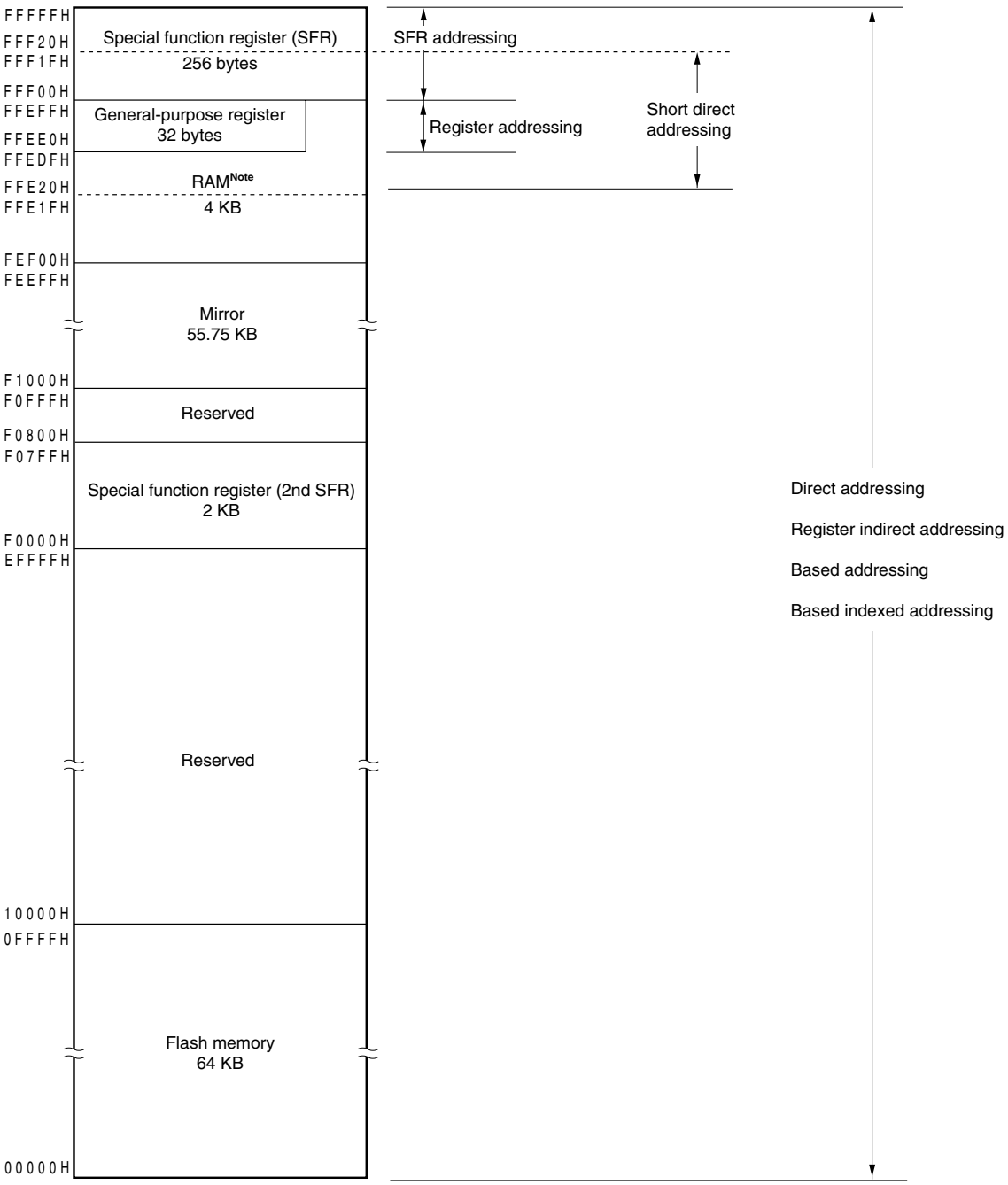
Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

Figure 4-14. Correspondence Between Data Memory and Addressing (μPD78F1003, 78F1006, 78F1009)



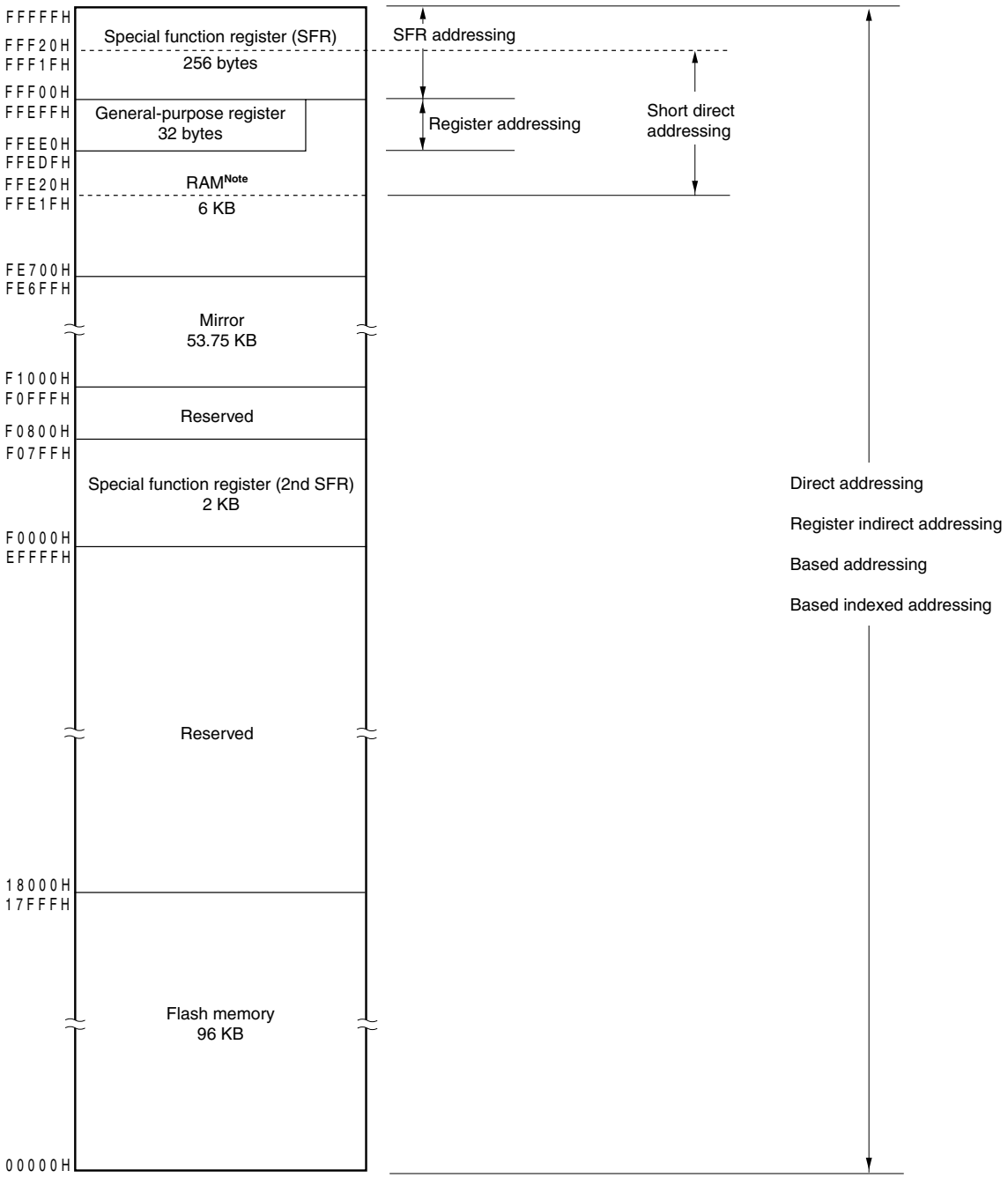
Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FF300H to FF6FFH also cannot be used with the μPD78F1003, 78F1006 and 78F1009.

Figure 4-15. Correspondence Between Data Memory and Addressing (μPD78F1010)



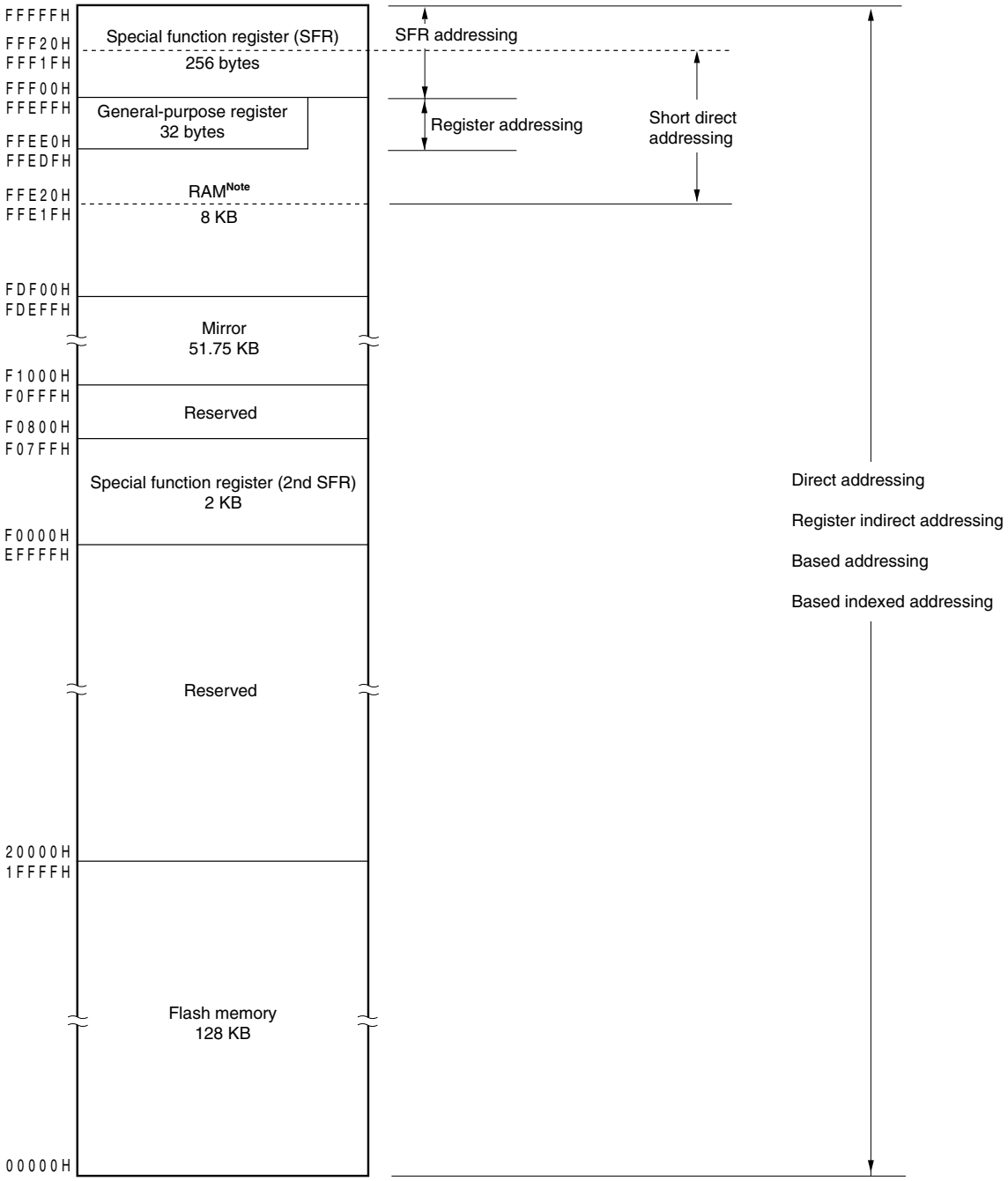
Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

Figure 4-16. Correspondence Between Data Memory and Addressing (μPD78F1011, 78F1013)



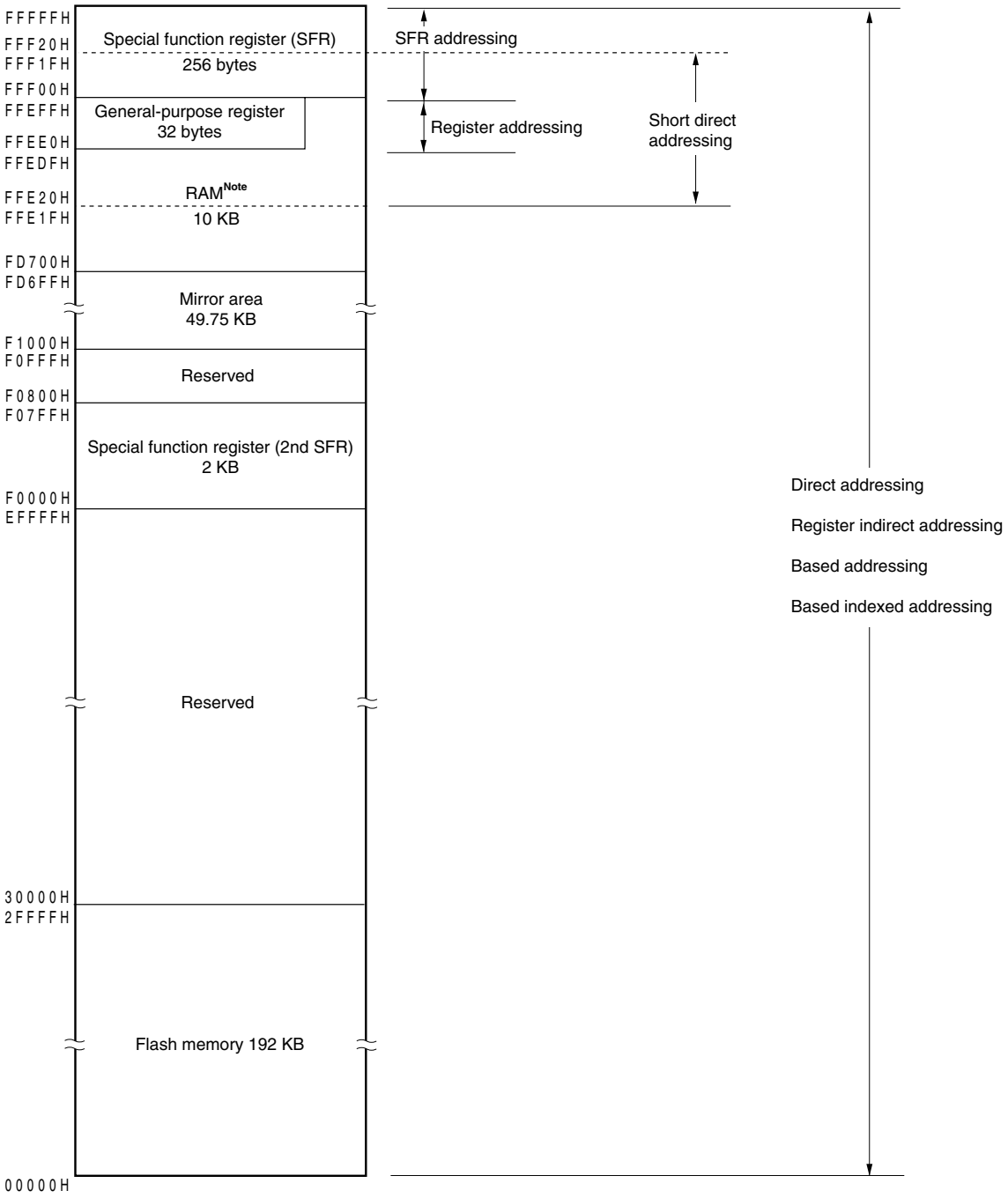
Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

Figure 4-17. Correspondence Between Data Memory and Addressing (μPD78F1012, 78F1014)



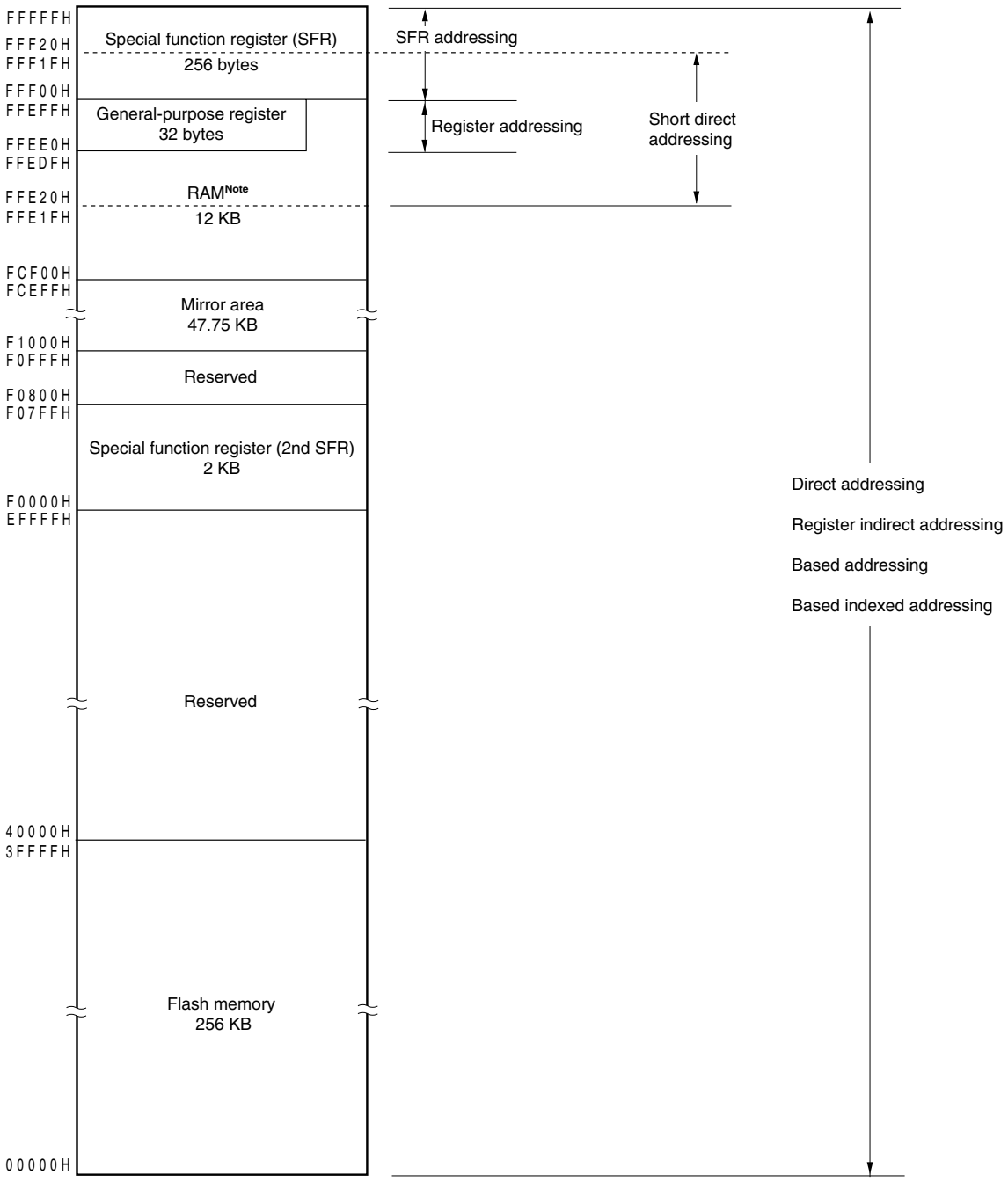
Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FDF00H to FE2FFH also cannot be used with the μPD78F1012 and 78F1014.

Figure 4-18. Correspondence Between Data Memory and Addressing (μPD78F1027, 78F1029)



Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

Figure 4-19. Correspondence Between Data Memory and Addressing (μPD78F1028, 78F1030)



Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FCF00H to FD2FFH also cannot be used with the μPD78F1028 and 78F1030.

4.2 Processor Registers

The 78K0R/Kx3-L products incorporate the following processor registers.

4.2.1 Control registers

The control registers control the program sequence, statuses and stack memory. The control registers consist of a program counter (PC), a program status word (PSW) and a stack pointer (SP).

(1) Program counter (PC)

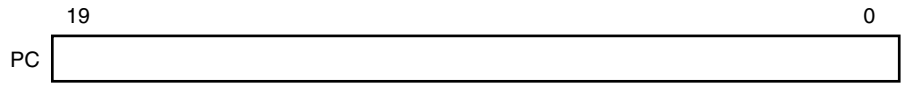
The program counter is a 20-bit register that holds the address information of the next program to be executed.

In normal operation, PC is automatically incremented according to the number of bytes of the instruction to be fetched.

When a branch instruction is executed, immediate data and register contents are set.

Reset signal generation sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 4-20. Format of Program Counter



(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags set/reset by instruction execution.

Program status word contents are stored in the stack area upon vectored interrupt request is acknowledged or PUSH PSW instruction execution and are restored upon execution of the RETB, RETI and POP PSW instructions. Reset signal generation sets the PSW register to 06H.

Figure 4-21. Format of Program Status Word

	7							0
PSW	IE	Z	RBS1	AC	RBS0	ISP1	ISP0	CY

(a) Interrupt enable flag (IE)

This flag controls the interrupt request acknowledge operations of the CPU.

When 0, the IE flag is set to the interrupt disabled (DI) state, and all maskable interrupt requests are disabled.

When 1, the IE flag is set to the interrupt enabled (EI) state and interrupt request acknowledgment is controlled with an in-service priority flag (ISP1, ISP0), an interrupt mask flag for various interrupt sources, and a priority specification flag.

The IE flag is reset (0) upon DI instruction execution or interrupt acknowledgment and is set (1) upon EI instruction execution.

(b) Zero flag (Z)

When the operation result is zero, this flag is set (1). It is reset (0) in all other cases.

(c) Register bank select flags (RBS0, RBS1)

These are 2-bit flags to select one of the four register banks.

In these flags, the 2-bit information that indicates the register bank selected by SEL RBn instruction execution is stored.

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flags (ISP1, ISP0)

This flag manages the priority of acknowledgeable maskable vectored interrupts. Vectored interrupt requests specified lower than the value of ISP0 and ISP1 flags by the priority specification flag registers (PRn0L, PRn0H, PRn1L, PRn1H, PRn2L, PRn2H) (see **18.3 (3)**) can not be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

Remark n = 0, 1

(f) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal RAM area can be set as the stack area.

Figure 4-22. Format of Stack Pointer

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The SP is decremented ahead of write (save) to the stack memory and is incremented after read (restored) from the stack memory.

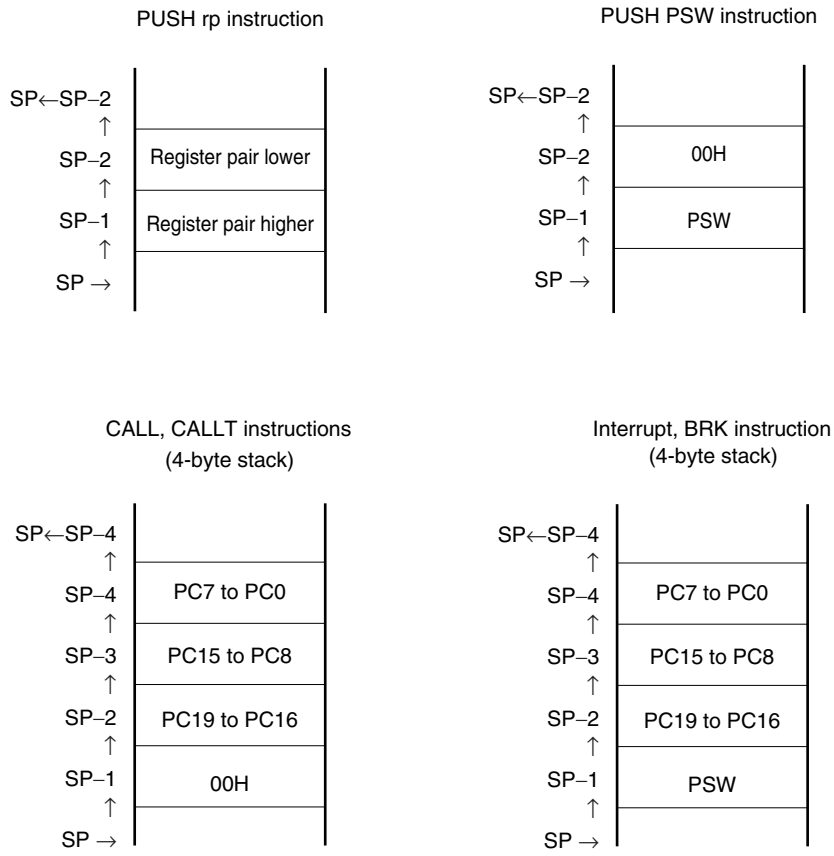
Each stack operation saves data as shown in Figure 4-19.

Caution 1. Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.

2. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space as a stack area.

3. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FF300H to FF6FFH and FDF00H to FE2FFH also cannot be used with the μPD78F1003, 78F1006 and 78F1009, and μPD78F1012 and 78F1014, 78F1027, 78F1028, 78F1029, and 78F1030, respectively.

Figure 4-23. Data to Be Saved to Stack Memory



4.2.2 General-purpose registers

General-purpose registers are mapped at particular addresses (FFEE0H to FFEFFH) of the data memory. The general-purpose registers consists of 4 banks, each bank consisting of eight 8-bit registers (X, A, C, B, E, D, L, and H).

Each register can be used as an 8-bit register, and two 8-bit registers can also be used in a pair as a 16-bit register (AX, BC, DE, and HL).

These registers can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

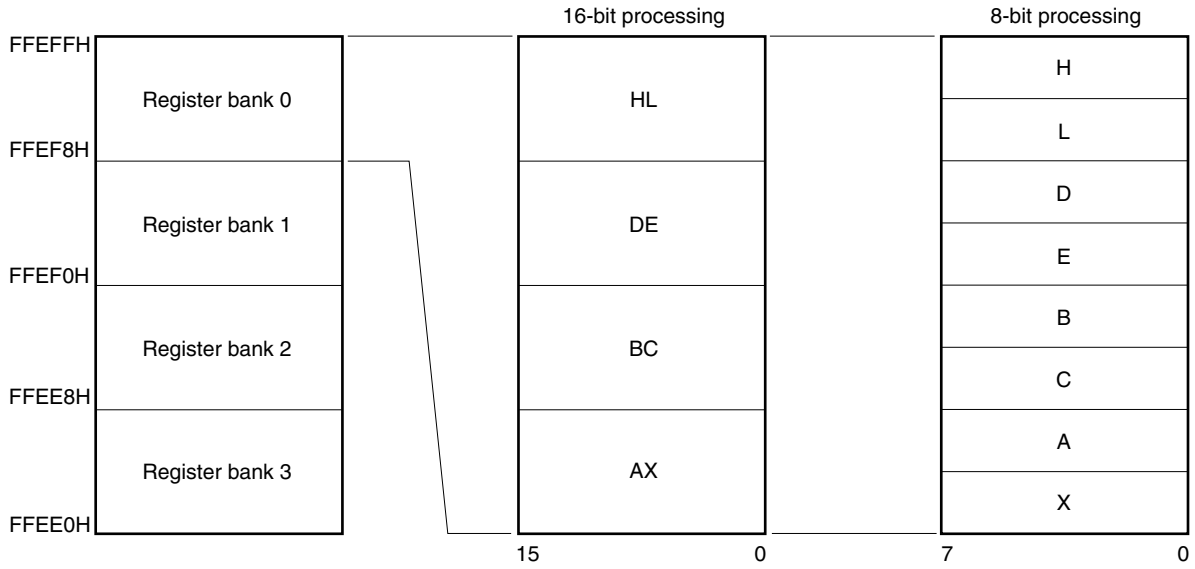
Register banks to be used for instruction execution are set by the CPU control instruction (SEL RBn). Because of the 4-register bank configuration, an efficient program can be created by switching between a register for normal processing and a register for interrupts for each bank.

Cautions 1. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.

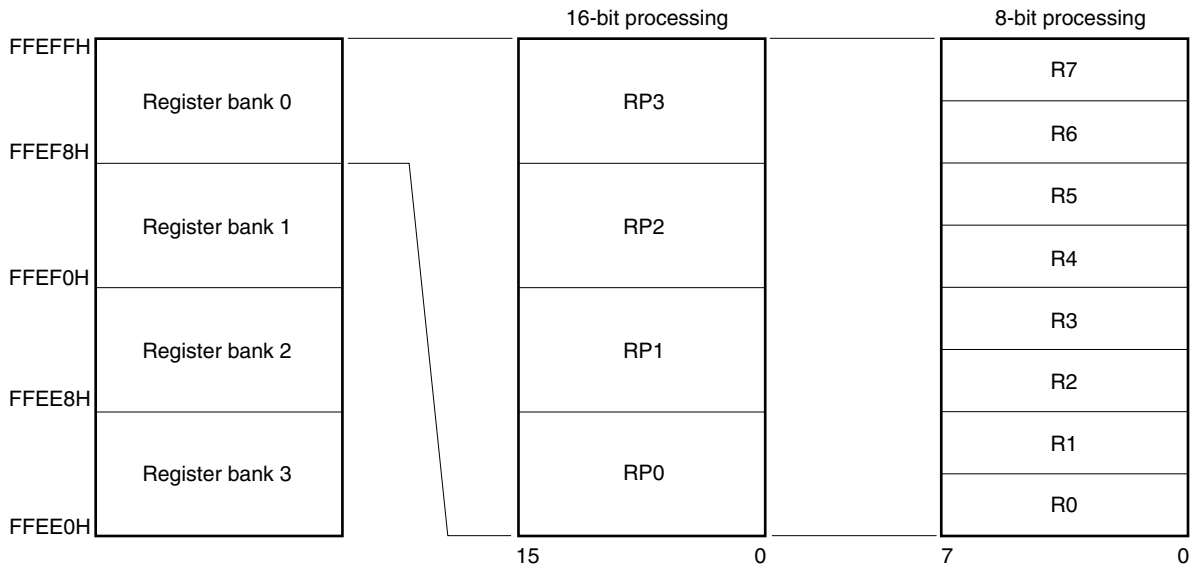
2. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FF300H to FF6FFH and FDF00H to FE2FFH also cannot be used with the μPD78F1003, 78F1006 and 78F1009, and μPD78F1012, 78F1014, 78F1027, 78F1028, 78F1029, and 78F1030, respectively.

Figure 4-24. Configuration of General-Purpose Registers

(a) Function name



(b) Absolute name



4.2.3 ES and CS registers

The ES register is used for data access and the CS register is used to specify the higher address when a branch instruction is executed.

The default value of the ES register after reset is 0FH, and that of the CS register is 00H.

Figure 4-25. Configuration of ES and CS Registers

	7	6	5	4	3	2	1	0
ES	0	0	0	0	ES3	ES2	ES1	ES0

	7	6	5	4	3	2	1	0
CS	0	0	0	0	CS3	CP2	CP1	CP0

4.2.4 Special function registers (SFRs)

Unlike a general-purpose register, each SFR has a special function.

SFRs are allocated to the FFF00H to FFFFFH area.

SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit). This manipulation can also be specified with an address.
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr). This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (sfrp). When specifying an address, describe an even address.

Table 4-5 gives a list of the SFRs. The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of a special function register. It is a reserved word in the RA78K0R, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0R. When using the RA78K0R, ID78K0R-QB, and SM+ for 78K0R, symbols can be written as an instruction operand.
- R/W
  Indicates whether the corresponding SFR can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulable bit units
  "√" indicates the manipulable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Caution Do not access addresses to which extended SFRs are not assigned.

Remark For extended SFRs (2nd SFRs), see **4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

Table 4-5. SFR List (1/6)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
				1-bit	8-bit	16-bit								
FFF00H	Port register 0	P0	R/W	√	√	–	00H	–	–	–	√	√	√	√
FFF01H	Port register 1	P1	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF02H	Port register 2	P2	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF03H	Port register 3	P3	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF04H	Port register 4	P4	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF05H	Port register 5	P5	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF06H	Port register 6	P6	R/W	√	√	–	00H	–	–	√	√	√	√	√
FFF07H	Port register 7	P7	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF08H	Port register 8	P8	R/W	√	√	–	00H	√	√	√	√	√	–	√
FFF09H	Port register 9	P9	R/W	√	√	–	00H	–	–	–	–	–	√	√
FFF0BH	Port register 11	P11	R/W	√	√	–	00H	–	–	–	–	–	√	√
FFF0CH	Port register 12	P12	R/W	√	√	–	Undefined	√	√	√	√	√	√	√
FFF0DH	Port register 13	P13	R/W	√	√	–	00H	–	–	–	–	–	√	√
FFF0EH	Port register 14	P14	R/W	√	√	–	00H	–	–	√	√	√	√	√
FFF0FH	Port register 15	P15	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF10H	Serial data register 00	TXD0/SIO00 SDR00	R/W	–	√	√	0000H	√	√	√	√	√	√	√
FFF11H		–		–	–			√	√	√	√	√	√	√
FFF12H	Serial data register 01	RXD0/SIO01 SDR01	R/W	–	√	√	0000H	√	√	√	√	√	√	√
FFF13H		–		–	–			√	√	√	√	√	√	√
FFF14H	Serial data register 12	TXD3 SDR12	R/W	–	√	√	0000H	–	–	–	–	–	√	√
FFF15H		–		–	–			–	–	–	–	–	√	√
FFF16H	Serial data register 13	RXD3 SDR13	R/W	–	√	√	0000H	–	–	–	–	–	√	√
FFF17H		–		–	–			–	–	–	–	–	√	√
FFF18H	Timer data register 00	TDR00	R/W	–	–	√	0000H	√	√	√	√	√	√	√
FFF19H														
FFF1AH	Timer data register 01	TDR01	R/W	–	–	√	0000H	√	√	√	√	√	√	√
FFF1BH														
FFF1EH	10-bit A/D conversion result register	ADCR	R	–	–	√	0000H	√	√	√	√	√	√	√
FFF1FH	8-bit A/D conversion result register	ADCRH	R	–	√	–	00H	√	√	√	√	√	√	√
FFF20H	Port mode register 0	PM0	R/W	√	√	–	FFH	–	–	–	√	√	√	√
FFF21H	Port mode register 1	PM1	R/W	√	√	–	FFH	√	√	√	√	√	√	√
FFF22H	Port mode register 2	PM2	R/W	√	√	–	FFH	√	√	√	√	√	√	√
FFF23H	Port mode register 3	PM3	R/W	√	√	–	FFH	√	√	√	√	√	√	√
FFF24H	Port mode register 4	PM4	R/W	√	√	–	FFH	√	√	√	√	√	√	√

Table 4-5. SFR List (2/6)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
				1-bit	8-bit	16-bit								
FFF25H	Port mode register 5	PM5	R/W	√	√	–	FFH	√	√	√	√	√	√	√
FFF26H	Port mode register 6	PM6	R/W	√	√	–	FFH	–	–	√	√	√	√	√
FFF27H	Port mode register 7	PM7	R/W	√	√	–	FFH	√	√	√	√	√	√	√
FFF28H	Port mode register 8	PM8	R/W	√	√	–	FFH	√	√	√	√	√	–	√
FFF29H	Port mode register 9	PM9	R/W	√	√	–	FFH	–	–	–	–	–	√	√
FFF2BH	Port mode register 11	PM11	R/W	√	√	–	FFH	–	–	–	–	–	√	√
FFF2CH	Port mode register 12	PM12	R/W	√	√	–	FFH	√	√	√	√	√	√	√
FFF2DH	Port mode register 13	PM13	R/W	√	√	–	FEH	–	–	–	–	–	–	√
FFF2EH	Port mode register 14	PM14	R/W	√	√	–	FFH	–	–	–	–	√	√	√
FFF2FH	Port mode register 15	PM15	R/W	√	√	–	FFH	√	√	√	√	√	√	√
FFF30H	A/D converter mode register	ADM	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF31H	Analog input channel specification register	ADS	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF37H	Key return mode register	KRM	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF38H	External interrupt rising edge enable register 0	EGP0	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF39H	External interrupt falling edge enable register 0	EGN0	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF3AH	External interrupt rising edge enable register 1	EGP1	R/W	√	√	–	00H	–	–	–	–	–	√	√
FFF3BH	External interrupt falling edge enable register 1	EGN1	R/W	√	√	–	00H	–	–	–	–	–	√	√
FFF3CH	Input switch control register	ISC	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF3EH	Timer input select register 0	TIS0	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF3FH	Timer input select register 1	TIS1	R/W	√	√	–	00H	–	–	–	–	–	√	√
FFF44H	Serial data register 02	TXD1/SIO10 / SDR02	R/W	–	√	√	0000H	√	√	√	√	√	√	√
FFF45H		–		–	–			√	√	√	√	√	√	√
FFF46H	Serial data register 03	RXD1 / SDR03	R/W	–	√	√	0000H	√	√	√	√	√	√	√
FFF47H		–		–	–			√	√	√	√	√	√	√
FFF48H	Serial data register 10	TXD2/SIO20 / SDR10	R/W	–	√	√	0000H	–	–	–	–	–	√	√
FFF49H		–		–	–			–	–	–	–	–	√	√
FFF4AH	Serial data register 11	RXD2 / SDR11	R/W	–	√	√	0000H	–	–	–	–	–	√	√
FFF4BH		–		–	–			–	–	–	–	–	√	√
FFF4CH	Serial data register 20	SIO40/TxD4 / SDR20	R/W	–	√	√	0000H	–	–	–	–	–	Note	Note
FFF4DH		–		–	–			–	–	–	–	–	Note	Note

Note Those are only mounted in the 78K0R/KF3-L (μ PD78F1027 and 78F1028) and the 78K0R/KG3-L (μ PD78F1029 and 78F1030).

Table 4-5. SFR List (3/6)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset	KC3-L (40 pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
				1-bit	8-bit	16-bit								
FFF4EH	Serial data register 21	SIO41/ RxD4 SDR21	R/W	–	√	√	0000H	–	–	–	–	–	Note 1	Note 1
FFF4FH		–		–	–			–	–	–	–	–	Note 1	Note 1
FFF50H	IICA shift register	IICA	R/W	–	√	–	00H	–	–	√	√	√	√	√
FFF51H	IICA status register	IICS	R	√	√	–	00H	–	–	√	√	√	√	√
FFF52H	IICA flag register	IICF	R/W	√	√	–	00H	–	–	√	√	√	√	√
FFF64H	Timer data register 02	TDR02	R/W	–	–	√	0000H	√	√	√	√	√	√	√
FFF65H														
FFF66H	Timer data register 03	TDR03	R/W	–	–	√	0000H	√	√	√	√	√	√	√
FFF67H														
FFF68H	Timer data register 04	TDR04	R/W	–	–	√	0000H	√	√	√	√	√	√	√
FFF69H														
FFF6AH	Timer data register 05	TDR05	R/W	–	–	√	0000H	√	√	√	√	√	√	√
FFF6BH														
FFF6CH	Timer data register 06	TDR06	R/W	–	–	√	0000H	√	√	√	√	√	√	√
FFF6DH														
FFF6EH	Timer data register 07	TDR07	R/W	–	–	√	0000H	√	√	√	√	√	√	√
FFF6FH														
FFF70H	Timer data register 10	TDR10	R/W	–	–	√	0000H	–	–	–	–	–	√	√
FFF71H														
FFF72H	Timer data register 11	TDR11	R/W	–	–	√	0000H	–	–	–	–	–	√	√
FFF73H														
FFF74H	Timer data register 12	TDR12	R/W	–	–	√	0000H	–	–	–	–	–	√	√
FFF75H														
FFF76H	Timer data register 13	TDR13	R/W	–	–	√	0000H	–	–	–	–	–	√	√
FFF77H														
FFF90H	Sub-count register	RSUBC	R	–	–	√	0000H	–	√	√	√	√	√	√
FFF91H														
FFF92H	Second count register	SEC	R/W	–	√	–	00H	–	√	√	√	√	√	√
FFF93H	Minute count register	MIN	R/W	–	√	–	00H	–	√	√	√	√	√	√
FFF94H	Hour count register	HOUR	R/W	–	√	–	12H Note 2	–	√	√	√	√	√	√
FFF95H	Week count register	WEEK	R/W	–	√	–	00H	–	√	√	√	√	√	√
FFF96H	Day count register	DAY	R/W	–	√	–	01H	–	√	√	√	√	√	√
FFF97H	Month count register	MONTH	R/W	–	√	–	01H	–	√	√	√	√	√	√

Notes 1. Those are only mounted in the 78K0R/KF3-L (μ PD78F1027 and 78F1028) and the 78K0R/KG3-L (μ PD78F1029 and 78F1030).

2. The value of this register is 00H if the AMPM bit (bit 3 of real-time counter control register 0 (RTCC0)) is set to 1 after reset.

Table 4-5. SFR List (4/6)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
				1-bit	8-bit	16-bit								
FFF98H	Year count register	YEAR	R/W	–	√	–	00H	–	√	√	√	√	√	√
FFF99H	Watch error correction register	SUBCUD	R/W	–	√	–	00H	–	√	√	√	√	√	√
FFF9AH	Alarm minute register	ALARMWM	R/W	–	√	–	00H	–	√	√	√	√	√	√
FFF9BH	Alarm hour register	ALARMWH	R/W	–	√	–	12H	–	√	√	√	√	√	√
FFF9CH	Alarm week register	ALARMWW	R/W	–	√	–	00H	–	√	√	√	√	√	√
FFF9DH	Real-time counter control register 0	RTCC0	R/W	√	√	–	00H	–	√	√	√	√	√	√
FFF9EH	Real-time counter control register 1	RTCC1	R/W	√	√	–	00H	–	√	√	√	√	√	√
FFF9FH	Real-time counter control register 2	RTCC2	R/W	√	√	–	00H	–	√	√	√	√	√	√
FFFA0H	Clock operation mode control register	CMC	R/W	–	√	–	00H	√	√	√	√	√	√	√
FFFA1H	Clock operation status control register	CSC	R/W	√	√	–	C0H	√	√	√	√	√	√	√
FFFA2H	Oscillation stabilization time counter status register	OSTC	R	√	√	–	00H	√	√	√	√	√	√	√
FFFA3H	Oscillation stabilization time select register	OSTS	R/W	–	√	–	07H	√	√	√	√	√	√	√
FFFA4H	System clock control register	CKC	R/W	√	√	–	09H	√	√	√	√	√	√	√
FFFA5H	Clock output select register 0	CKS0	R/W	√	√	–	00H	–	–	√	√	√	√	√
FFFA6H	Clock output select register 1	CKS1	R/W	√	√	–	00H	–	–	–	–	√	√	√
FFFA8H	Reset control flag register	RESF	R	–	√	–	Undefined Note 1	√	√	√	√	√	√	√
FFFA9H	Low-voltage detection register	LVIM	R/W	√	√	–	00H Note 2	√	√	√	√	√	√	√
FFFAAH	Low-voltage detection level select register	LVIS	R/W	√	√	–	0EH Note 3	√	√	√	√	√	√	√
FFFABH	Watchdog timer enable register	WDTE	R/W	–	√	–	1A/9A Note 4	√	√	√	√	√	√	√

Notes 1. The reset value of the RESF register varies depending on the reset source.

2. The reset value of the LVIM register varies depending on the reset source and the setting of the option byte.

3. The reset value of the LVIS register varies depending on the reset source.

4. The reset value of the WDTE register is determined by the setting of the option byte.

Table 4-5. SFR List (5/6)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
FFFB0H	DMA SFR address register 0	DSA0		R/W	–	√	–	00H	√	√	√	√	√	√	√
FFFB1H	DMA SFR address register 1	DSA1		R/W	–	√	–	00H	√	√	√	√	√	√	√
FFFB2H	DMA RAM address register 0L	DRA0L	DRA0	R/W	–	√	√	00H	√	√	√	√	√	√	√
FFFB3H	DMA RAM address register 0H	DRA0H		R/W	–	√		00H	√	√	√	√	√	√	√
FFFB4H	DMA RAM address register 1L	DRA1L	DRA1	R/W	–	√	√	00H	√	√	√	√	√	√	√
FFFB5H	DMA RAM address register 1H	DRA1H		R/W	–	√		00H	√	√	√	√	√	√	√
FFFB6H	DMA byte count register 0L	DBC0L	DBC0	R/W	–	√	√	00H	√	√	√	√	√	√	√
FFFB7H	DMA byte count register 0H	DBC0H		R/W	–	√		00H	√	√	√	√	√	√	√
FFFB8H	DMA byte count register 1L	DBC1L	DBC1	R/W	–	√	√	00H	√	√	√	√	√	√	√
FFFB9H	DMA byte count register 1H	DBC1H		R/W	–	√		00H	√	√	√	√	√	√	√
FFFBAH	DMA mode control register 0	DMC0		R/W	√	√	–	00H	√	√	√	√	√	√	√
FFFBBH	DMA mode control register 1	DMC1		R/W	√	√	–	00H	√	√	√	√	√	√	√
FFFBCH	DMA operation control register 0	DRC0		R/W	√	√	–	00H	√	√	√	√	√	√	√
FFFBDH	DMA operation control register 1	DRC1		R/W	√	√	–	00H	√	√	√	√	√	√	√
FFFBEH	Back ground event control register	BECTL		R/W	√	√	–	00H	√	√	√	√	√	√	√
FFFC0H	–	PFCMD[Note]		–	–	–	–	Undefined	√	√	√	√	√	√	√
FFFC2H	–	PFS[Note]		–	–	–	–	Undefined	√	√	√	√	√	√	√
FFFC4H	–	FLPMC[Note]		–	–	–	–	Undefined	√	√	√	√	√	√	√
FFFD0H	Interrupt request flag register 2L	IF2L	IF2	R/W	√	√	√	00H	√	√	√	√	√	√	√
FFFD1H	Interrupt request flag register 2H	IF2H		R/W	√	√		00H	–	–	–	–	–	√	√
FFFD4H	Interrupt mask flag register 2L	MK2L	MK2	R/W	√	√	√	FFH	√	√	√	√	√	√	√
FFFD5H	Interrupt mask flag register 2H	MK2H		R/W	√	√		FFH	–	–	–	–	–	√	√
FFFD8H	Priority specification flag register 02L	PR02L	PR02	R/W	√	√	√	FFH	√	√	√	√	√	√	√
FFFD9H	Priority specification flag register 02H	PR02H		R/W	√	√		FFH	–	–	–	–	–	√	√
FFFDCH	Priority specification flag register 12L	PR12L	PR12	R/W	√	√	√	FFH	√	√	√	√	√	√	√
FFFDDH	Priority specification flag register 12H	PR12H		R/W	√	√		FFH	–	–	–	–	–	√	√
FFFE0H	Interrupt request flag register 0L	IF0L	IF0	R/W	√	√	√	00H	√	√	√	√	√	√	√
FFFE1H	Interrupt request flag register 0H	IF0H		R/W	√	√		00H	√	√	√	√	√	√	√
FFFE2H	Interrupt request flag register 1L	IF1L	IF1	R/W	√	√	√	00H	√	√	√	√	√	√	√
FFFE3H	Interrupt request flag register 1H	IF1H		R/W	√	√		00H	√	√	√	√	√	√	√
FFFE4H	Interrupt mask flag register 0L	MK0L	MK0	R/W	√	√	√	FFH	√	√	√	√	√	√	√
FFFE5H	Interrupt mask flag register 0H	MK0H		R/W	√	√		FFH	√	√	√	√	√	√	√

Note Do not directly operate this SFR, because it is to be used in the self programming library.

Table 4-5. SFR List (6/6)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit							
FFFE6H	Interrupt mask flag register 1L	MK1L	MK1	R/W	√	√	√	FFH	√	√	√	√	√	√
FFFE7H	Interrupt mask flag register 1H	MK1H		R/W	√	√		FFH	√	√	√	√	√	√
FFFE8H	Priority specification flag register 00L	PR00L	PR00	R/W	√	√	√	FFH	√	√	√	√	√	√
FFFE9H	Priority specification flag register 00H	PR00H		R/W	√	√		FFH	√	√	√	√	√	√
FFFEAH	Priority specification flag register 01L	PR01L	PR01	R/W	√	√	√	FFH	√	√	√	√	√	√
FFFEBH	Priority specification flag register 01H	PR01H		R/W	√	√		FFH	√	√	√	√	√	√
FFFECH	Priority specification flag register 10L	PR10L	PR10	R/W	√	√	√	FFH	√	√	√	√	√	√
FFFEDH	Priority specification flag register 10H	PR10H		R/W	√	√		FFH	√	√	√	√	√	√
FFFEEH	Priority specification flag register 11L	PR11L	PR11	R/W	√	√	√	FFH	√	√	√	√	√	√
FFFEFH	Priority specification flag register 11H	PR11H		R/W	√	√		FFH	√	√	√	√	√	√
FFFF0H	Multiplication/division data register A (L)	MDAL/MULA		R/W	–	–	√	0000H	√	√	√	√	√	√
FFFF1H														
FFFF2H	Multiplication/division data register A (H)	MDAH/MULB		R/W	–	–	√	0000H	√	√	√	√	√	√
FFFF3H														
FFFF4H	Multiplication/division data register B (H)	MDBH/MULOH		R/W	–	–	√	0000H	√	√	√	√	√	√
FFFF5H														
FFFF6H	Multiplication/division data register B (L)	MDBL/MULOL		R/W	–	–	√	0000H	√	√	√	√	√	√
FFFF7H														
FFFFEH	Processor mode control register	PMC		R/W	√	√	–	00H	√	√	√	√	√	√

Remark For extended SFRs (2nd SFRs), see **Table 4-6 Extended SFR (2nd SFR) List**.

4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)

Unlike a general-purpose register, each extended SFR (2nd SFR) has a special function.

Extended SFRs are allocated to the F0000H to F07FFH area. SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

Extended SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (!addr16.bit). This manipulation can also be specified with an address.
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (!addr16). This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (!addr16). When specifying an address, describe an even address.

Table 4-6 gives a list of the extended SFRs. The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of an extended SFR. It is a reserved word in the RA78K0R, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0R. When using the RA78K0R, ID78K0R-QB, and SM+ for 78K0R, symbols can be written as an instruction operand.
- R/W
  Indicates whether the corresponding extended SFR can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulable bit units
  "√" indicates the manipulable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Caution Do not access addresses to which extended SFRs are not assigned.

Remark For SFRs in the SFR area, see **4.2.4 Special function registers (SFRs)**.

Table 4-6. Extended SFR (2nd SFR) List (1/8)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
				1-bit	8-bit	16-bit								
F0017H	A/D port configuration register	ADPC	R/W	–	√	–	10H	√	√	√	√	√	√	√
F0030H	Pull-up resistor option register 0	PU0	R/W	√	√	–	00H	–	–	–	√	√	√	√
F0031H	Pull-up resistor option register 1	PU1	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0033H	Pull-up resistor option register 3	PU3	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0034H	Pull-up resistor option register 4	PU4	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0035H	Pull-up resistor option register 5	PU5	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0036H	Pull-up resistor option register 6	PU6	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0037H	Pull-up resistor option register 7	PU7	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0038H	Pull-up resistor option register 8	PU8	R/W	√	√	–	00H	–	–	–	–	–	–	√
F0039H	Pull-up resistor option register 9	PU9	R/W	√	√	–	00H	–	–	–	–	–	√	√
F003BH	Pull-up resistor option register 11	PU11	R/W	√	√	–	00H	–	–	–	–	–	√	√
F003CH	Pull-up resistor option register 12	PU12	R/W	√	√	–	00H	√	√	√	√	√	√	√
F003DH	Pull-up resistor option register 13	PU13	R/W	√	√	–	00H	–	–	–	–	–	–	√
F003EH	Pull-up resistor option register 14	PU14	R/W	√	√	–	00H	–	–	–	–	√	√	√
F0040H	Port input mode register 0	PIM0	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0041H	Port input mode register 1	PIM1	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0043H	Port input mode register 3	PIM3	R/W	√	√	–	00H	√	√	√	√	√	–	–
F0047H	Port input mode register 7	PIM7	R/W	√	√	–	00H	√	√	√	√	√	–	–
F0048H	Port input mode register 8	PIM8	R/W	√	√	–	00H	√	√	√	√	√	–	–
F004EH	Port input mode register 14	PIM14	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0050H	Port output mode register 0	POM0	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0051H	Port output mode register 1	POM1	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0053H	Port output mode register 0	POM3	R/W	√	√	–	00H	√	√	√	√	√	–	–
F0057H	Port output mode register 1	POM7	R/W	√	√	–	00H	√	√	√	√	√	–	–
F005EH	Port output mode register 14	POM14	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0060H	Noise filter enable register 0	NFEN0	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0061H	Noise filter enable register 1	NFEN1	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0062H	Noise filter enable register 2	NFEN2	R/W	√	√	–	00H	√	√	√	√	√	√	√
F00E0H	Multiplication/division data register C (L)	MDCL	R	–	–	√	0000H	√	√	√	√	√	√	√
F00E2H	Multiplication/division data register C (H)	MDCH	R	–	–	√	0000H	√	√	√	√	√	√	√
F00E8H	Multiplication/division control register	MDUC	R/W	√	√	–	00H	√	√	√	√	√	√	√
F00F0H	Peripheral enable register 0	PER0	R/W	√	√	–	00H	√	√	√	√	√	√	√
F00F1H	Peripheral enable register 1	PER1	R/W	√	√	–	00H	√	√	√	√	√	Note	Note
F00F2H	Peripheral enable register 2	PER2	R/W	√	√	–	00H	√	√	√	√	√	–	–

Note Those are only mounted in the 78K0R/KF3-L (μPD78F1027 and 78F1028) and the 78K0R/KG3-L (μPD78F1029 and 78F1030).

Table 4-6. Extended SFR (2nd SFR) List (2/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
F00F3H	Operation speed mode control register	OSMC		R/W	–	√	–	00H	√	√	√	√	√	√	√
F00F4H	Regulator mode control register	RMC		R/W	–	√	–	00H	√	√	√	√	√	√	√
F00F6H	20 MHz internal high-speed oscillation control register	DSCCTL		R/W	√	√	–	00H	√	√	√	√	√	√	√
F00FEH	BCD adjust result register	BCDADJ		R	–	√	–	Undefined	√	√	√	√	√	√	√
F0100H	Serial status register 00	SSR00L	SSR00	R	–	√	√	0000H	√	√	√	√	√	√	√
F0101H		–			–	–			√	√	√	√	√	√	√
F0102H	Serial status register 01	SSR01L	SSR01	R	–	√	√	0000H	√	√	√	√	√	√	√
F0103H		–			–	–			√	√	√	√	√	√	√
F0104H	Serial status register 02	SSR02L	SSR02	R	–	√	√	0000H	√	√	√	√	√	√	√
F0105H		–			–	–			√	√	√	√	√	√	√
F0106H	Serial status register 03	SSR03L	SSR03	R	–	√	√	0000H	√	√	√	√	√	√	√
F0107H		–			–	–			√	√	√	√	√	√	√
F0108H	Serial flag clear trigger register 00	SIR00L	SIR00	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F0109H		–			–	–			√	√	√	√	√	√	√
F010AH	Serial flag clear trigger register 01	SIR01L	SIR01	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F010BH		–			–	–			√	√	√	√	√	√	√
F010CH	Serial flag clear trigger register 02	SIR02L	SIR02	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F010DH		–			–	–			√	√	√	√	√	√	√
F010EH	Serial flag clear trigger register 03	SIR03L	SIR03	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F010FH		–			–	–			√	√	√	√	√	√	√
F0110H	Serial mode register 00	SMR00		R/W	–	–	√	0020H	√	√	√	√	√	√	√
F0111H															
F0112H	Serial mode register 01	SMR01		R/W	–	–	√	0020H	√	√	√	√	√	√	√
F0113H															
F0114H	Serial mode register 02	SMR02		R/W	–	–	√	0020H	√	√	√	√	√	√	√
F0115H															
F0116H	Serial mode register 03	SMR03		R/W	–	–	√	0020H	√	√	√	√	√	√	√
F0117H															
F0118H	Serial communication operation setting register 00	SCR00		R/W	–	–	√	0087H	√	√	√	√	√	√	√
F0119H															
F011AH	Serial communication operation setting register 01	SCR01		R/W	–	–	√	0087H	√	√	√	√	√	√	√
F011BH															
F011CH	Serial communication operation setting register 02	SCR02		R/W	–	–	√	0087H	√	√	√	√	√	√	√
F011DH															
F011EH	Serial communication operation setting register 03	SCR03		R/W	–	–	√	0087H	√	√	√	√	√	√	√
F011FH															

Table 4-6. Extended SFR (2nd SFR) List (3/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
F0120H	Serial channel enable status register 0	SE0L	SE0	R	√	√	√	0000H	√	√	√	√	√	√	√
F0121H		–			–	–			√	√	√	√	√	√	√
F0122H	Serial channel start register 0	SS0L	SS0	R/W	√	√	√	0000H	√	√	√	√	√	√	√
F0123H		–			–	–			√	√	√	√	√	√	√
F0124H	Serial channel stop register 0	ST0L	ST0	R/W	√	√	√	0000H	√	√	√	√	√	√	√
F0125H		–			–	–			√	√	√	√	√	√	√
F0126H	Serial clock select register 0	SPS0L	SPS0	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F0127H		–			–	–			√	√	√	√	√	√	√
F0128H	Serial output register 0	SO0		R/W	–	–	√	0F0FH	√	√	√	√	√	√	√
F0129H															
F012AH	Serial output enable register 0	SOE0L	SOE0	R/W	√	√	√	0000H	√	√	√	√	√	√	√
F012BH		–			–	–			√	√	√	√	√	√	√
F0134H	Serial output level register 0	SOL0L	SOL0	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F0135H		–			–	–			√	√	√	√	√	√	√
F0140H	Serial status register 10	SSR10L	SSR10	R	–	√	√	0000H	–	–	–	–	–	√	√
F0141H		–			–	–			–	–	–	–	–	√	√
F0142H	Serial status register 11	SSR11L	SSR11	R	–	√	√	0000H	–	–	–	–	–	√	√
F0143H		–			–	–			–	–	–	–	–	√	√
F0144H	Serial status register 12	SSR12L	SSR12	R	–	√	√	0000H	–	–	–	–	–	√	√
F0145H		–			–	–			–	–	–	–	–	√	√
F0146H	Serial status register 13	SSR13L	SSR13	R	–	√	√	0000H	–	–	–	–	–	√	√
F0147H		–			–	–			–	–	–	–	–	√	√
F0148H	Serial flag clear trigger register 10	SIR10L	SIR10	R/W	–	√	√	0000H	–	–	–	–	–	√	√
F0149H		–			–	–			–	–	–	–	–	√	√
F014AH	Serial flag clear trigger register 11	SIR11L	SIR11	R/W	–	√	√	0000H	–	–	–	–	–	√	√
F014BH		–			–	–			–	–	–	–	–	√	√
F014CH	Serial flag clear trigger register 12	SIR12L	SIR12	R/W	–	√	√	0000H	–	–	–	–	–	√	√
F014DH		–			–	–			–	–	–	–	–	√	√
F014EH	Serial flag clear trigger register 13	SIR13L	SIR13	R/W	–	√	√	0000H	–	–	–	–	–	√	√
F014FH		–			–	–			–	–	–	–	–	√	√
F0150H	Serial mode register 10	SMR10		R/W	–	–	√	0020H	–	–	–	–	–	√	√
F0151H															
F0152H	Serial mode register 11	SMR11		R/W	–	–	√	0020H	–	–	–	–	–	√	√
F0153H															
F0154H	Serial mode register 12	SMR12		R/W	–	–	√	0020H	–	–	–	–	–	√	√
F0155H															
F0156H	Serial mode register 13	SMR13		R/W	–	–	√	0020H	–	–	–	–	–	√	√
F0157H															

Table 4-6. Extended SFR (2nd SFR) List (4/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
F0158H	Serial communication operation setting register 10	SCR10		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F0159H															
F015AH	Serial communication operation setting register 11	SCR11		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F015BH															
F015CH	Serial communication operation setting register 12	SCR12		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F015DH															
F015EH	Serial communication operation setting register 13	SCR13		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F015FH															
F0160H	Serial channel enable status register 1	SE1L	SE1	R	√	√	√	0000H	–	–	–	–	–	√	√
F0161H		–			–	–			–	–	–	–	–	√	√
F0162H	Serial channel start register 1	SS1L	SS1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F0163H		–			–	–			–	–	–	–	–	√	√
F0164H	Serial channel stop register 1	ST1L	ST1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F0165H		–			–	–			–	–	–	–	–	√	√
F0166H	Serial clock select register 1	SPS1L	SPS1	R/W	–	√	√	0000H	–	–	–	–	–	√	√
F0167H		–			–	–			–	–	–	–	–	√	√
F0168H	Serial output register 1	SO1		R/W	–	–	√	0F0FH	–	–	–	–	–	√	√
F0169H															
F016AH	Serial output enable register 1	SOE1L	SOE1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F016BH		–			–	–			–	–	–	–	–	√	√
F0174H	Serial output level register 1	SOL1L	SOL1	R/W	–	√	√	0000H	–	–	–	–	–	√	√
F0175H		–			–	–			–	–	–	–	–	√	√
F0180H	Timer counter register 00	TCR00		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0181H															
F0182H	Timer counter register 01	TCR01		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0183H															
F0184H	Timer counter register 02	TCR02		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0185H															
F0186H	Timer counter register 03	TCR03		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0187H															
F0188H	Timer counter register 04	TCR04		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0189H															
F018AH	Timer counter register 05	TCR05		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F018BH															
F018CH	Timer counter register 06	TCR06		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F018DH															
F018EH	Timer counter register 07	TCR07		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F018FH															

Table 4-6. Extended SFR (2nd SFR) List (5/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
F0190H	Timer mode register 00	TMR00		R/W	–	–	√	0000H	√	√	√	√	√	√	√
F0191H															
F0192H	Timer mode register 01	TMR01		R/W	–	–	√	0000H	√	√	√	√	√	√	√
F0193H															
F0194H	Timer mode register 02	TMR02		R/W	–	–	√	0000H	√	√	√	√	√	√	√
F0195H															
F0196H	Timer mode register 03	TMR03		R/W	–	–	√	0000H	√	√	√	√	√	√	√
F0197H															
F0198H	Timer mode register 04	TMR04		R/W	–	–	√	0000H	√	√	√	√	√	√	√
F0199H															
F019AH	Timer mode register 05	TMR05		R/W	–	–	√	0000H	√	√	√	√	√	√	√
F019BH															
F019CH	Timer mode register 06	TMR06		R/W	–	–	√	0000H	√	√	√	√	√	√	√
F019DH															
F019EH	Timer mode register 07	TMR07		R/W	–	–	√	0000H	√	√	√	√	√	√	√
F019FH															
F01A0H	Timer status register 00	TSR00L	TSR00	R	–	√	√	0000H	√	√	√	√	√	√	√
F01A1H		–			–	–			√	√	√	√	√	√	√
F01A2H	Timer status register 01	TSR01L	TSR01	R	–	√	√	0000H	√	√	√	√	√	√	√
F01A3H		–			–	–			√	√	√	√	√	√	√
F01A4H	Timer status register 02	TSR02L	TSR02	R	–	√	√	0000H	√	√	√	√	√	√	√
F01A5H		–			–	–			√	√	√	√	√	√	√
F01A6H	Timer status register 03	TSR03L	TSR03	R	–	√	√	0000H	√	√	√	√	√	√	√
F01A7H		–			–	–			√	√	√	√	√	√	√
F01A8H	Timer status register 04	TSR04L	TSR04	R	–	√	√	0000H	√	√	√	√	√	√	√
F01A9H		–			–	–			√	√	√	√	√	√	√
F01AAH	Timer status register 05	TSR05L	TSR05	R	–	√	√	0000H	√	√	√	√	√	√	√
F01ABH		–			–	–			√	√	√	√	√	√	√
F01ACH	Timer status register 06	TSR06L	TSR06	R	–	√	√	0000H	√	√	√	√	√	√	√
F01ADH		–			–	–			√	√	√	√	√	√	√
F01AEH	Timer status register 07	TSR07L	TSR07	R	–	√	√	0000H	√	√	√	√	√	√	√
F01AFH		–			–	–			√	√	√	√	√	√	√
F01B0H	Timer channel enable status register 0	TE0L	TE0	R	√	√	√	0000H	√	√	√	√	√	√	√
F01B1H		–			–	–			√	√	√	√	√	√	√
F01B2H	Timer channel start register 0	TS0L	TS0	R/W	√	√	√	0000H	√	√	√	√	√	√	√
F01B3H		–			–	–			√	√	√	√	√	√	√
F01B4H	Timer channel stop register 0	TT0L	TT0	R/W	√	√	√	0000H	√	√	√	√	√	√	√
F01B5H		–			–	–			√	√	√	√	√	√	√

Table 4-6. Extended SFR (2nd SFR) List (6/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
F01B6H	Timer clock select register 0	TPS0L	TPS0	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F01B7H		–			–	–			√	√	√	√	√	√	√
F01B8H	Timer output register 0	TO0L	TO0	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F01B9H		–			–	–			√	√	√	√	√	√	√
F01BAH	Timer output enable register 0	TOE0L	TOE0	R/W	√	√	√	0000H	√	√	√	√	√	√	√
F01BBH		–			–	–			√	√	√	√	√	√	√
F01BCH	Timer output level register 0	TOL0L	TOL0	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F01BDH		–			–	–			√	√	√	√	√	√	√
F01BEH	Timer output mode register 0	TOM0L	TOM0	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F01BFH		–			–	–			√	√	√	√	√	√	√
F01C0H	Timer counter register 10	TCR10		R	–	–	√	FFFFH	–	–	–	–	–	√	√
F01C1H															
F01C2H	Timer counter register 11	TCR11		R	–	–	√	FFFFH	–	–	–	–	–	√	√
F01C3H															
F01C4H	Timer counter register 12	TCR12		R	–	–	√	FFFFH	–	–	–	–	–	√	√
F01C5H															
F01C6H	Timer counter register 13	TCR13		R	–	–	√	FFFFH	–	–	–	–	–	√	√
F01C7H															
F01C8H	Timer mode register 10	TMR10		R/W	–	–	√	0000H	–	–	–	–	–	√	√
F01C9H															
F01CAH	Timer mode register 11	TMR11		R/W	–	–	√	0000H	–	–	–	–	–	√	√
F01CBH															
F01CCH	Timer mode register 12	TMR12		R/W	–	–	√	0000H	–	–	–	–	–	√	√
F01CDH															
F01CEH	Timer mode register 13	TMR13		R/W	–	–	√	0000H	–	–	–	–	–	√	√
F01CFH															
F01D0H	Timer status register 10	TSR10L	TSR10	R	–	√	√	0000H	–	–	–	–	–	√	√
F01D1H		–			–	–			–	–	–	–	–	√	√
F01D2H	Timer status register 11	TSR11L	TSR11	R	–	√	√	0000H	–	–	–	–	–	√	√
F01D3H		–			–	–			–	–	–	–	–	√	√
F01D4H	Timer status register 12	TSR12L	TSR12	R	–	√	√	0000H	–	–	–	–	–	√	√
F01D5H		–			–	–			–	–	–	–	–	√	√
F01D6H	Timer status register 13	TSR13L	TSR13	R	–	√	√	0000H	–	–	–	–	–	√	√
F01D7H		–			–	–			–	–	–	–	–	√	√
F01D8H	Timer channel enable status register 1	TE1L	TE1	R	√	√	√	0000H	–	–	–	–	–	√	√
F01D9H		–			–	–			–	–	–	–	–	√	√
F01DAH	Timer channel start register 1	TS1L	TS1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F01DBH		–			–	–			–	–	–	–	–	√	√

Table 4-6. Extended SFR (2nd SFR) List (7/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit							
F01DCH	Timer channel stop register 1	TT1L	TT1	R/W	√	√	√	0000H	–	–	–	–	√	√
F01DDH		–			–	–			–	–	–	–	√	√
F01DEH	Timer clock select register 1	TPS1L	TPS1	R/W	–	√	√	0000H	–	–	–	–	√	√
F01DFH		–			–	–			–	–	–	–	√	√
F01E0H	Timer output register 1	TO1L	TO1	R/W	–	√	√	0000H	–	–	–	–	√	√
F01E1H		–			–	–			–	–	–	–	√	√
F01E2H	Timer output enable register 1	TOE1L	TOE1	R/W	√	√	√	0000H	–	–	–	–	√	√
F01E3H		–			–	–			–	–	–	–	√	√
F01E4H	Timer output level register 1	TOL1L	TOL1	R/W	–	√	√	0000H	–	–	–	–	√	√
F01E5H		–			–	–			–	–	–	–	√	√
F01E6H	Timer output mode register 1	TOM1L	TOM1	R/W	–	√	√	0000H	–	–	–	–	√	√
F01B7H		–			–	–			–	–	–	–	√	√
F0200H	Serial status register 20	SSR20L	SSR20	R/W	–	√	√	0000H	–	–	–	–	Note	Note
F0201H		–			–	–			–	–	–	–	Note	Note
F0202H	Serial status register 21	SSR21L	SSR21	R/W	–	√	√	0000H	–	–	–	–	Note	Note
F0203H		–			–	–			–	–	–	–	Note	Note
F0204H	Serial flag clear trigger register 20	SIR20L	SIR20	R/W	–	√	√	0000H	–	–	–	–	Note	Note
F0205H		–			–	–			–	–	–	–	Note	Note
F0206H	Serial flag clear trigger register 21	SIR21L	SIR21	R/W	–	√	√	0000H	–	–	–	–	Note	Note
F0207H		–			–	–			–	–	–	–	Note	Note
F0208H	Serial mode register 20	SMR20		R/W	–	–	√	0020H	–	–	–	–	Note	Note
F0209H														
F020AH	Serial mode register 21	SMR21		R/W	–	–	√	0020H	–	–	–	–	Note	Note
F020BH														
F020CH	Serial communication operation setting register 20	SCR20		R/W	–	–	√	0087H	–	–	–	–	Note	Note
F020DH														
F020EH	Serial communication operation setting register 21	SCR21		R/W	–	–	√	0087H	–	–	–	–	Note	Note
F020FH														
F0210H	Serial channel enable status register 2	SE2L	SE2	R	√	√	√	0000H	–	–	–	–	Note	Note
F0211H		–			–	–			–	–	–	–	Note	Note
F0212H	Serial channel start register 2	SS2L	SS2	R/W	√	√	√	0000H	–	–	–	–	Note	Note
F0213H		–			–	–			–	–	–	–	Note	Note
F0214H	Serial channel stop register 2	ST2L	ST2	R/W	√	√	√	0000H	–	–	–	–	Note	Note
F0215H		–			–	–			–	–	–	–	Note	Note
F0216H	Serial clock select register2	SPS2L	SPS2	R/W	√	√	√	0000H	–	–	–	–	Note	Note
F0217H		–			–	–			–	–	–	–	Note	Note

Note Those are only mounted in the 78K0R/KF3-L (μPD78F1027 and 78F1028) and the 78K0R/KG3-L (μPD78F1029 and 78F1030).

Table 4-6. Extended SFR (2nd SFR) List (8/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
F0218H	Serial output register 2	SO2		R/W	–	–	√	0303H	–	–	–	–	–	Note	Note
F0219H									–	–	–	–	–	Note	Note
F021AH	Serial output enable register 2	SOE2L	SOE2	R/W	√	√	√	0000H	–	–	–	–	–	Note	Note
F021BH		–			–	–			–	–	–	–	–	Note	Note
F0220H	Serial output level register 2	SOL2L	SOL2	R/W	√	√	√	0000H	–	–	–	–	–	Note	Note
F0221H		–			–	–			–	–	–	–	–	Note	Note
F0230H	IICA control register 0	IICCTL0		R/W	√	√	–	00H	–	–	√	√	√	√	√
F0231H	IICA control register 1	IICCTL1		R/W	√	√	–	00H	–	–	√	√	√	√	√
F0232H	IICA low-level width setting register	IICWL		R/W	–	√	–	FFH	–	–	√	√	√	√	√
F0233H	IICA high-level width setting register	IICWH		R/W	–	√	–	FFH	–	–	√	√	√	√	√
F0234H	Slave address register	SVA		R/W	–	√	–	00H	–	√	√	√	√	√	√
F0240H	Programmable gain amplifier control register	OAM		R/W	√	√	–	00H	√	√	√	√	√	–	–
F0241H	Comparator 0 control register	C0CTL		R/W	√	√	–	00H	√	√	√	√	√	–	–
F0242H	Comparator 0 internal reference voltage setting register	C0RVM		R/W	√	√	–	00H	√	√	√	√	√	–	–
F0243H	Comparator 1 control register	C1CTL		R/W	√	√	–	00H	√	√	√	√	√	–	–
F0244H	Comparator 1 internal reference voltage setting register	C1RVM		R/W	√	√	–	00H	√	√	√	√	√	–	–

Note Those are only mounted in the 78K0R/KF3-L (μ PD78F1027 and 78F1028) and the 78K0R/KG3-L (μ PD78F1029 and 78F1030).

Remark For SFRs in the SFR area, see **Table 4-5 SFR List**.

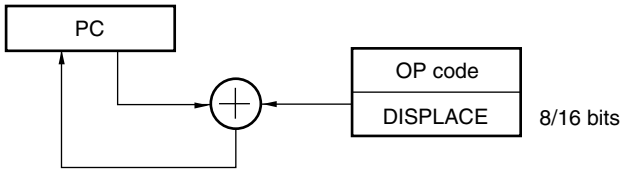
4.3 Instruction Address Addressing

4.3.1 Relative addressing

[Function]

Relative addressing stores in the program counter (PC) the result of adding a displacement value included in the instruction word (signed complement data: −128 to +127 or −32768 to +32767) to the program counter (PC)'s value (the start address of the next instruction), and specifies the program address to be used as the branch destination. Relative addressing is applied only to branch instructions.

Figure 4-26. Outline of Relative Addressing



4.3.2 Immediate addressing

[Function]

Immediate addressing stores immediate data of the instruction word in the program counter, and specifies the program address to be used as the branch destination.

For immediate addressing, CALL !!addr20 or BR !!addr20 is used to specify 20-bit addresses and CALL !addr16 or BR !addr16 is used to specify 16-bit addresses. 0000 is set to the higher 4 bits when specifying 16-bit addresses.

Figure 4-27. Example of CALL !!addr20/BR !!addr20

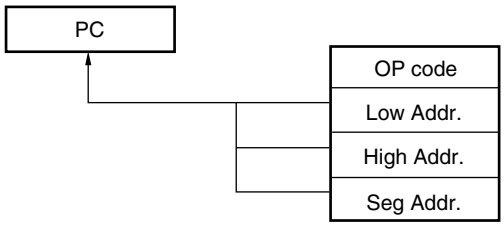
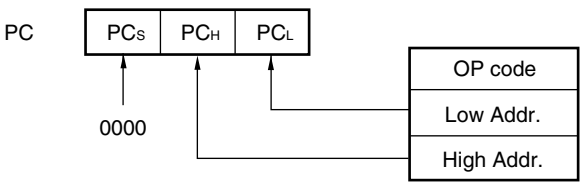


Figure 4-28. Example of CALL !addr16/BR !addr16



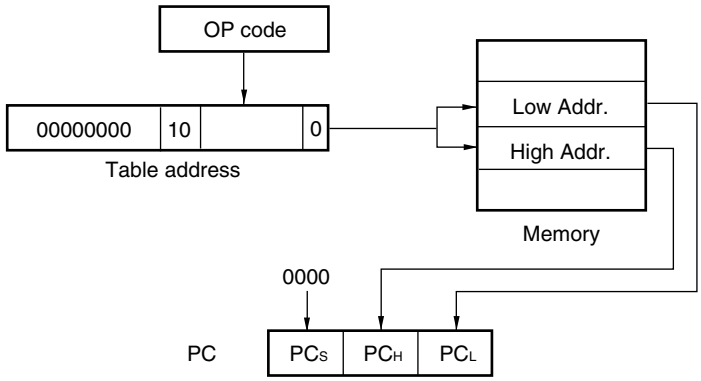
4.3.3 Table indirect addressing

[Function]

Table indirect addressing specifies a table address in the CALLT table area (0080H to 00BFH) with the 5-bit immediate data in the instruction word, stores the contents at that table address and the next address in the program counter (PC) as 16-bit data, and specifies the program address. Table indirect addressing is applied only for CALLT instructions.

In the 78K0R microcontrollers, branching is enabled only to the 64 KB space from 00000H to 0FFFFH.

Figure 4-29. Outline of Table Indirect Addressing

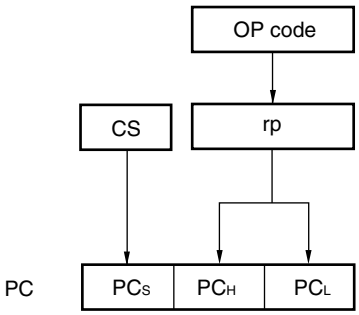


4.3.4 Register direct addressing

[Function]

Register direct addressing stores in the program counter (PC) the contents of a general-purpose register pair (AX/BC/DE/HL) and CS register of the current register bank specified with the instruction word as 20-bit data, and specifies the program address. Register direct addressing can be applied only to the CALL AX, BC, DE, HL, and BR AX instructions.

Figure 4-30. Outline of Register Direct Addressing



4.4 Addressing for Processing Data Addresses

4.4.1 Implied addressing

[Function]

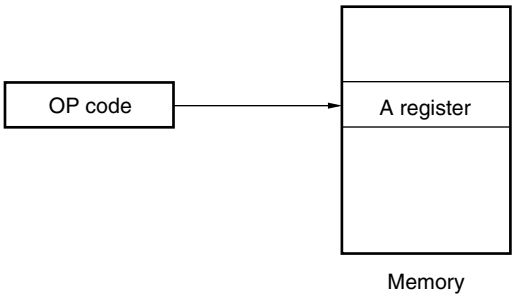
Instructions for accessing registers (such as accumulators) that have special functions are directly specified with the instruction word, without using any register specification field in the instruction word.

[Operand format]

Because implied addressing can be automatically employed with an instruction, no particular operand format is necessary.

Implied addressing can be applied only to MULU X.

Figure 4-31. Outline of Implied Addressing



4.4.2 Register addressing

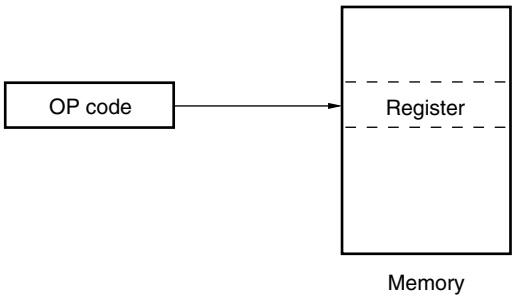
[Function]

Register addressing accesses a general-purpose register as an operand. The instruction word of 3-bit long is used to select an 8-bit register and the instruction word of 2-bit long is used to select a 16-bit register.

[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

Figure 4-32. Outline of Register Addressing



4.4.3 Direct addressing

[Function]

Direct addressing uses immediate data in the instruction word as an operand address to directly specify the target address.

[Operand format]

Identifier	Description
ADDR16	Label or 16-bit immediate data (only the space from F0000H to FFFFFH is specifiable)
ES: ADDR16	Label or 16-bit immediate data (higher 4-bit addresses are specified by the ES register)

Figure 4-33. Example of ADDR16

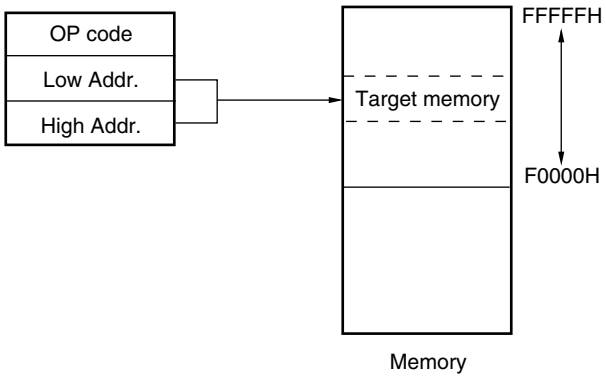
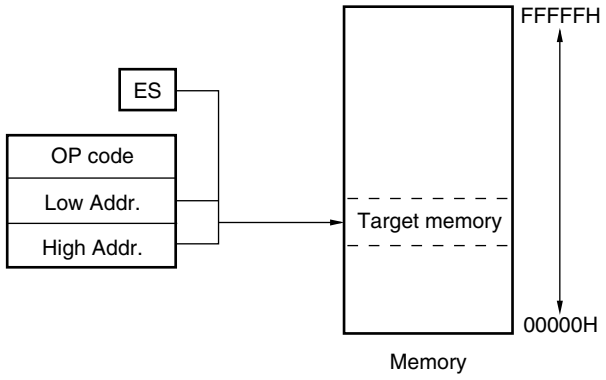


Figure 4-34. Example of ES:ADDR16



4.4.4 Short direct addressing

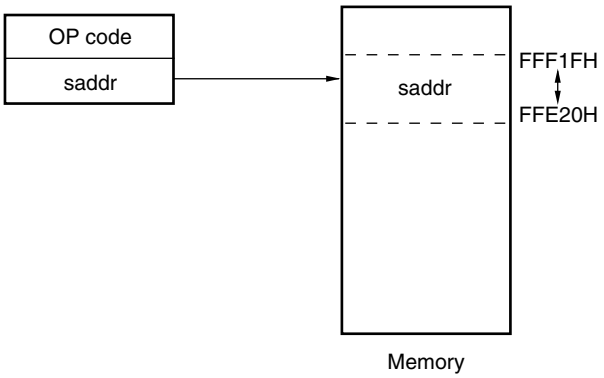
[Function]

Short direct addressing directly specifies the target addresses using 8-bit data in the instruction word. This type of addressing is applied only to the space from FFE20H to FFF1FH.

[Operand format]

Identifier	Description
SADDR	Label, FFE20H to FFF1FH immediate data, or 0FE20H to 0FF1FH immediate data (only the space from FFE20H to FFF1FH is specifiable)
SADDRP	Label, FFE20H to FFF1FH immediate data, or 0FE20H to 0FF1FH immediate data (even address only) (only the space from FFE20H to FFF1FH is specifiable)

Figure 4-35. Outline of Short Direct Addressing



Remark SADDR and SADDRP are used to describe the values of addresses FE20H to FF1FH with 16-bit immediate data (higher 4 bits of actual address are omitted), and the values of addresses FFE20H to FFF1FH with 20-bit immediate data.

Regardless of whether SADDR or SADDRP is used, addresses within the space from FFE20H to FFF1FH are specified for the memory.

4.4.5 SFR addressing

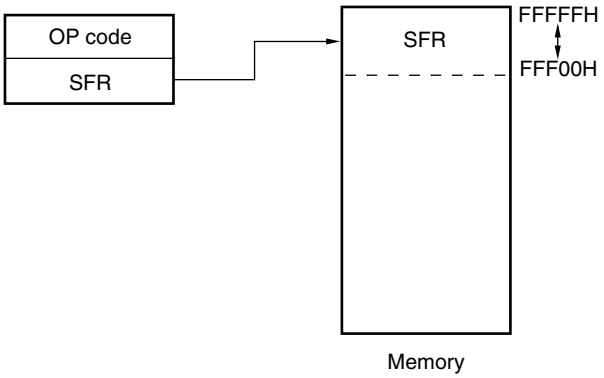
[Function]

SFR addressing directly specifies the target SFR addresses using 8-bit data in the instruction word. This type of addressing is applied only to the space from FFF00H to FFFFFH.

[Operand format]

Identifier	Description
SFR	SFR name
SFRP	16-bit-manipulatable SFR name (even address only)

Figure 4-36. Outline of SFR Addressing



4.4.6 Register indirect addressing

[Function]

Register indirect addressing directly specifies the target addresses using the contents of the register pair specified with the instruction word as an operand address.

[Operand format]

Identifier	Description
–	[DE], [HL] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[DE], ES:[HL] (higher 4-bit addresses are specified by the ES register)

Figure 4-37. Example of [DE], [HL]

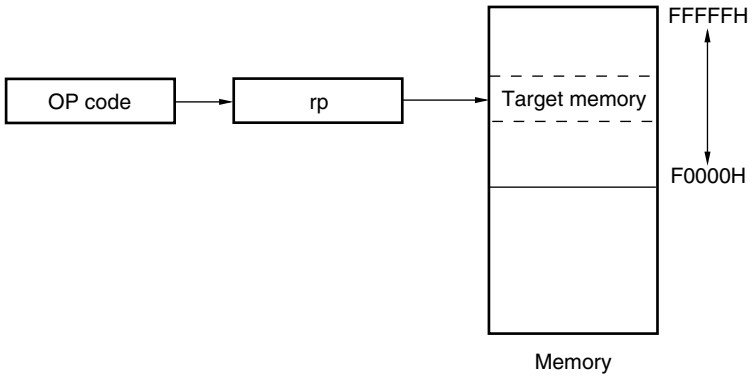
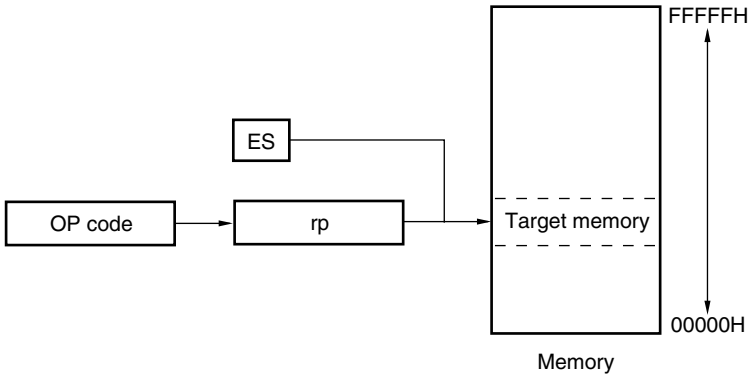


Figure 4-38. Example of ES:[DE], ES:[HL]



4.4.7 Based addressing

[Function]

Based addressing uses the contents of a register pair specified with the instruction word as a base address, and 8-bit immediate data or 16-bit immediate data as offset data. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
–	[HL + byte], [DE + byte], [SP + byte] (only the space from F0000H to FFFFFH is specifiable)
–	word[B], word[C] (only the space from F0000H to FFFFFH is specifiable)
–	word[BC] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[HL + byte], ES:[DE + byte] (higher 4-bit addresses are specified by the ES register)
–	ES:word[B], ES:word[C] (higher 4-bit addresses are specified by the ES register)
–	ES:word[BC] (higher 4-bit addresses are specified by the ES register)

Figure 4-39. Example of [SP+byte]

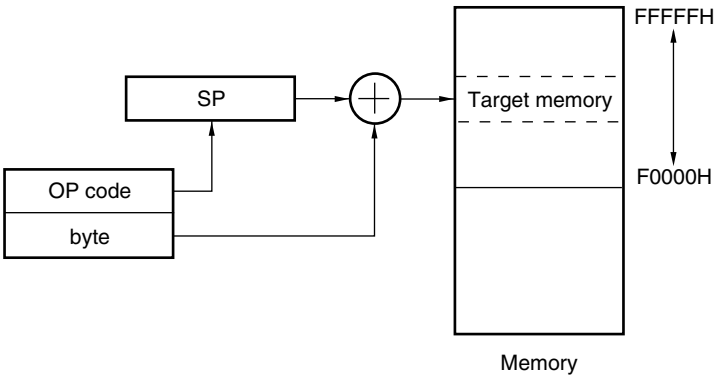


Figure 4-40. Example of [HL + byte], [DE + byte]

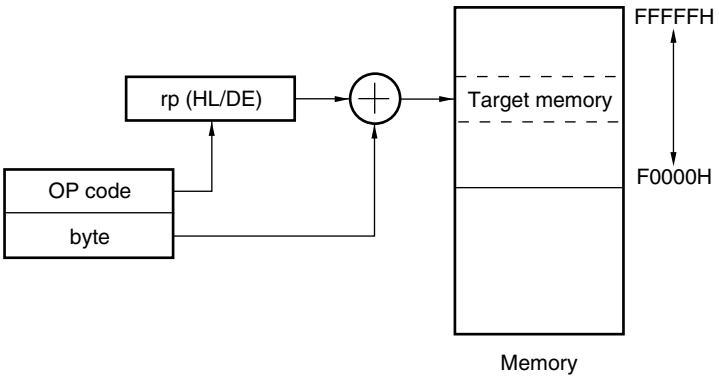


Figure 4-41. Example of word[B], word[C]

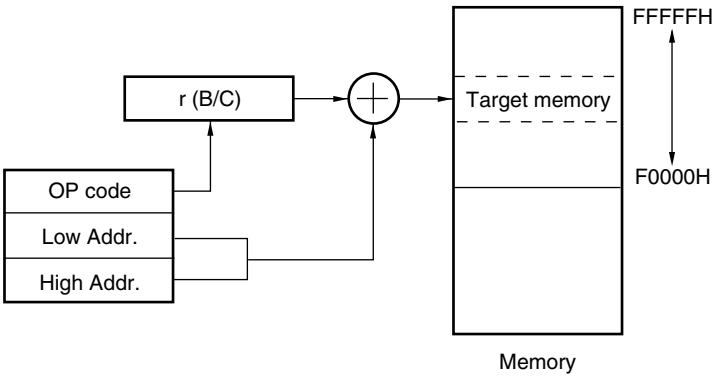


Figure 4-42. Example of word[BC]

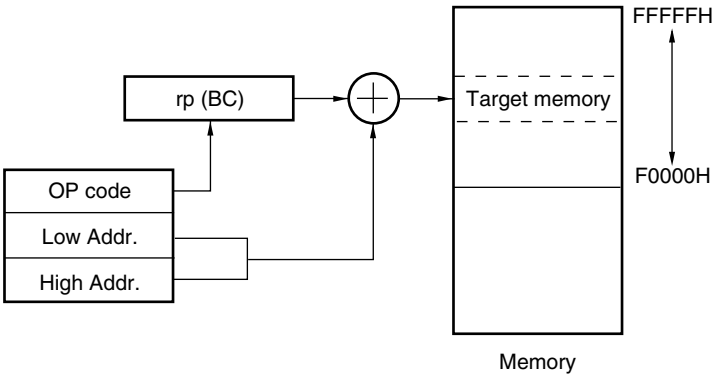


Figure 4-43. Example of ES:[HL + byte], ES:[DE + byte]

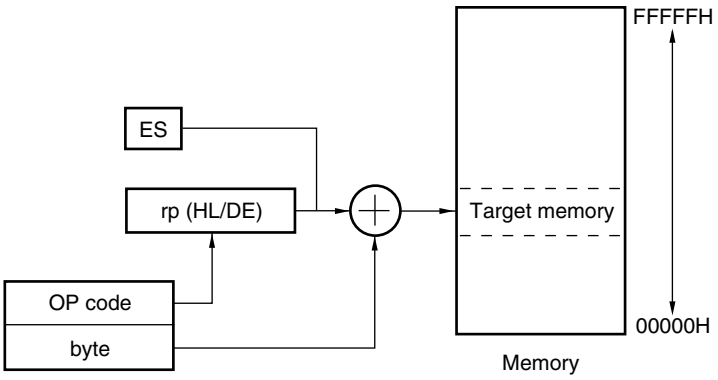


Figure 4-44. Example of ES:word[B], ES:word[C]

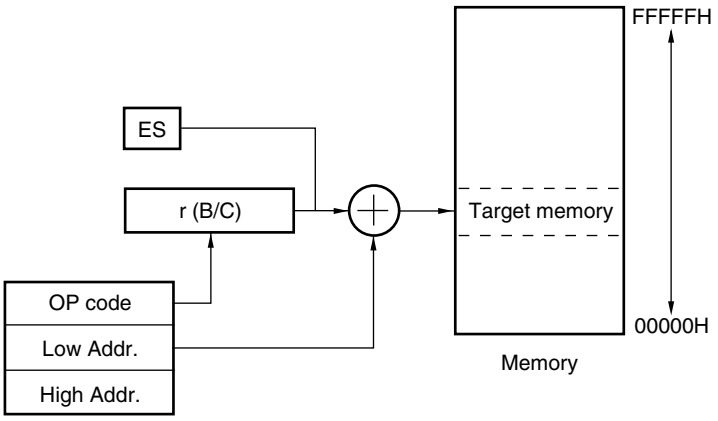
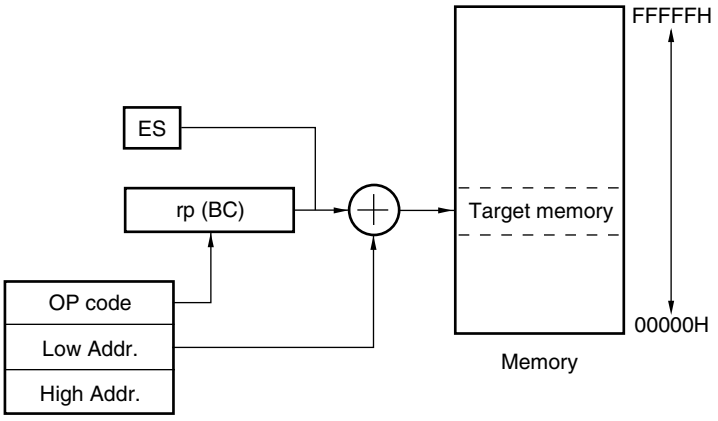


Figure 4-45. Example of ES:word[BC]



4.4.8 Based indexed addressing

[Function]

Based indexed addressing uses the contents of a register pair specified with the instruction word as the base address, and the content of the B register or C register similarly specified with the instruction word as offset address. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
–	[HL+B], [HL+C] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[HL+B], ES:[HL+C] (higher 4-bit addresses are specified by the ES register)

Figure 4-46. Example of [HL+B], [HL+C]

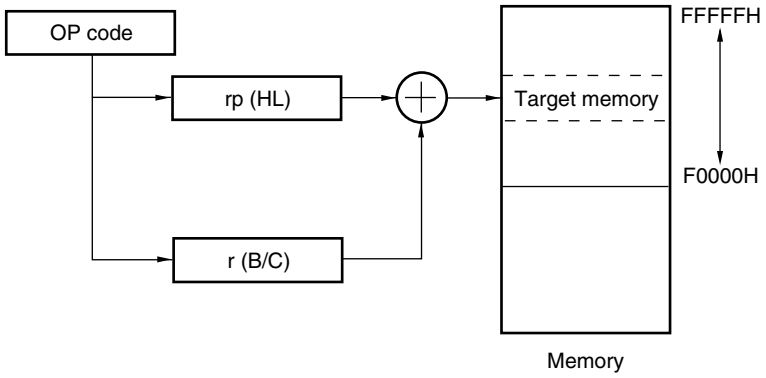
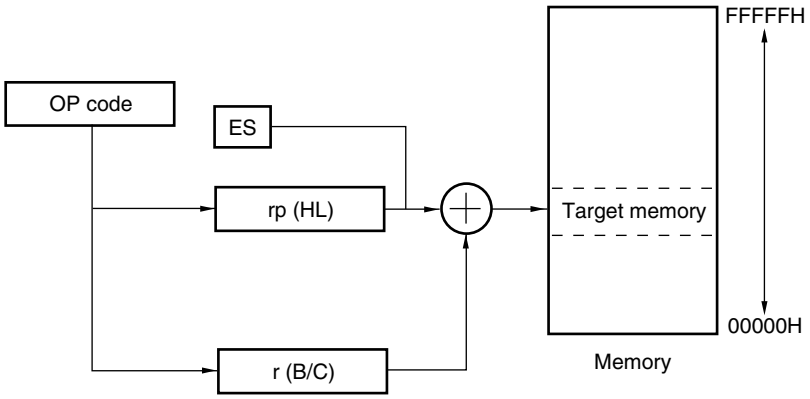


Figure 4-47. Example of ES:[HL+B], ES:[HL+C]



4.4.9 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents. This addressing is automatically employed when the PUSH, POP, subroutine call, and return instructions are executed or the register is saved/restored upon generation of an interrupt request.

Stack addressing is applied only to the internal RAM area.

[Operand format]

Identifier	Description
–	PUSH AX/BC/DE/HL POP AX/BC/DE/HL CALL/CALLT RET BRK RETB (Interrupt request generated) RETI

CHAPTER 5 PORT FUNCTIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

Caution For the functions of the port in the 78K0R/KF3-L and 78K0R/KG3-L, see CHAPTER 6 PORT FUNCTIONS (78K0R/KF3-L and 78K0R/KG3-L).

5.1 Port Functions

Pin I/O buffer power supplies depend on the product. The relationship between these power supplies and the pins is shown below.

Table 5-1. Pin I/O Buffer Power Supplies (AV_{REF}, V_{DD})

- 78K0R/KC3-L: 40-pin plastic WQFN (6x6) Note 1
  44-pin plastic LQFP (10x10)
  48-pin plastic TQFP (fine pitch) (7x7)
  48-pin plastic WQFN (7x7) Note 1
- 78K0R/KD3-L: 52-pin plastic LQFP (10x10)

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27, P150 to P152 Note 2, P80 to P83 Note 3
EV_{DD}	• Port pins other than P20 to P27, P150 to P152 Note 2, P80 to P83 Note 3 • Pins other than port pins

Notes 1. Under development
2. 40-pin and 44-pin products of the 78K0R/KC3-L do not have a P152 pin.
3. 40-pin product of the 78K0R/KC3-L does not have a P82 pin.

Table 5-2. Pin I/O Buffer Power Supplies (AV_{REF}, EV_{DD}, V_{DD})

- 78K0R/KE3-L: 64-pin plastic FBGA (5x5)
  64-pin plastic FBGA (4x4)
  64-pin plastic TQFP (fine pitch) (7x7)
  64-pin plastic LQFP (fine pitch) (10x10)
  64-pin plastic LQFP (12x12)

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27, P150 to P153, P80 to P83
EV_{DD}	• Port pins other than P20 to P27, P150 to P153, P80 to P83, and P121 to P124 • $\overline{\text{RESET}}$ pin and FLMD0 pin
V_{DD}	• P121 to P124 • Pins other than port pins (other than $\overline{\text{RESET}}$ pin and FLMD0 pin)

The 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L microcontrollers are provided with digital I/O ports, which enable variety of control operations. The functions of each port are shown in Table 5-3.

In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)**.

Table 5-3. Port Functions (1/2)

KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	Function Name	I/O	Function	After Reset	Alternate Function
–	–	–	√	√	P00	I/O	Port 0. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI00
–	–	–	√	√	P01				TO00
√	√	√	√	√	P10	I/O	Port 1. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI02/TO02
√	√	√	√	√	P11				TI03/TO03
√	√	√	√	√	P12				TI04/TO04/ RTCDIV/RTCCL Note 1
√	√	√	√	√	P13				TI05/TO05
–	–	–	–	√	P14				TI06/TO06
–	–	–	–	√	P15				TI07/TO07
–	–	–	–	√	P16				–
–	–	–	–	√	P17				–
√	√	√	√	√	P20 to P27	I/O	Port 2. I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
√	√	√	√	√	P30	I/O	Port 3. I/O port. Input of P31 and P32 can be set to TTL buffer. Output of P30 to P32 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SO10/TxD1
√	√	√	√	√	P31				SI10/RxD1/SDA10 /INTP1
√	√	√	√	√	P32				$\overline{SCK10}$/SCL10/ INTP2
–	–	–	–	√	P33				–
√	√	√	√	√	P40 Note 2	I/O	Port 4. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
√	√	√	√	√	P41				TOOL1
–	–	–	–	√	P42				–
–	–	–	–	√	P43				–
√	√	√	√	√	P50	I/O	Port 5. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI06/TO06 Note 3
√	√	√	√	√	P51				TI07/TO07 Note 3
–	√	√	√	√	P52				RTC1HZ/SLTI/ SLTO
–	–	–	–	√	P53				–

Notes 1. 40-pin product of the 78K0R/KC3-L does not have a RTCDIV/RTCCL pin.

2. If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally (see **Caution** in **2.2.5 P40 to P43 (port 4)**).

3. TI06/TO06 and TI07/TO07 are shared only in the 78K0R/KC3-L and 78K0R/KD3-L. The 78K0R/KE3-L does not have a sharing function.

Table 5-3. Port Functions (2/2)

KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	Function Name	I/O	Function	After Reset	Alternate Function
–	–	√	√	√	P60	I/O	Port 6. I/O port. Output of P60 and P61 is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
–	–	√	√	√	P61				SDA0
√	√	√	√	√	P70	I/O	Port 7. I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
√	√	√	√	√	P71				KR1/SI01/INTP5
√	√	√	√	√	P72				KR2/$\overline{\text{SCK01}}$/INTP6
√	√	√	√	√	P73				KR3/SO00/TxD0
√	√	√	√	√	P74				KR4/SI00/RxD0
√	√	√	√	√	P75				KR5/$\overline{\text{SCK00}}$
–	–	–	√	√	P76				KR6
–	–	–	√	√	P77				KR7
√	√	√	√	√	P80	I/O	Port 8. I/O port. Inputs/output can be specified in 1-bit units. Inputs of P80 to P83 can be set as comparator inputs or programmable gain amplifier inputs.	Analog input	CMP0P/INTP3/PGAI
√	√	√	√	√	P81				CMP0M
–	√	√	√	√	P82				CMP1P/INTP7
√	√	√	√	√	P83				CMP1M
√	√	√	√	√	P120	I/O	Port 12. I/O port and input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
√	√	√	√	√	P121	Input			X1
√	√	√	√	√	P122				X2/EXCLK
–	√	√	√	√	P123				XT1
–	√	√	√	√	P124				XT2
–	–	√	√	√	P140	Output	Port 14. Output port and I/O port. For only P141, input/output can be specified. For only P141, use of an on-chip pull-up resistor can be specified by a software setting.	Output port	PCLBUZ0
–	–	–	–	√	P141	I/O		Input port	PCLBUZ1
√	√	√	√	√	P150	I/O	Port 15. I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8
√	√	√	√	√	P151				ANI9
–	–	√	√	√	P152				ANI10
–	–	–	–	√	P153				ANI11

5.2 Port Configuration

Ports include the following hardware.

Table 5-4. Port Configuration

Item	Configuration
Control registers	• 78K0R/KC3-L (40-pin and 44-pin products) Port mode registers (PM1 to PM5, PM7, PM8, PM12, PM15) Port registers (P1 to P5, P7, P8, P12, P15) Pull-up resistor option registers (PU1, PU3 to PU5, PU7, PU12) Port input mode registers (PIM3, PIM7, PIM8) Port output mode registers (POM3, POM7) A/D port configuration register (ADPC) • 78K0R/KC3-L (48-pin products) Port mode registers (PM1 to PM8, PM12, PM15) Port registers (P1 to P8, P12, P14, P15) Pull-up resistor option registers (PU1, PU3 to PU5, PU7, PU12) Port input mode registers (PIM3, PIM7, PIM8) Port output mode registers (POM3, POM7) A/D port configuration register (ADPC) • 78K0R/KD3-L Port mode registers (PM0 to PM8, PM12, PM15) Port registers (P0 to P8, P12, P14, P15) Pull-up resistor option registers (PU0, PU1, PU3 to PU5, PU7, PU12) Port input mode registers (PIM3, PIM7, PIM8) Port output mode registers (POM3, POM7) A/D port configuration register (ADPC) • 78K0R/KE3-L Port mode registers (PM0 to PM8, PM12, PM14, PM15) Port registers (P0 to P8, P12, P14, P15) Pull-up resistor option registers (PU0, PU1, PU3 to PU5, PU7, PU12, PU14) Port input mode registers (PIM3, PIM7, PIM8) Port output mode registers (POM3, POM7) A/D port configuration register (ADPC)
Port	• 78K0R/KC3-L (40-pin products) Total: 33 (CMOS I/O: 31, CMOS input: 2) • 78K0R/KC3-L (44-pin products) Total: 37 (CMOS I/O: 33, CMOS input: 4) • 78K0R/KC3-L (48-pin products) Total: 41 (CMOS I/O: 34, CMOS input: 4, CMOS output: 1, N-ch open drain I/O: 2) • 78K0R/KD3-L Total: 45 (CMOS I/O: 38, CMOS input: 4, CMOS output: 1, N-ch open drain I/O: 2) • 78K0R/KE3-L Total: 55 (CMOS I/O: 48, CMOS input: 4, CMOS output: 1, N-ch open drain I/O: 2)
Pull-up resistor	• 78K0R/KC3-L (40-pin products) Total: 18 • 78K0R/KC3-L (44-pin products) Total: 19 • 78K0R/KC3-L (48-pin products) Total: 19 • 78K0R/KD3-L Total: 23 • 78K0R/KE3-L Total: 32

5.2.1 Port 0

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P00/TI00	–		–	√	√
P11/TO00	–		–	√	√

Port 0 is an I/O port with an output latch. Port 0 can be set to the input mode or output mode in 1-bit units using port mode register 0 (PM0). When the P00 and P01 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 0 (PU0).

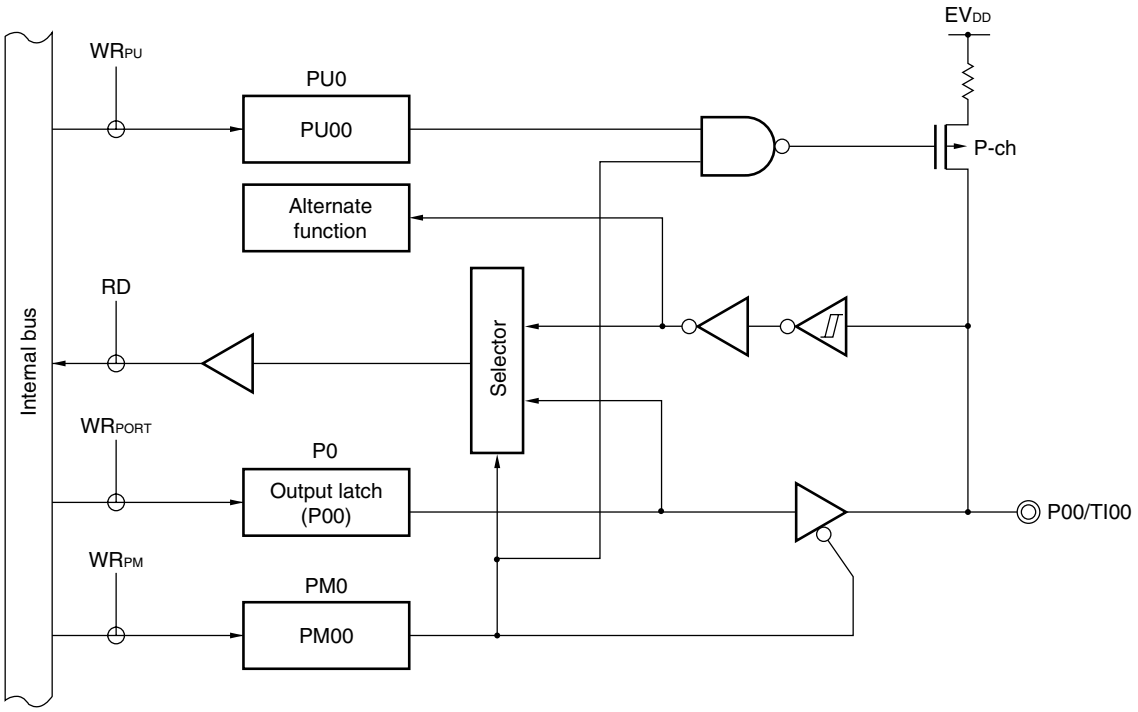
This port can also be used for timer I/O.

Reset signal generation sets port 0 to input mode.

Figures 5-1 and 5-2 show block diagrams of port 0.

Caution To use P01/TO00 as a general-purpose port, set bit 0 (TO00) of timer output register 0 (TO0) and bit 0 (TOE00) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

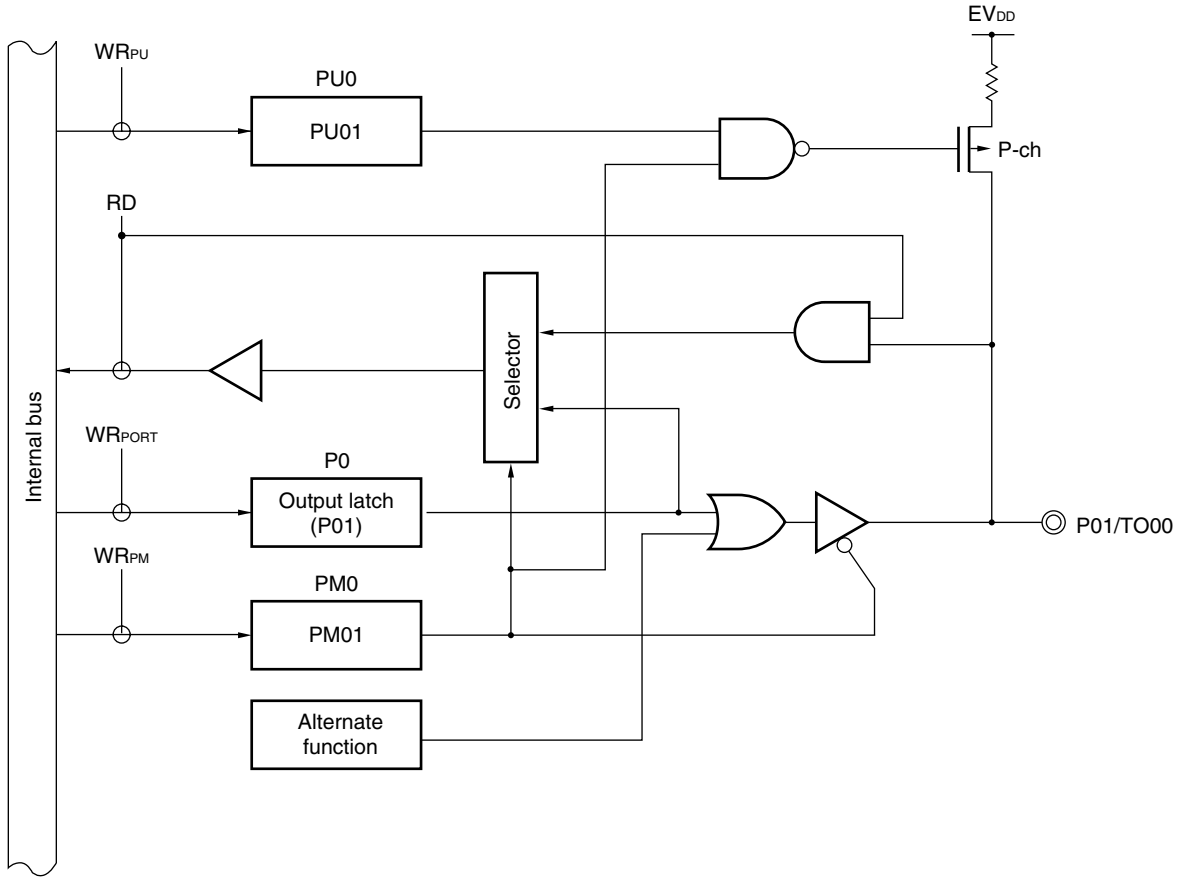
Figure 5-1. Block Diagram of P00



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WRxx: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-2. Block Diagram of P01



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WRxx: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

5.2.2 Port 1

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P10/TI02/TO02	√		√	√	√
P11/TO00/TI03/TO03	√		√	√	√
P12/TI04/TO04/RTCDIV/RTCCL	P12/TI04/TO04[Note 1]	√	√	√	√
P13/TI05/TO05	√		√	√	√
P14/TI06/TO06	–[Note 2]		–[Note 2]	–[Note 2]	√
P15/TI07/TO07	–[Note 2]		–[Note 2]	–[Note 2]	√
P16	–		–	–	√
P17	–		–	–	√

Notes 1. 40-pin product of the 78K0R/KC3-L does not have a RTCDIV/RTCCL pin.

2. TI06/TO06 and TI07/TO07 are shared with P50 and P51, respectively, in products other than the 78K0R/KE3-L.

Remark √: Mounted

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P17 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

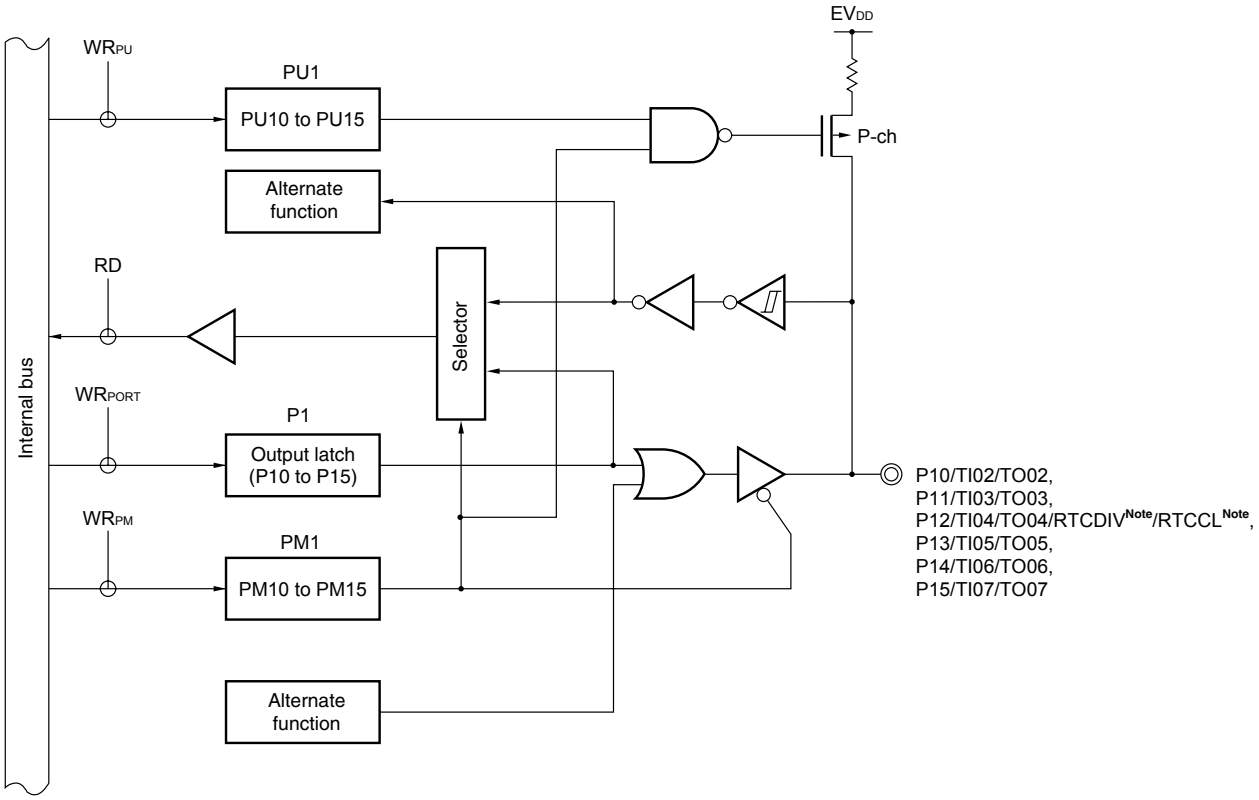
This port can also be used for timer I/O and real-time counter clock output.

Reset signal generation sets port 1 to input mode.

Figures 5-3 and 5-4 show block diagrams of port 1.

Caution To use P10/TI02/TO02, P11/TI03/TO03, P12/TI04/TO04/RTCDIV/RTCCL, P13/TI05/TO05, P14/TI06/TO06, or P15/TI07/TO07 as a general-purpose port, set bits 2 to 7 (TO02 to TO07) of timer output register 0 (TO0) and bits 2 to 7 (TOE02 to TOE07) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

Figure 5-3. Block Diagram of P10 to P15

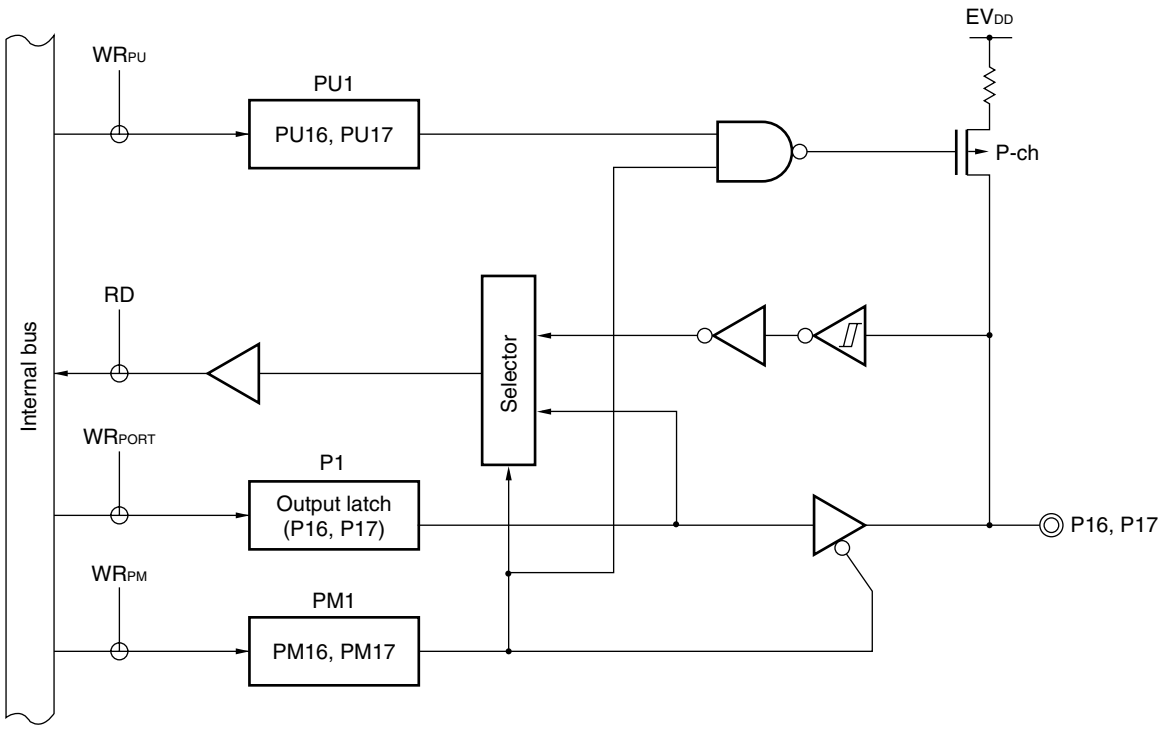


Note 40-pin product of the 78K0R/KC3-L does not have a RTCDIV/RTCCL pin.

P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Remark With products not provided with an EVDD or EVSS pin, replace EVDD with VDD, or replace EVSS with VSS.

Figure 5-4. Block Diagram of P16 and P17



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

5.2.3 Port 2

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P20/ANI0	√		√	√	√
P21/ANI1	√		√	√	√
P22/ANI2	√		√	√	√
P23/ANI3	√		√	√	√
P24/ANI4	√		√	√	√
P25/ANI5	√		√	√	√
P26/ANI6	√		√	√	√
P27/ANI7	√		√	√	√

Remark √: Mounted

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2).

This port can also be used for A/D converter analog input.

To use P20/ANI0 to P27/ANI7 as digital input pins, set them in the digital I/O mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM2 register. Use these pins starting from the lower bit.

To use P20/ANI0 to P27/ANI7 as digital output pins, set them in the digital I/O mode by using the ADPC register and in the output mode by using the PM2 register.

To use P20/ANI0 to P27/ANI7 as analog input pins, set them in the analog input mode by using the ADPC register and in the input mode by using the PM2 register. Use these pins starting from the upper bit.

Table 5-5. Setting Functions of P20/ANI0 to P27/ANI7 Pins

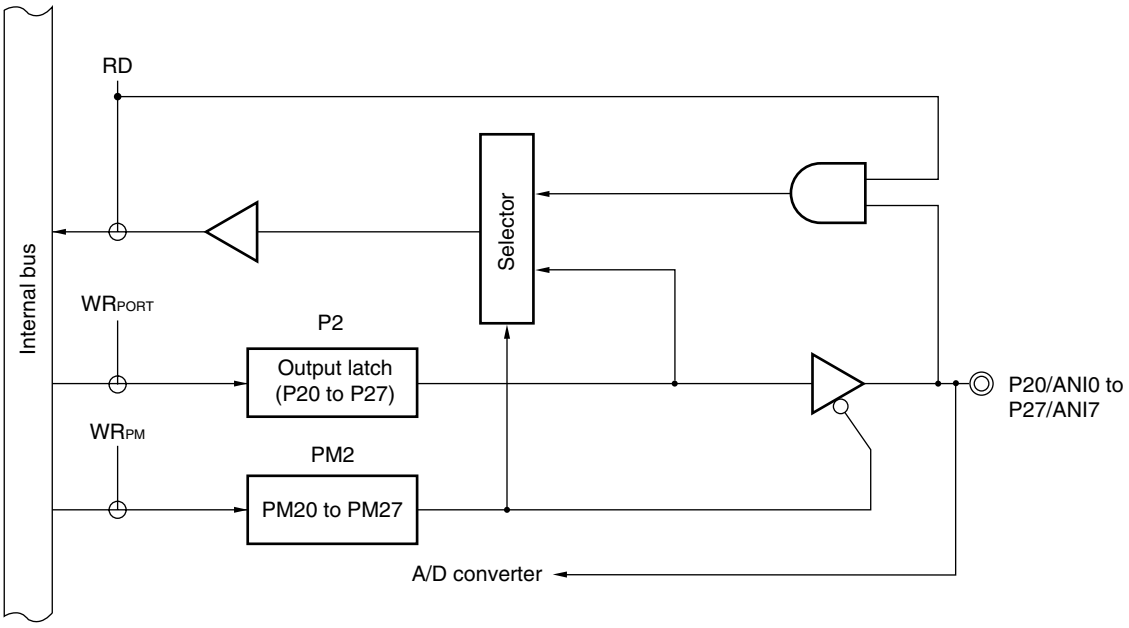
ADPC Register	PM2 Register	ADS Register	P20/ANI0 to P27/ANI7 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

All P20/ANI0 to P27/ANI7 are set in the digital input mode when the reset signal is generated.

Figure 5-5 shows a block diagram of port 2.

Caution Make the AV_{REF} pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

Figure 5-5. Block Diagram of P20 to P27



P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

5.2.4 Port 3

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P30/SO10/TxD1	√		√	√	√
P31/SI10/RxD1/ SDA10/INTP1	√		√	√	√
P32/$\overline{\text{SCK10}}$/ SCL10/INTP2	√		√	√	√
P33	–		–	–	√

Remark √: Mounted

Port 3 is an I/O port with an output latch. Port 3 can be set to the input mode or output mode in 1-bit units using port mode register 3 (PM3). When the P30 to P33 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 3 (PU3).

Input to the P31 and P32 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 3 (PIM3).

Output from the P30 to P32 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 3 (POM3).

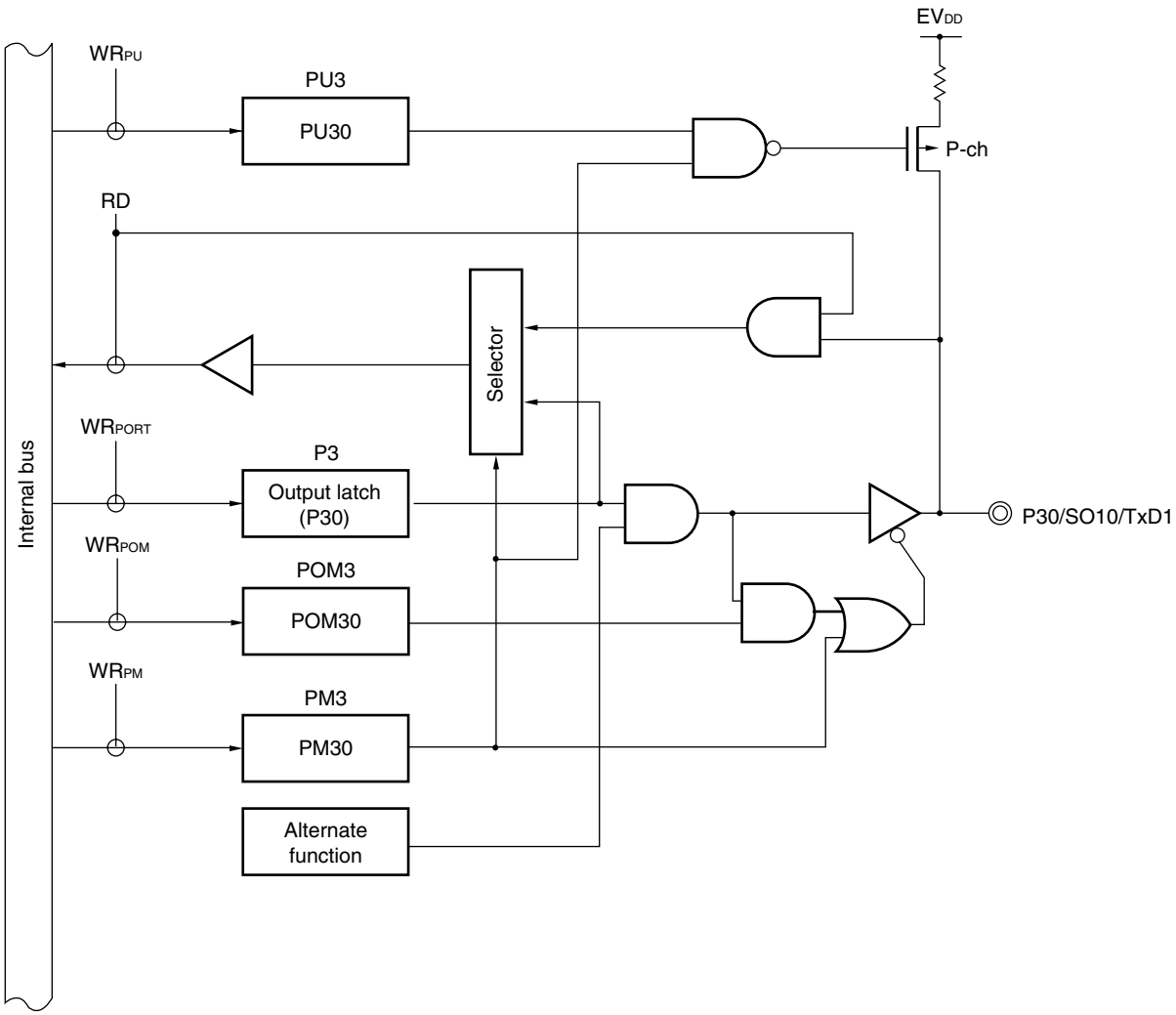
This port can also be used for serial interface data I/O, clock I/O, and external interrupt request input.

Reset signal generation sets port 3 to input mode.

Figures 5-6 to 5-8 show block diagrams of port 3.

Caution To use P30/SO10/TxD1, P31/SI10/RxD1/SDA10/INTP1, P32/$\overline{\text{SCK10}}$/SCL10/INTP2 as a general-purpose port, note the serial array unit setting. For details, refer to Table 14-7 Relationship Between Register Settings and Pins (Channel 2: CSI10, UART1 Transmission, IIC10) and Table 14-8 Relationship Between Register Settings and Pins (Channel 3: UART1 Reception).

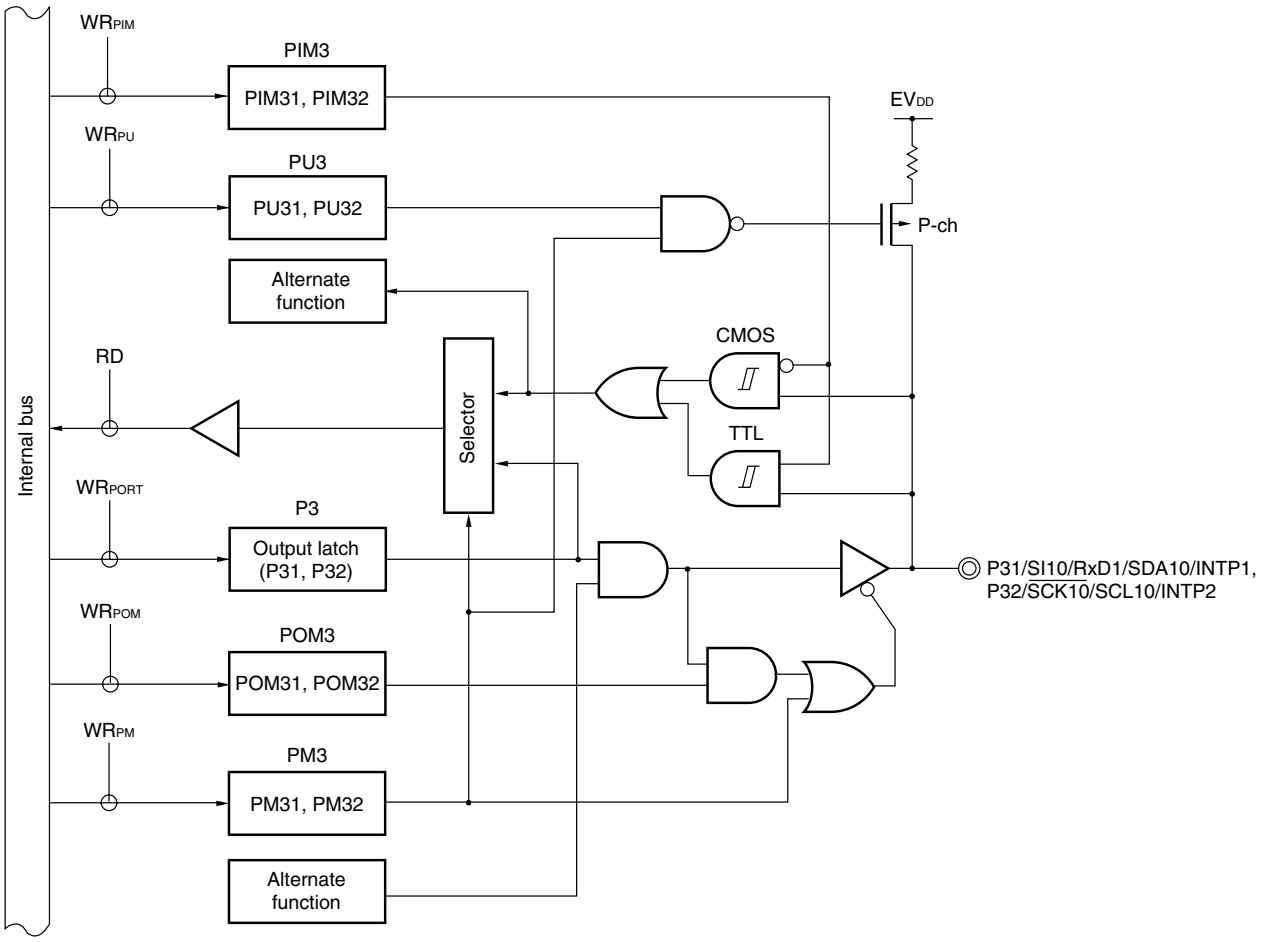
Figure 5-6. Block Diagram of P30



P3: Port register 3
PU3: Pull-up resistor option register 3
POM3: Port output mode register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

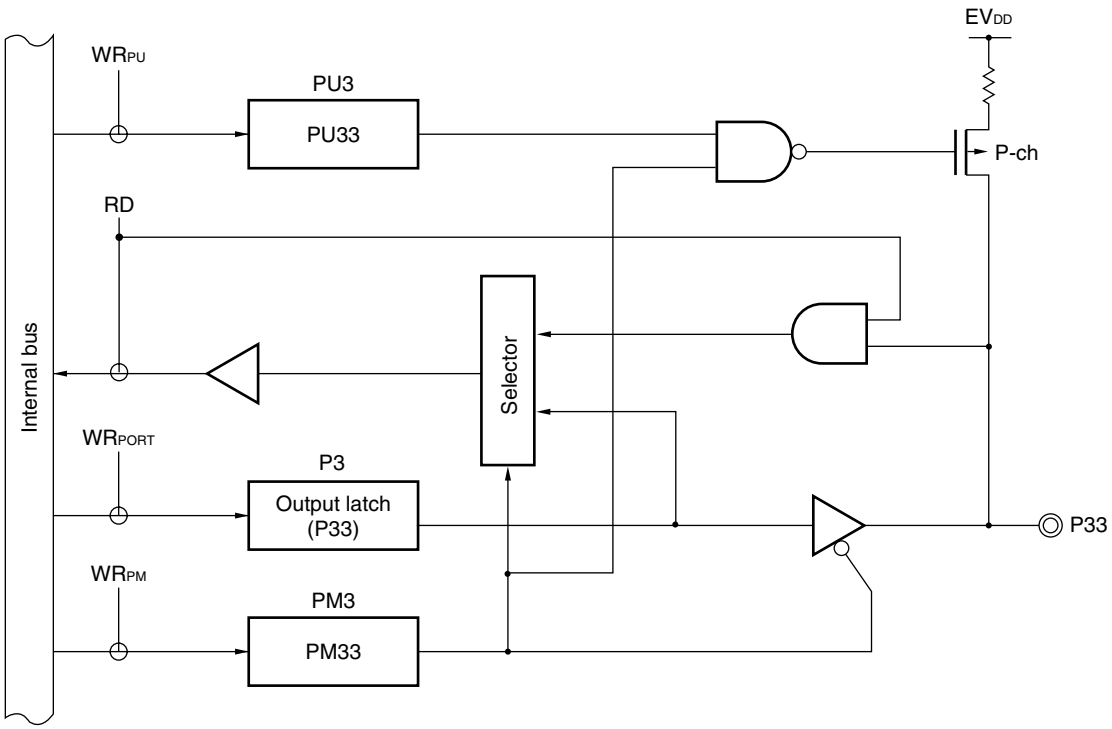
Figure 5-7. Block Diagram of P31 and P32



P3: Port register 3
PU3: Pull-up resistor option register 3
PIM3: Port input mode register 3
POM3: Port output mode register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-8. Block Diagram of P33



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

5.2.5 Port 4

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P40/TOOL0	√		√	√	√
P41/TOOL1	√		√	√	√
P42	–		–	–	√
P43	–		–	–	√

Remark √: Mounted

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P43 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 4 (PU4)[Note].

This port can also be used for flash memory programmer/debugger data I/O and clock output.

Reset signal generation sets port 4 to input mode.

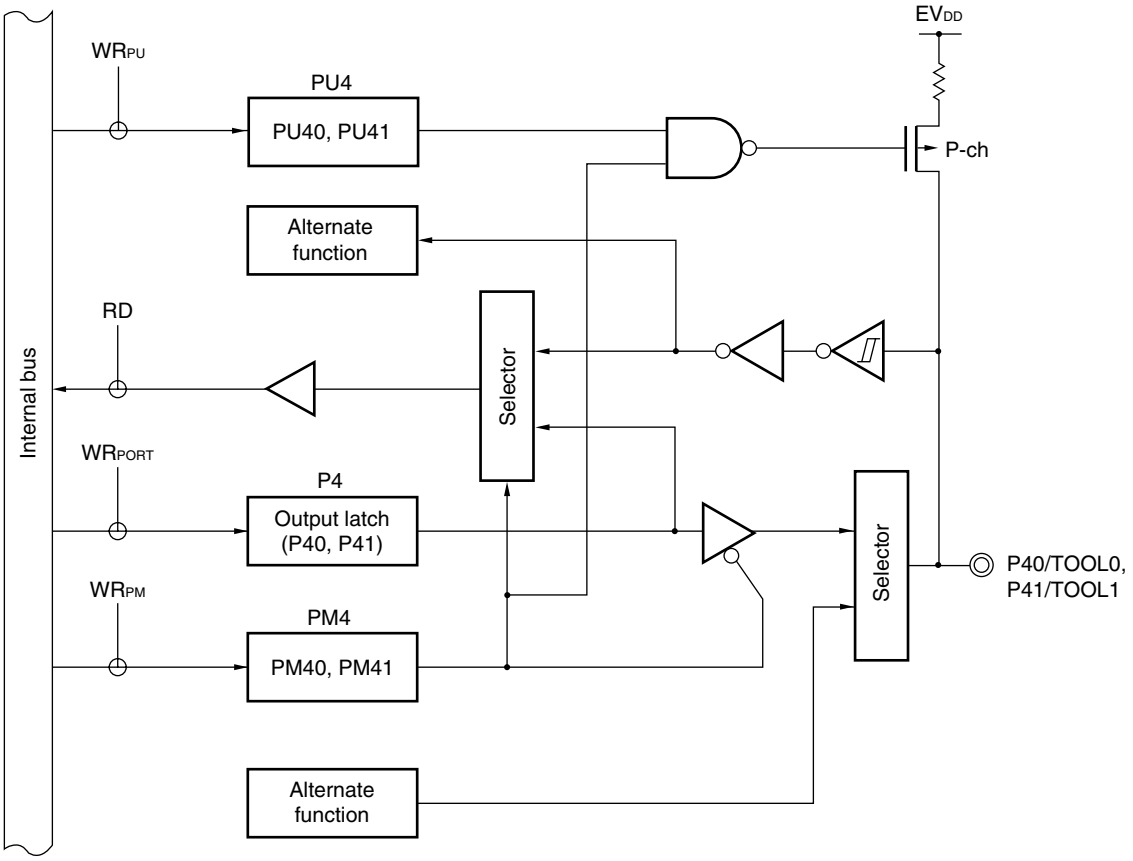
Figures 5-9 and 5-10 show block diagrams of port 4.

Note When a tool is connected, the P40 and P41 pins cannot be connected to a pull-up resistor.

Caution When a tool is connected, the P40 pin cannot be used as a port pin.
When the on-chip debug function is used, the P41 pin can be used as follows by the mode setting on the debugger.

1-line mode: can be used as a port (P41).
2-line mode: used as a TOOL1 pin and cannot be used as a port (P41).

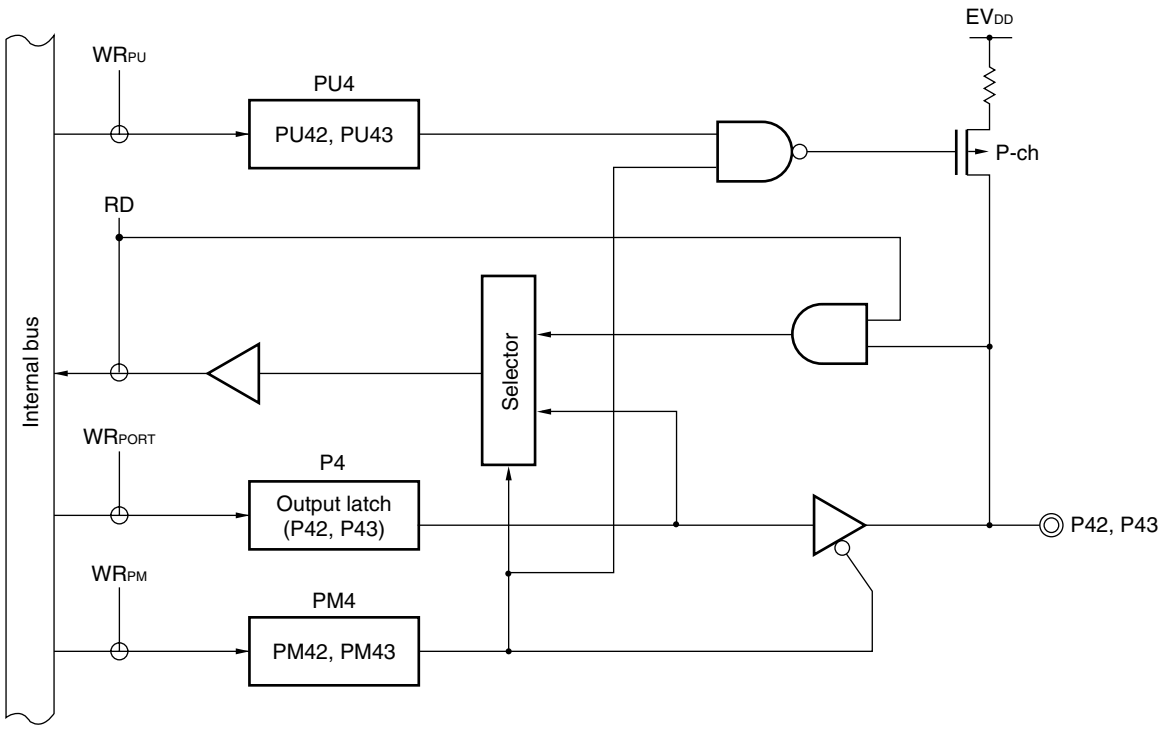
Figure 5-9. Block Diagram of P40 and P41



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-10. Block Diagram of P42 and P43



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

5.2.6 Port 5

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P50/TI06/TO06	√		√	√	P50[Note]
P51/TI07/TO07	√		√	√	P51[Note]
P52/RTC1HZ/ SLTI/SLTO	–	√	√	√	√
P53	–		–	–	√

Note TI06/TO06 and TI07/TO07 are shared only in the 78K0R/KC3-L and 78K0R/KD3-L. The 78K0R/KE3-L does not have a sharing function.

Remark √: Mounted

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units using port mode register 5 (PM5). When the P50 to P53 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

This port can also be used for real-time counter correction clock output and timer I/O.

Reset signal generation sets port 5 to input mode.

Figures 5-11 to 5-13 show block diagrams of port 5.

Caution 1. To use P50/TI06/TO06 and P51/TI07/TO07 as a general-purpose port, set bits 6 and 7 (TO06 and TO07) of timer output register 0 (TO0) and bits 6 and 7 (TOE06 and TOE07) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

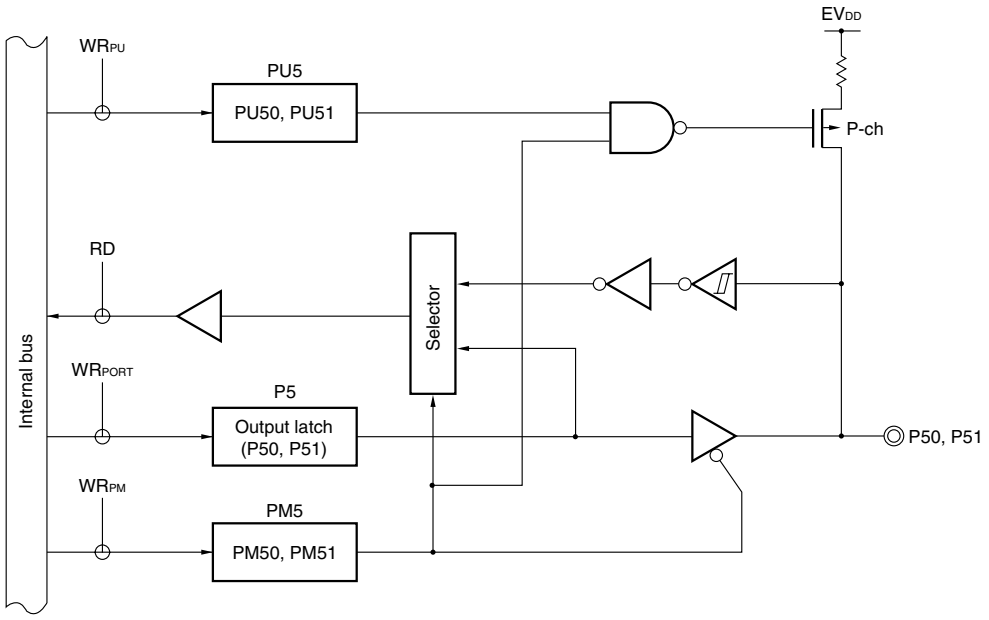
2. To use P52/RTC1HZ/SLTI/SLTO as a general-purpose port, check which timer I/O pin of which channel n is selected in the input switching control register (ISC) setting. Also, set bit n (TO0n) of timer output register 0 (TO0) and bit n (TOE0n) of timer output enable register 0 (TOE0) to "0", which is the same setting as in the initial state of each.

3. In the case of the 78K0R/KC3-L (40-pin), be sure to clear bit2 of the PM5 register to "0" after the reset release.

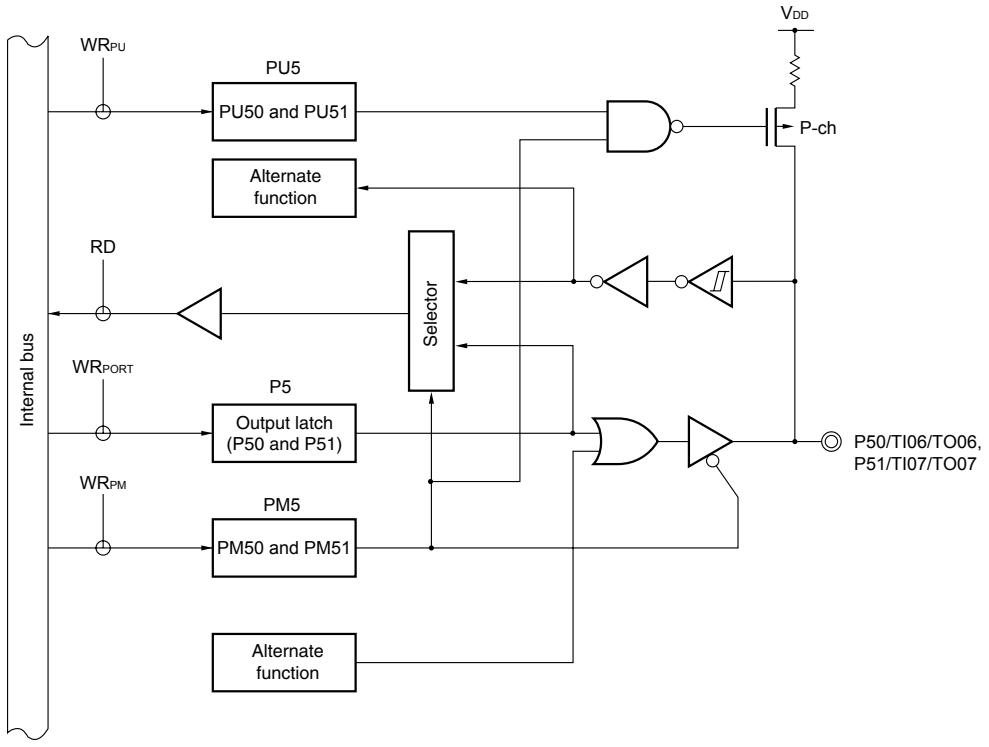
Remark n = 0, 1

Figure 5-11. Block Diagram of P50 and P51

(1) 78K0R/KE3-L

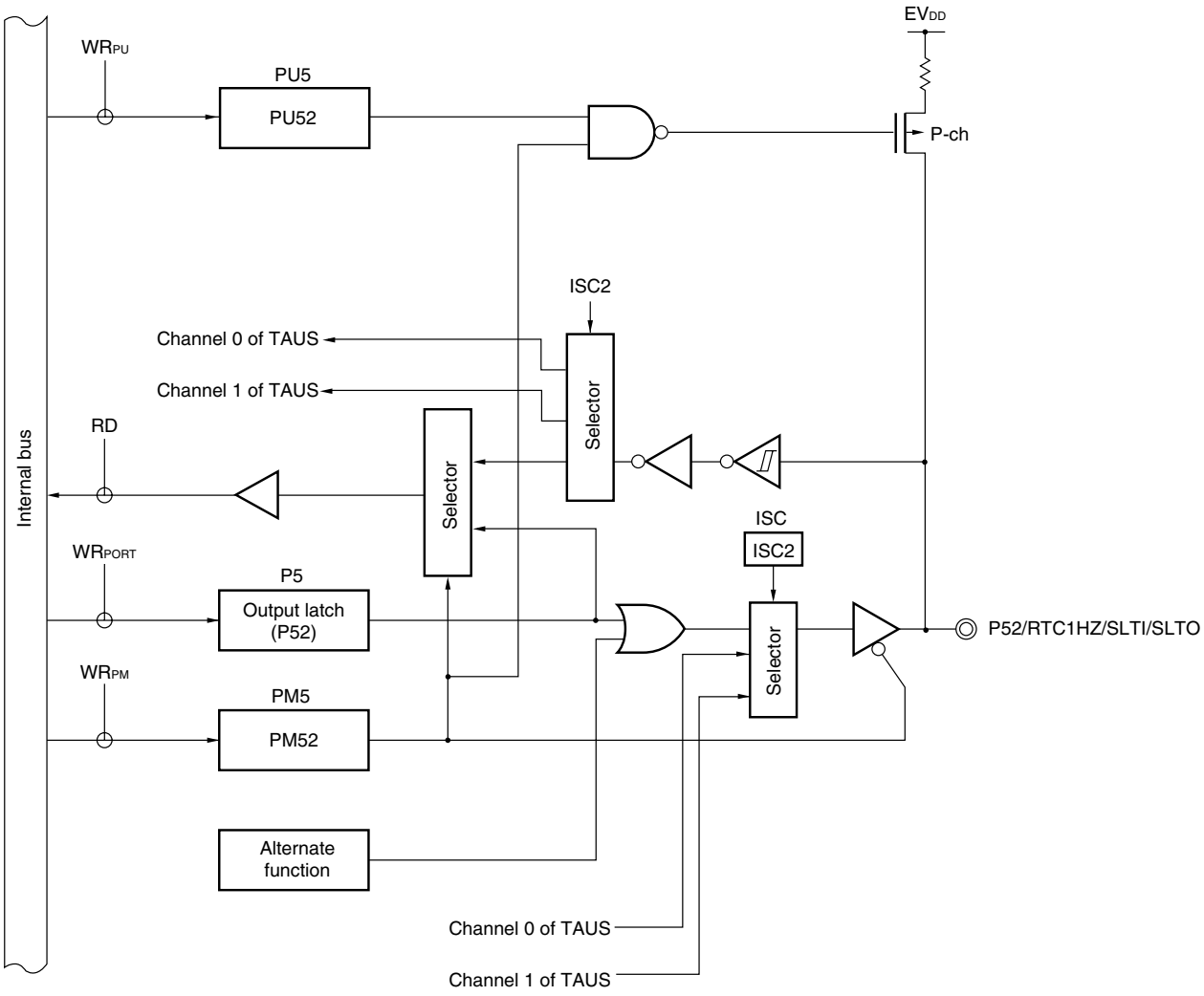


(2) Products other than 78K0R/KE3-L



P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

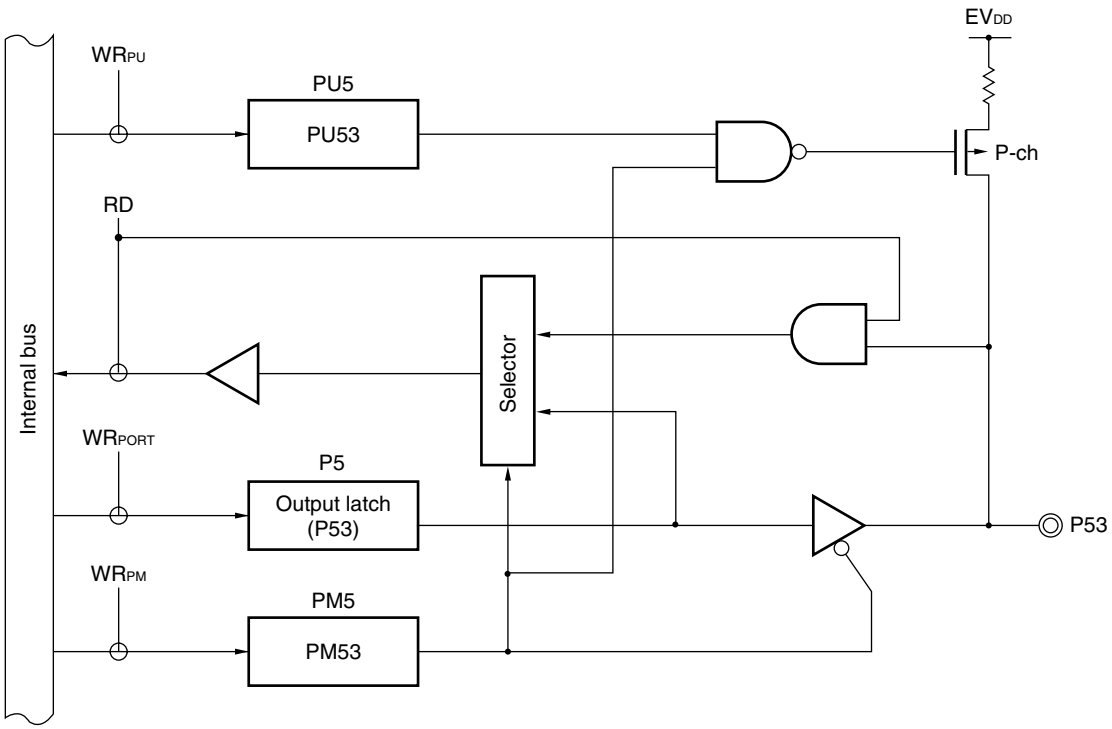
Figure 5-12. Block Diagram of P52



P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal
ISC: Input switch control register

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-13. Block Diagram of P53



P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

5.2.7 Port 6

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P60/SCL0	–		√	√	√
P61/SDA0	–		√	√	√

Remark √: Mounted

Port 6 is an I/O port with an output latch. Port 6 can be set to the input mode or output mode in 1-bit units using port mode register 6 (PM6).

The output of the P60 and P61 pins is N-ch open-drain output (6 V tolerance).

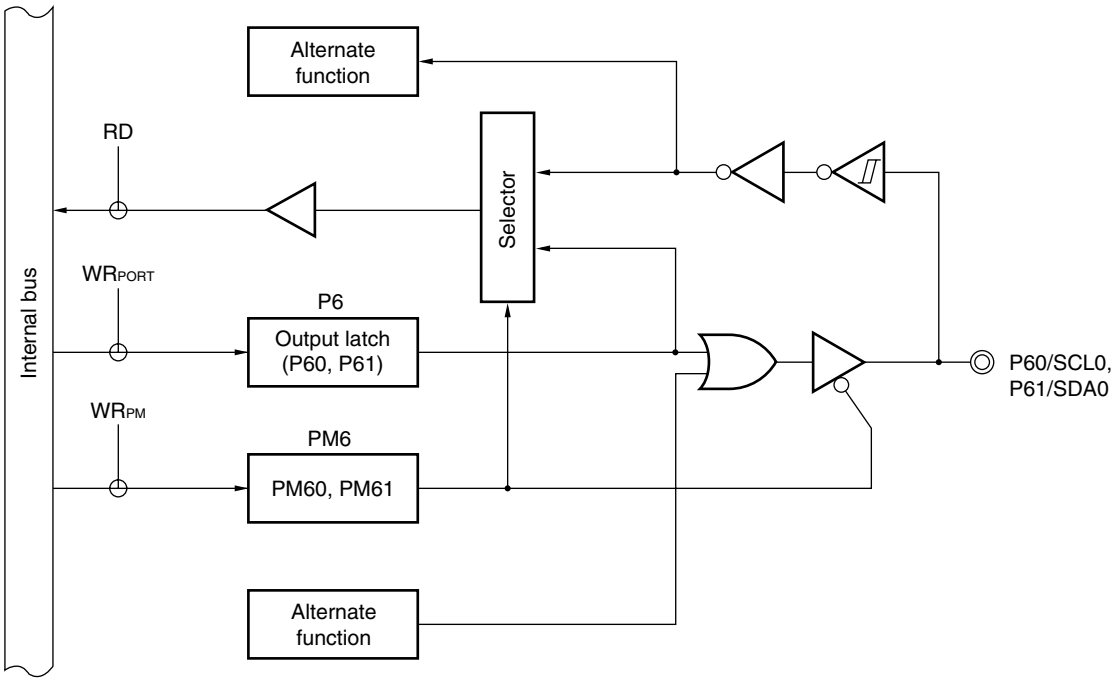
This port can also be used for serial interface data I/O and clock I/O.

Reset signal generation sets port 6 to input mode.

Figure 5-14 shows block diagram of port 6.

Caution When using P60/SCL0 or P61/SDA0 as a general-purpose port, stop the operation of serial interface IICA.

Figure 5-14. Block Diagram of P60 and P61



P6: Port register 6

PM6: Port mode register 6

RD: Read signal

WR××: Write signal

5.2.8 Port 7

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P70/KR0/SO01/INTP4	√		√	√	√
P71/KR1/SI01/INTP5	√		√	√	√
P72/KR2/$\overline{\text{SCK01}}$/INTP6	√		√	√	√
P73/KR3/SO00/TxD0	√		√	√	√
P74/KR4/SI00/RxD0	√		√	√	√
P75/KR5/$\overline{\text{SCK00}}$	√		√	√	√
P76/KR6	–		–	√	√
P77/KR7	–		–	√	√

Remark √: Mounted

Port 7 is an I/O port with an output latch. Port 7 can be set to the input mode or output mode in 1-bit units using port mode register 7 (PM7). When the P70 to P77 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 7 (PU7).

Input to the P71, P72, P74, and P75 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 7 (PIM7).

Output from the P70, P72, P73, and P75 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 7 (POM7).

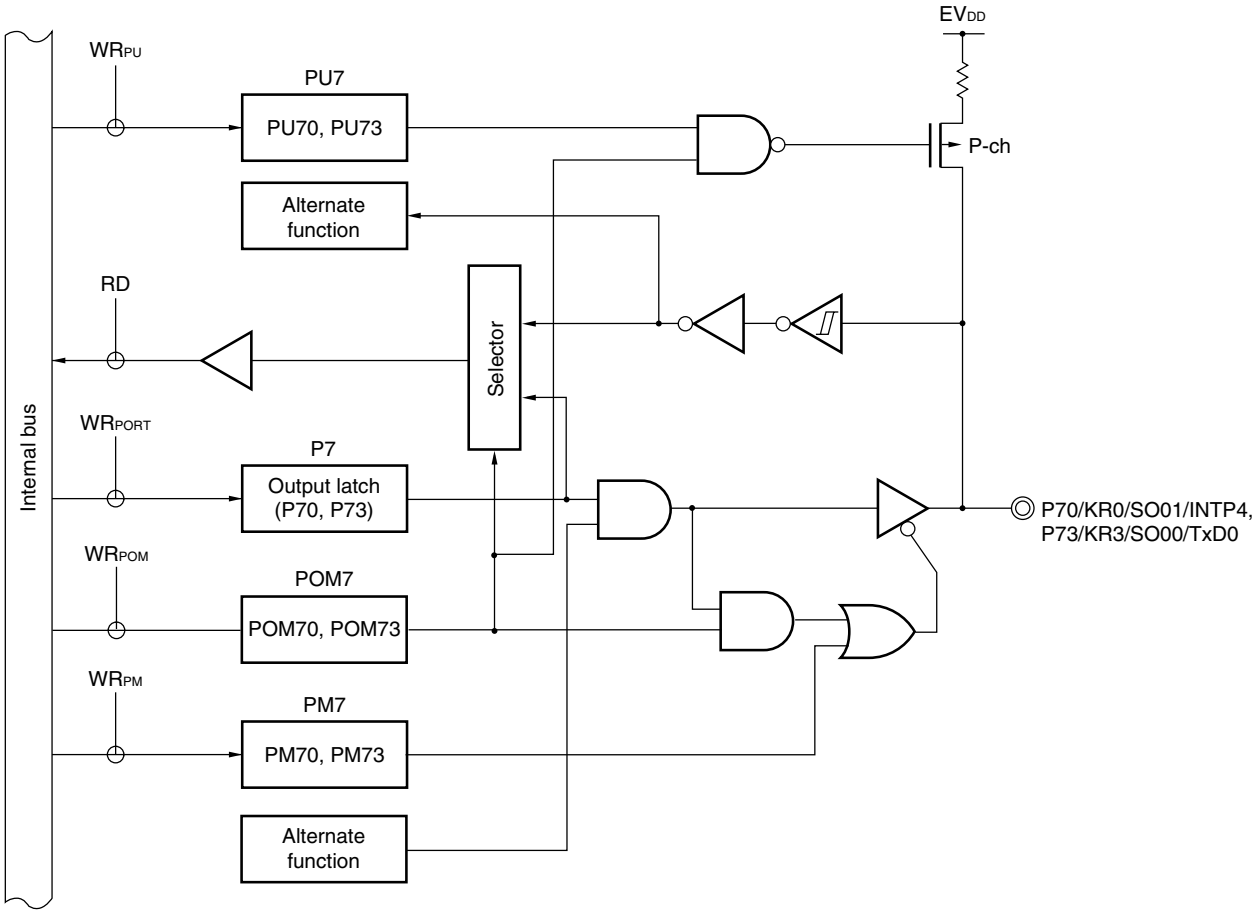
This port can also be used for key return input, serial interface data I/O, clock I/O, and external interrupt request input.

Reset signal generation sets port 7 to input mode.

Figures 5-15 to 5-18 show block diagrams of port 7.

Caution To use P70/KR0/SO01/INTP4, P71/KR1/SI01/INTP5, P72/KR2/$\overline{\text{SCK01}}$/INTP6, P73/KR3/SO00/TxD0, P74/KR4/SI00/RxD0, P75/KR5/$\overline{\text{SCK00}}$ as a general-purpose port, note the serial array unit setting. For details, refer to Table 14-5 Relationship Between Register Settings and Pins (Channel 0: CSI00, UART0 Transmission) and Table 14-6 Relationship Between Register Settings and Pins (Channel 1: CSI01, UART0 Reception).

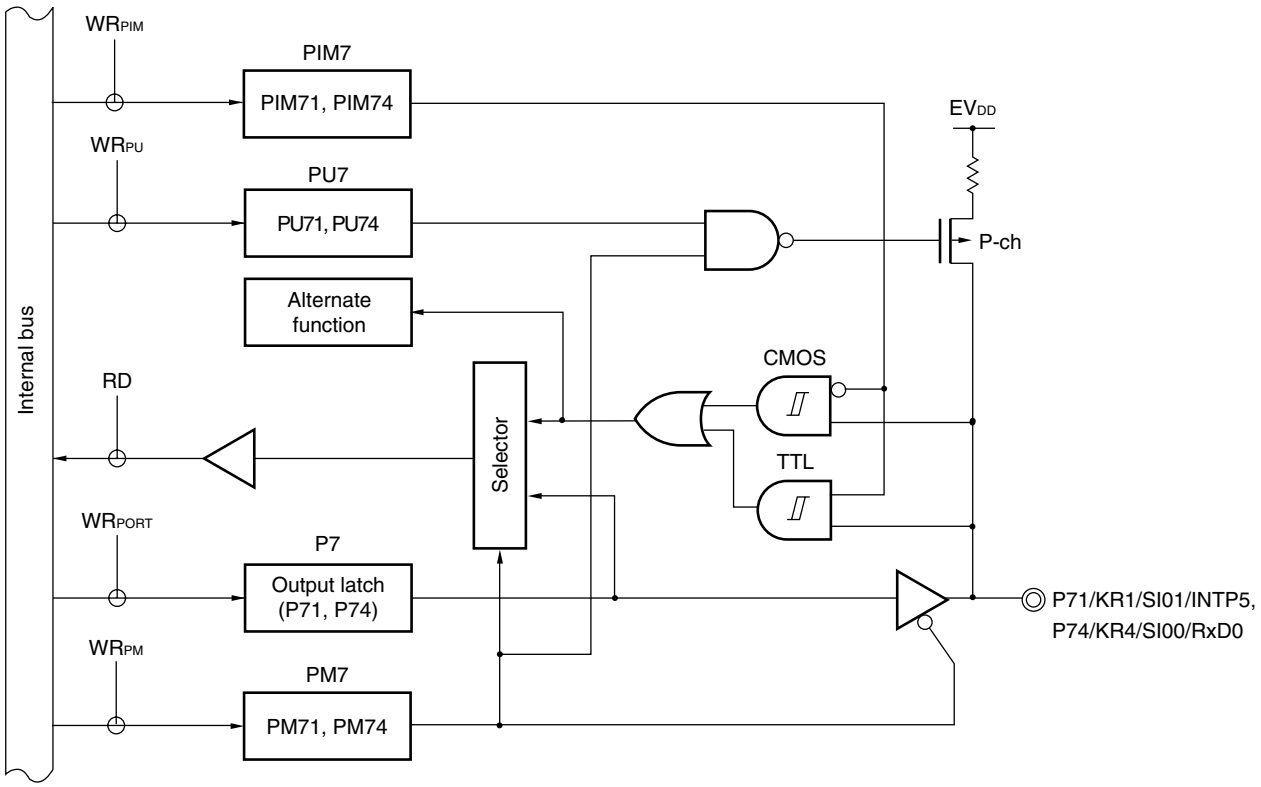
Figure 5-15. Block Diagram of P70 and P73



P7: Port register 7
PU7: Pull-up resistor option register 7
POM7: Port output mode register 7
PM7: Port mode register 7
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

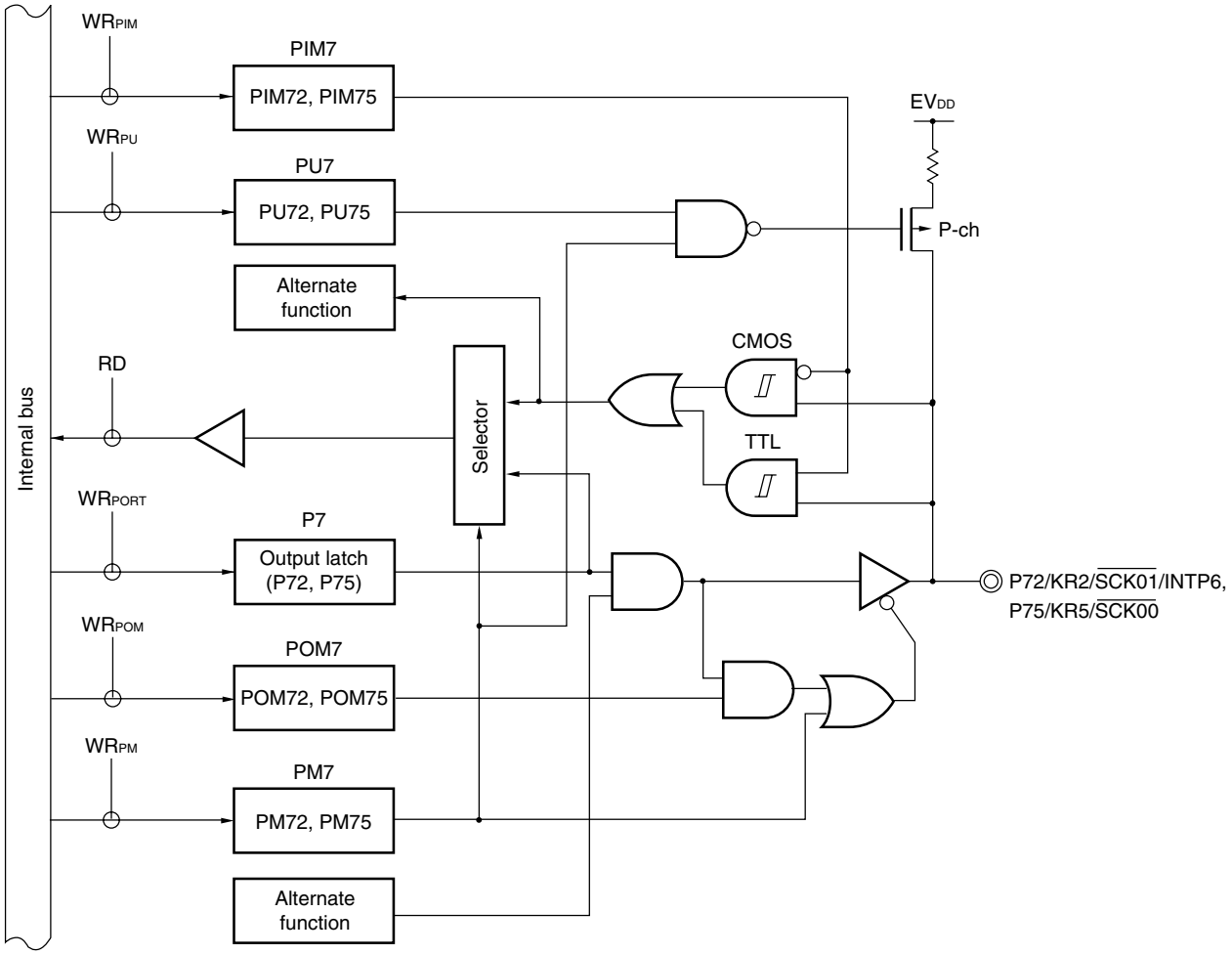
Figure 5-16. Block Diagram of P71 and P74



P7: Port register 7
PU7: Pull-up resistor option register 7
PM7: Port mode register 7
PIM7: Port input mode register 7
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

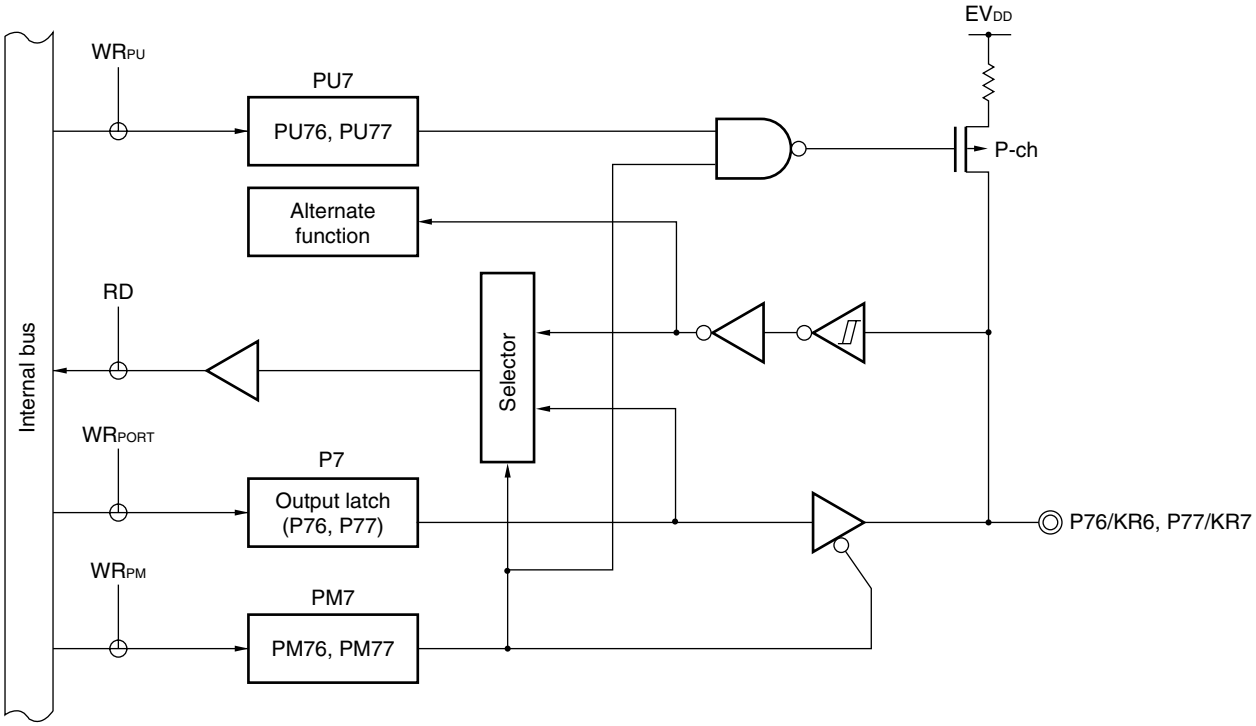
Figure 5-17. Block Diagram of P72 and P75



P7: Port register 7
PU7: Pull-up resistor option register 7
PM7: Port mode register 7
PIM7: Port input mode register 7
POM7: Port output mode register 7
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-18. Block Diagram of P76 and P77



P7: Port register 7
PU7: Pull-up resistor option register 7
PM7: Port mode register 7
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

5.2.9 Port 8

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P80/CMP0P/ INTP3/PGAI	√		√	√	√
P81/CMP0M	√		√	√	√
P82/CMP1P/ INTP7	–	√	√	√	√
P83/CMP1M	√		√	√	√

Remark √: Mounted

Port 8 is an I/O port with an output latch. Port 8 can be set to the input mode or output mode in 1-bit units using port mode register 8 (PM8).

Inputs to the P80 to P83 pins must be enabled or disabled in 1-bit units using port input mode register 8 (PIM8).

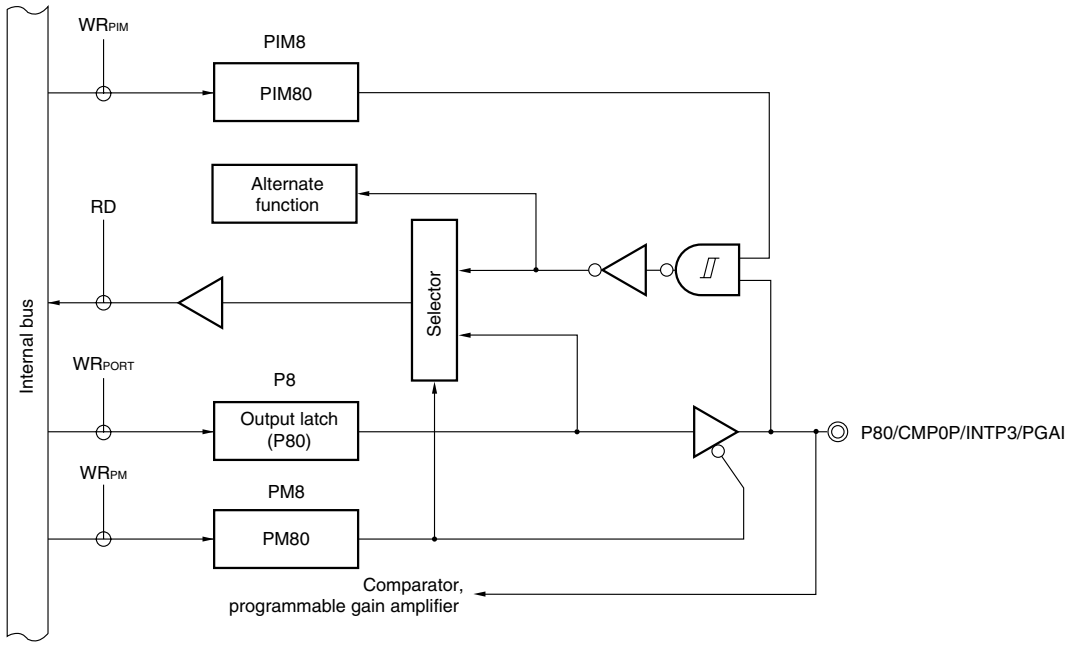
This port can also be used for an input voltage on the (+) sides of comparators 0 and 1, an input voltage on the (–) sides of comparators 0 and 1, an external interrupt request input, and a programmable gain amplifier input.

Reset signal generation sets port 8 to analog input mode.

Figures 5-19 to 5-21 show block diagrams of port 8.

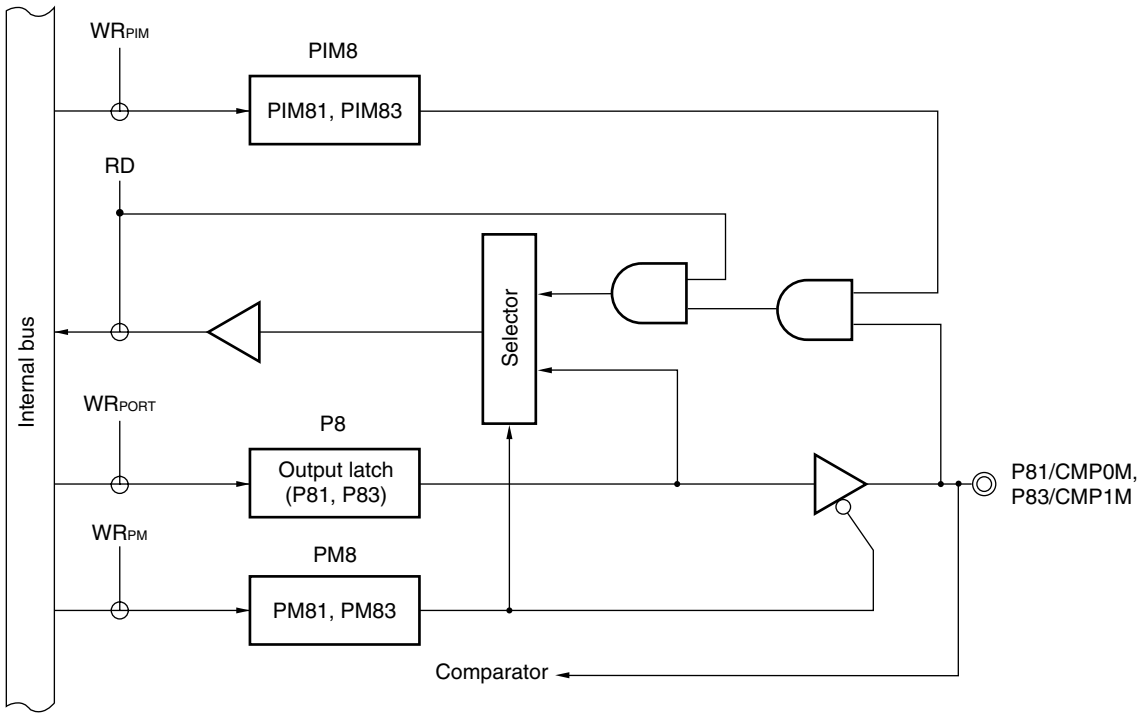
Caution In the case of the 78K0R/KC3-L (40-pin), be sure to clear bit2 of the PM8 register to "0" after the reset release.

Figure 5-19. Block Diagram of P80



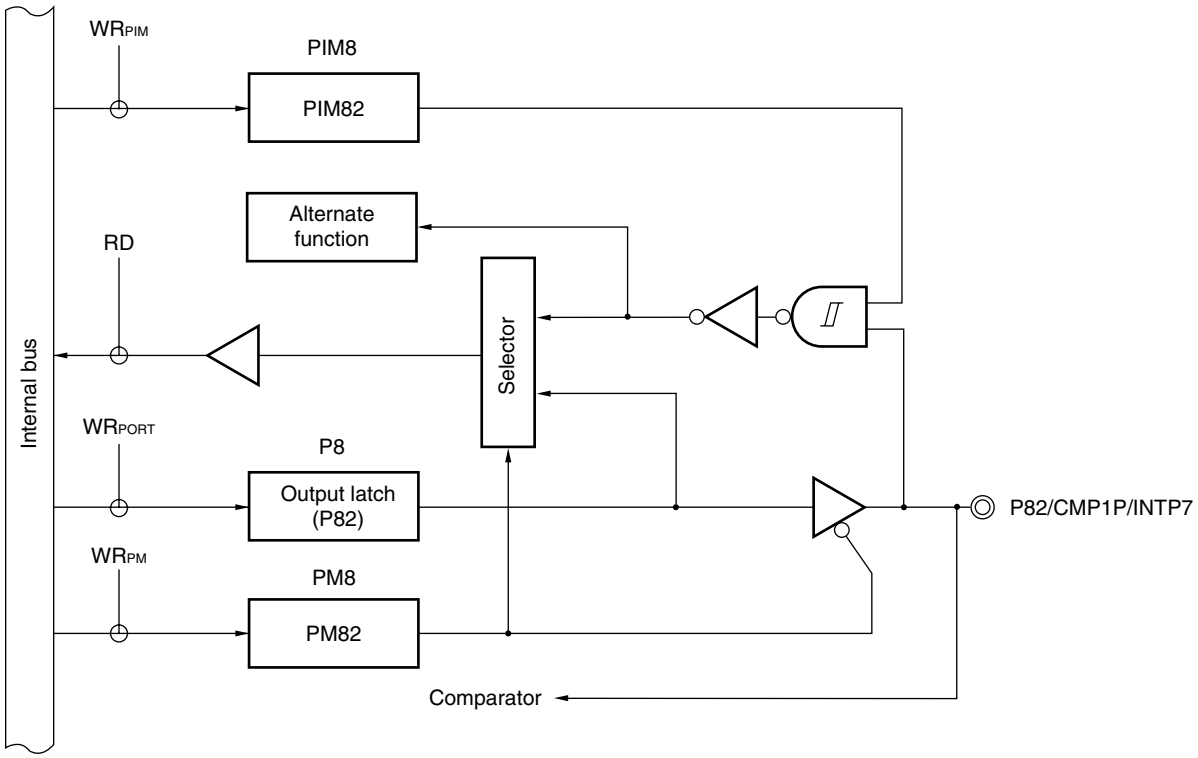
P8: Port register 8
PM8: Port mode register 8
PIM8: Port input mode register 8
RD: Read signal
WR××: Write signal

Figure 5-20. Block Diagram of P81 and P83



P8: Port register 8
PM8: Port mode register 8
PIM8: Port input mode register 8
RD: Read signal
WR××: Write signal

Figure 5-21. Block Diagram of P82



P8: Port register 8
PM8: Port mode register 8
PIM8: Port input mode register 8
RD: Read signal
WR××: Write signal

5.2.10 Port 12

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P120/INTP0/ EXLVI	√		√	√	√
P121/X1	√		√	√	√
P122/X2/ EXCLK	√		√	√	√
P123/XT1	–	√	√	√	√
P124/XT2	–	√	√	√	√

Remark √: Mounted

P120 is an I/O port with an output latch. Port 12 can be set to the input mode or output mode in 1-bit units using port mode register 12 (PM12). When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P124 are input ports.

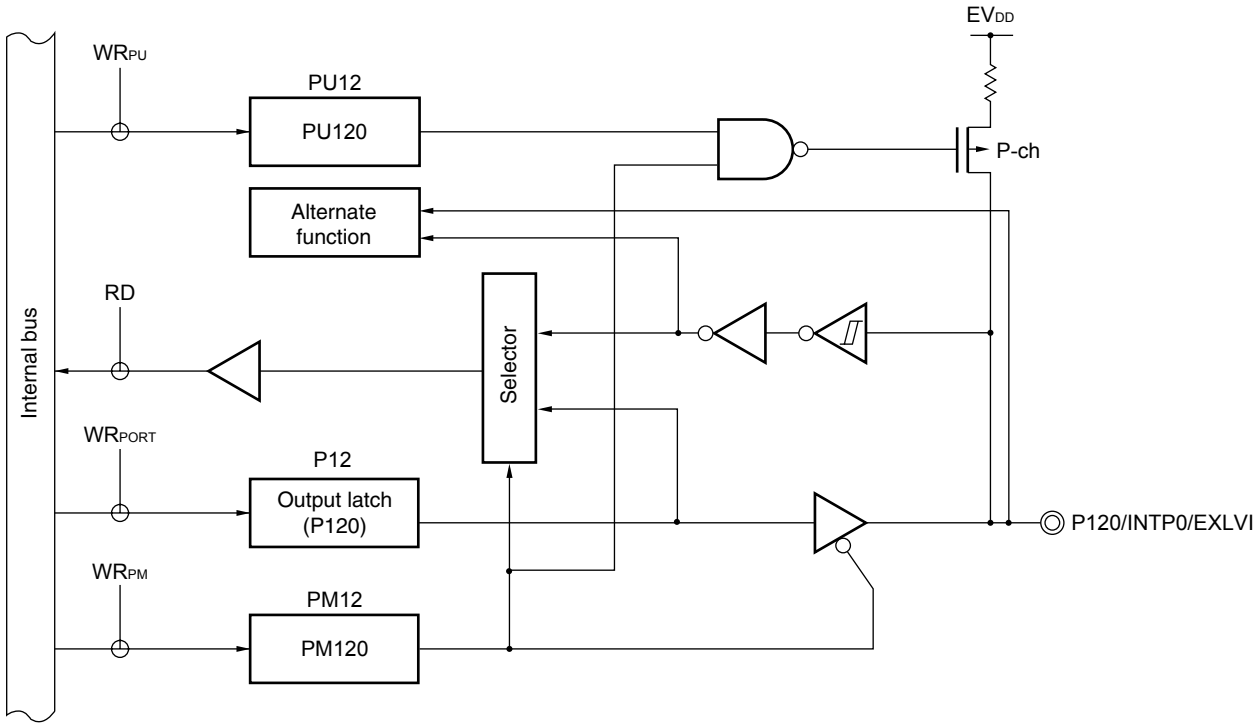
This port can also be used for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, and external clock input for main system clock.

Reset signal generation sets port 12 to input mode.

Figures 5-22 to 5-24 show block diagrams of port 12.

Caution The function setting on P121 to P124 is available only once after the reset release. The port once set for connection to an oscillator cannot be used as an input port unless the reset is performed.

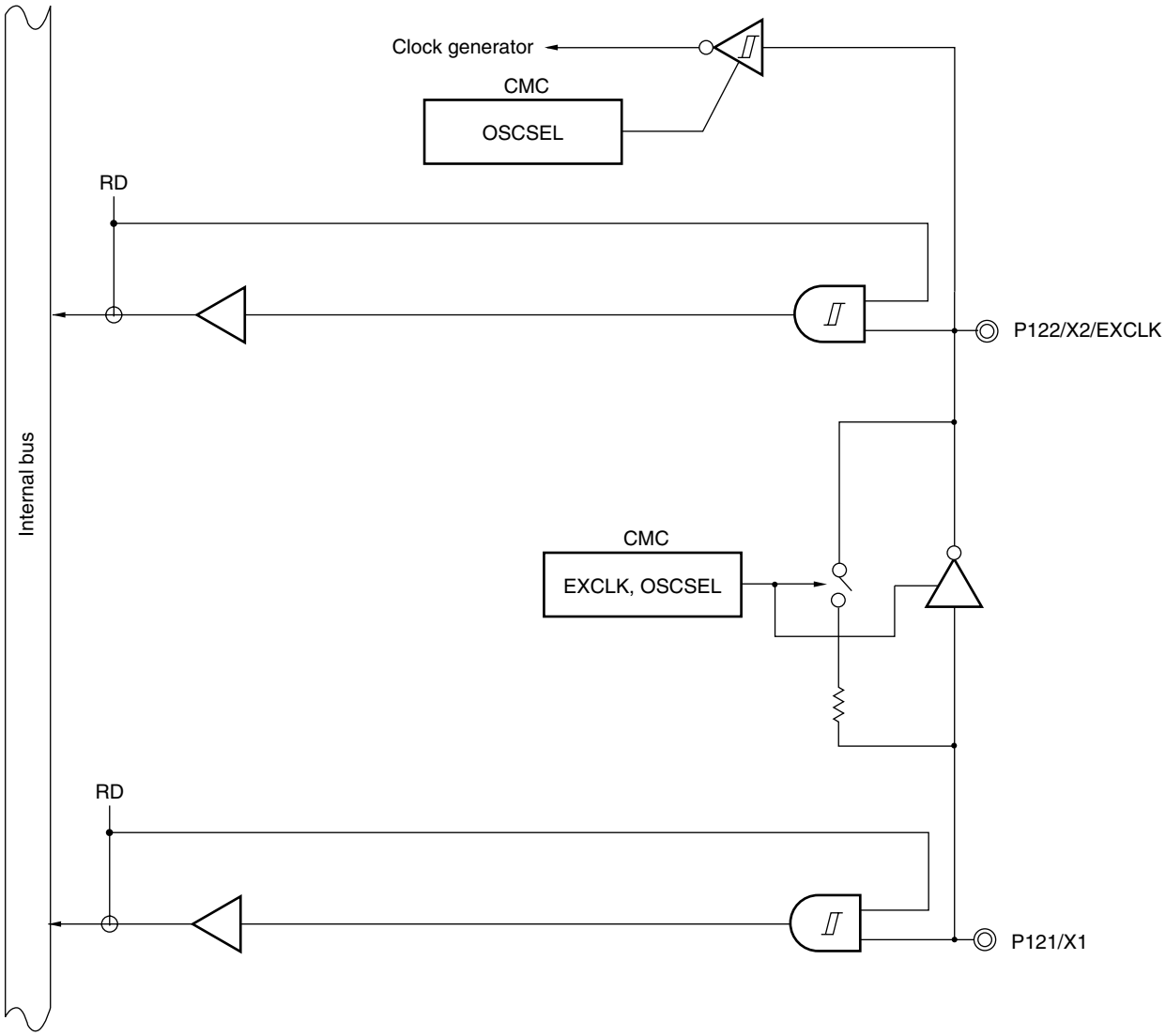
Figure 5-22. Block Diagram of P120



P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
RD: Read signal
WR××: Write signal

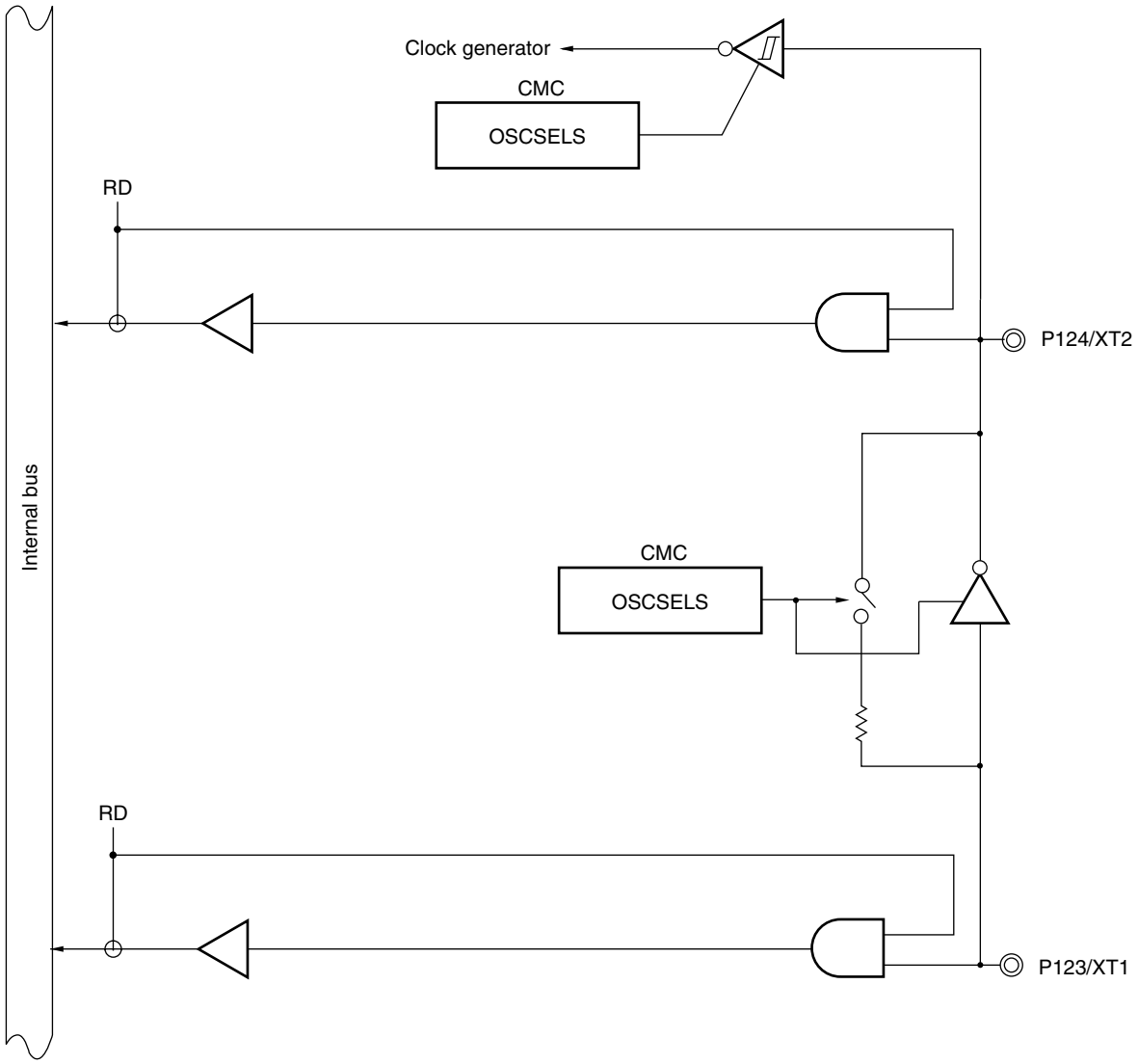
Remark With products not provided with an EVDD or EVSS pin, replace EVDD with VDD, or replace EVSS with VSS.

Figure 5-23. Block Diagram of P121 and P122



CMC: Clock operation mode control register
RD: Read signal

Figure 5-24. Block Diagram of P123 and P124



CMC: Clock operation mode control register
RD: Read signal

5.2.11 Port 14

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P140/PCLBUZ0	–		√	√	√
P141/PCLBUZ1	–		–	–	√

Remark √: Mounted

P140 is a port dedicated to output and is provided with an output latch.

P141 is an I/O port with an output latch. P141 can be set to the input mode or output mode in 1-bit units using port mode register 14 (PM14). When the P141 pin is used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 14 (PU14).

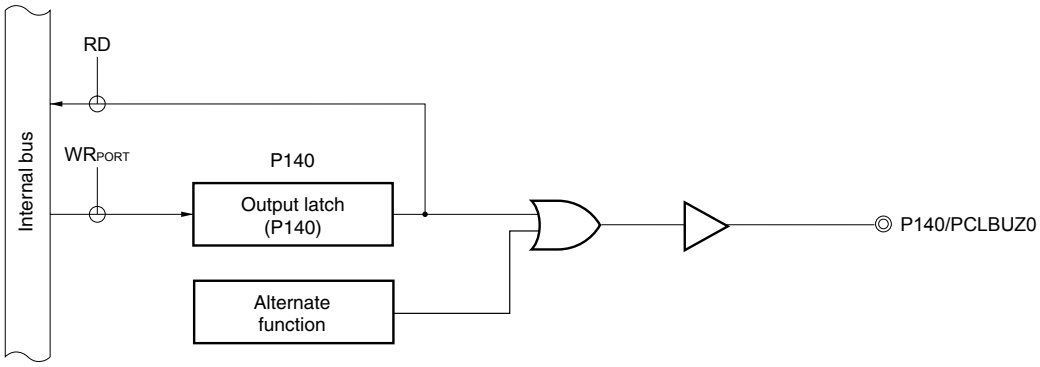
This port can also be used for clock/buzzer output.

Reset signal generation sets P141 to input mode.

Figures 5-25 and 5-26 show block diagrams of port 14.

Caution To use P140/PCLBUZ0 and P141/PCLBUZ1 as general-purpose ports, set bit 7 of clock output select registers 0 and 1 (CKS0, CKS1) to "0", which is the same as their default status setting.

Figure 5-25. Block Diagram of P140



P14: Port register 14
RD: Read signal
WR××: Write signal

Remark The P140 pin outputs a low level when it is used as a port function pin and a reset is effected. If P140 is set to output a high level, the output signal of P140 can be dummy-output as the CPU reset signal.

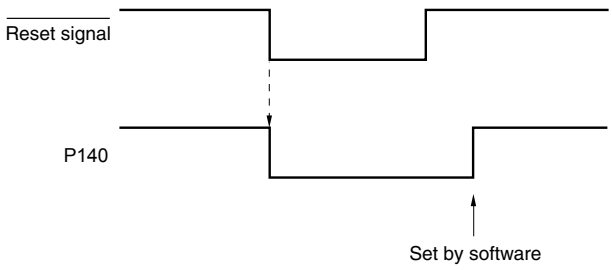
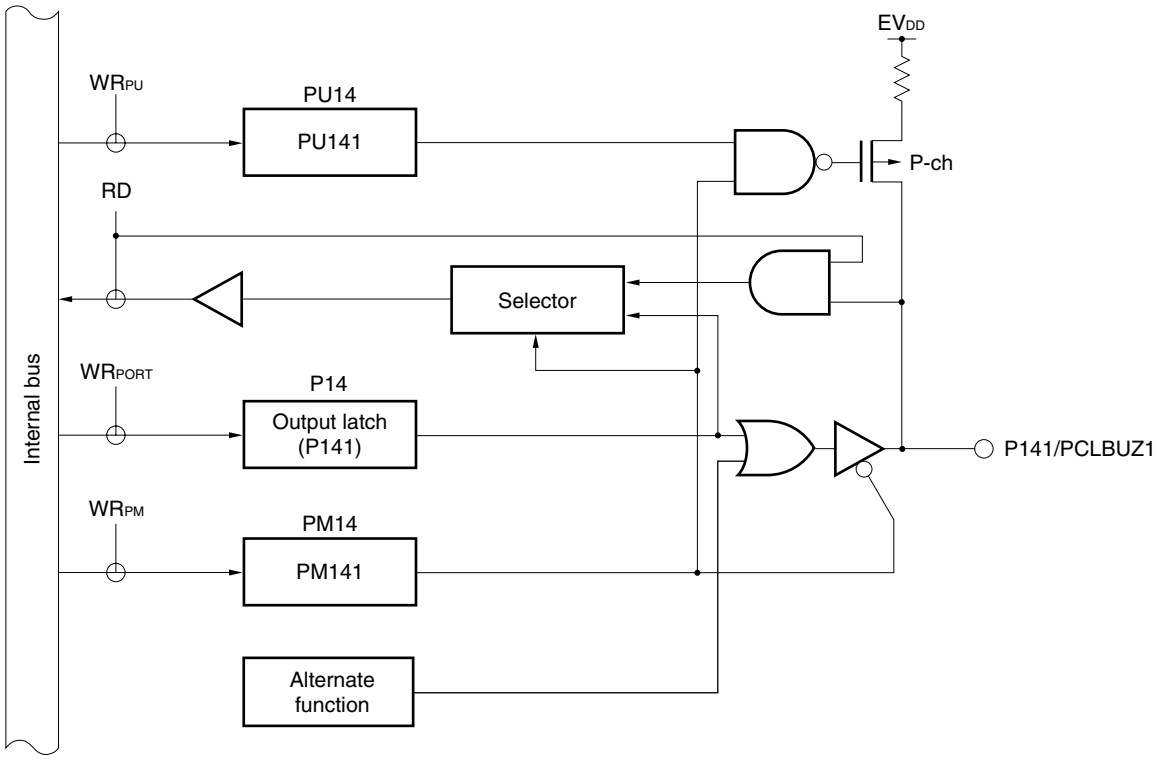


Figure 5-26. Block Diagram of P141



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
RD: Read signal
WR××: Write signal

5.2.12 Port 15

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P150/ANI8	√		√	√	√
P151/ANI9	√		√	√	√
P152/ANI10	–		√	√	√
P153/ANI11	–		–	–	√

Remark √: Mounted

Port 15 is an I/O port with an output latch. Port 15 can be set to the input mode or output mode in 1-bit units using port mode register 15 (PM15).

This port can also be used for A/D converter analog input.

To use P150/ANI8 to P153/ANI11 as digital input pins, set them in the digital I/O mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM15 register. Use these pins starting from the lower bit.

To use P150/ANI8 to P153/ANI11 as digital output pins, set them in the digital I/O mode by using the ADPC register and in the output mode by using the PM15 register.

Table 5-6. Setting Functions of P150/ANI8 to P153/ANI11 Pins

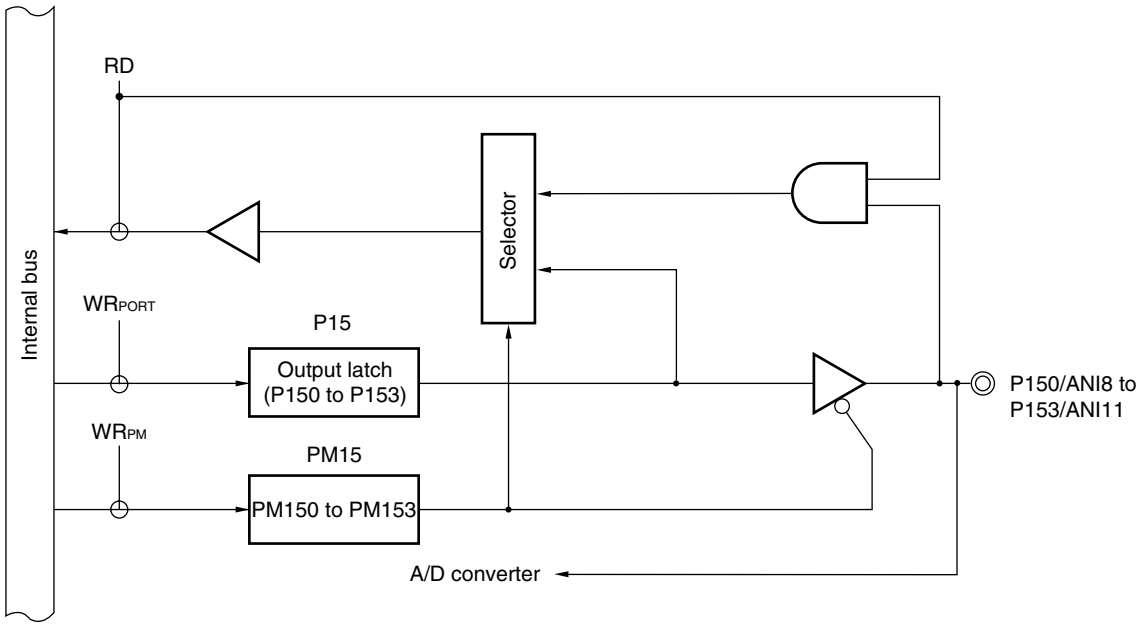
ADPC Register	PM15 Register	ADS Register	P150/ANI8 to P153/ANI11 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

All P150/ANI8 to P153/ANI11 are set in the digital input mode when the reset signal is generated.

Figure 5-27 shows block diagram of port 15.

Caution Make the AV_{REF} pin the same potential as the V_{DD} pin when port 15 is used as a digital port.

Figure 5-27. Block Diagram of P150 to P153



P15: Port register 15
PM15: Port mode register 15
RD: Read signal
WR××: Write signal

5.3 Registers Controlling Port Function

Port functions are controlled by the following six types of registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- Port input mode registers (PIM3, PIM7, PIM8)
- Port output mode registers (POM3, POM7)
- A/D port configuration register (ADPC)

(1) Port mode registers (PMxx)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH (PM13 is set to FEH).

When port pins are used as alternate-function pins, set the port mode register by referencing **5.5 Settings of Port Mode Register and Output Latch When Using Alternate Function**.

Figure 5-28. Format of Port Mode Register (78K0R/KC3-L (40-pin))

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM1	1	1	1	1	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	1	PM32	PM31	PM30	FFF23H	FFH	R/W
PM4	1	1	1	1	1	1	PM41	PM40	FFF24H	FFH	R/W
PM5	1	1	1	1	1	0	PM51	PM50	FFF25H	FFH	R/W
PM7	1	1	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM8	1	1	1	1	PM83	0	PM81	PM80	FFF28H	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM15	1	1	1	1	1	1	PM151	PM150	FFF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 1 to 5, 7, 8, 12, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Cautions 1. Be sure to set bits 4 to 7 of the PM1 register, bits 3 to 7 of the PM3 register, bits 2 to 7 of the PM4 register, bits 3 to 7 of the PM5 register, bits 6 and 7 of the PM7 register, bits 4 to 7 of the PM8 register, bits 1 to 7 of the PM12 register, and bits 2 to 7 of the PM15 register to 1.

2. Be sure to clear bit2 of the PM5 register and bit 2 of the PM8 register to "0" after the reset release.

Figure 5-29. Format of Port Mode Register (78K0R/KC3-L (44-pin and 48-pin))

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM1	1	1	1	1	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	1	PM32	PM31	PM30	FFF23H	FFH	R/W
PM4	1	1	1	1	1	1	PM41	PM40	FFF24H	FFH	R/W
PM5	1	1	1	1	1	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6 Note	1	1	1	1	1	1	PM61 Note	PM60 Note	FFF26H	FFH	R/W
PM7	1	1	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM8	1	1	1	1	PM83	PM82	PM81	PM80	FFF28H	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM15	1	1	1	1	1	PM152 Note	PM151	PM150	FFF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 1 to 8, 12, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note 48-pin products only.

Caution Be sure to set bits 4 to 7 of the PM1 register, bits 3 to 7 of the PM3 register, bits 2 to 7 of the PM4 register, bits 3 to 7 of the PM5 register, bits 2 to 7 of the PM6 register, bits 6 and 7 of the PM7 register, bits 4 to 7 of the PM8 register, bits 1 to 7 of the PM12 register, and bits 3 to 7 of the PM15 register to 1.

Figure 5-30. Format of Port Mode Register (78K0R/KD3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	1	1	1	1	1	PM01	PM00	FFF20H	FFH	R/W
PM1	1	1	1	1	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	1	PM32	PM31	PM30	FFF23H	FFH	R/W
PM4	1	1	1	1	1	1	PM41	PM40	FFF24H	FFH	R/W
PM5	1	1	1	1	1	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6	1	1	1	1	1	1	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM8	1	1	1	1	PM83	PM82	PM81	PM80	FFF28H	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM15	1	1	1	1	1	PM152	PM151	PM150	FFF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 8, 12, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits 2 to 7 of the PM0 register, bits 4 to 7 of the PM1 register, bits 3 to 7 of the PM3 register, bits 2 to 7 of the PM4 register, bits 3 to 7 of the PM5 register, bits 2 to 7 of the PM6 register, bits 4 to 7 of the PM8 register, bits 1 to 7 of the PM12 register, and bits 3 to 7 of the PM15 register to 1.

Figure 5-31. Format of Port Mode Register (78K0R/KE3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	1	1	1	1	1	PM01	PM00	FFF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	PM33	PM32	PM31	PM30	FFF23H	FFH	R/W
PM4	1	1	1	1	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
PM5	1	1	1	1	PM53	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6	1	1	1	1	1	1	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM8	1	1	1	1	PM83	PM82	PM81	PM80	FFF28H	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM14	1	1	1	1	1	1	PM141	0	FFF2EH	FEH	R/W
PM15	1	1	1	1	PM153	PM152	PM151	PM150	FFF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 8, 12, 14, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits 2 to 7 of the PM0 register, bits 4 to 7 of the PM3 register, bits 4 to 7 of the PM4 register, bits 4 to 7 of the PM5 register, bits 2 to 7 of the PM6 register, bits 4 to 7 of the PM8 register, bits 1 to 7 of the PM12 register, bits 2 to 7 of the PM14 register, and bits 4 to 7 of the PM15 register to 1. Also, be sure to set bit 0 of the PM14 register to 0.

(2) Port registers (Pxx)

These registers set the output latch value of a port.

If the data is read in the input mode, the pin level is read. If it is read in the output mode, the output latch value is read[Note].

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Note It is always 0 and never a pin level that is read out if a port is read during the input mode when P2 and P15 are set to function as an analog input for a A/D converter.

Figure 5-32. Format of Port Register (78K0R/KC3-L (40-pin))

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P1	0	0	0	0	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	0	0	0	0	0	P32	P31	P30	FFF03H	00H (output latch)	R/W
P4	0	0	0	0	0	0	P41	P40	FFF04H	00H (output latch)	R/W
P5	0	0	0	0	0	0	P51	P50	FFF05H	00H (output latch)	R/W
P7	0	0	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P8	0	0	0	0	P83	0	P81	P80	FFF08H	00H (output latch)	R/W
P12	0	0	0	0	0	P122	P121	P120	FFF0CH	Undefined	R/W[Note2]
P15	0	0	0	0	0	0	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	m = 1 to 8, 12, 14, 15 ; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Note P121 and P122 are read-only.

Figure 5-33. Format of Port Register (78K0R/KC3-L (44-pin and 48-pin))

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P1	0	0	0	0	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	0	0	0	0	0	P32	P31	P30	FFF03H	00H (output latch)	R/W
P4	0	0	0	0	0	0	P41	P40	FFF04H	00H (output latch)	R/W
P5	0	0	0	0	0	P52	P51	P50	FFF05H	00H (output latch)	R/W
P6 Note1	0	0	0	0	0	0	P61 Note1	P60 Note1	FFF06H	00H (output latch)	R/W
P7	0	0	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P8	0	0	0	0	P83	P82	P81	P80	FFF08H	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FFF0CH	Undefined	R/W Note2
P14 Note1	0	0	0	0	0	0	0	P140 Note1	FFF0EH	00H (output latch)	R/W
P15	0	0	0	0	0	P152 Note1	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	m = 1 to 8, 12, 14, 15 ; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Notes 1. P121 to P124 are read-only.

2. 48-pin products only.

Figure 5-34. Format of Port Register (78K0R/KD3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	0	0	0	0	0	P01	P00	FFF00H	00H (output latch)	R/W
P1	0	0	0	0	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	0	0	0	0	0	P32	P31	P30	FFF03H	00H (output latch)	R/W
P4	0	0	0	0	0	0	P41	P40	FFF04H	00H (output latch)	R/W
P5	0	0	0	0	0	P52	P51	P50	FFF05H	00H (output latch)	R/W
P6	0	0	0	0	0	0	P61	P60	FFF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P8	0	0	0	0	P83	P82	P81	P80	FFF08H	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FFF0CH	Undefined	R/W[Note]
P14	0	0	0	0	0	0	0	P140	FFF0EH	00H (output latch)	R/W
P15	0	0	0	0	0	P152	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	m = 0 to 8, 12, 14, 15 ; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Note P121 to P124 are read-only.

Figure 5-35. Format of Port Register (78K0R/KE3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	0	0	0	0	0	P01	P00	FFF00H	00H (output latch)	R/W
P1	P17	P16	P15	P14	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	0	0	0	0	P33	P32	P31	P30	FFF03H	00H (output latch)	R/W
P4	0	0	0	0	P43	P42	P41	P40	FFF04H	00H (output latch)	R/W
P5	0	0	0	0	P53	P52	P51	P50	FFF05H	00H (output latch)	R/W
P6	0	0	0	0	0	0	P61	P60	FFF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P8	0	0	0	0	P83	P82	P81	P80	FFF08H	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FFF0CH	Undefined	R/W[Note]
P14	0	0	0	0	0	0	P141	P140	FFF0EH	00H (output latch)	R/W
P15	0	0	0	0	P153	P152	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	m = 0 to 8, 12, 14, 15 ; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Note P121 to P124 are read-only.

(3) Pull-up resistor option registers (PUxx)

These registers specify whether the on-chip pull-up resistors are to be used or not. On-chip pull-up resistors can be used in 1-bit units only for the bits set to input mode of the pins to which the use of an on-chip pull-up resistor has been specified in these registers. On-chip pull-up resistors cannot be connected to bits set to output mode and bits used as alternate-function output pins, regardless of the settings of these registers.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 5-36. Format of Pull-up Resistor Option Register (78K0R/KC3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU1	0	0	0	0	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU3	0	0	0	0	0	PU32	PU31	PU30	F0033H	00H	R/W
PU4	0	0	0	0	0	0	PU41	PU40	F0034H	00H	R/W
PU5	0	0	0	0	0	PU52[Note]	PU51	PU50	F0035H	00H	R/W
PU7	0	0	PU75	PU74	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	F003CH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 1, 3 to 5, 7, 12 ; n = 0 to 5)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Note In the case of the 40-pin product, be sure to clear PU52 bit of the PU5 register to “0”.

Figure 5-37. Format of Pull-up Resistor Option Register (78K0R/KD3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	0	0	0	0	0	PU01	PU00	F0030H	00H	R/W
PU1	0	0	0	0	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU3	0	0	0	0	0	PU32	PU31	PU30	F0033H	00H	R/W
PU4	0	0	0	0	0	0	PU41	PU40	F0034H	00H	R/W
PU5	0	0	0	0	0	PU52	PU51	PU50	F0035H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	F003CH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 5, 7, 12 ; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Figure 5-38. Format of Pull-up Resistor Option Register (78K0R/KE3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	0	0	0	0	0	PU01	PU00	F0030H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU3	0	0	0	0	PU33	PU32	PU31	PU30	F0033H	00H	R/W
PU4	0	0	0	0	PU43	PU42	PU41	PU40	F0034H	00H	R/W
PU5	0	0	0	0	PU53	PU52	PU51	PU50	F0035H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	F003CH	00H	R/W
PU14	0	0	0	0	0	0	PU141	0	F003EH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 5, 7, 12, 14 ; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

(4) Port input mode registers (PIM3, PIM7, PIM8)

The PIM3 and PIM7 registers set the input buffer of P31, P32, P71, P72, P74, or P75 in 1-bit units.

TTL input buffer can be selected during serial communication with an external device of the different potential.

The PIM8 register is used to enable or disable the digital inputs to P80 to P83 in 1-bit units. When using a comparator or a programmable gain amplifier, the digital inputs are disabled (used as analog input) by software processing. To use port functions and alternative functions, the digital inputs must be enabled, because they are disabled (used as analog input) by default.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 5-39. Format of Port Input Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PIM3	0	0	0	0	0	PIM32	PIM31	0	F0043H	00H	R/W
PIM7	0	0	PIM75	PIM74	0	PIM72	PIM71	0	F0047H	00H	R/W
PIM8	0	0	0	0	PIM83	PIM82[Note]	PIM81	PIM80	F0048H	00H	R/W

PIMmn	Pmn pin input buffer selection (m = 3 and 7; n = 1, 2, 4, 5)
0	Normal input buffer
1	TTL input buffer

PIM8n	P8n pin digital input buffer selection (n = 0 to 3)
0	Disables digital input (used as analog input)
1	Enables digital input

Note In the case of the 40-pin product, be sure to clear PIM82 bit of the PIM8 register to “0”.

(5) Port output mode registers (POM3, POM7)

These registers set the output mode of P30 to P32, P70, P72, P73, or P75 in 1-bit units.

N-ch open drain output (V_{DD} tolerance) mode can be selected during serial communication with an external device of the different potential, and for the SDA10 pin during simplified I^2C communication with an external device of the same potential.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 5-40. Format of Port Output Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM3	0	0	0	0	0	POM32	POM31	POM30	F0053H	00H	R/W
POM7	0	0	POM75	0	POM73	POM72	0	POM70	F0057H	00H	R/W

POMmn	Pmn pin output mode selection (m = 3 and 7; n = 0 to 3 and 5)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance) mode

(6) A/D port configuration register (ADPC)

This register switches the ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI11/P153 pins to digital I/O of port or analog input of A/D converter.

The ADPC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 5-41. Format of A/D Port Configuration Register (ADPC)

Address: F0017H After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching											
					Port 15				Port 2							
					ANI11 /P153	ANI10 /P152	ANI9 /P151	ANI8 /P150	ANI7 /P27	ANI6 /P26	ANI5 /P25	ANI4 /P24	ANI3 /P23	ANI2 /P22	ANI1 /P21	ANI0 /P20
0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	0	1	A	A	A	A	A	A	A	A	A	A	A	D
0	0	0	1	0	A	A	A	A	A	A	A	A	A	A	D	D
0	0	0	1	1	A	A	A	A	A	A	A	A	A	D	D	D
0	0	1	0	0	A	A	A	A	A	A	A	A	D	D	D	D
0	0	1	0	1	A	A	A	A	A	A	A	D	D	D	D	D
0	0	1	1	0	A	A	A	A	A	A	D	D	D	D	D	D
0	0	1	1	1	A	A	A	A	A	D	D	D	D	D	D	D
0	1	0	0	0	A	A	A	A	D	D	D	D	D	D	D	D
0	1	0	0	1	A	A	A	D	D	D	D	D	D	D	D	D
0	1	0	1	0	A	A	D	D	D	D	D	D	D	D	D	D
0	1	0	1	1	A	D	D	D	D	D	D	D	D	D	D	D
1	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D
Other than the above					Setting prohibited											

Cautions 1. Set a channel to be used for A/D conversion in the input mode by using port mode register 2 and 15 (PM2, PM15).

2. Do not set the pin that is set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

3. Be sure to first set the ADCEN bit of peripheral enable register 0 (PER0) to 1 when setting up the ADPC register. If ADCEN = 0, writing to the ADPC register is ignored and specified values are returned to the initial values.

Remark P20/ANI0 to P27/ANI7, P150/ANI8, and P151/ANI9: 78K0R/KC3-L (40-pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L

5.4 Port Function Operations

Port operations differ depending on whether the input or output mode is set, as shown below.

5.4.1 Writing to I/O port

(1) Output mode

A value is written to the output latch by a transfer instruction, and the output latch contents are output from the pin.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

A value is written to the output latch by a transfer instruction, but since the output buffer is off, the pin status does not change.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

5.4.2 Reading from I/O port

(1) Output mode

The output latch contents are read by a transfer instruction. The output latch contents do not change.

(2) Input mode

The pin status is read by a transfer instruction. The output latch contents do not change.

5.4.3 Operations on I/O port

(1) Output mode

An operation is performed on the output latch contents, and the result is written to the output latch. The output latch contents are output from the pins.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

The pin level is read and an operation is performed on its contents. The result of the operation is written to the output latch, but since the output buffer is off, the pin status does not change.
The data of the output latch is cleared when a reset signal is generated.

5.4.4 Connecting to external device with different power potential (2.5 V, 3 V)

When ports 3 and 7 operate with V_{DD} = 4.0 V to 5.5 V, I/O connections with an external device that operates on a 2.5V or 3 V power supply voltage are possible.

Regarding inputs, normal input (CMOS)/TTL switching is possible on a bit-by-bit basis by port input mode registers 3 and 7 (PIM3 and PIM7).

Moreover, regarding outputs, different power potentials can be supported by switching the output buffer to the N-ch open drain (V_{DD} withstand voltage) by port output mode registers 3 and 7 (POM3 and POM7).

(1) Setting procedure when using I/O pins of UART0, UART1 CSI00, CSI01, and CSI10 functions

(a) Use as 2.5V or 3 V input port

<1> After reset release, the port mode is the input mode (Hi-Z).

<2> If pull-up is needed, externally pull up the pin to be used (on-chip pull-up resistor cannot be used).

In case of UART0: P74
In case of UART1: P31
In case of CSI00: P74, P75
In case of CSI01: P71, P72
In case of CSI10: P31, P32

<3> Set the corresponding bit of the PIM3 and PIM7 registers to 1 to switch to the TTL input buffer.

<4> V_{IH}/V_{IL} operates on a 2.5V or 3 V operating voltage.

(b) Use as 2.5V or 3 V output port

<1> After reset release, the port mode changes to the input mode (Hi-Z).

<2> Pull up externally the pin to be used (on-chip pull-up resistor cannot be used).

In case of UART0: P73
In case of UART1: P30
In case of CSI00: P73, P75
In case of CSI01: P70, P72
In case of CSI10: P30, P32

<3> Set the output latch of the corresponding port to 1.

<4> Set the corresponding bit of the POM3 and POM7 registers to 1 to set the N-ch open drain output (V_{DD} withstand voltage) mode.

<5> Set the output mode by manipulating the PM3 and PM7 registers.
At this time, the output data is high level, so the pin is in the Hi-Z state.

<6> Communication is started by setting the serial array unit.

(2) Setting procedure when using I/O pins of simplified IIC10 functions

<1> After reset release, the port mode is the input mode (Hi-Z).

<2> Externally pull up the pin to be used (on-chip pull-up resistor cannot be used).

In case of simplified IIC10: P31, P32

<3> Set the output latch of the corresponding port to 1.

<4> Set the corresponding bit of the POM3 register to 1 to set the N-ch open drain output (V_{DD} withstand voltage) mode.

<5> Set the corresponding bit of the PM3 register to the output mode (data I/O is possible in the output mode). At this time, the output data is high level, so the pin is in the Hi-Z state.

<6> Enable the operation of the serial array unit and set the mode to the simplified I^2C mode.

5.5 Settings of Port Mode Register and Output Latch When Using Alternate Function

To use the alternate function of a port pin, set the port mode register and output latch as shown in Table 5-7.

Table 5-7. Settings of Port Mode Register and Output Latch When Using Alternate Function (1/2)

Pin Name	Alternate Function		PIM8	PM××	P××
	Function Name	I/O			
P00	TI00	Input	–	1	×
P01	TO00	Output	–	0	0
P10	TI02	Input	–	1	×
	TO02	Output	–	0	0
P11	TI03	Input	–	1	×
	TO03	Output	–	0	0
P12	TI04	Input	–	1	×
	TO04	Output	–	0	0
	RTCDIV	Output	–	0	0
	RTCCL	Output	–	0	0
P13	TI05	Input	–	1	×
	TO05	Output	–	0	0
P14 Note 1	TI06 Note 1	Input	–	1	×
	TO06 Note 1	Output	–	0	0
P15 Note 1	TI07 Note 1	Input	–	1	×
	TO07 Note 1	Output	–	0	0
P20 to P27 Note 2	ANI0 to ANI7 Note 2	Input	–	1	×
P30	SO10	Output	–	0	1
	TxD1	Output	–	0	1
P31	SI10	Input	–	1	×
	RxD1	Input	–	1	×
	SDA10	I/O	–	0	1
	INTP1	Input	–	1	×
P32	$\overline{SCK10}$	Input	–	1	×
		Output	–	0	1
	SCL10	I/O	–	0	1
	INTP2	Input	–	1	×
P40	TOOL0	I/O	–	×	×
P41	TOOL1	Output	–	×	×
P50 Note 1	TI06 Note 1	Input	–	1	×
	TO06 Note 1	Output	–	0	0
P51 Note 1	TI07 Note 1	Input	–	1	×
	TO07 Note 1	Output	–	0	0

Remark ×: don't care
PM××: Port mode register
P××: Port output latch

(**Note** is listed on the next page after next.)

Table 5-7. Settings of Port Mode Register and Output Latch When Using Alternate Function (2/2)

Pin Name	Alternate Function		PIM8	PM××	P××
	Function Name	I/O			
P52	RTC1HZ	Output	–	0	0
	SLTI	Input	–	1	×
	SLTO	Output	–	0	0
P60	SCL0	I/O	–	0	0
P61	SDA0	I/O	–	0	0
P70	KR0	Input	–	1	×
	SO01	Output	–	0	1
	INTP4	Input	–	1	×
P71	KR1	Input	–	1	×
	SI01	Input	–	1	×
	INTP5	Input	–	1	×
P72	KR2	Input	–	1	×
	$\overline{SCK01}$	Input	–	1	×
		Output	–	0	1
	INTP6	Input	–	1	×
P73	KR3	Input	–	1	×
	SO00	Output	–	0	1
	TxD0	Output	–	0	1
P74	KR4	Input	–	1	×
	SI00	Input	–	1	×
	RxD0	Input	–	1	×
P75	KR5	Input	–	1	×
	$\overline{SCK00}$	Input	–	1	×
		Output	–	0	1
P76	KR6	Input	–	1	×
P77	KR7	Input	–	1	×
P80[Note 2]	CMP0P	Input	PIM80 = 0	1	×
	INTP3	Input	PIM80 = 1	1	×
	PGAI [Note 2]	Input	PIM80 = 0	1	×
P81	CMP0M	Input	PIM81 = 0	1	×
P82	CMP1P	Input	PIM82 = 0	1	×
	INTP7	Input	PIM82 = 1	1	×
P83	CMP1M	Input	PIM83 = 0	1	×
P120	INTP0	Input	–	1	×
	EXLVI	Input	–	1	×
P140	PCLBUZ0	Output	–	0	0
P141	PCLBUZ1	Output	–	0	0
P150 to P153[Note 2]	ANI8 to ANI11[Note 2]	Input	–	1	×

Remark ×: don't care
PM××: Port mode register
P××: Port output latch

(**Note** is listed on the next page.)

Notes 1. The ports with which the TI06/TO06 and TI07/TO07 pins are shared differ depending on the product.
78K0R/KC3-L, 78K0R/KD3-L: P50/TI06/TO06, P51/TI07/TO07
78K0R/KE3-L: P14/TI06/TO06, P15/TI07/TO07

2. The function of the ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI11/P153 pins can be selected by using the A/D port configuration register (ADPC), analog input channel specification register (ADS), and port mode registers 2, 15 (PM2, PM15).

Table 5-8. Setting Functions of ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI11/P153 Pins

ADPC Register	PM2 and PM15 Registers	ADS Register	ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI11/P153 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

Remark P20/ANI0 to P27/ANI7, P150/ANI8, and P151/ANI9: 78K0R/KC3-L (40pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L

5.6 Cautions on 1-bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P10 is an output port, P11 to P17 are input ports (all pin statuses are high level), and the port latch value of port 1 is 00H, if the output of output port P10 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 1 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L.

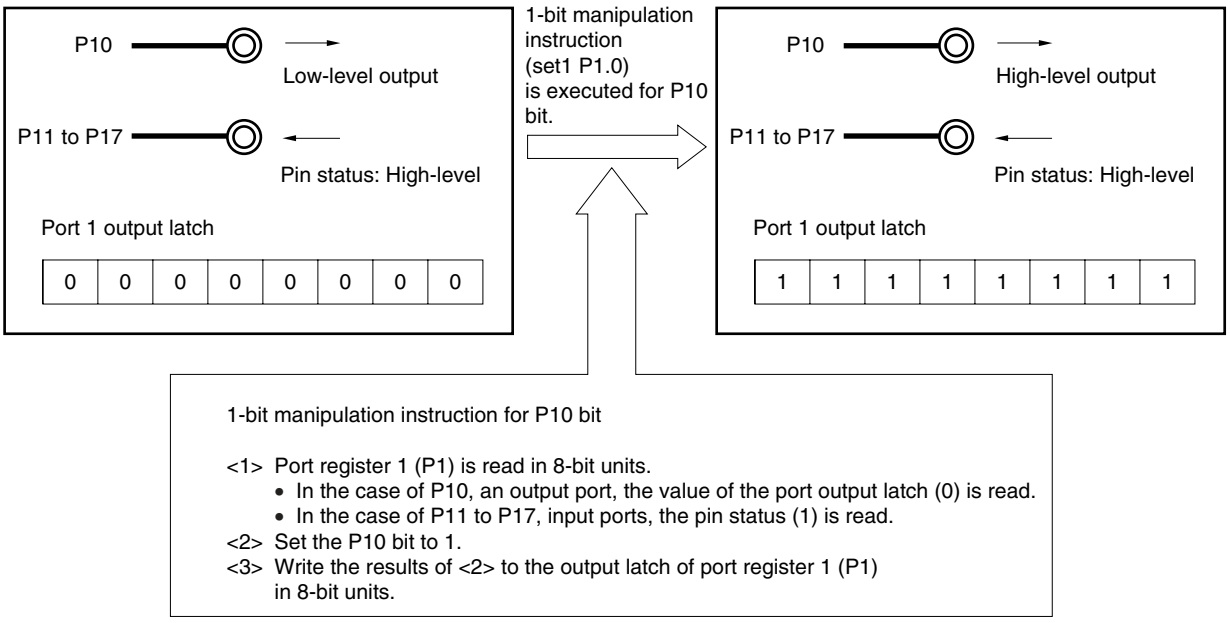
<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P10, which is an output port, is read, while the pin statuses of P11 to P17, which are input ports, are read. If the pin statuses of P11 to P17 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 5-42. Bit Manipulation Instruction (P10)



CHAPTER 6 PORT FUNCTIONS (78K0R/KF3-L, 78K0R/KG3-L)

Caution For the functions of the port in the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L, see CHAPTER 5 PORT FUNCTIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L).

6.1 Port Functions

Pin I/O buffer power supplies depend on the product. The relationship between these power supplies and the pins is shown below.

Table 6-1. Pin I/O Buffer Power Supplies (AV_{REF}, EV_{DD0}, V_{DD})

- 78K0R/KF3-L: 80-pin plastic LQFP (14x14)
  80-pin plastic LQFP (fine pitch) (12x12)

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27, P150 to P153
EV_{DD0}	• Port pins other than P20 to P27, P121 to P124, and P150 to P153 • $\overline{\text{RESET}}$ and FLMD0 pins
V_{DD}	• P121 to P124 • Pins other than port pins (excluding $\overline{\text{RESET}}$ and FLMD0 pins)

Table 6-2. Pin I/O Buffer Power Supplies (AV_{REF}, EV_{DD0}, EV_{DD1}, V_{DD})

- 78K0R/KG3-L: 100-pin plastic LQFP (14x20)
  100-pin plastic LQFP (fine pitch) (14x14)
  100-pin plastic FBGA (6x6)[Note]

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27, P150 to P157
EV_{DD0}, EV_{DD1}	• Port pins other than P20 to P27, P121 to P124, and P150 to P157 • $\overline{\text{RESET}}$ and FLMD0 pins
V_{DD}	• P121 to P124 • Pins other than port pins (excluding $\overline{\text{RESET}}$ and FLMD0 pins)

The 78K0R/KF3-L, 78K0R/KG3-L microcontrollers are provided with digital I/O ports, which enable variety of control operations. The functions of each port are shown in Table 6-3.

In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 3 PIN FUNCTIONS (78K0R/KF3-L, 78K0R/KG3-L)**.

Note μPD78F1013 and μPD78F1014 only

Table 6-3. Port Functions (1/4)

KF3-L	KG3-L	Function Name	I/O	Function	After Reset	Alternate Function
–	√	P00	I/O	Port 0. I/O port. Input of P03 and P04 can be set to TTL input buffer. Output of P02 to P04 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI00
–	√	P01				TO00
√	√	P02				SO10/TxD1
√	√	P03				SI10/RxD1/SDA10
√	√	P04				$\overline{\text{SCK10}}$/SCL10
√	√	P05				[KF3-L] TI05/TO05 [KG3-L] –
√	√	P06				[KF3-L] TI06/TO06 [KG3-L] –
√	√	P10	I/O	Port 1. I/O port. Input of P10 and P11 can be set to TTL input buffer. Output of P10 and P12 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK00}}$
√	√	P11				SI00/RxD0
√	√	P12				SO00/TxD0
√	√	P13				TxD3
√	√	P14				RxD3
√	√	P15				RTCDIV/RTCCL
√	√	P16				TI01/TO01/INTP5
√	√	P17				TI02/TO02
√	√	P20 to P27	I/O	Port 2. I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
√	√	P30	I/O	Port 3. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	RTC1HZ/INTP3
√	√	P31				TI03/TO03/INTP4
√	√	P40[Note]	I/O	Port 4. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
√	√	P41				TOOL1
√	√	P42				TI04/TO04
√	√	P43				$\overline{\text{SCK01}}$
√	√	P44				SI01
√	√	P45				SO01
√	√	P46				[KF3-L] – [KG3-L] INTP1/TI05/TO05
√	√	P47				[KF3-L] – [KG3-L] INTP2

Note If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally (see **Caution** in **3.2.5 P40 to P47 (port 4)**).

Table 6-3. Port Functions (2/4)

KF3-L	KG3-L	Function Name	I/O	Function	After Reset	Alternate Function
√	√	P50	I/O	Port 5. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	[KF3-L (μ PD78F1010, 78F1011, 78F1012)] INTP1 [KG3-L (μ PD78F1013, 78F1014)] – [KF3-L(μ PD78F1027, 78F1028)] INTP1/$\overline{\text{SCK40}}$ [KG3-L(μ PD78F1029, 78F1030)] $\overline{\text{SCK40}}$
√	√	P51				[KF3-L (μ PD78F1010, 78F1011, 78F1012)] INTP2 [KG3-L (μ PD78F1013, 78F1014)] – [KF3-L(μ PD78F1027, 78F1028)] INTP2/SI40/RxD4 [KG3-L(μ PD78F1029, 78F1030)] SI40/RxD4
√	√	P52				[KF3-L (μ PD78F1010, 78F1011, 78F1012)] TO00 [KG3-L (μ PD78F1013, 78F1014)] – [KF3-L(μ PD78F1027, 78F1028)] TO00/SO40/TxD4 [KG3-L(μ PD78F1029, 78F1030)] SO40/TxD4
√	√	P53				[KF3-L (μ PD78F1010, 78F1011, 78F1012)] TI00 [KG3-L (μ PD78F1013, 78F1014)] – [KF3-L (μ PD78F1027, 78F1028)] TI00/$\overline{\text{SCK41}}$ [KG3-L(μ PD78F1029, 78F1030)] $\overline{\text{SCK41}}$

Table 6-3. Port Functions (3/4)

KF3-L	KG3-L	Function Name	I/O	Function	After Reset	Alternate Function
√	√	P54	I/O	Port 5. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	[KF3-L (μ PD78F1010, 78F1011, 78F1012)] TI07/TO07 [KG3-L (μ PD78F1013, 78F1014)] – [KF3-L(μ PD78F1027, 78F1028)] TI00/TO07/SI41 [KG3-L(μ PD78F1029, 78F1030)] SI41
√	√	P55				KF3-L (μ PD78F1010, 78F1011, 78F1012)] PCLBUZ1/INTP7 [KG3-L (μ PD78F1013, 78F1014)] – [KF3-L (μ PD78F1027, 78F1028)] PCLBUZ1/INTP7/SO41 [KG3-L(μ PD78F1029, 78F1030)] SO41
–	√	P56				–
–	√	P57				–
√	√	P60	I/O	Port 6. I/O port. Output of P60 to P63 is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units. For only P64 to P67, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCL0
√	√	P61				SDA0
√	√	P62, P63				–
√	√	P64 to P67				TI10/TO10 to TI13/TO13
√	√	P70 to P73	I/O	Port 7. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0 to KR3
√	√	P74 to P77				KR4/INTP8 to KR7/INTP11
–	√	P80 to P87	I/O	Port 8. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–

Table 6-3. Port Functions (4/4)

KF3-L	KG3-L	Function Name	I/O	Function	After Reset	Alternate Function
√	–	P90	I/O	Port 9. I/O port. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
√	√	P91				
√	√	P110, P111	I/O	Port 11. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
√	√	P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
√	√	P121	Input			X1
√	√	P122				X2/EXCLK
√	√	P123				XT1
√	√	P124				XT2
√	√	P130	Output	Port 13. 1-bit output port and 1-bit I/O port. For only P131, use of an on-chip pull-up resistor can be specified by a software setting.	Output port	–
–	√	P131	I/O		Input port	TI06/TO06
√	√	P140	I/O	Port 14. I/O port. Input of P142 and P143 can be set to TTL input buffer. Output of P142 to P144 can be set to the N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0/INTP6
–	√	P141				PCLBUZ1/INTP7
√	√	P142				$\overline{SCK20}$/SCL20
√	√	P143				SI20/RxD2/SDA20
√	√	P144				SO20/TxD2
–	√	P145				TI07/TO07
√	√	P150	I/O	Port 15. I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8
√	√	P151				ANI9
√	√	P152				ANI10
√	√	P153				ANI11
–	√	P154				ANI12
–	√	P155				ANI13
–	√	P156				ANI14
–	√	P157				ANI15

6.2 Port Configuration

Ports include the following hardware.

Table 6-4. Port Configuration

Item	Configuration
Control registers	• 78K0R/KF3-L Port mode registers (PM0 to PM7, PM9, PM11, PM12, PM14, PM15) Port registers (P0 to P7, P9, P11 to P15) Pull-up resistor option registers (PU0, PU1, PU3 to PU7, PU9, PU11, PU12, PU14) Port input mode registers (PIM0, PIM1, PIM14) Port output mode registers (POM0, POM1, POM14) A/D port configuration register (ADPC) • 78K0R/KG3-L Port mode registers (PM0 to PM9, PM11 to PM15) Port registers (P0 to P9, P11 to P15) Pull-up resistor option registers (PU0, PU1, PU3 to PU9, PU11 to PU14) Port input mode registers (PIM0, PIM1, PIM14) Port output mode registers (POM0, POM1, POM14) A/D port configuration register (ADPC)
Port	• 78K0R/KF3-L Total: 71 (CMOS I/O: 62, CMOS input: 4, CMOS output: 1, N-ch open drain I/O: 4) • 78K0R/KG3-L Total: 89 (CMOS I/O: 80, CMOS input: 4, CMOS output: 1, N-ch open drain I/O: 4)
Pull-up resistor	• 78K0R/KF3-L Total: 50 • 78K0R/KG3-L Total: 64

6.2.1 Port 0

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P00/TI00	–Note 1	√
P01/TO00	–Note 1	√
P02/SO10/TxD1	√	√
P03/SI10/RxD1/SDA10	√	√
P04/$\overline{\text{SCK10}}$/SCL10	√	√
P05/TI05/TO05	√	P05Note 2
P06/TI06/TO06	√	P06Note 2

Notes 1. TI00 and TO00 are shared with P53 and P52, respectively, in the 78K0R/KF3-L.

2. TI05/TO05 and TI06/TO06 are shared with P46 and P131, respectively, in the 78K0R/KG3-L.

Port 0 is an I/O port with an output latch. Port 0 can be set to the input mode or output mode in 1-bit units using port mode register 0 (PM0). When the P00 to P06 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 0 (PU0).

Input to the P03 and P04 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 0 (PIM0).

Output from the P02 to P04 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 0 (POM0).

This port can also be used for timer I/O, serial interface data I/O, and clock I/O.

Reset signal generation sets port 0 to input mode.

Figures 6-1 to 6-5 show block diagrams of port 0.

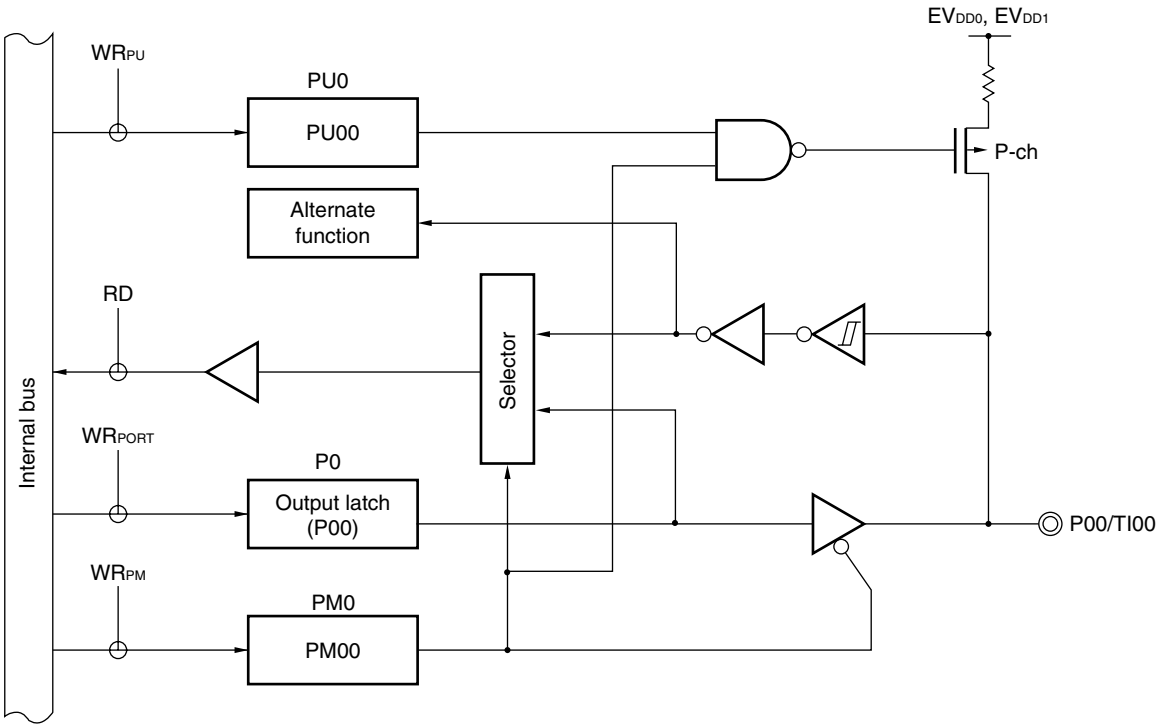
Cautions 1. To use P01/TO00 as a general-purpose port, set bit 0 (TO00) of timer output register 0 (TO0) and bit 0 (TOE00) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

2. To use P02/SO10/TxD1, P03/SI10/RxD1/SDA10, or P04/$\overline{\text{SCK10}}$/SCL10 as a general-purpose port, note the serial array unit 0 setting. For details, refer to the following tables.

- **Table 14-11 Relationship Between Register Settings and Pins (Channel 2 of Unit 0: CSI10, UART1 Transmission, IIC10)**
- **Table 14-12 Relationship Between Register Settings and Pins (Channel 3 of Unit 0: UART1 Reception)**

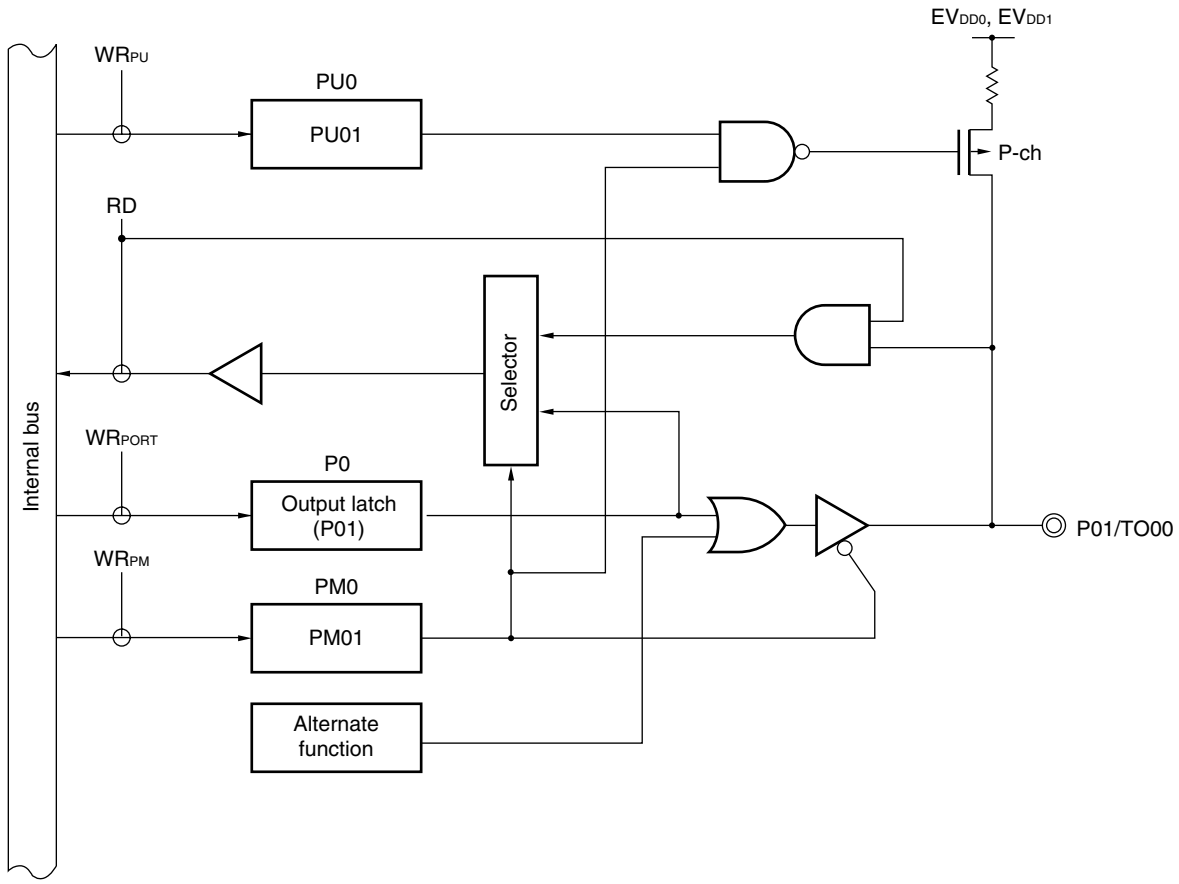
3. To use P05/TI05/TO05 or P06/TI06/TO06 as a general-purpose port, set bits 5 and 6 (TO05, TO06) of timer output register 0 (TO0) and bits 5 and 6 (TOE05, TOE06) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

Figure 6-1. Block Diagram of P00



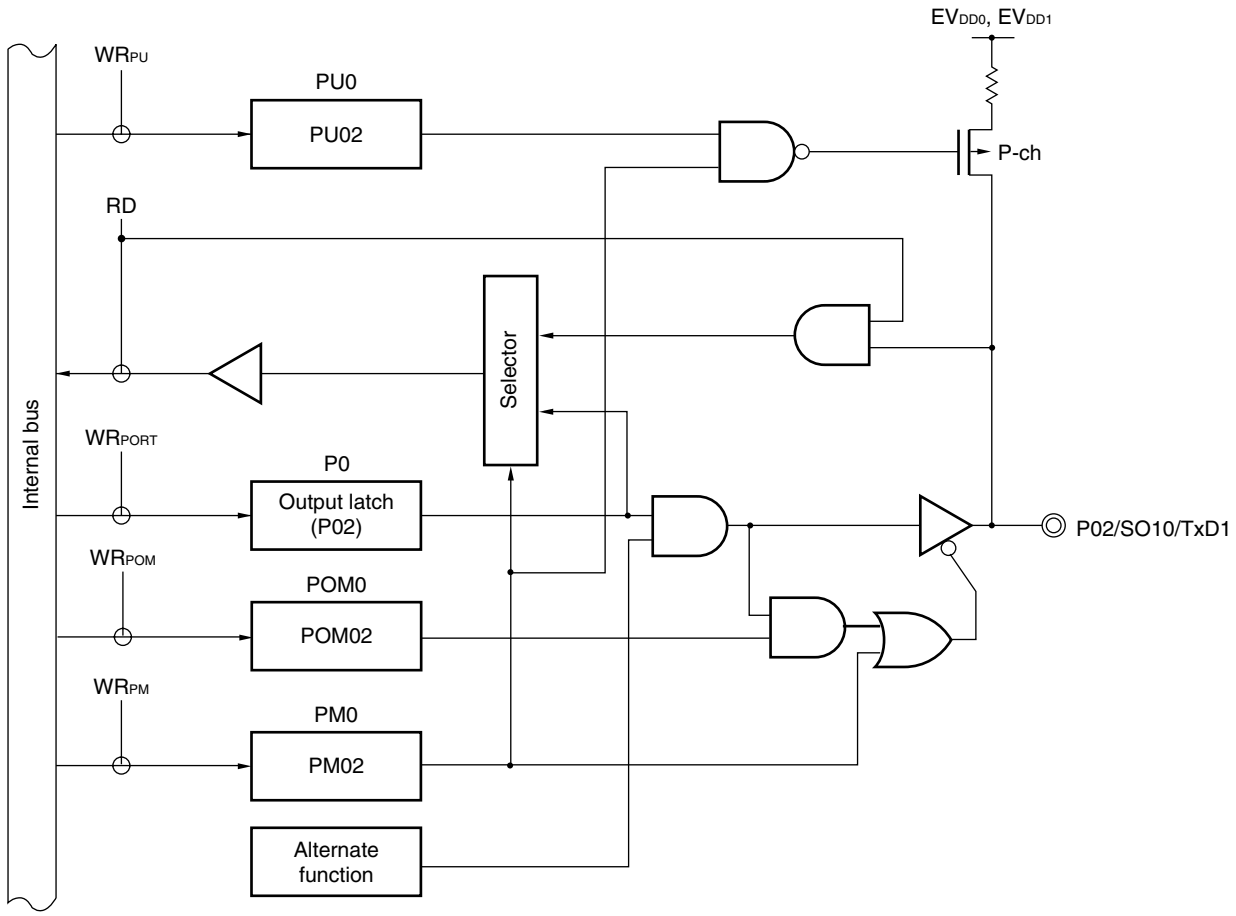
P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

Figure 6-2. Block Diagram of P01



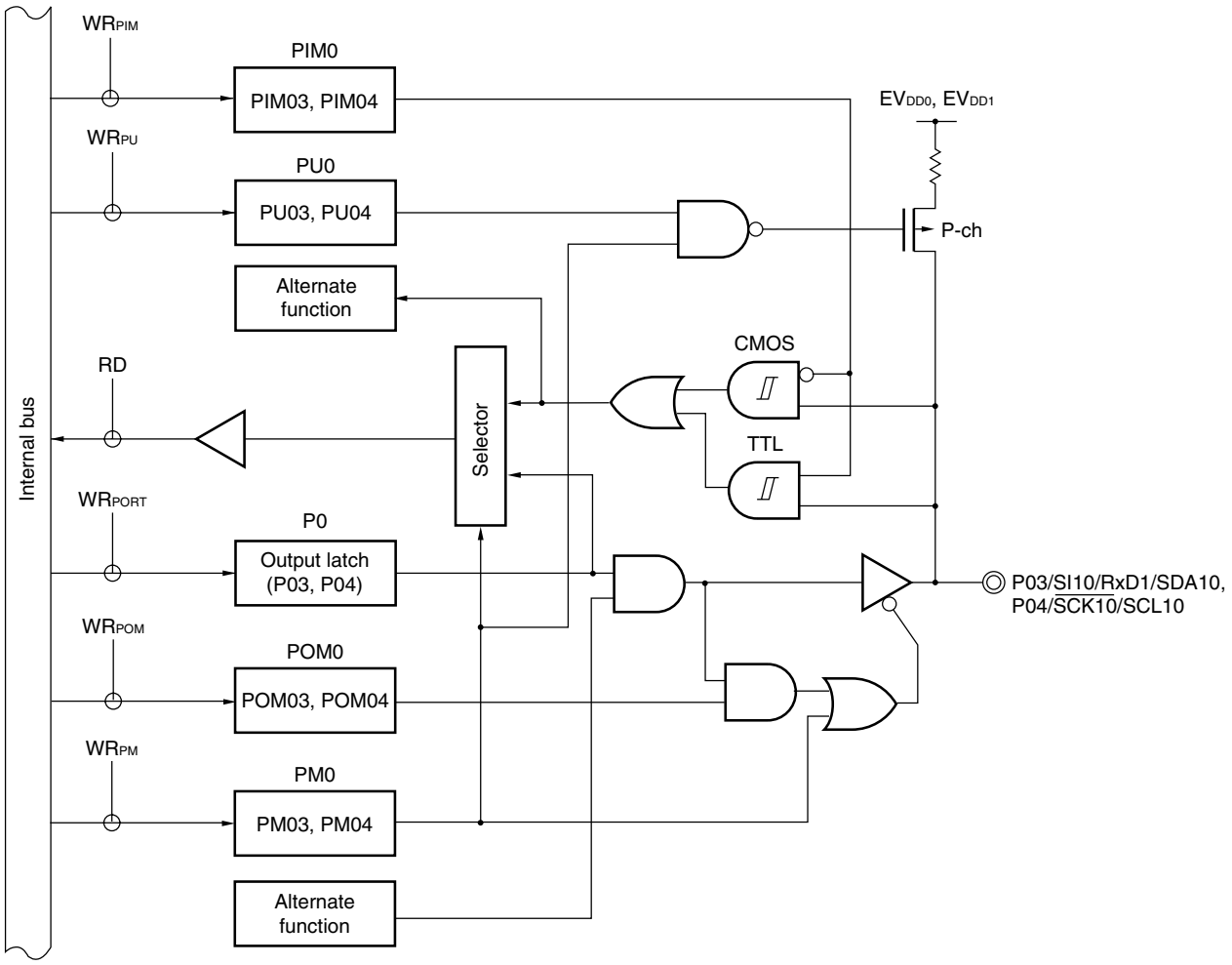
P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

Figure 6-3. Block Diagram of P02



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
POM0: Port output mode register 0
RD: Read signal
WR××: Write signal

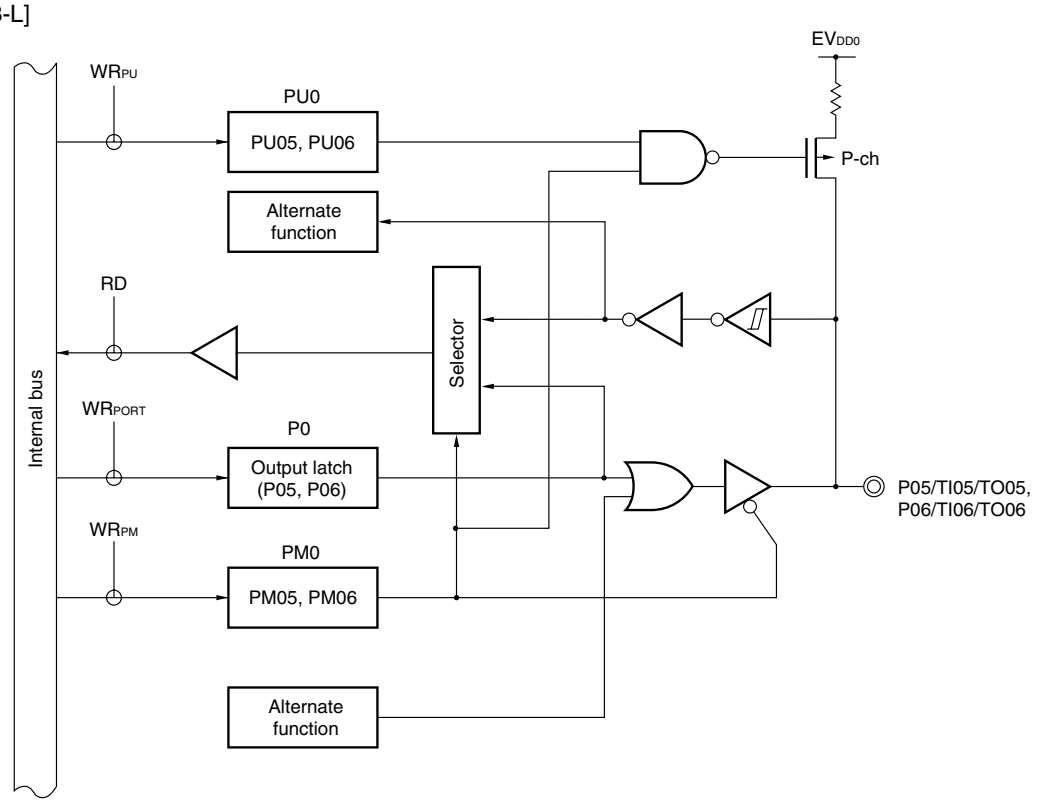
Figure 6-4. Block Diagram of P03 and P04



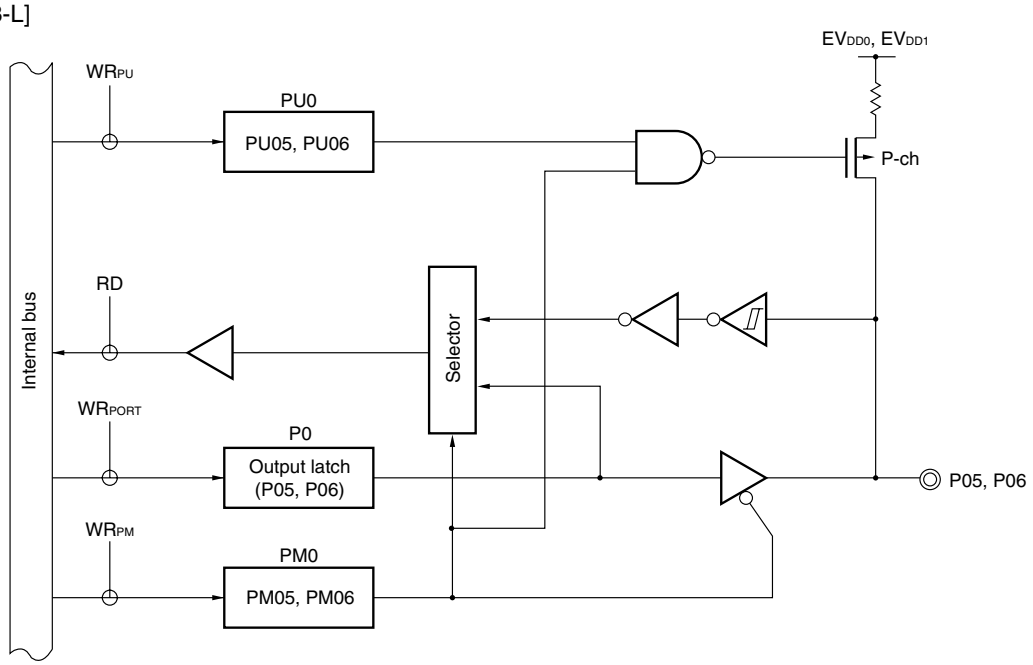
P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
PIM0: Port input mode register 0
POM0: Port output mode register 0
RD: Read signal
WR××: Write signal

Figure 6-5. Block Diagram of P05 and P06

[78K0R/KF3-L]



[78K0R/KG3-L]



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

6.2.2 Port 1

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P10/$\overline{\text{SCK00}}$	√	√
P11/SI00/RxD0	√	√
P12/SO00/TxD0	√	√
P13/TxD3	√	√
P14/RxD3	√	√
P15/RTCDIV/RTCCL	√	√
P16/TI01/TO01/INTP5	√	√
P17/TI02/TO02	√	√

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P17 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

Input to the P10 and P11 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 1 (PIM1).

Output from the P10 and P12 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 1 (POM1).

This port can also be used for external interrupt request input, serial interface data I/O, clock I/O, timer I/O, and real-time counter clock output.

Reset signal generation sets port 1 to input mode.

Figures 6-6 to 6-12 show block diagrams of port 1.

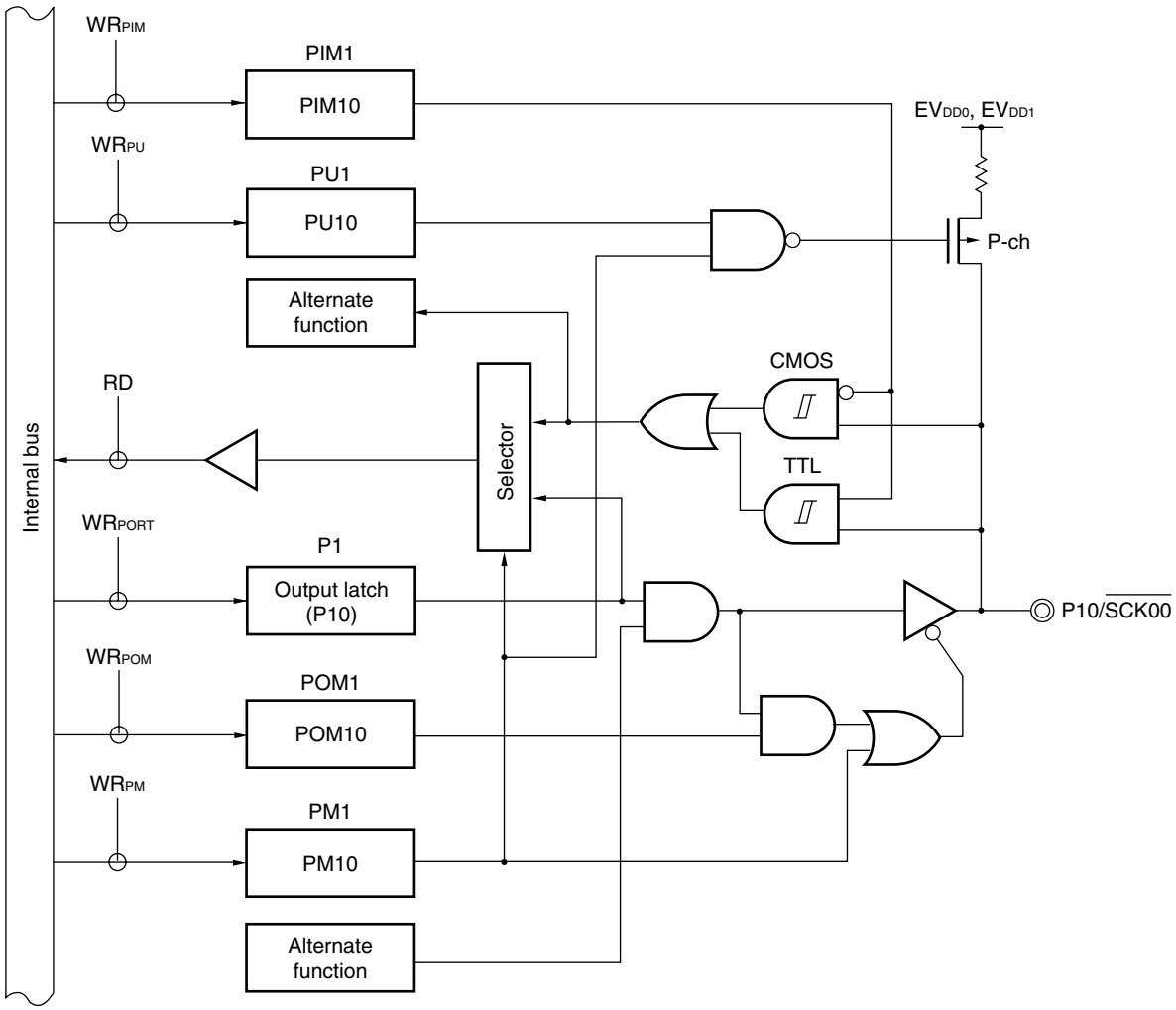
Cautions 1. To use P10/$\overline{\text{SCK00}}$, P11/SI00/RxD0, or P12/SO00/TxD0, P13/TxD3, P14/RxD3 as a general-purpose port, note the serial array unit setting. For details, refer to the following tables.

- **Table 14-9 Relationship Between Register Settings and Pins (Channel 0 of Unit 0: CSI00, UART0 Transmission)**
- **Table 14-10 Relationship Between Register Settings and Pins (Channel 1 of Unit 0: CSI01, UART0 Reception)**
- **Table 14-15 Relationship Between Register Settings and Pins (Channel 2 of Unit 1: UART3 Transmission)**
- **Table 14-16 Relationship Between Register Settings and Pins (Channel 3 of Unit 1: UART3 Reception)**

2. To use P16/TI01/TO01/INTP5 or P17/TI02/TO02 as a general-purpose port, set bits 1 and 2 (TO01, TO02) of timer output register 0 (TO0) and bits 1 and 2 (TOE01, TOE02) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

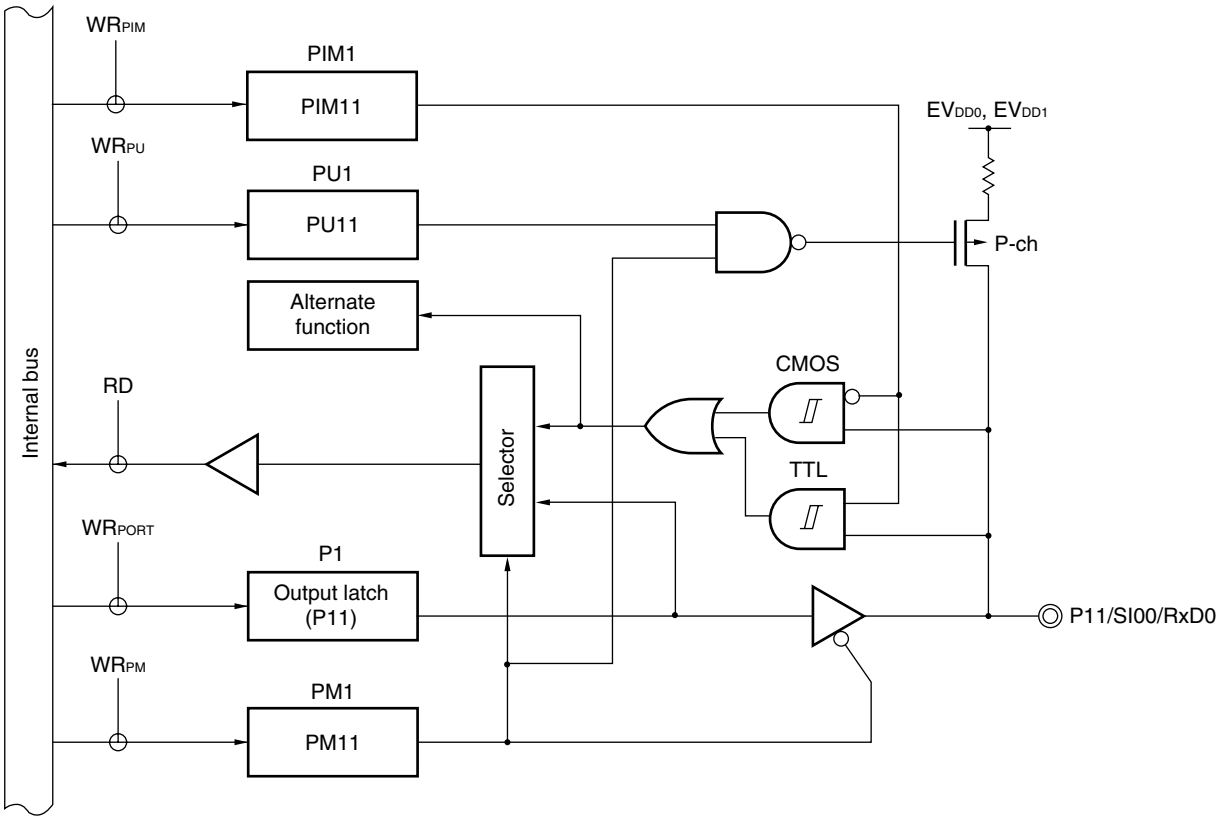
3. To use P15/RTCDIV/RTCCL as a general-purpose port, set bit 4 (RCLOE0) of real-time counter control register 0 (RTCC0) and bit 6 (RCLOE2) of real-time counter control register 2 (RTCC2) to "0", which is the same as their default status settings.

Figure 6-6. Block Diagram of P10



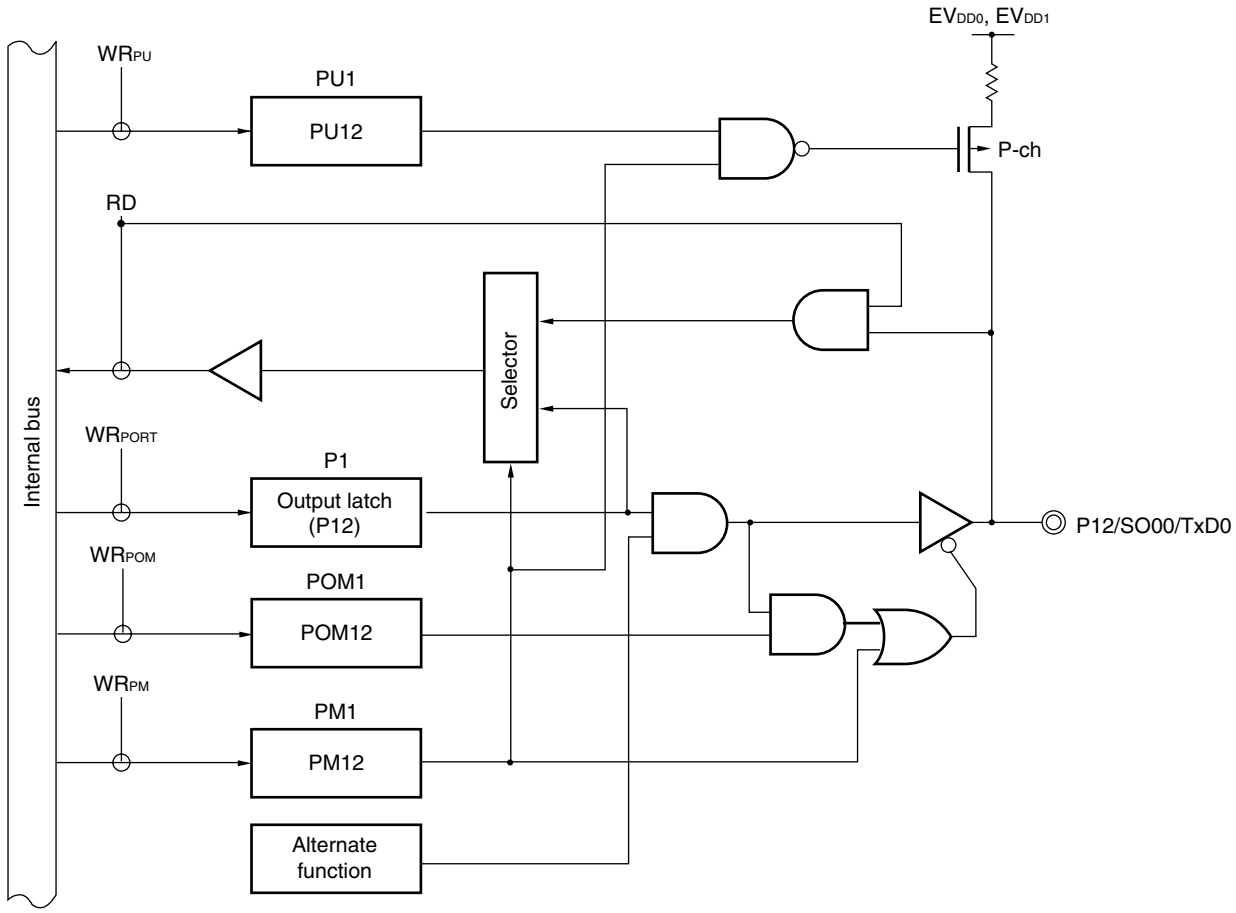
P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
PIM1: Port input mode register 1
POM1: Port output mode register 1
RD: Read signal
WR××: Write signal

Figure 6-7. Block Diagram of P11



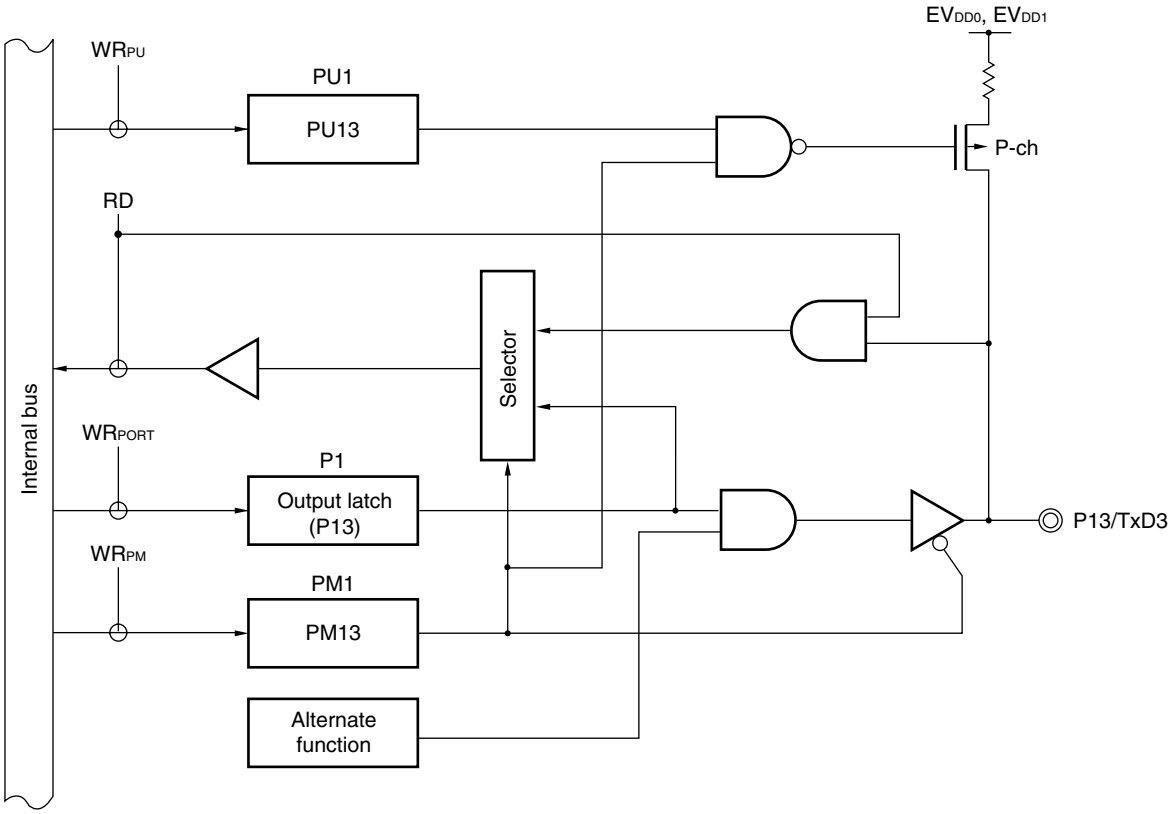
P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
PIM1: Port input mode register 1
RD: Read signal
WR××: Write signal

Figure 6-8. Block Diagram of P12



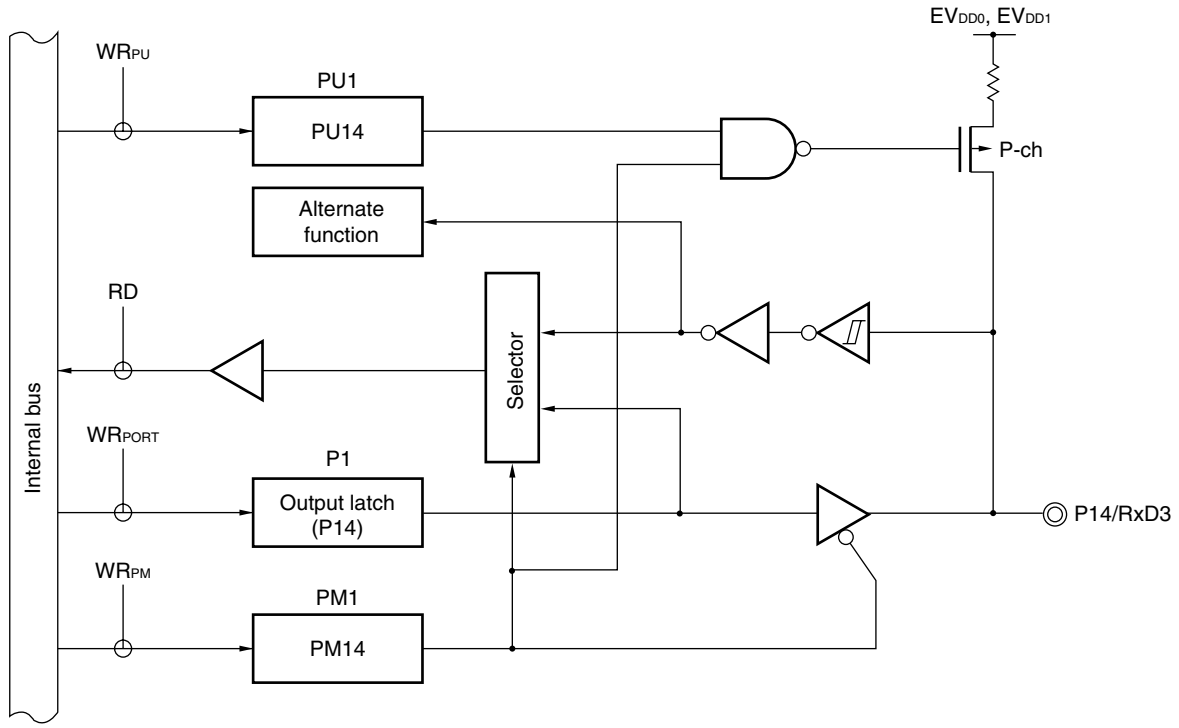
P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
POM1: Port output mode register 1
RD: Read signal
WR××: Write signal

Figure 6-9. Block Diagram of P13



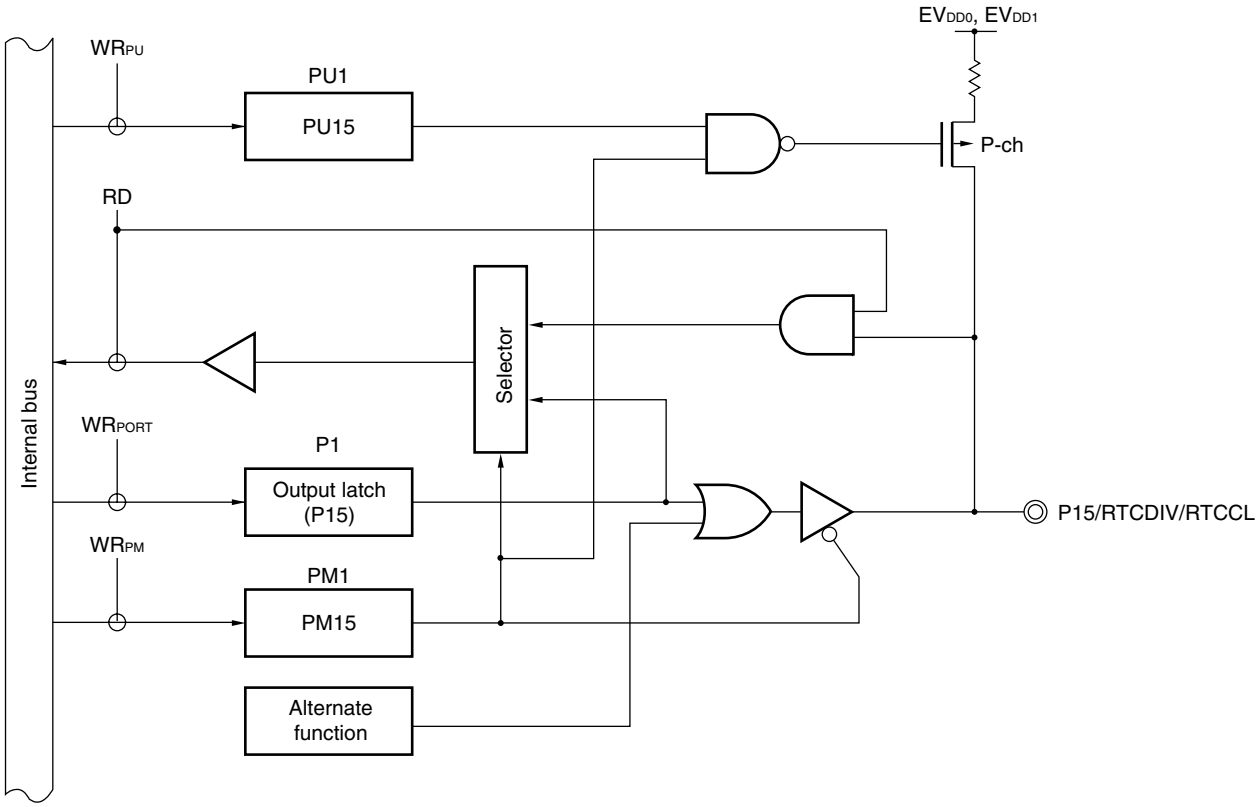
P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 6-10. Block Diagram of P14



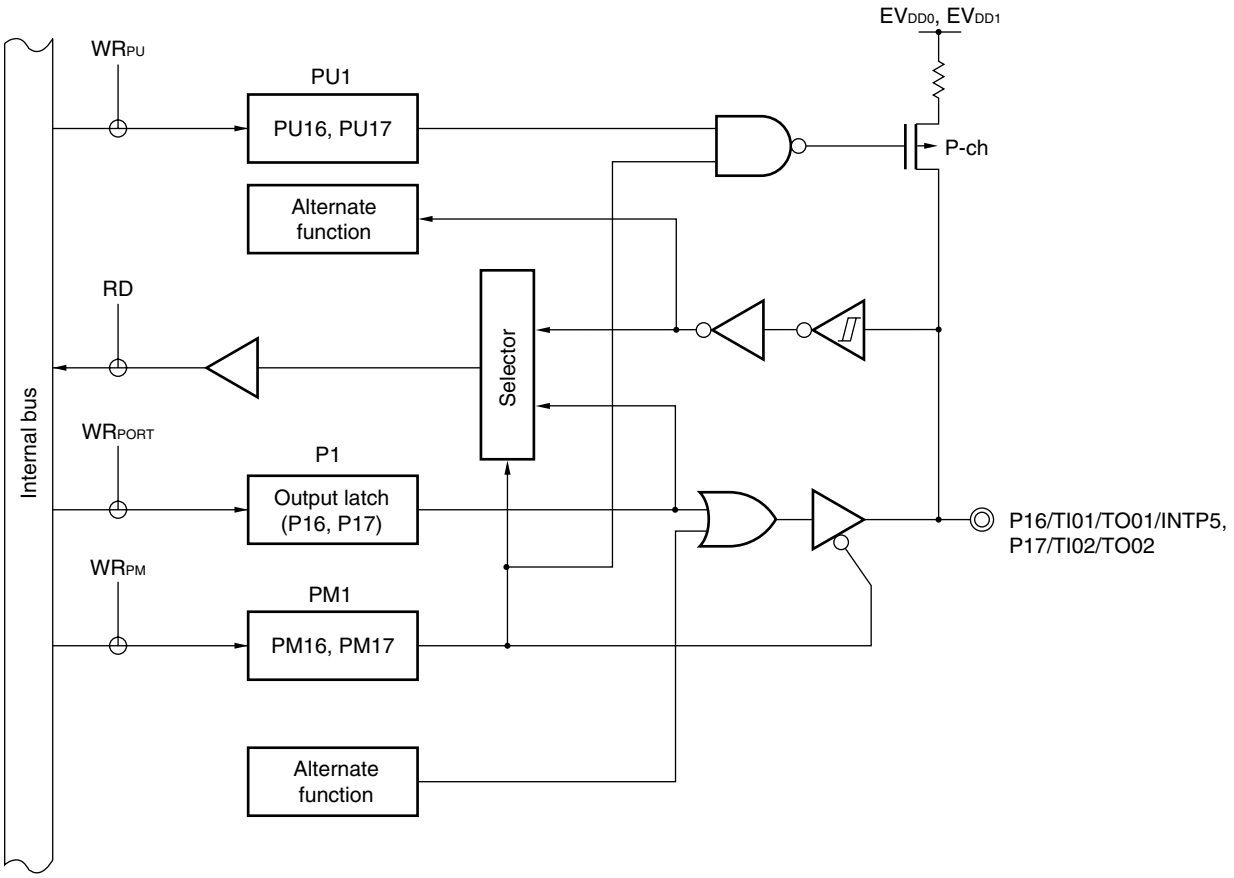
P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 6-11. Block Diagram of P15



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 6-12. Block Diagram of P16 and P17



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

6.2.3 Port 2

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P20/ANI0	√	√
P21/ANI1	√	√
P22/ANI2	√	√
P23/ANI3	√	√
P24/ANI4	√	√
P25/ANI5	√	√
P26/ANI6	√	√
P27/ANI7	√	√

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2).

This port can also be used for A/D converter analog input.

To use P20/ANI0 to P27/ANI7 as digital input pins, set them in the digital I/O mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM2 register. Use these pins starting from the lower bit.

To use P20/ANI0 to P27/ANI7 as digital output pins, set them in the digital I/O mode by using the ADPC register and in the output mode by using the PM2 register.

To use P20/ANI0 to P27/ANI7 as analog input pins, set them in the analog input mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM2 register. Use these pins starting from the upper bit.

Table 6-5. Setting Functions of P20/ANI0 to P27/ANI7 Pins

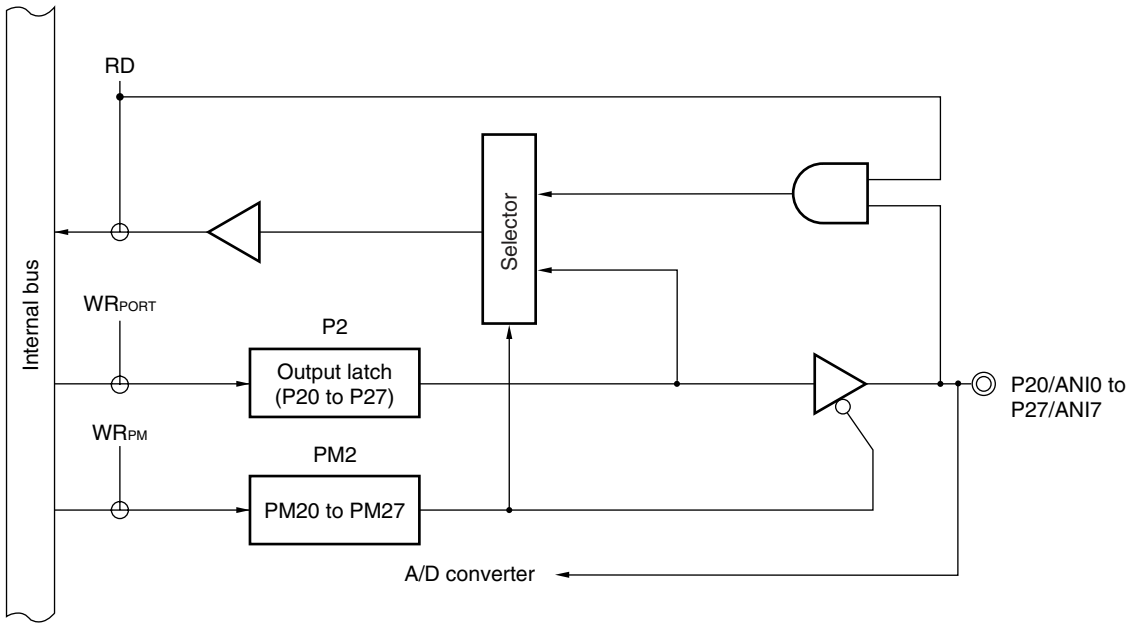
ADPC Register	PM2 Register	ADS Register	P20/ANI0 to P27/ANI7 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

All P20/ANI0 to P27/ANI7 are set in the digital input mode when the reset signal is generated.

Figure 6-13 shows a block diagram of port 2.

Caution See 3.2.16 AV_{REF}, AV_{SS}, V_{DD}, EV_{DD0}, EV_{DD1}, V_{SS}, EV_{SS0}, EV_{SS1} for the voltage to be applied to the AV_{REF} pin when using port 2 as a digital I/O.

Figure 6-13. Block Diagram of P20 to P27



P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

6.2.4 Port 3

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P30/RTC1HZ/INTP3	√	√
P31/TI03/TO03/INTP4	√	√

Port 3 is an I/O port with an output latch. Port 3 can be set to the input mode or output mode in 1-bit units using port mode register 3 (PM3). When the P30 and P31 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 3 (PU3).

This port can also be used for external interrupt request input, timer I/O, and real-time counter correction clock output.

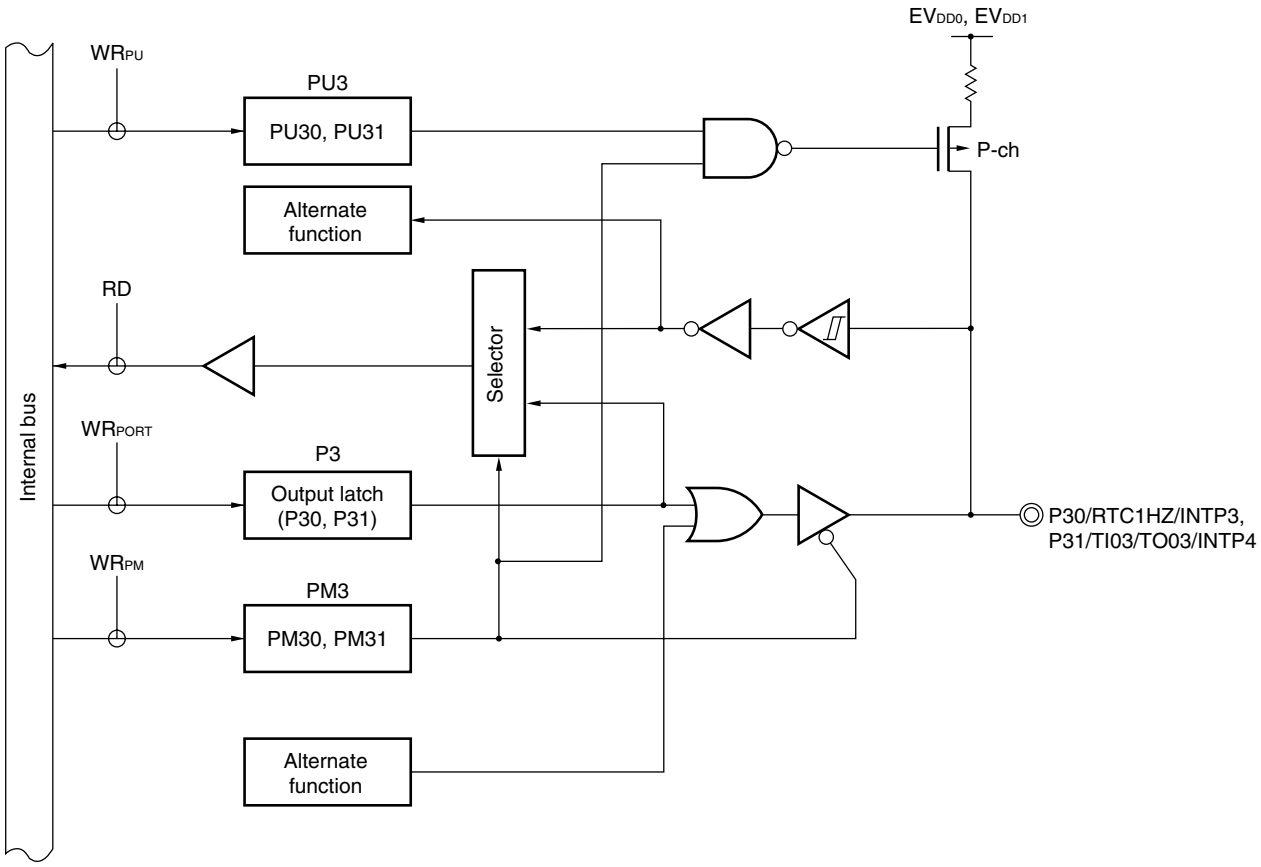
Reset signal generation sets port 3 to input mode.

Figure 6-14 shows block a diagram of port 3.

Cautions 1. To use P31/TI03/TO03/INTP4 as a general-purpose port, set bit 3 (TO03) of timer output register 0 (TO0) and bit 3 (TOE03) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

2. To use P30/RTC1HZ/INTP3 as a general-purpose port, set bit 5 (RCLOE1) of real-time counter control register 0 (RTCC0) to "0", which is the same as its default status setting.

Figure 6-14. Block Diagram of P30 and P31



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

6.2.5 Port 4

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P40/TOOL0	√	√
P41/TOOL1	√	√
P42/TI04/TO04	√	√
P43/$\overline{\text{SCK01}}$	√	√
P44/SI01	√	√
P45/SO01	√	√
P46/INTP1/TI05/TO05	P46 Note 1	√
P47/INTP2	P47 Note 2	√

Notes 1. INTP1 and TI05/TO05 are shared with P50 and P05, respectively, in the 78K0R/KF3-L.

2. INTP2 is shared with P51, in the 78K0R/KF3-L.

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P47 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 4 (PU4)[Note].

This port can also be used for external interrupt request input, serial interface data I/O, clock I/O, flash memory programmer/debugger data I/O, clock output, and timer I/O.

Reset signal generation sets port 4 to input mode.

Figures 6-15 to 6-22 show block diagrams of port 4.

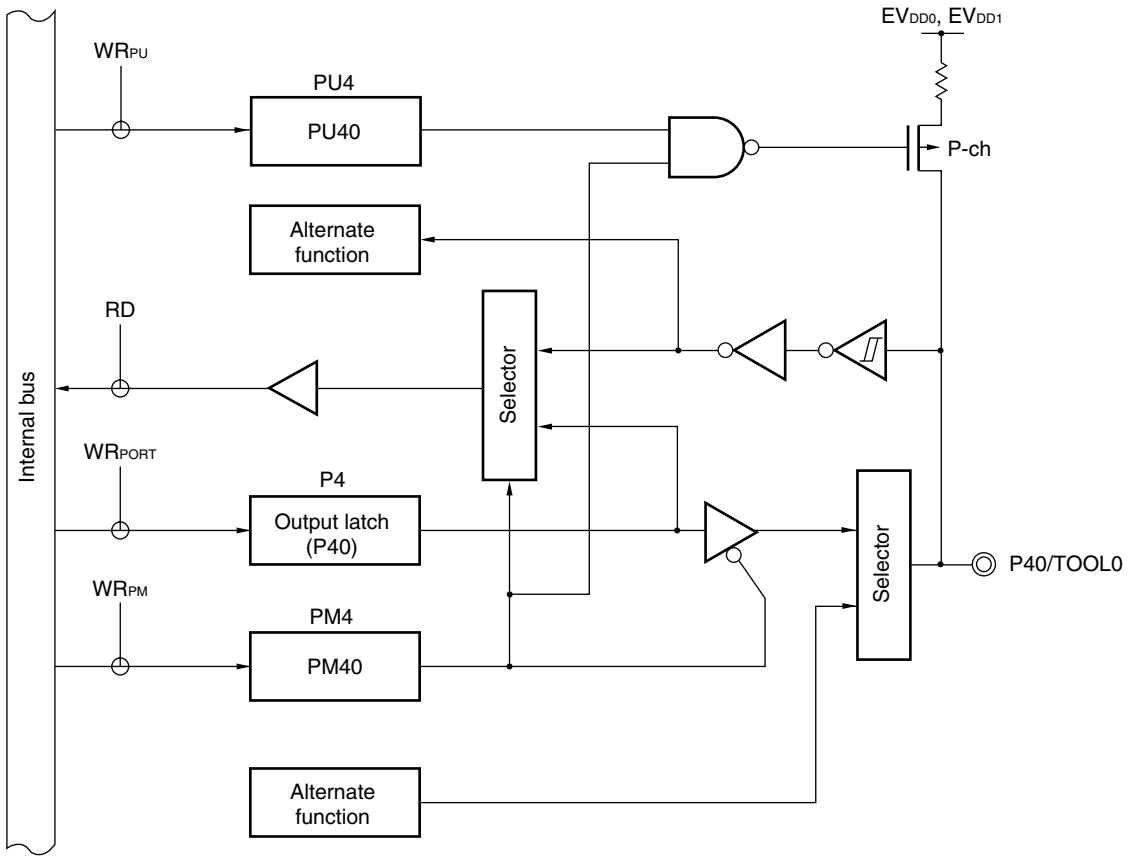
Note When a tool is connected, the P40 and P41 pins cannot be connected to a pull-up resistor.

Cautions 1. When a tool is connected, the P40 pin cannot be used as a port pin.
When the on-chip debug function is used, the P41 pin can be used as follows by the mode setting on the debugger.
1-line mode: can be used as a port (P41).
2-line mode: used as a TOOL1 pin and cannot be used as a port (P41).

2. To use P43/$\overline{\text{SCK01}}$, P44/SI01, or P45/SO01 as a general-purpose port, note the serial array unit 0 setting. For details, refer to Table 14-10 Relationship Between Register Settings and Pins (Channel 1 of Unit 0: CSI01, UART0 reception).

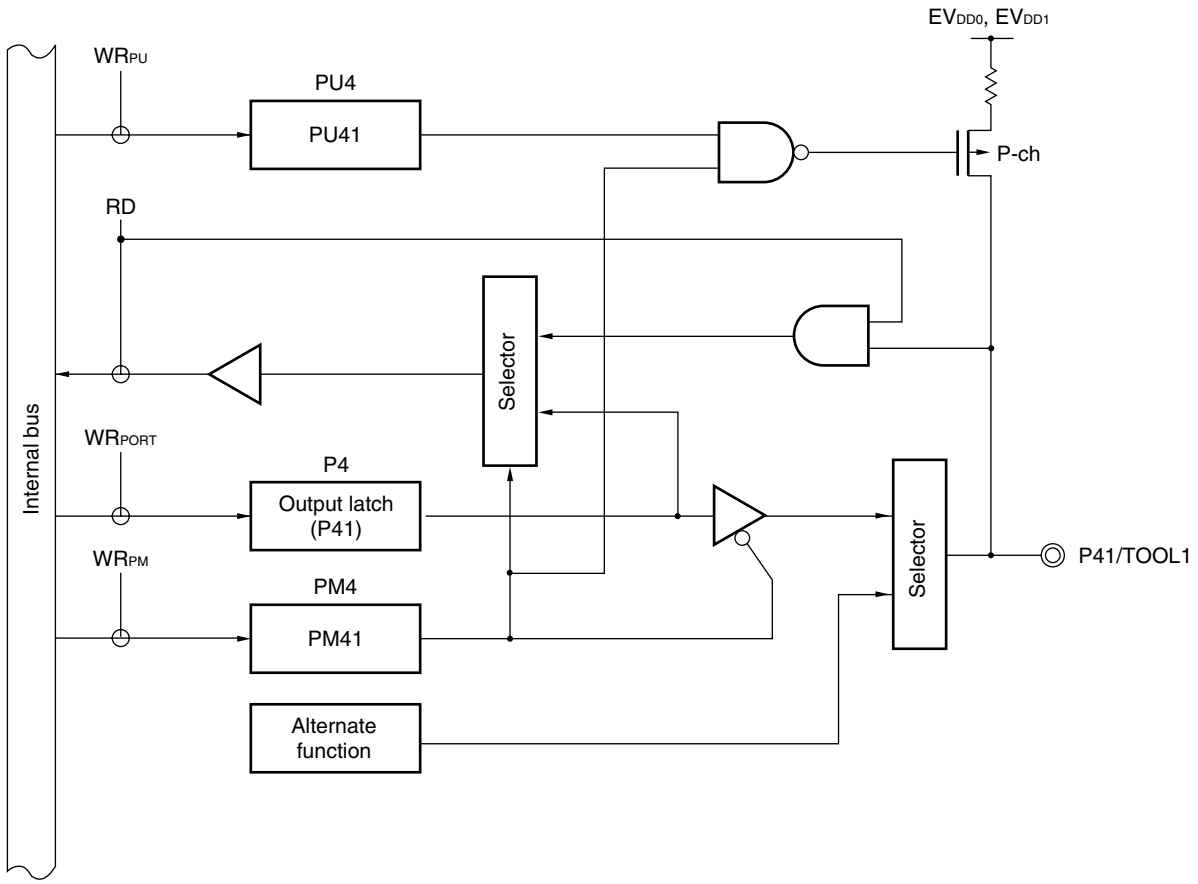
3. To use P42/TI04/TO04 or P46/INTP1/TI05/TO05 as a general-purpose port, set bits 4 and 5 (TO04, TO05) of timer output register 0 (TO0) and bits 4 and 5 (TOE04, TOE05) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

Figure 6-15. Block Diagram of P40



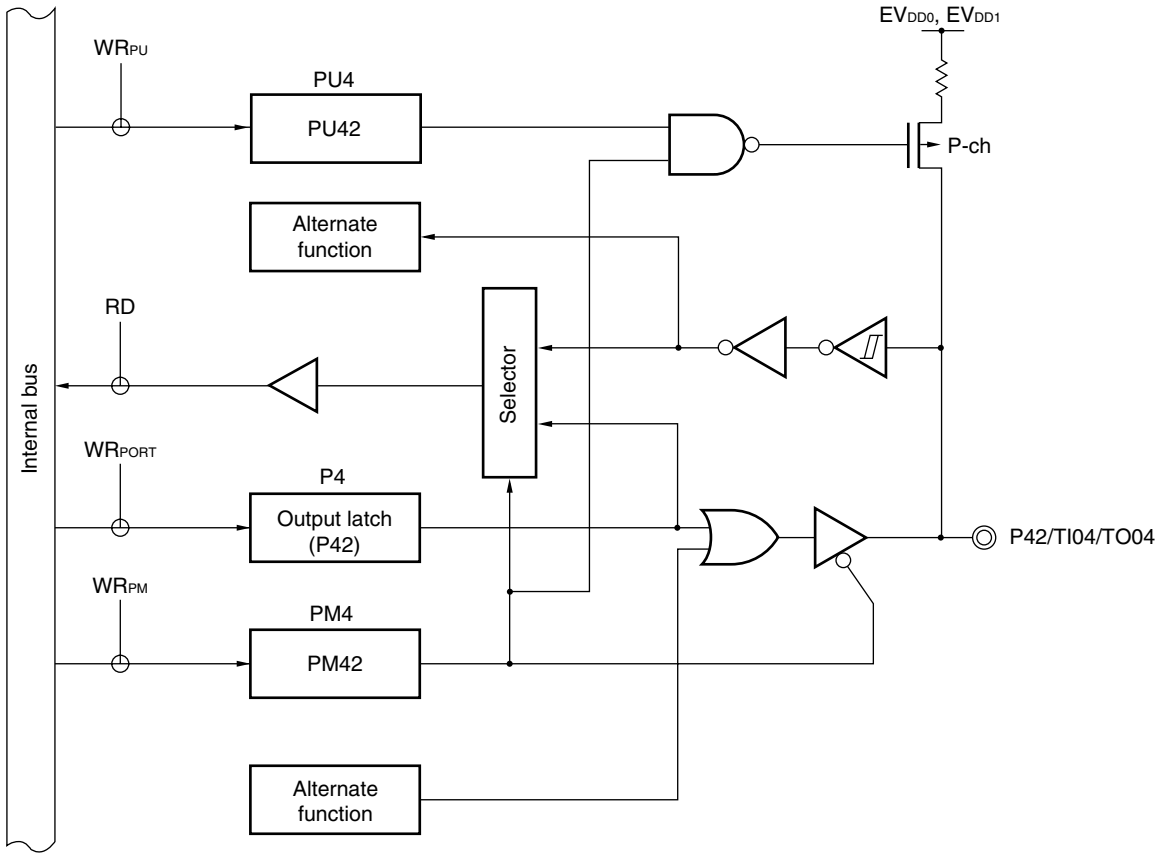
P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-16. Block Diagram of P41



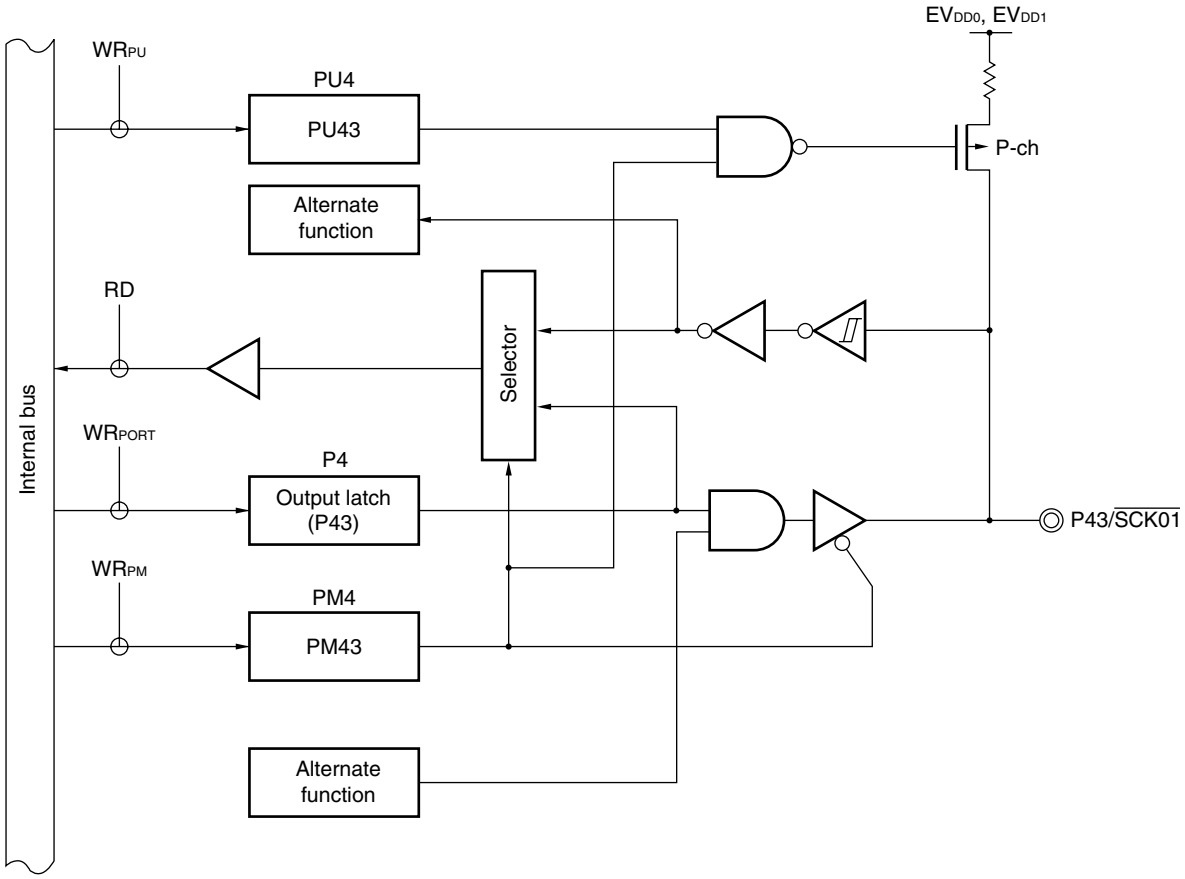
P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-17. Block Diagram of P42



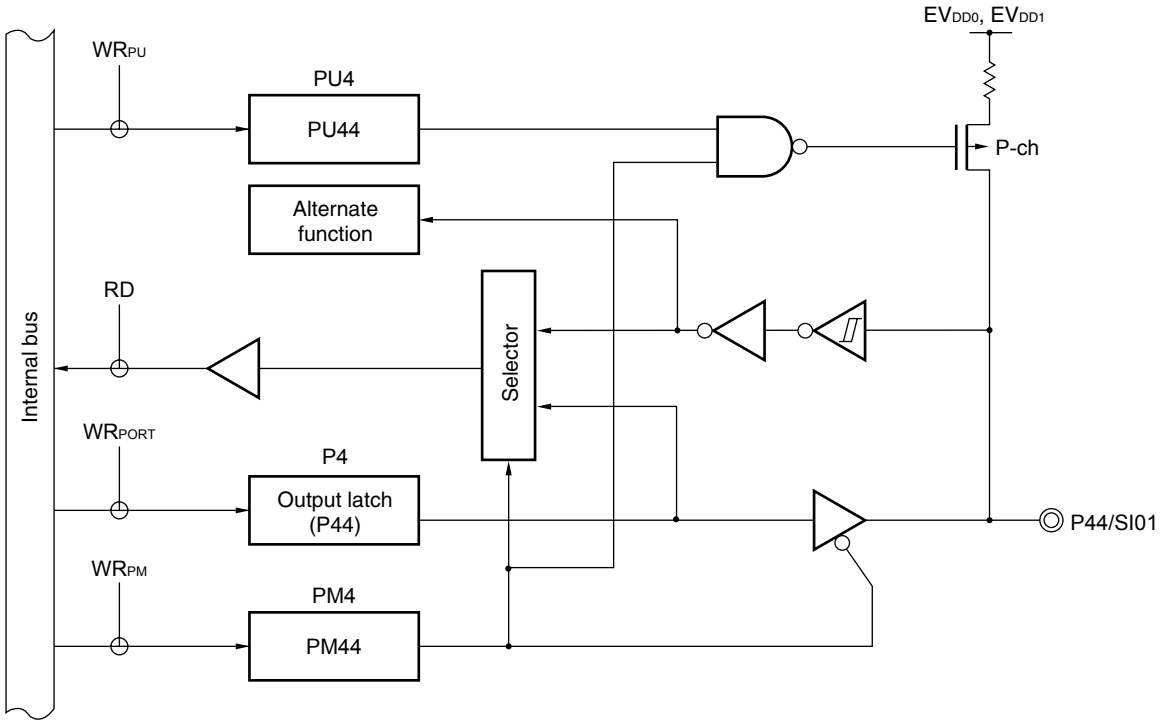
P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-18. Block Diagram of P43



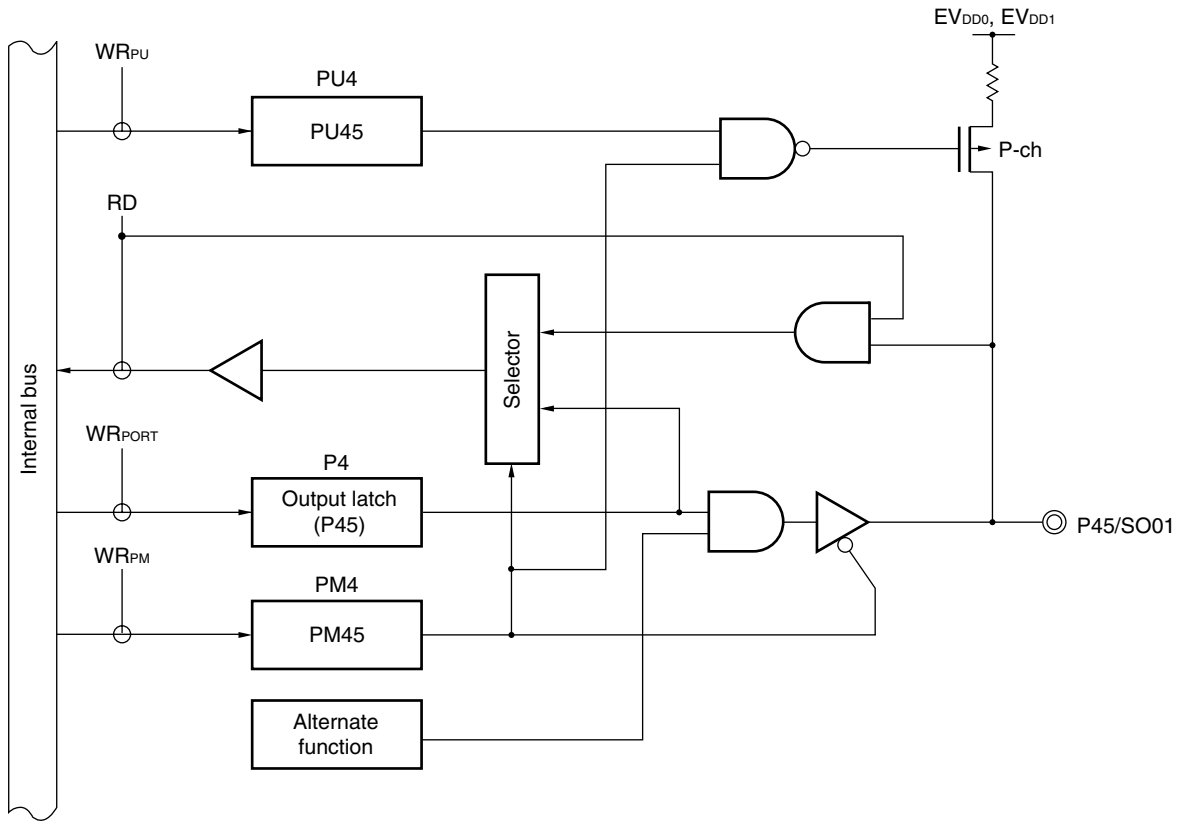
P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-19. Block Diagram of P44



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

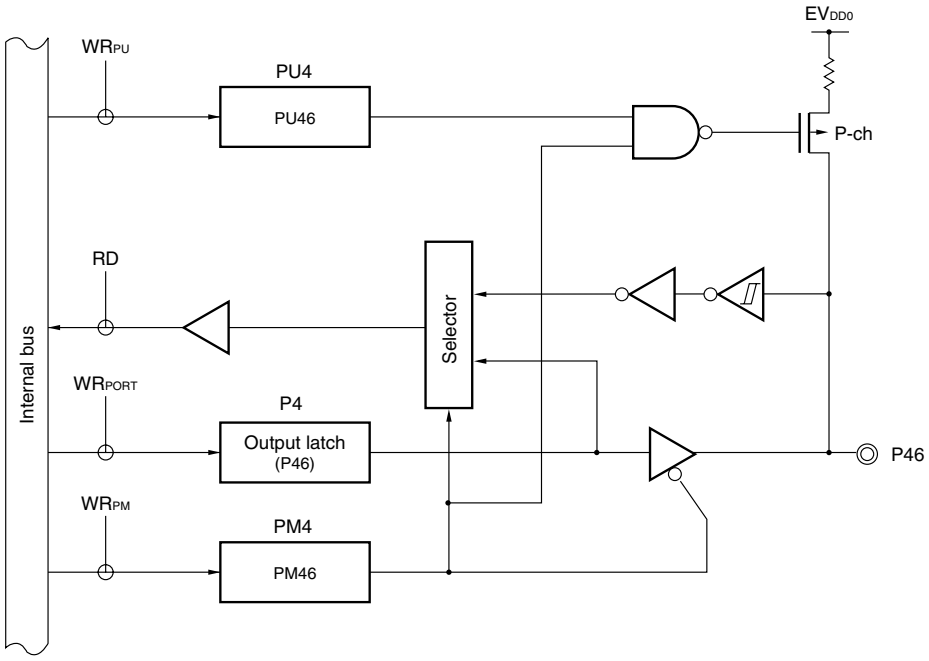
Figure 6-20. Block Diagram of P45



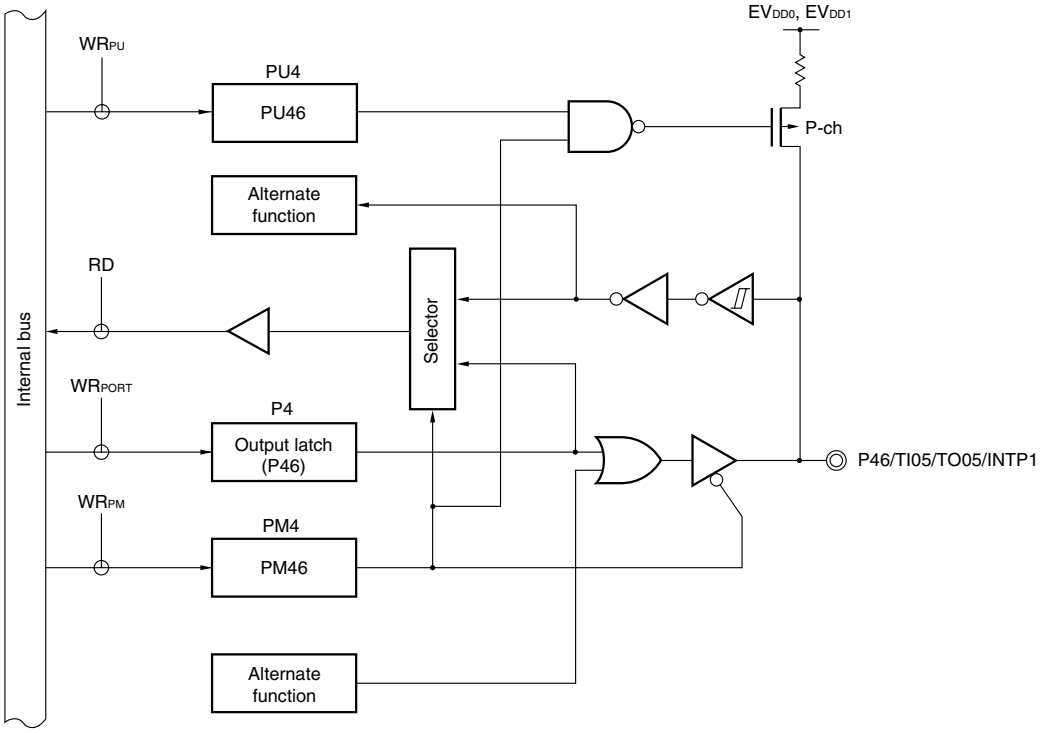
P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-21. Block Diagram of P46

[78K0R/KF3-L]



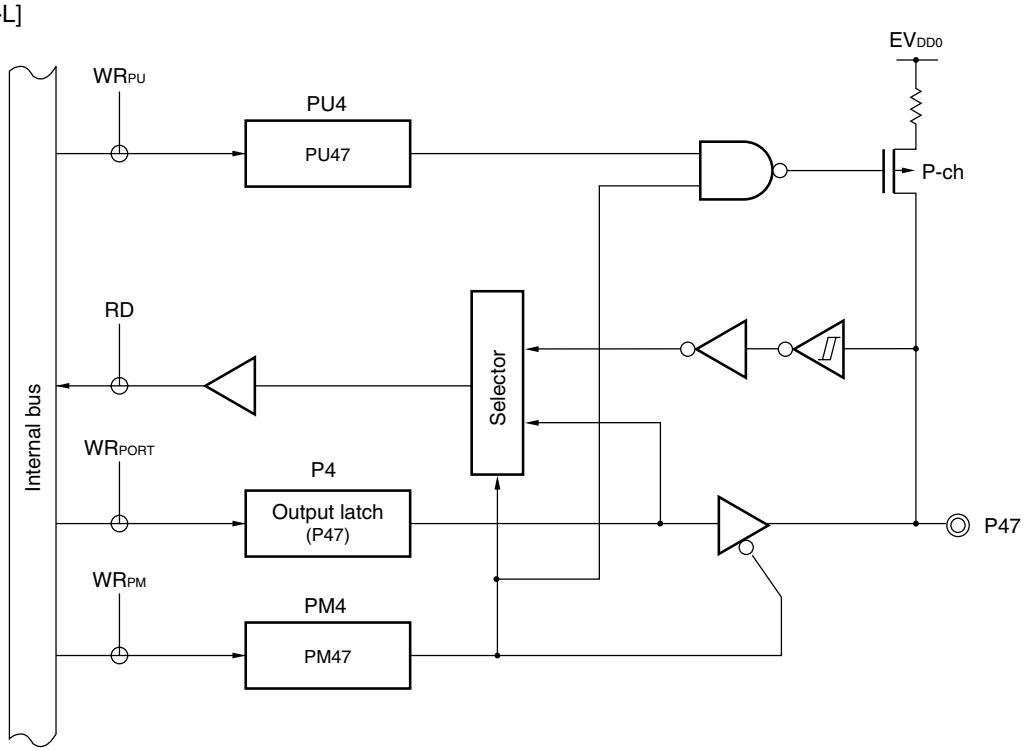
[78K0R/KG3-L]



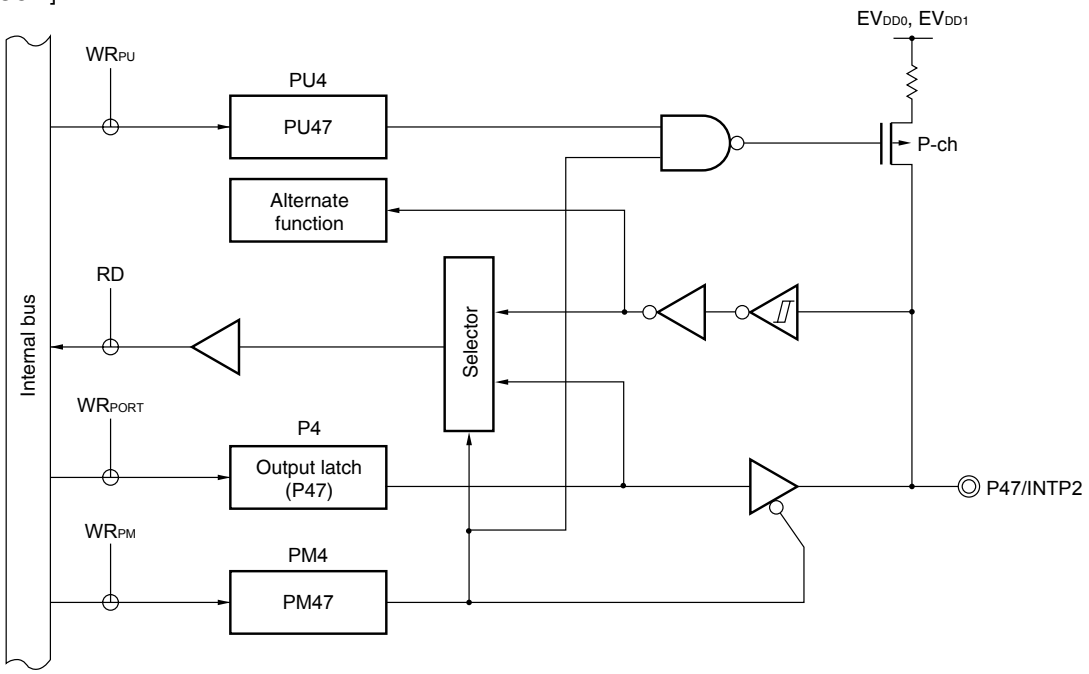
P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-22. Block Diagram of P47

[78K0R/KF3-L]



[78K0R/KG3-L]



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

6.2.6 Port 5 (μPD78F1010, 78F1011, 78F1012, 78F1013, 78F1014)

	78K0R/KF3-L (μPD78F101y: y = 0 to 2)	78K0R/KG3-L (μPD78F101y: y = 3, 4)
P50/INTP1	√	P50 Note
P51/INTP2	√	P51 Note
P52/TO00	√	P52 Note
P53/TI00	√	P53 Note
P54/TI07/TO07	√	P54 Note
P55/PCLBUZ1/INTP7	√	P55 Note
P56	–	√
P57	–	√

Note The following pins are shared in the 78K0R/KG3-L.

- P46/INTP1
- P47/INTP2
- P01/TO00
- P00/TI00
- P145/TI07/TO07
- P141/PCLBUZ1/INTP7

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units using port mode register 5 (PM5). When the P50 to P57 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

This port can also be used for external interrupt request input, timer I/O, and clock/buzzer output.

Reset signal generation sets port 5 to input mode.

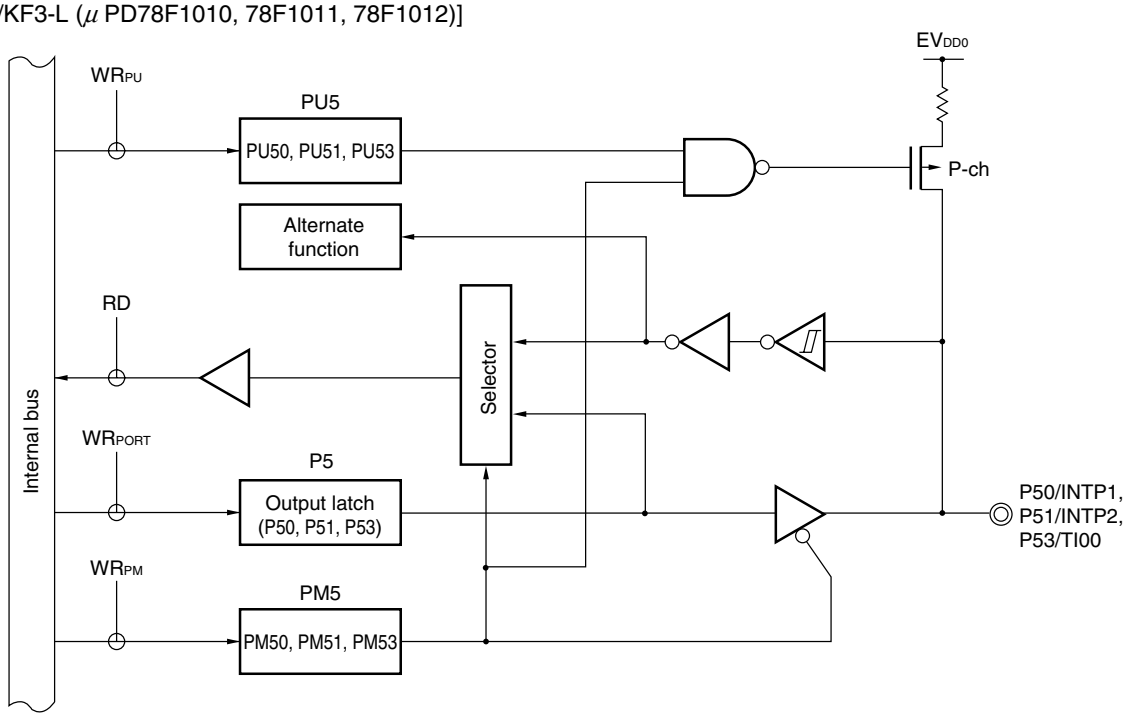
Figures 6-23 to 6-26 show block diagrams of port 5.

Cautions 1. To use P52/TO00 or P54/TI07/TO07 as a general-purpose port, set bits 0 and 7 (TO00, TO07) of timer output register 0 (TO0) and bits 0 and 7 (TOE00, TOE07) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

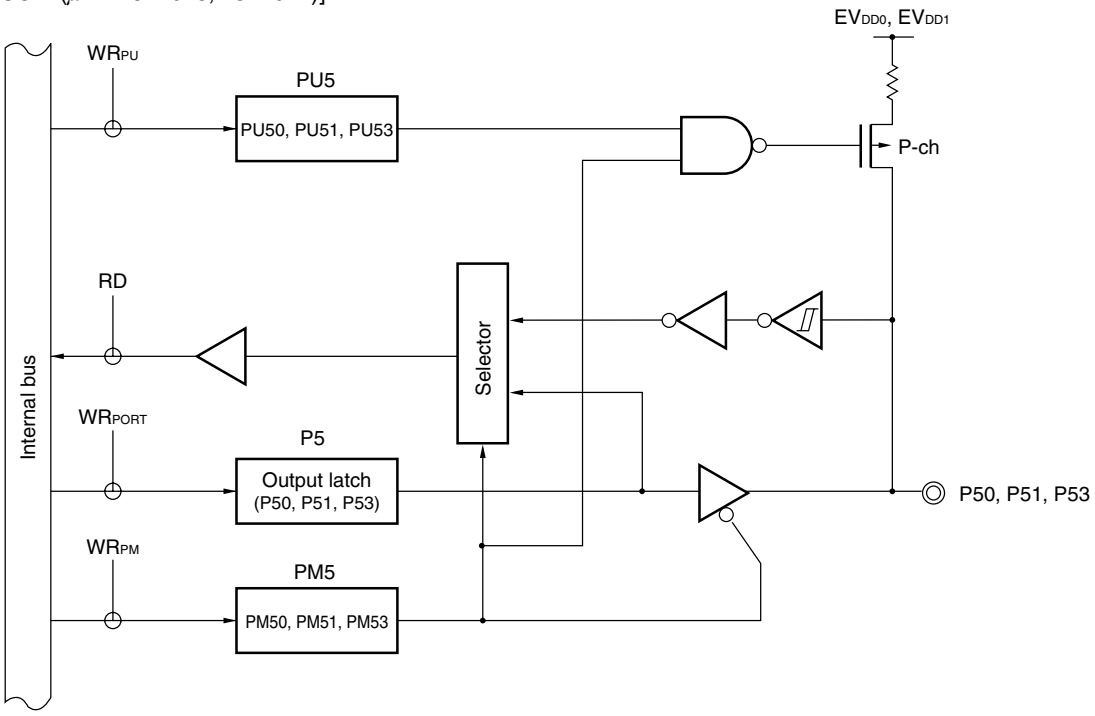
2. To use P55/PCLBUZ1/INTP7 as a general-purpose port, set bit 7 of clock output select register 1 (CKS1) to "0", which is the same as their default status settings.

Figure 6-23. Block Diagram of P50, P51, and P53

[78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012)]



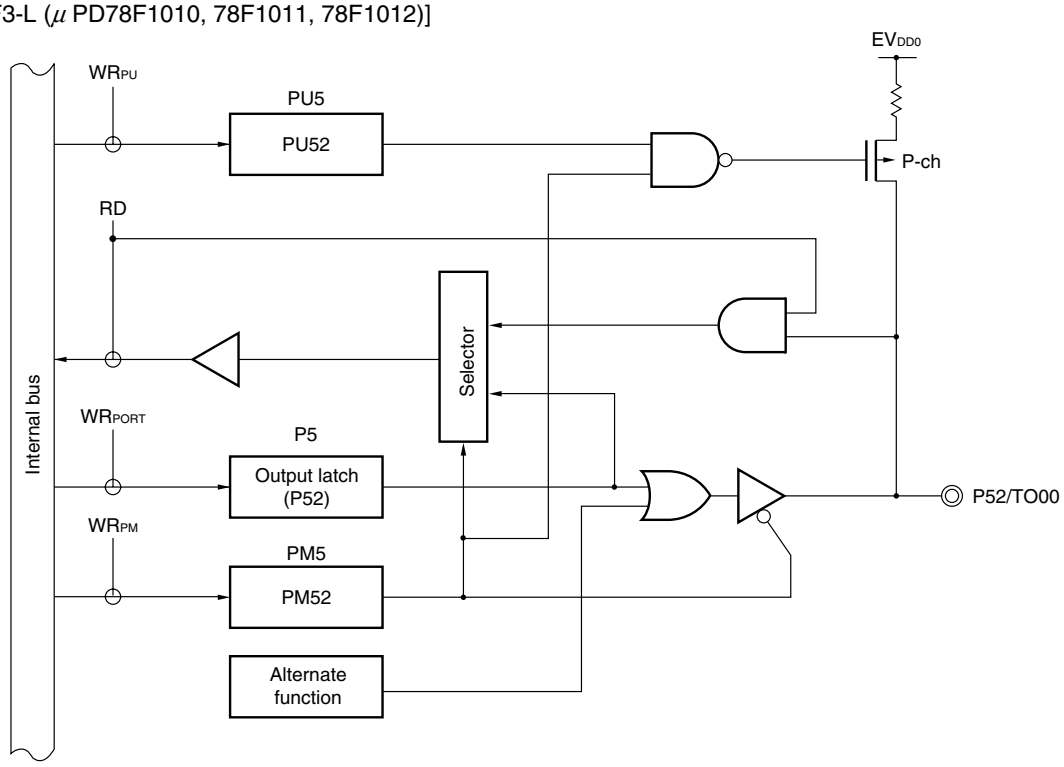
[78K0R/KG3-L (μPD78F1013, 78F1014)]



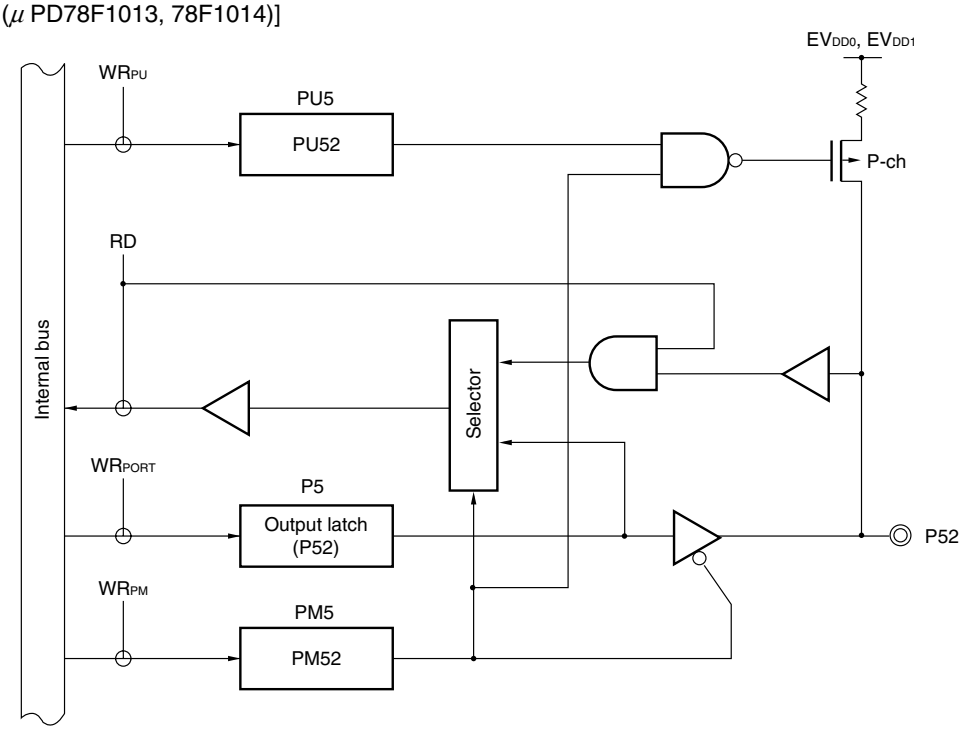
P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

Figure 6-24. Block Diagram of P52

[78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012)]



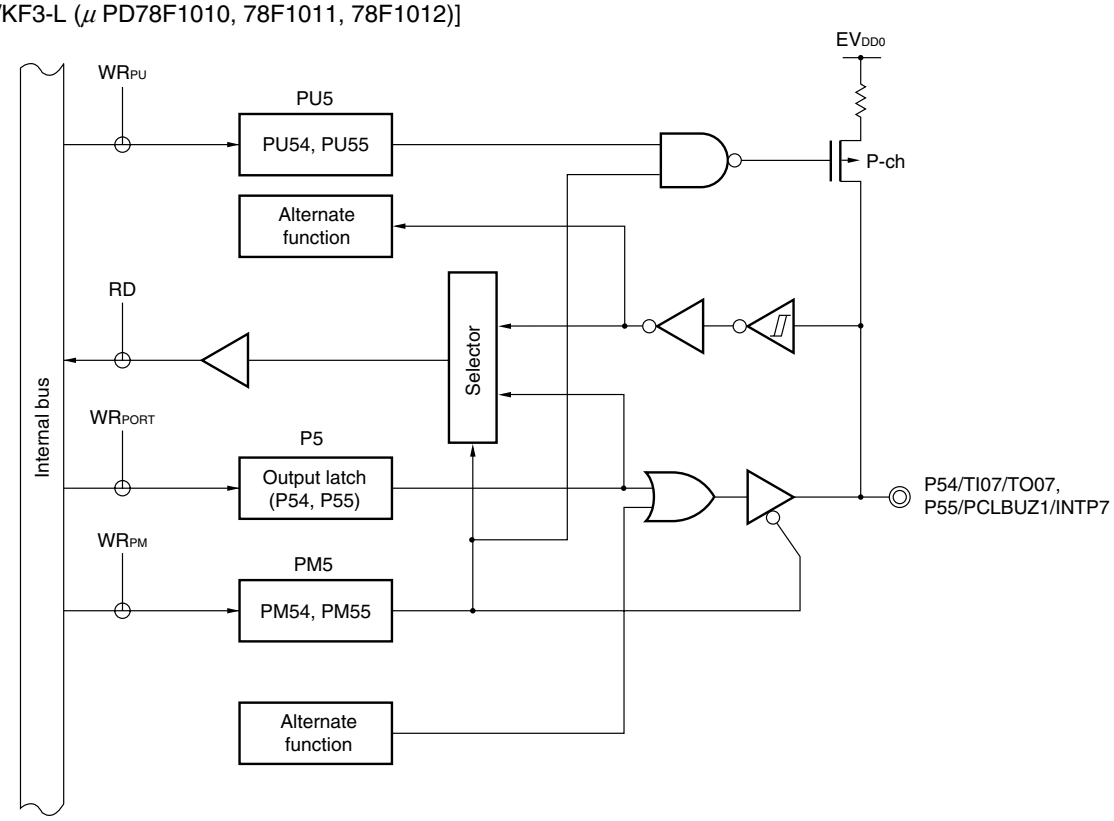
[78K0R/KG3-L (μPD78F1013, 78F1014)]



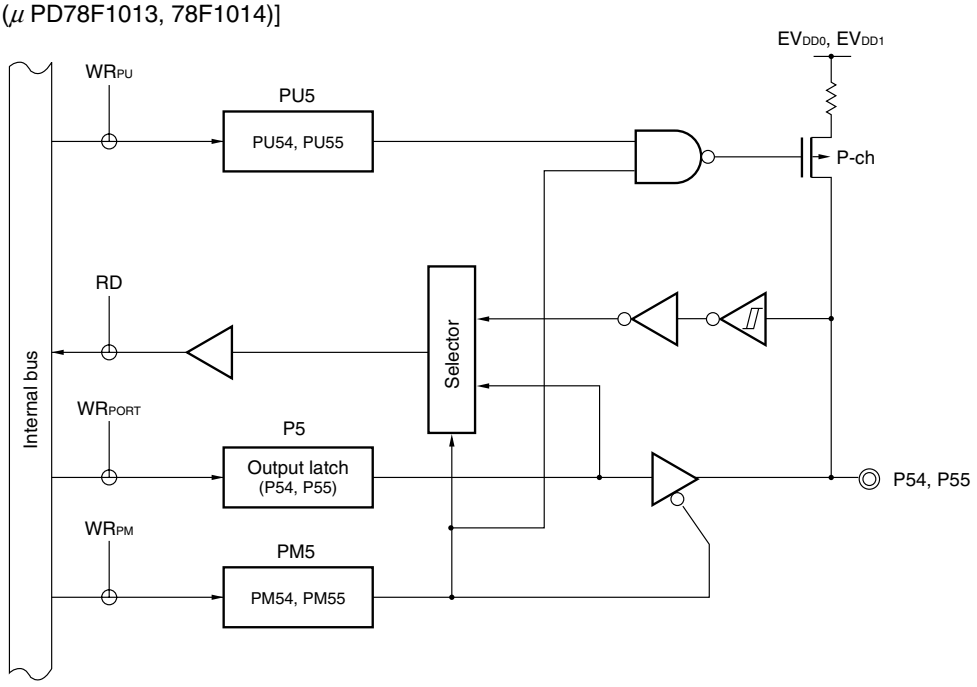
P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

Figure 6-25. Block Diagram of P54 and P55

[78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012)]

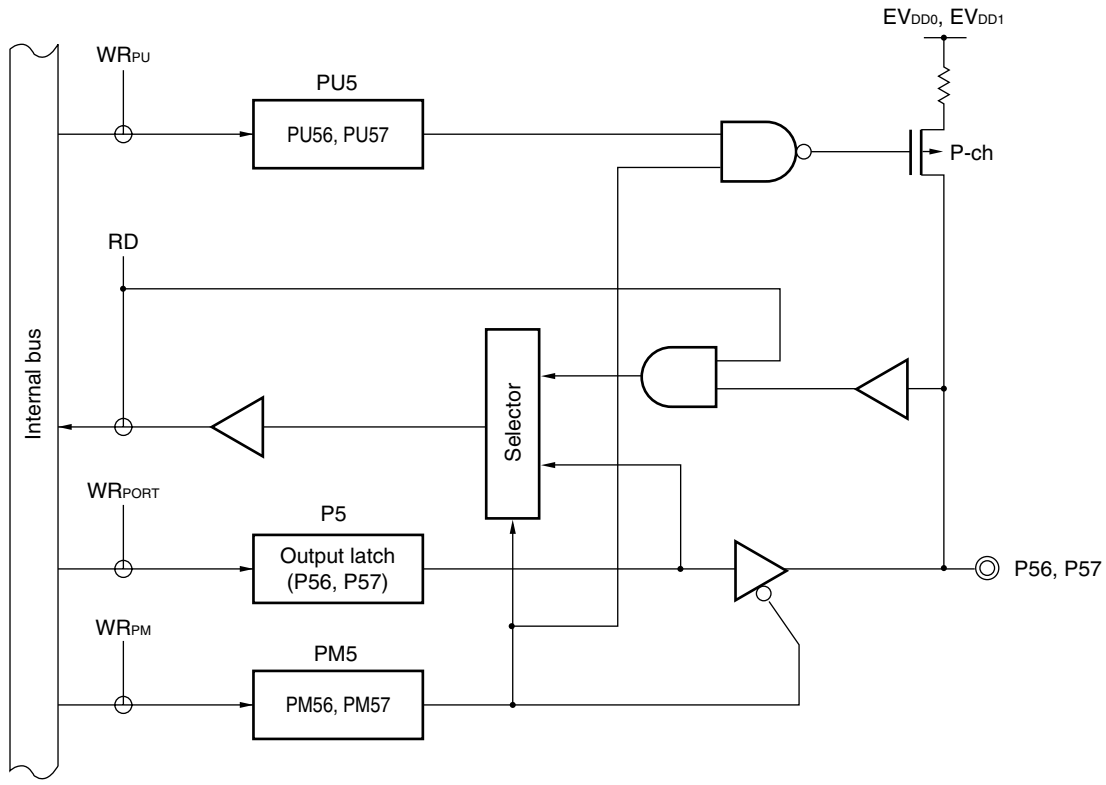


[78K0R/KG3-L (μPD78F1013, 78F1014)]



P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

Figure 6-26. Block Diagram of P56 and P57



P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

6.2.7 Port 5 (μPD78F1027, 78F1028, 78F1029, 78F1030)

	78K0R/KF3-L (μPD78F10xx: xx = 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 29, 30)
P50/$\overline{\text{SCK40}}$/INTP1	√	P50/$\overline{\text{SCK40}}$ Note
P51/SI40/RxD4/INTP2	√	P51/SI40/RxD4 Note
P52/SO40/TO00/TxD4	√	P52/SO40/TxD4 Note
P53/$\overline{\text{SCK41}}$/TI00	√	P53/$\overline{\text{SCK41}}$ Note
P54/SI41/TI07/TO07	√	P54/SI41 Note
P55/PCLBUZ1/SO41/ INTP7	√	P55/SO41 Note
P56	–	√
P57	–	√

Note The following pins are shared in the 78K0R/KG3-L.

- P46/INTP1
- P47/INTP2
- P01/TO00
- P00/TI00
- P145/TI07/TO07
- P141/PCLBUZ1/INTP7

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units using port mode register 5 (PM5). When the P50 to P57 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

This port can also be used for serial interface data I/O, clock I/O, external interrupt request input, timer I/O, and clock/buzzer output.

Reset signal generation sets port 5 to input mode.

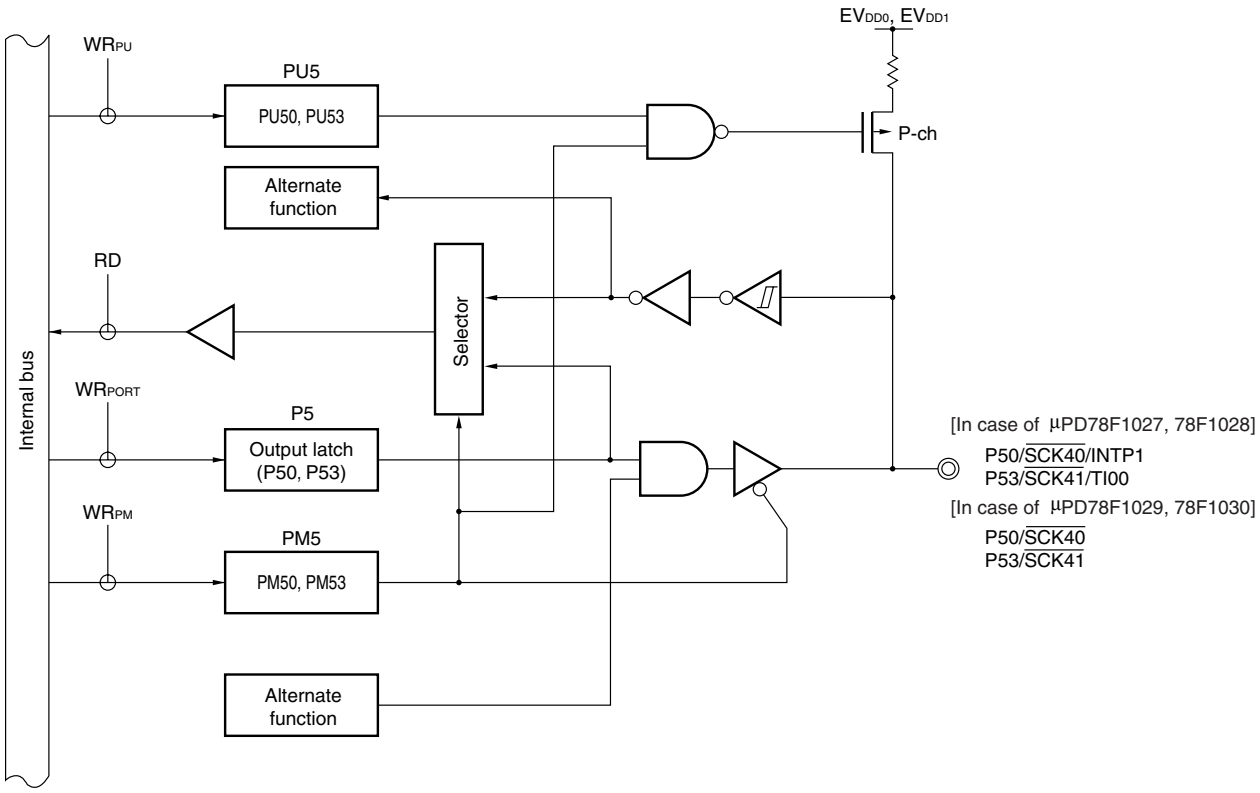
Figures 6-27 to 6-32 show block diagrams of port 5.

Cautions 1. To use P52/SO40/TO00/TxD4(P52/SO40/TO00, in case of KG3-L) or P54/SI41/TI07/TO07(P54/SI41, in case of KG3-L) as a general-purpose port, set bits 0 and 7 (TO00, TO07) of timer output register 0 (TO0) and bits 0 and 7 (TOE00, TOE07) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

2. To use P55/PCLBUZ1/SO41/INTP7(P55/SO41, in case of KG3-L) as a general-purpose port, set bit 7 of clock output select register 1 (CKS1) to "0", which is the same as their default status settings.

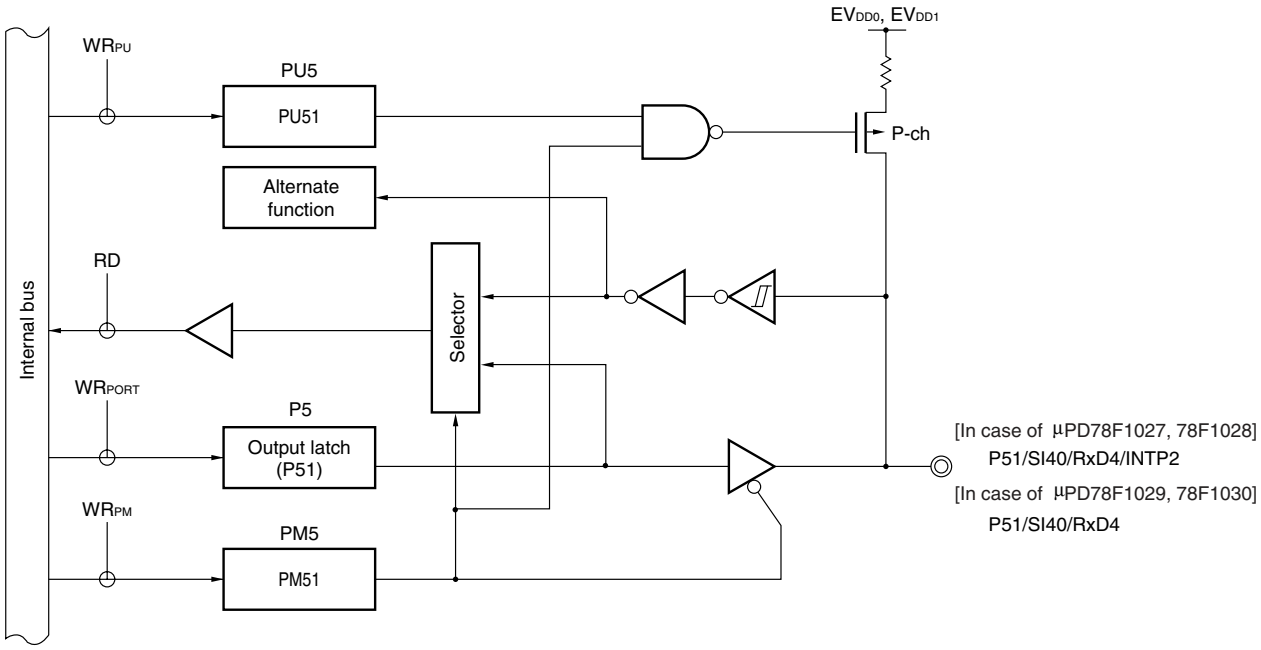
3. To use P50/$\overline{\text{SCK40}}$/INTP1, P51/SI40/RxD4/INTP2, P52/SO40/TO00/TxD4, P53/$\overline{\text{SCK41}}$/TI00, P54/SI41/TI07/TO07, and P55/PCLBUZ1/SO41/INTP7 as a general-purpose port, note the serial array unit setting. For details, refer to Table 1 Table 14-17. Relationship between register settings and pins (Channel 0 of unit 2: CSI40, UART4 transmission) (μPD78F1027, 78F1028, 78F1029, 78F1030 only) and Table 14-18. Relationship between register settings and pins (Channel 1 of unit 2: CSI41, UART4 reception) (μPD78F1027, 78F1028, 78F1029, 78F1030 only).

Figure 6-27. Block Diagram of P50 and P53



P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

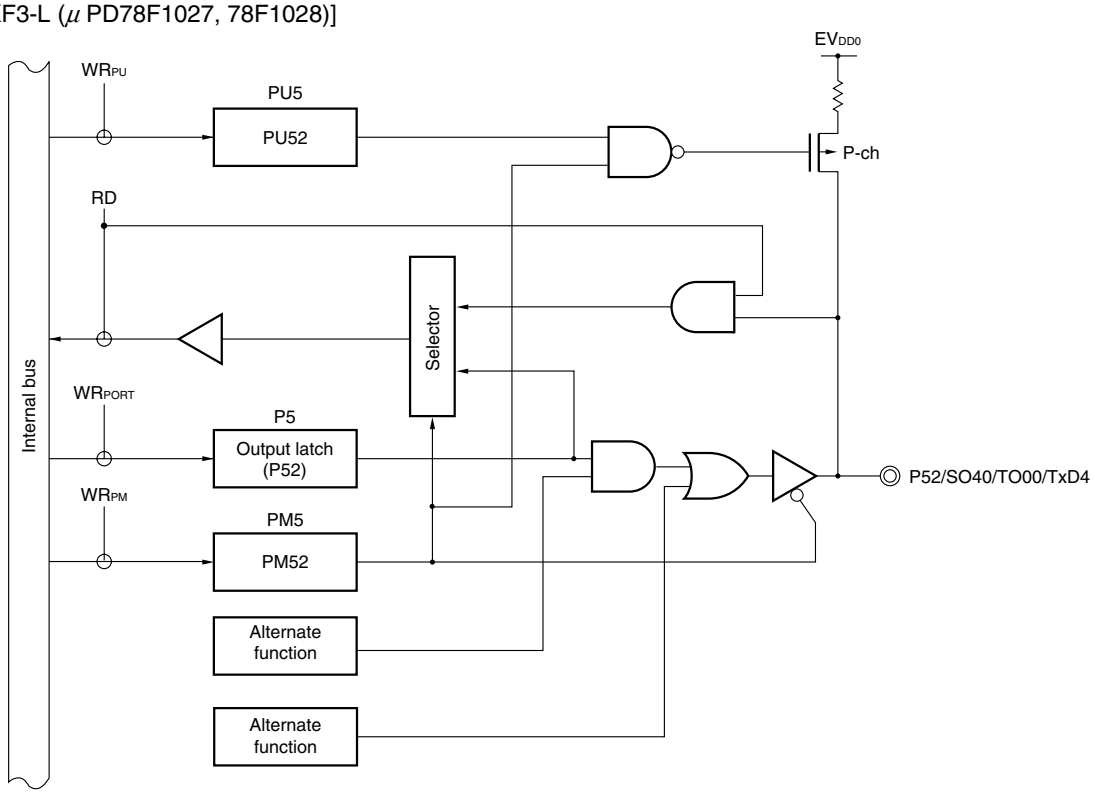
Figure 6-28. Block Diagram of P51



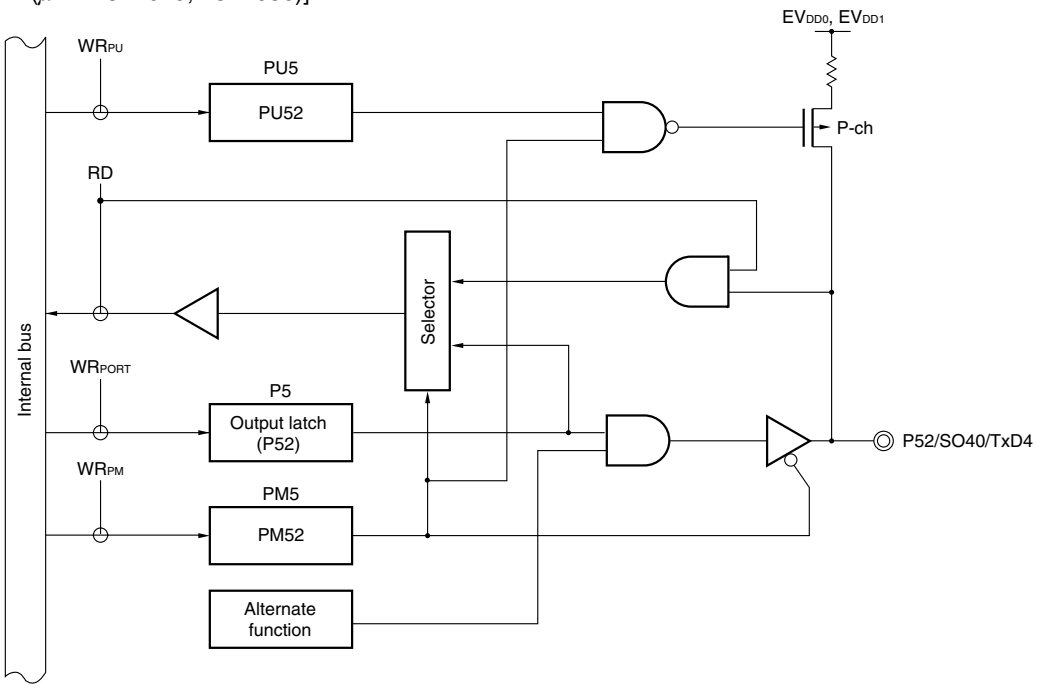
P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

Figure 6-29. Block Diagram of P52

[78K0R/KF3-L (μPD78F1027, 78F1028)]



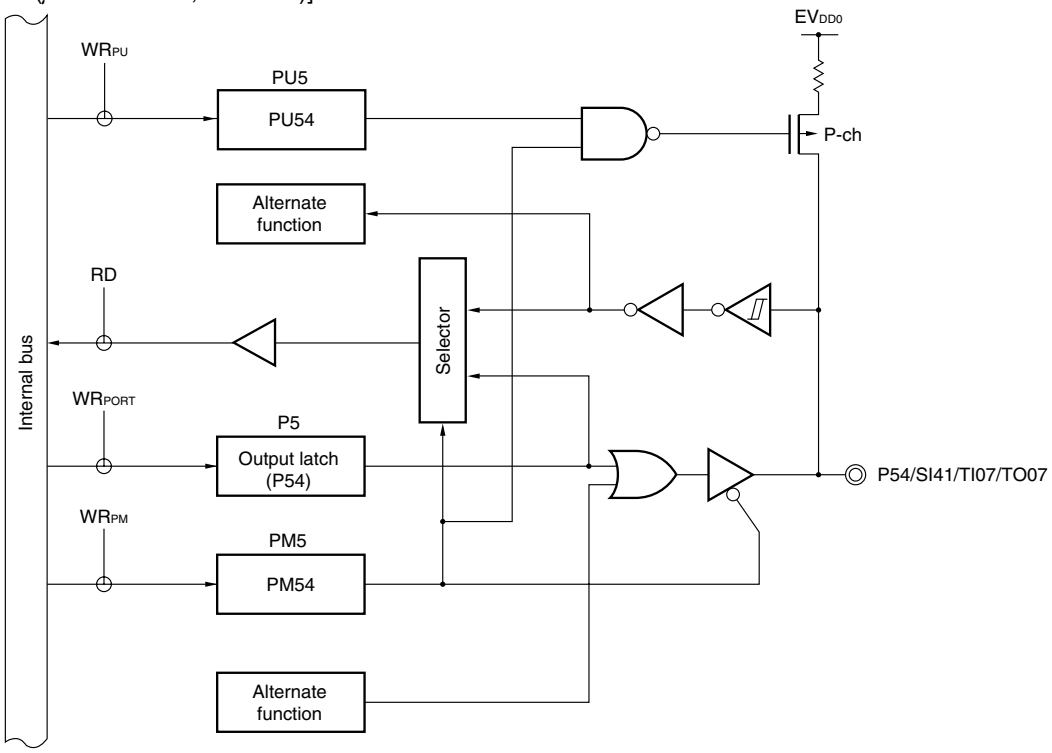
[78K0R/KG3-L (μPD78F1029, 78F1030)]



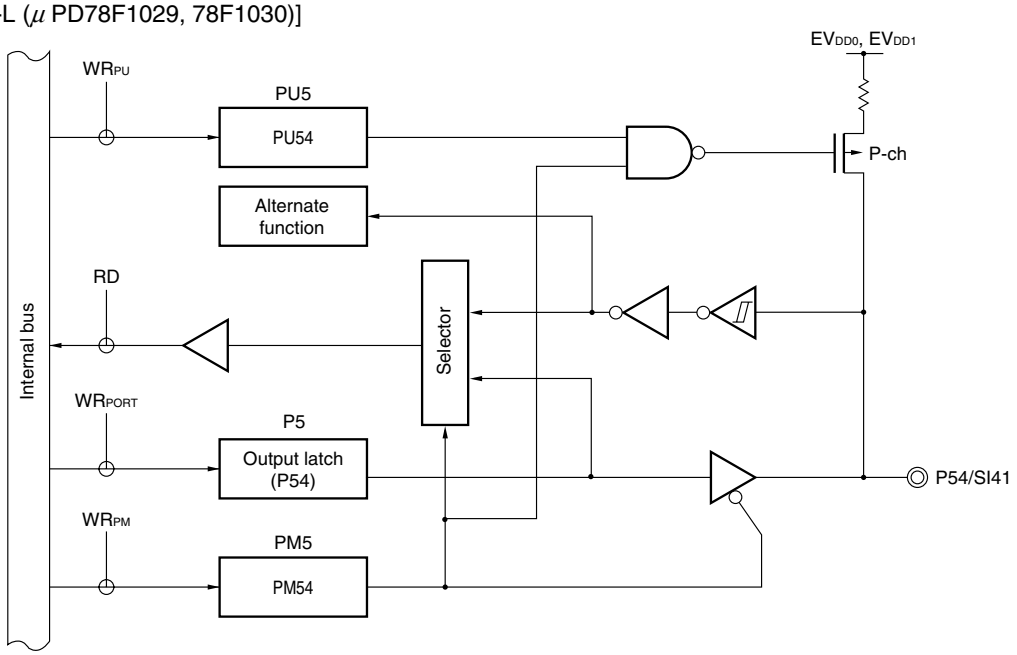
P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

Figure 6-30. Block Diagram of P54

[78K0R/KF3-L (μPD78F1027, 78F1028)]



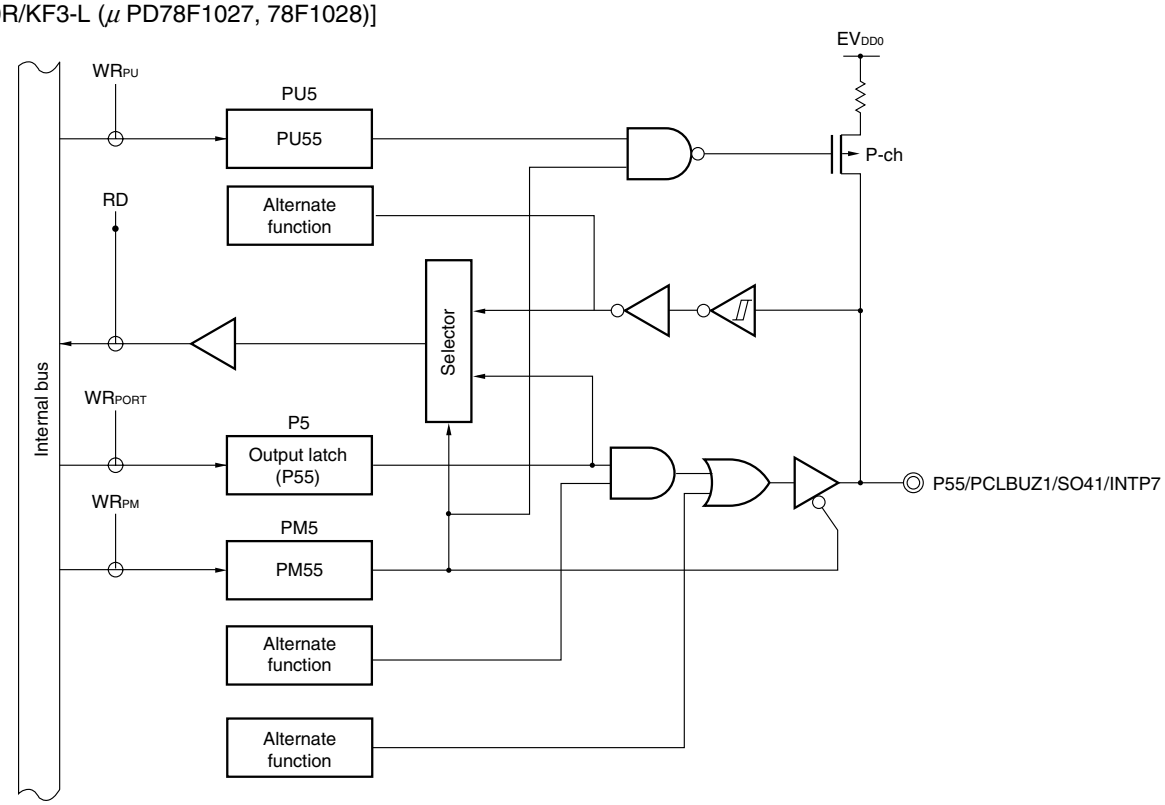
[78K0R/KG3-L (μPD78F1029, 78F1030)]



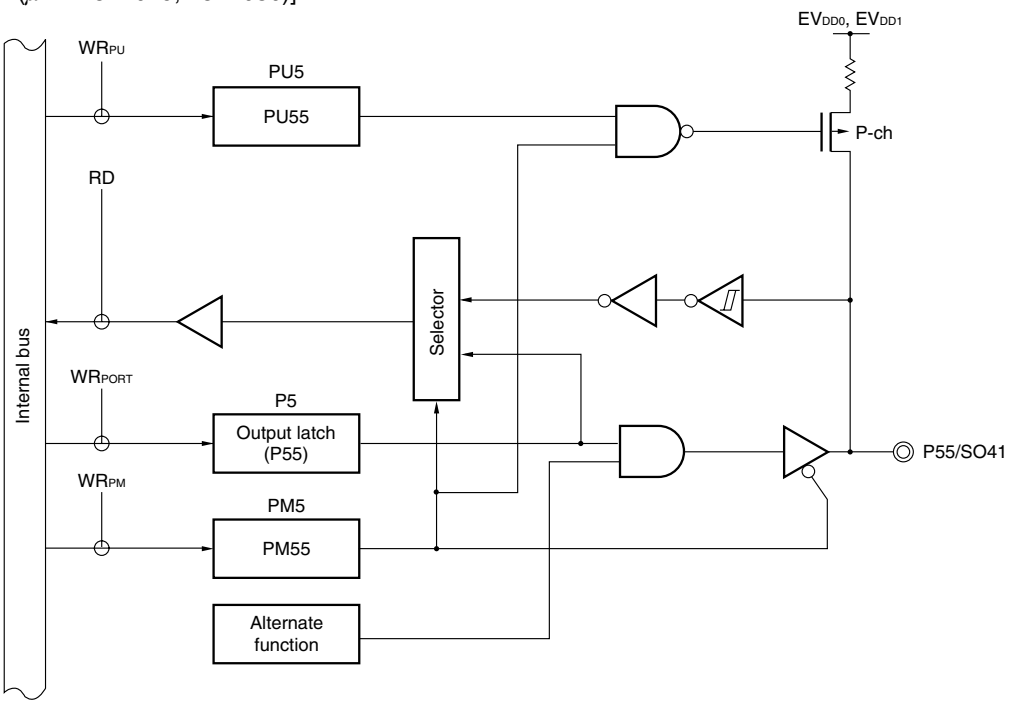
P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

Figure 6-31. Block Diagram of P55

[78K0R/KF3-L (μPD78F1027, 78F1028)]

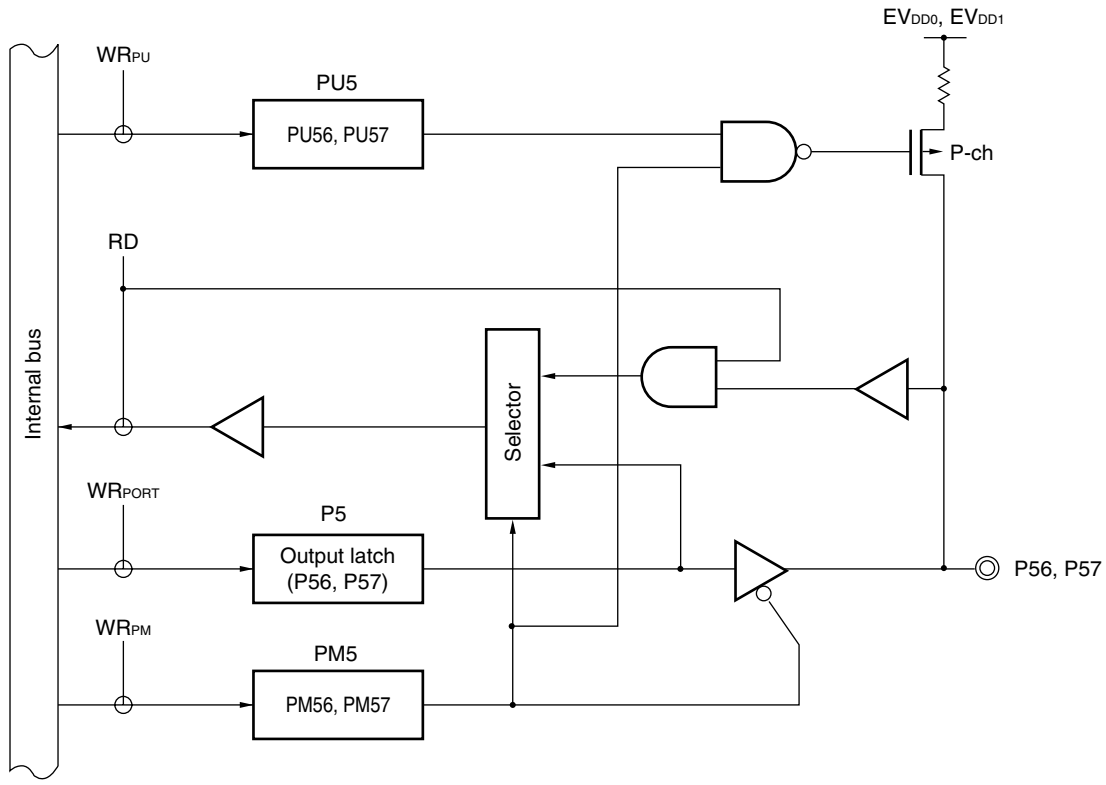


[78K0R/KG3-L (μPD78F1029, 78F1030)]



P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

Figure 6-32. Block Diagram of P56 and P57



P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

6.2.8 Port 6

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P60/SCL0	√	√
P61/SDA0	√	√
P62	√	√
P63	√	√
P64/TI10/TO10	√	√
P65/TI11/TO11	√	√
P66/TI12/TO12	√	√
P67/TI13/TO13	√	√

Port 6 is an I/O port with an output latch. Port 6 can be set to the input mode or output mode in 1-bit units using port mode register 6 (PM6). When the P64 to P67 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 6 (PU6).

The output of the P60 to P63 pins is N-ch open-drain output (6 V tolerance).

This port can also be used for serial interface data I/O, clock I/O, and timer I/O.

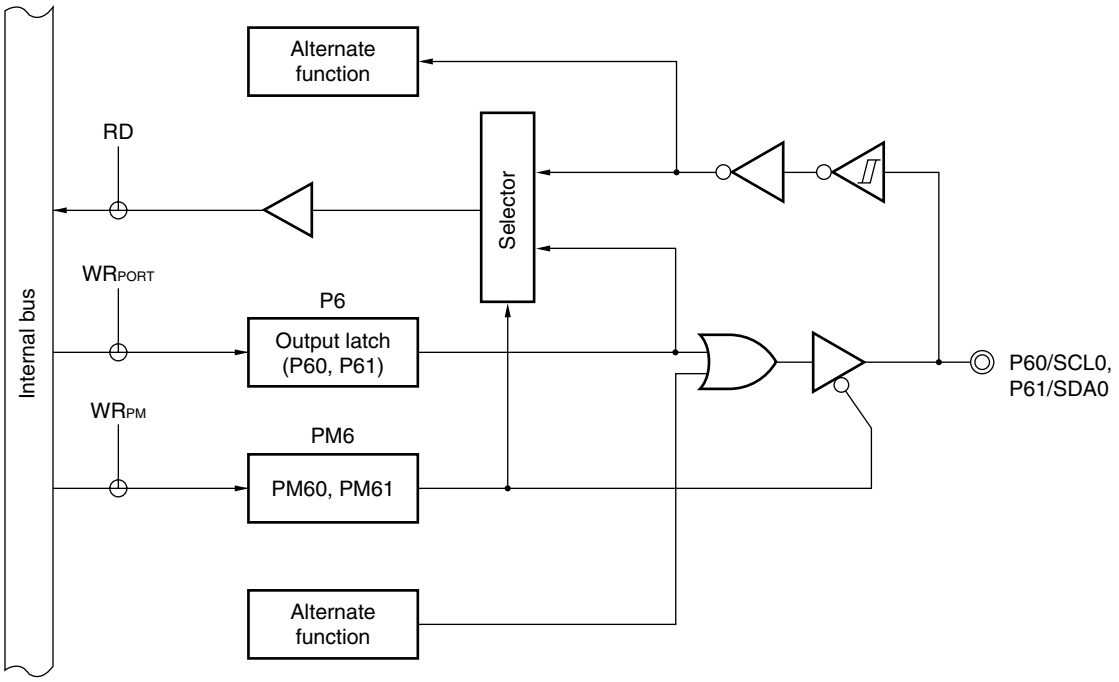
Reset signal generation sets port 6 to input mode.

Figures 6-33 to 6-36 show block diagrams of port 6.

Cautions 1. Stop the operation of serial interface IICA when using P60/SCL0 and P61/SDA0 as general-purpose ports.

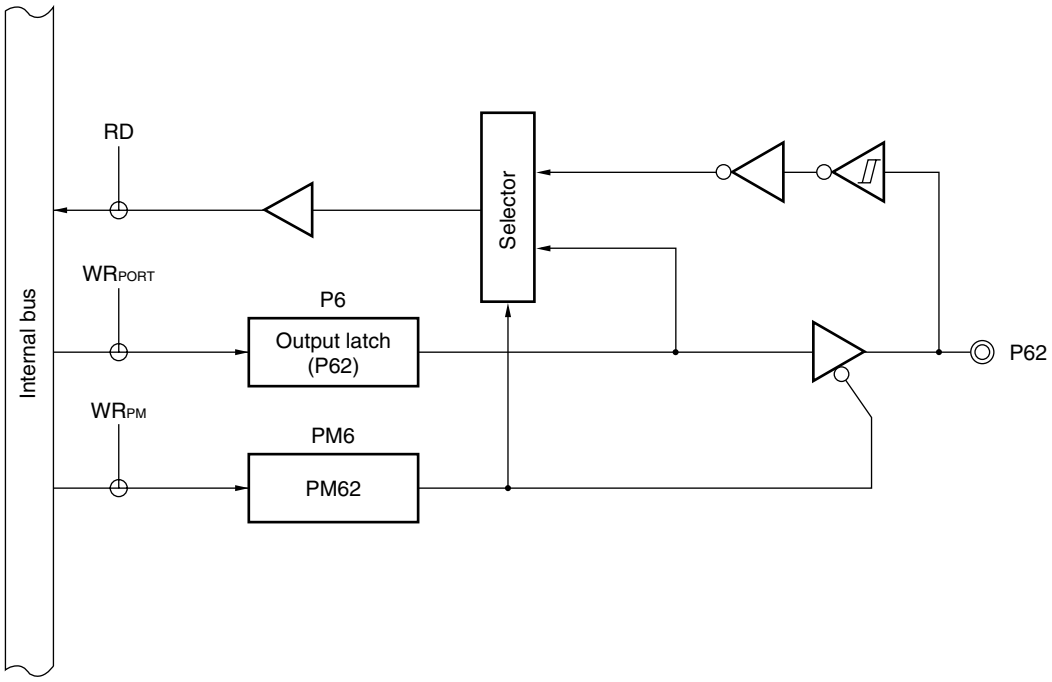
2. To use P64/TI10/TO10 to P67/TI13/TO13 as a general-purpose port, set bits 0 to 3 (TO10 to TO13) of timer output register 1 (TO1) and bits 0 to 3 (TOE10 to TOE13) of timer output enable register 1 (TOE1) to "0", which is the same as their default status setting.

Figure 6-33. Block Diagram of P60 and P61



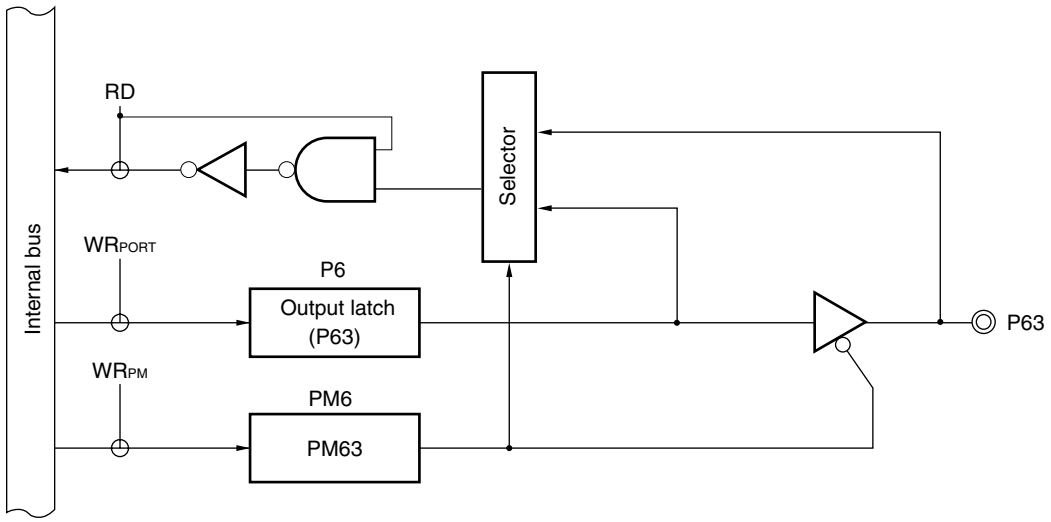
P6: Port register 6
PM6: Port mode register 6
RD: Read signal
WR××: Write signal

Figure 6-34. Block Diagram of P62



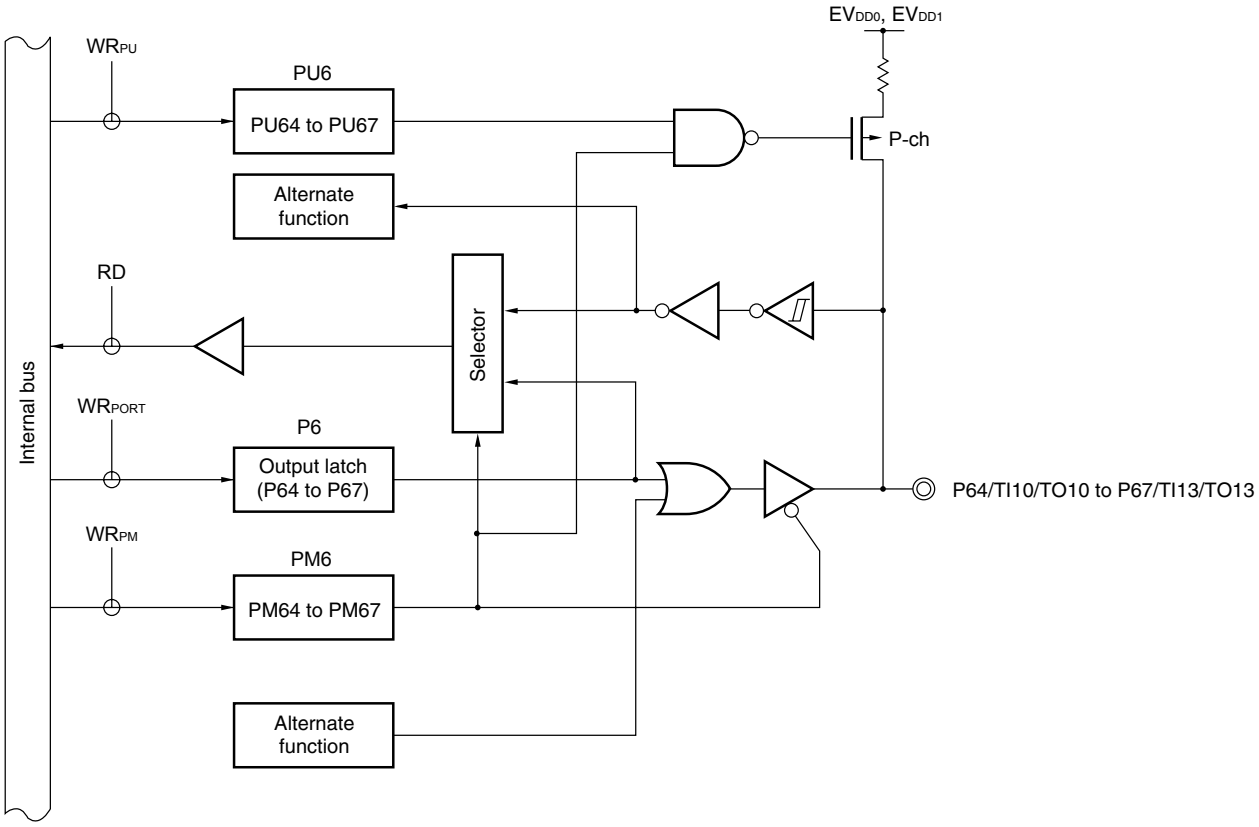
P6: Port register 6
PM6: Port mode register 6
RD: Read signal
WR××: Write signal

Figure 6-35. Block Diagram of P63



P6: Port register 6
PM6: Port mode register 6
RD: Read signal
WR××: Write signal

Figure 6-36. Block Diagram of P64 to P67



P6: Port register 6
PU6: Pull-up resistor option register 6
PM6: Port mode register 6
RD: Read signal
WR××: Write signal

6.2.9 Port 7

	78K0R/KF3-L (μPD78F10xx: xx = 10 to 12, 27,28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P70/KR0	√	√
P71/KR1	√	√
P72/KR2	√	√
P73/KR3	√	√
P74/KR4/INTP8	√	√
P75/KR5/INTP9	√	√
P76/KR6/INTP10	√	√
P77/KR7/INTP11	√	√

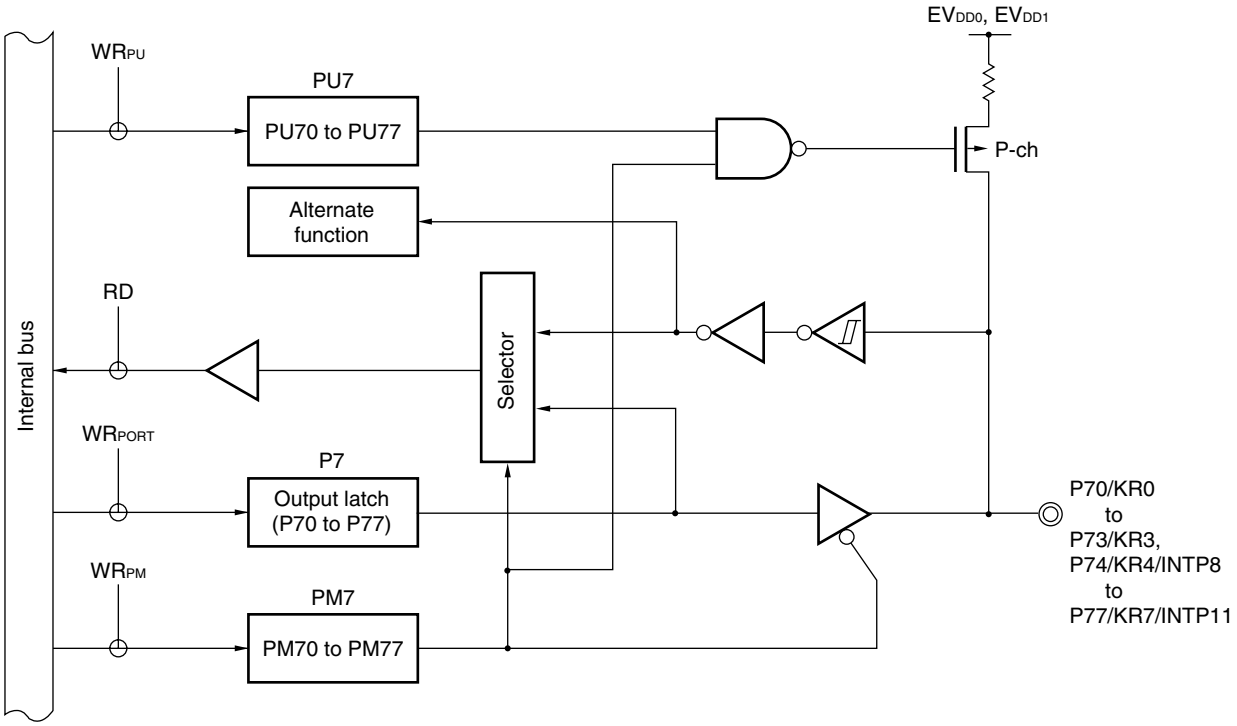
Port 7 is an I/O port with an output latch. Port 7 can be set to the input mode or output mode in 1-bit units using port mode register 7 (PM7). When used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 7 (PU7).

This port can also be used for key return input and interrupt request input.

Reset signal generation sets port 7 to input mode.

Figure 6-37 shows a block diagram of port 7.

Figure 6-37. Block Diagram of P70 to P77



P7: Port register 7
PU7: Pull-up resistor option register 7
PM7: Port mode register 7
RD: Read signal
WR××: Write signal

6.2.10 Port 8

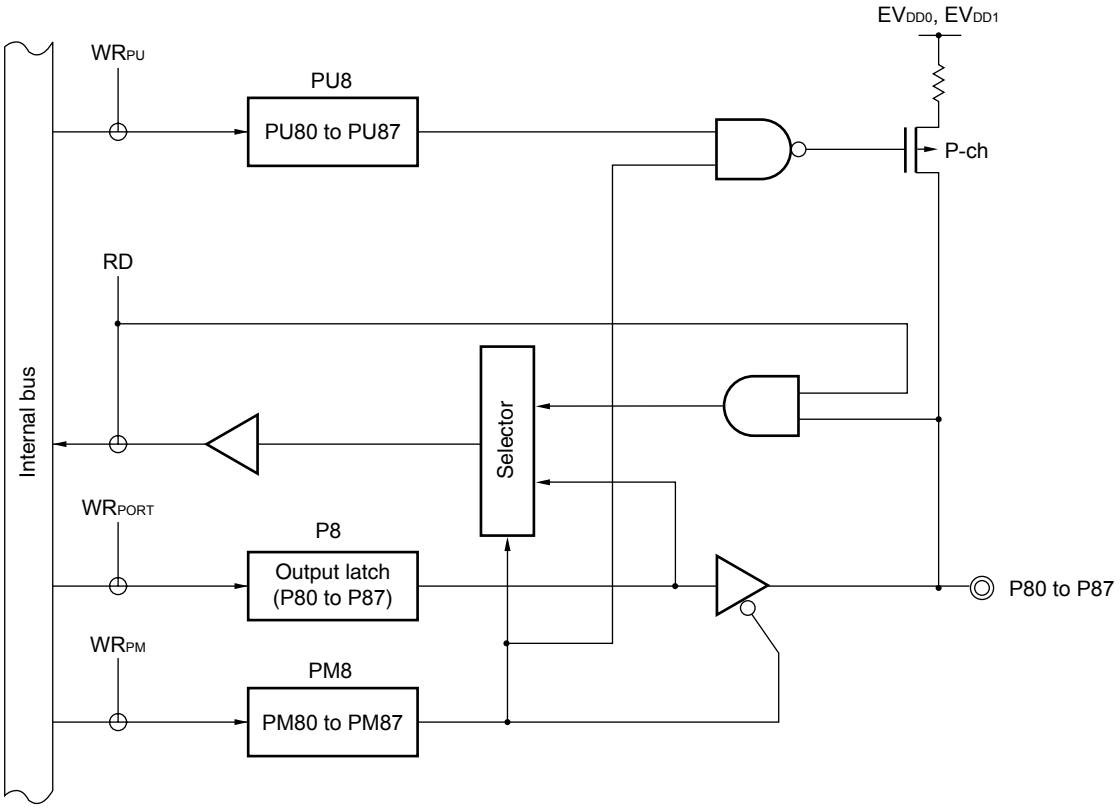
	78K0R/KF3-L (μPD78F10xx: xx = 10 to 12, 27,28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P80	–	√
P81	–	√
P82	–	√
P83	–	√
P84	–	√
P85	–	√
P86	–	√
P87	–	√

Port 8 is an I/O port with an output latch. Port 8 can be set to the input mode or output mode in 1-bit units using port mode register 8 (PM8). When the P80 to P87 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 8 (PU8).

Reset signal generation sets port 8 to input mode.

Figure 6-38 shows a block diagram of port 8.

Figure 6-38. Block Diagram of P80 to P87



P8: Port register 8
PU8: Pull-up resistor option register 8
PM8: Port mode register 8
RD: Read signal
WR××: Write signal

6.2.11 Port 9

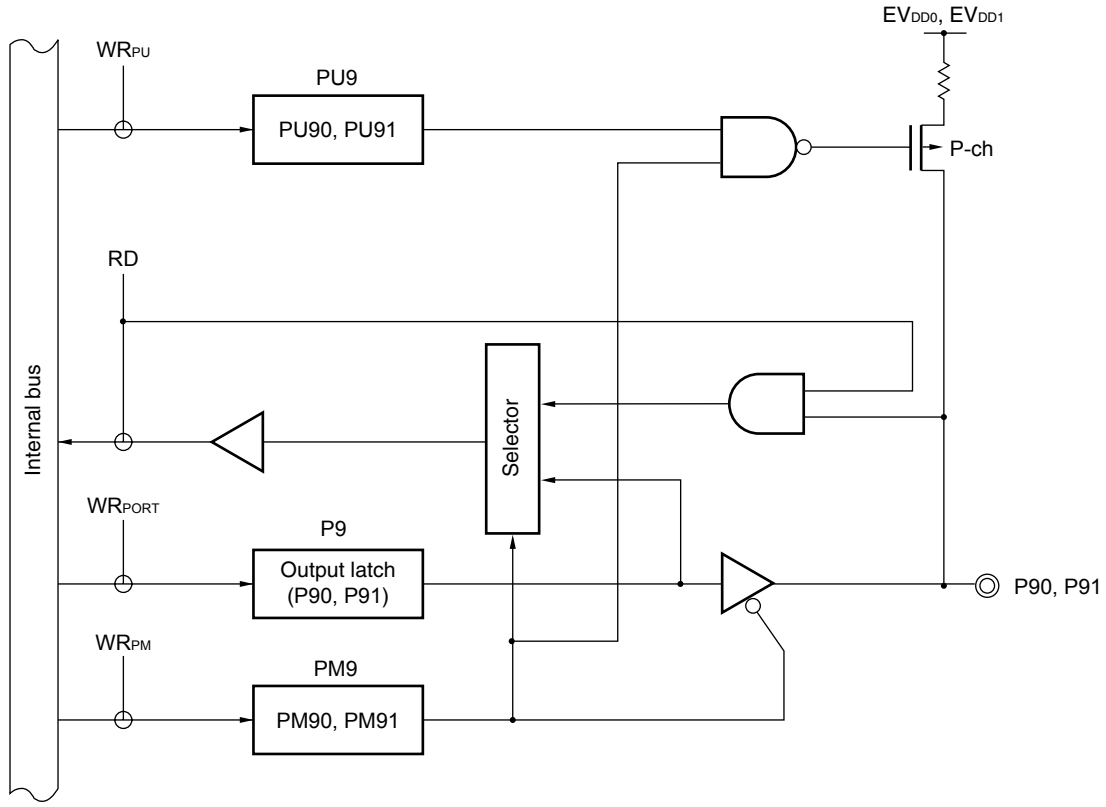
	78K0R/KF3-L (μPD78F10xx: xx = 10 to 12, 27,28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P90	√	–
P91	√	√

P91 is an I/O port with an output latch. Port 9 can be set to the input mode or output mode in 1-bit units using port mode register 9 (PM9). When the P90 and P91 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 9 (PU9).

Reset signal generation sets port 9 to input mode.

Figure 6-39 shows a block diagram of port 9.

Figure 6-39. Block Diagram of P90 and P91



P9: Port register 9
PU9: Pull-up resistor option register 9
PM9: Port mode register 9
RD: Read signal
WR××: Write signal

6.2.12 Port 11

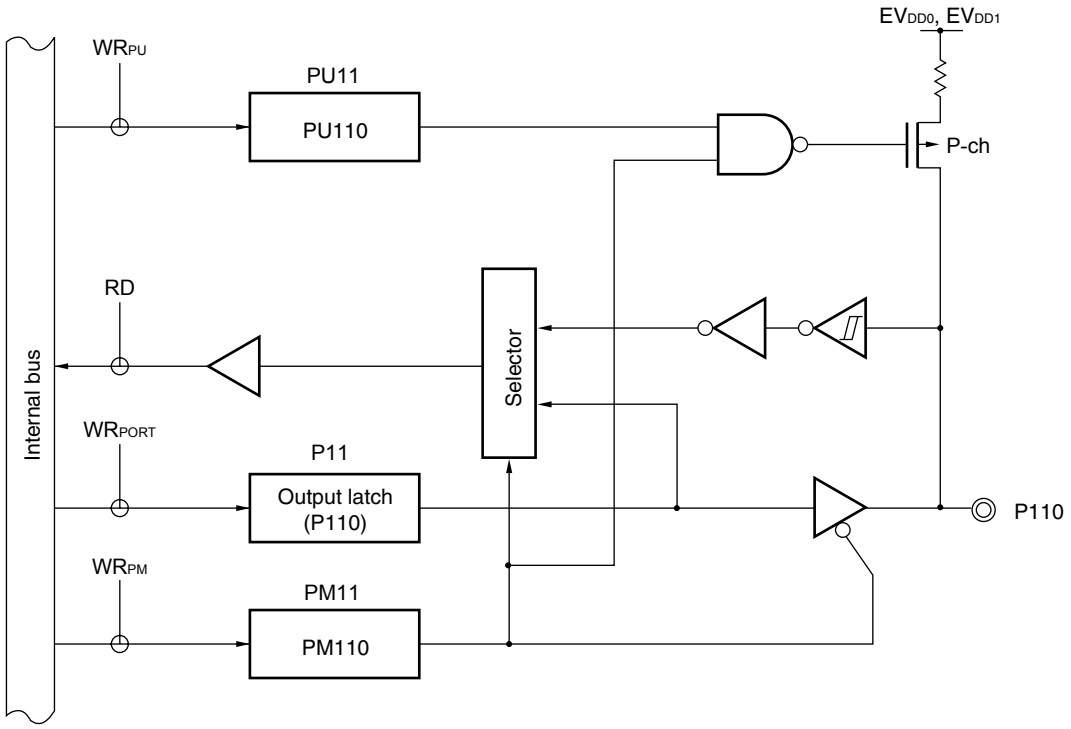
	78K0R/KF3-L (μPD78F10xx: xx = 10 to 12, 27,28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P110	√	√
P111	√	√

Port 11 is an I/O port with an output latch. Port 11 can be set to the input mode or output mode in 1-bit units using port mode register 11 (PM11). When the P110 and P111 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 11 (PU11).

Reset signal generation sets port 11 to input mode.

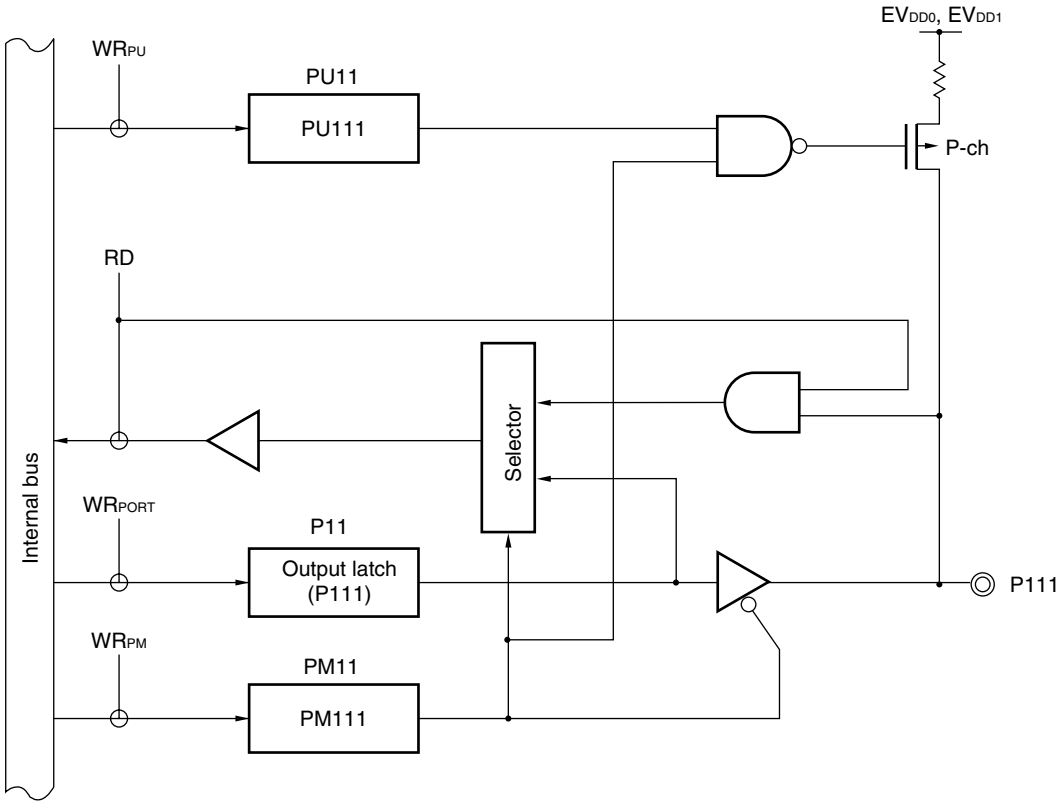
Figures 6-40 and 6-41 show a block diagram of port 11.

Figure 6-40. Block Diagram of P110



P11: Port register 11
PU11: Pull-up resistor option register 11
PM11: Port mode register 11
RD: Read signal
WR××: Write signal

Figure 6-41. Block Diagram of P111



P11: Port register 11
PU11: Pull-up resistor option register 11
PM11: Port mode register 11
RD: Read signal
WR××: Write signal

6.2.13 Port 12

	78K0R/KF3-L (μPD78F10xx: xx = 10 to 12, 27,28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P120/INTP0/EXLVI	√	√
P121/X1	√	√
P122/X2/EXCLK	√	√
P123/XT1	√	√
P124/XT2	√	√

P120 is an I/O port with an output latch. Port 12 can be set to the input mode or output mode in 1-bit units using port mode register 12 (PM12). When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P124 are 4-bit input ports.

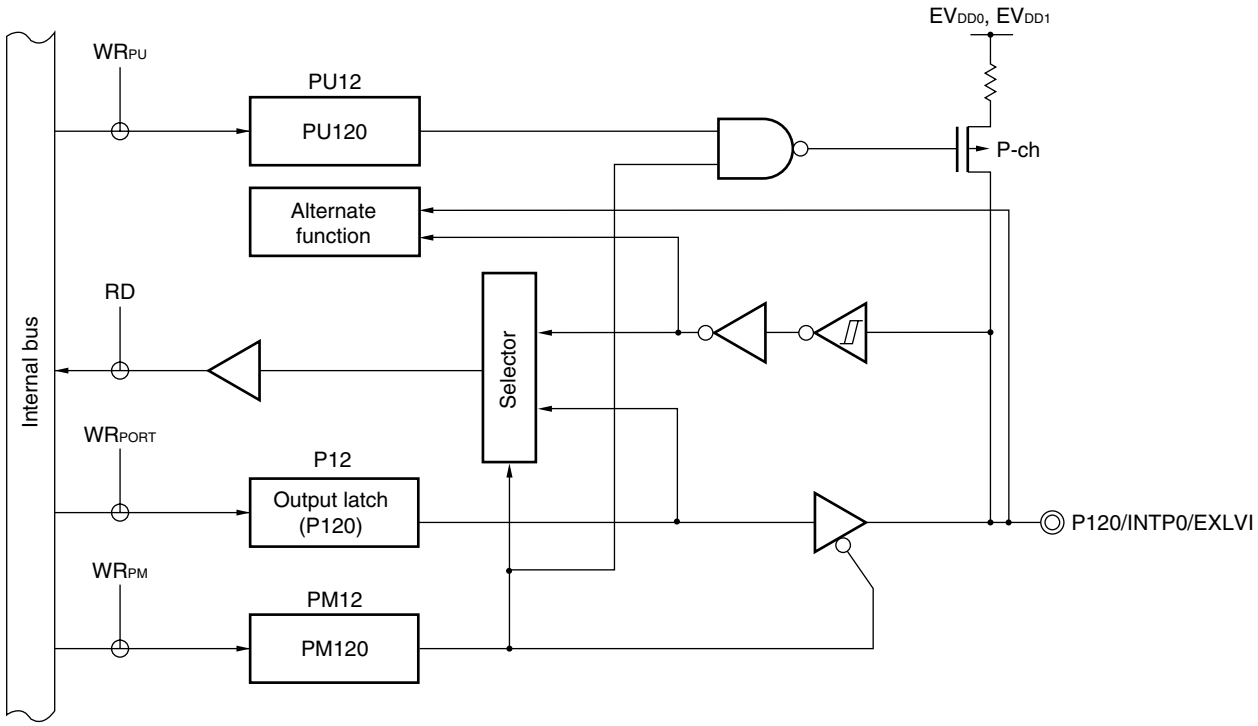
This port can also be used for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, and external clock input for main system clock.

Reset signal generation sets port 12 to input mode.

Figures 6-42 to 6-44 show block diagrams of port 12.

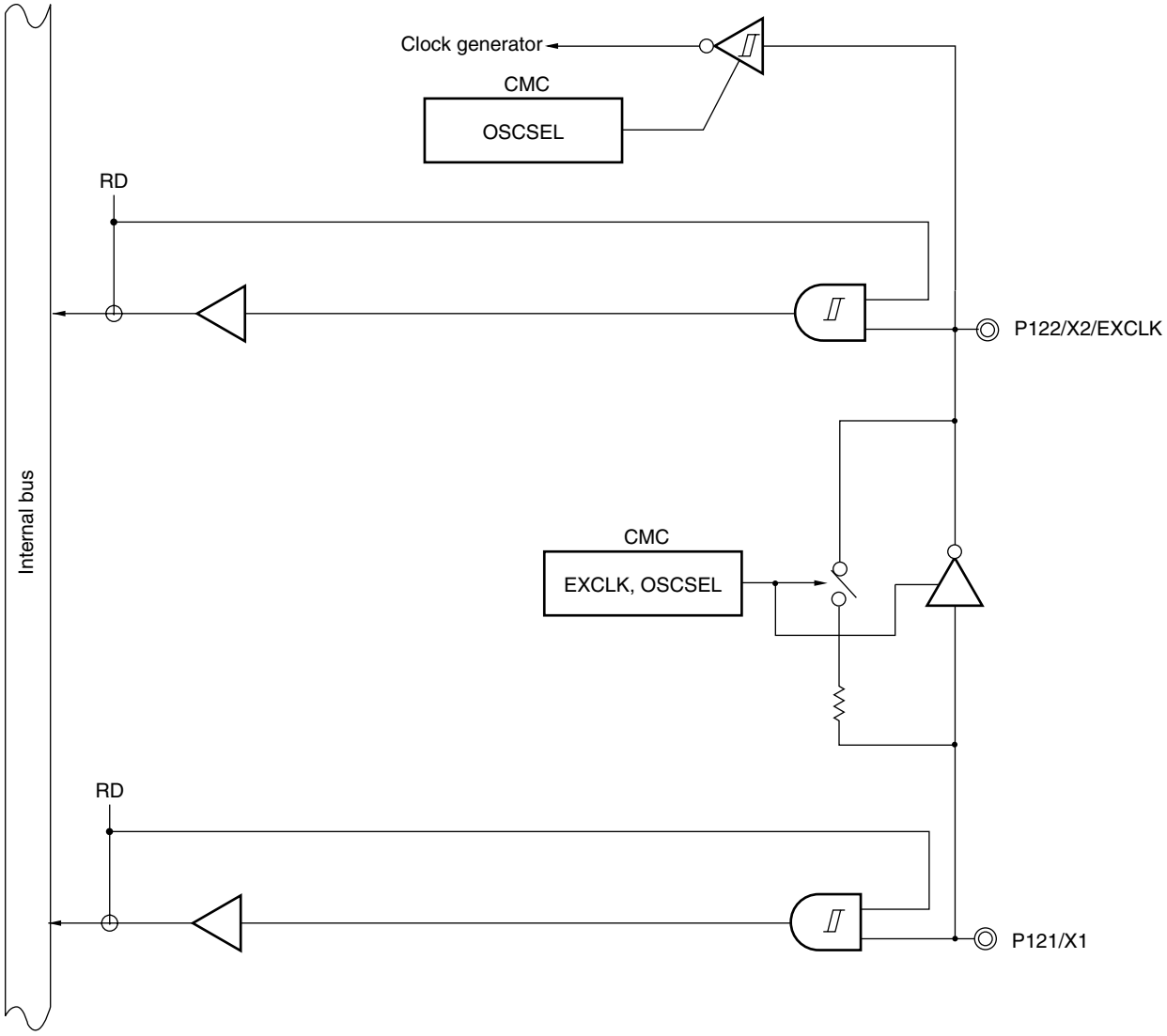
Caution The function setting on P121 to P124 is available only once after the reset release. The port once set for connection to an oscillator cannot be used as an input port unless the reset is performed.

Figure 6-42. Block Diagram of P120



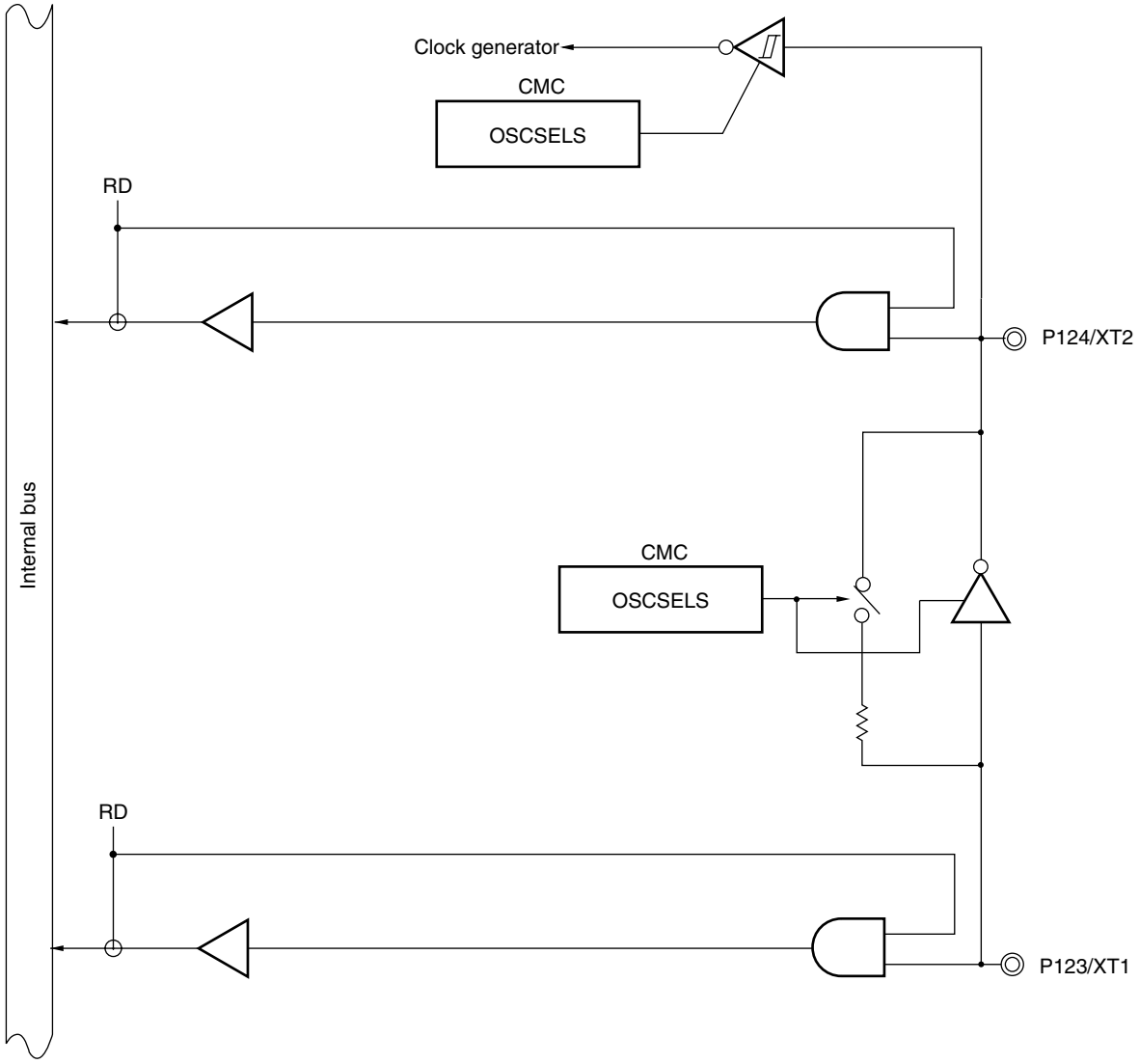
P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
RD: Read signal
WR××: Write signal

Figure 6-43. Block Diagram of P121 and P122



CMC: Clock operation mode control register
RD: Read signal

Figure 6-44. Block Diagram of P123 and P124



CMC: Clock operation mode control register
RD: Read signal

6.2.14 Port 13

	78K0R/KF3-L (μPD78F10xx: xx = 10 to 12, 27,28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P130/INTP1	√	√
P131/TI06/TO06	–Note	√

Note TI06/TO06 is shared with P06, in the 78K0R/KF3-L.

P130 is a 1-bit output-only port with an output latch.

P131 is a 1-bit I/O port with an output latch. When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 13 (PU13).

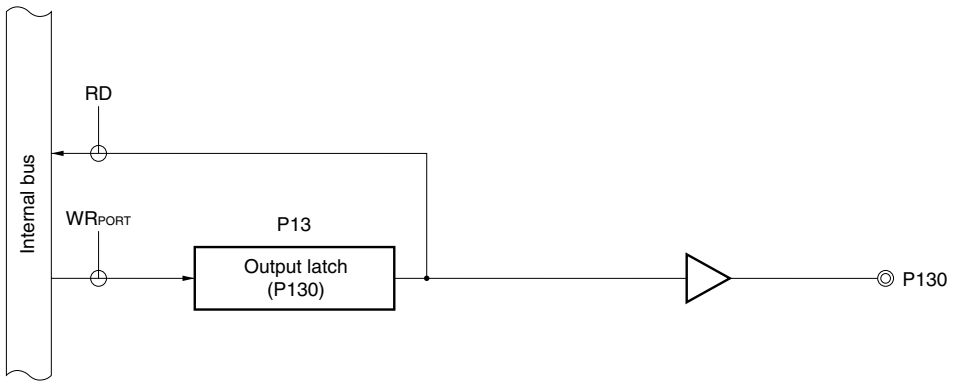
Reset signal generation sets port 13 to input mode.

This port can also be used for timer I/O.

Figures 6-45 and 6-46 show block diagrams of port 13.

Caution To use P131/TI06/TO06 as a general-purpose port, set bit 6 (TO06) of timer output register 0 (TO0) and bit 6 (TOE06) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

Figure 6-45. Block Diagram of P130



P13: Port register 13
RD: Read signal
WR××: Write signal

Remark When reset is effected, P130 outputs a low level. If P130 is set to output a high level before reset is effected, the output signal of P130 can be dummy-output as the CPU reset signal.

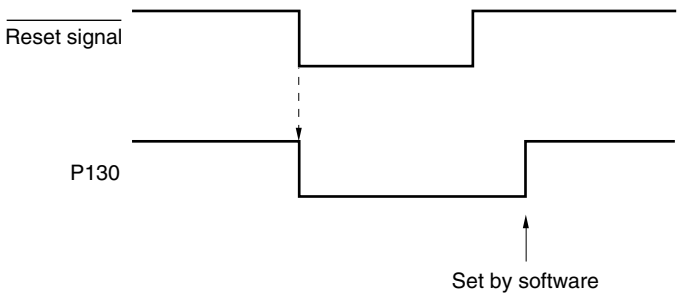
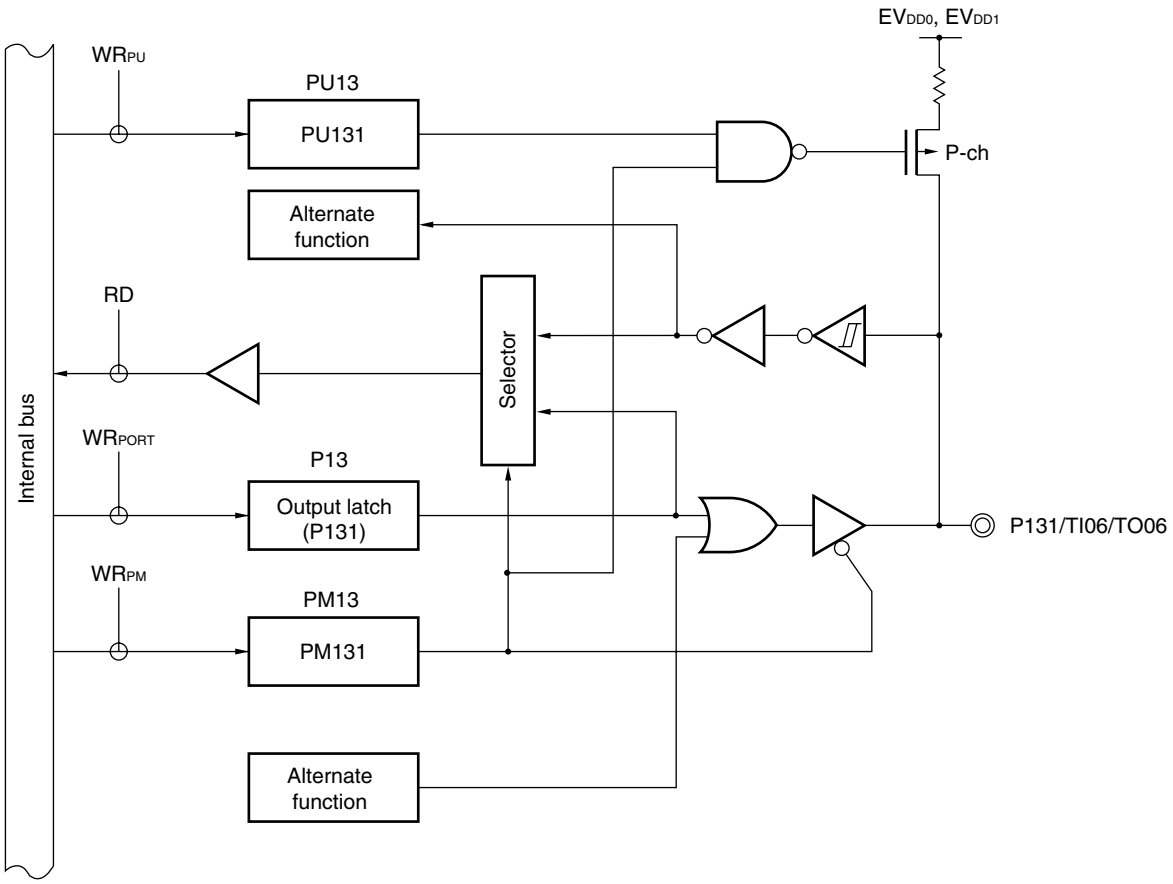


Figure 6-46. Block Diagram of P131



P13: Port register 13
PU13: Pull-up resistor option register 13
PM13: Port mode register 13
RD: Read signal
WR××: Write signal

6.2.15 Port 14

	78K0R/KF3-L (μPD78F10xx: xx = 10 to 12, 27,28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P140/PCLBUZ0/INTP6	√	√
P141/PCLBUZ1/INTP7	– Note 1	√
P142/$\overline{\text{SCK20}}$/SCL20	√	√
P143/SI20/RxD2/SDA20	√	√
P144/SO20/TxD2	√	√
P145/TI07/TO07	– Note 2	√

Notes 1. PCLBUZ/INTP7 is shared with P55, in the 78K0R/KF3-L.

2. TI07/TO07 is shared with P54, in the 78K0R/KF3-L.

Port 14 is an I/O port with an output latch. Port 14 can be set to the input mode or output mode in 1-bit units using port mode register 14 (PM14). When the P140 to P145 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 14 (PU14).

Input to the P142 and P143 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 14 (PIM14).

Output from the P142 to P144 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 14 (POM14).

This port can also be used for timer I/O, external interrupt request input, clock/buzzer output, serial interface data I/O, and clock I/O.

Reset signal generation sets port 14 to input mode.

Figures 6-47 to 6-50 show block diagrams of port 14.

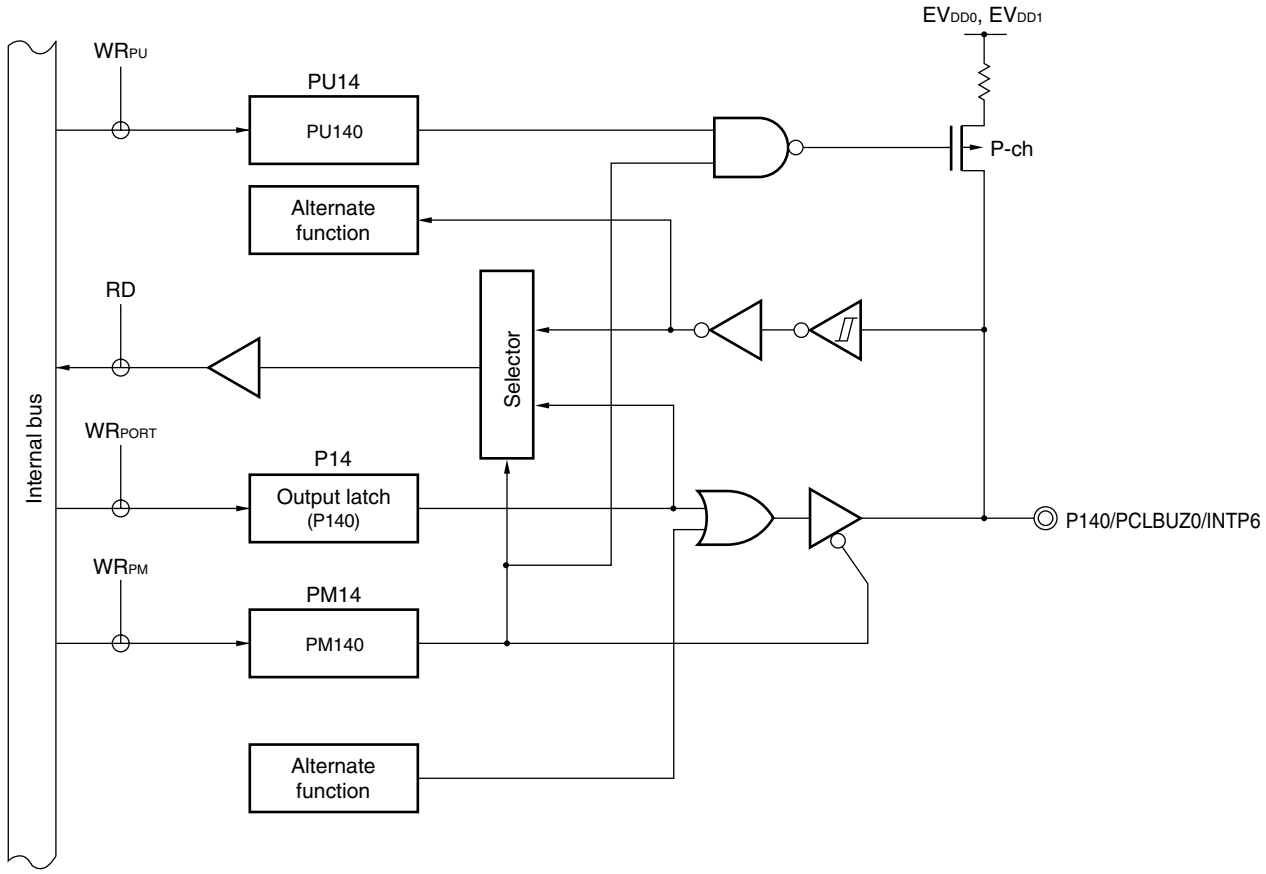
Cautions 1. To use P142/$\overline{\text{SCK20}}$/SCL20, P143/SI20/RxD2/SDA20, or P144/SO20/TxD2 as a general-purpose port, note the serial array unit 1 setting. For details, refer to the following tables.

- **Table 14-13 Relationship Between Register Settings and Pins (Channel 0 of Unit 1: CSI20, UART2 Transmission, IIC20)**
- **Table 14-14 Relationship Between Register Settings and Pins (Channel 1 of Unit 1: UART2 Reception)**

2. To use P145/TI07/TO07 as a general-purpose port, set bit 7 (TO07) of timer output register 0 (TO0) and bit 7 (TOE07) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

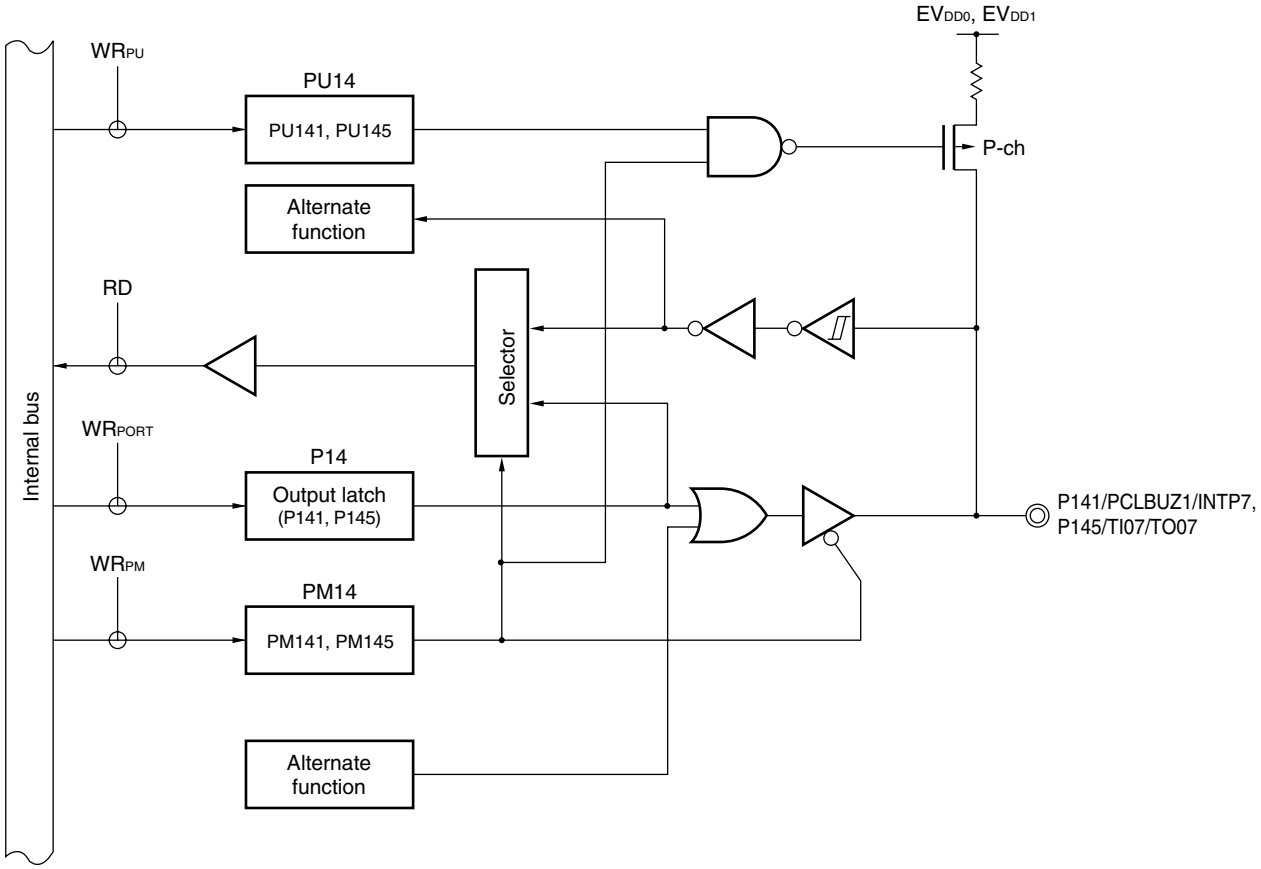
3. To use P140/PCLBUZ0/INTP6 or P141/PCLBUZ1/INTP7 as a general-purpose port, set bit 7 of clock output select registers 0 and 1 (CKS0, CKS1) to "0", which is the same as their default status settings.

Figure 6-47. Block Diagram of P140



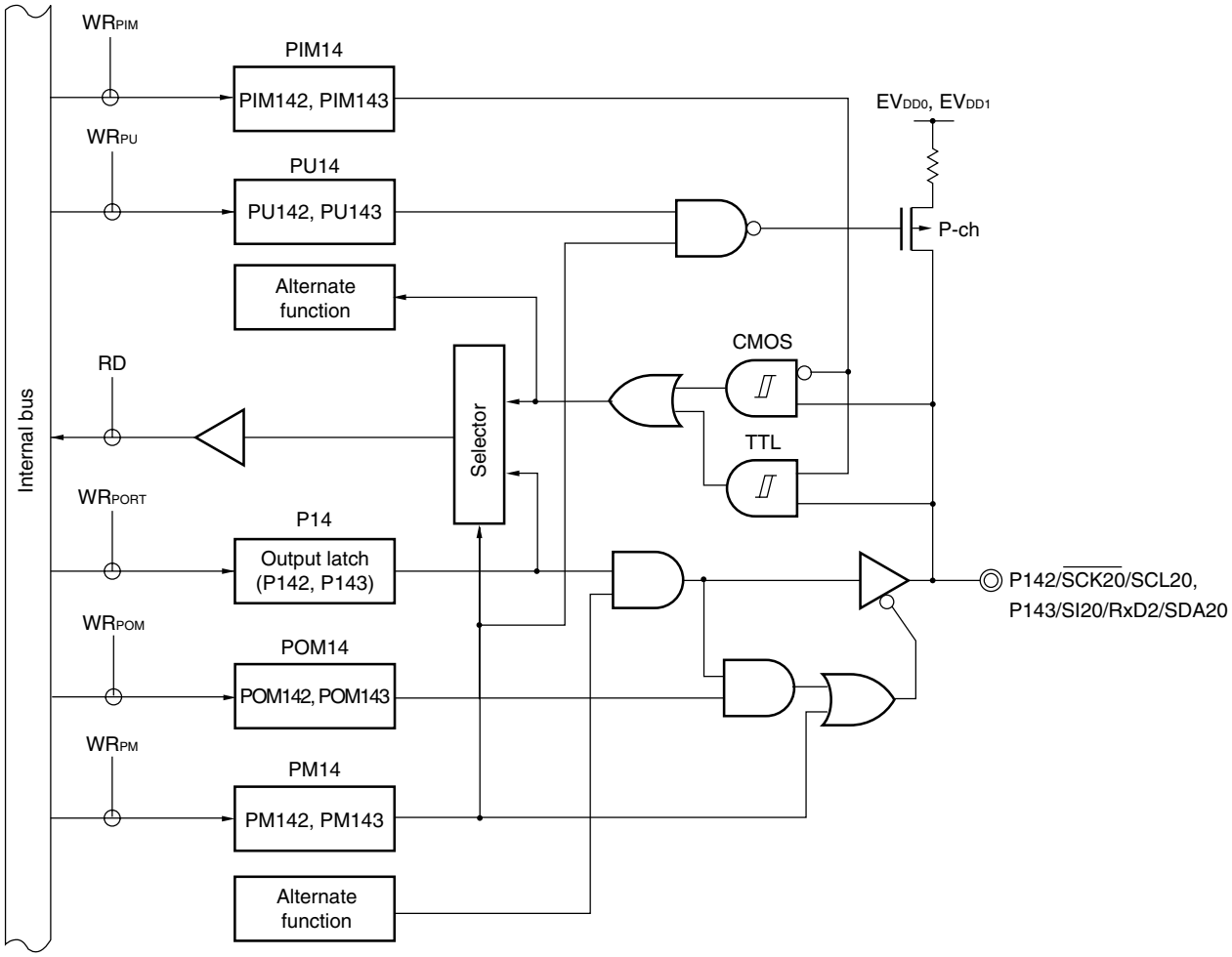
P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
RD: Read signal
WR××: Write signal

Figure 6-48. Block Diagram of P141 and P145



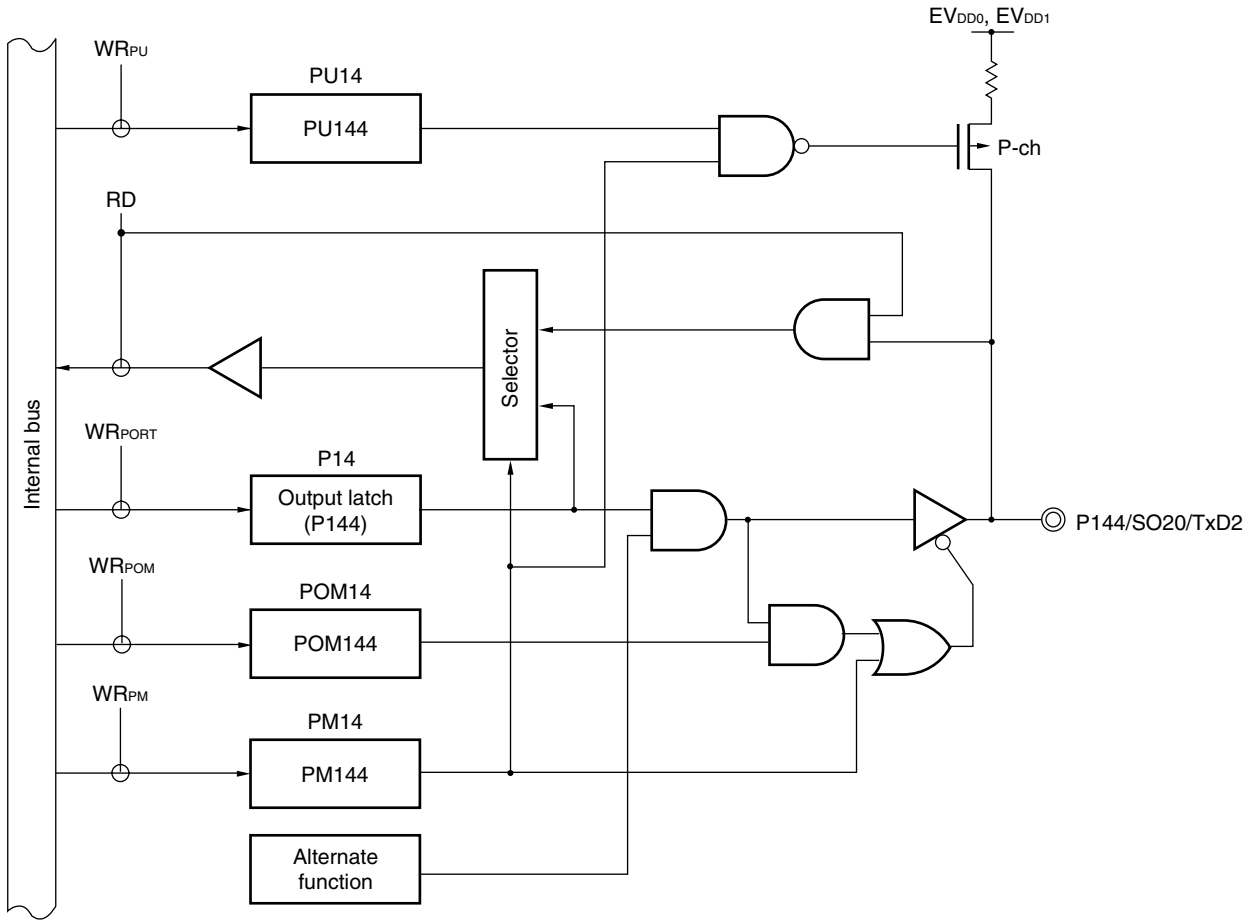
P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
RD: Read signal
WR××: Write signal

Figure 6-49. Block Diagram of P142 and P143



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
PIM14: Port input mode register 14
POM14: Port output mode register 14
RD: Read signal
WR××: Write signal

Figure 6-50. Block Diagram of P144



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
POM14: Port output mode register 14
RD: Read signal
WR××: Write signal

6.2.16 Port 15

	78K0R/KF3-L (μPD78F10xx: xx = 10 to 12, 27,28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P150/ANI8	√	√
P151/ANI9	√	√
P152/ANI10	√	√
P153/ANI11	√	√
P154/ANI12	–	√
P155/ANI13	–	√
P156/ANI14	–	√
P157/ANI15	–	√

Port 15 is an I/O port with an output latch. Port 15 can be set to the input mode or output mode in 1-bit units using port mode register 15 (PM15).

This port can also be used for A/D converter analog input.

To use P150/ANI8 to P157/ANI15 as digital input pins, set them in the digital I/O mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM15 register. Use these pins starting from the lower bit.

To use P150/ANI8 to P157/ANI15 as digital output pins, set them in the digital I/O mode by using the ADPC register and in the output mode by using the PM15 register.

Table 6-6. Setting Functions of P150/ANI8 to P157/ANI15 Pins

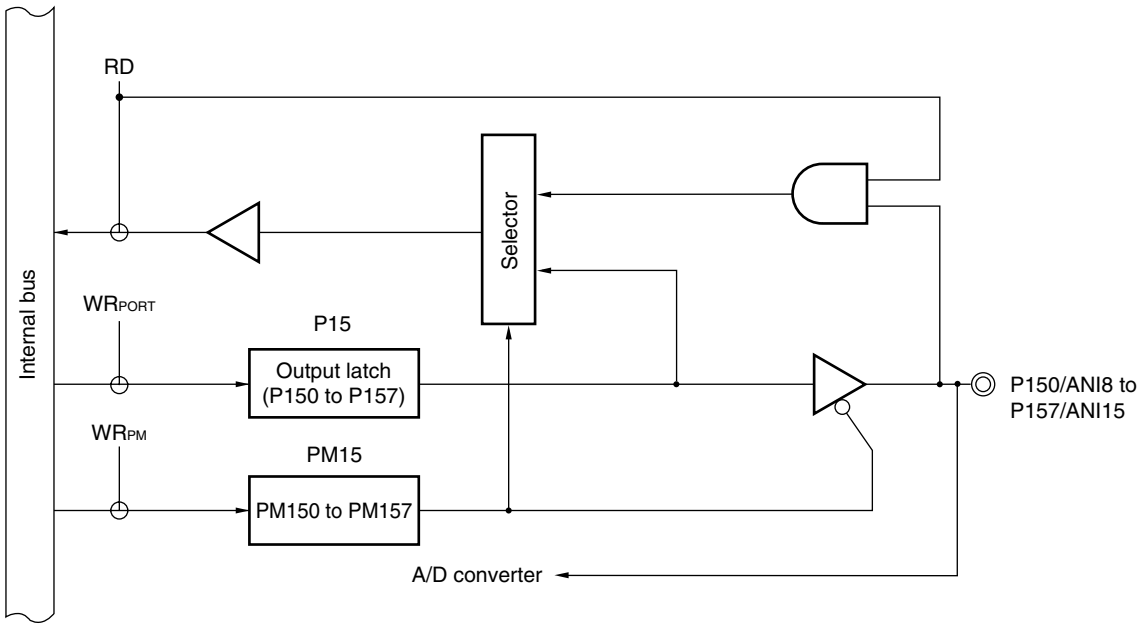
ADPC Register	PM15 Register	ADS Register	P150/ANI8 to P157/ANI15 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

All P150/ANI8 to P157/ANI15 are set in the digital input mode when the reset signal is generated.

Figure 6-51 shows a block diagram of port 15.

Caution See 3.2.16 AV_{REF}, AV_{SS}, V_{DD}, EV_{DD0}, EV_{DD1}, V_{SS}, EV_{SS0}, EV_{SS1} for the voltage to be applied to the AV_{REF} pin when using port 15 as a digital I/O.

Figure 6-51. Block Diagram of P150 to P157



P15: Port register 15
PM15: Port mode register 15
RD: Read signal
WR××: Write signal

6.3 Registers Controlling Port Function

Port functions are controlled by the following six types of registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- Port input mode registers (PIM0, PIM1, PIM14)
- Port output mode registers (POM0, POM1, POM14)
- A/D port configuration register (ADPC)

(1) Port mode registers (PMxx)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH (FEH for PM13).

When port pins are used as alternate-function pins, set the port mode register by referencing **6.5 Settings of Port Mode Register, and Output Latch When Using Alternate Function**.

Figure 6-52. Format of Port Mode Register (78K0R/KF3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	1	1	FFF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	1	1	PM31	PM30	FFF23H	FFH	R/W
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
PM5	1	1	PM55	PM54	PM53	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM9	1	1	1	1	1	1	PM91	PM90	FFF29H	FFH	R/W
PM11	1	1	1	1	1	1	PM111	PM110	FFF2BH	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM14	1	1	1	PM144	PM143	PM142	1	PM140	FFF2EH	FFH	R/W
PM15	1	1	1	1	PM153	PM152	PM151	PM150	FFF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 7, 9, 11, 12, 14, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits 0, 1 and 7 of the PM0 register, bits 2 to 7 of the PM3 register, bits 6 and 7 of the PM5 register, bits 2 to 7 of the PM9 register, bits 2 to 7 of the PM11 register, bits 1 to 7 of the PM12 register, bits 1 and 5 to 7 of the PM14 register, and bits 4 to 7 of the PM15 register to "1".

Figure 6-53. Format of Port Mode Register (78K0R/KG3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	1	1	PM31	PM30	FFF23H	FFH	R/W
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM8	PM87	PM86	PM85	PM84	PM83	PM82	PM81	PM80	FFF28H	FFH	R/W
PM9	1	1	1	1	1	1	PM91	1	FFF29H	FFH	R/W
PM11	1	1	1	1	1	1	PM111	PM110	FFF2BH	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM13	1	1	1	1	1	1	PM131	0	FFF2DH	FEH	R/W
PM14	1	1	PM145	PM144	PM143	PM142	PM141	PM140	FFF2EH	FFH	R/W
PM15	PM157	PM156	PM155	PM154	PM153	PM152	PM151	PM150	FFF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 9, 11 to 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bit 7 of the PM0 register, bits 2 to 7 of the PM3 register, bits 0 and 2 to 7 of the PM9 register, bits 2 to 7 of the PM11 register, bits 1 to 7 of the PM12 register, bits 2 to 7 of the PM13 register, and bits 6 and 7 of the PM14 register to "1". And be sure to set bit 0 of the PM13 register to "0".

(2) Port registers (Pxx)

These registers set the output latch value of a port.

If the data is read in the input mode, the pin level is read. If it is read in the output mode, the output latch value is read[Note].

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Note It is always 0 and never a pin level that is read out if a port is read during the input mode when P2 and P15 are set to function as an analog input for a A/D converter.

Figure 6-54. Format of Port Register (78K0R/KF3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	P06	P05	P04	P03	P02	0	0	FFF00H	00H (output latch)	R/W
P1	P17	P16	P15	P14	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	0	0	0	0	0	0	P31	P30	FFF03H	00H (output latch)	R/W
P4	P47	P46	P45	P44	P43	P42	P41	P40	FFF04H	00H (output latch)	R/W
P5	0	0	P55	P54	P53	P52	P51	P50	FFF05H	00H (output latch)	R/W
P6	P67	P66	P65	P64	P63	P62	P61	P60	FFF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P9	0	0	0	0	0	0	P91	P90	FFF09H	00H (output latch)	R/W
P11	0	0	0	0	0	0	P111	P110	FFF0BH	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FFF0CH	Undefined	R/W[Note]
P13	0	0	0	0	0	0	0	P130	FFF0DH	00H (output latch)	R/W
P14	0	0	0	P144	P143	P142	0	P140	FFF0EH	00H (output latch)	R/W
P15	0	0	0	0	P153	P152	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	m = 0 to 7, 9, 11 to 15; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Note P121 to P124 are read-only.

Figure 6-55. Format of Port Register (78K0R/KG3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	P06	P05	P04	P03	P02	P01	P00	FFF00H	00H (output latch)	R/W
P1	P17	P16	P15	P14	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	0	0	0	0	0	0	P31	P30	FFF03H	00H (output latch)	R/W
P4	P47	P46	P45	P44	P43	P42	P41	P40	FFF04H	00H (output latch)	R/W
P5	P57	P56	P55	P54	P53	P52	P51	P50	FFF05H	00H (output latch)	R/W
P6	P67	P66	P65	P64	P63	P62	P61	P60	FFF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P8	P87	P86	P85	P84	P83	P82	P81	P80	FFF08H	00H (output latch)	R/W
P9	0	0	0	0	0	0	P91	0	FFF09H	00H (output latch)	R/W
P11	0	0	0	0	0	0	P111	P110	FFF0BH	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FFF0CH	Undefined	R/W[Note]
P13	0	0	0	0	0	0	P131	P130	FFF0DH	00H (output latch)	R/W
P14	0	0	P145	P144	P143	P142	P141	P140	FFF0EH	00H (output latch)	R/W
P15	P157	P156	P155	P154	P153	P152	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	m = 0 to 9, 11 to 15; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Note P121 to P124 are read-only.

(3) Pull-up resistor option registers (PUxx)

These registers specify whether the on-chip pull-up resistors are to be used or not. On-chip pull-up resistors can be used in 1-bit units only for the bits set to input mode of the pins to which the use of an on-chip pull-up resistor has been specified in these registers. On-chip pull-up resistors cannot be connected to bits set to output mode and bits used as alternate-function output pins, regardless of the settings of these registers.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 6-56. Format of Pull-up Resistor Option Register (78K0R/KF3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	PU06	PU05	PU04	PU03	PU02	0	0	F0030H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU3	0	0	0	0	0	0	PU31	PU30	F0033H	00H	R/W
PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40	F0034H	00H	R/W
PU5	0	0	PU55	PU54	PU53	PU52	PU51	PU50	F0035H	00H	R/W
PU6	PU67	PU66	PU65	PU64	0	0	0	0	F0036H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU9	0	0	0	0	0	0	PU91	PU90	F0039H	00H	R/W
PU11	0	0	0	0	0	0	PU111	PU110	F003BH	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	F003CH	00H	R/W
PU14	0	0	0	PU144	PU143	PU142	0	PU140	F003EH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 7, 9, 11, 12, 14; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Figure 6-57. Format of Pull-up Resistor Option Register (78K0R/KG3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	PU06	PU05	PU04	PU03	PU02	PU01	PU00	F0030H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU3	0	0	0	0	0	0	PU31	PU30	F0033H	00H	R/W
PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40	F0034H	00H	R/W
PU5	PU57	PU56	PU55	PU54	PU53	PU52	PU51	PU50	F0035H	00H	R/W
PU6	PU67	PU66	PU65	PU64	0	0	0	0	F0036H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU8	PU87	PU86	PU85	PU84	PU83	PU82	PU81	PU80	F0038H	00H	R/W
PU9	0	0	0	0	0	0	PU91	0	F0039H	00H	R/W
PU11	0	0	0	0	0	0	PU111	PU110	F003BH	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	F003CH	00H	R/W
PU13	0	0	0	0	0	0	PU131	0	F003DH	00H	R/W
PU14	0	0	PU145	PU144	PU143	PU142	PU141	PU140	F003EH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 9, 11 to 14; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

(4) Port input mode registers (PIM0, PIM1, PIM14)

These registers set the input buffer of P03, P04, P10, P11, P142, or P143 in 1-bit units.

TTL input buffer can be selected during serial communication with an external device of the different potential.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 6-58. Format of Port Input Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PIM0	0	0	0	PIM04	PIM03	0	0	0	F0040H	00H	R/W
PIM1	0	0	0	0	0	0	PIM11	PIM10	F0044H	00H	R/W
PIM14	0	0	0	0	PIM143	PIM142	0	0	F004EH	00H	R/W

PIMmn	Pmn pin input buffer selection (m = 0, 1, 14; n = 0 to 4)
0	Normal input buffer
1	TTL input buffer

(5) Port output mode registers (POM0, POM1, POM14)

These registers set the output mode of P02 to P04, P10, P12, or P142 to P144 in 1-bit units.

N-ch open drain output (V_{DD} tolerance) mode can be selected during serial communication with an external device of the different potential, and for the SDA10 and SDA20 pins during simplified I^2C communication with an external device of the same potential.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 6-59. Format of Port Input Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM0	0	0	0	POM04	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	0	0	0	POM12	0	POM10	F0051H	00H	R/W
POM14	0	0	0	POM144	POM143	POM142	0	0	F005EH	00H	R/W

POMmn	Pmn pin output mode selection (m = 0, 1, 14; n = 0, 2 to 4)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance) mode

(6) A/D port configuration register (ADPC)

This register switches the P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 pins to digital I/O of port or analog input of A/D converter.

The ADPC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 6-60. Format of A/D Port Configuration Register (ADPC)

Address: F0017H After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching															
					Port 15								Port 2							
					ANI15/P157	ANI14/P156	ANI13/P155	ANI12/P154	ANI11/P153	ANI10/P152	ANI9/P151	ANI8/P150	ANI7/P27	ANI6/P26	ANI5/P25	ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	D
0	0	0	1	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	D	D
0	0	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D
0	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D
0	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D
0	0	1	1	0	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D
0	0	1	1	1	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D
0	1	0	0	0	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D
0	1	0	0	1	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	D
0	1	0	1	0	A	A	A	A	A	A	D	D	D	D	D	D	D	D	D	D
0	1	0	1	1	A	A	A	A	A	D	D	D	D	D	D	D	D	D	D	D
0	1	1	0	0	A	A	A	A	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	0	1	A	A	A	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	1	0	A	A	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	1	1	A	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
1	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Other than above					Setting prohibited															

Cautions 1. Set the channel used for A/D conversion to the input mode by using port mode registers 2 and 15 (PM2, PM15).

2. Do not set the pin set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

3. P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 are set as analog inputs in the order of P157/ANI15, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 as analog inputs, start designing from P157/ANI15.

4. Be sure to first set the ADCEN bit of peripheral enable register 0 (PER0) to 1 when setting up the ADPC register. If ADCEN = 0, writing to the ADPC register is ignored and specified values are returned to the initial values.

Remark P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KF3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P157/ANI15: 78K0R/KG3-L

6.4 Port Function Operations

Port operations differ depending on whether the input or output mode is set, as shown below.

6.4.1 Writing to I/O port

(1) Output mode

A value is written to the output latch by a transfer instruction, and the output latch contents are output from the pin.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

A value is written to the output latch by a transfer instruction, but since the output buffer is off, the pin status does not change.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

6.4.2 Reading from I/O port

(1) Output mode

The output latch contents are read by a transfer instruction. The output latch contents do not change.

(2) Input mode

The pin status is read by a transfer instruction. The output latch contents do not change.

6.4.3 Operations on I/O port

(1) Output mode

An operation is performed on the output latch contents, and the result is written to the output latch. The output latch contents are output from the pins.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

The pin level is read and an operation is performed on its contents. The result of the operation is written to the output latch, but since the output buffer is off, the pin status does not change.
The data of the output latch is cleared when a reset signal is generated.

6.4.4 Connecting to external device with different potential (2.5 V, 3 V)

When parts of ports 0, 1, 14 operate with V_{DD} = 4.0 to 5.5 V, I/O connections with an external device that operates on 2.5 V, 3 V power supply voltage are possible.

Regarding inputs, CMOS/TTL switching is possible on a bit-by-bit basis by the port input mode registers (PIM0, PIM1, PIM14).

Moreover, regarding outputs, different potentials can be supported by switching the output buffer to the N-ch open drain (V_{DD} withstand voltage) by the port output mode registers (POM0, POM1, POM14).

(1) Setting procedure when using I/O pins of UART0 to UART2, CSI00, CSI10, and CSI20 functions

(a) Use as 2.5 V, 3 V input port

<1> After reset release, the port mode is the input mode (Hi-Z).

<2> If pull-up is needed, externally pull up the pin to be used (on-chip pull-up resistor cannot be used).

In case of UART0:	P11
In case of UART1:	P03
In case of UART2:	P143
In case of CSI00:	P10, P11
In case of CSI10:	P03, P04
In case of CSI20:	P142, P143

<3> Set the corresponding bit of the PIMn register to 1 to switch to the TTL input buffer.

<4> V_{IH}/V_{IL} operates on 2.5 V, 3 V operating voltage.

(b) Use as 2.5 V, 3 V output port

<1> After reset release, the port mode changes to the input mode (Hi-Z).

<2> Pull up externally the pin to be used (on-chip pull-up resistor cannot be used).

In case of UART1:	P12
In case of UART1:	P02
In case of UART2:	P144
In case of CSI00:	P10, P12
In case of CSI10:	P02, P04
In case of CSI20:	P142, P144

<3> Set the output latch of the corresponding port to 1.

<4> Set the corresponding bit of the POMn register to 1 to set the N-ch open drain output (V_{DD} withstand voltage) mode.

<5> Set the output mode by manipulating the PMn register.
At this time, the output data is high level, so the pin is in the Hi-Z state.

<6> Communication is started by setting the serial array unit.

Remark n = 0, 1, 14

(2) Setting procedure when using I/O pins of simplified IIC10 and IIC20 functions

<1> After reset release, the port mode is the input mode (Hi-Z).

<2> Externally pull up the pin to be used (on-chip pull-up resistor cannot be used).

In case of simplified IIC10: P03, P04
In case of simplified IIC20: P142, P143

<3> Set the output latch of the corresponding port to 1.

<4> Set the corresponding bit of the POMn register to 1 to set the N-ch open drain output (V_{DD} withstand voltage) mode.

<5> Set the corresponding bit of the PMn register to the output mode (data I/O is possible in the output mode). At this time, the output data is high level, so the pin is in the Hi-Z state.

<6> Enable the operation of the serial array unit and set the mode to the simplified IIC mode.

Remark n = 0, 14

6.5 Settings of Port Mode Register, and Output Latch When Using Alternate Function

To use the alternate function of a port pin, set the port mode register, and output latch as shown in Table 6-7 or Table 6-8.

Table 6-7. Settings of Port Mode Register, and Output Latch When Using Alternate Function (78K0R/KF3-L) (1/2)

Pin Name	Alternate Function		PM××	P××	Pin Name	Alternate Function		PM××	P××
	Function Name	I/O				Function Name	I/O		
P02	SO10	Output	0	1	P40	TOOL0	I/O	×	×
	TxD1	Output	0	1	P41	TOOL1	Output	×	×
P03	SI10	Input	1	×	P42	TI04	Input	1	×
	RxD1	Input	1	×		TO04	Output	0	0
	SDA10	I/O	0	1	P43	$\overline{\text{SCK01}}$	Input	1	×
P04	$\overline{\text{SCK10}}$	Input	1	×			Output	0	1
		Output	0	1	P44	SI01	Input	1	×
	SCL10	I/O	0	1	P45	SO01	Output	0	1
P05, P06	TI05, TI06	Input	1	×	P50	$\overline{\text{SCK40}}$	Input	1	×
	TO05, TO06	Output	0	0			Output	0	1
P10	$\overline{\text{SCK00}}$	Input	1	×		INTP1	Input	1	×
		Output	0	1	P51	SI40	Input	1	×
P11	SI00	Input	1	×		RxD4	Input	1	×
	RxD0	Input	1	×		INTP2	Input	1	×
P12	SO00	Output	0	1	P52	SO40	Output	0	1
	TxD0	Output	0	1		TxD4	Output	0	1
P13	TxD3	Output	0	1		TO00	Output	0	0
P14	RxD3	Input	1	×	P53	$\overline{\text{SCK41}}$	Input	1	×
P15	RTCDIV	Output	0	0			Output	0	1
	RTCCL	Output	0	0		TI00	Input	1	×
P16	TI01	Input	1	×	P54	SI41	Input	1	×
	TO01	Output	0	0		TI07	Input	1	×
	INTP5	Input	1	×		TO07	Output	0	0
P17	TI02	Input	1	×	P55	SO41	Output	0	1
	TO02	Output	0	0		PCLBUZ1	Output	0	0
P20 to P27[Note]	ANI0 to ANI7[Note]	Input	1	×		INTP7	Input	1	×
P30	RTC1HZ	Output	0	0	P60	SCL0	I/O	0	0
	INTP3	Input	1	×	P61	SDA0	I/O	0	0
P31	TI03	Input	1	×	P64 to P67	TI10 to TI13	Input	1	×
	TO03	Output	0	0		TO10 to TO13	Output	0	0
	INTP4	Input	1	×	P70 to P73	KR0 to KR3	Input	1	×

Remark ×: don't care
PM××: Port mode register
P××: Port output latch

(**Note** is listed on the next page.)

Table 6-7. Settings of Port Mode Register, and Output Latch When Using Alternate Function (78K0R/KF3-L) (2/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P74 to P77	INTP8 to INTP11	Input	1	×
	KR4 to KR7	Input	1	×
P120	INTP0	Input	1	×
	EXLVI	Input	1	×
P140	PCLBUZ0	Output	0	0
	INTP6	Input	1	×
P142	$\overline{\text{SCK20}}$	Input	1	×
		Output	0	1
	SCL20	I/O	0	1
P143	SI20	Input	1	×
	RxD2	Input	1	×
	SDA20	I/O	0	1
P144	SO20	Output	0	1
	TxD2	Output	0	1
P150 to P153Note	ANI8 to ANI11Note	Input	1	×

Note The functions of the ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI11/P153 pins can be selected by using the A/D port configuration register (ADPC), analog input channel specification register (ADS), and port mode registers 2, 15 (PM2, PM15).

ADPC Register	PM2 and PM15 Registers	ADS Register	ANI0/P20 to ANI7/P27, ANI8/P150 to ANI11/P153 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

Remark ×: don't care
PM××: Port mode register
P××: Port output latch

Table 6-8. Settings of Port Mode Register, and Output Latch When Using Alternate Function (78K0R/KG3-L)

Pin Name	Alternate Function		PMxx	Pxx	Pin Name	Alternate Function		PMxx	Pxx
	Function Name	I/O				Function Name	I/O		
P00	TI00	Input	1	×	P46	TI05	Input	1	×
P01	TO00	Output	0	0		TO05	Output	0	0
P02	SO10	Output	0	1		INTP1	Input	1	×
	TxD1	Output	0	1	P47	INTP2	Input	1	×
P03	SI10	Input	1	×	P50	$\overline{\text{SCK40}}$	Input	1	×
	RxD1	Input	1	×			Output	0	1
	SDA10	I/O	0	1	P51	SI40	Input	1	×
P04	$\overline{\text{SCK10}}$	Input	1	×		RxD4	Input	1	×
		Output	0	1	P52	SO40	Output	0	1
	SCL10	I/O	0	1		TxD4	Output	0	1
P10	$\overline{\text{SCK00}}$	Input	1	×	P53	$\overline{\text{SCK41}}$	Input	1	×
		Output	0	1	P54	SI41	Input	1	×
P11	SI00	Input	1	×	P55	SO41	Output	0	1
	RxD0	Input	1	×	P60	SCL0	I/O	0	0
P12	SO00	Output	0	1	P61	SDA0	I/O	0	0
	TxD0	Output	0	1	P64 to P67	TI10 to TI13	Input	1	×
P13	TxD3	Output	0	1		TO10 to TO13	Output	0	0
P14	RxD3	Input	1	×	P70 to P73	KR0 to KR3	Input	1	×
P15	RTCDIV	Output	0	0	P74 to P77	INTP8 to INTP11	Input	1	×
	RTCCL	Output	0	0		KR4 to KR7	Input	1	×
P16	TI01	Input	1	×	P120	INTP0	Input	1	×
	TO01	Output	0	0		EXLVI	Input	1	×
	INTP5	Input	1	×	P131	TI06	Input	1	×
P17	TI02	Input	1	×		TO06	Output	0	0
	TO02	Output	0	0	P140	PCLBUZ0	Output	0	0
P20 to P27[Note]	ANI0 to ANI7[Note]	Input	1	×		INTP6	Input	1	×
P30	RTC1HZ	Output	0	0	P141	PCLBUZ1	Output	0	0
	INTP3	Input	1	×		INTP7	Input	1	×
P31	TI03	Input	1	×	P142	$\overline{\text{SCK20}}$	Input	1	×
	TO03	Output	0	0			Output	0	1
	INTP4	Input	1	×		SCL20	I/O	0	1
P40	TOOL0	I/O	×	×	P143	SI20	Input	1	×
P41	TOOL1	Output	×	×		RxD2	Input	1	×
P42	TI04	Input	1	×		SDA20	I/O	0	1
	TO04	Output	0	0	P144	SO20	Output	0	1
P43	$\overline{\text{SCK01}}$	Input	1	×		TxD2	Output	0	1
		Output	0	1	P145	TI07	Input	1	×
P44	SI01	Input	1	×		TO07	Output	0	0
P45	SO01	Output	0	1	P150 to P157[Note]	ANI8 to ANI15[Note]	Input	1	×

Remark ×: don't care
PMxx: Port mode register
Pxx: Port output latch

(**Note** is listed on the next page.)

Note The functions of the ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI15/P157 pins can be selected by using the A/D port configuration register (ADPC), analog input channel specification register (ADS), and port mode registers 2, 15 (PM2, PM15).

ADPC Register	PM2 and PM15 Registers	ADS Register	ANI0/P20 to ANI7/P27, ANI8/P150 to ANI15/P157 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

6.6 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P10 is an output port, P11 to P17 are input ports (all pin statuses are high level), and the port latch value of port 1 is 00H, if the output of output port P10 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 1 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the 78K0R/KF3-L and 78K0R/KG3-L.

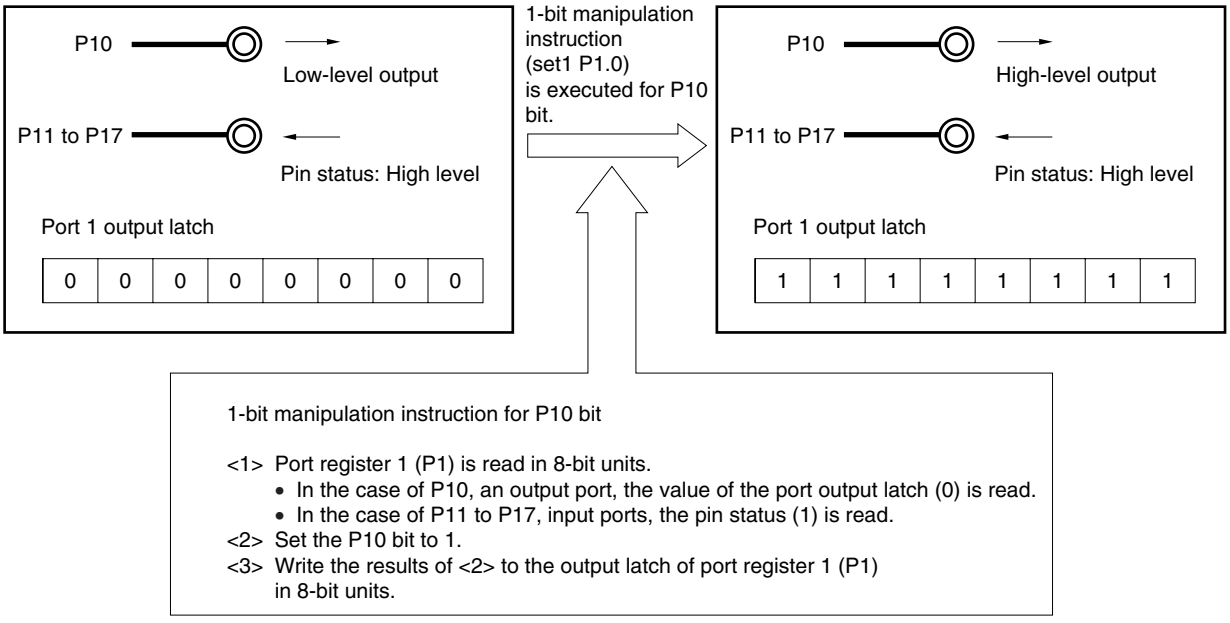
<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P10, which is an output port, is read, while the pin statuses of P11 to P17, which are input ports, are read. If the pin statuses of P11 to P17 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 6-61. Bit Manipulation Instruction (P10)



CHAPTER 7 CLOCK GENERATOR

7.1 Functions of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.
The following three kinds of system clocks and clock oscillators are selectable.

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 2 to 20 MHz by connecting a resonator to X1 and X2.
Oscillation can be stopped by executing the STOP instruction or setting of the MSTOP bit (bit 7 of the clock operation status control register (CSC)).

<2> Internal high-speed oscillator[Note]

This circuit oscillates clocks of f_{IH} = 1 and 8 MHz (TYP.). After a reset release, the CPU always starts operating with this internal high-speed oscillation clock. Oscillation can be stopped by executing the STOP instruction or setting the HIOSTOP bit (bit 0 of the CSC register).

<3> 20 MHz internal high-speed oscillation clock oscillator[Note]

This circuit oscillates a clock of f_{IH20} = 20 MHz (TYP.). Oscillation can be started by setting bit 0 (DSCON) of the 20 MHz internal high-speed oscillation control register (DSCCTL) to 1 with $V_{DD} \geq 2.7$ V. Oscillation can be stopped by setting the DSCON bit to 0.

Note To use the 1, 8, or 20 MHz internal high-speed oscillation clock, use the option byte to set the frequency in advance (for details, see **CHAPTER 25 OPTION BYTE**). Also, the internal high-speed oscillator automatically starts oscillating after reset release. To use the 20 MHz internal high-speed oscillator to operate the microcontroller, oscillation is started by setting bit 0 (DSCON) of the 20 MHz internal high-speed oscillation control register (DSCCTL) to 1.

An external main system clock (f_{EX} = 2 to 20 MHz) can also be supplied from the EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or setting of the MSTOP bit.
As the main system clock, a high-speed system clock (X1 clock or external main system clock) or internal high-speed oscillation clock can be selected by setting of the MCM0 bit (bit 4 of the system clock control register (CKC)).

(2) Subsystem clock[Note]

- **XT1 clock oscillator**

  This circuit oscillates a clock of f_{SUB} = 32.768 kHz by connecting a 32.768 kHz resonator to XT1 and XT2. Oscillation can be stopped by setting the XTSTOP bit (bit 6 of the clock operation status control register (CSC)).

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Remark f_X: X1 clock oscillation frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{IH20}: 20 MHz internal high-speed oscillation clock frequency
f_{EX}: External main system clock frequency
f_{SUB}: Subsystem clock frequency

(3) Internal low-speed oscillation clock (clock dedicated to watchdog timer)

- **Internal low-speed oscillator**

  This circuit oscillates a clock of f_{IL} = 30 kHz (TYP.).

  The internal low-speed oscillation clock cannot be used as the CPU clock. The only hardware that operates with the internal low-speed oscillation clock is the watchdog timer.

  Oscillation is stopped when the watchdog timer stops.

Remarks 1. f_{IL}: Internal low-speed oscillation clock frequency

2. The watchdog timer stops in the following cases.

- When bit 4 (WDTON) of an option byte (000C0H) = 0
- If the HALT or STOP instruction is executed when bit 4 (WDTON) of an option byte (000C0H) = 1 and bit 0 (WDSTBYON) = 0

7.2 Configuration of Clock Generator

The clock generator includes the following hardware.

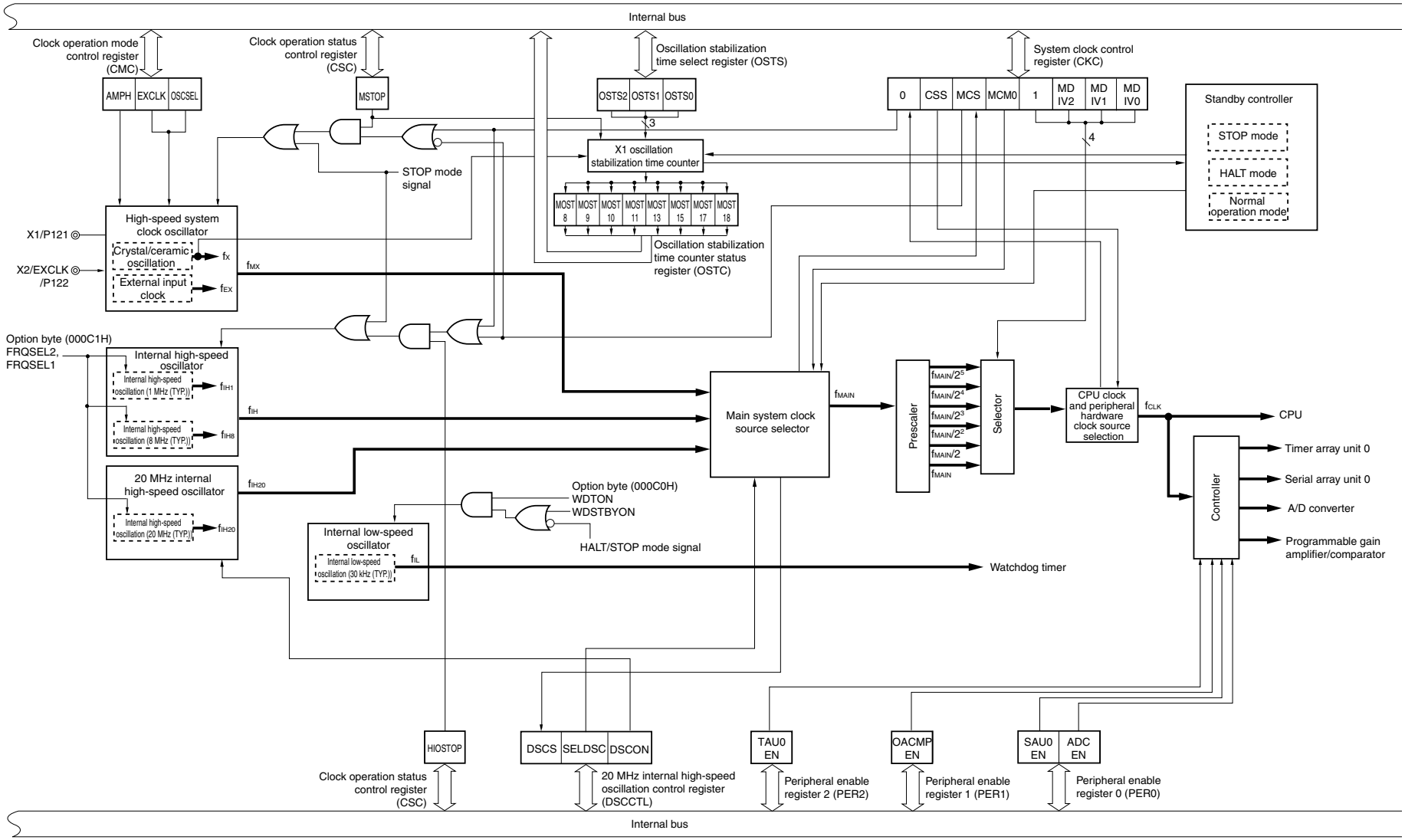
Table 7-1. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode control register (CMC) System clock control register (CKC) Clock operation status control register (CSC) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS) 20 MHz internal high-speed oscillation control register (DSCCTL) Peripheral enable registers 0, 1, 2 Note 1 (PER0, PER1, PER2 Note 1) Operation speed mode control register (OSMC)
Oscillators	X1 oscillator XT1 oscillator Note 2 Internal high-speed oscillator Internal low-speed oscillator

Notes 1. The PER2 register is only mounted in the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L.

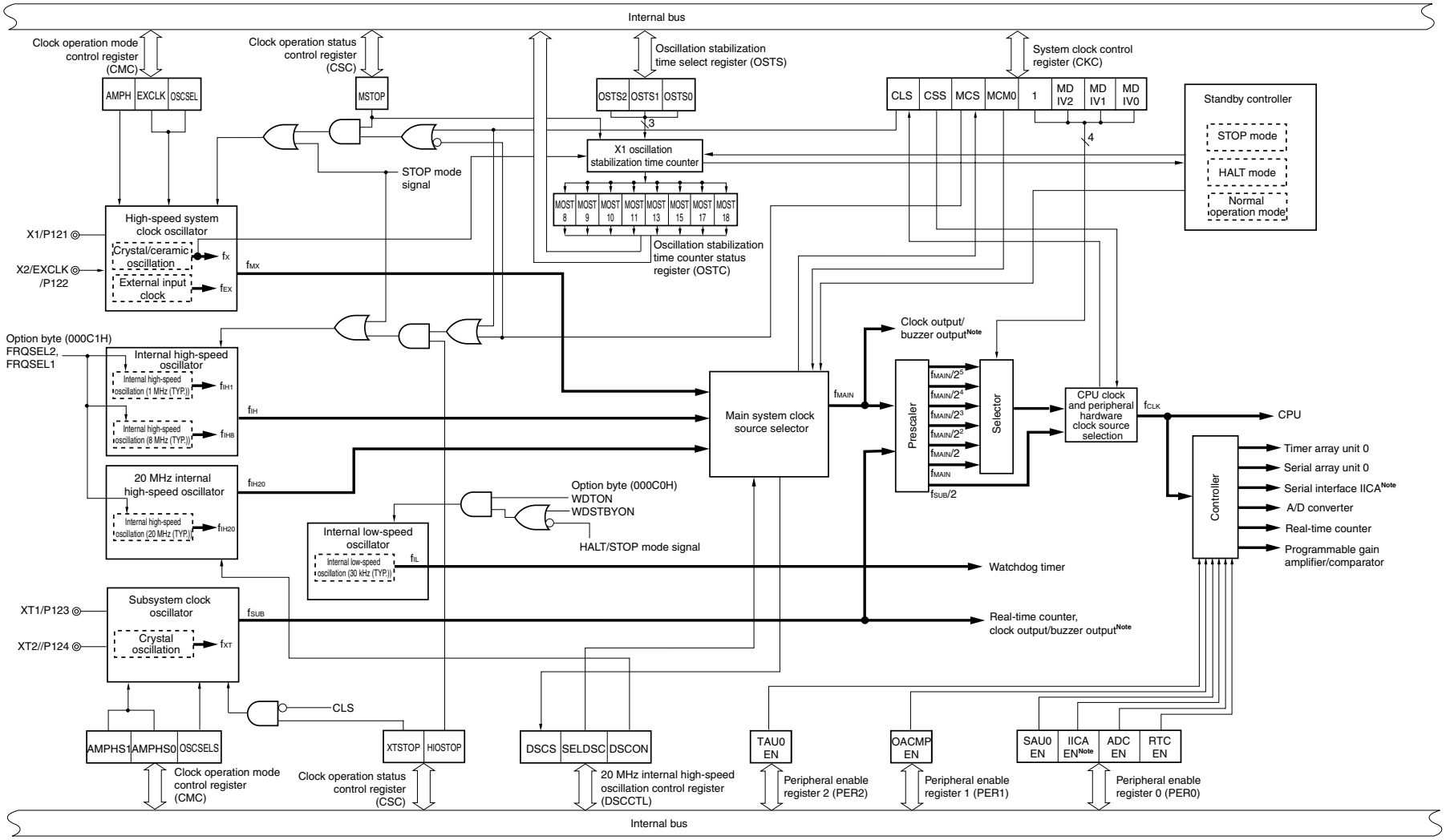
2. The 78K0R/KC3-L (40-pin) doesn't have the XT1 oscillator (subsystem clock).

Figure 7-1. Block Diagram of Clock Generator (78K0R/KC3-L (40-pin))



(**Remark** is listed on p.343 .)

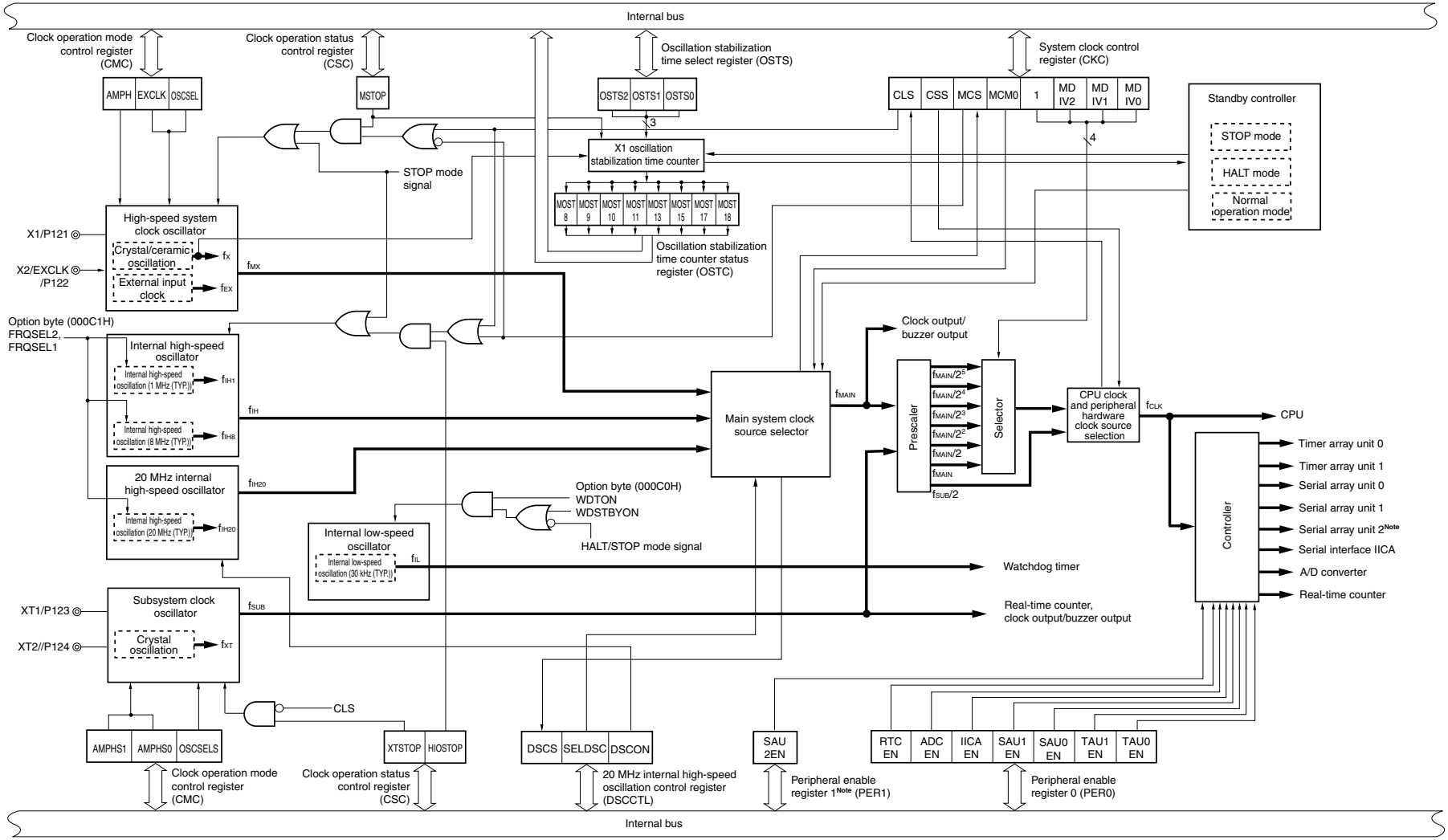
Figure 7-2. Block Diagram of Clock Generator (78K0R/KC3-L (44-pin and 48-pin), 78K0R/KD3-L, 78K0R/KE3-L)



Note This is not mounted onto 44-pin product of the 78K0R/KC3-L.

(**Remark** is listed on the next page after next.)

Figure 7-3. Block Diagram of Clock Generator (78K0R/KF3-L, 78K0R/KG3-L)



Note Those are are only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

(**Remark** is listed on the next page.)

Remark f_X: X1 clock oscillation frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{IH20}: 20 MHz internal high-speed oscillation clock frequency
f_{EX}: External main system clock frequency
f_{MX}: High-speed system clock frequency
f_{MAIN}: Main system clock frequency
f_{XT}: XT1 clock oscillation frequency
f_{SUB}: Subsystem clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency
f_{IL}: Internal low-speed oscillation clock frequency

7.3 Registers Controlling Clock Generator

The following eight registers are used to control the clock generator.

- Clock operation mode control register (CMC)
- System clock control register (CKC)
- Clock operation status control register (CSC)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)
- 20 MHz internal high-speed oscillation control register (DSCCTL)
- Peripheral enable registers 0, 1, 2Note (PER0, PER1, PER2Note)
- Operation speed mode control register (OSMC)

Note The PER2 register is only mounted in the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L.

(1) Clock operation mode control register (CMC)

This register is used to set the operation mode of the X1/P121, X2/EXCLK/P122, XT1/P123, and XT2/P124Note pins, and to select a gain of the oscillator.

The CMC register can be written only once by an 8-bit memory manipulation instruction after reset release. This register can be read by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Note The 78K0R/KC3-L (40-pin) doesn't have the XT1 and XT2 oscillator.

Figure 7-4. Format of Clock Operation Mode Control Register (CMC)

Address: FFFA0H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL	0	OSCSELS Note	0	AMPHS1	AMPHS0	AMPH

EXCLK	OSCSEL	High-speed system clock pin operation mode	X1/P121 pin	X2/EXCLK/P122 pin
0	0	Input port mode	Input port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

OSCSELS Note	Subsystem clock pin operation mode	XT1/P123 pin	XT2/P124 pin
0	Input port mode	Input port	
1	XT1 oscillation mode	Crystal resonator connection	

AMPHS1	AMPHS0	XT1 oscillator oscillation mode selection
0	0	Low power consumption oscillation (default)
0	1	Normal oscillation
1	0	Ultra-low power consumption oscillation
1	1	

AMPH	Control of X1 clock oscillation frequency
0	2 MHz ≤ f_X ≤ 10 MHz
1	10 MHz < f_X ≤ 20 MHz

Note OSCSELS bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), bit 4 is fixed to 0.

Cautions
1. **The CMC register can be written only once after reset release, by an 8-bit memory manipulation instruction.**
2. **After reset release, set the CMC register before X1 or XT1 oscillation is started as set by the clock operation status control register (CSC).**
3. **Be sure to set the AMPH bit to 1 if the X1 clock oscillation frequency exceeds 10 MHz.**
4. **When the CMC register is used at the default value (00H), be sure to set 00H to this register after reset release in order to prevent malfunctioning during a program loop.**
5. **The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption. Note the following points when designing the circuit.**
   - **Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.**
   - **When using the ultra-low power consumption oscillation (AMPHS1 = 1) as the mode of the XT1 oscillator, use the recommended resonators described in CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L).**

(Cautions and Remark are given on the next page.)

- **Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the ultra-low power consumption oscillation (AMPHS1 = 1) is selected.**
- **Configure the circuit of the circuit board, using material with little wiring resistance.**
- **Place a ground pattern that has the same potential as V_{SS} as much as possible near the XT1 oscillator.**
- **Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.**
- **When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.**

Remark fx: X1 clock frequency

(2) System clock control register (CKC)

This register is used to select a CPU/peripheral hardware clock and a division ratio.

The CKC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 09H.

Figure 7-5. Format of System Clock Control Register (CKC)

Address: FFFA4H After reset: 09H R/W[Note 1]

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
CKC	CLS[Note 2]	CSS	MCS	MCM0	1	MDIV2	MDIV1	MDIV0

CLS[Note 2]	Status of CPU/peripheral hardware clock (f_{CLK})
0	Main system clock (f_{MAIN})
1	Subsystem clock divided by 2 ($f_{SUB}/2$)

MCS	Status of Main system clock (f_{MAIN})
0	Internal high-speed oscillation clock (f_{IH}) or 20 MHz internal high-speed oscillation clock (f_{IH20})
1	High-speed system clock (f_{MX})

MCM0	Main system clock (f_{MAIN}) operation control
0	Selects the internal high-speed oscillation clock (f_{IH}) or 20 MHz internal high-speed oscillation clock (f_{IH20}) as the main system clock (f_{MAIN})
1	Selects the high-speed system clock (f_{MX}) as the main system clock (f_{MAIN})

CSS	MDIV2	MDIV1	MDIV0	Selection of CPU/peripheral hardware clock (f_{CLK})
0	0	0	0	f_{MAIN}
	0	0	1	$f_{MAIN}/2$ (This is the default setting if MCM0 = 0.)
	0	1	0	$f_{MAIN}/2^2$
	0	1	1	$f_{MAIN}/2^3$ [Note 3]
	1	0	0	$f_{MAIN}/2^4$ [Note 3]
	1	0	1	$f_{MAIN}/2^5$ [Notes 3, 4]
1 [Note 5]	×	×	×	$f_{SUB}/2$
Other than above				Setting prohibited

Notes 1. Bits 7 and 5 are read-only.

2. CLS bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), bit 7 is fixed to 0.

3. Setting is prohibited if the 1 MHz Internal high-speed oscillation clock frequency (f_{IH1}) is selected as the main system clock (f_{MAIN}).

4. Setting is prohibited if the high-speed system clock (f_{MX}) is selected as the main system clock (f_{MAIN}) and if $f_{MX} < 4$ MHz.

5. Changing the value of the MCM0 bit is prohibited while the CSS bit is set to 1.

(**Remarks** and **Cautions** are listed on the next page.)

Remarks 1. f_{IH}: Internal high-speed oscillation clock frequency
f_{IH20}: 20 MHz Internal high-speed oscillation clock frequency
f_{IH1}: 1 MHz Internal high-speed oscillation clock frequency
f_{MX}: High-speed system clock frequency
f_{SUB}: Subsystem clock frequency
2. ×: don't care

Cautions 1. Be sure to set bit 3 to 1.
2. The clock set by the CSS, MCM0, and MDIV2 bits to MDIV0 is supplied to the CPU and peripheral hardware. If the CPU clock is changed, therefore, the clock supplied to peripheral hardware (except the real-time counter, clock output/buzzer output, and watchdog timer) is also changed at the same time. Consequently, stop each peripheral function when changing the CPU/peripheral hardware clock.
3. If the subsystem clock is used as the peripheral hardware clock, the operations of the A/D converter and IICA are not guaranteed. For the operating characteristics of the peripheral hardware, refer to the chapters describing the various peripheral hardware as well as CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L).

The fastest instruction can be executed in 1 clock of the CPU clock in the 78K0R/Kx3-L. Therefore, the relationship between the CPU clock (f_{CLK}) and the minimum instruction execution time is as shown in Table 7-2.

Table 7-2. Relationship Between CPU Clock and Minimum Instruction Execution Time

CPU Clock (Value set by the MDIV2 to MDIV0 bits)	Minimum Instruction Execution Time: $1/f_{CLK}$				
	Main System Clock (CSS = 0)				Subsystem Clock [Note] (CSS = 1)
	High-Speed System Clock (MCM0 = 1)		Internal High-Speed Oscillation Clock (MCM0 = 0)		
	At 10 MHz Operation	At 20 MHz Operation	At 8 MHz (TYP.) Operation	At 20 MHz (TYP.) Operation	At 32.768 kHz Operation
f_{MAIN}	0.1 μs	0.05 μs	0.125 μs (TYP.)	0.05 μs (TYP.)	–
$f_{MAIN}/2$	0.2 μs	0.1 μs	0.25 μs (TYP.) (default)	0.1 μs (TYP.)	–
$f_{MAIN}/2^2$	0.4 μs	0.2 μs	0.5 μs (TYP.)	0.2 μs (TYP.)	–
$f_{MAIN}/2^3$	0.8 μs	0.4 μs	1.0 μs (TYP.)	0.4 μs (TYP.)	–
$f_{MAIN}/2^4$	1.6 μs	0.8 μs	2.0 μs (TYP.)	0.8 μs (TYP.)	–
$f_{MAIN}/2^5$	3.2 μs	1.6 μs	4.0 μs (TYP.)	1.6 μs (TYP.)	–
$f_{SUB}/2$	–		–		61 μs

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Remark f_{MAIN}: Main system clock frequency (f_{IH}, f_{IH20}, or f_{MX})
f_{SUB}: Subsystem clock frequency

(3) Clock operation status control register (CSC)

This register is used to control the operations of the high-speed system clock, internal high-speed oscillation clock, and subsystem clock[Note] (except the 20 MHz internal high-speed oscillation clock and internal low-speed oscillation clock).

The CSC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to C0H.

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Figure 7-5. Format of Clock Operation Status Control Register (CSC)

Address: FFFA1H After reset: C0H R/W

Symbol	<7>	<6>	5	4	3	2	1	<0>
CSC	MSTOP	XTSTOP[Note 1]	0	0	0	0	0	HIOSTOP

MSTOP	High-speed system clock operation control		
	X1 oscillation mode	External clock input mode	Input port mode
0	X1 oscillator operating	External clock from EXCLK pin is valid	Input port
1	X1 oscillator stopped	External clock from EXCLK pin is invalid	

XTSTOP[Note 1]	Subsystem clock operation control	
	XT1 oscillation mode	Input port mode
0	XT1 oscillator operating	Input port
1	XT1 oscillator stopped	

HIOSTOP	Internal high-speed oscillation clock operation control
0	Internal high-speed oscillator operating
1	Internal high-speed oscillator stopped [Note 2]

Notes 1. XTSTOP bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), bit 6 is fixed to 0.

2. The 1 MHz or 8 MHz (TYP.) internal high-speed oscillation clock stops. Stopping the internal high-speed oscillator (HIOSTOP = 1) is prohibited while the 20 MHz internal high-speed oscillation clock is operating (DSCON = 1). Stop the 20 MHz internal high-speed oscillation clock by using the 20 MHz internal high-speed oscillation control register (DSCCTL) and not the HIOSTOP bit.

Cautions 1. After reset release, set the clock operation mode control register (CMC) before setting the CSC register.

2. To start X1 oscillation as set by the MSTOP bit, check the oscillation stabilization time of the X1 clock by using the oscillation stabilization time counter status register (OSTC).

3. When starting XT1 oscillation by setting the XSTOP bit, wait for oscillation of the subsystem clock to stabilize by setting a wait time using software.

4. Do not stop the clock selected for the CPU peripheral hardware clock (f_{CLK}) with the OSC register.

5. The setting of the flags of the register to stop clock oscillation (invalidate the external clock input) and the condition before clock oscillation is to be stopped are as Table 7-3.

6. Set the oscillation stabilization time select register (OSTS) before setting the MSTOP bit to 0 after releasing reset. Note that if the OSTS register is being used with its default settings, the OSTS register is not required to be set here.

Table 7-3. Condition Before Stopping Clock Oscillation and Flag Setting

Clock	Condition Before Stopping Clock (Invalidating External Clock Input)	Setting of CSC Register Flags
X1 clock External main system clock	CPU and peripheral hardware clocks operate with a clock other than the high-speed system clock. (CLS = 0 and MCS = 0, or CLS = 1)	MSTOP = 1
Subsystem clock Note	CPU and peripheral hardware clocks operate with a clock other than the subsystem clock. (CLS = 0)	XTSTOP = 1
Internal high-speed oscillation clock	CPU and peripheral hardware clocks operate with a clock other than the internal high-speed oscillator clock and 20 MHz internal high-speed oscillation clock. (CLS = 0 and MCS = 1, or CLS = 1)	HIOSTOP = 1

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

(4) Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter.

The X1 clock oscillation stabilization time can be checked in the following case,

- If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating.

The OSTC register can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset signal is generated, the STOP instruction and MSTOP (bit 7 of clock operation status control register (CSC)) = 1 clear the OSTC register to 00H.

Remark The oscillation stabilization time counter starts counting in the following cases.

- When oscillation of the X1 clock starts (EXCLK, OSCSEL = 0, 1 → MSTOP = 0)
- When the STOP mode is released

Figure 7-7. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFFA2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18

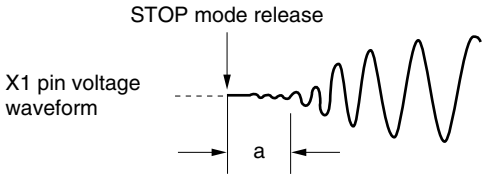
MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18	Oscillation stabilization time status		
									fx = 10 MHz	fx = 20 MHz
0	0	0	0	0	0	0	0	2^8/fx max.	25.6 μs max.	12.8 μs max.
1	0	0	0	0	0	0	0	2^8/fx min.	25.6 μs min.	12.8 μs min.
1	1	0	0	0	0	0	0	2^9/fx min.	51.2 μs min.	25.6 μs min.
1	1	1	0	0	0	0	0	2^{10}/fx min.	102.4 μs min.	51.2 μs min.
1	1	1	1	0	0	0	0	2^{11}/fx min.	204.8 μs min.	102.4 μs min.
1	1	1	1	1	0	0	0	2^{13}/fx min.	819.2 μs min.	409.6 μs min.
1	1	1	1	1	1	0	0	2^{15}/fx min.	3.27 ms min.	1.64 ms min.
1	1	1	1	1	1	1	0	2^{17}/fx min.	13.11 ms min.	6.55 ms min.
1	1	1	1	1	1	1	1	2^{18}/fx min.	26.21 ms min.	13.11 ms min.

Cautions 1. After the above time has elapsed, the bits are set to 1 in order from the MOST8 bit and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the oscillation stabilization time select register (OSTS).
In the following cases, set the oscillation stabilization time of the OSTS register to the value greater than the count value which is to be checked by the OSTC register after the oscillation starts.

- **If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock.**
- **If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating.**
(Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

(5) Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation automatically waits for the time set using the OSTS register after the STOP mode is released.

When the internal high-speed oscillation clock is selected as the CPU clock, confirm with the oscillation stabilization time counter status register (OSTC) that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using the OSTC register.

The OSTS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets the OSTS register to 07H.

Figure 7-8. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFFA3H After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				f_X = 10 MHz	f_X = 20 MHz
0	0	0	$2^8/f_X$	25.6 μs	Setting prohibited
0	0	1	$2^9/f_X$	51.2 μs	25.6 μs
0	1	0	$2^{10}/f_X$	102.4 μs	51.2 μs
0	1	1	$2^{11}/f_X$	204.8 μs	102.4 μs
1	0	0	$2^{13}/f_X$	819.2 μs	409.6 μs
1	0	1	$2^{15}/f_X$	3.27 ms	1.64 ms
1	1	0	$2^{17}/f_X$	13.11 ms	6.55 ms
1	1	1	$2^{18}/f_X$	26.21 ms	13.11 ms

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.

2. Setting the oscillation stabilization time to 20 μs or less is prohibited.

3. Change the setting of the OSTS register before setting the MSTOP bit of the clock operation status control register (CSC) to 0.

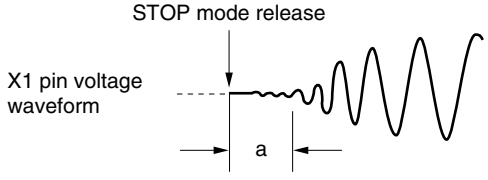
4. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

5. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the OSTS register.

In the following cases, set the oscillation stabilization time of the OSTS register to the value greater than the count value which is to be checked by the OSTC register after the oscillation starts.

- **If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock.**
- **If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating. (Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)**

6. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_X: X1 clock oscillation frequency

(6) 20 MHz internal high-speed oscillation control register (DSCCTL)

This register controls the 20 MHz internal high-speed oscillation clock (DSC) function.

This register can be used to control oscillation of the 20 MHz internal high-speed oscillation clock (f_{IH20}) and select the 20 MHz internal high-speed oscillation clock (f_{IH20}) as the CPU/peripheral hardware clock.

The DSCCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-9. Format of 20 MHz Internal High-Speed Oscillation Control Register (DSCCTL)

Address: F00F6H After reset: 00H R/W[Note]

Symbol	7	6	5	4	<3>	<2>	1	<0>
DSCCTL	0	0	0	0	DSCS	SELDSC	0	DSCON

DSCS	20 MHz internal high-speed oscillation supply status flag
0	Not supplied
1	Supplied (The CPU/peripheral hardware clock (f_{CLK}) operates on the 20 MHz internal high-speed oscillation clock.)

SELDSC	Selection of 20 MHz internal high-speed oscillation for CPU/peripheral hardware clock (f_{CLK})
0	Does not select 20 MHz internal high-speed oscillation (clock selected by the system clock control register (CKC) is supplied to f_{CLK})
1	Selects 20 MHz internal high-speed oscillation (20 MHz internal high-speed oscillation is supplied to f_{CLK})

DSCON	Operating or stopping 20 MHz internal high-speed oscillation clock (f_{IH20})
0	Stopped
1	Operated

Note Bit 3 is read-only.

Cautions 1. 20 MHz internal oscillation can only be used if $V_{DD} \geq 2.7$ V.

2. Set the SELDSC bit when 100 μs have elapsed after the DSCON bit has been set with $V_{DD} \geq 2.7$ V.

3. The internal high-speed oscillator must be operated (HIOSTOP = 0) when DSCON = 1.

4. If 1 MHz internal oscillation is selected by using the option byte, 20 MHz internal high-speed oscillation cannot be used. Do not set (1) the DSCON bit.

(7) Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2)

These registers are used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

The 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L include the PER0, PER1, and PER2 registers. The 78K0R/KF3-L and 78K0R/KG3-L, however, only include the PER0 and PER1[Note 1] registers. Note also that the bits incorporated in the PER0 register differ depending on the product.

To use the peripheral functions below, which are controlled by this register, set (1) the bit corresponding to each function before specifying the initial settings of the peripheral functions.

- Real-time counter[Note 2]
- A/D converter
- Serial interface IICA[Note 3]
- Serial array unit 0
- Serial array unit 1 [Note 4]
- Serial array unit 2 [Note 1]
- Timer array unit 0
- Timer array unit 1 [Note 4]
- Comparators/programmable gain amplifiers [Note 5]

The PER0, PER1, and PER2 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Notes 1. PER1 register is only mounted in the μPD78F1027 to 78F1030.

2. This is not mounted onto 40-pin product of the 78K0R/KC3-L.

3. This is not mounted onto 44-pin and 48-pin products of the 78K0R/KC3-L.

4. 78K0R/KF3-L, 78K0R/KG3-L only.

5. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only.

Figure 7-10. Format of Peripheral Enable Registers 0, 1, 2 (PER0, PER1, PER2) (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) (1/2)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	3	<2>	1	0
PER0	RTCEN Note 1	0	ADCEN	IICAEN Note 2	0	SAU0EN	0	0

Address: F00F1H After reset: 00H R/W

Symbol	7	6	5	4	<3>	2	1	0
PER1	0	0	0	0	OACMPEN	0	0	0

Address: F00F2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
PER2	0	0	0	0	0	0	0	TAU0EN

Bit 7 (PER0)

RTCEN Note 1	Control of real-time counter (RTC) input clock supply Note 3
0	Stops input clock supply. • SFR used by the real-time counter (RTC) cannot be written. • The real-time counter (RTC) is in the reset status.
1	Enables input clock supply. • SFR used by the real-time counter (RTC) can be read and written.

Bit 5 (PER0)

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFR used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFR used by the A/D converter can be read and written.

Bit 4 (PER0)

IICAEN Note 2	Control of serial interface IICA input clock supply
0	Stops input clock supply. • SFR used by the serial interface IICA cannot be written. • The serial interface IICA is in the reset status.
1	Enables input clock supply. • SFR used by the serial interface IICA can be read and written.

Notes 1. This is not mounted onto 40-pin product of the 78K0R/KC3-L.

2. This is not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.

3. The input clock that can be controlled by the RTCEN bit is used when the register that is used by the real-time counter (RTC) is accessed from the CPU. The RTCEN bit cannot control supply of the operating clock (f_{SUB}) to RTC.

Caution Be sure to clear bits 0, 1, 3, and 6 (40-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6, and 7, 44-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, and 6) of the PER0 register, bits 0 to 2 and 4 to 7 of the PER1 register, and bits 1 to 7 of the PER2 register to 0.

Figure 7-10. Format of Peripheral Enable Registers 0, 1, 2 (PER0, PER1, PER2)
(78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) (2/2)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	3	<2>	1	0
PER0	RTCEN Note 1	0	ADCEN	IICAEN Note 2	0	SAU0EN	0	0

Address: F00F1H After reset: 00H R/W

Symbol	7	6	5	4	<3>	2	1	0
PER1	0	0	0	0	OACMPEN	0	0	0

Address: F00F2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
PER2	0	0	0	0	0	0	0	TAU0EN

Bit 2 (PER0)

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 0 cannot be written. • The serial array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by the serial array unit 0 can be read and written.

Bit 3 (PER1)

OACMPEN	Control of comparator and programmable gain amplifier input clock supply
0	Stops input clock supply. • SFR used by the comparator and programmable gain amplifier cannot be written. • The comparator and programmable gain amplifier is in the reset status.
1	Enables input clock supply. • SFR used by the comparator and programmable gain amplifier can be read and written.

Bit 0 (PER2)

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by timer array unit 0 can be read and written.

Notes 1. This is not mounted onto 40-pin product of the 78K0R/KC3-L.

2. This is not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.

Caution Be sure to clear bits 0, 1, 3, and 6 (40-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6, and 7, 44-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, and 6) of the PER0 register, bits 0 to 2 and 4 to 7 of the PER1 register, and bits 1 to 7 of the PER2 register to 0.

Figure 7-11. Format of Peripheral Enable Registers 0 and 1 (PER0, PER1) (78K0R/KF3-L, 78K0R/KG3-L) (1/2)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN	0	ADCEN	IICAEN	SAU1EN	SAU0EN	TAU1EN	TAU0EN

Address: F00F1H After reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	0
PER1 Note 1	0	0	0	0	0	0	SAU2EN Note 1	0

RTCEN	Control of real-time counter (RTC) input clock supply Note 2
0	Stops input clock supply. • SFR used by the real-time counter (RTC) cannot be written. • The real-time counter (RTC) is in the reset status.
1	Supplies input clock. • SFR used by the real-time counter (RTC) can be read and written.

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFR used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Supplies input clock. • SFR used by the A/D converter can be read and written.

IICAEN	Control of serial interface IICA input clock supply
0	Stops input clock supply. • SFR used by the serial interface IICA cannot be written. • The serial interface IICA is in the reset status.
1	Supplies input clock. • SFR used by the serial interface IICA can be read and written.

SAU1EN Note 1	Control of serial array unit 1 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 1 cannot be written. • The serial array unit 1 is in the reset status.
1	Supplies input clock. • SFR used by the serial array unit 1 can be read and written.

Notes 1. PER1 register and SAU2EN bit are only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

2. The input clock that can be controlled by the RTCEN bit is used when the register that is used by the real-time counter (RTC) is accessed from the CPU. The RTCEN bit cannot control supply of the operating clock (f_{SUB}) to RTC.

Caution Be sure to clear bit 6 of the PER0 register and bits 0, and 2 to 7 of the PER1 register to 0.

Figure 7-11. Format of Peripheral Enable Registers 0 and 1 (PER0, PER1) (78K0R/KF3-L, 78K0R/KG3-L) (2/2)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN	0	ADCEN	IICAEN	SAU1EN	SAU0EN	TAU1EN	TAU0EN

Address: F00F1H After reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	0
PER1Note	0	0	0	0	0	0	SAU2ENNote	0

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 0 cannot be written. • The serial array unit 0 is in the reset status.
1	Supplies input clock. • SFR used by the serial array unit 0 can be read and written.

TAU1EN	Control of timer array unit 1 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 1 cannot be written. • Timer array unit 1 is in the reset status.
1	Supplies input clock. • SFR used by timer array unit 1 can be read and written.

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	Supplies input clock. • SFR used by timer array unit 0 can be read and written.

SAU2ENNote	Control of serial array unit 2 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 2 cannot be written. • The serial array unit 2 is in the reset status.
1	Supplies input clock. • SFR used by the serial array unit 2 can be read and written.

Note PER1 register is only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

Caution Be sure to clear bit 6 of the PER0 register and bits 0, and 2 to 7 of the PER1 register to 0.

(8) Operation speed mode control register (OSMC)

This register is used to reduce power consumption by stopping as many unnecessary clock functions as possible.

The FLPC and FSEL bits can be used to control the step-up circuit of the flash memory for high-speed operation.

If the microcontroller operates on a system clock of 10 MHz or more, set this register to 01B.

If the microcontroller operates at low speed on a system clock of 10 MHz or less, power consumption can be reduced, because the voltage booster can be stopped by setting this register to its initial value, 00B. Furthermore, when CPU operates with the system clock of 1 MHz, the power consumption can be further reduced by setting the FLPC bit to 1.

If the RTCLPC bit is set to 1 and real-time counter is operating, current consumption can be reduced, because the circuit that synchronizes the clock to the peripheral functions, except the real-time counter[Note 1], is stopped in STOP mode and in HALT mode while subsystem clock[Note 2] is selected as CPU clock.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Notes 1. 40-pin product of the 78K0R/KC3-L does not have real-time counter.

2. 40-pin product of the 78K0R/KC3-L does not have subsystem clock.

Figure 7-12. Format of Operation Speed Mode Control Register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	0	0	0	FLPC	FSEL

FLPC	FSEL	f_{CLK} frequency selection
0	0	Operates at a frequency of 10 MHz or less (default).
0	1	Operates at a frequency higher than 10 MHz.
1	0	Operates at a frequency of 1 MHz.
1	1	Setting prohibited

RTCLPC[Note]	Setting in STOP mode and in HALT mode while subsystem clock is selected as CPU clock
0	Enables supply of subsystem clock to peripheral functions (See Table 20-1 for peripheral functions whose operations are enabled.)
1	Stops supply of subsystem clock to peripheral functions other than real-time counter

Note 40-pin product of the 78K0R/KC3-L does not have RTCLPC bit. Be sure to clear RTCLPC bit to 0.

Cautions 1. Write "1" to the FSEL bit before the following two operations.
- **Changing the clock prior to dividing f_{CLK} to a clock other than f_{IH}.**
- **Operating the DMA controller.**

2. The CPU waits (140.5 clock (f_{CLK})) when "1" is written to the FSEL bit. Interrupt requests issued during a wait will be suspended. However, counting the oscillation stabilization time of f_X can continue even while the CPU is waiting.

3. To increase f_{CLK} to 10 MHz or higher, set the FSEL bit to "1", then change f_{CLK} after three or more clocks have elapsed.

4. To set the FSEL bit to 0, set f_{CLK} to 10 MHz or less in advance.

5. Set FSEL = 0 to shift to STOP mode while $V_{DD} \leq 2.7$ V.

(Cautions are given on the next page.)

6. **The HALT mode current when STOP mode and when the subsystem clock is used can be reduced by setting the RTCLPC bit to 1. However, no clock can be supplied to the peripheral functions other than the real-time counter during HALT mode while subsystem clock is selected as CPU clock. Set bit 7 (RTCEN) of peripheral enable registers 0 (PER0), to 1, and all of bits 0 to 6 of the PER0 register, bits 0 to 7 of peripheral enable register 1 (PER1), and bits 0 to 7 of peripheral enable register 2 (PER2) to 0 before setting subsystem clock HALT mode.**
7. **If the FLPC bit is set to a frequency of 1 MHz or less and then set (1), it cannot be cleared (0) or set to a frequency of more than 1 MHz.**

7.4 System Clock Oscillator

7.4.1 X1 oscillator

The X1 oscillator oscillates with a crystal resonator or ceramic resonator (2 to 20 MHz) connected to the X1 and X2 pins.

An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

To use the X1 oscillator, set bits 7 and 6 (EXCLK, OSCSEL) of the clock operation mode control register (CMC) as follows.

- Crystal or ceramic oscillation: EXCLK, OSCSEL = 0, 1
- External clock input: EXCLK, OSCSEL = 1, 1

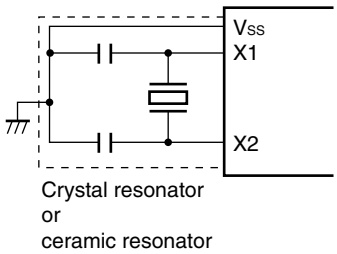
When the X1 oscillator is not used, set the input port mode (EXCLK, OSCSEL = 0, 0).

When the pins are not used as input port pins, either, see **Table 2-3 Connection of Unused Pins (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)** or **Table 3-3 Connection of Unused Pins (78K0R/KF3-L, 78K0R/KG3-L)**.

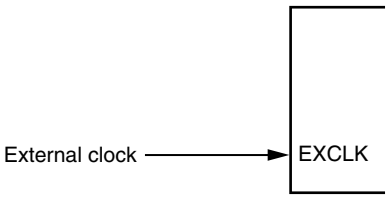
Figure 7-13 shows an example of the external circuit of the X1 oscillator.

Figure 7-13. Example of External Circuit of X1 Oscillator

(a) Crystal or ceramic oscillation



(b) External clock



Cautions are listed on the next page.

7.4.2 XT1 oscillator (products other than 78K0R/KC3-L (40-pin))

The XT1 oscillator oscillates with a crystal resonator (standard: 32.768 kHz) connected to the XT1 and XT2 pins.

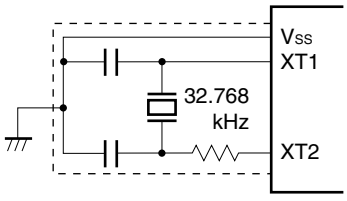
To use the XT1 oscillator, set bit 4 (OSCSELS) of the clock operation mode control register (CMC) to 1.

When the XT1 oscillator is not used, set the input port mode (OSCSELS = 0).

When the pins are not used as input port pins, either, see **Table 2-3 Connection of Unused Pins (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)** or **Table 3-3 Connection of Unused Pins (78K0R/KF3-L, 78K0R/KG3-L)**.

Figure 7-14 shows an example of the external circuit of the XT1 oscillator.

Figure 7-14. Example of External Circuit of XT1 Oscillator (Crystal Oscillation)



(Cautions are listed on the next page.)

Caution 1. When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in the Figures 7-13 and 7-14 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

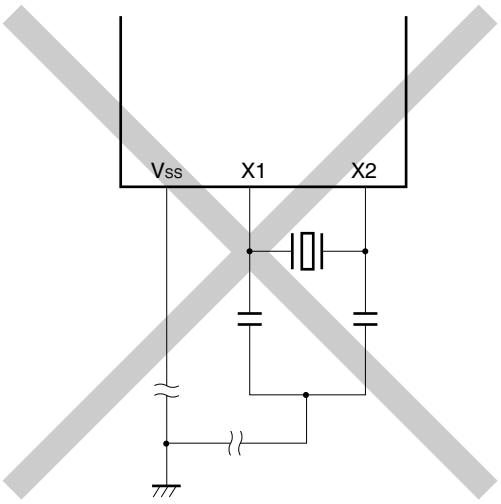
The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption. Note the following points when designing the circuit.

- **Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.**
- **When using the ultra-low power consumption oscillation (AMPHS1 = 1) as the mode of the XT1 oscillator, use the recommended resonators described in CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L).**
- **Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the ultra-low power consumption oscillation (AMPHS1 = 1) is selected.**
- **Configure the circuit of the circuit board, using material with little wiring resistance.**
- **Place a ground pattern that has the same potential as V_{SS} as much as possible near the XT1 oscillator.**
- **Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.**
- **When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.**

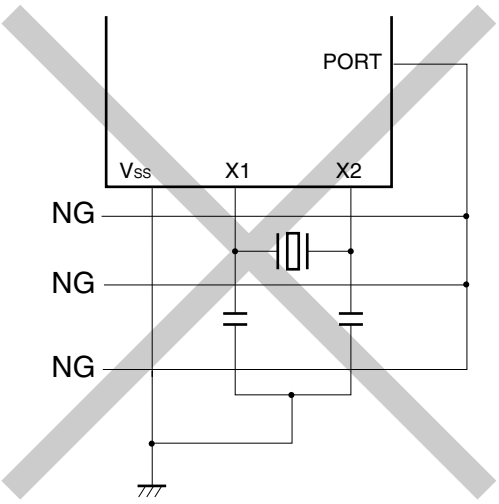
Figure 7-15 shows examples of incorrect resonator connection.

Figure 7-15. Examples of Incorrect Resonator Connection (1/2)

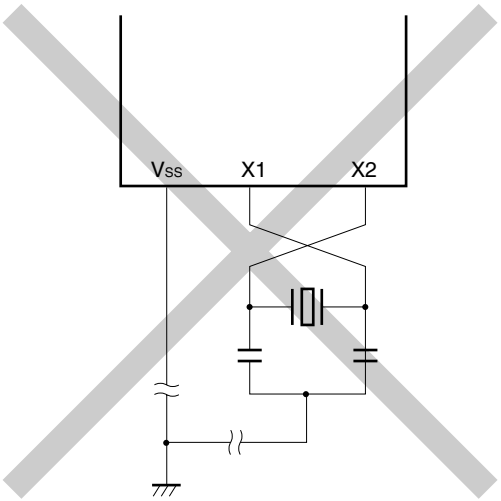
(a) Too long wiring



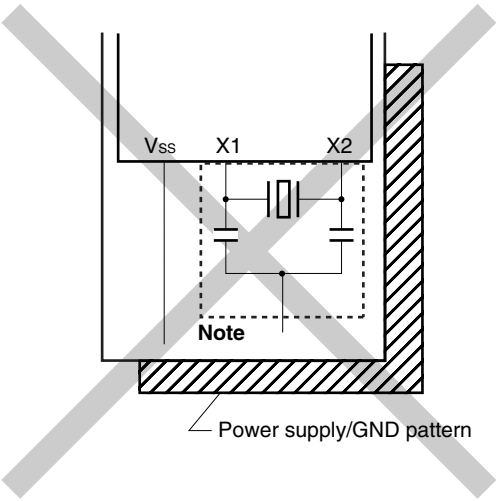
(b) Crossed signal line



(c) The X1 and X2 signal line wires cross.



(d) A power supply/GND pattern exists under the X1 and X2 wires.

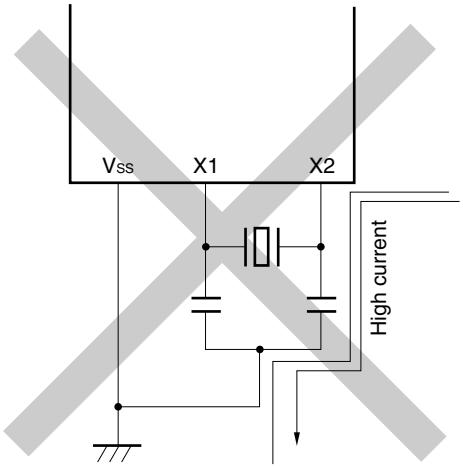


Note Do not place a power supply/GND pattern under the wiring section (section indicated by a broken line in the figure) of the X1 and X2 pins and the resonators in a multi-layer board or double-sided board.
Do not configure a layout that will cause capacitance elements and affect the oscillation characteristics.

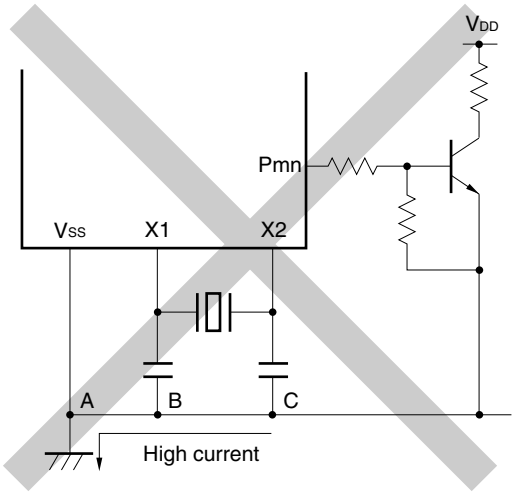
Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

Figure 7-15. Examples of Incorrect Resonator Connection (2/2)

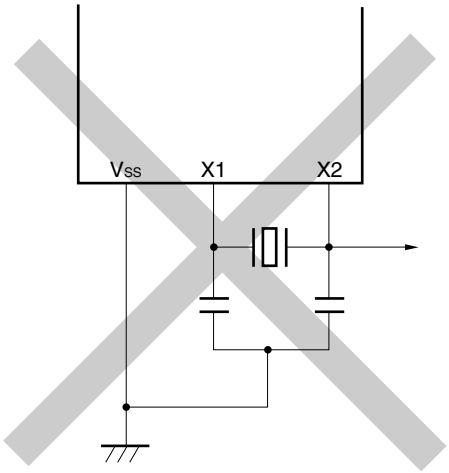
(e) Wiring near high alternating current



(f) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)



(g) Signals are fetched



Caution When X2 and XT1 are wired in parallel, the crosstalk noise of X2 may increase with XT1, resulting in malfunctioning.

Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

7.4.3 Internal high-speed oscillator

The internal high-speed oscillator is incorporated in the 78K0R/Kx3-L (1, 8 and 20 MHz (TYP.)). Oscillation can be controlled by bit 0 (HIOSTOP) of the clock operation status control register (CSC) and bit 0 (DSCON) of the 20 MHz internal high-speed oscillation control register (DSCCTL).

Caution To use the 1, 8, or 20 MHz internal high-speed oscillation clock, use the option byte to set the frequency in advance (for details, see CHAPTER 25 OPTION BYTE). Also, the internal high-speed oscillator automatically starts oscillating after reset release. (If 8 MHz or 20 MHz is selected by using the option byte, the microcontroller operates using the 8 MHz internal high-speed oscillator.) To use the 20 MHz internal high-speed oscillator to operate the microcontroller, oscillation is started by setting bit 0 (DSCON) of the DSCCTL register to 1 with $V_{DD} \geq 2.7$ V.

7.4.4 Internal low-speed oscillator

The internal low-speed oscillator is incorporated in the 78K0R/Kx3-L.

The internal low-speed oscillation clock is used only as the watchdog timer clock. The internal low-speed oscillation clock cannot be used as the CPU clock.

After a reset release, the internal low-speed oscillator automatically starts oscillation, and the watchdog timer is driven (30 kHz (TYP.)) if the watchdog timer operation is enabled by the option byte.

The internal low-speed oscillator continues oscillation except when the watchdog timer stops. When the watchdog timer operates, the internal low-speed oscillation clock does not stop, even in case of a program loop.

7.4.5 Prescaler

The prescaler generates a CPU/peripheral hardware clock by dividing the main system clock and subsystem clock.

7.5 Clock Generator Operation

The clock generator generates the following clocks and controls the operation modes of the CPU, such as standby mode (see **Figure 7-1 and 7-2**).

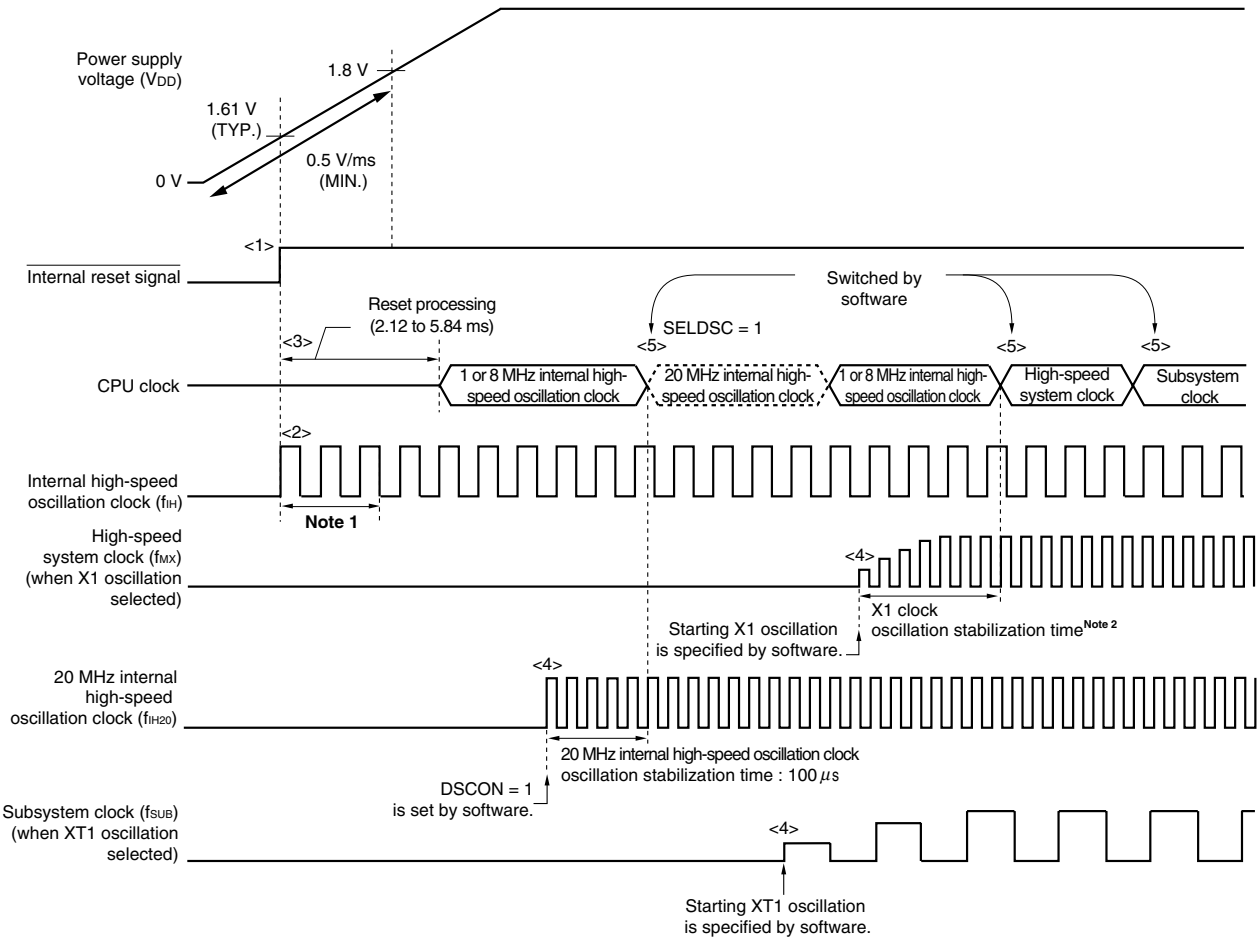
- Main system clock f_{MAIN}
  - High-speed system clock f_{MX}
    X1 clock f_X
    External main system clock f_{EX}
  - Internal high-speed oscillation clock f_{IH}
  - 20 MHz internal high-speed oscillation clock f_{IH20}
- Subsystem clock f_{SUB} Note
- Internal low-speed oscillation clock f_{IL}
- CPU/peripheral hardware clock f_{CLK}

Note The 78K0R/KC3-L(40-pin) doesn't have the XT1 oscillator (subsystem clock).

The CPU starts operation when the internal high-speed oscillator starts outputting after a reset release in the 78K0R/Kx3-L.

When the power supply voltage is turned on, the clock generator operation is shown in Figure 7-16 and Figure 7-17.

Figure 7-16. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Stopped Is Set (Option Byte: LVIOFF = 1))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 1.61 V (TYP.), the reset is released and the internal high-speed oscillator Note 3 automatically starts oscillation.

<3> The CPU starts operation on the internal high-speed oscillation clock Note 3 after a reset processing such as waiting for the voltage of the power supply or regulator to stabilize has been performed after reset release.

<4> Set the start of oscillation of the X1 or XT1 clock Note 4 via software (see **7.6.4 Example of setting X1 oscillation clock** and **7.6.5 Example of setting XT1 oscillation clock**).

Switch to oscillation using the 20 MHz internal high-speed oscillation clock after confirming that the power supply voltage is at least 2.7 V and setting the DSCON bit to 1 by using software.

<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see **7.6.4 Example of setting X1 oscillation clock** and **7.6.5 Example of setting XT1 oscillation clock**).

Switch to the 20 MHz internal high-speed oscillation clock by setting the DSCON bit (bit 0 of the 20 MHz internal high-speed oscillation control register (DSCCTL)), waiting for 100 μs, and then setting the SELDSC bit to 1 by using software Note 5.

(**Notes** and **Cautions** are listed on the next page.)

Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

2. When releasing a reset, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC).

3. The microcontroller operates on the 8 MHz internal high-speed oscillation clock if 8 MHz or 20 MHz is selected for the internal high-speed oscillator by using the option byte or on the 1 MHz internal high-speed oscillation clock if 1 MHz is selected.

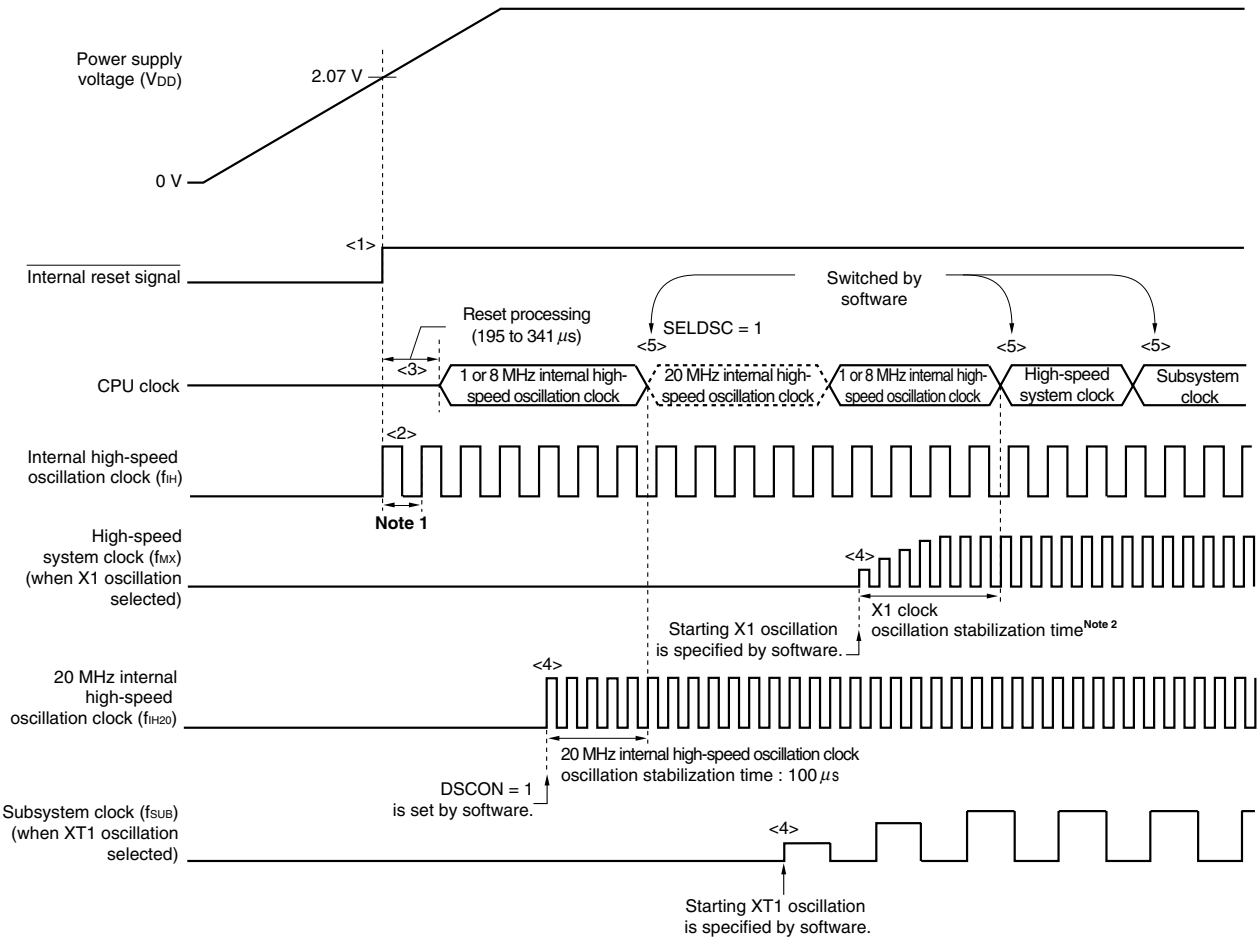
4. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

5. If the internal high-speed oscillator is set to 1 MHz by using the option byte, the 20 MHz internal high-speed oscillation clock cannot be used.

Cautions 1. If the voltage rises with a slope of less than 0.5 V/ms (MIN.) from power application until the voltage reaches 1.8 V, input a low level to the $\overline{\text{RESET}}$ pin from power application until the voltage reaches 1.8 V, or set the LVI default start function stopped by using the option byte (LVIOFF = 0) (see Figure 7-17). By doing so, the CPU operates with the same timing as <2> and thereafter in Figure 7-16 after reset release by the $\overline{\text{RESET}}$ pin.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

Figure 7-17. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Enabled Is Set (Option Byte: LVIOFF = 0))



<1> When the power is turned on, an internal reset signal is generated by the low-voltage detector (LVI) circuit.

<2> When the power supply voltage exceeds 2.07 V (TYP.), the reset is released and the internal high-speed oscillator Note 3 automatically starts oscillation.

<3> After the reset is released and reset processing is performed, the CPU starts operation on the internal high-speed oscillation clock Note 3.

<4> Set the start of oscillation of the X1 or XT1 clock Note 4 via software (see **7.6.4 Example of setting X1 oscillation clock** and **7.6.5 Example of setting XT1 oscillation clock**).

Switch to oscillation using the 20 MHz internal high-speed oscillation clock after setting the DSCON bit to 1 by using software.

<5> When switching the CPU clock to the X1 or XT1 clock Note 4, wait for the clock oscillation to stabilize, and then set switching via software (see **7.6.4 Example of setting X1 oscillation clock** and **7.6.5 Example of setting XT1 oscillation clock**).

Switch to the 20 MHz internal high-speed oscillation clock after confirming that the power supply voltage is at least 2.7 V, setting the DSCON bit (bit 0 of the 20 MHz internal high-speed oscillation control register (DSCCTL)), waiting for 100 μs, and then setting the SELDSC bit to 1 by using software Note 5.

(**Notes** and **Cautions** are listed on the next page.)

Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

2. When releasing a reset, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC).

3. The microcontroller operates on the 8 MHz internal high-speed oscillation clock if 8 MHz or 20 MHz is selected for the internal high-speed oscillator by using the option byte or on the 1 MHz internal high-speed oscillation clock if 1 MHz is selected.

4. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

5. If the internal high-speed oscillator is set to 1 MHz by using the option byte, the 20 MHz internal high-speed oscillation clock cannot be used.

Cautions 1. A voltage stabilization time (about 2.12 to 5.84 ms) is required after the supply voltage reaches 1.61 V (TYP.). If the time for the supply voltage to rise from 1.61 V (TYP.) to 2.07 V (TYP.) is shorter than the voltage stabilization time, reset processing is entered after the voltage stabilization time elapses.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

7.6 Controlling Clock

7.6.1 Example of setting 8 MHz internal high-speed oscillator

To use the 8 MHz internal high-speed oscillation clock as the CPU/peripheral hardware clock (f_{CLK}), set 000C1H of the option byte to FBH. Use the system clock control register (CKC) to specify the division ratio for the clock to be supplied to the CPU/peripheral hardware clock after releasing reset. When using the default division setting (f_{IH}/2 = 4 MHz), the CKC register is not required to be set.

[Option byte setting]

Set address 000C1H to FBH.

Option byte (000C1H)	7	6	5	4	3	2	1	0
	1	1	1	1	1	FRQSEL2	FRQSEL1	LVIOFF
						0	1	1

LVIOFF bit: Set this bit to 0 to turn on the LVI by default when releasing the power-on-reset.

[Register settings]

<1> Use the MDIV2 to MDIV0 bits of the CKC register to specify the division ratio for the CPU/peripheral hardware clock.

CKC	7	6	5	4	3	2	1	0
	CLS Note	CSS	MCS	MCM0		MDIV2	MDIV1	MDIV0
	0	0	0	0	1	0/1	0/1	0/1

Note CLS bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), be sure to clear CLS bit to 0.

7.6.2 Example of setting 1 MHz internal high-speed oscillator

To use the 1 MHz internal high-speed oscillation clock as the CPU/peripheral hardware clock (f_{CLK}), set 000C1H of the option byte to FDH. Use the system clock control register (CKC) to specify the division ratio for the clock to be supplied to the CPU/peripheral hardware clock after releasing reset. When using the default division setting (f_{IH}/2 = 0.5 MHz), the CKC register is not required to be set.

[Option byte setting]

Set address 000C1H to FDH.

Option byte (000C1H)	7	6	5	4	3	2	1	0
	1	1	1	1	1	FRQSEL2	FRQSEL1	LVIOFF
						1	0	1

LVIOFF bit: Set this bit to 0 to turn on the LVI by default when releasing the power-on-reset.

[Register settings]

<1> Use the MDIV2 to MDIV0 bits of the CKC register to specify the division ratio for the CPU/peripheral hardware clock.

CKC	7	6	5	4	3	2	1	0
	CLS Note	CSS	MCS	MCM0		MDIV2	MDIV1	MDIV0
	0	0	0	0	1	0/1	0/1	0/1

Note CLS bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), be sure to clear CLS bit to 0.

7.6.3 Example of setting 20 MHz internal high-speed oscillator

To use the 20 MHz internal high-speed oscillation clock as the CPU/peripheral hardware clock (f_{CLK}), set 000C1H of the option byte to FBH. After releasing reset, set the operation speed mode control register (OSMC) and then the 20 MHz internal high-speed oscillation control register (DSCCTL).

[Option byte setting]

Set address 000C1H to FBH.

Option byte (000C1H)

7	6	5	4	3	2	1	0
					FRQSEL2	FRQSEL1	LVIOFF
1	1	1	1	1	0	1	1

LVIOFF bit: Set this bit to 0 to turn on the LVI by default when releasing the power-on-reset.

[Register settings] Set the register in the order of <1> to <5> below.

<1> Set the OSMC register so that the microcontroller operates at a frequency exceeding 10 MHz.

OSMC

7	6	5	4	3	2	1	0
RTCLPC[Note]						FLPC	FSEL
0	0	0	0	0	0	0	1

RTCLPC bit[Note]: Set this bit to 1 to operate only the watch in sub-HALT mode (ultra-low current consumption).

Note RTCLPC bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), be sure to clear RTCLPC bit to 0.

<2> Set (1) the DSCON bit of the DSCCTL register to operate the 20 MHz internal high-speed oscillator.

DSCCTL

7	6	5	4	3	2	1	0
				DSCS	SELDSC		DSCON
0	0	0	0	0	0	0	1

<3> Set (1) the DSCON bit and then wait for 100 μs.

<4> Set (1) the SELDSC bit of the DSCCTL register to switch the internal high-speed oscillation clock from 8 MHz to 20 MHz.

DSCCTL

7	6	5	4	3	2	1	0
				DSCS	SELDSC		DSCON
0	0	0	0	0	1	0	1

<5> Use the MDIV2 to MDIV0 bits of the CKC register to specify the division ratio for the CPU/peripheral hardware clock.

CKC

7	6	5	4	3	2	1	0
CLS[Note]	CSS	MCS	MCM0		MDIV2	MDIV1	MDIV0
0	0	0	0	1	0/1	0/1	0/1

Note CLS bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), be sure to clear CLS bit to 0.

7.6.4 Example of setting X1 oscillation clock

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the internal high-speed oscillation clock. To subsequently change the clock to the X1 oscillation clock, set the oscillator and start oscillation by using the operation speed mode control register (OSMC), clock operation mode control register (CMC), and clock operation status control register (CSC) and wait for oscillation to stabilize by using the oscillation stabilization time counter status register (OSTC). After the oscillation stabilizes, set the X1 oscillation clock to f_{CLK} by using the system clock control register (CKC).

Set the frequency of the internal oscillation clock to be supplied immediately after releasing reset by using the option byte.

[Option byte setting]

Set address 000C1H to FBH.

Option byte (000C1H)

7	6	5	4	3	2	1	0
					FRQSEL2	FRQSEL1	LVIOFF
1	1	1	1	1	0	1	1

LVIOFF bit: Set this bit to 0 to turn on the LVI by default when releasing the power-on-reset.

FRQSEL2 and FRQSEL1 bits: Set the FRQSEL2 and FRQSEL1 bits to 1 and 0, respectively, to set the internal oscillation clock frequency to 1 MHz.

[Register settings] Set the register in the order of <1> to <5> below.

<1> Use the OSMC register to set the frequency of the CPU/peripheral hardware.

OSMC

7	6	5	4	3	2	1	0
RTCLPC[Note]						FLPC	FSEL
0	0	0	0	0	0	0	1

FSEL bit: Set this bit to 0 if the CPU/peripheral hardware clock is 10 MHz or less.

RTCLPC bit[Note]: Set this bit to 1 to operate only the watch in sub-HALT mode (ultra-low current consumption).

Note RTCLPC bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), be sure to clear RTCLPC bit to 0.

<2> Set (1) the OSCSEL bit of the CMC register to operate the X1 oscillator.

CMC

7	6	5	4	3	2	1	0
EXCLK	OSCSEL		OSCSELS[Note]		AMPHS1	AMPHS0	AMPH
0	1	0	0	0	0	0	1

AMPH bit: Set this bit to 0 if the X1 oscillation clock is 10 MHz or less.

OSCSELS bit[Note]: Set this bit to 1 to set P122 and P123 to XT1 oscillation mode.

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

Note OSCSELS bit is not provided in the 78K0R/KC3-L (40-pin).

<3> Clear (0) the MSTOP bit of the CSC register to start oscillating the X1 oscillator.

CSC

7	6	5	4	3	2	1	0
MSTOP	XTSTOP[Note]						HIOSTOP
0	1	0	0	0	0	0	0

XTSTOP bit[Note]: Set this bit to 0 to oscillate the XT1 oscillator.

Note XTSTOP bit is not provided in the 78K0R/KC3-L (40-pin).

<4> Use the OSTC register to wait for oscillation of the X1 oscillator to stabilize.

Example: Wait until the bits reach the following values when a wait of at least 102.4 μs is set based on a 10 MHz resonator.

	7	6	5	4	3	2	1	0
OSTC	MOST8	MOST9	MOST10	MOST11	MOST13	MOST15	MOST17	MOST18
	1	1	1	0	0	0	0	0

<5> Use the MCM0 bit of the CKC register to specify the X1 oscillation clock as the CPU/peripheral hardware clock.

Use the MDIV2 to MDIV0 bits to specify the division ratio.

	7	6	5	4	3	2	1	0
CKC	CLS[Note]	CSS	MCS	MCM0		MDIV2	MDIV1	MDIV0
	0	0	0	1	1	0/1	0/1	0/1

Note CLS bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), bit 7 is fixed to 0.

7.6.5 Example of setting XT1 oscillation clock (products other than 78K0R/KC3-L (40-pin))

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the internal high-speed oscillation clock. To subsequently change the clock to the XT1 oscillation clock, set the oscillator and start oscillation by using the operation speed mode control register (OSMC), clock operation mode control register (CMC), and clock operation status control register (CSC), set the XT1 oscillation clock to f_{CLK} by using the system clock control register (CKC).

Set the frequency of the internal oscillation clock to be supplied immediately after releasing reset by using the option byte.

[Option byte setting]

Set address 000C1H to FBH.

	7	6	5	4	3	2	1	0
Option byte (000C1H)						FRQSEL2	FRQSEL1	LVIOFF
	1	1	1	1	1	0	1	1

LVIOFF bit: Set this bit to 0 to turn on the LVI by default when releasing the power-on-reset.

FRQSEL2 and FRQSEL1 bits: Set the FRQSEL2 and FRQSEL1 bits to 1 and 0, respectively, to set the internal oscillation clock frequency to 1 MHz.

[Register settings] Set the register in the order of <1> to <5> below.

<1> Use the OSMC register to set the frequency of the CPU/peripheral hardware.

	7	6	5	4	3	2	1	0
OSMC	RTCLPC						FLPC	FSEL
	0	0	0	0	0	0	0	0

RTCLPC bit: Set this bit to 1 to operate only the watch in sub-HALT mode (ultra-low current consumption).

<2> Set (1) the OSCSELS bit of the CMC register to operate the XT1 oscillator.

	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL		OSCSELS		AMPHS1	AMPHS0	AMPH
	0	0	0	1	0	0/1	0/1	0

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

<3> Clear (0) the XTSTOP bit of the CSC register to start oscillating the XT1 oscillator.

	7	6	5	4	3	2	1	0
CSC	MSTOP	XTSTOP						HIOSTOP
	1	0	0	0	0	0	0	0

<4> Use the timer function or another function to wait for oscillation of the subsystem clock to stabilize by using software.

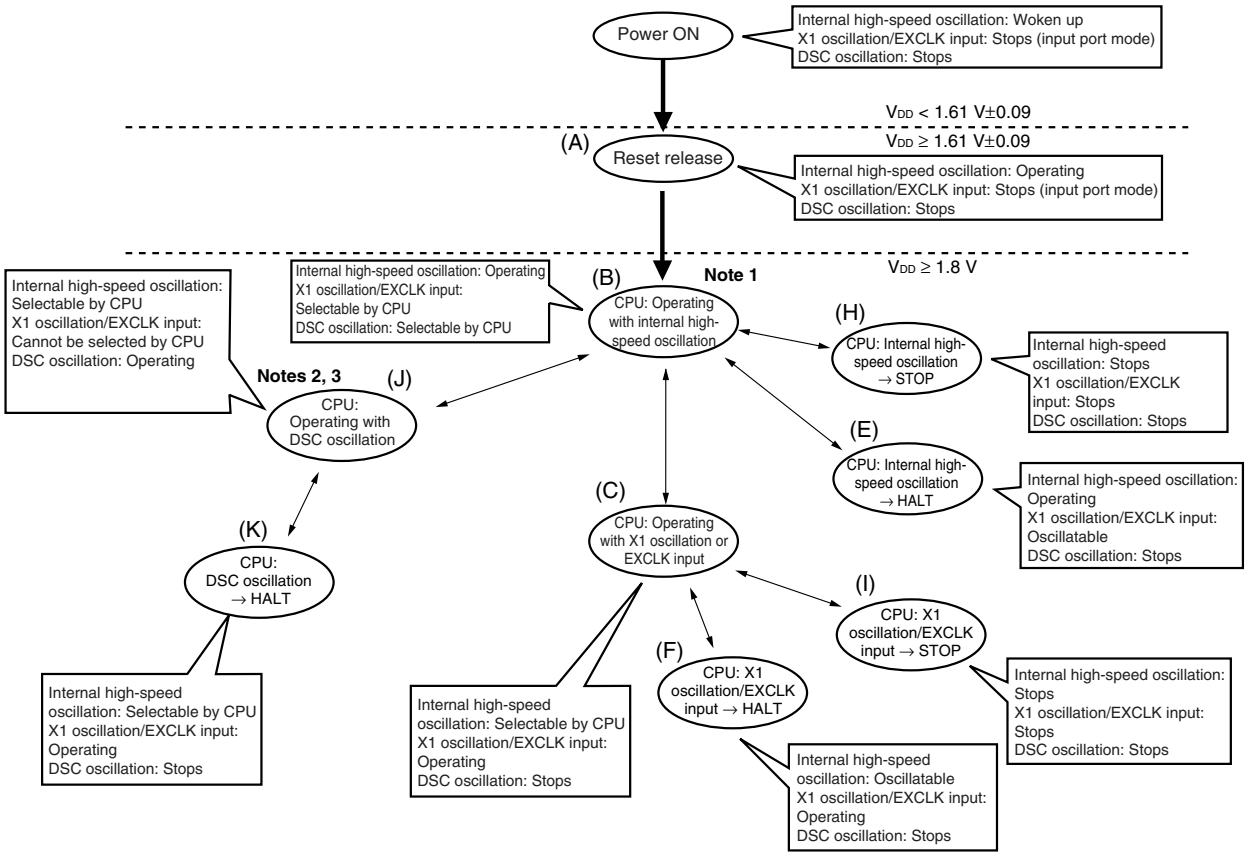
<5> Use the CSS bit of the CKC register to specify the XT1 oscillation clock as the CPU/peripheral hardware clock.

	7	6	5	4	3	2	1	0
CKC	CLS	CSS	MCS	MCM0		MDIV2	MDIV1	MDIV0
	0	1	0	0	1	0	0	0

7.6.6 CPU clock status transition diagram

Figure 7-18 and Figure 7-19 show the CPU clock status transition diagram of this product.

Figure 7-18. CPU Clock Status Transition Diagram (78K0R/KC3-L (40-pin))



Notes 1. After reset release, an operation at one of the following operating frequencies is started, because $f_{CLK} = f_{IH}/2$ has been selected by setting the system clock control register (CKC) to 09H.

- When 1 MHz has been selected by using the option byte: 500 kHz (1 MHz/2)
- When 8 MHz or 20 MHz has been selected by using the option byte: 4 MHz (8 MHz/2)

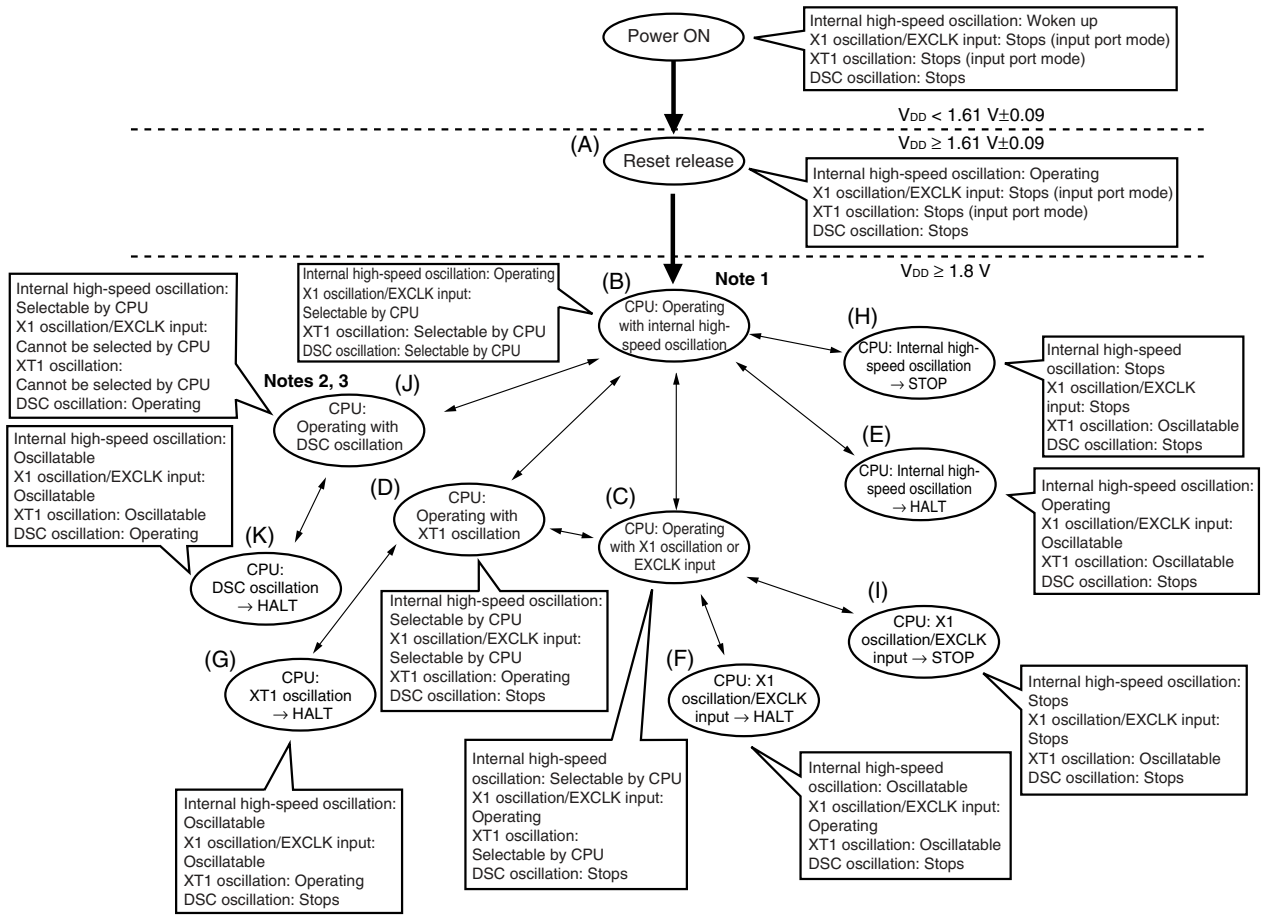
2. Specify 20 MHz internal oscillation after checking that V_{DD} is at least 2.7 V.

3. 20 MHz internal oscillation cannot be used if 1 MHz internal oscillation is selected by using the option byte.

Remarks 1. If the low-power-supply detector (LVI) is set to ON by default by the option bytes, the reset will not be released until the power supply voltage (V_{DD}) exceeds 2.07 V±0.2 V.
After the reset operation, the status will shift to (B) in the above figure.

2. DSC: 20 MHz internal high-speed oscillation clock

Figure 7-19. CPU Clock Status Transition Diagram (78K0R/KC3-L (44-pin, 48-pin), KD3-L, KE3-L, KF3-L, KG3-L)



Notes 1. After reset release, an operation at one of the following operating frequencies is started, because $f_{CLK} = f_{IH}/2$ has been selected by setting the system clock control register (CKC) to 09H.

- When 1 MHz has been selected by using the option byte: 500 kHz (1 MHz/2)
- When 8 MHz or 20 MHz has been selected by using the option byte: 4 MHz (8 MHz/2)

2. Specify 20 MHz internal oscillation after checking that V_{DD} is at least 2.7 V.

3. 20 MHz internal oscillation cannot be used if 1 MHz internal oscillation is selected by using the option byte.

Remarks 1. If the low-power-supply detector (LVI) is set to ON by default by the option bytes, the reset will not be released until the power supply voltage (V_{DD}) exceeds 2.07 V±0.2 V.
After the reset operation, the status will shift to (B) in the above figure.

2. DSC: 20 MHz internal high-speed oscillation clock

Table 7-4 shows transition of the CPU clock and examples of setting the SFR registers.

Table 7-4. CPU Clock Transition and SFR Register Setting Examples (1/6)

(1) CPU operating with internal high-speed oscillation clock (B) after reset release (A)

Status Transition	SFR Register Setting
(A) → (B)	SFR registers do not have to be set (default status after reset release).

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			CSC Register	OSMC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH	MSTOP	FSEL		MCM0
(A) → (B) → (C) (X1 clock: 2 MHz ≤ fx ≤ 10 MHz)	0	1	0	0	0	Must be checked	1
(A) → (B) → (C) (X1 clock: 10 MHz < fx ≤ 20 MHz)	0	1	1	0	1 Note 2	Must be checked	1
(A) → (B) → (C) (external main clock)	1	1	×	0	0/1 Note 2	Must not be checked	1

Notes 1. The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

2. FSEL = 1 when f_{CLK} > 10 MHz

If a divided clock is selected and f_{CLK} ≤ 10 MHz, use with FSEL = 0 is possible even if fx > 10 MHz.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)).

Remark ×: don't care

(3) CPU operating with subsystem clock (D) after reset release (A) (products other than 78K0R/KC3-L (40-pin))

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note			CSC Register	Waiting for Oscillation Stabilization	CKC Register
	OSCSELS	AMPHS1	AMPHS0	XTSTOP		CSS
(A) → (B) → (D)	1	0/1	0/1	0	Necessary	1

Note The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

Remark (A) to (K) in Table 7-4 correspond to (A) to (K) in Figure 7-19.

Table 7-4. CPU Clock Transition and SFR Register Setting Examples (2/6)

(4) CPU operating with 20 MHz internal high-speed oscillation clock (J) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	DSCCTL Register Note	Waiting for Oscillation Stabilization	DSCCTL Register
	DSCON		SELDSC
(A) → (B) → (J)	1	Necessary (100 μs)	1

Note Check that $V_{DD} \geq 2.7$ V and set DSCON = 1.

(5) CPU clock changing from internal high-speed oscillation clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			OSTS Register	CSC Register	OSMC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH		MSTOP	FSEL		MCM0
(B) → (C) (X1 clock: 2 MHz ≤ fX ≤ 10 MHz)	0	1	0	**Note 2**	0	0	Must be checked	1
(B) → (C) (X1 clock: 10 MHz < fX ≤ 20 MHz)	0	1	1	**Note 2**	0	1 Note 3	Must be checked	1
(B) → (C) (external main clock)	1	1	×	**Note 2**	0	0/1	Must not be checked	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Notes 1. The clock operation mode control register (CMC) can be changed only once after reset release. This setting is not necessary if it has already been set.

2. Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

3. FSEL = 1 when f_{CLK} > 10 MHz

If a divided clock is selected and $f_{CLK} \leq 10$ MHz, use with FSEL = 0 is possible even if f_X > 10 MHz.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)).

Remarks 1. ×: don't care

2. (A) to (K) in Table 7-4 correspond to (A) to (K) in Figure 7-19.

Table 7-4. CPU Clock Transition and SFR Register Setting Examples (3/6)

(6) CPU clock changing from internal high-speed oscillation clock (B) to subsystem clock (D) (products other than 78K0R/KC3-L (40-pin))

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register[Note]	CSC Register	Waiting for Oscillation Stabilization	CKC Register
	OSCSELS	XTSTOP		CSS
(B) → (D)	1	0	Necessary	1

Unnecessary if the CPU is operating with the subsystem clock

Note The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

(7) CPU clock changing from internal high-speed oscillation clock (B) to 20 MHz internal high-speed oscillation clock (J)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	DSCCTL Register[Note]	Waiting for Oscillation Stabilization	DSCCTL Register
	DSCON		SELDSC
(B) → (J)	1	Necessary (100 μs)	1

Unnecessary if the CPU is operating with the 20 MHz internal high-speed oscillation clock

Note Check that $V_{DD} \geq 2.7$ V and set DSCON = 1.

(8) CPU clock changing from high-speed system clock (C) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register	Oscillation accuracy stabilization time	CKC Register
	HIOSTOP		MCM0
(C) → (B)	0	10 μ s	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

Remark (A) to (K) in Table 7-4 correspond to (A) to (K) in Figure 7-19.

Table 7-4. CPU Clock Transition and SFR Register Setting Examples (4/6)

(9) CPU clock changing from high-speed system clock (C) to subsystem clock (D) (products other than 78K0R/KC3-L (40-pin))

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register	Waiting for Oscillation Stabilization	CKC Register
	XTSTOP		CSS
(C) → (D)	0	Necessary	1

Unnecessary if the CPU is operating with the subsystem clock

(10) CPU clock changing from subsystem clock (D) to internal high-speed oscillation clock (B) (products other than 78K0R/KC3-L (40-pin))

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register	CKC Register	
	HIOSTOP	MCM0	CSS
(D) → (B)	0	0	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

Unnecessary if this register is already set

Remark (A) to (K) in Table 7-4 correspond to (A) to (K) in Figure 7-19.

Table 7-4. CPU Clock Transition and SFR Register Setting Examples (5/6)

(11) CPU clock changing from subsystem clock (D) to high-speed system clock (C) (products other than 78K0R/KC3-L (40-pin))

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	OSTS Register	CSC Register	OSMC Register	OSTC Register	CKC Register	
		MSTOP	FSEL		MCM0	CSS
(D) → (C) (X1 clock: 2 MHz ≤ fx ≤ 10 MHz)	**Note 1**	0	0	Must be checked	1	0
(D) → (C) (X1 clock: 10 MHz < fx ≤ 20 MHz)	**Note 1**	0	1 Note 2	Must be checked	1	0
(D) → (C) (external main clock)	**Note 1**	0	0/1	Must not be checked	1	0

Unnecessary if the CPU is operating with the high-speed system clock

Unnecessary if these registers are already set

Notes 1. Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

2. FSEL = 1 when f_{CLK} > 10 MHz

If a divided clock is selected and f_{CLK} ≤ 10 MHz, use with FSEL = 0 is possible even if fx > 10 MHz.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)).

(12) CPU clock changing from 20 MHz internal high-speed oscillation clock (J) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	DSCCTL Register	
	SELDSC	DSCON
(J) → (B)	0	0

Remark (A) to (K) in Table 7-4 correspond to (A) to (K) in Figure 7-19.

Table 7-4. CPU Clock Transition and SFR Register Setting Examples (6/6)

(13) • HALT mode (E) set while CPU is operating with internal high-speed oscillation clock (B)
- **HALT mode (F) set while CPU is operating with high-speed system clock (C)**
- **HALT mode (G) set while CPU is operating with subsystem clock (D) (products other than 78K0R/KC3-L (40-pin))**
- **HALT mode (K) set while CPU is operating with 20 MHz internal high-speed oscillation clock (J)**

Status Transition	Setting
(B) → (E) (C) → (F) (D) → (G) (J) → (K)	Executing HALT instruction

(14) • STOP mode (H) set while CPU is operating with internal high-speed oscillation clock (B)
- **STOP mode (I) set while CPU is operating with high-speed system clock (C)**

(Setting sequence) ⟶

Status Transition		Setting		
(B) → (H)		Stopping peripheral functions that cannot operate in STOP mode	–	Executing STOP instruction
(C) → (I)	In X1 oscillation		Sets the OSTS register	
	External main system clock		–	

Remark (A) to (K) in Table 7-4 correspond to (A) to (K) in Figure 7-19.

7.6.7 Condition before changing CPU clock and processing after changing CPU clock

Condition before changing the CPU clock and processing after changing the CPU clock are shown below.

Table 7-5. Changing CPU Clock (1/2)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
Internal high-speed oscillation clock	X1 clock	Stabilization of X1 oscillation • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time	Operating current can be reduced by stopping internal high-speed oscillator (HIOSTOP = 1).
	External main system clock	Enabling input of external clock from the EXCLK pin • OSCSEL = 1, EXCLK = 1, MSTOP = 0	
	Subsystem clock Note	Stabilization of XT1 oscillation • OSCSELS = 1, XTSTOP = 0 • After elapse of oscillation stabilization time	
	20 MHz internal high-speed oscillation clock	Stabilization of DSC oscillation with 20 MHz set by using the option byte • $V_{DD} \geq 2.7$ V • After elapse of oscillation stabilization time (100 μs) after setting to DSCON = 1 • SELDSC = 1	–
X1 clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator • HIOSTOP = 0	X1 oscillation can be stopped (MSTOP = 1).
	External main system clock	Transition not possible (To change the clock, set it again after executing reset once.)	–
	Subsystem clock Note	Stabilization of XT1 oscillation • OSCSELS = 1, XTSTOP = 0 • After elapse of oscillation stabilization time	X1 oscillation can be stopped (MSTOP = 1).
	20 MHz internal high-speed oscillation clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–
External main system clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator • HIOSTOP = 0	External main system clock input can be disabled (MSTOP = 1).
	X1 clock	Transition not possible (To change the clock, set it again after executing reset once.)	–
	Subsystem clock Note	Stabilization of XT1 oscillation • OSCSELS = 1, XTSTOP = 0 • After elapse of oscillation stabilization time	External main system clock input can be disabled (MSTOP = 1).
	20 MHz internal high-speed oscillation clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Table 7-5. Changing CPU Clock (2/2)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
Subsystem clock[Note]	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator and selection of internal high-speed oscillation clock as main system clock • HIOSTOP = 0, MCS = 0	XT1 oscillation can be stopped (XTSTOP = 1)
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from the EXCLK pin and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	
	20 MHz internal high-speed oscillation clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–
20 MHz internal high-speed oscillation clock	Internal high-speed oscillation clock	• SELDSC = 0 (Set when changing the clock.)	20 MHz internal high-speed oscillation clock can be stopped (DSCON = 0)
	X1 clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–
	External main system clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–
	Subsystem clock[Note]	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

7.6.8 Time required for switchover of CPU clock and main system clock

By setting bits 0 to 2, 4, and 6 (MDIV0 to MDIV2, MCM0, CSS) of the system clock control register (CKC), the CPU clock can be switched (between the main system clock and the subsystem clock), main system clock can be switched (between the internal high-speed oscillation clock and the high-speed system clock), and the division ratio of the main system clock can be changed.

The actual switchover operation is not performed immediately after rewriting to the CKC register; operation continues on the pre-switchover clock for several clocks (see Table 7-6 to Table 7-9).

Whether the CPU is operating on the main system clock or the subsystem clock can be ascertained using bit 7 (CLS) of the CKC register. Whether the main system clock is operating on the high-speed system clock or internal high-speed oscillation clock can be ascertained using bit 5 (MCS) of the CKC register.

When the CPU clock is switched, the peripheral hardware clock is also switched.

Table 7-6. Maximum Time Required for Main System Clock Switchover

Clock A	Switching directions	Clock B	Remark
f_{MAIN}	←→ (changing the division ratio)	f_{MAIN}	See Table 7-7
f_{IH}	←→	f_{MX}	See Table 7-8
f_{MAIN}	←→	f_{SUB} Note	See Table 7-9

Table 7-7. Maximum Number of Clocks Required for f_{MAIN} ↔ f_{MAIN} (Changing the Division Ratio)

Set Value Before Switchover	Set Value After Switchover	
	Clock A	Clock B
Clock A		1 + f_A/f_B clock
Clock B	1 + f_B/f_A clock	

Table 7-8. Maximum Number of Clocks Required for f_{IH} ↔ f_{MX}

Set Value Before Switchover		Set Value After Switchover	
MCM0		MCM0	
		0 ($f_{MAIN} = f_{IH}$)	1 ($f_{MAIN} = f_{MX}$)
0 ($f_{MAIN} = f_{IH}$)	$f_{MX} \geq f_{IH}$		1 + f_{IH}/f_{MX} clock
	$f_{MX} < f_{IH}$		$2f_{IH}/f_{MX}$ clock
1 ($f_{MAIN} = f_{MX}$)	$f_{MX} \geq f_{IH}$	$2f_{MX}/f_{IH}$ clock	
	$f_{MX} < f_{IH}$	1 + f_{MX}/f_{IH} clock	

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

(**Remarks 1 and 2** are listed on the next page.)

Table 7-9. Maximum Number of Clocks Required for $f_{MAIN} \leftrightarrow f_{SUB}$ Note

Set Value Before Switchover	Set Value After Switchover	
CSS	CSS	
	0 ($f_{CLK} = f_{MAIN}$)	1 ($f_{CLK} = f_{SUB}$)
0 ($f_{CLK} = f_{MAIN}$)		1 + $2f_{MAIN}/f_{SUB}$ clock
1 ($f_{CLK} = f_{SUB}$)	2 + f_{SUB}/f_{MAIN} clock	

Remarks 1. The number of clocks listed in Table 7-7 to Table 7-9 is the number of CPU clocks before switchover.

2. Calculate the number of clocks in Table 7-7 to Table 7-9 by removing the decimal portion.

Example When switching the main system clock from the internal high-speed oscillation clock to the high-speed system clock (@ oscillation with f_{IH} = 8 MHz, f_{MX} = 10 MHz)

1 + f_{IH}/f_{MX} = 1 + 8/10 = 1 + 0.8 = 1.8 → 2 clocks

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

7.6.9 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

Table 7-10. Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
Internal high-speed oscillation clock	MCS = 1 or CLS = 1 (The CPU is operating on a clock other than the internal high-speed oscillation clock.)	HIOSTOP = 1
X1 clock External main system clock	MCS = 0 or CLS = 1 (The CPU is operating on a clock other than the high-speed system clock.)	MSTOP = 1
Subsystem clock Note	CLS = 0 (The CPU is operating on a clock other than the subsystem clock.)	XTSTOP = 1
20 MHz internal high-speed oscillation clock	SELDSC = 0 (The main system clock is operating on a clock other than the 20 MHz internal high-speed oscillation clock.)	DSCON = 0

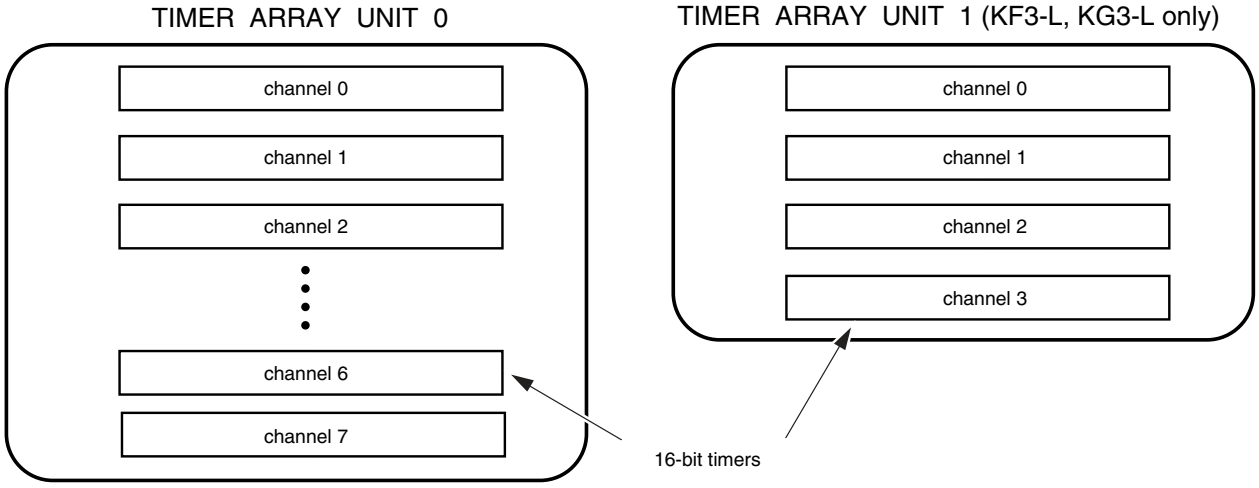
Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

CHAPTER 8 TIMER ARRAY UNIT

The 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L include a single timer array unit (timer array unit 0), whereas the 78K0R/KF3-L and 78K0R/KG3-L include two timer array units (timer array units 0 and 1).

The timer array unit 0 has eight 16-bit timers and the timer array unit 1 has four 16-bit timers.

Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more “channels” can be used to create a high-accuracy timer.



For details about each function, see the table below.

Independent channel operation function	Simultaneous channel operation function
• Interval timer (→ refer to 8.7.1) • Square wave output (→ refer to 8.7.1) • External event counter (→ refer to 8.7.2) • Divider function [Note] (→ refer to 8.7.3) • Input pulse interval measurement (→ refer to 8.7.4) • Measurement of high-/low-level width of input signal (→ refer to 8.7.5)	• One-shot pulse output(→ refer to 8.8.1) • PWM output(→ refer to 8.8.2) • Multiple PWM output(→ refer to 8.8.3)

Note Only channel 0 of timer array unit 0 in the 78K0R/KD3-L, 78K0R/KE3-L, 78K0R/KF3-L, and 78K0R/KG3-L.

Channel 7 of the unit 0 can be used to realize LIN-bus reception processing in combination with UART of the serial array unit.

The UART channel used for LIN-bus communication differs as follows depending on the product.

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: UART0 of the serial array unit 0
78K0R/KF3-L, 78K0R/KG3-L: UART3 of the serial array unit 1

8.1 Functions of Timer Array Unit

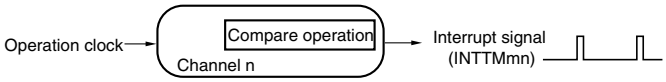
Timer array unit has the following functions.

8.1.1 Independent channel operation function

By operating a channel independently, it can be used for the following purposes without being affected by the operation mode of other channels.

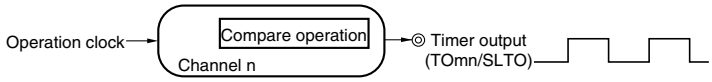
(1) Interval timer

Each timer of a unit can be used as a reference timer that generates an interrupt (INTTMmn) at fixed intervals.



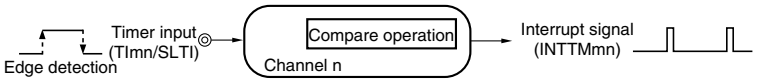
(2) Square wave output

A toggle operation is performed each time INTTMmn interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TOmn, SLTO).



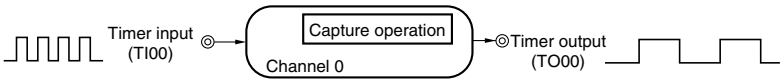
(3) External event counter

Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TImn, SLTI) has reached a specific value.



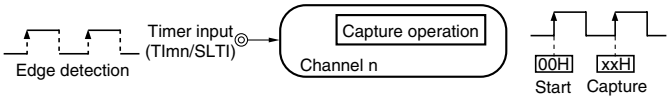
(4) Divider function [Note]

A clock input from a timer input pin (TI00) is divided and output from an output pin (TO00).



(5) Input pulse interval measurement

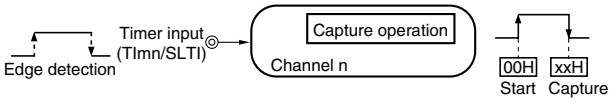
Counting is started by the valid edge of a pulse signal input to a timer input pin (TImn, SLTI). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.



(**Note**, **Caution,** and **Remark** are listed on the next page.)

(6) Measurement of high-/low-level width of input signal

Counting is started by a single edge of the signal input to the timer input pin (TImn, SLTI), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.



Note Only channel 0 of timer array unit 0 in the 78K0R/KD3-L, 78K0R/KE3-L, 78K0R/KF3-L, and 78K0R/KG3-L.

Caution Only the 78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, and 78K0R/KE3-L include the SLTI and SLTO pins.

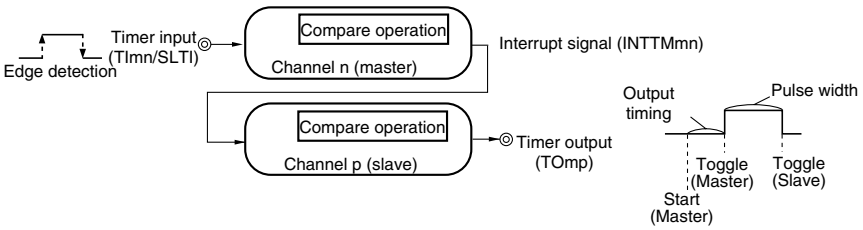
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn) and the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.1.2 Simultaneous channel operation function

By using the combination of a master channel (a reference timer mainly controlling the cycle) and slave channels (timers operating according to the master channel), channels can be used for the following purposes.

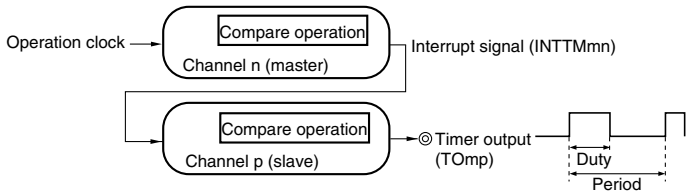
(1) One-shot pulse output

Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.



(2) PWM (Pulse Width Modulation) output

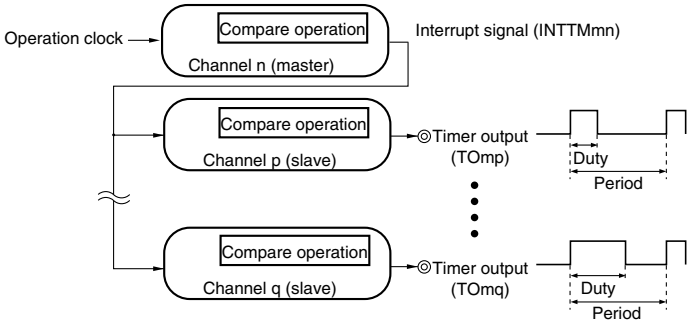
Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.



(**Cautions** and **Remark** are listed on the next page.)

(3) Multiple PWM (Pulse Width Modulation) output

By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.



Cautions 1. The following rules apply when using multiple channels simultaneously.

- **Only an even-numbered channel (channel 0, 2, 4, …) can be specified as the master channel.**
- **Only channels with lower channel numbers than the master channel can be specified as slave channels (multiple slave channels can be set).**

For details about the rules of simultaneous channel operation function, see 8.4 Basic Rules of Simultaneous Channel Operation Function.

2. Only the 78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, and 78K0R/KE3-L include the SLTI and SLTO pins.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number 1, q: Slave channel number 2[Note]
When m = 0: $n < p < q \leq 7$
When m = 1: $n < p < q \leq 3$
(Where p and q are a consecutive integer greater than n)

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

8.1.3 LIN-bus supporting function (channel 7 only)

Timer array unit 0 is used to check whether signals received in LIN-bus communication match the LIN-bus communication format.

(1) Detection of wakeup signal

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxDk) of UARTk and the count value of the timer is captured at the rising edge. In this way, a low-level width can be measured. If the low-level width is greater than a specific value, it is recognized as a wakeup signal.

(2) Detection of sync break field

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxDk) of UARTk after a wakeup signal is detected, and the count value of the timer is captured at the rising edge. In this way, a low-level width is measured. If the low-level width is greater than a specific value, it is recognized as a sync break field.

(3) Measurement of pulse width of sync field

After a sync break field is detected, the low-level width and high-level width of the signal input to the serial data input pin (RxDk) of UARTk are measured. From the bit interval of the sync field measured in this way, a baud rate is calculated.

Remarks 1. The UART channel used for LIN-bus communication differs as follows depending on the product.
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: k = 0 (UART0, RxD0 input pin)
78K0R/KF3-L, 78K0R/KG3-L: k = 3 (UART3, RxD3 input pin)

2. For details about setting up the operations used to implement the LIN-bus, see **8.3 (13) Input switch control register (ISC)** and **8.7.5 Operation as input signal high-/low-level width measurement**.

8.2 Configuration of Timer Array Unit

Timer array unit includes the following hardware.

Table 8-1. Configuration of Timer Array Unit

Item	Configuration	
	78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L	78K0R/KF3-L, 78K0R/KG3-L
Timer/counter	Timer/counter register mn (TCRmn)	
Register	Timer data register mn (TDRmn)	
Timer input	TI00 to TI07 (78K0R/KC3-L (40-pin) : TI02 to TI07), SLTI[Note 1] pins, RxD0 pin (for LIN-bus)	TI00 to TI07, TI10 to TI13, RxD3 pin (for LIN-bus)
Timer output	TO00 to TO07(78K0R/KC3-L (40-pin) : TO02 to TO07), SLTO[Note 1] pins, output controller	TO00 to TO07, TO10 to TO13, output controller
Control registers	<Registers of unit setting block> • Peripheral enable registers 0, 2 (PER0, PER2)[Note 2] • Timer clock select register m (TPSm) • Timer channel enable status register m (TEm) • Timer channel start register m (TSm) • Timer channel stop register m (TTm) • Timer input select register m (TISm) • Timer output enable register m (TOEm) • Timer output register m (TOm) • Timer output level register m (TOLm) • Timer output mode register m (TOMm)	
	<Registers of each channel> • Timer mode register mn (TMRmn) • Timer status register mn (TSRmn) • Input switch control register (ISC) • Noise filter enable registers 1, 2 (NFEN1, NFEN2) • Port mode register (PMxx)[Note 3] • Port register (Pxx)[Note 3]	

Notes 1. 40-pin product of the 78K0R/KC3-L does not have a SLTI and SLTO pins.

2. Set the PER2 register in the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L. Set the PER0 register in the 78K0R/KF3-L and 78K0R/KG3-L.

3. The port mode registers (PMxx) and port registers (Pxx) to be set differ depending on the product. for details, **see 8. 3 (15) Port mode registers 0, 1, 3 to 6, 13, 14 (PM0, PM1, PM3 to PM6, PM13, PM14).**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

The presence or absence of timer I/O pins in each timer array unit channel depends on the product.

Timer array unit channels		I/O Pins of Each Product						
		KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
TAU0	Channel 0	–			P00/TI00, P01/TO00		P52/TI00, P53/TO00	P00/TI00, P01/TO00
		–	P52/SLTI/SLTO Note					
	Channel 1	–	P52/SLTI/SLTO Note				P16/TI01/TO01	
	Channel 2	P10/TI02/TO02					P17/TI02/TO02	
	Channel 3	P11/TI03/TO03					P31/TI03/TO03	
	Channel 4	P12/TI04/TO04					P42/TI04/TO04	
	Channel 5	P13/TI05/TO05					P05/TI05/TO05	P46/TI05/TO05
	Channel 6	P50/TI06/TO06				P14/TI06/TO06	P06/TI06/TO06	P131/TI06/TO06
	Channel 7	P51/TI07/TO07				P15/TI07/TO07	P54/TI07/TO07	P145/TI07/TO07
TAU1	Channel 0	–					P64/TI10/TO10	
	Channel 1	–					P65/TI11/TO11	
	Channel 2	–					P66/TI12/TO12	
	Channel 3	–					P67/TI13/TO13	

Note In the 78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, and 78K0R/KE3-L, the P52/SLTI/SLTO pin can be used as the timer I/O pin of channels 0 and 1. When using channel 0 in the 78K0R/KD3-L and 78K0R/KE3-L, the input switch control register (ISC) can be used to select whether to use the P00/TI00, P01/TO00, and P52/SLTI/SLTO pins for timer I/O. For details about the ISC register, see **8.3 (13) Input switch control register (ISC)**.

Caution Hereinafter, the timer I/O pins are described as TImn and TOmn (n = x), which also includes the selection of the SLTI and SLTO pins.

Remarks 1. When timer input and timer output are shared by the same pin, either only timer input or only timer output can be used.

2. The P52/SLTI/SLTO pin can only be assigned as the timer I/O pin for either channel 0 or channel 1. The SLTI and SLTO pins cannot be selected as the timer I/O for channels 2 to 7.

Figures 8-1 to 8-5 show the block diagram.

Figure 8-1. Entire Configuration of Timer Array Unit 0 (78K0R/KC3-L (40-pin))

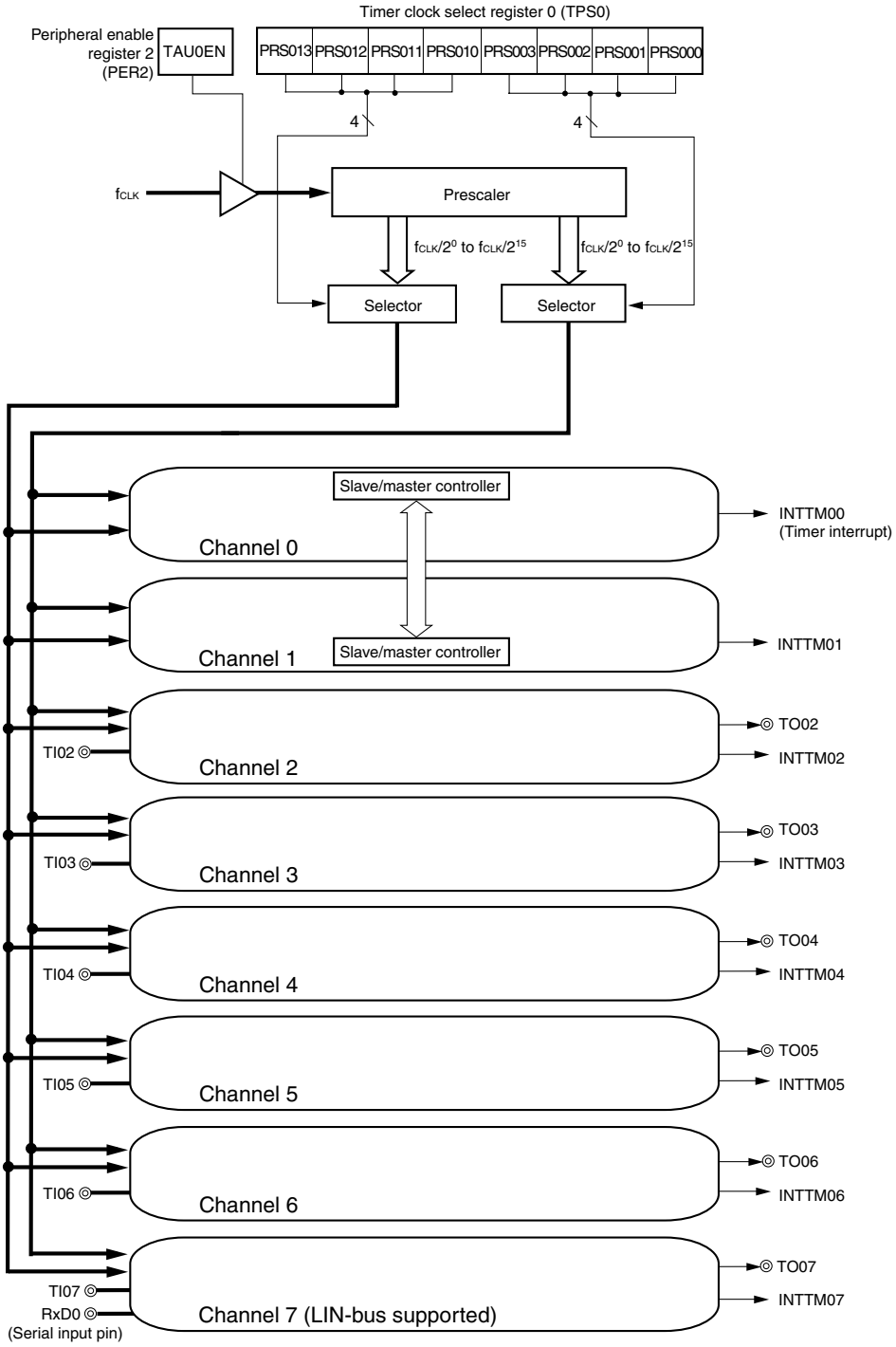
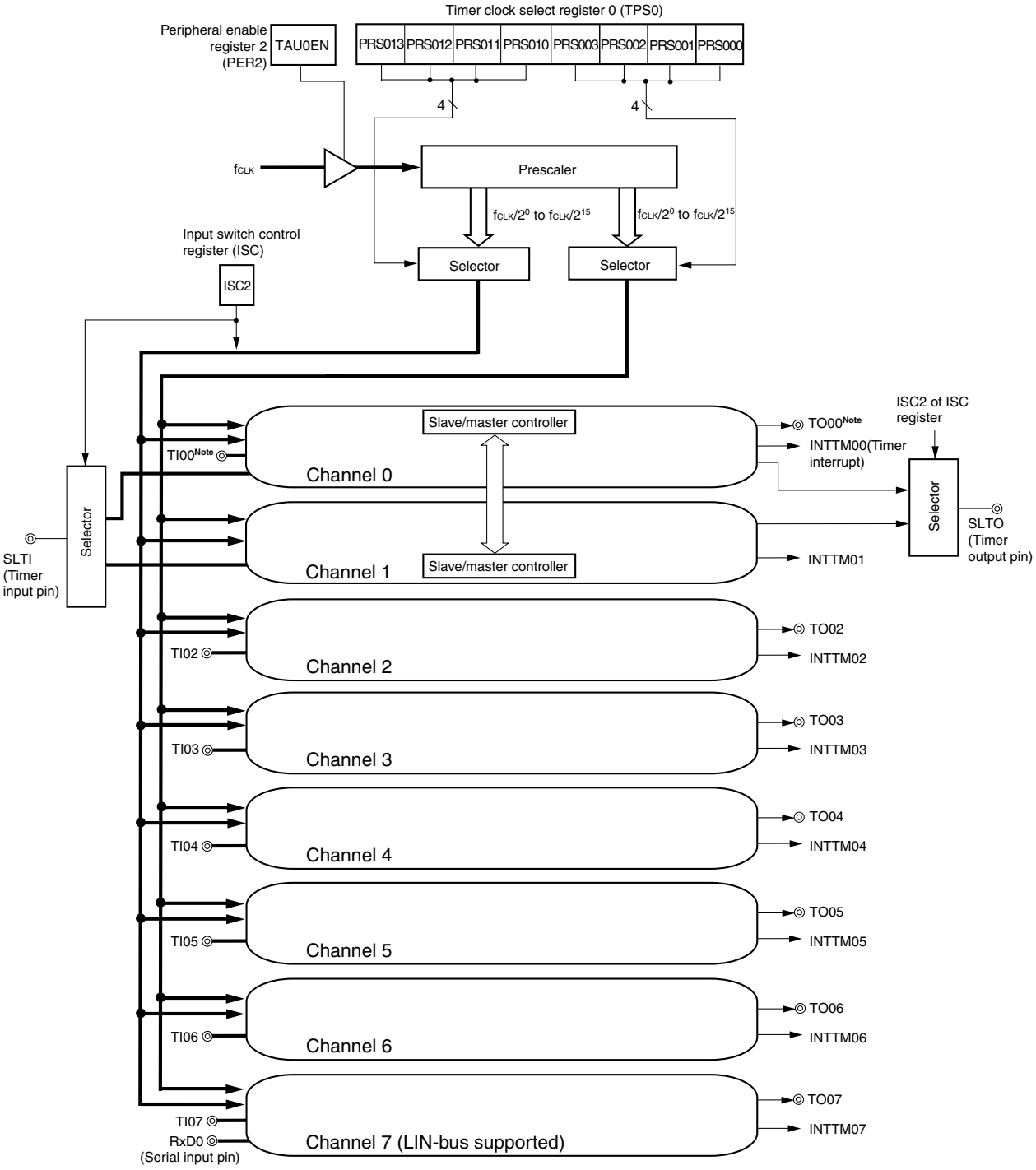


Figure 8-2. Entire Configuration of Timer Array Unit 0 (78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, 78K0R/KE3-L)



Note 78K0R/KD3-L and 78K0R/KE3-L only

Figure 8-3. Entire Configuration of Timer Array Unit 0 (78K0R/KF3-L, 78K0R/KG3-L)

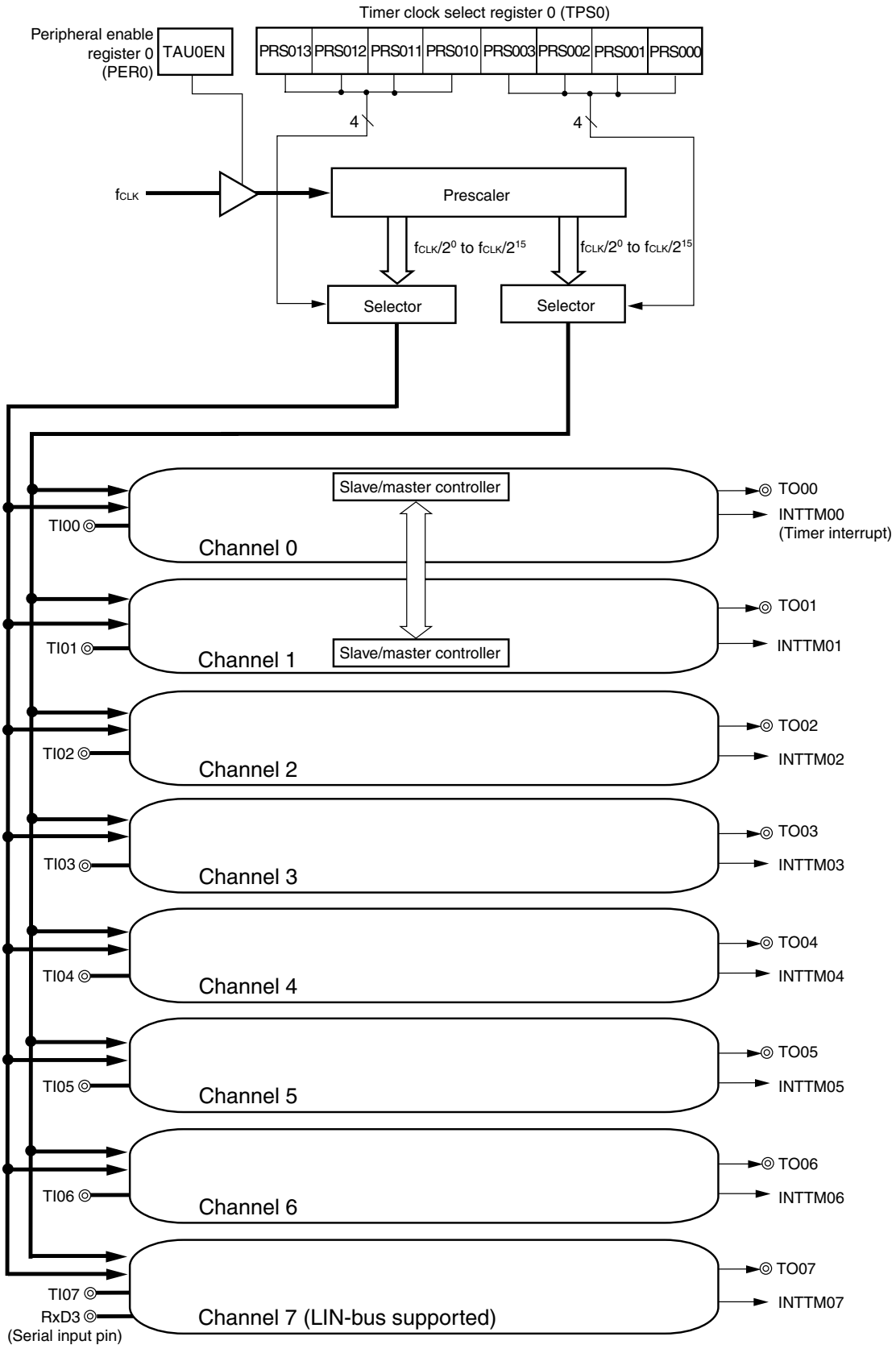


Figure 8-4. Entire Configuration of Timer Array Unit 1 (78K0R/KF3-L, 78K0R/KG3-L only)

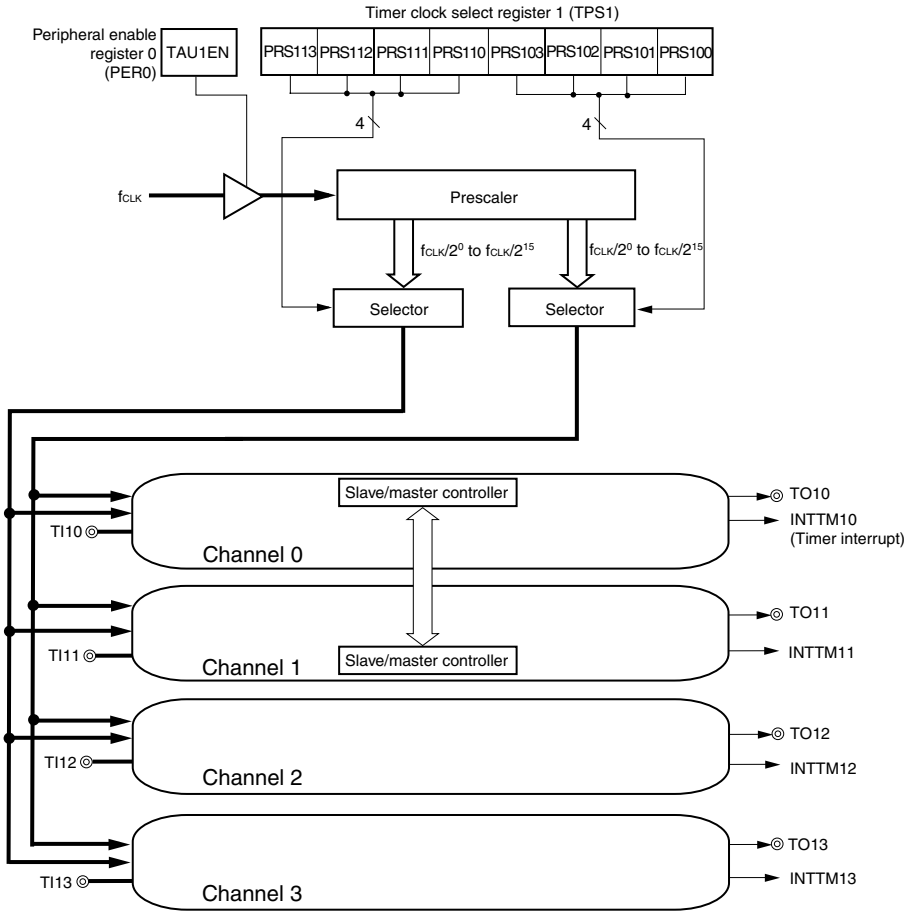
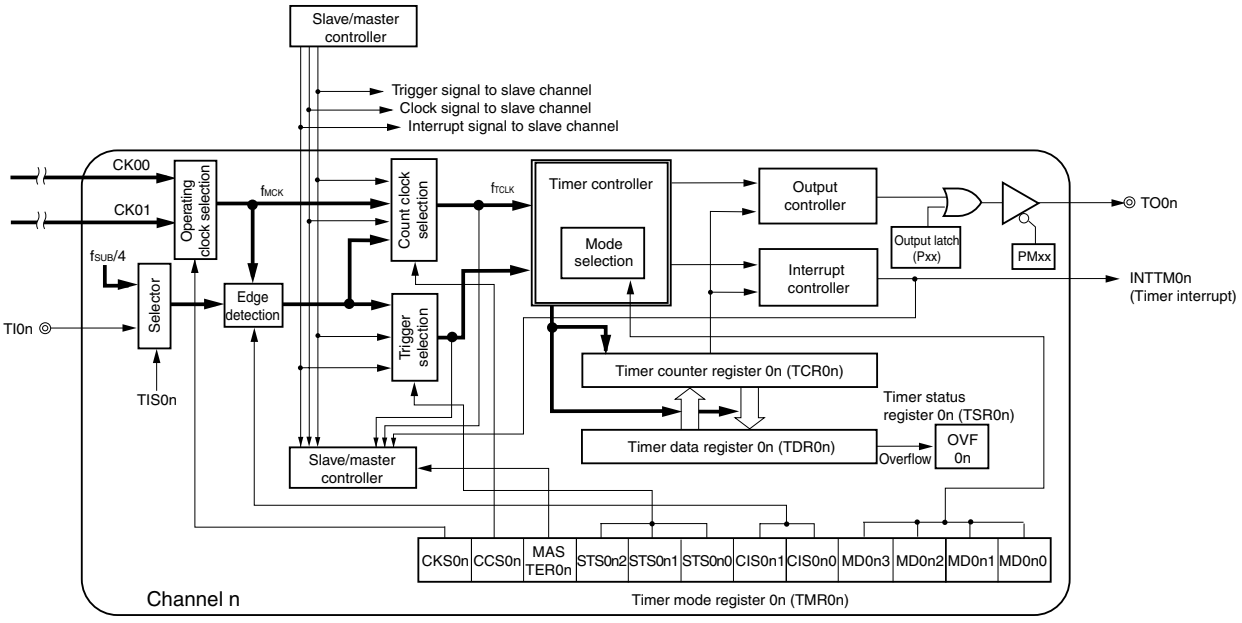


Figure 8-5. Internal Block Diagram of Channel of Timer Array Unit 0



Remark n = 0 to 7

(1) Timer/counter register mn (TCRmn)

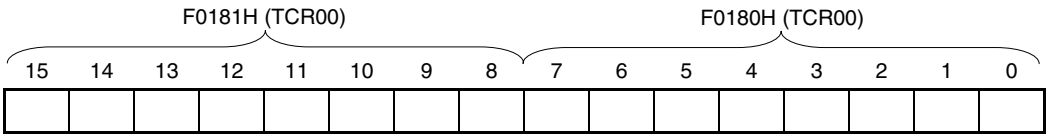
The TCRmn register is a 16-bit read-only register and is used to count clocks.

The value of this counter is incremented or decremented in synchronization with the rising edge of a count clock.

Whether the counter is incremented or decremented depends on the operation mode that is selected by the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn) (refer to **8.3 (3) Timer mode register mn (TMRmn)**).

Figure 8-6. Format of Timer/Counter Register mn (TCRmn)

Address: F0180H, F0181H (TCR00) to F018EH, F018FH (TCR07) After reset: FFFFH R
F01C0H, F01C1H (TCR10) to F01C6H, F01C7H (TCR13)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

The count value can be read by reading timer/counter register mn (TCRmn).

The count value is set to FFFFH in the following cases.

- When the reset signal is generated
- When the TAU0EN bit (in case of TAU0) or TAU1EN bit (in case of TAU1) of peripheral enable registers 0, 2 (PER0, PER2) are cleared
- When counting of the slave channel has been completed in the PWM output mode
- When counting of the master/slave channel has been completed in the one-shot pulse output mode
- When counting of the slave channel has been completed in the multiple PWM output mode

The count value is cleared to 0000H in the following cases.

- When the start trigger is input in the capture mode
- When capturing has been completed in the capture mode

Caution The count value is not captured to timer data register mn (TDRmn) even when the TCRmn register is read.

The TCRmn register read value differs as follows according to operation mode changes and the operating status.

Table 8-2. Timer/counter Register mn (TCRmn) Read Value in Various Operation Modes

Operation Mode	Count Mode	Timer/counter register mn (TCRmn) Read Value[Note]			
		Value if the operation mode was changed after releasing reset	Value if the operation mode was changed after count operation paused (TTmn = 1)	Value if the Operation was restarted after count operation paused (TTmn = 1)	Value when waiting for a start trigger after one count
Interval timer mode	Count down	FFFFH	Undefined	Stop value	–
Capture mode	Count up	0000H	Undefined	Stop value	–
Event counter mode	Count down	FFFFH	Undefined	Stop value	–
One-count mode	Count down	FFFFH	Undefined	Stop value	FFFFH
Capture & one-count mode	Count up	0000H	Undefined	Stop value	Capture value of TDRmn register + 1

Note This indicates the value read from the TCRmn register when channel n has stopped operating as a timer (TEmn = 0) and has been enabled to operate as a counter (TSmn = 1). The read value is held in the TCRmn register until the count operation starts.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(2) Timer data register mn (TDRmn)

This is a 16-bit register from which a capture function and a compare function can be selected.

The capture or compare function can be switched by selecting an operation mode by using the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn).

The value of the TDRmn register can be changed at any time.

This register can be read or written in 16-bit units.

Reset signal generation clears this register to 0000H.

Figure 8-7. Format of Timer Data Register mn (TDRmn)

Address: FFF18H, FFF19H (TDR00), FFF1AH, FFF1BH (TDR01), FFF64H, FFF65H (TDR02) to FFF6EH, FFF6FH (TDR07) FFF70H, FFF71H (TDR10) to FFF76H, FFF77H (TDR13) After reset: 0000H R/W

	FFF19H (TDR00)								FFF18H (TDR00)							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDRmn																

(i) When timer data register mn (TDRmn) is used as compare register

Counting down is started from the value set to the TDRmn register. When the count value reaches 0000H, an interrupt signal (INTTMmn) is generated. The TDRmn register holds its value until it is rewritten.

Caution The TDRmn register does not perform a capture operation even if a capture trigger is input, when it is set to the compare function.

(ii) When timer data register mn (TDRmn) is used as capture register

The count value of timer/counter register mn (TCRmn) is captured to the TDRmn register when the capture trigger is input.

A valid edge of the TImn pin can be selected as the capture trigger. This selection is made by timer mode register mn (TMRmn).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.3 Registers Controlling Timer Array Unit

Timer array unit is controlled by the following registers.

- Peripheral enable registers 0, 2 (PER0, PER2) Note 1
- Timer clock select register m (TPSm)
- Timer mode register mn (TMRmn)
- Timer status register mn (TSRmn)
- Timer channel enable status register m (TEm)
- Timer channel start register m (TSm)
- Timer channel stop register m (TTm)
- Timer input select register m (TISm)
- Timer output enable register m (TOEm)
- Timer output register m (TOm)
- Timer output level register m (TOLm)
- Timer output mode register m (TOMm)
- Input switch control register (ISC)
- Noise filter enable registers 1, 2 (NFEN1, NFEN2)
- Port mode register (PMxx) Note 2
- Port register (Pxx) Note 2

Notes 1. Set the PER2 register in the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L. Set the PER0 register in the 78K0R/KF3-L and 78K0R/KG3-L.

2. The port mode registers (PMxx) and port registers (Pxx) to be set differ depending on the product. for details, **see 8. 3 (15) Port mode registers 0, 1, 3 to 6, 13, 14 (PM0, PM1, PM3 to PM6, PM13, PM14).**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(1) Peripheral enable registers 0, 2 (PER0, PER2)

These registers are used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the timer array unit is used, be sure to set the following bits to 1.

- 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L
  When timer array unit 0 is used → Bit 0 (TAU0EN) of the PER2 register
- 78K0R/KF3-L, 78K0R/KG3-L
  When timer array unit 0 is used → Bit 0 (TAU0EN) of the PER0 register
  When timer array unit 1 is used → Bit 1 (TAU1EN) of the PER0 register

The PER0 and PER2 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 8-8. Format of Peripheral Enable Register 0 (PER0) (78K0R/KF3-L, 78K0R/KG3-L)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN	0	ADCEN	IICAEN	SAU1EN	SAU0EN	TAU1EN	TAU0EN

TAUmEN	Control of timer array unit m input clock (m = 0, 1)
0	Stops supply of input clock. • SFR used by the timer array unit m cannot be written. • The timer array unit m is in the reset status.
1	Supplies input clock. • SFR used by the timer array unit m can be read/written.

Cautions 1. When setting the timer array unit m, be sure to set the TAU0EN and TAU1EN bits to 1 first. If TAU0EN, TAU1EN = 0, writing to a control register of timer array unit m is ignored, and all read values are default values (except for the timer input select register m (TISm), input switch control register (ISC), noise filter enable registers 1, 2 (NFEN1, NFEN2), port mode registers 0, 1, 3, 4, 6, 13, 14 (PM0, PM1, PM3, PM4, PM6, PM13, PM14), and port registers 0, 1, 3, 4, 6, 13, 14 (P0, P1, P3, P4, P6, P13, P14)).

2. Be sure to clear bit 6 to 0.

Remark m = 0, 1

Figure 8-9. Format of Peripheral Enable Register 2 (PER2) (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

Address: F00F2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
PER2	0	0	0	0	0	0	0	TAU0EN

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by timer array unit 0 can be read/written.

Cautions 1. When setting timer array unit 0, be sure to set TAU0EN to 1 first. If TAU0EN = 0, writing to a control register of timer array unit 0 is ignored, and all read values are default values (except for timer input select register 0 (TIS0), input switch control register (ISC), noise filter enable registers 1, 2 (NFEN1, 2), port mode registers 0, 1, 5 (PM0, PM1, PM5), and port registers 0, 1, 5 (P0, P1, P5)).

2. Be sure to clear bits 1 to 7 of the PER2 register to 0.

(2) Timer clock select register m (TPSm)

The TPSm register is a 16-bit register that is used to select two types of operation clocks (CKm0, CKm1) that are commonly supplied to each channel. CKm1 is selected by bits 7 to 4 of the TPSm register, and CKm0 is selected by bits 3 to 0.

Rewriting of the TPSm register during timer operation is possible only in the following cases.

If the PRSm00 to PRSm03 bits can be rewritten:

All channels for which CKm0 is selected as the operation clock (CKSmn = 0) are stopped (TEmn = 0).

If the PRSm10 to PRSm13 bits can be rewritten:

All channels for which CKm1 is selected as the operation clock (CKSmn = 1) are stopped (TEmn = 0).

The TPSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TPSm register can be set with an 8-bit memory manipulation instruction with TPSmL.

Reset signal generation clears this register to 0000H.

Figure 8-10. Format of Timer Clock Select register m (TPSm)

Address: F01B6H, F01B7H (TPS0) After reset: 0000H R/W

F01DEH, F01DFH (TPS1)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPSm	0	0	0	0	0	0	0	0	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00

PRS mk3	PRS mk2	PRS mk1	PRS mk0		Selection of operation clock (CKmk) Note			
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), stop timer array unit (TTm = 00FFH).
The timer array unit must also be stopped if the operating clock specified by using the CKSmn bit (f_{MCK}), the valid edge of the signal input from the TImn pin, or the subsystem clock divided by 4 ($f_{SUB}/4$) is selected as the count clock (f_{TCLK}).

Caution Be sure to clear bits 15 to 8 to "0".

Remarks 1. f_{CLK}: CPU/peripheral hardware clock frequency

2. m: Unit number (m = 0, 1), k = 0, 1
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: m = 0
78K0R/KF3-L, 78K0R/KG3-L: m = 0, 1

(3) Timer mode register mn (TMRmn)

The TMRmn register sets an operation mode of channel n. It is used to select an operation clock (f_{MCK}), a count clock, whether the timer operates as the master or a slave, a start trigger and a capture trigger, the valid edge of the timer input, and an operation mode (interval, capture, event counter, one-count, or capture & one-count).

Rewriting the TMRmn register is prohibited when the register is in operation (when TEmn = 1). However, bits 7 and 6 (CISmn1, CISmn0) can be rewritten even while the register is operating with some functions (when TEmn = 1) (for details, see **8.7 Independent Channel Operation Function of Timer Array Unit** and **8.8 Simultaneous Channel Operation Function of Timer Array Unit**.

The TMRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 8-11. Format of Timer Mode Register mn (TMRmn) (1/3)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

F01C8H, F01C9H (TMR10) to F01CEH, F01CFH (TMR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKS mn	0	0	CCS mn	MAST ERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

CKS mn	Selection of operation clock (f_{MCK}) of channel n
0	Operation clock CKm0 set by timer clock select register m (TPSm)
1	Operation clock CKm1 set by timer clock select register m (TPSm)
Operation clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated depending on the setting of the CCSmn bit.	

CCS mn	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn bit
1	Valid edge of input signal input from the TImn pin/subsystem clock divided by 4 (f_{SUB}/4) Note
Count clock (f_{TCLK}) is used for the timer/counter, output controller, and interrupt controller.	

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Cautions 1. Be sure to clear bits 14, 13, 5, and 4 to "0".

2. The timer array unit must be stopped (TTm = 00FFH) if the clock selected for f_{CLK} is changed (by changing the value of the system clock control register (CKC)), even if the operating clock specified by using the CKSmn bit (f_{MCK}), the valid edge of the signal input from the TImn pin, or the subsystem clock divided by 4 (f_{SUB}/4) is selected as the count clock (f_{TCLK}).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-11. Format of Timer Mode Register mn (TMRmn) (2/3)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W
F01C8H, F01C9H (TMR10) to F01CEH, F01CFH (TMR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKSmn	0	0	CCSmn	MASTERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

MASTERmn	Selection between using channel n independently or simultaneously with another channel(as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only the even channel can be set as a master channel (MASTERmn = 1). Be sure to use odd-numbered channels as slave channels (MASTERmn = 0). Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.	

STSmn2	STSmn1	STSmn0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

CISmn1	CISmn0	Selection of TImn pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge
If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B.		

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-11. Format of Timer Mode Register mn (TMRmn) (3/3)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W
F01C8H, F01C9H (TMR10) to F01CEH, F01CFH (TMR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKS mn	0	0	CCS mn	MAST ERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

MD mn3	MD mn2	MD mn1	MD mn0	Operation mode of channel n	Count operation of TCR	Independent operation
0	0	0	1/0	Interval timer mode	Counting down	Possible
0	1	0	1/0	Capture mode	Counting up	Possible
0	1	1	0	Event counter mode	Counting down	Possible
1	0	0	1/0	One-count mode	Counting down	Impossible
1	1	0	0	Capture & one-count mode	Counting up	Possible
Other than above				Setting prohibited		
The operation of the MDmn0 bit varies depending on each operation mode (see table below).						

Operation mode (Value set by the MDmn3 to MDmn1 bits (see table above))	MD mn0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode Note 1 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation Note 2. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Notes 1. In one-count mode, interrupt output (INTTMmn) when starting a count operation and TOmn output are not controlled.

2. If the start trigger (TSmn = 1) is issued during operation, the counter is cleared, an interrupt is generated, and recounting is started.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(4) Timer status register mn (TSRmn)

The TSRmn register indicates the overflow status of the counter of channel n.

The TSRmn register is valid only in the capture mode (MDmn3 to MDmn1 = 010B) and capture & one-count mode (MDmn3 to MDmn1 = 110B). It will not be set in any other mode. See Table 8-3 for the operation of the OVF bit in each operation mode and set/clear conditions.

The TSRmn register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the TSRmn register can be set with an 8-bit memory manipulation instruction with TSRmnL.

Reset signal generation clears this register to 0000H.

Figure 8-12. Format of Timer Status Register mn (TSRmn)

Address: F01A0H, F01A1H (TSR00) to F01AEH, F01AFH (TSR07) After reset: 0000H R
F01D0H, F01D1H (TSR10) to F01D6H, F01D7H (TSR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSRmn	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OVF

OVF	Counter overflow status of channel n
0	Overflow does not occur.
1	Overflow occurs.
When OVF = 1, this flag is cleared (OVF = 0) when the next value is captured without overflow.	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Table 8-3. OVF Bit Operation and Set/Clear Conditions in Each Operation Mode

Timer operation mode	OVF bit	Set/clear conditions
• Capture mode	clear	When no overflow has occurred upon capturing
• Capture & one-count mode	set	When an overflow has occurred upon capturing
• Interval timer mode • Event counter mode • One-count mode	clear	–
	set	(Use prohibited, not set and not cleared)

Remark The OVF bit does not change immediately after the counter has overflowed, but changes upon the subsequent capture.

(5) Timer channel enable status register m (TEm)

The TEm register is used to enable or stop the timer operation of each channel.

When a bit of timer channel start register m (TSm) is set to 1, the corresponding bit of this register is set to 1.

When a bit of timer channel stop register m (TTm) is set to 1, the corresponding bit of this register is cleared to 0.

The TEm register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the TEm register can be set with a 1-bit or 8-bit memory manipulation instruction with TEmL.

Reset signal generation clears this register to 0000H.

Figure 8-13. Format of Timer Channel Enable Status register m (TEm)

Address: F01B0H, F01B1H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TE0	0	0	0	0	0	0	0	0	TE07	TE06	TE05	TE04	TE03	TE02	TE01	TE00

Address: F01D8H, F01D9H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TE1	0	0	0	0	0	0	0	0	0	0	0	0	TE13	TE12	TE11	TE10

TEmn	Indication of operation enable/stop status of channel n
0	Operation is stopped.
1	Operation is enabled.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(6) Timer channel start register m (TSm)

The TSm register is a trigger register that is used to clear timer/counter register mn (TCRmn) and start the counting operation of each channel.

When a bit (TSmn) of this register is set to 1, the corresponding bit (TEmn) of timer channel enable status register m (TEm) is set to 1. The TSmn bit is immediately cleared when operation is enabled (TEmn = 1), because it is a trigger bit.

The TSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TSm register can be set with a 1-bit or 8-bit memory manipulation instruction with TSmL.

Reset signal generation clears this register to 0000H.

Figure 8-14. Format of Timer Channel Start register m (TSm)

Address: F01B2H, F01B3H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS0	0	0	0	0	0	0	0	0	TS07	TS06	TS05	TS04	TS03	TS02	TS01	TS00

Address: F01DAH, F01DBH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS1	0	0	0	0	0	0	0	0	0	0	0	0	TS13	TS12	TS11	TS10

TSmn	Operation enable (start) trigger of channel n
0	No trigger operation
1	The TEmn bit is set to 1 and the count operation becomes enabled. The TCRmn register count operation start in the count operation enabled state varies depending on each operation mode (see Table 8-4).

Caution Be sure to clear bits 15 to 8 of the TS0 register and bits 15 to 4 of the TS1 register to "0"

Remarks 1. When the TSm register is read, 0 is always read.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

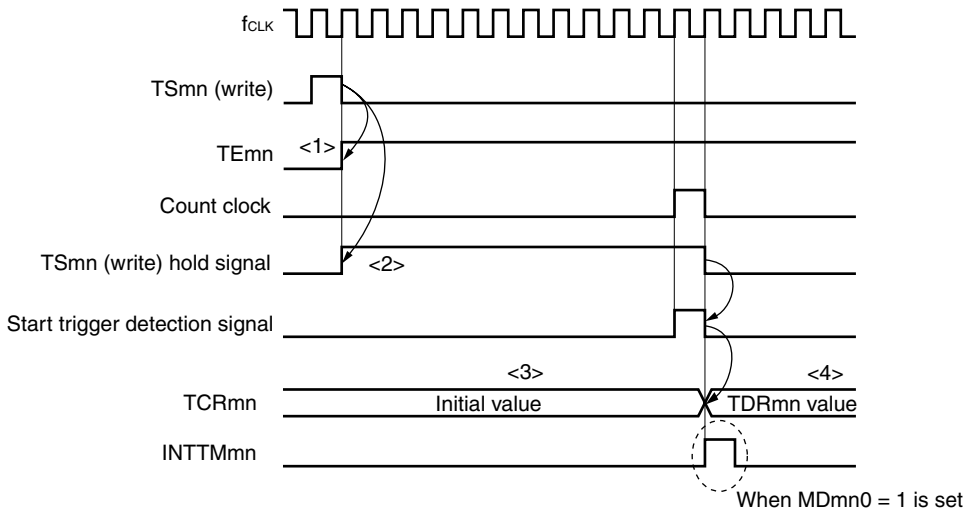
Table 8-4. Operations from Count Operation Enabled State to Timer/counter Register mn (TCRmn) Count Start

Timer operation mode	Operation when TSmn = 1 is set
• Interval timer mode	No operation is carried out from start trigger detection (TSmn=1) until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation (see **8.3 (6) (a) Start timing in interval timer mode**).
• Event counter mode	Writing 1 to the TSmn bit loads the value of the TDRmn register to the TCRmn register. The subsequent count clock performs count down operation. The external trigger detection selected by the STSmn2 to STSmn0 bits in the TMRmn register does not start count operation (see **8.3 (6) (b) Start timing in event counter mode**).
• Capture mode	No operation is carried out from start trigger detection until count clock generation. The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation (see **8.3 (6) (c) Start timing in capture mode**).
• One-count mode	The waiting-for-start-trigger state is entered by writing 1 to the TSmn bit while the timer is stopped (TEmn = 0). No operation is carried out from start trigger detection until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation (see **8.3 (6) (d) Start timing in one-count mode**).
• Capture & one-count mode	The waiting-for-start-trigger state is entered by writing 1 to the TSmn bit while the timer is stopped (TEmn = 0). No operation is carried out from start trigger detection until count clock generation. The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation (see **8.3 (6) (e) Start timing in capture & one-count mode**).

(a) Start timing in interval timer mode

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.
<2> The write data to the TSmn bit is held until count clock generation.
<3> Timer/counter register mn (TCRmn) holds the initial value until count clock generation.
<4> On generation of count clock, the value of timer data register mn (TDRmn) is loaded to the TCRmn register and count starts.

Figure 8-15. Start Timing (In Interval Timer Mode)



Caution In the first cycle operation of count clock after writing the TSmn bit, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting MDmn0 = 1.

(b) Start timing in event counter mode

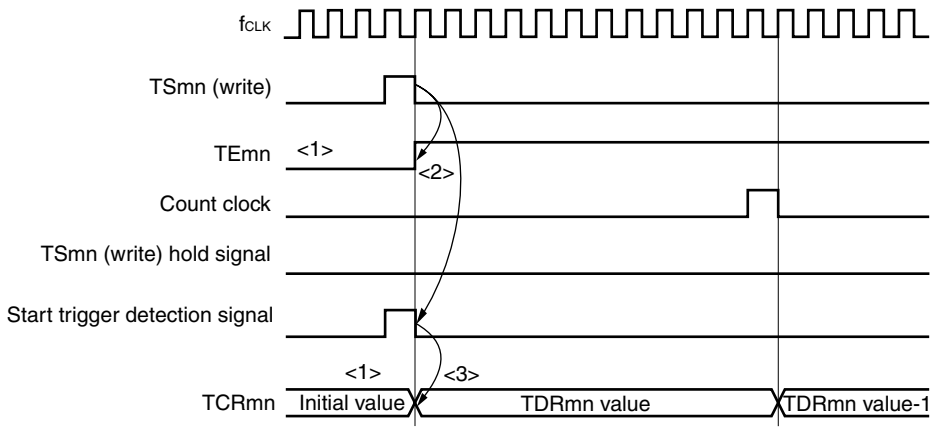
<1> Timer/counter register mn (TCRmn) holds its initial value while operation is stopped (TEmn = 0).

<2> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.

<3> As soon as 1 has been written to the TSmn bit and 1 has been set to the TEmn bit, the value of timer data register mn (TDRmn) is loaded to the TCRmn register to start counting.

<4> After that, the TCRmn register value is counted down according to the count clock.

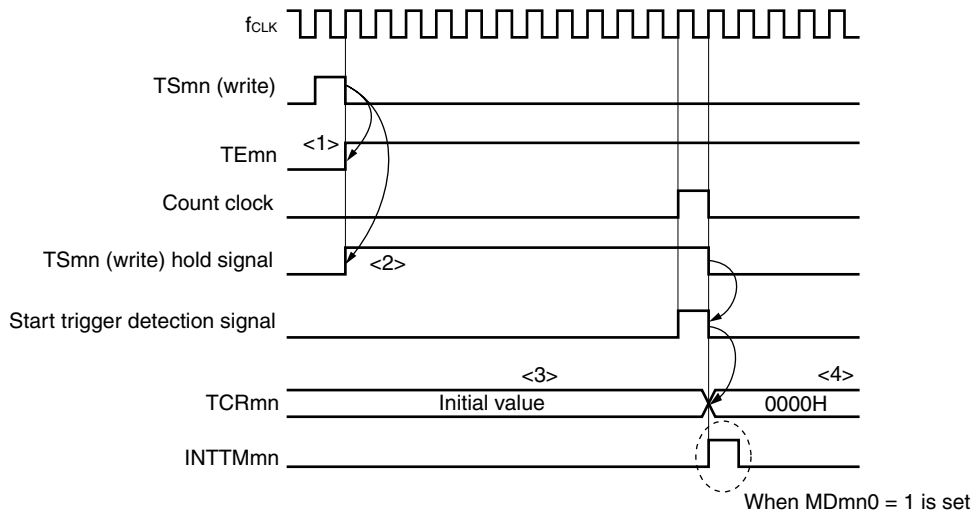
Figure 8-16. Start Timing (In Event Counter Mode)



(c) Start timing in capture mode

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.
<2> The write data to the TSmn bit is held until count clock generation.
<3> Timer/counter register mn (TCRmn) holds the initial value until count clock generation.
<4> On generation of count clock, 0000H is loaded to the TCRmn register and count starts.

Figure 8-17. Start Timing (In Capture Mode)



Caution In the first cycle operation of count clock after writing the TSmn bit, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting MDmn0 = 1.

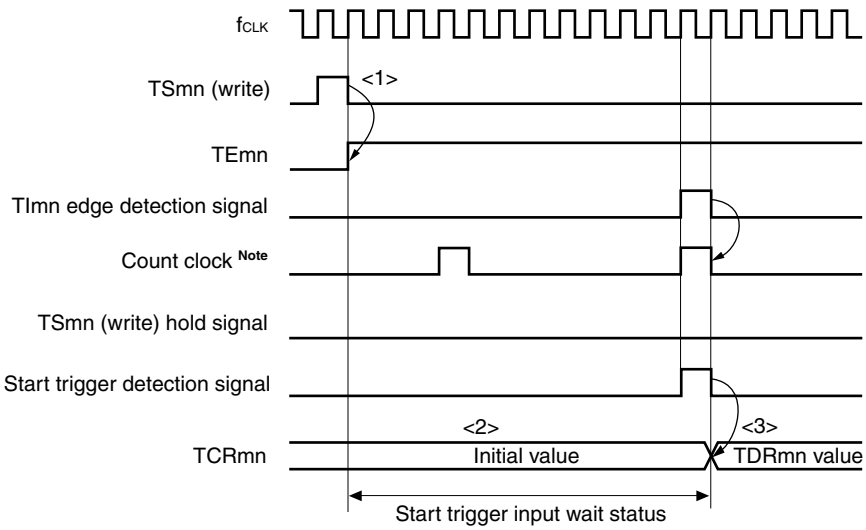
(d) Start timing in one-count mode

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.

<2> Enters the start trigger input wait status, and timer/counter register mn (TCRmn) holds the initial value.

<3> On start trigger detection, the value of timer data register mn (TDRmn) is loaded to the TCRmn register and count starts.

Figure 8-18. Start Timing (In One-count Mode)



Note When the one-count mode is set, the operation clock (f_{MCK}) is selected as count clock (CCSmn = 0).

Caution An input signal sampling error is generated since operation starts upon start trigger detection (If the TImn pin input signal is used as a start trigger, an error of one count clock occurs.).

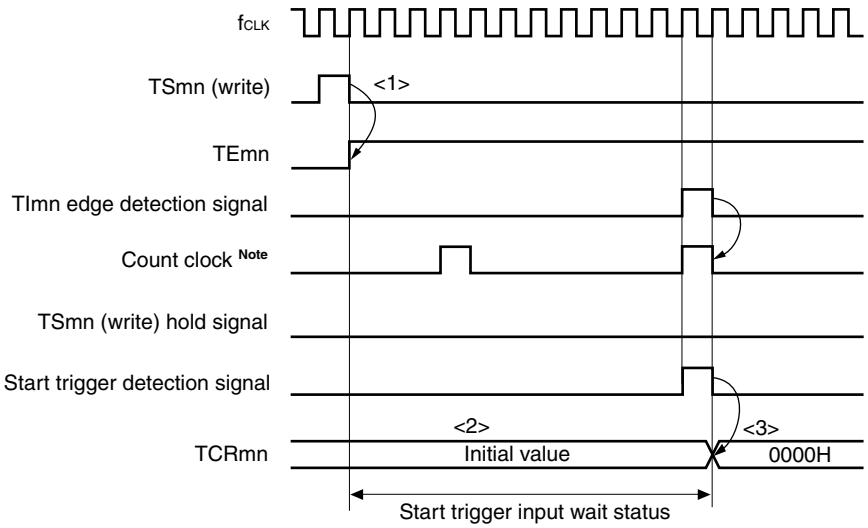
(e) Start timing in capture & one-count mode

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.

<2> Enters the start trigger input wait status, and timer/counter register mn (TCRmn) holds the initial value.

<3> On start trigger detection, 0000H is loaded to the TCRmn register and count starts.

Figure 8-19. Start Timing (In Capture & One-count Mode)



Note When the capture & one-count mode is set, the operation clock (f_{MCK}) is selected as count clock (CCSmn = 0).

Caution An input signal sampling error is generated since operation starts upon start trigger detection (If the TImn pin input signal is used as a start trigger, an error of one count clock occurs.)

(7) Timer channel stop register m (TTm)

The TTm register is a trigger register that is used to clear timer/counter register mn (TCRmn) and start the counting operation of each channel.

When a bit (TTmn) of this register is set to 1, the corresponding bit (TEmn) of timer channel enable status register m (TEm) is cleared to 0. The TTmn bit is immediately cleared when operation is stopped (TEmn = 0), because it is a trigger bit.

The TTm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TTm register can be set with a 1-bit or 8-bit memory manipulation instruction with TTmL.

Reset signal generation clears this register to 0000H.

Figure 8-20. Format of Timer Channel Stop register m (TTm)

Address: F01B4H, F01B5H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TT0	0	0	0	0	0	0	0	0	TT07	TT06	TT05	TT04	TT03	TT02	TT01	TT00

Address: F01DCH, F01DDH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TT1	0	0	0	0	0	0	0	0	0	0	0	0	TT13	TT12	TT11	TT10

TTmn	Operation stop trigger of channel n
0	No trigger operation
1	Operation is stopped (stop trigger is generated).

Caution Be sure to clear bits 15 to 8 of the TT0 register and bits 15 to 4 of the TT1 register to "0".

Remarks 1. When the TTm register is read, 0 is always read.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(8) Timer input select register m (TISm)

The TISm register is used to select whether a signal input to the timer input pin (TImn) or the subsystem clock divided by four ($f_{SUB}/4$)[Note] is valid for each channel.

The TISm register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Figure 8-21. Format of Timer Input Select register m (TISm)

Address: FFF3EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	TIS07	TIS06	TIS05	TIS04	TIS03	TIS02	TIS01	TIS00

Address: FFF3FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS1	0	0	0	0	TIS13	TIS12	TIS11	TIS10

TISmn	Selection of timer input/subsystem clock used with channel n
0	Input signal of timer input pin (TImn)
1	Subsystem clock divided by 4 ($f_{SUB}/4$)[Note]

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(9) Timer output enable register m (TOEm)

The TOEm register is used to enable or disable timer output of each channel.

Channel n for which timer output has been enabled becomes unable to rewrite the value of the TOmn bit of timer output register m (TOm) described later by software, and the value reflecting the setting of the timer output function through the count operation is output from the timer output pin (TOmn).

The TOEm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOEm register can be set with a 1-bit or 8-bit memory manipulation instruction with TOEmL.

Reset signal generation clears this register to 0000H.

Figure 8-22. Format of Timer Output Enable register m (TOEm)

Address: F01BAH, F01BBH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00

Address: F01E2H, F01E3H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE1	0	0	0	0	0	0	0	0	0	0	0	0	TOE13	TOE12	TOE11	TOE10

TOEmn	Timer output enable/disable of channel n
0	The TOmn operation stopped by count operation (timer channel output bit). Writing to the TOmn bit is enabled. The TOmn pin functions as data output, and it outputs the level set to the TOmn bit. The output level of the TOmn pin can be manipulated by software.
1	The TOmn operation enabled by count operation (timer channel output bit). Writing to the TOmn bit is disabled (writing is ignored). The TOmn pin functions as timer output, and the TOEmn bit is set or reset depending on the timer operation. The TOmn pin outputs the square-wave or PWM depending on the timer operation.

Caution Be sure to clear bits 15 to 8 of the TOE0 register and bits 15 to 4 of the TOE1 register to "0".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(10) Timer output register m (TOm)

The TOm register is a buffer register of timer output of each channel.

The value of each bit in this register is output from the timer output pin (TOmn) of each channel.

The TOmn bit oh this register can be rewritten by software only when timer output is disabled (TOEmn = 0). When timer output is enabled (TOEmn = 1), rewriting this register by software is ignored, and the value is changed only by the timer operation.

When using the following timer output pins as port function pins, set the corresponding TOmn bit to 0.

78K0R/KC3-L: P10/TO02, P11/TO03, P12/TO04, P13/TO05, P50/TO06, P51/TO07, P52/SLTO[Note]
78K0R/KD3-L: P01/TO00, P10/TO02, P11/TO03, P12/TO04, P13/TO05, P50/TO06, P51/TO07, P52/SLTO
78K0R/KE3-L: P01/TO00, P10/TO02, P11/TO03, P12/TO04, P13/TO05, P14/TO06, P15/TO07, P52/SLTO
78K0R/KF3-L: P53/TO00, P16/TO01, P17/TO02, P31/TO03, P42/TO04, P05/TO05, P06/TO06, P54/TO07, P64/TO10, P65/TO11, P66/TO12, P67/TO13
78K0R/KG3-L: P01/TO00, P16/TO01, P17/TO02, P31/TO03, P42/TO04, P46/TO05, P131/TO06, P145/TO07, P64/TO10, P65/TO11, P66/TO12, P67/TO13

Note The 78K0R/KC3-L (40-pin) doesn't have the SLTI and SLTO pins .

The TOm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOm register can be set with an 8-bit memory manipulation instruction with TOmL.

Reset signal generation clears this register to 0000H.

Figure 8-23. Format of Timer Output register m (TOm)

Address: F01B8H, F01B9H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO0	0	0	0	0	0	0	0	0	TO07	TO06	TO05	TO04	TO03	TO02	TO01	TO00

Address: F01E0H, F01E1H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO1	0	0	0	0	0	0	0	0	0	0	0	0	TO13	TO12	TO11	TO10

TOmn	Timer output of channel n
0	Timer output value is "0".
1	Timer output value is "1".

Caution Be sure to clear bits 15 to 8 of the TO0 register and bits 15 to 4 of the TO1 register to "0".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(11) Timer output level register m (TOLm)

The TOLm register is a register that controls the timer output level of each channel.

The setting of the inverted output of channel n by this register is reflected at the timing of set or reset of the timer output signal while the timer output is enabled (TOEmn = 1) in the slave channel output mode (TOMmn = 1). In the master channel output mode (TOMmn = 0), this register setting is invalid.

The TOLm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOLm register can be set with an 8-bit memory manipulation instruction with TOLmL.

Reset signal generation clears this register to 0000H.

Figure 8-24. Format of Timer Output Level register m (TOLm)

Address: F01BCH, F01BDH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOL0	0	0	0	0	0	0	0	0	TOL07	TOL06	TOL05	TOL04	TOL03	TOL02	TOL01	TOL00

Address: F01E4H, F01E5H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOL1	0	0	0	0	0	0	0	0	0	0	0	0	TOL13	TOL12	TOL11	TOL10

TOLmn	Control of timer output level of channel n
0	Positive logic output (active-high)
1	Inverted output (active-low)

Caution Be sure to clear bits 15 to 8 of the TOL0 register and bits 15 to 4 of the TOL1 register to "0".

Remarks 1. If the value of this register is rewritten during timer operation, the timer output is inverted when the timer output signal changes next, instead of immediately after the register value is rewritten.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(12) Timer output mode register m (TOMm)

The TOMm register is used to control the timer output mode of each channel.

When a channel is used for the independent channel operation function, set the corresponding bit of the channel to be used to 0.

When a channel is used for the simultaneous channel operation function (PWM output, one-shot pulse output, or multiple PWM output), set the corresponding bit of the master channel to 0 and the corresponding bit of the slave channel to 1.

The setting of each channel n by this register is reflected at the timing when the timer output signal is set or reset while the timer output is enabled (TOEmn = 1).

The TOMm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOMm register can be set with an 8-bit memory manipulation instruction with TOMmL.

Reset signal generation clears this register to 0000H.

Figure 8-25. Format of Timer Output Mode register m (TOMm)

Address: F01BEH, F01BFH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOM0	0	0	0	0	0	0	0	0	TOM07	TOM06	TOM05	TOM04	TOM03	TOM02	TOM01	TOM00

Address: F01E6, F01E7H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOM1	0	0	0	0	0	0	0	0	0	0	0	0	TOM13	TOM12	TOM11	TOM10

TOMmn	Control of timer output mode of channel n
0	Master channel output mode (to produce toggle output by timer interrupt request signal (INTTMmn))
1	Slave channel output mode (output is set by the timer interrupt request signal (INTTMmn) of the master channel, and reset by the timer interrupt request signal (INTTMmp) of the slave channel)

Caution Be sure to clear bits 15 to 8 of the TOM0 register and bits 15 to 4 of the TOM1 register to "0".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13
p: Slave channel number [Note]
When m = 0: Master channel n = 0, 2, 4, 6, n < p ≤ 7
When m = 1: Master channel n = 0, 2, n < p ≤ 3
(where p is a consecutive integer greater than n)

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

(13) Input switch control register (ISC)

The ISC1 and ISC0 bits of the ISC register are used to implement LIN-bus communication operation by using channel 7 in association with the serial array unit. When the ISC1 bit is set to 1, the input signal of the serial data input pin (RxDk) is selected as a timer input signal.

The ISC2 bit is set to select the P52/SLTI/SLTO pin as the timer I/O pin of timer channels 0 and 1 (78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, 78K0R/KE3-L only).

The ISC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 8-26. Format of Input Switch Control Register (ISC)

Address: FFF3CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	0	0	0	ISC2 Note 1	ISC1	ISC0

ISC2 Note 1	Selecting P52/SLTI/SLTO Pin as Timer I/O Pin			
	Channel 0		Channel 1	
	Input Pin	Output Pin	Input Pin	Output Pin
0	P00/TI00 Note 2	P01/TO00 Note 2	P52/SLTI	P52/SLTO
1	P52/SLTI	P52/SLTO	–	–

ISC1	Switching channel 7 input of timer array unit 0
0	Uses the input signal of the TI07 pin as a timer input (normal operation).
1	Input signal of the RxDk pin is used as timer input (detects the wakeup signal and measures the low width of the sync break field and the pulse width of the sync field).

ISC0	Switching external interrupt (INTP0) input
0	Uses the input signal of the INTP0 pin as an external interrupt (normal operation).
1	Uses the input signal of the RxDk pin as an external interrupt (wakeup signal detection).

Notes 1. 78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, 78K0R/KE3-L only.

2. 78K0R/KD3-L and 78K0R/KE3-L only. Only the P52/SLTI/SLTO pin can be assigned to channels 0 and 1 in the 78K0R/KC3-L (44-pin, 48-pin).

Caution Be sure to clear bits 7 to 3 to "0" in the 78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, and 78K0R/KE3-L. Be sure to clear bits 7 to 2 to "0" in the 78K0R/KC3-L (40-pin).
Be sure to clear bits 7 to 2 to "0" in the 78K0R/KF3-L and 78K0R/KG3-L.

Remarks 1. When the LIN-bus communication function is used, select the input signal of the RxDk pin by setting ISC1 to 1.

2. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: k = 0 (RxD0)
78K0R/KF3-L, 78K0R/KG3-L: k = 3 (RxD3)

(14) Noise filter enable registers 1, 2 (NFEN1, NFEN2)

The NFEN1 and NFEN2 registers are used to set whether the noise filter can be used for the timer input signal to each channel.

Enable the noise filter by setting the corresponding bits to 1 on the pins in need of noise removal.

When the noise filter is ON, match detection and synchronization of the 2 clocks is performed with the CPU/peripheral hardware clock (f_{MCK}). When the noise filter is OFF, only synchronization is performed with the CPU/peripheral hardware clock (f_{MCK}).

The NFEN1 and NFEN2 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 8-27. Format of Noise Filter Enable Registers 1, 2 (NFEN1, NFEN2)
(78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

Address: F0061H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN1	TNFEN07	TNFEN06	TNFEN05	TNFEN04	TNFEN03	TNFEN02	0	TNFEN00 Note1

Address: F0062H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN2	0	0	0	TNFENSL Note 2	0	0	0	0

TNFEN07	Enable/disable using noise filter of TI07/TO07/P15 (P51) pin Note 3 or RxD0/P74 pin input signal Note 3
0	Noise filter OFF
1	Noise filter ON

TNFEN06	Enable/disable using noise filter of TI06/TO06/P14 (P50) pin Note 3 input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN05	Enable/disable using noise filter of TI05/TO05/P13 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN04	Enable/disable using noise filter of TI04/TO04/RTCDIV/RTCCL/P12 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN03	Enable/disable using noise filter of TI03/TO03/P11 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN02	Enable/disable using noise filter of TI02/TO02/P10 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN00 Note1	Enable/disable using noise filter of TI00/P00 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFENSL Note 2	Enable/disable using noise filter of SLTI/SLTO/P52 pin input signal
0	Noise filter OFF
1	Noise filter ON

Notes 1. 78K0R/KD3-L and 78K0R/KE3-L only
2. TNFENSL bit is not provided in the 78K0R/KC3-L (40-pin).
3. TI06/TO06 and TI07/TO07 are shared with P50 and P51, respectively, in products other than the 78K0R/KE3-L.
4. The applicable pin can be switched by setting the ISC1 bit of the ISC register.
ISC1 = 0: Whether or not to use the noise filter of the TI07 pin can be selected.
ISC1 = 1: Whether or not to use the noise filter of the RxD0 pin can be selected.

Figure 8-28. Format of Noise Filter Enable Registers 1, 2 (NFEN1, NFEN2) (78K0R/KF3-L, 78K0R/KG3-L) (1/2)

Address: F0061H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN1	TNFEN07	TNFEN06	TNFEN05	TNFEN04	TNFEN03	TNFEN02	TNFEN01	TNFEN00

Address: F0062H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN2	0	0	0	0	TNFEN13	TNFEN12	TNFEN11	TNFEN10

TNFEN07	Enable/disable using noise filter of the following pin input signal 78K0R/KF3-L: SI41[Note 1]/TI07/TO07/P54 pin or RxD3/P14 pin[Note 2] 78K0R/KG3-L: TI07/TO07/P145 pin or RxD3/P14 pin[Note 2]
0	Noise filter OFF
1	Noise filter ON

TNFEN06	Enable/disable using noise filter of the following pin input signal 78K0R/KF3-L: TI06/TO06/P06 pin 78K0R/KG3-L: TI06/TO06/P131 pin
0	Noise filter OFF
1	Noise filter ON

TNFEN05	Enable/disable using noise filter of the following pin input signal 78K0R/KF3-L: TI05/TO05/P05 pin 78K0R/KG3-L: TI05/TO05/P146 pin
0	Noise filter OFF
1	Noise filter ON

TNFEN04	Enable/disable using noise filter of TI04/TO04/P42 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN03	Enable/disable using noise filter of TI03/TO03/INTP4/P31 pin input signal
0	Noise filter OFF
1	Noise filter ON

Notes 1. SI41 pin is only mounted in the μPD78F1027 and 78F1028.

2. The applicable pin can be switched by setting the ISC1 bit of the ISC register.

ISC1 = 0: Whether or not to use the noise filter of the TI07 pin can be selected.

ISC1 = 1: Whether or not to use the noise filter of the RxD3 pin can be selected.

Figure 8-28. Format of Noise Filter Enable Registers 1, 2 (NFEN1, NFEN2) (78K0R/KF3-L, 78K0R/KG3-L) (2/2)

Address: F0061H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN1	TNFEN07	TNFEN06	TNFEN05	TNFEN04	TNFEN03	TNFEN02	TNFEN01	TNFEN00

Address: F0062H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN2	0	0	0	0	TNFEN13	TNFEN12	TNFEN11	TNFEN10

TNFEN02	Enable/disable using noise filter of TI02/TO02/P17 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN01	Enable/disable using noise filter of TI01/TO01/INTP5/P16 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN00	Enable/disable using noise filter of the following pin input signal 78K0R/KF3-L: $\overline{\text{SCK41}}$[Note]/TI00/P53 pin 78K0R/KG3-L: TI00/P00 pin
0	Noise filter OFF
1	Noise filter ON

TNFEN13	Enable/disable using noise filter of TI13/TO13/P67 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN12	Enable/disable using noise filter of TI12/TO12/P66 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN11	Enable/disable using noise filter of TI11/TO11/P65 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN10	Enable/disable using noise filter of TI10/TO10/P64 pin input signal
0	Noise filter OFF
1	Noise filter ON

Note $\overline{\text{SCK41}}$ pin is only mounted in the μPD78F1027 and 78F1028.

(15) Port mode registers 0, 1, 3 to 6, 13, 14 (PM0, PM1, PM3 to PM6, PM13, PM14)

These registers set input/output of ports 0, 1, 3 to 6, 13, 14 in 1-bit units.

The port pins that are shared with the timer I/O pins differ depending on the product. When using the timer array unit, set the following port mode registers according to the product used.

78K0R/KC3-L: PM1, PM5
78K0R/KD3-L: PM1, PM5
78K0R/KE3-L: PM0, PM1, PM5
78K0R/KF3-L: PM0, PM1, PM3-PM6
78K0R/KG3-L: PM0, PM1, PM3, PM4, PM6, PM13, PM14

When using the ports (such as P01/TO00 and P10/TO02/TI02) to be shared with the timer output pin for timer output, set the port mode register (PMxx) bit and port register (Pxx) bit corresponding to each port to 0.

Example: When using P10/TO02/TI02 for timer output
Set the PM10 bit of port mode register 1 to 0.
Set the P10 bit of port register 1 to 0.

When using the ports (such as P00/TI00 and P10/TO02/TI02) to be shared with the timer output pin for timer input, set the port mode register (PMxx) bit corresponding to each port to 1. At this time, the port register (Pxx) bit may be 0 or 1.

Example: When using P10/TO02/TI02 for timer input
Set the PM10 bit of port mode register 1 to 1.
Set the P10 bit of port register 1 to 0 or 1.

The PM0, PM1, PM3 to PM6, PM13, PM14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 8-29. Format of Port Mode Registers 0, 1, 5 (PM0, PM1, PM5) (78K0R/KE3-L)

Address: FFF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	1	1	1	1	1	PM01	PM00

Address: FFF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF25H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM5	1	1	1	1	PM53	PM52	PM51	PM50

PMmn	Pmn pin I/O mode selection (m = 0, 1, 5; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode registers 0, 1, and 5 of the 78K0R/KE3-L product. See below for the format of the port mode register of other products.
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: 5.3 (1) Port mode registers (PMxx).
78K0R/KF3-L, 78K0R/KG3-L: 6.3 (1) Port mode registers (PMxx).

8.4 Basic Rules of Simultaneous Channel Operation Function

When simultaneously using multiple channels, namely, a combination of a master channel (a reference timer mainly counting the cycle) and slave channels (timers operating according to the master channel), the following rules apply.

(1) Only an even channel (channel 0, 2, 4, etc.) can be set as a master channel.
(2) Any channel, except channel 0, can be set as a slave channel.
(3) The slave channel must be lower than the master channel.
Example: If channel 2 of the TAU0 is set as a master channel, channel 3 or those that follow (channels 3, 4, 5, etc.) can be set as a slave channel.
If channel 0 of the TAU1 is set as a master channel, channel 1 or those that follow (channels 1, 2, 3) can be set as a slave channel.

(4) Two or more slave channels can be set for one master channel.
(5) When two or more master channels are to be used, slave channels with a master channel between them may not be set.
Example: If channels 0 and 4 are set as master channels, channels 1 to 3 can be set as the slave channels of master channel 0. Channels 5 to 7 cannot be set as the slave channels of master channel 0.

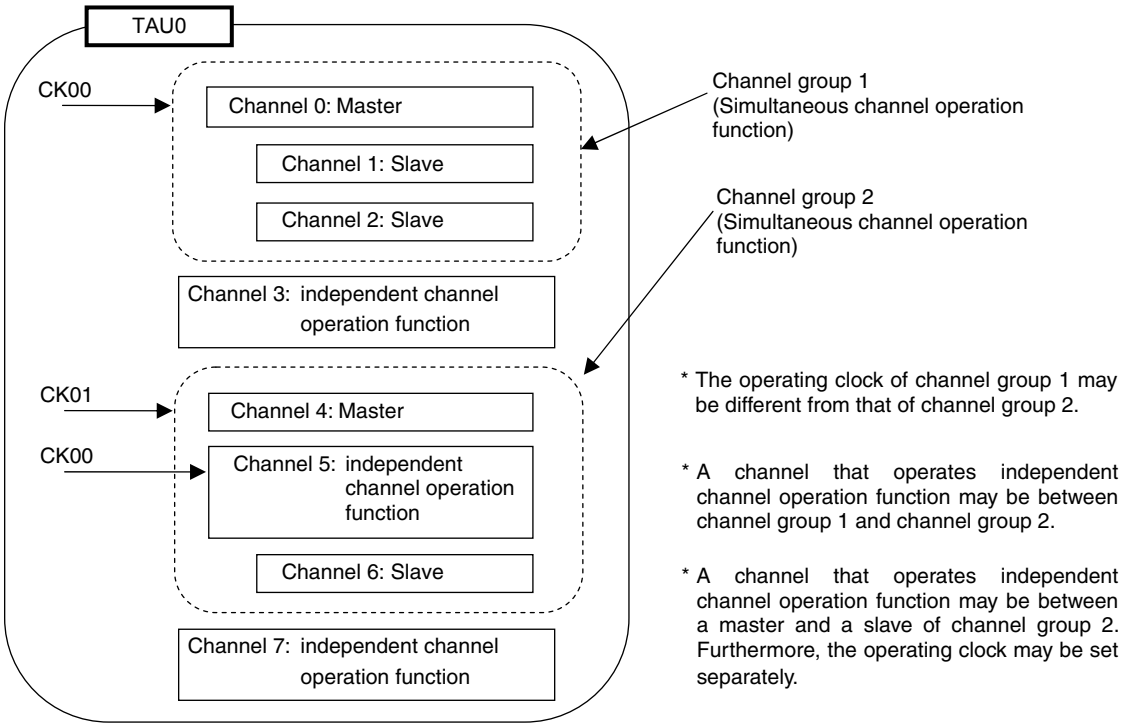
(6) The operating clock for a slave channel in combination with a master channel must be the same as that of the master channel. The CKS bit (bit 15 of timer mode register mn (TMRmn)) of the slave channel that operates in combination with the master channel must be the same value as that of the master channel.
(7) A master channel can transmit INTTMmn (interrupt), start software trigger, and count clock to the lower channels.
(8) A slave channel can use INTTMmn (interrupt), a start software trigger, or the count clock of the master channel as a source clock, but cannot transmit its own INTTMmn (interrupt), start software trigger, or count clock to channels with lower channel numbers.
(9) A master channel cannot use INTTMmn (interrupt), a start software trigger, or the count clock from the other higher master channel as a source clock.
(10) To simultaneously start channels that operate in combination, the channel start trigger bit (TSmn) of the channels in combination must be set at the same time.
(11) To stop the channels in combination simultaneously, the channel stop trigger bit (TTmn) of the channels in combination must be set at the same time.

The rules of the simultaneous channel operation function are applied in a channel group (a master channel and slave channels forming one simultaneous channel operation function).

If two or more channel groups that do not operate in combination are specified, the basic rules of the simultaneous channel operation function in **8.4 Basic Rules of Simultaneous Channel Operation Function** do not apply to the channel groups.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Example



* The operating clock of channel group 1 may be different from that of channel group 2.

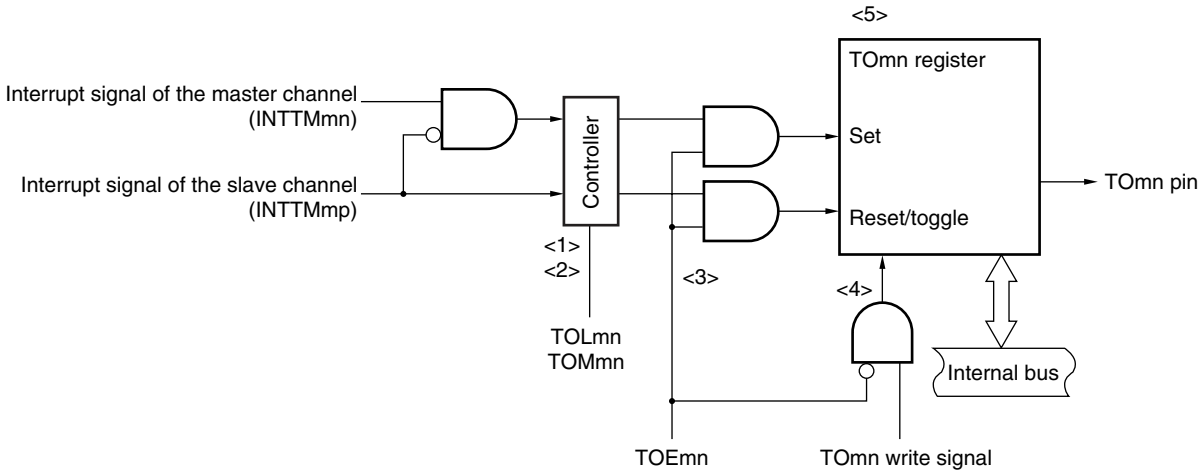
* A channel that operates independent channel operation function may be between channel group 1 and channel group 2.

* A channel that operates independent channel operation function may be between a master and a slave of channel group 2. Furthermore, the operating clock may be set separately.

8.5 Channel Output (TOmn pin) Control

8.5.1 TOmn pin output circuit configuration

Figure 8-30. Output Circuit Configuration



The following describes the TOmn pin output circuit.

<1> When TOMmn = 0 (master channel output mode), the set value of timer output level register m (TOLm) is ignored and only INTTMmp (slave channel timer interrupt) is transmitted to timer output register m (TOm).

<2> When TOMmn = 1 (slave channel output mode), both INTTMmn (master channel timer interrupt) and INTTMmp (slave channel timer interrupt) are transmitted to the TOm register.
At this time, the TOLm register becomes valid and the signals are controlled as follows:

When TOLmn = 0:	Forward operation (INTTMmn → set, INTTMmp → reset)
When TOLmn = 1:	Reverse operation (INTTMmn → reset, INTTMmp → set)

When INTTMmn and INTTMmp are simultaneously generated, (0% output of PWM), INTTMmp (reset signal) takes priority, and INTTMmn (set signal) is masked.

<3> While timer output is enabled (TOEmn = 1), INTTMmn (master channel timer interrupt) and INTTMmp (slave channel timer interrupt) are transmitted to the TOm register. Writing to the TOm register (TOmn write signal) becomes invalid.
When TOEmn = 1, the TOmn pin output never changes with signals other than interrupt signals.
To initialize the TOmn pin output level, it is necessary to set timer operation is stopeed (TOEmn = 0) and to write a value to the TOm register.

<4> While timer output is disabeled (TOEmn = 0), writing to the TOmn bit to the target channel (TOmn write signal) becomes valid. When timer output is disabeled (TOEmn = 0), neither INTTMmn (master channel timer interrupt) nor INTTMmp (slave channel timer interrupt) is transmitted to the TOm register.

<5> The TOm register can always be read, and the TOmn pin output level can be checked.

(**Remark** is listed on the next page.)

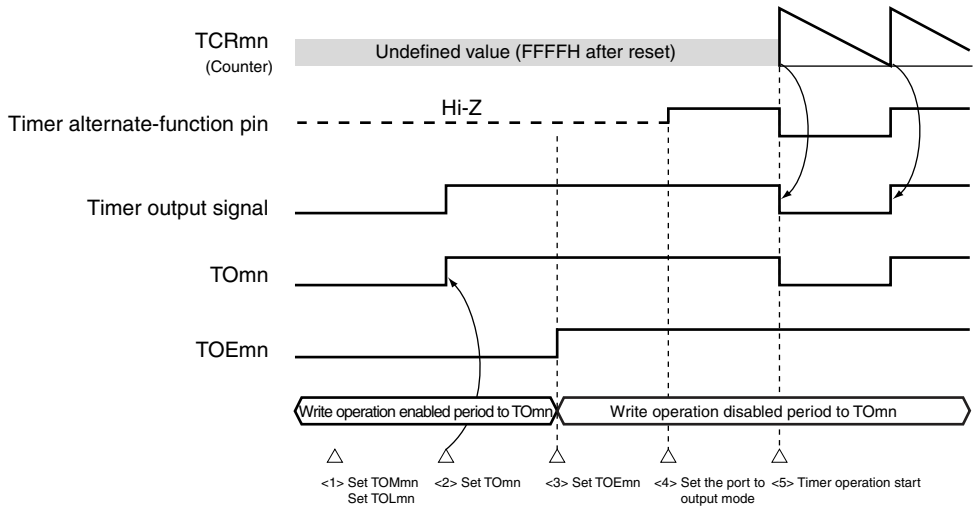
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13
p: Slave channel number [Note]
When m = 0: Master channel n = 0, 2, 4, 6, $n < p \leq 7$
When m = 1: Master channel n = 0, 2, $n < p \leq 3$
(Where p is a consecutive integer greater than n)

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

8.5.2 TOmn Pin Output Setting

The following figure shows the procedure and status transition of the TOmn output pin from initial setting to timer operation start.

Figure 8-31. Status Transition from Timer Output Setting to Operation Start



<1> The operation mode of timer output is set.

- TOMmn bit (0: Master channel output mode, 1: Slave channel output mode)
- TOLmn bit (0: Forward output, 1: Reverse output)

<2> The timer output signal is set to the initial status by setting timer output register m (TOm).

<3> The timer output operation is enabled by writing 1 to the TOEmn bit (writing to the TOm register is disabled).

<4> The port I/O setting is set to output (see **8.3 (15) Port mode registers 0, 1, 3 to 6, 13, 14 (PM0, PM1, PM3 to PM6, PM13, PM14)**).

<5> The timer operation is enabled (TSmn = 1).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.5.3 Cautions on Channel Output Operation

(1) Changing values set in the registers TOm, TOEm, TOLm, and TOMm during timer operation

Since the timer operations (operations of timer/counter register mn (TCRmn) and timer data register mn (TDRmn)) are independent of the TOmn output circuit and changing the values set in timer output register m (TOm), timer output enable register m (TOEm), timer output level register m (TOLm), and timer output mode register m (TOMm) does not affect the timer operation, the values can be changed during timer operation. To output an expected waveform from the TOmn pin by timer operation, however, set the TOm, TOEm, TOLm, and TOMm registers to the values stated in the register setting example of each operation.

When the values set to the TOEm, TOLm, and TOMm registers (but not the TOm register) are changed close to the occurrence of the timer interrupt (INTTMmn) of each channel, the waveform output to the TOmn pin might differ, depending on whether the values are changed immediately before or immediately after the timer interrupt (INTTMmn) occurs.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.

78K0R/KC3-L (40-pin):	mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin):	mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L:	mn = 00 to 07, 10 to 13

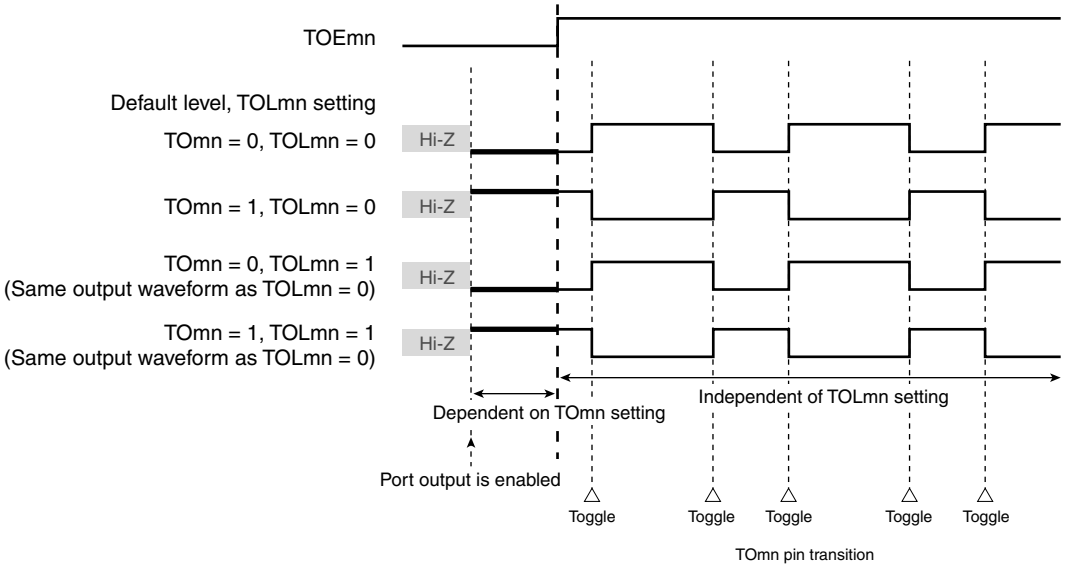
(2) Default level of TOmn pin and output level after timer operation start

The change in the output level of the TOmn pin when timer output register m (TOm) is written while timer output is disabled (TOEmn = 0), the initial level is changed, and then timer output is enabled (TOEmn = 1) before port output is enabled, is shown below.

(a) When operation starts with master channel output mode (TOMmn = 0) setting

The setting of timer output level register m (TOLm) is invalid when master channel output mode (TOMmn = 0). When the timer operation starts after setting the default level, the toggle signal is generated and the output level of the TOmn pin is reversed.

Figure 8-32. TOmn Pin Output Status at Toggle Output (TOMmn = 0)



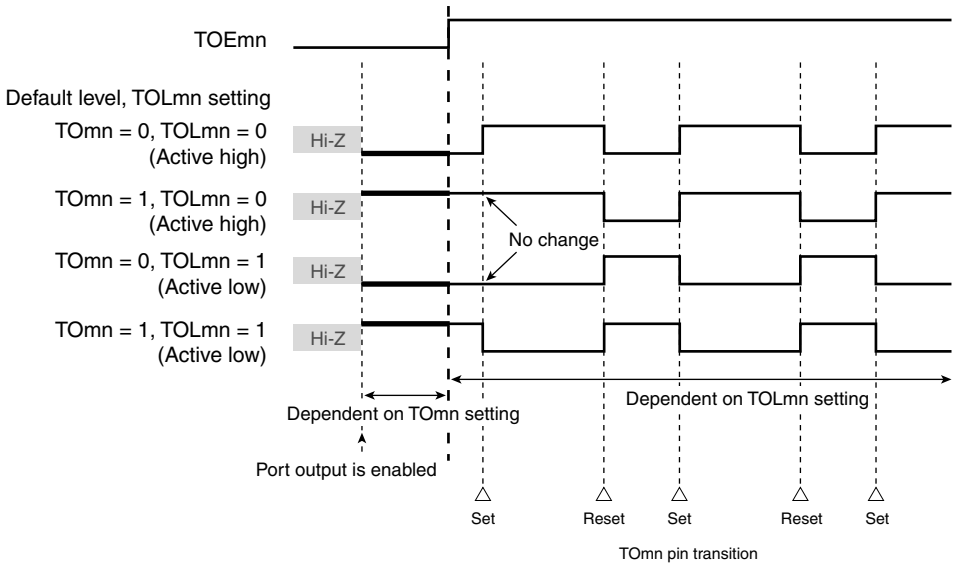
Remarks 1. Toggle: Reverse TOmn pin output status

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(b) When operation starts with slave channel output mode (TOMmn = 1) setting (PWM output))

When slave channel output mode (TOMmn = 1), the active level is determined by timer output level register m (TOLm) setting.

Figure 8-33. TOmn Pin Output Status at PWM Output (TOMmn = 1)



Remarks 1. Set: The output signal of the TOmn pin changes from inactive level to active level.
Reset: The output signal of the TOmn pin changes from active level to inactive level.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

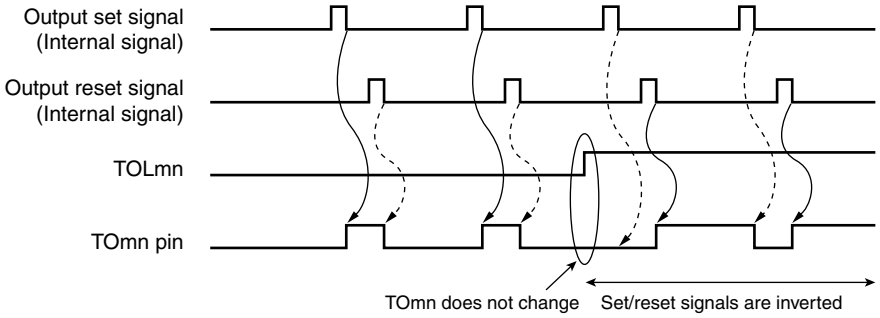
(3) Operation of TOmn pin in slave channel output mode (TOMmn = 1)

(a) When timer output level register m (TOLm) setting has been changed during timer operation

When the TOLm register setting has been changed during timer operation, the setting becomes valid at the generation timing of the TOmn pin change condition. Rewriting the TOLm register does not change the output level of the TOmn pin.

The operation when TOMmn is set to 1 and the value of the TOLm register is changed while the timer is operating (TEmn = 1) is shown below.

Figure 8-34. Operation when TOLm Register Has Been Changed during Timer Operation



Remarks 1. Set: The output signal of the TOmn pin changes from inactive level to active level.
Reset: The output signal of the TOmn pin changes from active level to inactive level.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(b) Set/reset timing

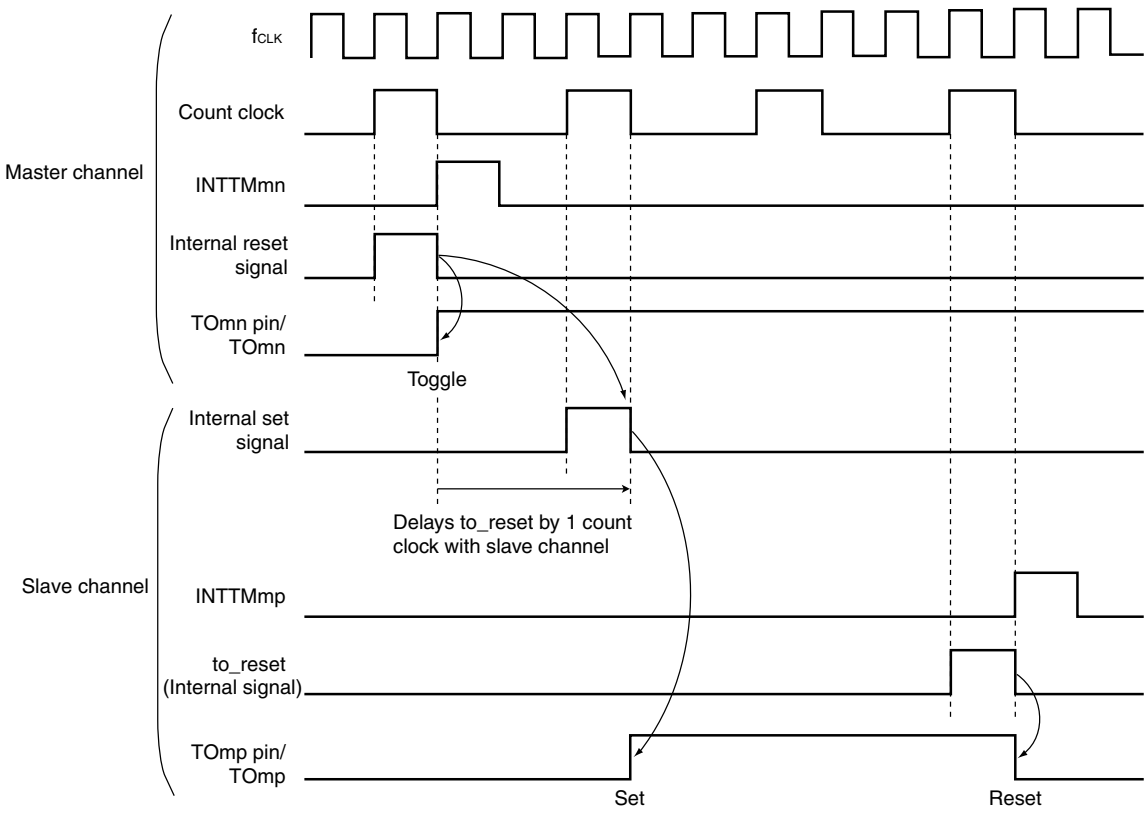
To realize 0%/100% output at PWM output, the TOmn pin/TOmn bit set timing at master channel timer interrupt (INTTMmn) generation is delayed by 1 count clock by the slave channel.

If the set condition and reset condition are generated at the same time, a higher priority is given to the latter.

Figure 8-35 shows the set/reset operating statuses where the master/slave channels are set as follows.

Master channel: TOEmn = 1, TOMmn = 0, TOLmn = 0
Slave channel: TOEmp = 1, TOMmp = 1, TOLmp = 0

Figure 8-35. Set/Reset Timing Operating Statuses



Remarks 1. Internal reset signal: TOmn pin reset/toggle signal
Internal set signal: TOmn pin set signal

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13
p: Slave channel number [Note]
When m = 0: Master channel n = 0, 2, 4, 6, $n < p \leq 7$
When m = 1: Master channel n = 0, 2, $n < p \leq 3$
(Where p is a consecutive integer greater than n)

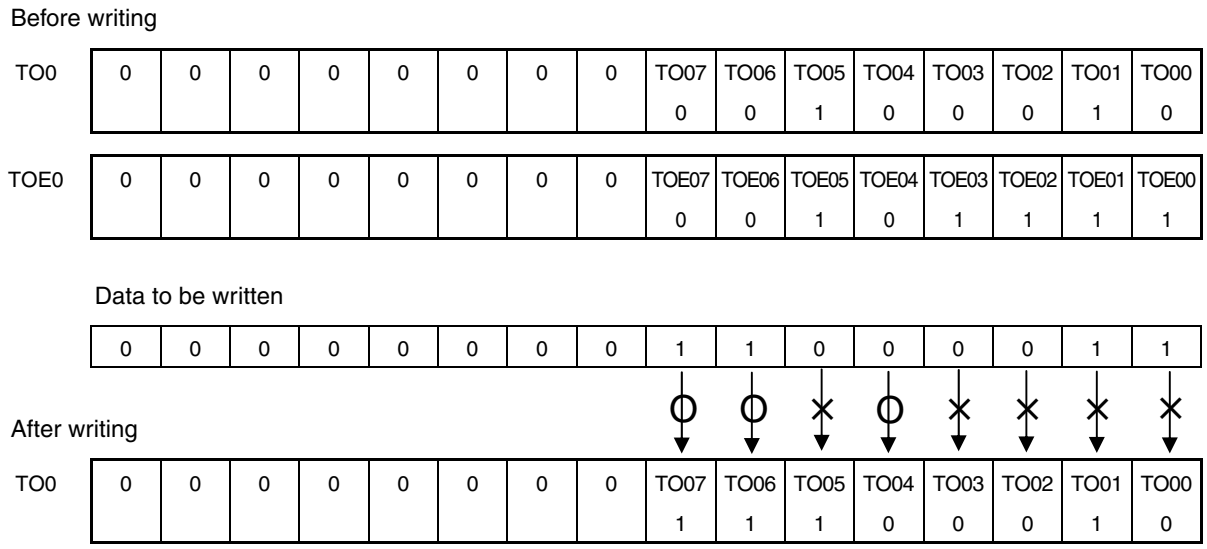
Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

8.5.4 Collective manipulation of TOmn bit

In timer output register m (TOm), the setting bits for all the channels are located in one register in the same way as timer channel start register m (TSm). Therefore, the TOmn bit of all the channels can be manipulated collectively.

Only the desired bits can also be manipulated by enabling writing only to the TOmn bits (TOEmn = 0) that correspond to the relevant bits of the channel used to perform output (TOmn).

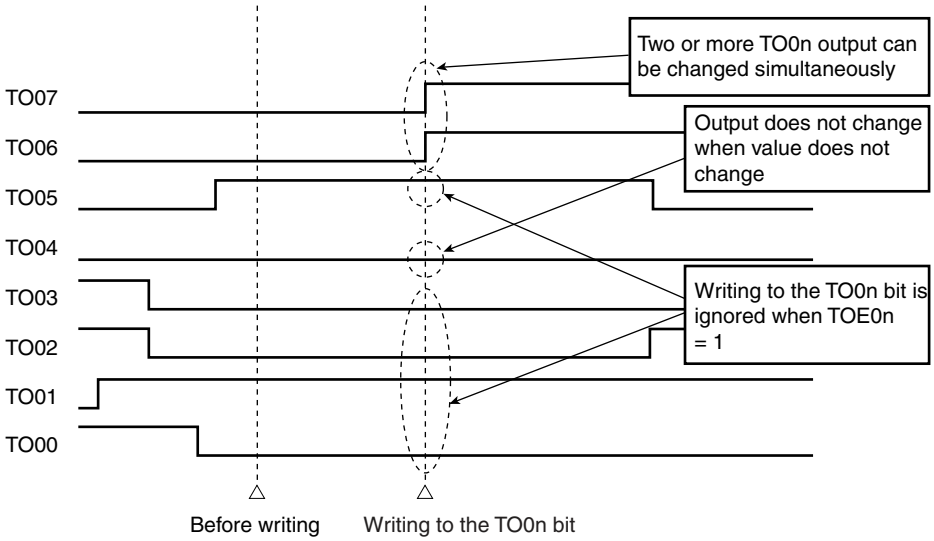
Figure 8-36. Example of TOmn Bit Collective Manipulation



Writing is done only to the TOmn bit with TOEmn = 0, and writing to the TOmn bit with TOEmn = 1 is ignored.

TOmn (channel output) to which TOEmn = 1 is set is not affected by the write operation. Even if the write operation is done to the TOmn bit, it is ignored and the output change by timer operation is normally done.

Figure 8-37. TOmn Pin Statuses by Collective Manipulation of TOmn Bit



(Caution and Remark are given on the next page.)

Caution While timer output is enabled (TOEmn = 1), even if the output by timer interrupt of each timer (INTTMmn) contends with writing to the TOmn bit, output is normally done to the TOmn pin.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.5.5 Timer Interrupt and TOmn Pin Output at Operation Start

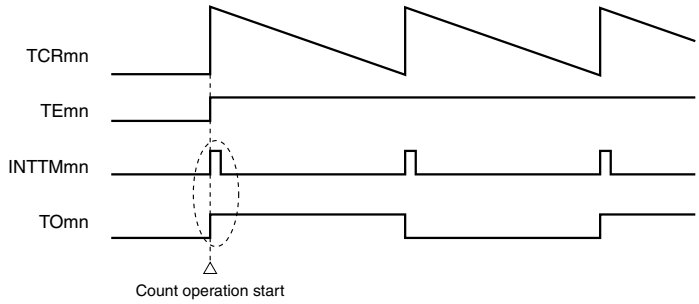
In the interval timer mode or capture mode, the MDmn0 bit in timer mode register mn (TMRmn) sets whether or not to generate a timer interrupt at count start.

When MDmn0 is set to 1, the count operation start timing can be known by the timer interrupt (INTTMmn) generation.

In the other modes, neither timer interrupt at count operation start nor TOmn output is controlled.

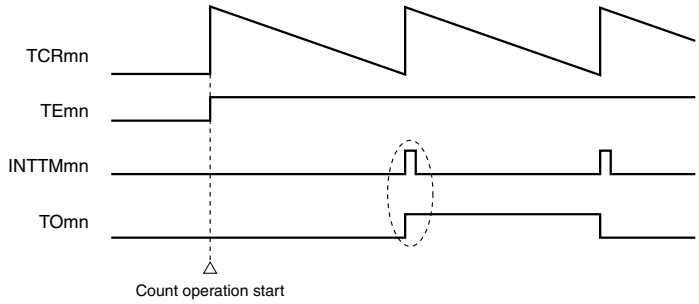
Figures 8-37 and 8-38 show operation examples when the interval timer mode (TOEmn = 1, TOMmn = 0) is set.

Figure 8-38. When MDmn0 is set to 1



When MDmn0 is set to 1, a timer interrupt (INTTMmn) is output at count operation start, and TOmn performs a toggle operation.

Figure 8-39. When MDmn0 is set to 0



When MDmn0 is set to 0, a timer interrupt (INTTMmn) is not output at count operation start, and TOmn does not change either. After counting one cycle, INTTMmn is output and TOmn performs a toggle operation.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

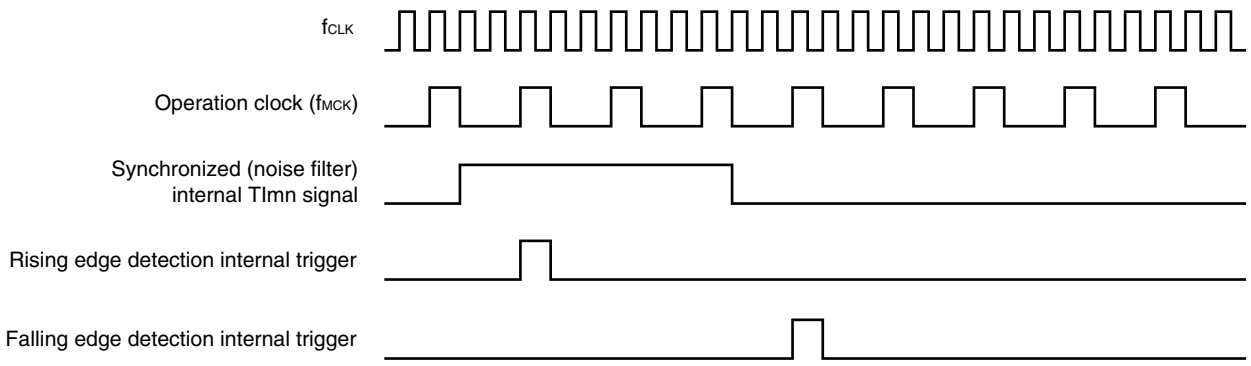
8.6 Channel Input (TImn Pin) Control

8.6.1 TImn edge detection circuit

(1) Edge detection basic operation timing

Edge detection circuit sampling is done in accordance with the operation clock (f_{MCK}).

Figure 8-40. Edge Detection Basic Operation Timing



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn) and the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.7 Independent Channel Operation Function of Timer Array Unit

8.7.1 Operation as interval timer/square wave output

(1) Interval timer

The timer array unit can be used as a reference timer that generates INTTMmn (timer interrupt) at fixed intervals. The interrupt generation period can be calculated by the following expression.

Generation period of INTTMmn (timer interrupt) = Period of count clock × (Set value of TDRmn + 1)

In products other than the 78K0R/KC3-L (40-pin), A subsystem clock divided by four ($f_{SUB}/4$) can be selected as the count clock, in addition to CKm0 and CKm1. Consequently, the interval timer can be operated with the count clock fixed to $f_{SUB}/4$, regardless of the f_{CLK} frequency (main system clock, subsystem clock). However, be sure to change the clock selected as f_{CLK} (change the value of the system clock control register (CKC)) after stopping all channels of timer array unit (timer channel stop register m (TTm) = 00FFH).

(2) Operation as square wave output

TOmn performs a toggle operation as soon as INTTMmn has been generated, and outputs a square wave with a duty factor of 50%.

The period and frequency for outputting a square wave from TOmn can be calculated by the following expressions.

- Period of square wave output from TOmn = Period of count clock × (Set value of TDRmn + 1) × 2
- Frequency of square wave output from TOmn = Frequency of count clock/{(Set value of TDRmn + 1) × 2}

Timer/counter register mn (TCRmn) operates as a down counter in the interval timer mode.

The TCRmn register loads the value of timer data register mn (TDRmn) at the first count clock after the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1. If the MDmn0 bit of timer mode register mn (TMRmn) is 0 at this time, INTTMmn is not output and TOmn is not toggled. If the MDmn0 bit of the TMRmn register is 1, INTTMmn is output and TOmn is toggled.

After that, the TCRmn register count down in synchronization with the count clock.

When TCRmn = 0000H, INTTMmn is output and TOmn is toggled at the next count clock. At the same time, the TCRmn register loads the value of the TDRmn register again. After that, the same operation is repeated.

The TDRmn register can be rewritten at any time. The new value of the TDRmn register becomes valid from the next period.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the operation of square wave output and the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

2. f_{CLK}: CPU/peripheral hardware clock frequency
f_{SUB}: Subsystem clock oscillation frequency

Figure 8-41. Block Diagram of Operation as Interval Timer/Square Wave Output

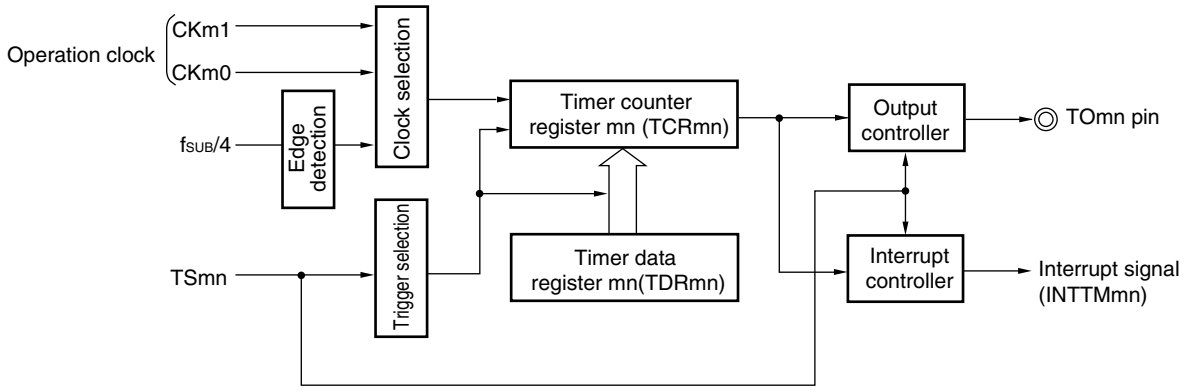
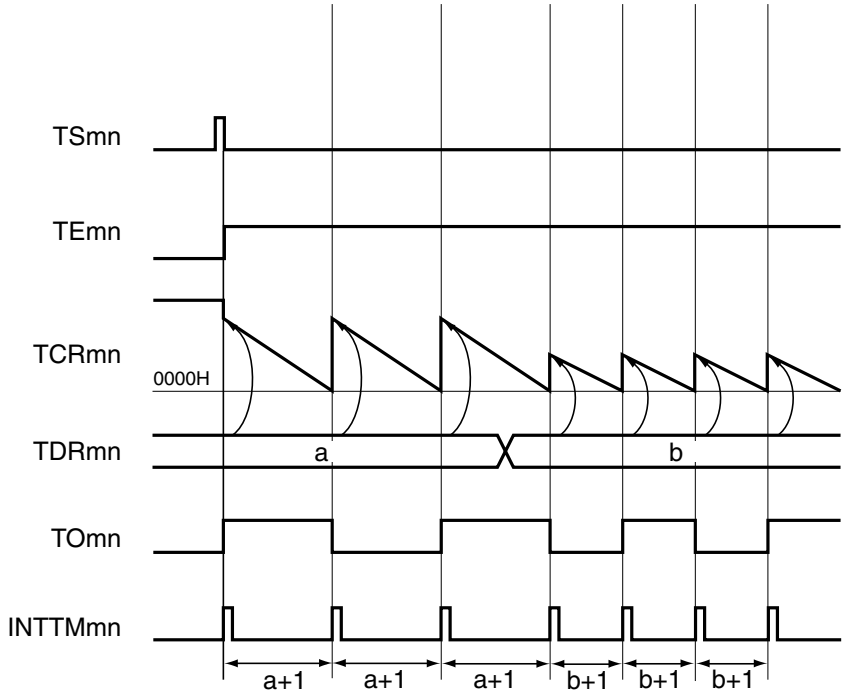


Figure 8-42. Example of Basic Timing of Operation as Interval Timer/Square Wave Output (MDmn0 = 1)



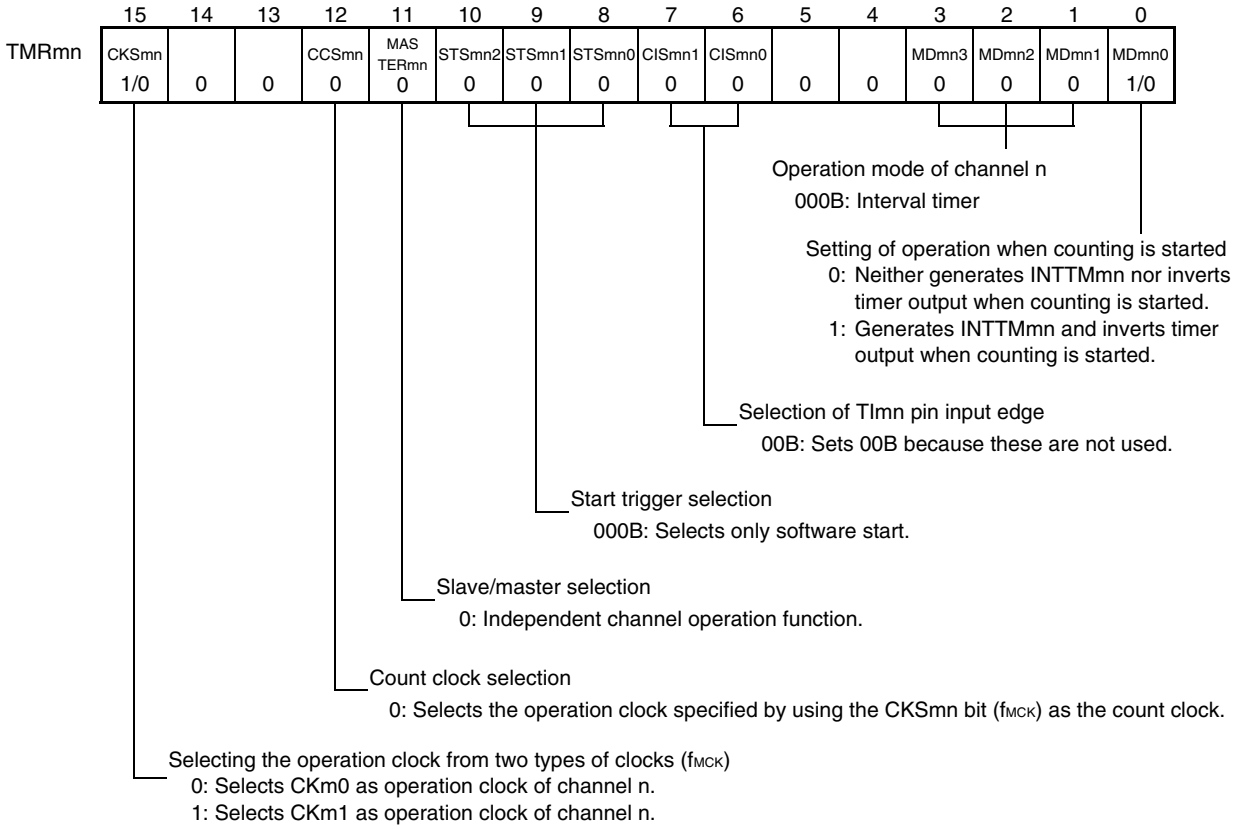
Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the operation of square wave output and the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

2. TSmn: Bit n of timer channel start register m (TSm)
TEmn: Bit n of timer channel enable status register m (TEm)
TCRmn: Timer/counter register mn (TCRmn)
TDRmn: Timer data register mn (TDRmn)
TOmn: TOmn pin output signal

Figure 8-43. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (1/3)

(1) When CKm0 or CKm1 is selected as count clock

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn 1/0	0: Outputs 0 from TOmn. 1: Outputs 1 from TOmn.

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn 1/0	0: Stops the TOmn output operation by counting operation. 1: Enables the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn 0	0: Cleared to 0 when TOMmn = 0 (master channel output mode)

(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn 0	0: Sets master channel output mode.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the operation of square wave output and the timer output pin (TOmn), mn changes as below.

78K0R/KC3-L (40-pin):	mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin):	mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L:	mn = 00 to 07, 10 to 13

Figure 8-43. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (2/3)

(2) When f_{SUB}/4 is selected as count clock (products other than 78K0R/KC3-L (40-pin))

(a) Timer mode register mn (TMRmn)

TMRmn

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKSmn			CCSmn	MAS TERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0			MDmn3	MDmn2	MDmn1	MDmn0
1/0	0	0	1	0	0	0	0	1/0	1/0	0	0	0	0	0	1/0

Operation mode of channel n
000B: Interval timer

Setting of operation when counting is started
0: Neither generates INTTMmn nor inverts timer output when counting is started.
1: Generates INTTMmn and inverts timer output when counting is started.

f_{SUB}/4 edge selection
00B: Detects falling edge (counts on f_{SUB}/4 cycles).
01B: Detects rising edge (counts on f_{SUB}/4 cycles).
10B: Detects both edges (counts on f_{SUB}/2 cycles).
11B: Setting prohibited

Start trigger selection
000B: Selects only software start.

Slave/master selection
0: Independent channel operation function.

Count clock selection
1: Selects subsystem clock divided by four (f_{SUB}/4).

Operation clock selection
0: Selects CKm0 as operation clock of channel n.
1: Selects CKm1 as operation clock of channel n.
f_{CLK} (no division) is selected as selected operation clock by the TPSm register.

(b) Timer clock select register m (TPSm)

TPSm

Bits 7 to 4, 3 to 0
PRSmk3 to PRSmk0
0000

0000B: Selects f_{CLK} (no division) as operation clock selected by the CKSmn bit of the TMRmn register.
k = 0 (bits 0 to 3) when CKm0 is selected and k = 1 (bits 4 to 7) when CKm1 is selected

(c) Timer input select register m (TISm)

TISm

Bit n
TISmn
1

1: Selects subsystem clock divided by four (f_{SUB}/4).

(d) Timer output register m (TOm)

TOm

Bit n
TOmn
1/0

0: Outputs 0 from TOmn.
1: Outputs 1 from TOmn.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the operation of square wave output and the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

2. f_{SUB}: Subsystem clock oscillation frequency

Figure 8-43. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (3/3)

(2) When f_{SUB}/4 is selected as count clock (continued)

(e) Timer output enable register m (TOEm)

	Bit n		
TOEm	TOEmn	0: Stops the TOmn output operation by counting operation.	
	1/0	1: Enables the TOmn output operation by counting operation.	

(f) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn	0: Cleared to 0 when TOMmn = 0 (master channel output mode)
	0	

(g) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn	0: Sets master channel output mode.
	0	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the operation of square wave output and the timer output pin (TOmn), mn changes as below.

78K0R/KC3-L (40-pin):	mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin):	mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L:	mn = 00 to 07, 10 to 13

Figure 8-44. Operation Procedure of Interval Timer/Square Wave Output Function (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode register mn (TMRmn) (determines operation mode of channel). Sets the TISmn bit to 1 (f_{SUB}/4) when f_{SUB}/4 is selected as the count clock. Sets interval (period) value to timer data register mn (TDRmn).	Channel stops operating. (Clock is supplied and some power is consumed.)
	To use the TOmn output Clears the TOMmn bit of timer output mode register m (TOMm) to 0 (master channel output mode). Clears the TOLmn bit to 0. Sets the TOmn bit and determines default level of the TOmn output. →	The TOmn pin goes into Hi-Z output state. The TOmn default setting level is output when the port mode register is in the output mode and the port register is 0.
	Sets the TOEmn bit to 1 and enables operation of TOmn. →	TOmn does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmn pin outputs the TOmn set level.
Operation start	(Sets the TOEmn bit to 1 only if using TOmn output and resuming operation.). Sets the TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and count operation starts. Value of the TDRmn register is loaded to timer/counter register mn (TCRmn) at the count clock input. INTTMmn is generated and TOmn performs toggle operation if the MDmn0 bit of the TMRmn register is 1.
During operation	Set values of the TMRmn register, TOMmn, and TOLmn bits cannot be changed. Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TOm and TOEm registers can be changed.	Counter (TCRmn) counts down. When count value reaches 0000H, the value of the TDRmn register is loaded to the TCRmn register again and the count operation is continued. By detecting TCRmn = 0000H, INTTMmn is generated and TOmn performs toggle operation. After that, the above operation is repeated.
Operation stop	The TTmn bit is set to 1. → The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops. The TOmn output is not initialized but holds current status.
	The TOEmn bit is cleared to 0 and value is set to the TOmn bit. →	The TOmn pin outputs the TOmn bit set level.

Operation is resumed.

(**Note** and **Remark** are listed on the next page.)

Figure 8-44. Operation Procedure of Interval Timer/Square Wave Output Function (2/2)

	Software Operation	Hardware Status
TAU stop	To hold the TOmn pin output level Clears the TOmn bit to 0 after the value to be held is set to the port register. →	The TOmn pin output level is held by port function.
	When holding the TOmn pin output level is not necessary Switches the port mode register to input mode. →	The TOmn pin output level goes into Hi-Z output state.
	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0.[Note] →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmn bit is cleared to 0 and the TOmn pin is set to port mode.)

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the operation of square wave output and the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.7.2 Operation as external event counter

The timer array unit can be used as an external event counter that counts the number of times the valid input edge (external event) is detected in the TImn pin. When a specified count value is reached, the event counter generates an interrupt. The specified number of counts can be calculated by the following expression.

Specified number of counts = Set value of TDRmn + 1

Timer/counter register mn (TCRmn) operates as a down counter in the event counter mode.

The TCRmn register loads the value of timer data register mn (TDRmn) by setting any channel start trigger bit (TSmn) of timer channel start register m (TSm) to 1.

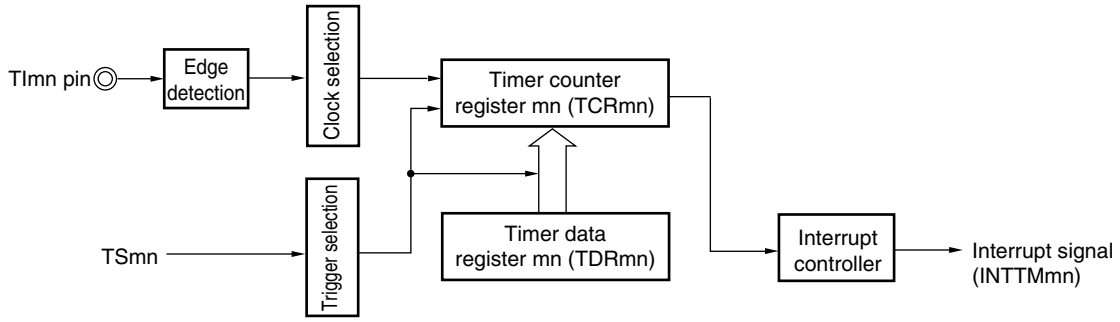
The TCRmn register counts down each time the valid input edge of the TImn pin has been detected. When TCRmn = 0000H, the TCRmn register loads the value of the TDRmn register again, and outputs INTTMmn.

After that, the above operation is repeated.

An irregular waveform that depends on external events is output from the TOmn pin. Stop the output by setting the TOEmn bit of timer output enable register m (TOEm) to 0.

The TDRmn register can be rewritten at any time. The new value of the TDRmn register becomes valid during the next count period.

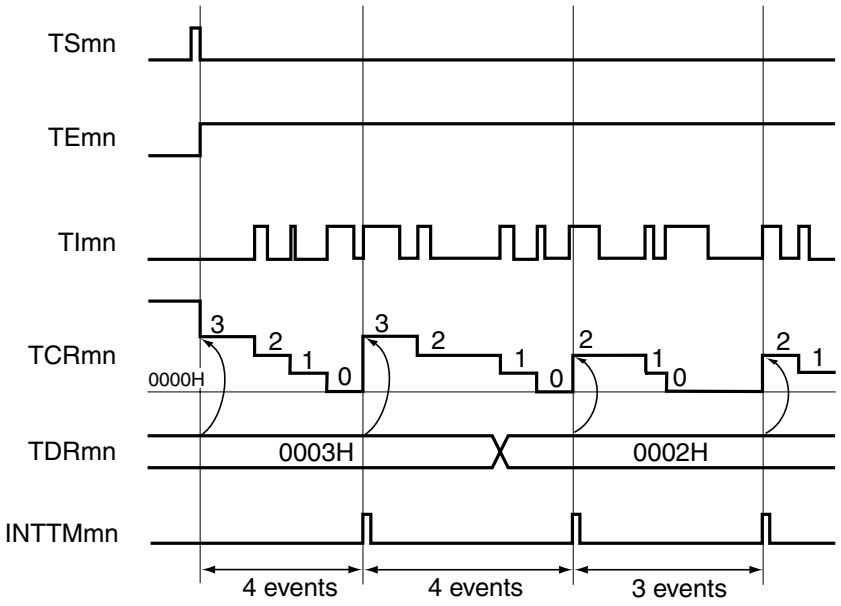
Figure 8-45. Block Diagram of Operation as External Event Counter



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

78K0R/KC3-L (40-pin):	mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin):	mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L:	mn = 00 to 07, 10 to 13

Figure 8-46. Example of Basic Timing of Operation as External Event Counter



Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

78K0R/KC3-L (40-pin): mn = 02 to 07

78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07

78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07

78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

2. TSmn: Bit n of timer channel start register m (TSm)

TEmn: Bit n of timer channel enable status register m (TEm)

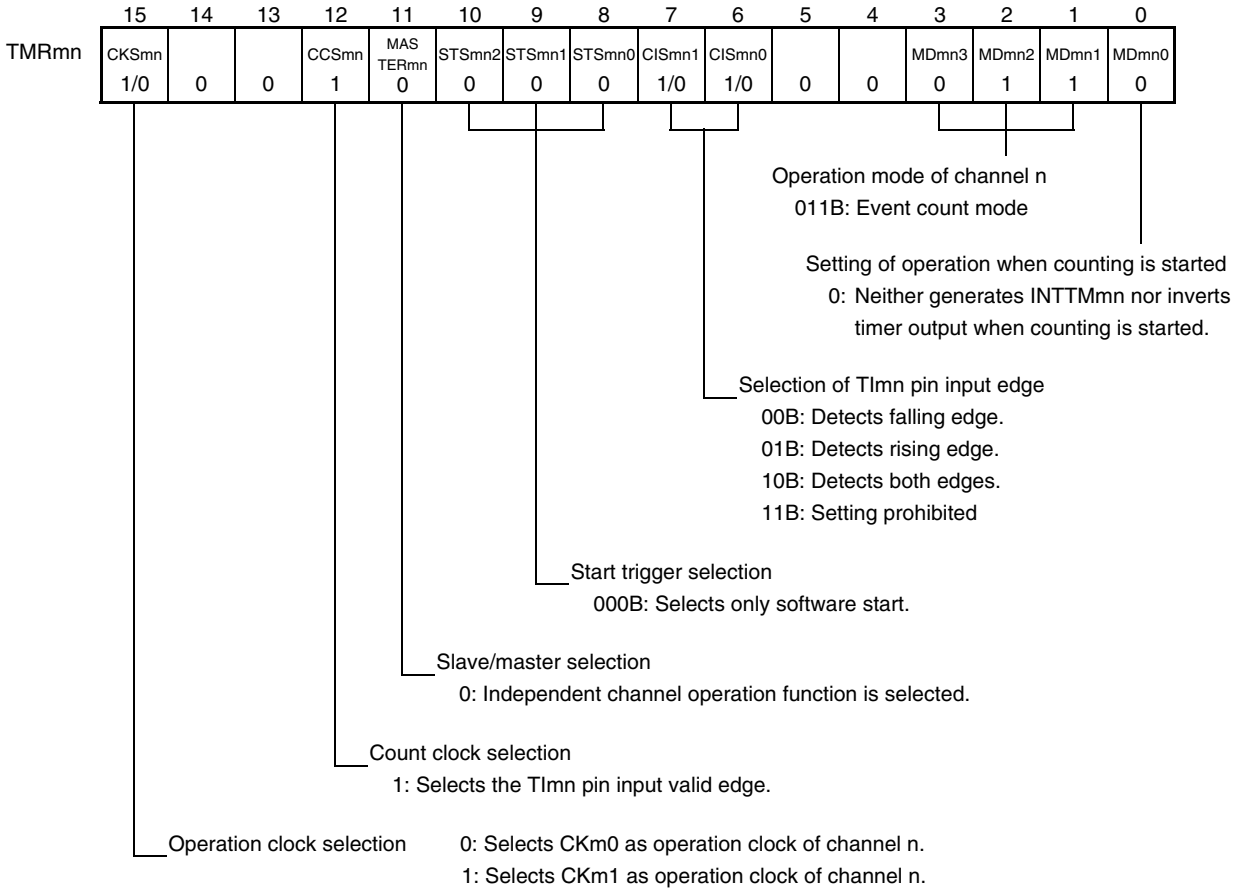
TImn: TImn pin input signal

TCRmn: Timer/counter register mn (TCRmn)

TDRmn: Timer data register mn (TDRmn)

Figure 8-47. Example of Set Contents of Registers in External Event Counter Mode

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn	0: Outputs 0 from TOmn.
	0	

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn	0: Stops the TOmn output operation by counting operation.
	0	

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn	0: Cleared to 0 when TOMmn = 0 (master channel output mode).
	0	

(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn	0: Sets master channel output mode.
	0	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-48. Operation Procedure When External Event Counter Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode register mn (TMRmn) (determines operation mode of channel). Sets number of counts to timer data register mn (TDRmn). Clears the TOEmn bit of timer output enable register m (TOEm) to 0.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and count operation starts. Value of the TDRmn register is loaded to timer/counter register mn (TCRmn) and detection of the TImn pin input edge is awaited.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	Counter (TCRmn) counts down each time input edge of the TImn pin has been detected. When count value reaches 0000H, the value of the TDRmn register is loaded to the TCRmn register again, and the count operation is continued. By detecting TCRmn = 0000H, the INTTMmn output is generated. After that, the above operation is repeated.
Operation stop	The TTmn bit is set to 1. → The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops.
TAU stop	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0. Note →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.7.3 Operation as frequency divider (channel 0 of 78K0R/KD3-L, KE3-L, KF3-L. KG3-L only)

The timer array unit can be used as a frequency divider that divides a clock input to the TI00 pin and outputs the result from the TO00 pin.

The divided clock frequency output from TO00 can be calculated by the following expression.

- When rising edge/falling edge is selected:
  Divided clock frequency = Input clock frequency/{(Set value of TDR00 + 1) × 2}
- When both edges are selected:
  Divided clock frequency ≅ Input clock frequency/(Set value of TDR00 + 1)

Timer/counter register 00 (TCR00) operates as a down counter in the interval timer mode.

After the channel start trigger bit (TS00) of timer channel start register 0 (TS0) is set to 1, the TCR00 register loads the value of timer data register 00 (TDR00) when the TI00 valid edge is detected.

If the MD000 bit of timer mode register 00 (TMR00) is 0 at this time, INTTM00 is not output and TO00 is not toggled. If the MD000 bit of timer mode register 00 (TMR00) is 1, INTTM00 is output and TO00 is toggled.

After that, the TCR00 register counts down at the valid edge of the TI00 pin. When TCR00 = 0000H, it toggles TO00. At the same time, the TCR00 register loads the value of the TDR00 register again, and continues counting.

If detection of both the edges of the TI00 pin is selected, the duty factor error of the input clock affects the divided clock period of the TO00 output.

The period of the TO00 output clock includes a sampling error of one period of the operation clock.

Clock period of TO00 output = Ideal TO00 output clock period ± Operation clock period (error)

The TDR00 register can be rewritten at any time. The new value of the TDR00 register becomes valid during the next count period.

Figure 8-49. Block Diagram of Operation as Frequency Divider

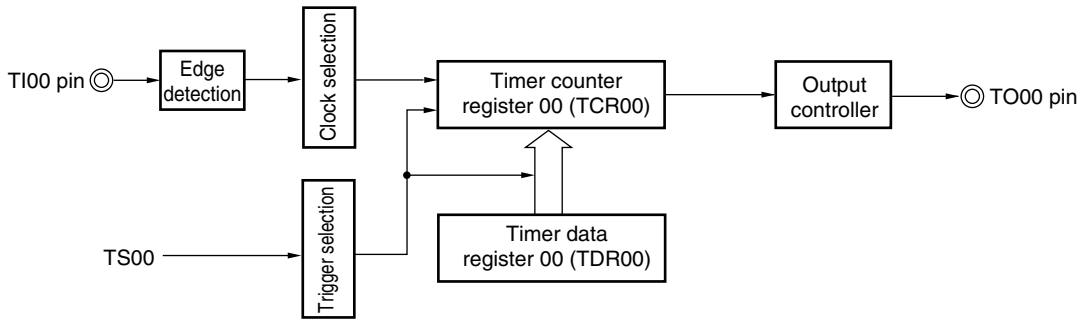
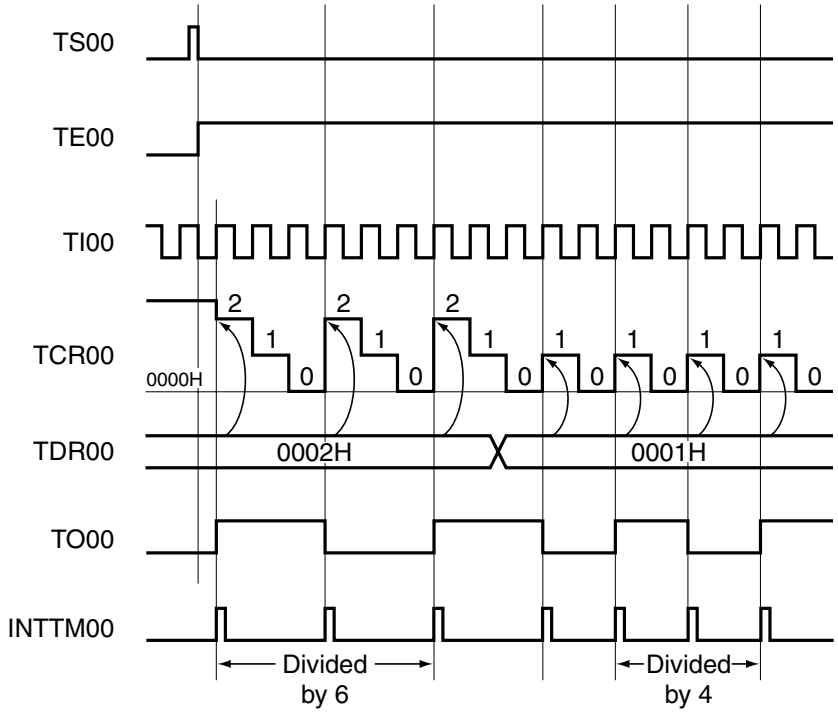


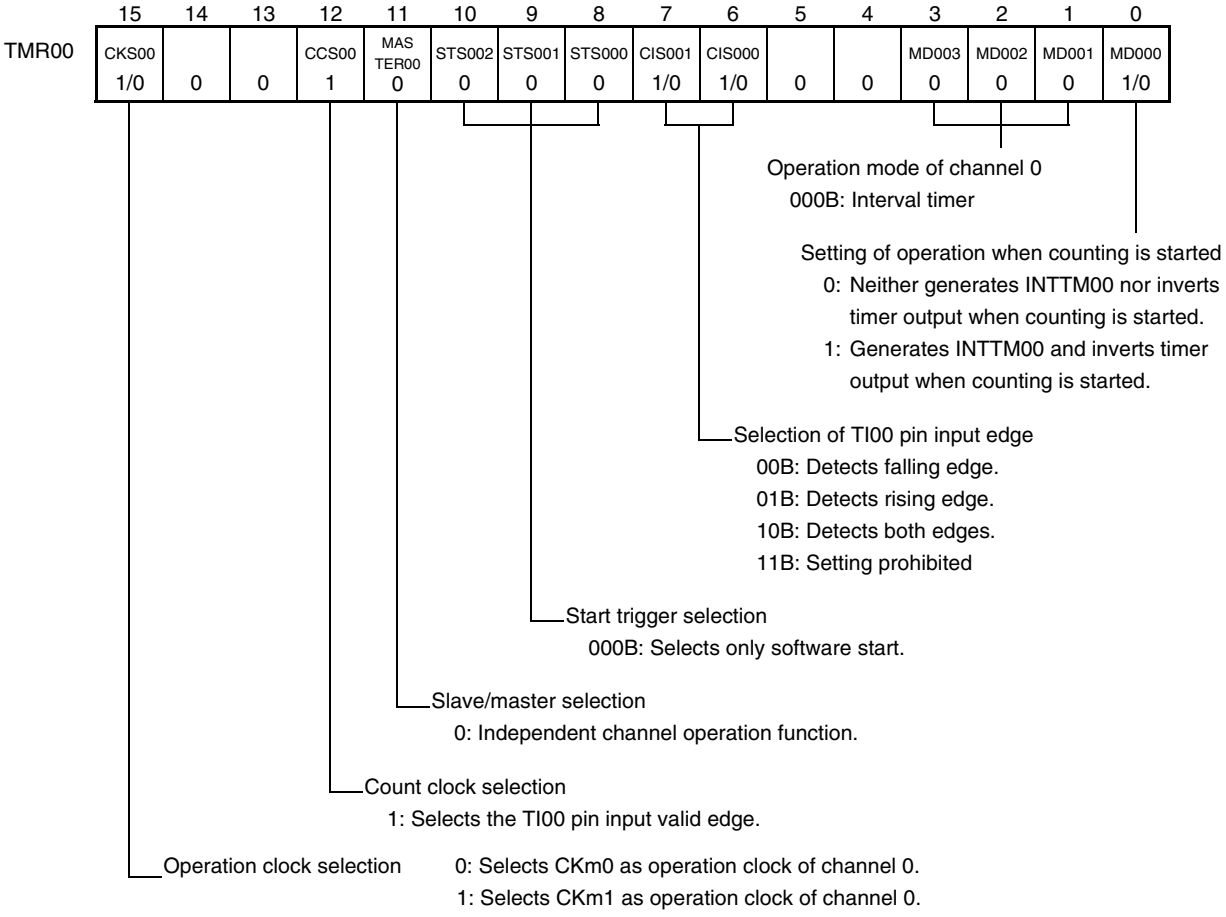
Figure 8-50. Example of Basic Timing of Operation as Frequency Divider (MD000 = 1)



Remark TS00: Bit n of timer channel start register 0 (TS0)
TE00: Bit n of timer channel enable status register 0 (TE0)
TI00: TI00 pin input signal
TCR00: Timer/counter register 00 (TCR00)
TDR00: Timer data register 00 (TDR00)
TO00: TO00 pin output signal

Figure 8-51. Example of Set Contents of Registers During Operation as Frequency Divider

(a) Timer mode register 00 (TMR00)



(b) Timer output register 0 (TO0)

	Bit 0	
TO0	TO00 1/0	0: Outputs 0 from TO00. 1: Outputs 1 from TO00.

(c) Timer output enable register 0 (TOE0)

	Bit 0	
TOE0	TOE00 1/0	0: Stops the TO00 output operation by counting operation. 1: Enables the TO00 output operation by counting operation.

(d) Timer output level register 0 (TOL0)

	Bit 0	
TOL0	TOL00 0	0: Cleared to 0 when TOM00 = 0 (master channel output mode)

(e) Timer output mode register 0 (TOM0)

	Bit 0	
TOM0	TOM00 0	0: Sets master channel output mode.

Figure 8-52. Operation Procedure When Frequency Divider Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN bit of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register 0 (TPS0). Determines clock frequencies of CK00 and CK01.	
Channel default setting	Sets timer mode register mn (TMRmn) (determines operation mode of channel and selects the detection edge). Sets interval (period) value to timer data register 00 (TDR00).	Channel stops operating. (Clock is supplied and some power is consumed.)
	Clears the TOM00 bit of timer output mode register 0 (TOM0) to 0 (master channel output mode). Clears the TOL00 bit to 0. Sets the TO00 bit and determines default level of the TO00 output. →	The TO00 pin goes into Hi-Z output state. The TO00 default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets the TOE00 bit to 1 and enables operation of TO00. →	TO00 does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TO00 pin outputs the TO00 set level.
Operation start	Sets the TOE00 bit to 1 (only when operation is resumed). Sets the TS00 bit to 1. → The TS00 bit automatically returns to 0 because it is a trigger bit.	TE00 = 1, and count operation starts. Value of the TDR00 register is loaded to timer/counter register 00 (TCR00) at the count clock input. INTTM00 is generated and TO00 performs toggle operation if the MD000 bit of the TMR00 register is 1.
During operation	Set value of the TDR00 register can be changed. The TCR00 register can always be read. The TSR00 register is not used. Set values of the TO0 and TOE0 registers can be changed. Set values of the TMR00 register, TOM00, and TOL00 bits cannot be changed.	Counter (TCR00) counts down. When count value reaches 0000H, the value of the TDR00 register is loaded to the TCR00 register again, and the count operation is continued. By detecting TCR00 = 0000H, INTTM00 is generated and TO00 performs toggle operation. After that, the above operation is repeated.
Operation stop	The TT00 bit is set to 1. → The TT00 bit automatically returns to 0 because it is a trigger bit.	TE00 = 0, and count operation stops. The TCR00 register holds count value and stops. The TO00 output is not initialized but holds current status.
	The TOE00 bit is cleared to 0 and value is set to the TO00 bit. →	The TO00 pin outputs the TO00 set level.
TAU stop	To hold the TO00 pin output level Clears the TO00 bit to 0 after the value to be held is set to the port register. →	The TO00 pin output level is held by port function.
	When holding the TO00 pin output level is not necessary Switches the port mode register to input mode. →	The TO00 pin output level goes into Hi-Z output state.
	The TAU0EN bit of the PER0 or PER2 register is cleared to 0. Note →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TO00 bit is cleared to 0 and the TO00 pin is set to port mode).

Operation is resumed. → Operation start

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN bit of the PER0 register

8.7.4 Operation as input pulse interval measurement

The count value can be captured at the TImn valid edge and the interval of the pulse input to TImn can be measured.

The pulse interval can be calculated by the following expression.

TImn input pulse interval = Period of count clock × ((10000H × TSRmn: OVF) + (Capture value of TDRmn + 1))

Caution The TImn pin input is sampled using the operating clock selected with the CKSmn bit of timer mode register mn (TMRmn), so an error of up to one operating clock cycle occurs.

Timer/counter register mn (TCRmn) operates as an up counter in the capture mode.

When the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, the TCRmn register counts up from 0000H in synchronization with the count clock.

When the TImn pin input valid edge is detected, the count value of the TCRmn register is transferred (captured) to timer data register mn (TDRmn) and, at the same time, the TCRmn register is cleared to 0000H, and the INTTMmn is output. If the counter overflows at this time, the OVF bit of timer status register mn (TSRmn) is set to 1. If the counter does not overflow, the OVF bit is cleared. After that, the above operation is repeated.

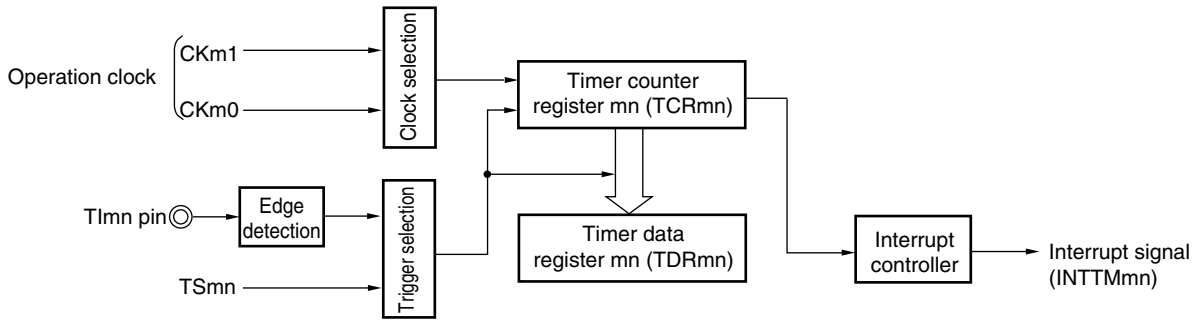
As soon as the count value has been captured to the TDRmn register, the OVF bit of the TSRmn register is updated depending on whether the counter overflows during the measurement period. Therefore, the overflow status of the captured value can be checked.

If the counter reaches a full count for two or more periods, it is judged to be an overflow occurrence, and the OVF bit of the TSRmn register is set to 1. However, a normal interval value cannot be measured for the OVF bit, if two or more overflows occur.

Set the STSmn2 to STSmn0 bits of the TMRmn register to 001B to use the valid edges of TImn as a start trigger and a capture trigger.

When TEmn = 1, a software operation (TSmn = 1) can be used as a capture trigger, instead of using the TImn pin input.

Figure 8-53. Block Diagram of Operation as Input Pulse Interval Measurement



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

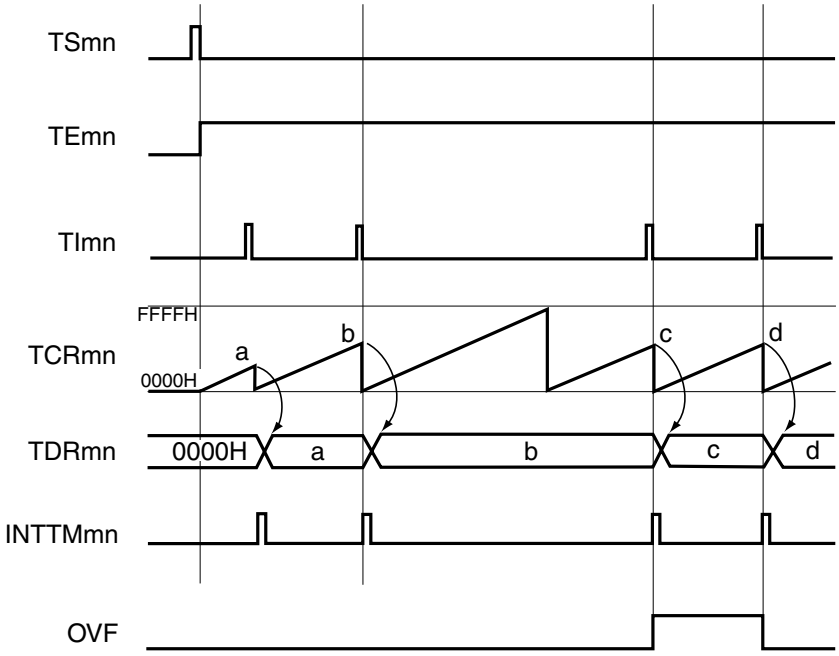
78K0R/KC3-L (40-pin): mn = 02 to 07

78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07

78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07

78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-54. Example of Basic Timing of Operation as Input Pulse Interval Measurement (MDmn0 = 0)



Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

78K0R/KC3-L (40-pin): mn = 02 to 07

78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07

78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07

78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

2. TSmn: Bit n of timer channel start register m (TSm)

TEmn: Bit n of timer channel enable status register m (TEm)

TImn: TImn pin input signal

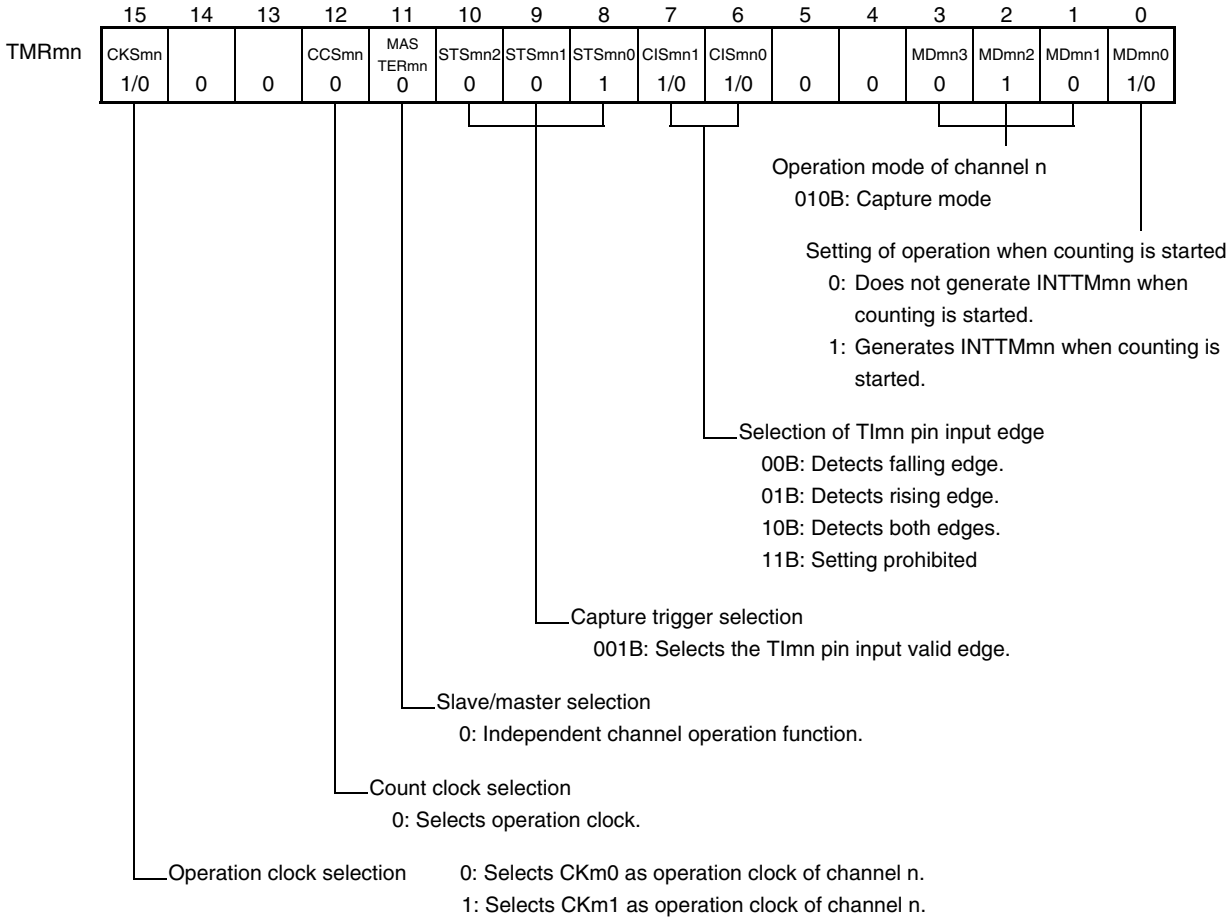
TCRmn: Timer/counter register mn (TCRmn)

TDRmn: Timer data register mn (TDRmn)

OVF: Bit 0 of timer status register mn (TSRmn)

Figure 8-55. Example of Set Contents of Registers to Measure Input Pulse Interval

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn	0: Outputs 0 from TOmn.
	0	

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn	0: Stops TOmn output operation by counting operation.
	0	

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn	0: Cleared to 0 when TOMmn = 0 (master channel output mode).
	0	

(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn	0: Sets master channel output mode.
	0	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-56. Operation Procedure When Input Pulse Interval Measurement Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode register mn (TMRmn) (determines operation mode of channel).	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets TSmn bit to 1. →	TEmn = 1, and count operation starts. Timer/counter register mn (TCRmn) is cleared to 0000H at the count clock input. When the MDmn0 bit of the TMRmn register is 1, INTTMmn is generated.
During operation	Set values of only the CISmn1 and CISmn0 bits of the TMRmn register can be changed. The TDRmn register can always be read. The TCRmn register can always be read. The TSRmn register can always be read. Set values of the TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	Counter (TCRmn) counts up from 0000H. When the TImn pin input valid edge is detected, the count value is transferred (captured) to timer data register mn (TDRmn). At the same time, the TCRmn register is cleared to 0000H, and the INTTMmn signal is generated. If an overflow occurs at this time, the OVF bit of timer status register mn (TSRmn) is set; if an overflow does not occur, the OVF bit is cleared. After that, the above operation is repeated.
Operation stop	The TTmn bit is set to 1. →	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops. The OVF bit of the TSRmn register is also held.
TAU stop	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0. Note →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.7.5 Operation as input signal high-/low-level width measurement

Caution When using a channel to implement the LIN-bus, set bit 1 (ISC1) of the input switch control register (ISC) to 1. In the following descriptions, read TImn as RxD0 if using the 78K0R/KC3-L, 78K0R/KD3-L, or 78K0R/KE3-L, and as RxD3 if using the 78K0R/KF3-L or 78K0R/KG3-L.

By starting counting at one edge of the TImn pin input and capturing the number of counts at another edge, the signal width (high-level width/low-level width) of TImn can be measured. The signal width of TImn can be calculated by the following expression.

Signal width of TImn input = Period of count clock × ((10000H × TSRmn: OVF) + (Capture value of TDRmn + 1))

Caution The TImn pin input is sampled using the operating clock selected with the CKSmn bit of timer mode register mn (TMRmn), so an error equivalent to one operation clock occurs.

Timer/counter register mn (TCRmn) operates as an up counter in the capture & one-count mode.

When the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, the TEmn bit is set to 1 and the TImn pin start edge detection wait status is set.

When the TImn pin input start edge (rising edge of the TImn pin input when the high-level width is to be measured) is detected, the counter counts up from 0000H in synchronization with the count clock. When the valid capture edge (falling edge of the TImn pin input when the high-level width is to be measured) is detected later, the count value is transferred to timer data register mn (TDRmn) and, at the same time, INTTMmn is output. If the counter overflows at this time, the OVF bit of timer status register mn (TSRmn) is set to 1. If the counter does not overflow, the OVF bit is cleared. The TCRmn register stops at the value “value transferred to the TDRmn register + 1”, and the TImn pin start edge detection wait status is set. After that, the above operation is repeated.

As soon as the count value has been captured to the TDRmn register, the OVF bit of the TSRmn register is updated depending on whether the counter overflows during the measurement period. Therefore, the overflow status of the captured value can be checked.

If the counter reaches a full count for two or more periods, it is judged to be an overflow occurrence, and the OVF bit of the TSRmn register is set to 1. However, a normal interval value cannot be measured for the OVF bit, if two or more overflows occur.

Whether the high-level width or low-level width of the TImn pin is to be measured can be selected by using the CISmn1 and CISmn0 bits of the TMRmn register.

Because this function is used to measure the signal width of the TImn pin input, the TSmn bit cannot be set to 1 while the TEmn bit is 1.

CISmn1, CISmn0 of TMRmn register = 10B: Low-level width is measured.

CISmn1, CISmn0 of TMRmn register = 11B: High-level width is measured.

Figure 8-57. Block Diagram of Operation as Input Signal High-/Low-Level Width Measurement

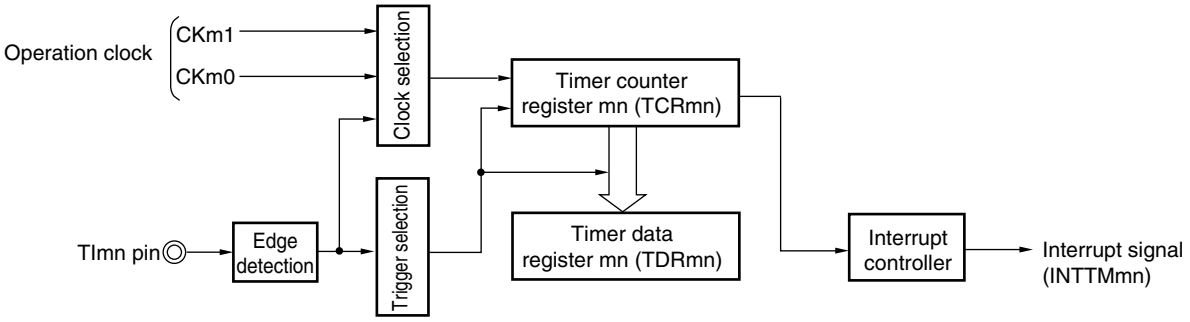
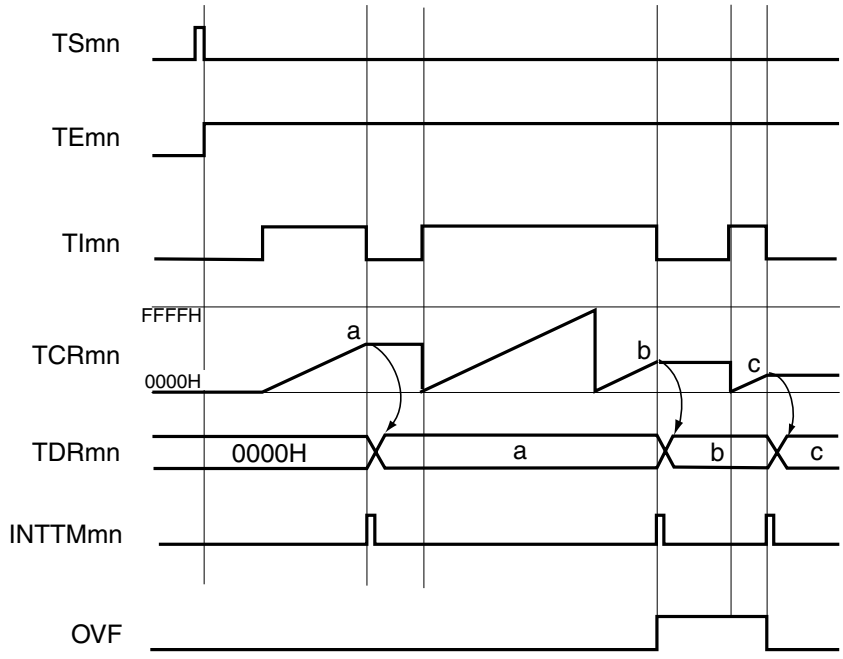


Figure 8-58. Example of Basic Timing of Operation as Input Signal High-/Low-Level Width Measurement

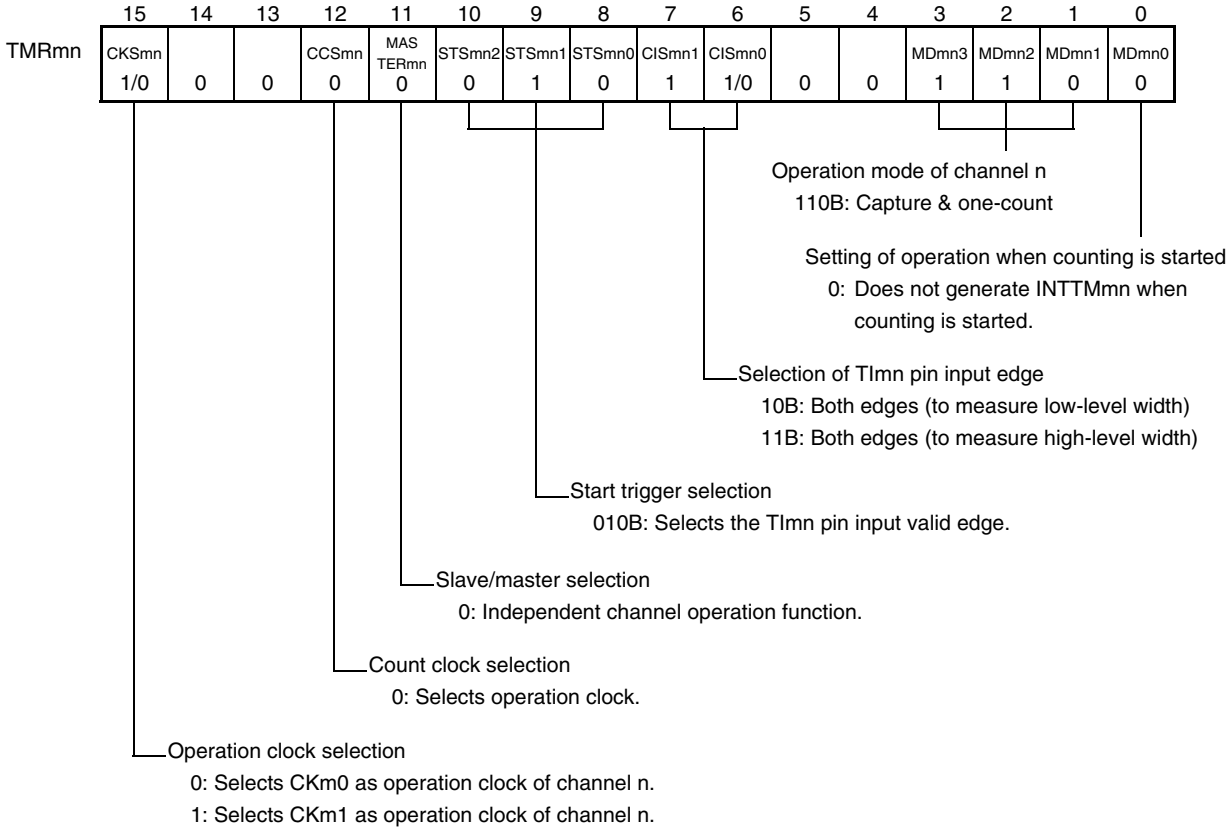


Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn) , mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

2. TSmn: Bit n of timer channel start register m (TSm)
TEmn: Bit n of timer channel enable status register m (TEm)
TImn: TImn pin input signal
TCRmn: Timer/counter register mn (TCRmn)
TDRmn: Timer data register mn (TDRmn)
OVF: Bit 0 of timer status register mn (TSRmn)

Figure 8-59. Example of Set Contents of Registers to Measure Input Signal High-/Low-Level Width

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn 0	0: Outputs 0 from TOmn.

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn 0	0: Stops the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn 0	0: Cleared to 0 when TOMmn = 0 (master channel output mode).

(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn 0	0: Sets master channel output mode.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn) and the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-60. Operation Procedure When Input Signal High-/Low-Level Width Measurement Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode register mn (TMRmn) (determines operation mode of channel). Clears the TOEmn bit to 0 and stops operation of TOmn.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. →	TEmn = 1, and the TImn pin start edge detection wait status is set.
	The TSmn bit automatically returns to 0 because it is a trigger bit.	
	Detects the TImn pin input count start valid edge. →	Clears timer/counter register mn (TCRmn) to 0000H and starts counting up.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	When the TImn pin start edge is detected, the counter (TCRmn) counts up from 0000H. If a capture edge of the TImn pin is detected, the count value is transferred to timer data register mn (TDRmn) and INTTMmn is generated. If an overflow occurs at this time, the OVF bit of timer status register mn (TSRmn) is set; if an overflow does not occur, the OVF bit is cleared. The TCRmn register stops the count operation until the next TImn pin start edge is detected.
Operation stop	The TTmn bit is set to 1. →	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops. The OVF bit of the TSRmn register is also held.
	The TTmn bit automatically returns to 0 because it is a trigger bit.	
TAU stop	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0. Note →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn) and the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.8 Simultaneous Channel Operation Function of Timer Array Unit

8.8.1 Operation as one-shot pulse output function

By using two channels as a set, a one-shot pulse having any delay pulse width can be generated from the signal input to the TImn pin.

The delay time and pulse width can be calculated by the following expressions.

Delay time = {Set value of TDRmn (master) + 2} × Count clock period
Pulse width = {Set value of TDRmp (slave)} × Count clock period

The master channel operates in the one-count mode and counts the delays. Timer/counter register mn (TCRmn) of the master channel starts operating upon start trigger detection and loads the value of timer data register mn (TDRmn).

The TCRmn register counts down from the value of the TDRmn register it has loaded, in synchronization with the count clock. When TCRmn = 0000H, it outputs INTTMmn and stops counting until the next start trigger is detected.

The slave channel operates in the one-count mode and counts the pulse width. The TCRmp register of the slave channel starts operation using INTTMmn of the master channel as a start trigger, and loads the value of the TDRmp register. The TCRmp register counts down from the value of The TDRmp register it has loaded, in synchronization with the count value. When count value = 0000H, it outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) is detected. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

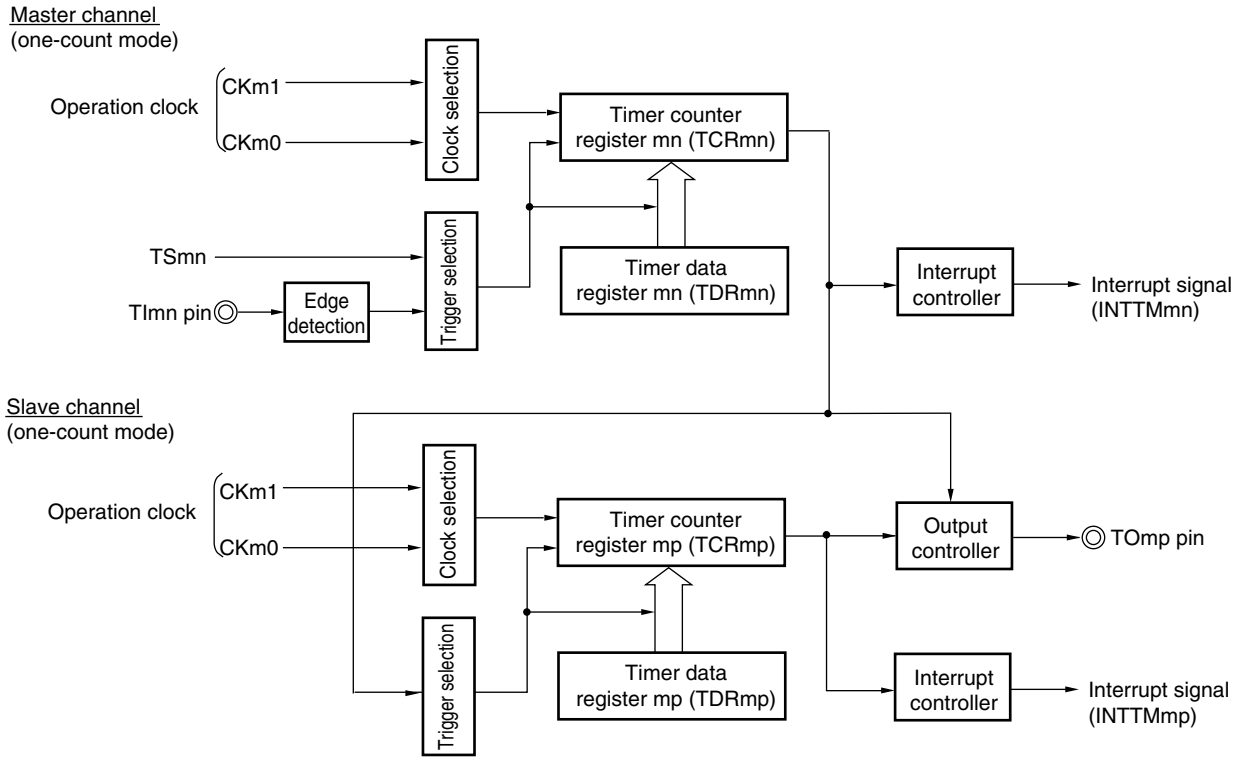
Instead of using the TImn pin input, a one-shot pulse can also be output using the software operation (TSmn = 1) as a start trigger.

Caution The timing of loading of timer data register mn (TDRmn) of the master channel is different from that of the TDRmp register of the slave channel. If the TDRmn and TDRmp registers are rewritten during operation, therefore, an illegal waveform is output. Rewrite the TDRmn register after INTTMmn is generated and the TDRmp register after INTTMmp is generated.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: $n < p \leq 7$
When m = 1: $n < p \leq 3$

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

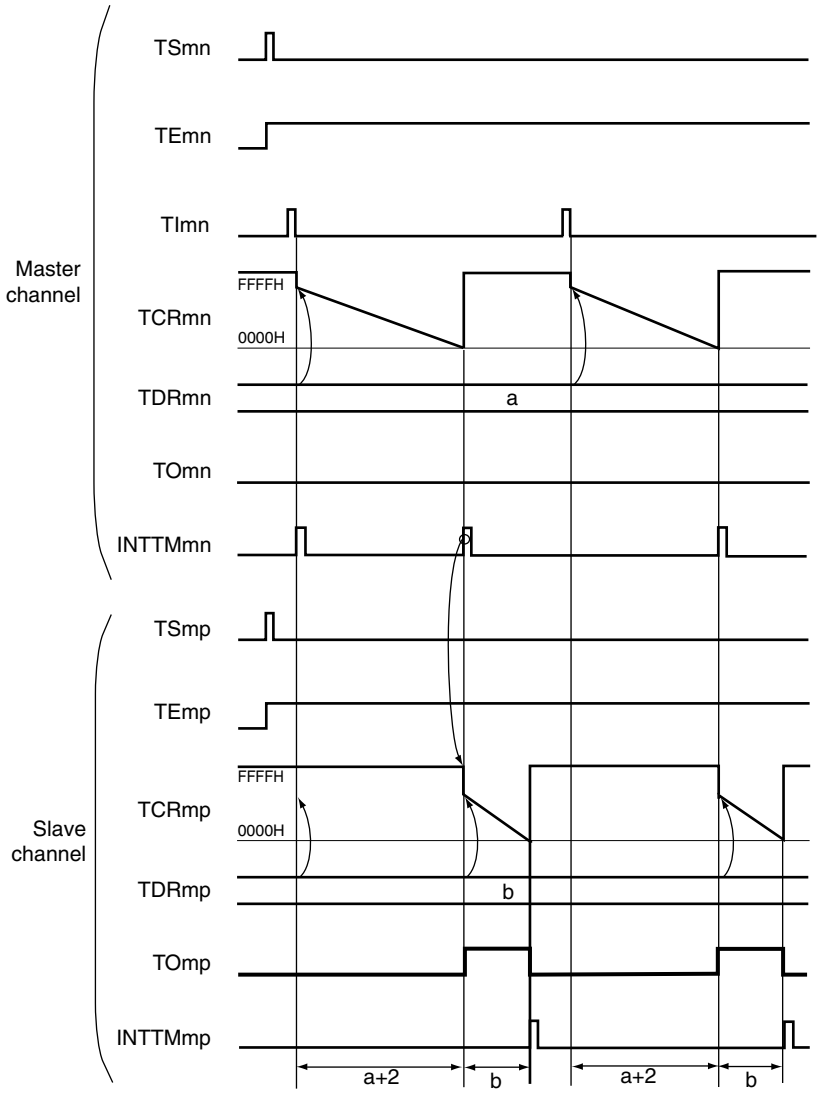
Figure 8-61. Block Diagram of Operation as One-Shot Pulse Output Function



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: n < p ≤ 7
When m = 1: n < p ≤ 3

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

Figure 8-62. Example of Basic Timing of Operation as One-Shot Pulse Output Function



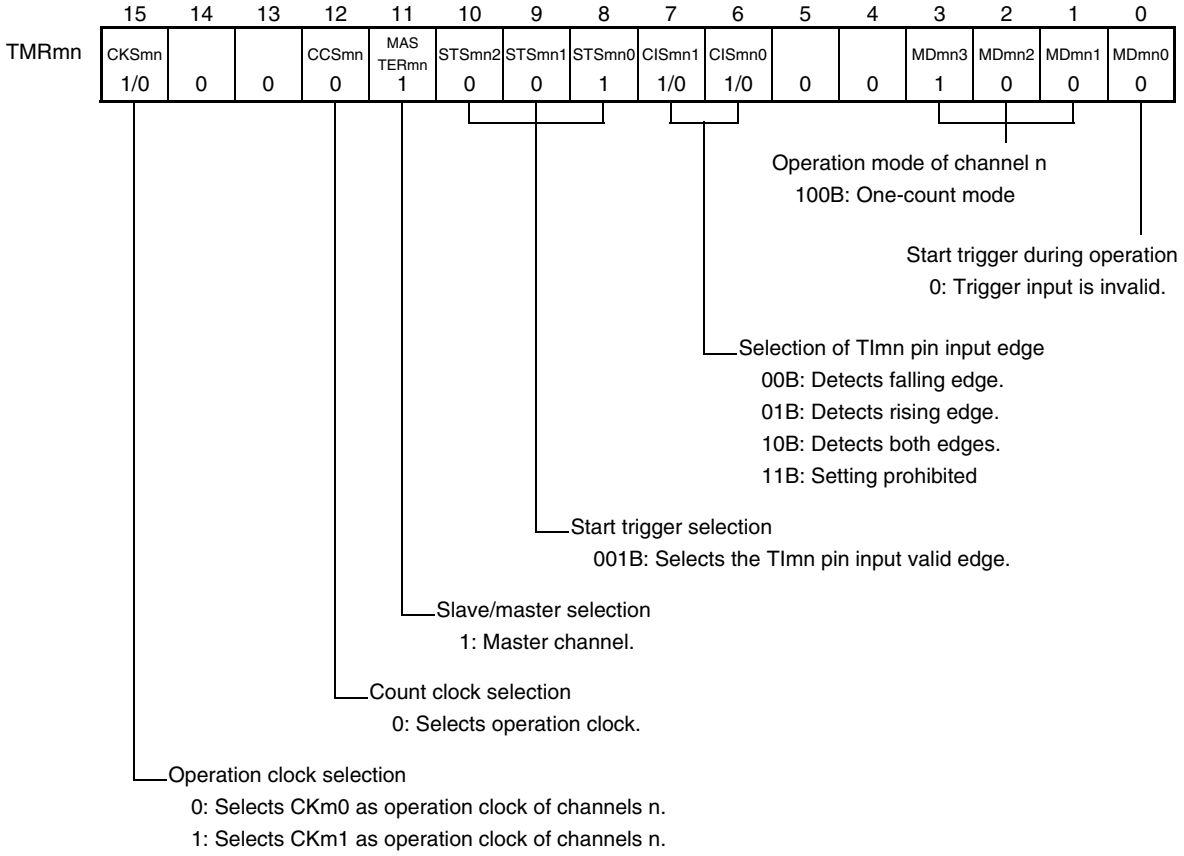
Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: n < p ≤ 7
When m = 1: n < p ≤3

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

2. TSmn, TSmp: Bit n, m of timer channel start register m (TSm)
TEmn, TEmp: Bit n, m of timer channel enable status register m (TEm)
TImn, TImp: TImn and TImp pins input signal
TCRmn, TCRmp: Timer/counter registers mn, mp (TCRmn, TCRmp)
TDRmn, TDRmp: Timer data registers mn, mp (TDRmn, TDRmp)
TOmn, TOmp: TOmn and TOmp pins output signal

Figure 8-63. Example of Set Contents of Registers When One-Shot Pulse Output Function Is Used (Master Channel)

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn 0	0: Outputs 0 from TOmn.

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn 0	0: Stops the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn 0	0: Cleared to 0 when TOMmn = 0 (master channel output mode).

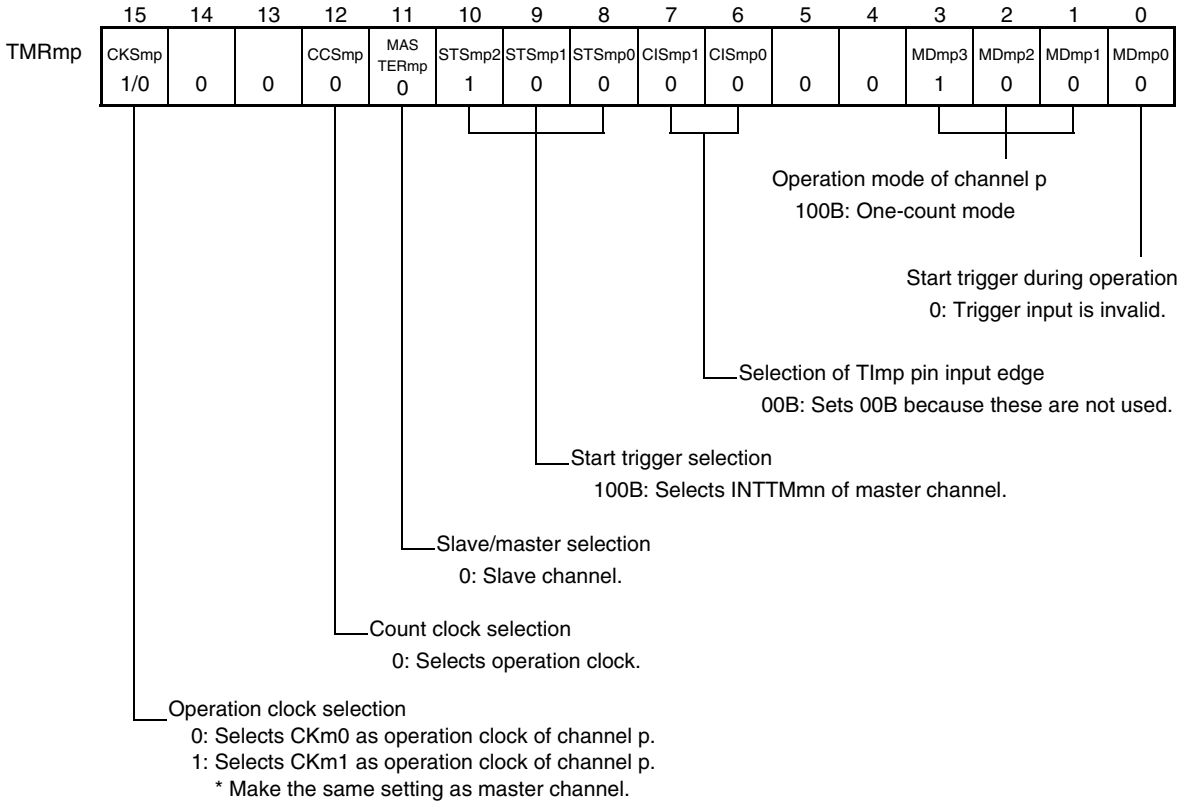
(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn 0	0: Sets master channel output mode.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12

Figure 8-64. Example of Set Contents of Registers When One-Shot Pulse Output Function Is Used (Slave Channel)

(a) Timer mode register mp (TMRmp)



(b) Timer output register m (TOm)

	Bit p	
TOm	TOmp 1/0	0: Outputs 0 from TOmp. 1: Outputs 1 from TOmp.

(c) Timer output enable register m (TOEm)

	Bit p	
TOEm	TOEmp 1/0	0: Stops the TOmp output operation by counting operation. 1: Enables the TOmp output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit p	
TOLm	TOLmp 1/0	0: Positive logic output (active-high) 1: Inverted output (active-low)

(e) Timer output mode register m (TOMm)

	Bit p	
TOMm	TOMmp 1	1: Sets the slave channel output mode.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: n < p ≤ 7
When m = 1: n < p ≤ 3

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

Figure 8-65. Operation Procedure of One-Shot Pulse Output Function (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode register mn, mp (TMRmn, TMRmp) of two channels to be used (determines operation mode of channels). An output delay is set to timer data register mn (TDRmn) of the master channel, and a pulse width is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of timer output mode register m (TOMm) is set to 1 (slave channel output mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output. →	The TOmp pin goes into Hi-Z output state. The TOmp default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets the TOEmp bit to 1 and enables operation of TOmp. →	TOmp does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmp pin outputs the TOmp set level.

(**Note** and **Remark** are listed on the next page.)

Figure 8-65. Operation Procedure of One-Shot Pulse Output Function (2/2)

	Software Operation	Hardware Status
Operation start	Sets the TOEmp bit (slave) to 1 (only when operation is resumed). The TSmn (master) and TSmp (slave) bits of timer channel start register m (TSm) are set to 1 at the same time. →	The TEmn and TEmp bits are set to 1 and the master channel enters the TImn input edge detection wait status. Counter stops operating.
	The TSmn and TSmp bits automatically return to 0 because they are trigger bits.	
	Detects the TImn pin input valid edge of master channel. →	Master channel starts counting.
During operation	Set values of only the CISmn1 and CISmn0 bits of the TMRmn register can be changed. Set values of the TMRmp, TDRmn, TDRmp registers, TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed. The TCRmn and TCRmp registers can always be read. The TSRmn and TSRmp registers are not used. Set values of the TOm and TOEm registers can be changed.	Master channel loads the value of the TDRmn register to timer/counter register mn (TCRmn) when the TImn pin valid input edge is detected, and the counter starts counting down. When the count value reaches TCRmn = 0000H, the INTTMmn output is generated, and the counter stops until the next valid edge is input to the TImn pin. The slave channel, triggered by INTTMmn of the master channel, loads the value of the TDRmp register to the TCRmp register, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn (master) and TTmp (slave) bits are set to 1 at the same time. →	TEmn, TEmp = 0, and count operation stops. The TCRmn and TCRmp registers hold count value and stop. The TOmp output is not initialized but holds current status.
	The TOEmp bit of slave channel is cleared to 0 and value is set to the TOmp bit. →	The TOmp pin outputs the TOmp set level.
TAU stop	To hold the TOmp pin output level Clears the TOmp bit to 0 after the value to be held is set to the port register. →	The TOmp pin output level is held by port function.
	When holding the TOmp pin output level is not necessary Switches the port mode register to input mode. →	The TOmp pin output level goes into Hi-Z output state.
	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0.[Note] →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)

Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: n < p ≤ 7
When m = 1: n < p ≤ 3

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

8.8.2 Operation as PWM function

Two channels can be used as a set to generate a pulse of any period and duty factor.

The period and duty factor of the output pulse can be calculated by the following expressions.

Pulse period = {Set value of TDRmn (master) + 1} × Count clock period
Duty factor [%] = {Set value of TDRmp (slave)}/{Set value of TDRmn (master) + 1} × 100
0% output: Set value of TDRmp (slave) = 0000H
100% output: Set value of TDRmp (slave) ≥ {Set value of TDRmn (master) + 1}

Remark The duty factor exceeds 100% if the set value of TDRmp (slave) > (set value of TDRmn (master) + 1), it summarizes to 100% output.

The master channel operates in the interval timer mode. If the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, an interrupt (INTTMmn) is output, the value set to timer data register mn (TDRmn) is loaded to timer/counter register mn (TCRmn), and the counter counts down in synchronization with the count clock. When the counter reaches 0000H, INTTMmn is output, the value of the TDRmn register is loaded again to the TCRmn register, and the counter counts down. This operation is repeated until the channel stop trigger bit (TTmn) of timer channel stop register m (TTm) is set to 1.

If two channels are used to output a PWM waveform, the period until the master channel counts down to 0000H is the PWM output (TOmp) cycle.

The slave channel operates in one-count mode. By using INTTMmn from the master channel as a start trigger, the TCRmp register loads the value of the TDRmp register and the counter counts down to 0000H. When the counter reaches 0000H, it outputs INTTMmp and waits until the next start trigger (INTTMmn from the master channel) is generated.

If two channels are used to output a PWM waveform, the period until the slave channel counts down to 0000H is the PWM output (TOmp) duty.

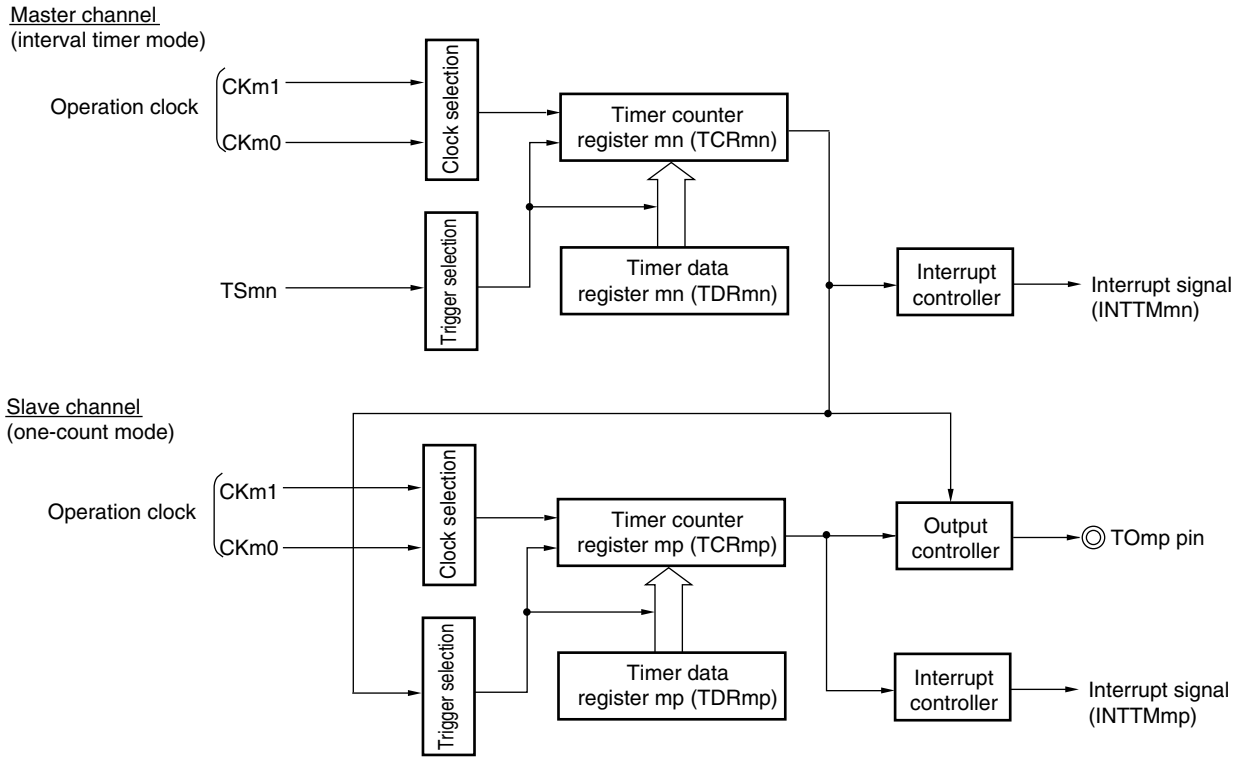
PWM output (TOmp) goes to the active level one clock after the master channel generates INTTMmn and goes to the inactive level when the TCRmp register of the slave channel becomes 0000H.

Caution To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel, a write access is necessary two times. The timing at which the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers is upon occurrence of INTTMmn of the master channel. Thus, when rewriting is performed split before and after occurrence of INTTMmn of the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, therefore, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: n < p ≤ 7
When m = 1: n < p ≤ 3

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

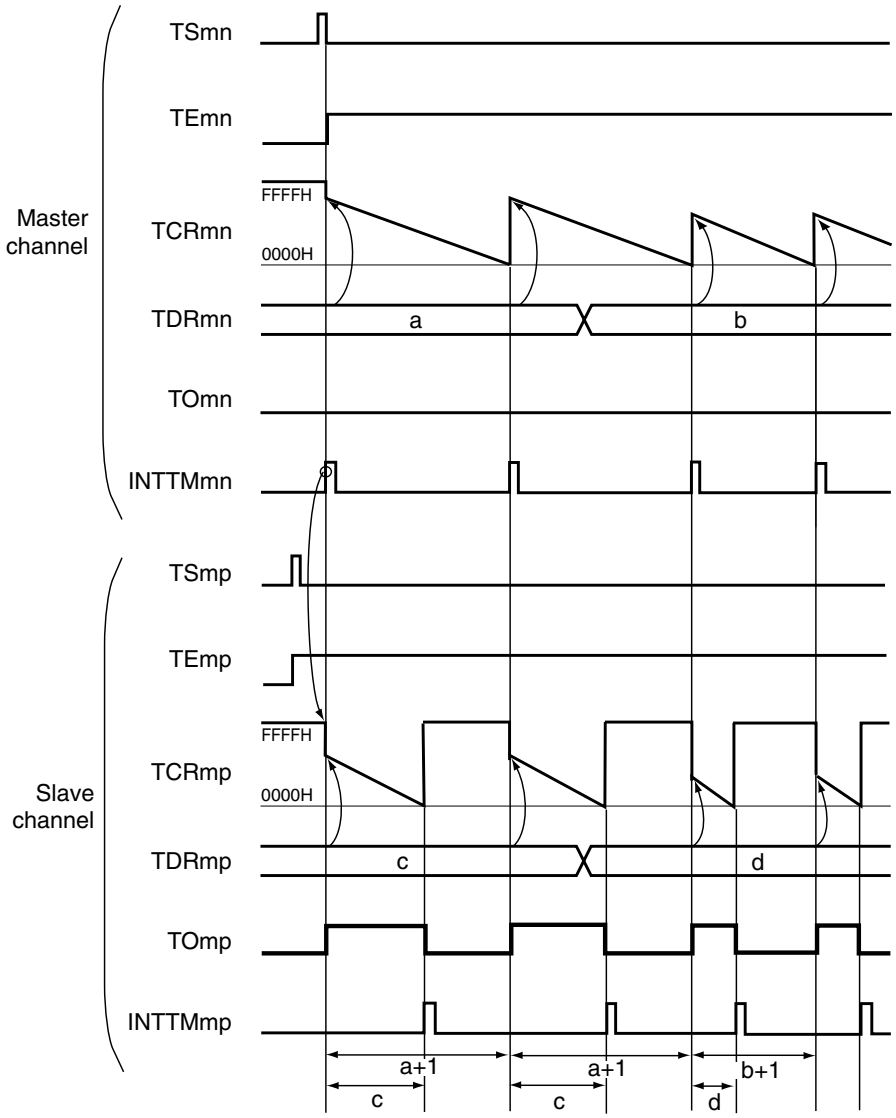
Figure 8-66. Block Diagram of Operation as PWM Function



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: $n < p \leq 7$
When m = 1: $n < p \leq 3$

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

Figure 8-67. Example of Basic Timing of Operation as PWM Function



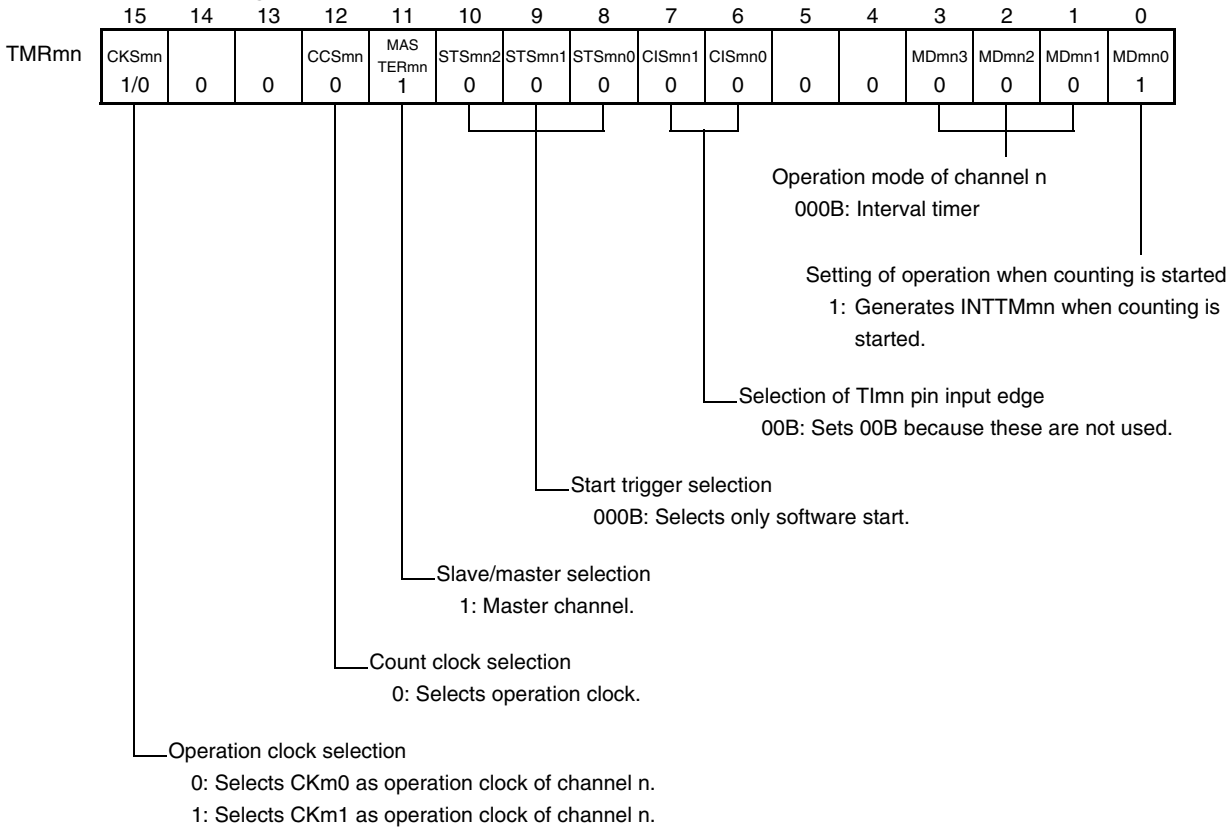
Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: n < p ≤ 7
When m = 1: n < p ≤ 3

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

2. TSmn, TSmp: Bit n, m of timer channel start register m (TSm)
TEmn, TEmp: Bit n, m of timer channel enable status register m (TEm)
TCRmn, TCRmp: Timer/counter registers mn, mp (TCRmn, TCRmp)
TDRmn, TDRmp: Timer data registers mn, mp (TDRmn, TDRmp)
TOmn, TOmp: TOmn and TOmp pins output signal

Figure 8-68. Example of Set Contents of Registers When PWM Function (Master Channel) Is Used

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn 0	0: Outputs 0 from TOmn.

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn 0	0: Stops the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn 0	0: Cleared to 0 when TOMmn = 0 (master channel output mode).

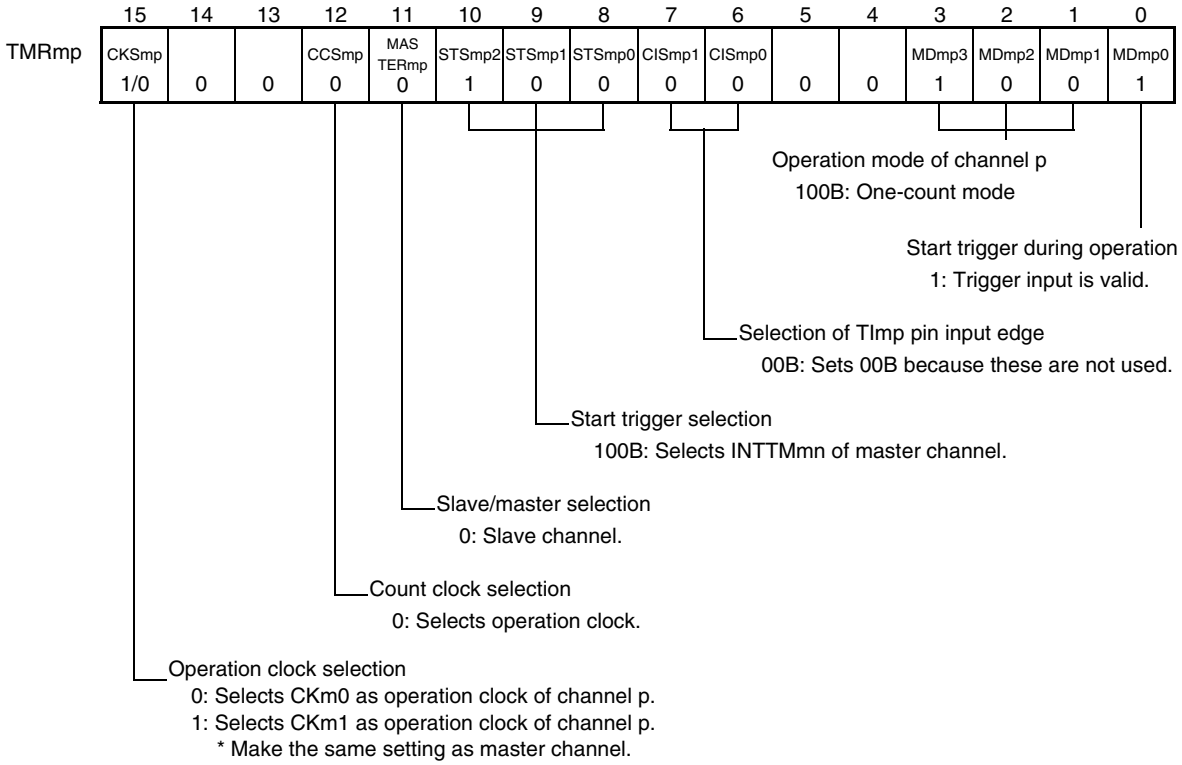
(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn 0	0: Sets master channel output mode.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12

Figure 8-69. Example of Set Contents of Registers When PWM Function (Slave Channel) Is Used

(a) Timer mode register mp (TMRmp)



(b) Timer output register m (TOm)

	Bit p	
TOm	TOmp 1/0	0: Outputs 0 from TOmp. 1: Outputs 1 from TOmp.

(c) Timer output enable register m (TOEm)

	Bit p	
TOEm	TOEmp 1/0	0: Stops the TOmp output operation by counting operation. 1: Enables the TOmp output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit p	
TOLm	TOLmp 1/0	0: Positive logic output (active-high) 1: Inverted output (active-low)

(e) Timer output mode register m (TOMm)

	Bit p	
TOMm	TOMmp 1	1: Sets the slave channel output mode.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: n < p ≤ 7
When m = 1: n < p ≤ 3

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

Figure 8-70. Operation Procedure When PWM Function Is Used (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode registers mn, mp (TMRmn, TMRmp) of two channels to be used (determines operation mode of channels). An interval (period) value is set to timer data register mn (TDRmn) of the master channel, and a duty factor is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of timer output mode register m (TOMm) is set to 1 (slave channel output mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output. →	The TOmp pin goes into Hi-Z output state. The TOmp default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets the TOEmp bit to 1 and enables operation of TOmp. →	TOmp does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmp pin outputs the TOmp set level.

(**Note** and **Remark** are listed on the next page.)

Figure 8-70. Operation Procedure When PWM Function Is Used (2/2)

	Software Operation	Hardware Status
Operation start	Sets the TOEmp bit (slave) to 1 (only when operation is resumed). The TSmn (master) and TSmp (slave) bits of timer channel start register m (TSm) are set to 1 at the same time. →	TEmn = 1, TEmp = 1 → When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.
	The TSmn and TSmp bits automatically return to 0 because they are trigger bits.	
During operation	Set values of the TMRmn and TMRmp registers, TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed. Set values of the TDRmn and TDRmp registers can be changed after INTTMmn of the master channel is generated. The TCRmn and TCRmp registers can always be read. The TSRmn and TSRmp registers are not used. Set values of the TOm and TOEm registers can be changed.	The counter of the master channel loads the TDRmn register value to timer/counter register mn (TCRmn), and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again. At the slave channel, the value of the TDRmp register is loaded to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn (master) and TTmp (slave) bits are set to 1 at the same time. →	TEmn, TEmp = 0, and count operation stops. The TCRmn and TCRmp registers hold count value and stop. The TOmp output is not initialized but holds current status.
	The TOEmp bit of slave channel is cleared to 0 and value is set to the TOmp bit. →	The TOmp pin outputs the TOmp set level.
TAU stop	To hold the TOmp pin output level Clears the TOmp bit to 0 after the value to be held is set to the port register. →	The TOmp pin output level is held by port function.
	When holding the TOmp pin output level is not necessary Switches the port mode register to input mode. →	The TOmp pin output level goes into Hi-Z output state.
	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0.[Note] →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)

Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: $n < p \leq 7$
When m = 1: $n < p \leq 3$

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

8.8.3 Operation as multiple PWM output function

By extending the PWM function and using multiple slave channels, many PWM waveforms with different duty values can be output.

For example, when using two slave channels, the period and duty factor of an output pulse can be calculated by the following expressions.

Pulse period = {Set value of TDRmn (master) + 1} × Count clock period
Duty factor 1 [%] = {Set value of TDRmp (slave 1)}/{Set value of TDRmn (master) + 1} × 100
Duty factor 2 [%] = {Set value of TDRmq (slave 2)}/{Set value of TDRmn (master) + 1} × 100

Remark Although the duty factor exceeds 100% if the set value of TDRmp (slave 1) > {set value of TDRmn (master) + 1} or if the {set value of TDRmq (slave 2)} > {set value of TDRmn (master) + 1}, it is summarized into 100% output.

Timer/counter register mn (TCRmn) of the master channel operates in the interval timer mode and counts the periods.

The TCRmp register of the slave channel 1 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmp pin. The TCRmp register loads the value of timer data register mp (TDRmp), using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmp = 0000H, TCRmp outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

In the same way as the TCRmp register of the slave channel 1, the TCRmq register of the slave channel 2 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmq pin. The TCRmq register loads the value of the TDRmq register, using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmq = 0000H, the TCRmq register outputs INTTMmq and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmq becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmq = 0000H.

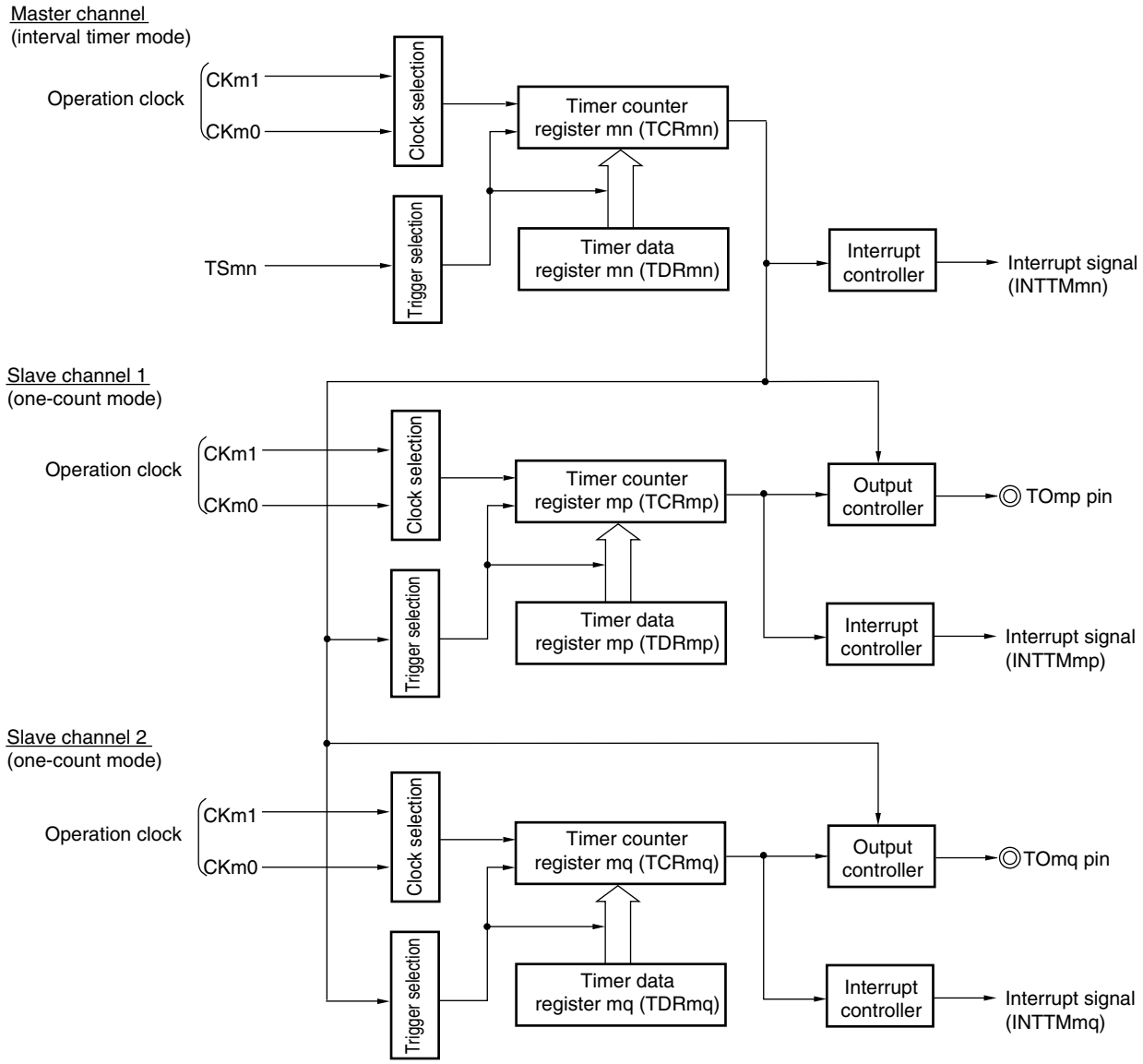
When channel 0 is used as the master channel as above, up to seven types of PWM signals can be output at the same time.

Caution To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel 1, write access is necessary at least twice. Since the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers after INTTMmn is generated from the master channel, if rewriting is performed separately before and after generation of INTTMmn from the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel (This applies also to the TDRmq register of the slave channel 2).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 10
p: Slave channel number 1, q: Slave channel number 2[Note]
When m = 0: n < p < q ≤ 7
When m = 1: n < p < q ≤ 3
(Where p and q are consecutive integers greater than n)

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

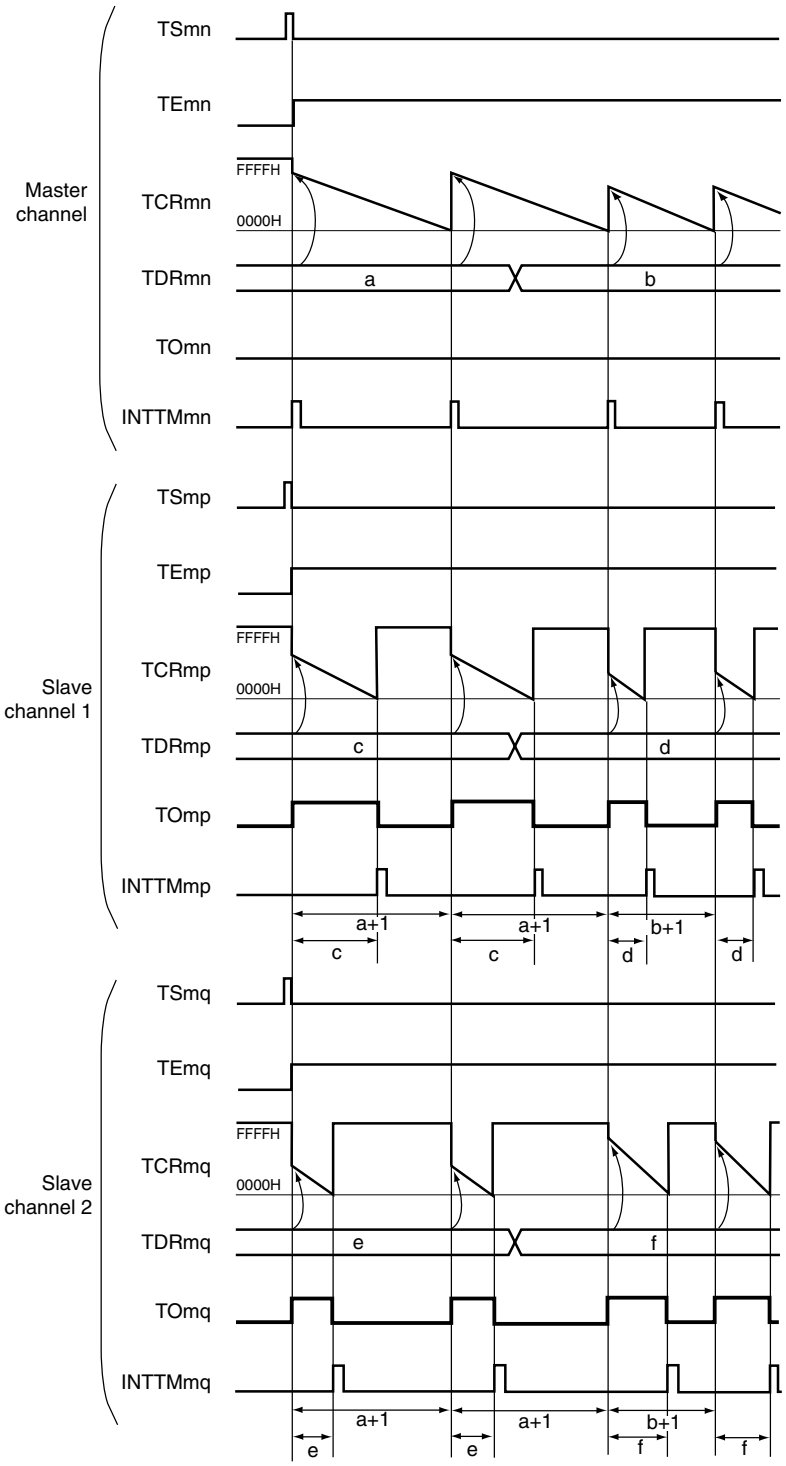
Figure 8-71. Block Diagram of Operation as Multiple PWM Output Function (output two types of PWMs)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 10
p: Slave channel number 1, q: Slave channel number 2[Note]
When m = 0: $n < p < q \leq 7$
When m = 1: $n < p < q \leq 3$
(Where p and q are consecutive integers greater than n)

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

Figure 8-72. Example of Basic Timing of Operation as Multiple PWM Output Function (output two types of PWMs) (1/2)



(**Remark** are listed on the next page.)

Figure 8-72. Example of Basic Timing of Operation as Multiple PWM Output Function (output two types of PWMs) (2/2)

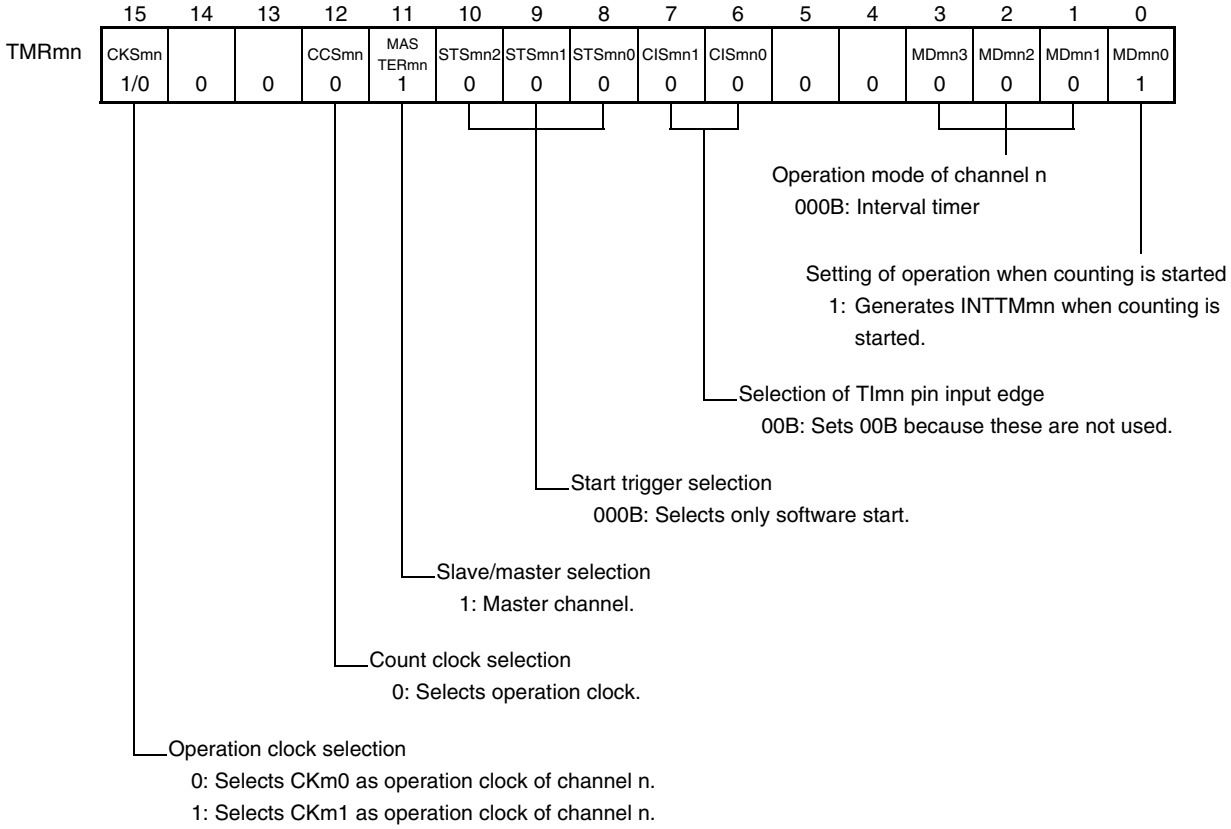
Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 10
p: Slave channel number 1, q: Slave channel number 2[Note]
When m = 0: $n < p < q \leq 7$
When m = 1: $n < p < q \leq 3$
(Where p and q are consecutive integers greater than n)

Note Since there is no function of timer I/O, channel 1 in the 78K0R/KC3-L (40-pin) can not used as slave channel.

2. TSmn, TSmp, TSmq: Bit n, p, q of timer channel start register m (TSm)
TEmn, TEmp, TEmq: Bit n, p, q of timer channel enable status register m (TEm)
TCRmn, TCRmp, TCRmq: Timer/counter registers mn, mp, mq (TCRmn, TCRmp, TCRmq)
TDRmn, TDRmp, TDRmq: Timer data registers mn, mp, mq (TDRmn, TDRmp, TDRmq)
TOmn, TOmp, TOmq: TOmn, TOmp, and TOmq pins output signal

Figure 8-73. Example of Set Contents of Registers When Multiple PWM Output Function (Master Channel) Is Used

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn	0: Outputs 0 from TOmn.
	0	

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn	0: Stops the TOmn output operation by counting operation.
	0	

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn	0: Cleared to 0 when TOMmn = 0 (master channel output mode).
	0	

(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn	0: Sets master channel output mode.
	0	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 10

Figure 8-74. Example of Set Contents of Registers When Multiple PWM Output Function (Slave Channel) Is Used (output two types of PWMs) (1/2)

(a) Timer mode register mp, mq (TMRmp, TMRmq)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmp	CKSmp			CCSmp	MAS TERmp	STSmp2	STSmp1	STSmp0	CISmp1	CISmp0			MDmp3	MDmp2	MDmp1	MDmp0
	1/0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
TMRmq	CKSmq			CCSmq	MAS TERmq	STSmq2	STSmq1	STSmq0	CISmq1	CISmq0			MDmq3	MDmq2	MDmq1	MDmq0
	1/0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1

Operation mode of channel p, q
100B: One-count mode

Start trigger during operation
1: Trigger input is valid.

Selection of TImp and TImq pins input edge
00B: Sets 00B because these are not used.

Start trigger selection
100B: Selects INTTMmn of master channel.

Slave/master selection
0: Slave channel.

Count clock selection
0: Selects operation clock.

Operation clock selection
0: Selects CKm0 as operation clock of channel p, q.
1: Selects CKm1 as operation clock of channel p, q.
* Make the same setting as master channel.

(b) Timer output register m (TOm)

	Bit q	Bit p
TOm	TOmq	TOmp
	1/0	1/0

0: Outputs 0 from TOmp or TOmq.
1: Outputs 1 from TOmp or TOmq.

(c) Timer output enable register m (TOEm)

	Bit q	Bit p
TOEm	TOEmq	TOEmp
	1/0	1/0

0: Stops the TOmp or TOmq output operation by counting operation.
1: Enables the TOmp or TOmq output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit q	Bit p
TOLm	TOLmq	TOLmp
	1/0	1/0

0: Positive logic output (active-high)
1: Inverted output (active-low)

(e) Timer output mode register m (TOMm)

	Bit q	Bit p
TOMm	TOMmq	TOMmp
	1	1

1: Sets the slave channel output mode.

(**Remark** is listed on the next page.)

Figure 8-74. Example of Set Contents of Registers When Multiple PWM Output Function (Slave Channel) Is Used (output two types of PWMs) (2/2)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 10
p: Slave channel number 1, q: Slave channel number 2[Note]
When m = 0: $n < p < q \leq 7$, When m = 1: $n < p < q \leq 3$
(Where p and q are consecutive integers greater than n)

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

Figure 8-75. Operation Procedure When Multiple PWM Output Function Is Used (1/3)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode registers mn, mp, mq (TMRmn, TMRmp, TMRmq) of each channel to be used (determines operation mode of channels). An interval (period) value is set to timer data register mn (TDRmn) of the master channel, and a duty factor is set to the TDRmp and TDRmq registers of the slave channels.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channels. The TOMmp and TOMmq bits of timer output mode register m (TOMm) are set to 1 (slave channel output mode). Clears the TOLmp and TOLmq bits to 0. Sets the TOmp and TOmq bits and determines default level of the TOmp and TOmq outputs. →	The TOmp and TOmq pins go into Hi-Z output state. The TOmp and TOmq default setting levels are output when the port mode register is in output mode and the port register is 0.
	Sets the TOEmp and TOEmq bits to 1 and enables operation of TOmp and TOmq. →	TOmp and TOmq do not change because channels stop operating.
	Clears the port register and port mode register to 0. →	The TOmp and TOmq pins output the TOmp and TOmq set levels.

(**Note** and **Remark** are listed on the next page.)

Figure 8-75. Operation Procedure When Multiple PWM Output Function Is Used (2/3)

	Software Operation	Hardware Status
Operation start	(Sets the TOEmp and TOEmq (slave) bits to 1 only when resuming operation.) The TSmn bit (master), and TSmp and TSmq (slave) bits of timer channel start register m (TSm) are set to 1 at the same time. The TSmn, TSmp, and TSmq bits automatically return to 0 because they are trigger bits.	→ TEmn = 1, TEmp, TEmq = 1 When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.
During operation	Set values of the TMRmn, TMRmp, TMRmq registers, TOMmn, TOMmp, TOMmq, TOLmn, TOLmp, and TOLmq bits cannot be changed. Set values of the TDRmn, TDRmp, and TDRmq registers can be changed after INTTMmn of the master channel is generated. The TCRmn, TCRmp, and TCRmq registers can always be read. The TSRmn, TSRmp, and TSRmq registers are not used. Set values of the TOm and TOEm registers can be changed.	The counter of the master channel loads the TDRmn register value to timer/counter register mn (TCRmn) and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again. At the slave channel 1, the values of the TDRmp register are transferred to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output levels of TOmp become active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. At the slave channel 2, the values of the TDRmq register are transferred to TCRmq regster, triggered by INTTMmn of the master channel, and the counter starts counting down. The output levels of TOmq become active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmq = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn bit (master), TTmp, and TTmq (slave) bits are set to 1 at the same time. The TTmn, TTmp, and TTmq bits automatically return to 0 because they are trigger bits.	→ TEmn, TEmp, TEmq = 0, and count operation stops. The TCRmn, TCRmp, and TCRmq registers hold count value and stop. The TOmp and TOmq output are not initialized but hold current status.
	The TOEmp and TOEmq bits of slave channels are cleared to 0 and value is set to the TOmp and TOmq bits.	→ The TOmp and TOmq pins output the TOmp and TOmq set levels.
TAU stop	To hold the TOmp and TOmq pin output levels Clears the TOmp and TOmq bits to 0 after the value to be held is set to the port register.	→ The TOmp and TOmq pin output levels are held by port function.
	When holding the TOmp and TOmq pin output levels are not necessary Switches the port mode register to input mode.	→ The TOmp and TOmq pin output levels go into Hi-Z output state.
	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0.[Note]	→ Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp and TOmq bits are cleared to 0 and the TOmp and TOmq pins are set to port mode.)

Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

(**Remark** is listed on the next page.)

Figure 8-75. Operation Procedure When Multiple PWM Output Function Is Used (3/3)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 10
p: Slave channel number 1, q: Slave channel number 2[Note]
When m = 0: $n < p < q \leq 7$, When m = 1: $n < p < q \leq 3$
(Where p and q are a consecutive integer greater than n)

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

CHAPTER 9 REAL-TIME COUNTER

Remark The 78K0R/KC3-L (40-pin) doesn't have the real-time counter.

9.1 Functions of Real-Time Counter

The real-time counter has the following features.

- Having counters of year, month, week, day, hour, minute, and second, and can count up to 99 years.
- Constant-period interrupt function (period: 1 month to 0.5 seconds)
- Alarm interrupt function (alarm: week, hour, minute)
- Interval interrupt function
- Pin output function of 1 Hz
- Pin output function of 512 Hz or 16.384 kHz or 32.768 kHz

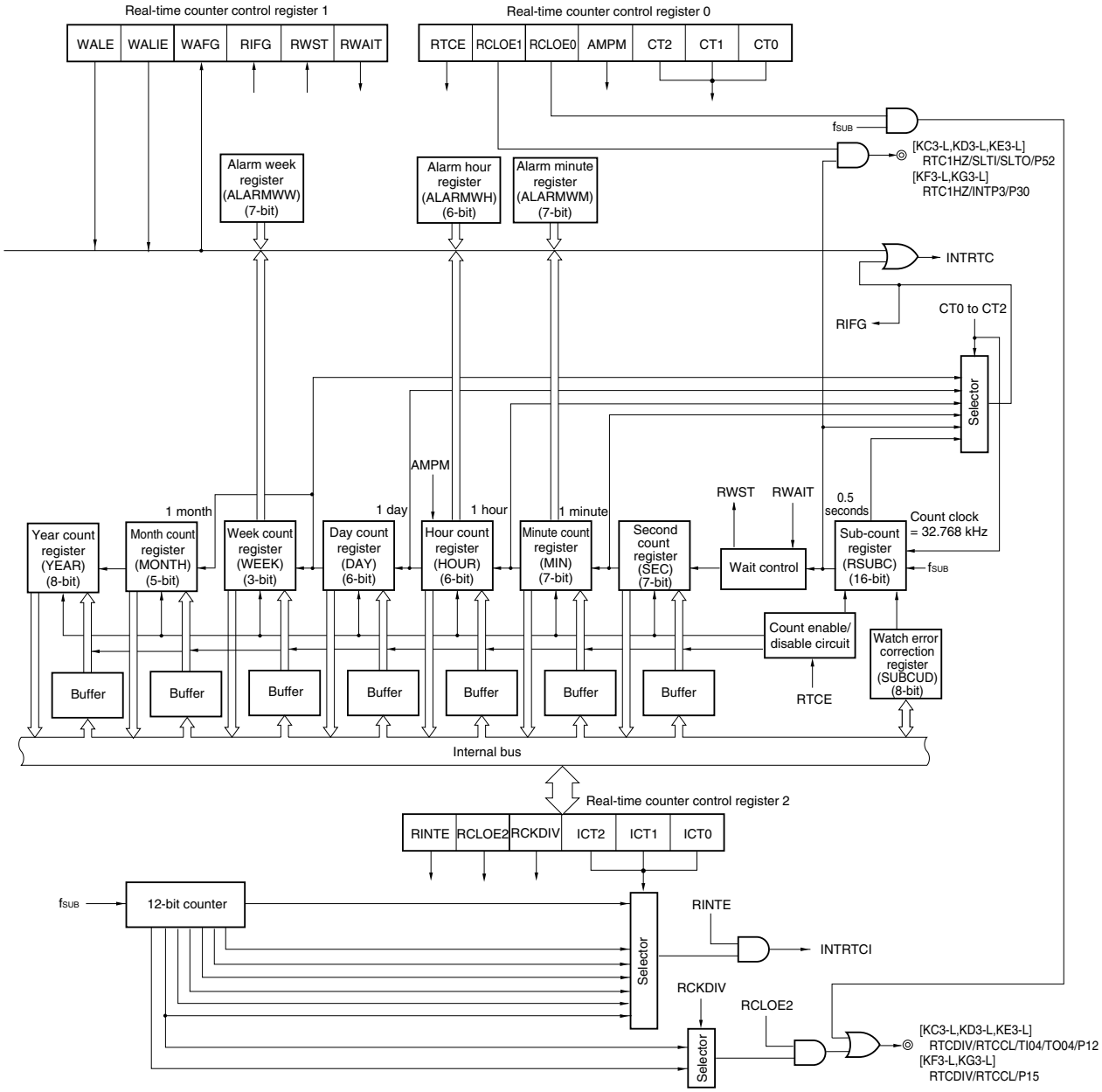
9.2 Configuration of Real-Time Counter

The real-time counter includes the following hardware.

Table 9-1. Configuration of Real-Time Counter

Item	Configuration
Control registers	Peripheral enable register 0 (PER0)
	Real-time counter control register 0 (RTCC0)
	Real-time counter control register 1 (RTCC1)
	Real-time counter control register 2 (RTCC2)
	Sub-count register (RSUBC)
	Second count register (SEC)
	Minute count register (MIN)
	Hour count register (HOUR)
	Day count register (DAY)
	Week count register (WEEK)
	Month count register (MONTH)
	Year count register (YEAR)
	Watch error correction register (SUBCUD)
	Alarm minute register (ALARMWM)
	Alarm hour register (ALARMWH)
	Alarm week register (ALARMWW)

Figure 9-1. Block Diagram of Real-Time Counter



9.3 Registers Controlling Real-Time Counter

The real-time counter is controlled by the following 16 registers.

- Peripheral enable register 0 (PER0)
- Real-time counter control register 0 (RTCC0)
- Real-time counter control register 1 (RTCC1)
- Real-time counter control register 2 (RTCC2)
- Sub-count register (RSUBC)
- Second count register (SEC)
- Minute count register (MIN)
- Hour count register (HOUR)
- Day count register (DAY)
- Week count register (WEEK)
- Month count register (MONTH)
- Year count register (YEAR)
- Watch error correction register (SUBCUD)
- Alarm minute register (ALARMWM)
- Alarm hour register (ALARMWH)
- Alarm week register (ALARMWW)

(1) Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the real-time counter is used, be sure to set bit 7 (RTCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-2. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN Note 1	0	ADCEN	IICAEN Note 2	SAU1EN Note 3	SAU0EN	TAU1EN Note 3	TAU0EN Note 3

RTCEN Note 1	Control of real-time counter (RTC) input clock supply Note 4
0	Stops input clock supply. • SFR used by the real-time counter (RTC) cannot be written. • The real-time counter (RTC) is in the reset status.
1	Enables input clock supply. • SFR used by the real-time counter (RTC) can be read/written.

Notes 1. That is not provided in 40-pin product of the 78K0R/KC3-L.

2. That is not provided in 40-pin and 44-pin products of the 78K0R/KC3-L.

3. 78K0R/KF3-L and 78K0R/KG3-L only.

4. The RTCEN bit is used to supply or stop the clock used when accessing the real-time counter (RTC) register from the CPU. The RTCEN bit cannot control supply of the operating clock (f_{SUB}) to RTC.

Cautions 1. When using the real-time counter, first set the RTCEN bit to 1, while oscillation of the subsystem clock (f_{SUB}) is stable. If RTCEN = 0, writing to a control register of the real-time counter is ignored, and, even if the register is read, only the default value is read.

2. Clock supply to peripheral functions other than the real-time counter can be stopped in HALT mode when the subsystem clock is used, by setting the RTCLPC bit of the operation speed mode control register (OSMC) to 1. In this case, set the RTCEN bit of the PER0 register to 1 and the other bits (bits 0 to 6) to 0. If using the 78K0R/KC3-L, 78K0R/KD3-L, or 78K0R/KE3-L, set bits 0 to 7 of the PER1 and PER2 registers to 0 also.

3. Be sure to clear the following bits to 0.
48-pin product of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: bits 0, 1, 3, 6
44-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6
40-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6, 7
78K0R/KF3-L, 78K0R/KG3-L: bit 6

(2) Real-time counter control register 0 (RTCC0)

The RTCC0 register is an 8-bit register that is used to start or stop the real-time counter operation, control the RTCCL and RTC1HZ pins, and set a 12- or 24-hour system and the constant-period interrupt function.

The RTCC0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-3. Format of Real-Time Counter Control Register 0 (RTCC0)

Address: FFF9DH After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	3	2	1	0
RTCC0	RTCE	0	RCLOE1	RCLOE0	AMPM	CT2	CT1	CT0

RTCE	Real-time counter operation control
0	Stops counter operation.
1	Starts counter operation.

RCLOE1	RTC1HZ pin output control
0	Disables output of the RTC1HZ pin (1 Hz).
1	Enables output of the RTC1HZ pin (1 Hz).

RCLOE0[Note]	RTCCL pin output control
0	Disables output of the RTCCL pin (32.768 kHz).
1	Enables output of the RTCCL pin (32.768 kHz).

AMPM	Selection of 12-/24-hour system
0	12-hour system (a.m. and p.m. are displayed.)
1	24-hour system
• Rewrite the AMPM bit value after setting the RWAIT bit (bit 0 of real-time counter control register 1 (RTCC1)) to 1. If the AMPM bit value is changed, the values of the hour count register (HOUR) change according to the specified time system. • Table 9-2 shows the displayed time digits that are displayed.	

CT2	CT1	CT0	Constant-period interrupt (INTRTC) selection
0	0	0	Does not use constant-period interrupt function.
0	0	1	Once per 0.5 s (synchronized with second count up)
0	1	0	Once per 1 s (same time as second count up)
0	1	1	Once per 1 m (second 00 of every minute)
1	0	0	Once per 1 hour (minute 00 and second 00 of every hour)
1	0	1	Once per 1 day (hour 00, minute 00, and second 00 of every day)
1	1	×	Once per 1 month (Day 1, hour 00 a.m., minute 00, and second 00 of every month)
When changing the values of the CT2 to CT0 bits while the counter operates (RTCE = 1), rewrite the values of the CT2 to CT0 bits after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, after rewriting the values of the CT2 to CT0 bits, enable interrupt servicing after clearing the RIFG and RTCIF flags.			

Note The RCLOE0 and RCLOE2 bits must not be enabled at the same time.

Caution If the RCLOE0 and RCLOE1 bits are changed when RTCE = 1, the last waveform of the 32.768 kHz and 1 Hz output signals may become short.

Remark ×: don't care

(3) Real-time counter control register 1 (RTCC1)

The RTCC1 register is an 8-bit register that is used to control the alarm interrupt function and the wait time of the counter.

The RTCC1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-4. Format of Real-Time Counter Control Register 1 (RTCC1) (1/2)

Address: FFF9EH After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	0	WAFG	RIFG	0	RWST	RWAIT

WALE	Alarm operation control
0	Match operation is invalid.
1	Match operation is valid.
When setting a value to the WALE bit while the counter operates (RTCE = 1) and WALIE = 1, rewrite the WALE bit after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG and RTCIF flags after rewriting the WALE bit. When setting each alarm register (WALIE flag of real-time counter control register 1 (RTCC1), the alarm minute register (ALARMWM), the alarm hour register (ALARMWH), and the alarm week register (ALARMWW)), set match operation to be invalid (“0”) for the WALE bit.	

WALIE	Control of alarm interrupt (INTRTC) function operation
0	Does not generate interrupt on matching of alarm.
1	Generates interrupt on matching of alarm.

WAFG	Alarm detection status flag
0	Alarm mismatch
1	Detection of matching of alarm
This is a status flag that indicates detection of matching with the alarm. It is valid only when WALE = 1 and is set to “1” one clock (32.768 kHz) after matching of the alarm is detected. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

Figure 9-4. Format of Real-Time Counter Control Register 1 (RTCC1) (2/2)

RIFG	Constant-period interrupt status flag
0	Constant-period interrupt is not generated.
1	Constant-period interrupt is generated.
This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to “1”. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

RWST	Wait status flag of real-time counter
0	Counter is operating.
1	Mode to read or write counter value
This status flag indicates whether the setting of the RWAIT bit is valid. Before reading or writing the counter value, confirm that the value of this flag is 1.	

RWAIT	Wait control of real-time counter
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
This bit controls the operation of the counter. Be sure to write “1” to it to read or write the counter value. Because the sub-count register (RSUBC) continues operation, complete reading or writing of it in 1 second, and clear this bit back to 0. When RWAIT = 1, it takes up to 1 clock (32.768 kHz) until the counter value can be read or written. If the RSUBC register overflows when RWAIT = 1, the counter counts up after RWAIT = 0. If the second count register is written, however, the RSUBC register is cleared.	

Caution If writing is performed to the RTCC1 register with a 1-bit manipulation instruction, the RIFG flag and WAFG flag may be cleared. Therefore, to perform writing to the RTCC1 register, be sure to use an 8-bit manipulation instruction. To prevent the RIFG flag and WAFG flag from being cleared during writing, disable writing by setting 1 to the corresponding bit. If the RIFG flag and WAFG flag are not used and the value may be changed, the RTCC1 register may be written by using a 1-bit manipulation instruction.

Remark Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

(4) Real-time counter control register 2 (RTCC2)

The RTCC2 register is an 8-bit register that is used to control the interval interrupt function and the RTCDIV pin.

The RTCC2 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-5. Format of Real-Time Counter Control Register 2 (RTCC2)

Address: FFF9FH After reset: 00H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
RTCC2	RINTE	RCLOE2	RCKDIV	0	0	ICT2	ICT1	ICT0

RINTE	ICT2	ICT1	ICT0	Interval interrupt (INTRTCI) selection
0	×	×	×	Interval interrupt is not generated.
1	0	0	0	$2^6/f_{XT}$ (1.953125 ms)
1	0	0	1	$2^7/f_{XT}$ (3.90625 ms)
1	0	1	0	$2^8/f_{XT}$ (7.8125 ms)
1	0	1	1	$2^9/f_{XT}$ (15.625 ms)
1	1	0	0	$2^{10}/f_{XT}$ (31.25 ms)
1	1	0	1	$2^{11}/f_{XT}$ (62.5 ms)
1	1	1	×	$2^{12}/f_{XT}$ (125 ms)

RCLOE2[Note]	RTCDIV pin output control
0	Output of the RTCDIV pin is disabled.
1	Output of the RTCDIV pin is enabled.

RCKDIV	Selection of RTCDIV pin output frequency
0	The RTCDIV pin outputs 512 Hz. (1.95 ms)
1	The RTCDIV pin outputs 16.384 kHz. (0.061 ms)

Notes The RCLOE0 and RCLOE2 bits must not be enabled at the same time.

Cautions 1. Change the ICT2, ICT1, and ICT0 bits when RINTE = 0.

2. When the output from the RTCDIV pin is stopped, the output continues after a maximum of two clocks of f_{XT} and enters the low level. While 512 Hz is output, and when the output is stopped immediately after entering the high level, a pulse of at least one clock width of f_{XT} may be generated.

3. After the real-time counter starts operating, the output width of the RTCDIV pin may be shorter than as set during the first interval period.

(5) Sub-count register (RSUBC)

The RSUBC register is a 16-bit register that counts the reference time of 1 second of the real-time counter. Normally, it takes a value of 0000H to 7FFFH and counts 1 second with a clock of 32.768 kHz.

The RSUBC register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Cautions 1. When a correction is made by using the watch error correction register (SUBCUD), the value may become 8000H or more.

2. This register is also cleared by reset effected by writing the second count register.

3. The value read from this register is not guaranteed if it is read during operation, because a value that is changing is read.

Figure 9-6. Format of Sub-Count Register (RSUBC)

Address: FFF90H After reset: 0000H R

Symbol	7	6	5	4	3	2	1	0
RSUBC	SUBC7	SUBC6	SUBC5	SUBC4	SUBC3	SUBC2	SUBC1	SUBC0

Address: FFF91H After reset: 0000H R

Symbol	7	6	5	4	3	2	1	0
RSUBC	SUBC15	SUBC14	SUBC13	SUBC12	SUBC11	SUBC10	SUBC9	SUBC8

(6) Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds.

It counts up when the sub-counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Set a decimal value of 00 to 59 to this register in BCD code. If a value outside the range is set, the register value returns to the normal value after 1 period.

The SEC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-7. Format of Second Count Register (SEC)

Address: FFF92H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SEC	0	SEC40	SEC20	SEC10	SEC8	SEC4	SEC2	SEC1

(7) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code. If a value outside the range is set, the register value returns to the normal value after 1 period.

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-8. Format of Minute Count Register (MIN)

Address: FFF93H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
MIN	0	MIN40	MIN20	MIN10	MIN8	MIN4	MIN2	MIN1

(8) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time counter control register 0 (RTCC0).

If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system.

If a value outside the range is set, the register value returns to the normal value after 1 period.

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Figure 9-9. Format of Hour Count Register (HOUR)

Address: FFF94H After reset: 12H R/W

Symbol	7	6	5	4	3	2	1	0
HOUR	0	0	HOUR20	HOUR10	HOUR8	HOUR4	HOUR2	HOUR1

Caution Bit 5 (HOUR20) of the HOUR register indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

Table 9-2 shows the relationship between the setting value of the AMPM bit, the hour count register (HOUR) value, and time.

Table 9-2. Displayed Time Digits

24-Hour Display (AMPM = 1)		12-Hour Display (AMPM = 0)	
Time	HOUR Register	Time	HOUR Register
0	00H	0 a.m.	12H
1	01H	1 a.m.	01H
2	02H	2 a.m.	02H
3	03H	3 a.m.	03H
4	04H	4 a.m.	04H
5	05H	5 a.m.	05H
6	06H	6 a.m.	06H
7	07H	7 a.m.	07H
8	08H	8 a.m.	08H
9	09H	9 a.m.	09H
10	10H	10 a.m.	10H
11	11H	11 a.m.	11H
12	12H	0 p.m.	32H
13	13H	1 p.m.	21H
14	14H	2 p.m.	22H
15	15H	3 p.m.	23H
16	16H	4 p.m.	24H
17	17H	5 p.m.	25H
18	18H	6 p.m.	26H
19	19H	7 p.m.	27H
20	20H	8 p.m.	28H
21	21H	9 p.m.	29H
22	22H	10 p.m.	30H
23	23H	11 p.m.	31H

The HOUR register value is set to 12-hour display when the AMPM bit is “0” and to 24-hour display when the AMPM bit is “1”.

In 12-hour display, the fifth bit of the HOUR register displays 0 for AM and 1 for PM.

(9) Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.
It counts up when the hour counter overflows.
This counter counts as follows.

- 01 to 31 (January, March, May, July, August, October, December)
- 01 to 30 (April, June, September, November)
- 01 to 29 (February, leap year)
- 01 to 28 (February, normal year)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code. If a value outside the range is set, the register value returns to the normal value after 1 period.
The DAY register can be set by an 8-bit memory manipulation instruction.
Reset signal generation clears this register to 01H.

Figure 9-10. Format of Day Count Register (DAY)

Address: FFF96H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
DAY	0	0	DAY20	DAY10	DAY8	DAY4	DAY2	DAY1

(10) Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays.

It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Set a decimal value of 00 to 06 to this register in BCD code. If a value outside the range is set, the register value returns to the normal value after 1 period.

The WEEK register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-11. Format of Week Count Register (WEEK)

Address: FFF95H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
WEEK	0	0	0	0	0	WEEK4	WEEK2	WEEK1

Caution The value corresponding to the month count register (MONTH) or the day count register (DAY) is not stored in the week count register (WEEK) automatically. After reset release, set the week count register as follow.

Day	WEEK
Sunday	00H
Monday	01H
Tuesday	02H
Wednesday	03H
Thursday	04H
Friday	05H
Saturday	06H

(11) Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months.

It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code. If a value outside the range is set, the register value returns to the normal value after 1 period.

The MONTH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Figure 9-12. Format of Month Count Register (MONTH)

Address: FFF97H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
MONTH	0	0	0	MONTH10	MONTH8	MONTH4	MONTH2	MONTH1

(12) Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years.

It counts up when the month count register (MONTH) overflows.

Values 00, 04, 08, …, 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Even if the MONTH register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code. If a value outside the range is set, the register value returns to the normal value after 1 period.

The YEAR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-13. Format of Year Count Register (YEAR)

Address: FFF98H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
YEAR	YEAR80	YEAR40	YEAR20	YEAR10	YEAR8	YEAR4	YEAR2	YEAR1

(13) Watch error correction register (SUBCUD)

This register is used to correct the watch with high accuracy when it is slow or fast by changing the value that overflows from the sub-count register (RSUBC) to the second count register (SEC) (reference value: 7FFFH).

The SUBCUD register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-14. Format of Watch Error Correction Register (SUBCUD)

Address: FFF99H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SUBCUD	DEV	F6	F5	F4	F3	F2	F1	F0

DEV	Setting of watch error correction timing
0	Corrects watch error when the second digits are at 00, 20, or 40 (every 20 seconds).
1	Corrects watch error only when the second digits are at 00 (every 60 seconds).
Writing to the SUBCUD register at the following timing is prohibited. • When DEV = 0 is set: For a period of SEC = 00H, 20H, 40H • When DEV = 1 is set: For a period of SEC = 00H	

F6	Setting of watch error correction value
0	Increases by {(F5, F4, F3, F2, F1, F0) – 1} × 2.
1	Decreases by {(/F5, /F4, /F3, /F2, /F1, /F0) + 1} × 2.
When (F6, F5, F4, F3, F2, F1, F0) = (*, 0, 0, 0, 0, 0, *), the watch error is not corrected. * is 0 or 1. /F5 to /F0 are the inverted values of the corresponding bits (000011 when 111100). Range of correction value: (when F6 = 0) 2, 4, 6, 8, … , 120, 122, 124 (when F6 = 1) –2, –4, –6, –8, … , –120, –122, –124	

The range of value that can be corrected by using the watch error correction register (SUBCUD) is shown below.

	DEV = 0 (correction every 20 seconds)	DEV = 1 (correction every 60 seconds)
Correctable range	–189.2 ppm to 189.2 ppm	–63.1 ppm to 63.1 ppm
Maximum excludes quantization error	± 1.53 ppm	± 0.51 ppm
Minimum resolution	± 3.05 ppm	± 1.02 ppm

Remark If a correctable range is −63.1 ppm or lower and 63.1 ppm or higher, set 0 to DEV.

(14) Alarm minute register (ALARMWM)

This register is used to set minutes of alarm.

The ALARMWM register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Caution Set a decimal value of 00 to 59 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

Figure 9-15. Format of Alarm Minute Register (ALARMWM)

Address: FFF9AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWM	0	WM40	WM20	WM10	WM8	WM4	WM2	WM1

(15) Alarm hour register (ALARMWH)

This register is used to set hours of alarm.

The ALARMWH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Caution Set a decimal value of 00 to 23, 01 to 12, or 21 to 32 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

Figure 9-16. Format of Alarm Hour Register (ALARMWH)

Address: FFF9BH After reset: 12H R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWH	0	0	WH20	WH10	WH8	WH4	WH2	WH1

Caution Bit 5 (WH20) of the ALARMWH register indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

(16) Alarm week register (ALARMWW)

This register is used to set date of alarm.

The ALARMWW register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-17. Format of Alarm Week Register (ALARMWW)

Address: FFF9CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWW	0	WW6	WW5	WW4	WW3	WW2	WW1	WW0

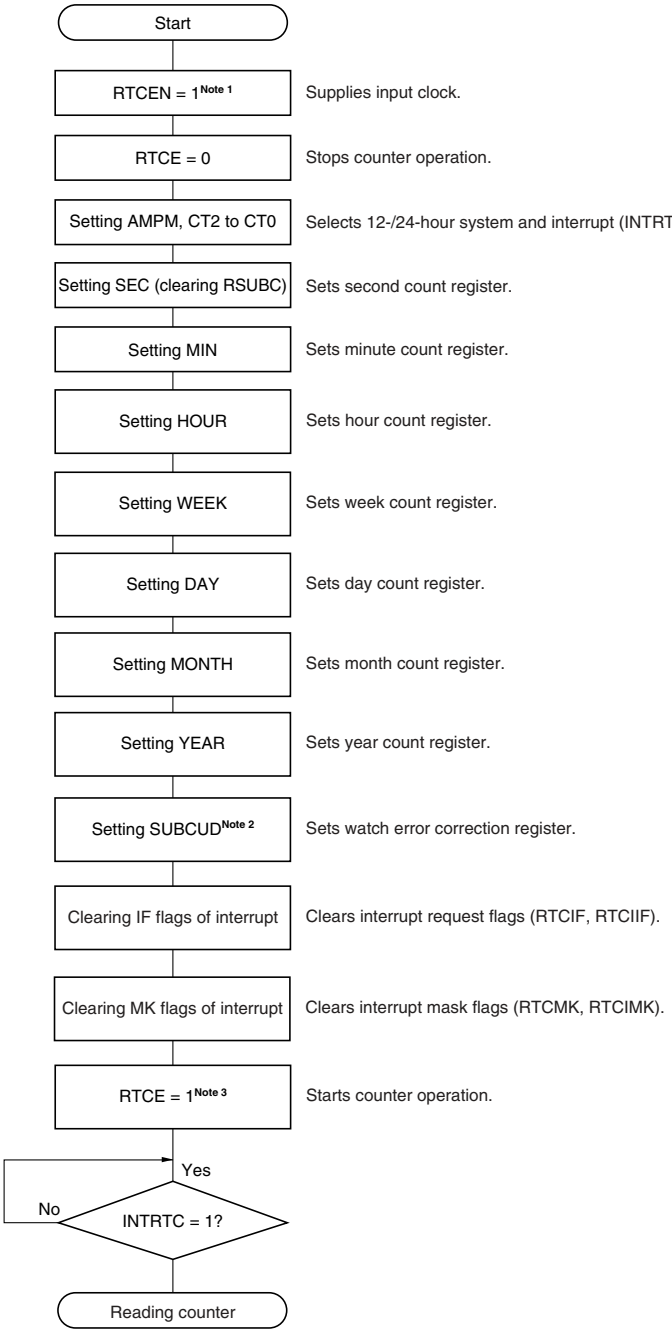
Here is an example of setting the alarm.

Time of Alarm	Day							12-Hour Display				24-Hour Display			
	Sunday WW0	Monday WW1	Tuesday WW2	Wednesday WW3	Thursday WW4	Friday WW5	Saturday WW6	Hour 10	Hour 1	Minute 10	Minute 1	Hour 10	Hour 1	Minute 10	Minute 1
Every day, 0:00 a.m.	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
Every day, 1:30 a.m.	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
Every day, 11:59 a.m.	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
Monday through Friday, 0:00 p.m.	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
Sunday, 1:30 p.m.	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
Monday, Wednesday, Friday, 11:59 p.m.	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

9.4 Real-Time Counter Operation

9.4.1 Starting operation of real-time counter

Figure 9-18. Procedure for Starting Operation of Real-Time Counter



Notes 1. First set the RTCEN bit to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.

2. Set up the SUBCUD register only if the watch error must be corrected. For details about how to calculate the correction value, see **9.4.8 Example of watch error correction of real-time counter**.

3. Confirm the procedure described in **9.4.2 Shifting to STOP mode after starting operation** when shifting to STOP mode without waiting for INTRTC = 1 after RTCE = 1.

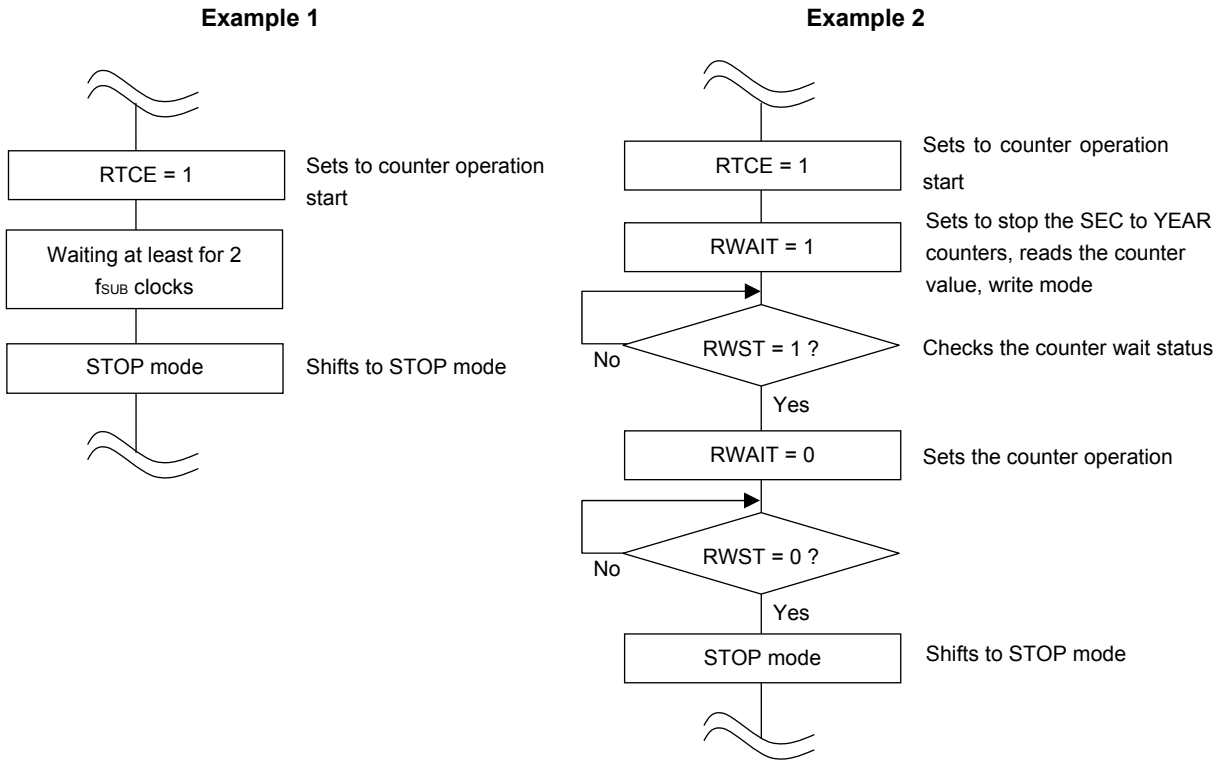
9.4.2 Shifting to STOP mode after starting operation

Perform one of the following processing when shifting to STOP mode immediately after setting the RTCE bit to 1.

However, after setting the RTCE bit to 1, this processing is not required when shifting to STOP mode after the first INTRTC interrupt has occurred.

- Shifting to STOP mode when at least two subsystem clocks (f_{SUB}) have elapsed after setting the RTCE bit to 1 (see **Figure 9-19**, **Example 1**).
- Checking by polling the RWST bit to become 1, after setting the RTCE bit to 1 and then setting the RWAIT bit to 1. Afterward, setting the RWAIT bit to 0 and shifting to STOP mode after checking again by polling that the RWST bit has become 0 (see **Figure 9-19**, **Example 2**).

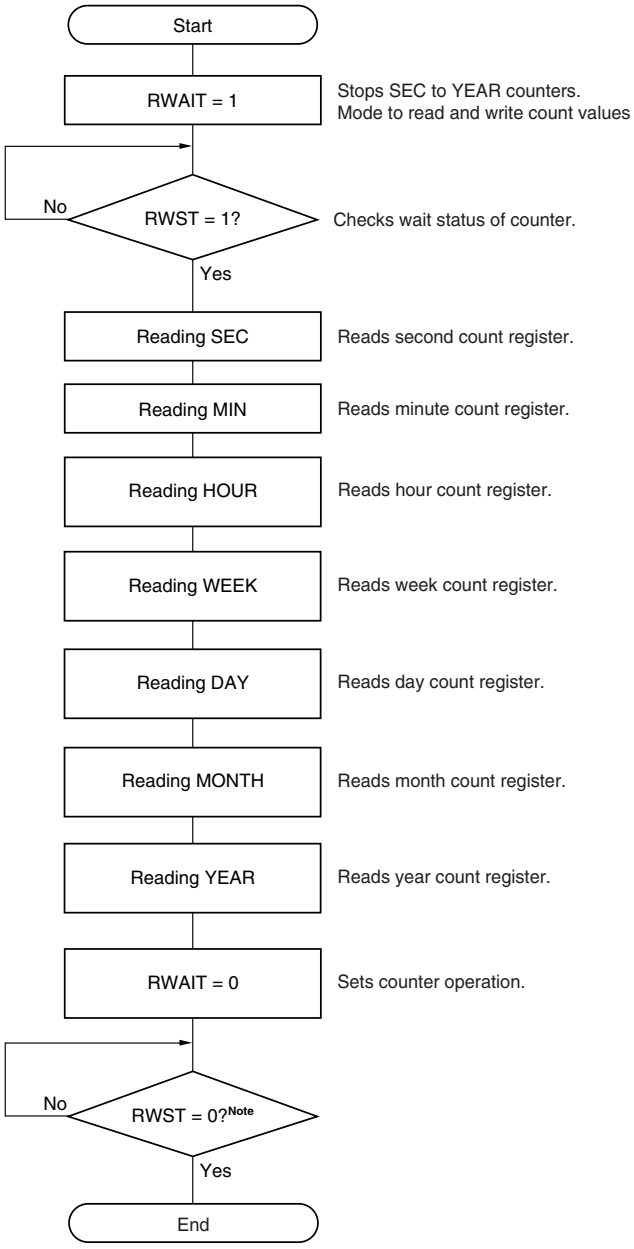
Figure 9-19. Procedure for Shifting to STOP Mode After Setting RTCE bit to 1



9.4.3 Reading/writing real-time counter

Read or write the counter after setting 1 to RWAIT first.

Figure 9-20. Procedure for Reading Real-Time Counter

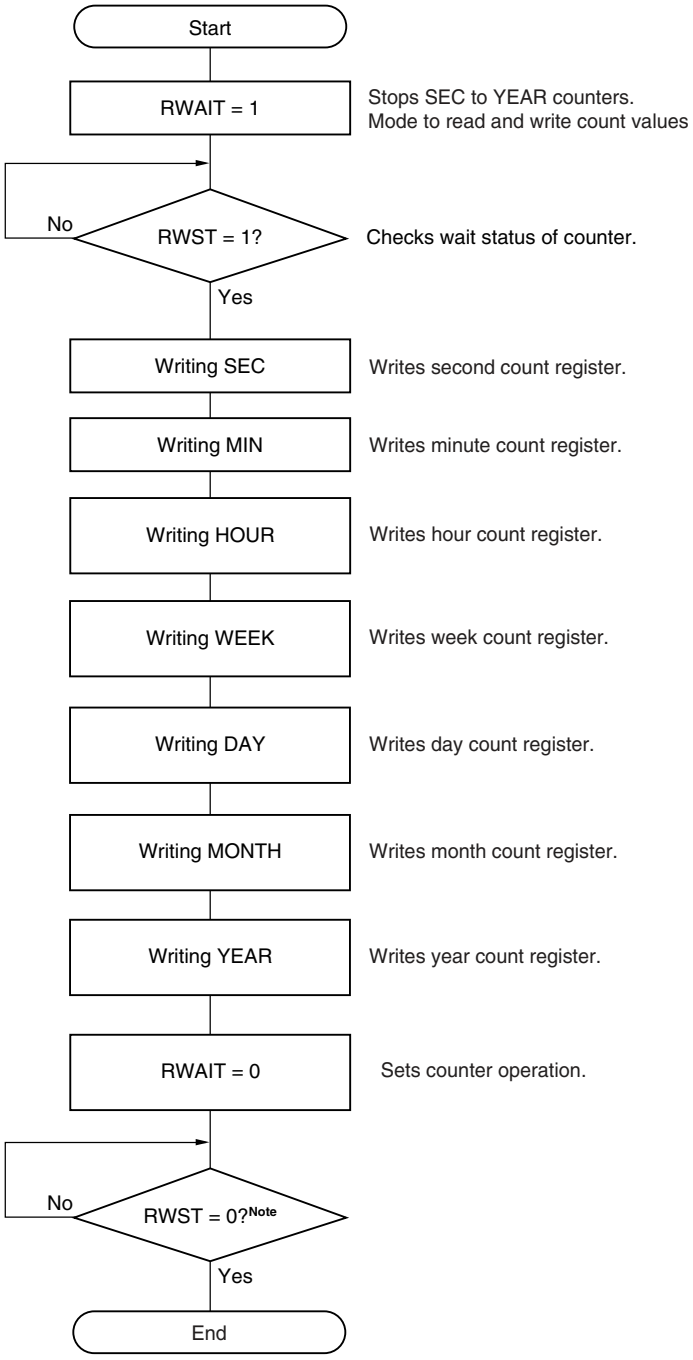


Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence.
All the registers do not have to be set and only some registers may be read.

Figure 9-21. Procedure for Writing Real-Time Counter



Note Be sure to confirm that RWST = 0 before setting STOP mode.

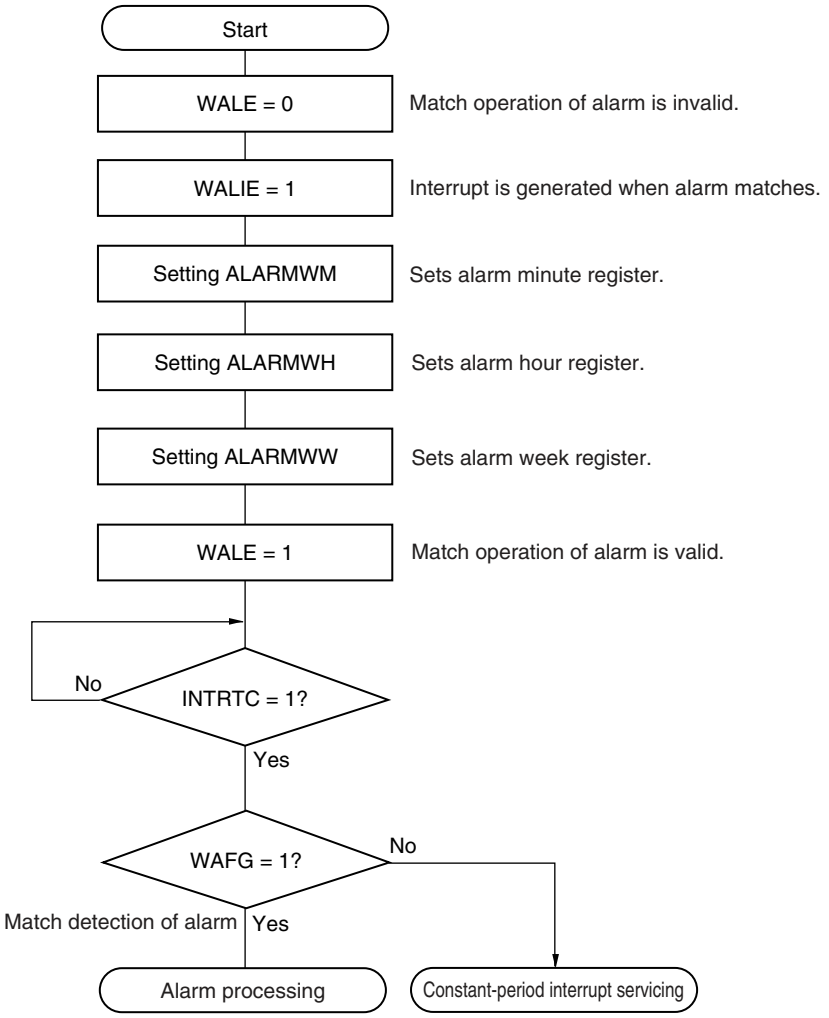
Caution Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence.
All the registers do not have to be set and only some registers may be written.

9.4.4 Setting alarm of real-time counter

Set time of alarm after setting 0 to WALE first.

Figure 9-22. Alarm Setting Procedure

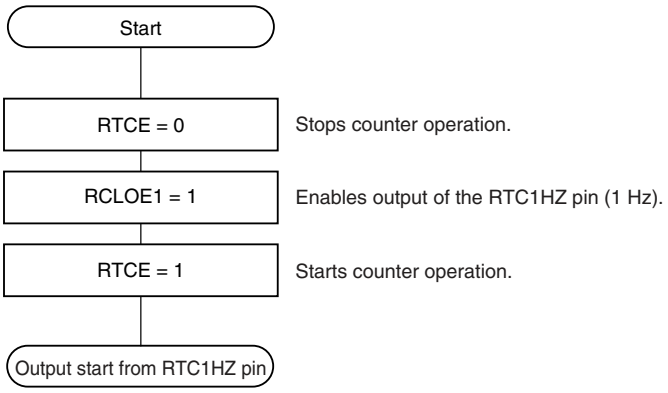


Remarks 1. The alarm week register (ALARMWW), alarm hour register (ALARMWH), and alarm week register (ALARMWW) may be written in any sequence.

2. Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

9.4.5 1 Hz output of real-time counter

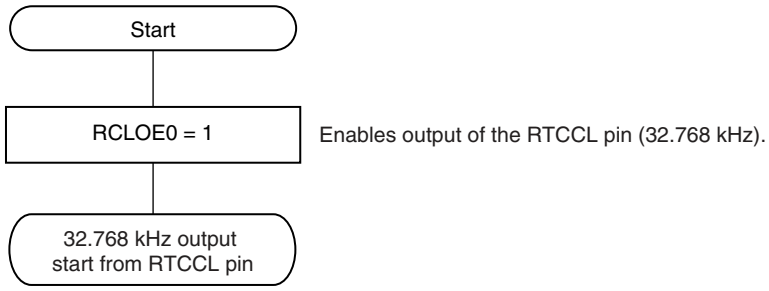
Figure 9-23. 1 Hz Output Setting Procedure



Caution First set the RTCEN bit to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.

9.4.6 32.768 kHz output of real-time counter

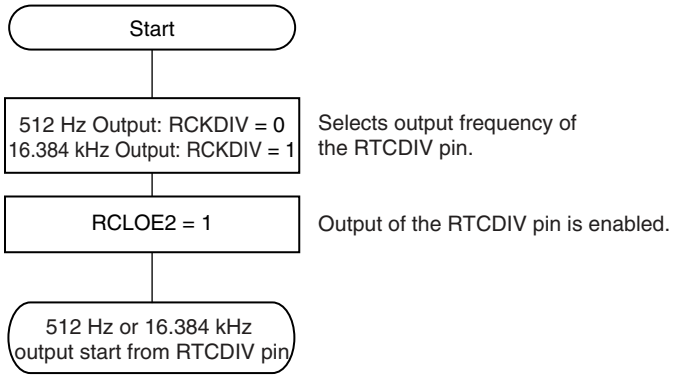
Figure 9-24. 32.768 kHz Output Setting Procedure



Caution First set the RTCEN bit to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.

9.4.7 512 Hz, 16.384 kHz output of real-time counter

Figure 9-25. 512 Hz, 16.384 kHz output Setting Procedure



Caution First set the RTCEN bit to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.

9.4.8 Example of watch error correction of real-time counter

The watch can be corrected with high accuracy when it is slow or fast, by setting a value to the watch error correction register.

Example of calculating the correction value

The correction value used when correcting the count value of the sub-count register (RSUBC) is calculated by using the following expression.

Set the DEV bit to 0 when the correction range is –63.1 ppm or less, or 63.1 ppm or more.

(When DEV = 0)

Correction value[Note] = Number of correction counts in 1 minute ÷ 3 = (Oscillation frequency ÷ Target frequency – 1) × 32768 × 60 ÷ 3

(When DEV = 1)

Correction value[Note] = Number of correction counts in 1 minute = (Oscillation frequency ÷ Target frequency – 1) × 32768 × 60

Note The correction value is the watch error correction value calculated by using bits 6 to 0 of the watch error correction register (SUBCUD).

(When F6 = 0) Correction value = {(F5, F4, F3, F2, F1, F0) – 1} × 2

(When F6 = 1) Correction value = – {(/F5, /F4, /F3, /F2, /F1, /F0) + 1} × 2

When (F6, F5, F4, F3, F2, F1, F0) is (*, 0, 0, 0, 0, 0, *), watch error correction is not performed. "*" is 0 or 1. /F5 to /F0 are bit-inverted values (000011 when 111100).

Remarks 1. The correction value is 2, 4, 6, 8, … 120, 122, 124 or –2, –4, –6, –8, … –120, –122, –124.

2. The oscillation frequency is the subsystem clock (f_{SUB}).
It can be calculated from the 32 kHz output frequency of the RTCCL pin or the output frequency of the RTC1HZ pin × 32768 when the watch error correction register is set to its initial value (00H).

3. The target frequency is the frequency resulting after correction performed by using the watch error correction register.

Correction example <1>

Example of correcting from 32772.3 Hz to 32768 Hz (32772.3 Hz – 131.2 ppm)

[Measuring the oscillation frequency]

The oscillation frequency[Note] of each product is measured by outputting about 32.768 kHz from the RTCCL pin or outputting about 1 Hz from the RTC1HZ pin when the watch error correction register (SUBCUD) is set to its initial value (00H).

Note See **9.4.5 1 Hz output of real-time counter** for the setting procedure of outputting about 1 Hz from the RTC1HZ pin, and **9.4.6 32.768 kHz output of real-time counter** for the setting procedure of outputting about 32 kHz from the RTCCL pin.

[Calculating the correction value]

(When the output frequency from the RTCCL pin is 32772.3 Hz)

If the target frequency is assumed to be 32768 Hz (32772.3 Hz – 131.2 ppm), the correction range for –131.2 ppm is –63.1 ppm or less, so assume DEV to be 0.

The expression for calculating the correction value when DEV is 0 is applied.

$$\begin{aligned}\text{Correction value} &= \text{Number of correction counts in 1 minute} \div 3\\ &= (\text{Oscillation frequency} \div \text{Target frequency} - 1) \times 32768 \times 60 \div 3\\ &= (32772.3 \div 32768 - 1) \times 32768 \times 60 \div 3\\ &= 86\end{aligned}$$

[Calculating the values to be set to (F6 to F0)]

(When the correction value is 86)

If the correction value is 0 or more (when delaying), assume F6 to be 0.

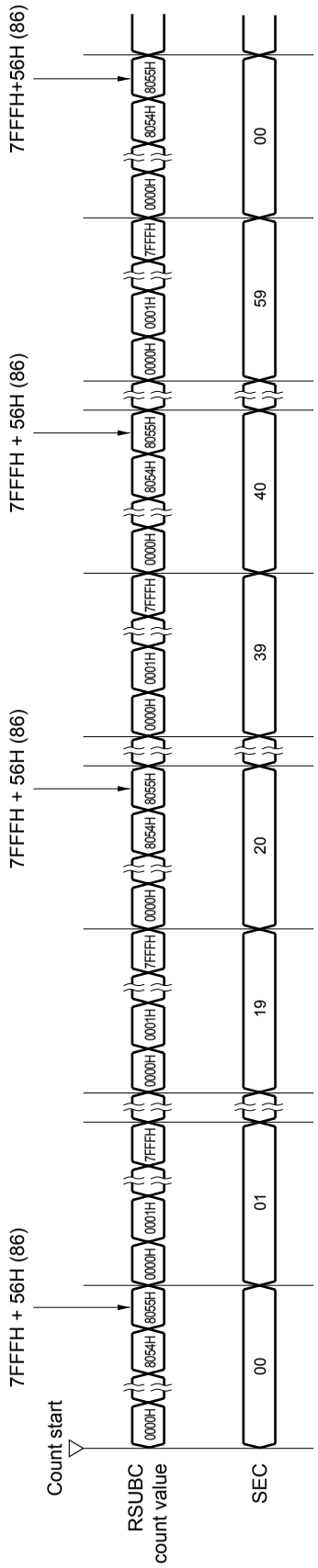
Calculate (F5, F4, F3, F2, F1, F0) from the correction value.

$$\begin{aligned}\{(F5, F4, F3, F2, F1, F0) - 1\} \times 2 &= 86\\ (F5, F4, F3, F2, F1, F0) &= 44\\ (F5, F4, F3, F2, F1, F0) &= (1, 0, 1, 1, 0, 0)\end{aligned}$$

Consequently, when correcting from 32772.3 Hz to 32768 Hz (32772.3 Hz – 131.2 ppm), setting the correction register such that DEV is 0 and the correction value is 86 (bits 6 to 0 of SUBCUD register: 0101100) results in 32768 Hz (0 ppm).

Figure 9-26 shows the operation when (DEV, F6, F5, F4, F3, F2, F1, F0) is (0, 0, 1, 0, 1, 1, 0, 0).

Figure 9-26. Operation when (DEV, F6, F5, F4, F3, F2, F1, F0) = (0, 0, 1, 0, 1, 1, 0, 0)



Correction example <2>

Example of correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm)

[Measuring the oscillation frequency]

The oscillation frequency[Note] of each product is measured by outputting about 32.768 kHz from the RTCCL pin or outputting about 1 Hz from the RTC1HZ pin when the watch error correction register (SUBCUD) is set to its initial value (00H).

Note See **9.4.5 1 Hz output of real-time counter** for the setting procedure of outputting about 1 Hz from the RTC1HZ pin, and **9.4.6 32.768 kHz output of real-time counter** for the setting procedure of outputting about 32 kHz from the RTCCL pin.

[Calculating the correction value]

(When the output frequency from the RTCCL pin is 0.9999817 Hz)

Oscillation frequency = 32768 × 0.9999817 ≈ 32767.4 Hz

Assume the target frequency to be 32768 Hz (32767.4 Hz + 18.3 ppm) and DEV to be 1.

The expression for calculating the correction value when DEV is 1 is applied.

Correction value = Number of correction counts in 1 minute
= (Oscillation frequency ÷ Target frequency − 1) × 32768 × 60
= (32767.4 ÷ 32768 − 1) × 32768 × 60
= −36

[Calculating the values to be set to (F6 to F0)]

(When the correction value is −36)

If the correction value is 0 or less (when quickening), assume F6 to be 1.

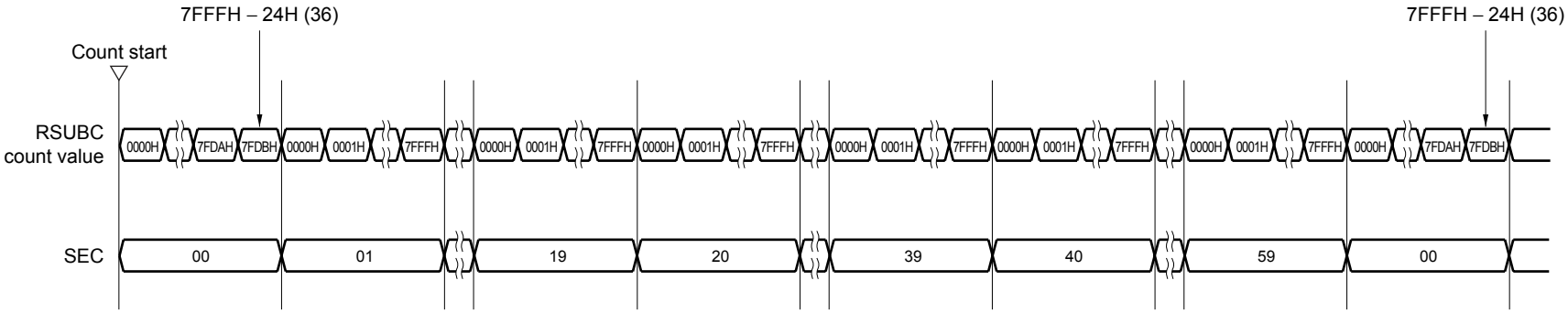
Calculate (F5, F4, F3, F2, F1, F0) from the correction value.

− {(/F5, /F4, /F3, /F2, /F1, /F0) − 1} × 2	= −36
(/F5, /F4, /F3, /F2, /F1, /F0)	= 17
(/F5, /F4, /F3, /F2, /F1, /F0)	= (0, 1, 0, 0, 0, 1)
(F5, F4, F3, F2, F1, F0)	= (1, 0, 1, 1, 1, 0)

Consequently, when correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm), setting the correction register such that DEV is 1 and the correction value is −36 (bits 6 to 0 of the SUBCUD register: 1101110) results in 32768 Hz (0 ppm).

Figure 9-27 shows the operation when (DEV, F6, F5, F4, F3, F2, F1, F0) is (1, 1, 1, 0, 1, 1, 1, 0).

Figure 9-27. Operation when (DEV, F6, F5, F4, F3, F2, F1, F0) = (1, 1, 1, 0, 1, 1, 1, 0)



CHAPTER 10 COMPARATORS/PROGRAMMABLE GAIN AMPLIFIERS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only)

The number of input pins of the comparators differs, depending on the product.

Input pins of the comparators	78K0R/KC3-L (40-pin)	78K0R/KC3-L (44, 48-pin)	78K0R/KD3-L	78K0R/KE3-L
CMP0P	√	√	√	√
CMP0M	√	√	√	√
CMP1P	−	√	√	√
CMP1M	√	√	√	√

10.1 Features of Comparator and Programmable Gain Amplifier

The features of the programmable gain amplifiers and comparators are described below.

○ Comparators
- A comparator is equipped with two channels (CMP0, CMP1).
- Negative-side input pins (CMP0M, CMP1M) and a positive-side input pin (CMP0P, CMP1P Note 1) can be connected.
- The output signal of a programmable gain amplifier can be used as the positive-side input signal of a comparator Note 2.
- The CMP0M and CMP1M pin inputs and the internal generation reference voltage (6 combinations for each comparator) can be selected as the reference voltage.
- The elimination width of the noise elimination digital filter can be selected.
- An interrupt request is generated when the reference voltage is exceeded (INTCMP0, INTCMP1).

○ Programmable gain amplifiers
- A programmable gain amplifier amplifies and outputs an analog voltage that is input. One among five amplification factors can be selected.
- The output signal of a programmable gain amplifier can be used as the positive-side input signal of a comparator Note 2.
- The output signal of a programmable gain amplifier can be selected as the analog input of an A/D converter.

Notes 1. There is no positive-side input pin (CMP1P) for comparator 1 in the 78K0R/KC3-L (40-pin). Only the signal output from the programmable gain amplifier can be used for the input voltage.

2. When using the output signals of the programmable gain amplifiers as the positive-side input signals of the comparators, the output signal is simultaneously input to both channels of comparators 0 and 1.

Figure 10-1. Block Diagram of Comparator/Programmable Gain Amplifier (78K0R/KC3-L (40-pin))

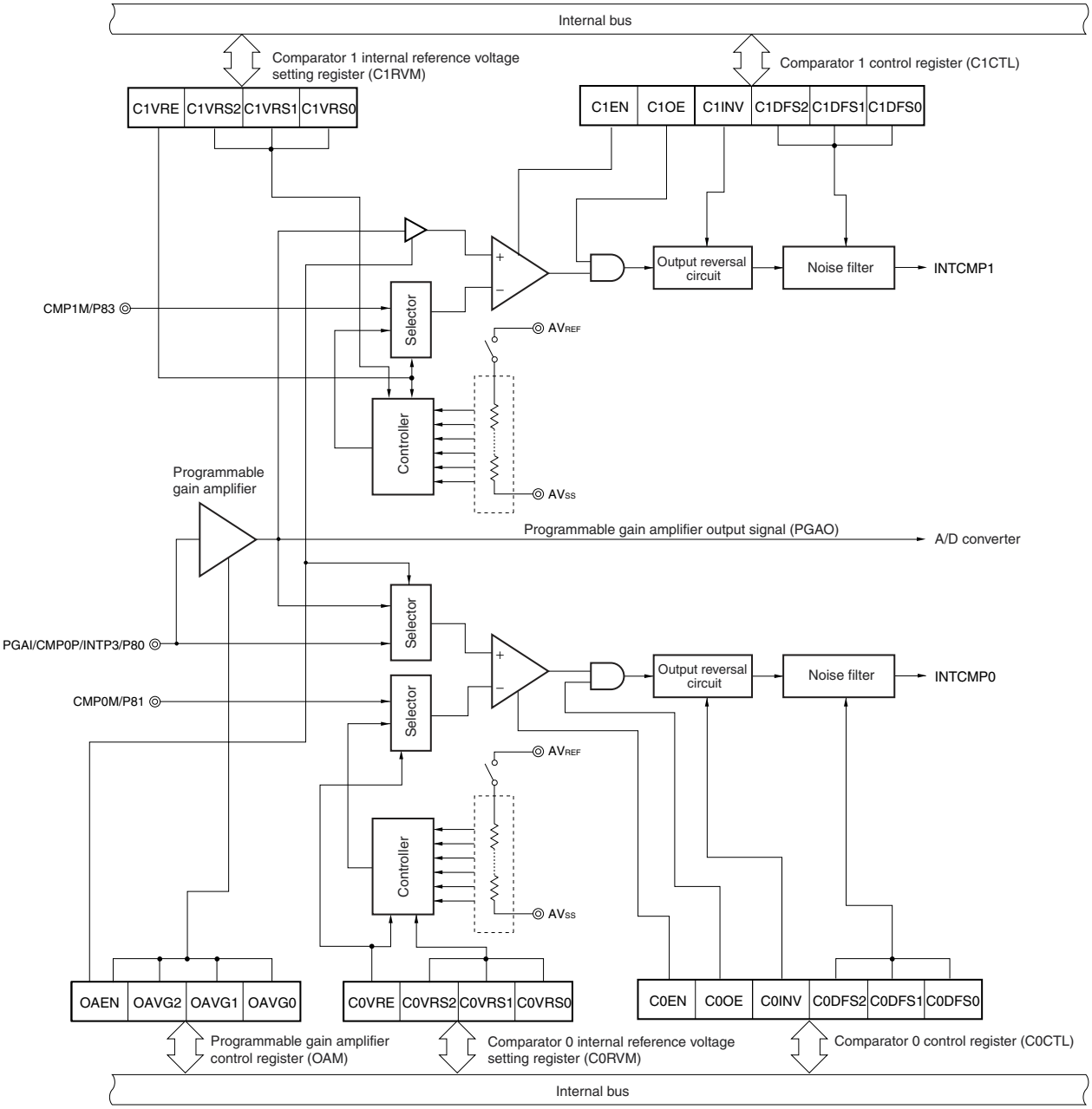
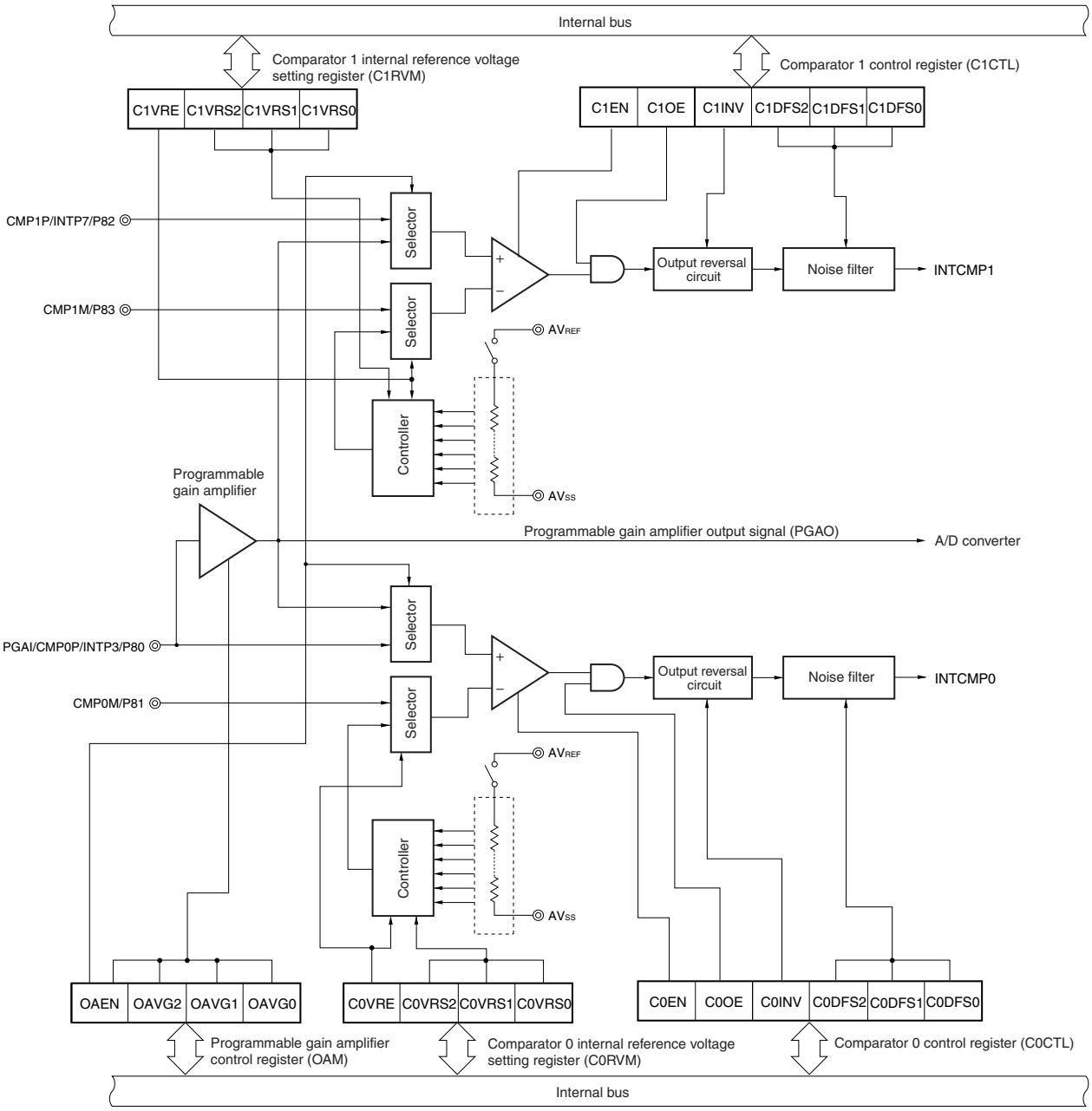


Figure 10-2. Block Diagram of Comparator/Programmable Gain Amplifier (78K0R/KC3-L (44-pin, 48-pin)), 78K0R/KD3-L, 78K0R/KE3-L



10.2 Configurations of Comparator and Programmable Gain Amplifier

The comparators and programmable gain amplifiers consist of the following hardware.

Table 10-1. Configurations of Comparator and Programmable Gain Amplifier

Item	Configuration
Control registers	Peripheral enable register 1 (PER1) Programmable gain amplifier control register (OAM) Comparator 0 and 1 control registers (C0CTL, C1CTL) Comparator 0 and 1 internal reference voltage setting registers (C0RVM, C1RVM) Port input mode register 8 (PIM8) Port mode register 8 (PM8)

10.3 Registers Controlling Comparators and Programmable Gain Amplifiers

The comparators and programmable gain amplifiers use the following eight registers.

- Peripheral enable register 1 (PER1)
- Programmable gain amplifier control register (OAM)
- Comparator 0 and 1 control registers (C0CTL, C1CTL)
- Comparator 0 and 1 internal reference voltage setting registers (C0RVM, C1RVM)
- Port input mode register 8 (PIM8)
- Port mode register 8 (PM8)

(1) Peripheral enable register 1 (PER1)

This register is used to enable or disable supplying the clock to the peripheral hardware. Power consumption and noise are reduced by stopping the clock supply to unused hardware.

Make sure to set bit 3 (OACMPEN) to 1 to use a comparator or a programmable gain amplifier.

The PER1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Cautions 1. Make sure to set the OACMPEN bit to 1 first, when setting the comparator or programmable gain amplifier. Writing to the control register of the comparator or programmable gain amplifier will be ignored and all values read will be initialized when the OACMPEN bit is set to 0.

2. Make sure to set bits 0 to 2 and bits 4 to 7 of the PER1 register to "0".

Figure 10-3. Format of Peripheral Enable Register 1 (PER1)

Address: F00F1H After reset: 00H R/W

Symbol	7	6	5	4	<3>	2	1	0
PER1	0	0	0	0	OACMPEN	0	0	0

OACMPEN	Control of comparator and programmable gain amplifier input clock supply
0	Stops input clock supply. • SFR used by the comparator and programmable gain amplifier cannot be written. • The comparator and programmable gain amplifier is in the reset status.
1	Enables input clock supply. • SFR used by the comparator and programmable gain amplifier can be read and written.

(2) Programmable gain amplifier control register (OAM)

This register is used to enable or disable the operation of a programmable gain amplifier and set the amplification factor.

The OAM register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-4. Format of Programmable Gain Amplifier Control Register (OAM)

Address: F0240H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
OAM	OAEN	0	0	0	0	OAVG2	OAVG1	OAVG0

OAEN	Programmable gain amplifier operation control
0	Stops operation
1	Enables operation Enables external input from the programmable gain amplifier input pin (PGAI) Inputs the programmable gain amplifier output signal as the positive-side input voltage of comparators 0 and 1

OAVG2	OAVG1	OAVG0	Input voltage amplification factor setting
0	0	1	×4
0	1	0	×6
0	1	1	×8
1	0	0	×10
1	0	1	×12
Other than the above			Setting prohibited

Cautions 1. Set the amplification factor before enabling (OAEN = 1) the operation of the programmable gain amplifier. Changing the amplification factor setting in the operation enabled state (OAEN = 1) is prohibited.

2. Set the comparator n control register (CnCTL) after setting the OAM register.

3. To select a program gain amplifier output signal (PGAO) as an analog input of the A/D converter, set OAEN = 1, wait for 3 μs by software, then start A/D conversion (ADCS = 1).

Remark n = 0, 1

(3) Comparator n control register (CnCTL)

This register is used to control the operation of comparator n, enable or disable comparator output, reverse the output, and set the noise elimination width.

The CnCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-5. Format of Comparator n Control Register (CnCTL)

Address: F0241H (C0CTL), F0242H (C1CTL) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CnCTL	CnEN	0	0	CnOE	CnINV	CnDFS2	CnDFS1	CnDFS0

CnEN	Comparator operation control
0	Stops operation
1	Enables operation Enables input to the external pins on the positive and negative sides of comparator n Notes 1, 2

CnOE	Enabling or disabling of comparator output
0	Disables output (output signal = fixed to low level)
1	Enables output

CnINV	Output reversal setting
0	Forward
1	Reverse Note 3

CnDFS2	CnDFS1	CnDFS0	Noise elimination width setting (f_{CLK} = 20 MHz)
0	0	0	Noise filter unused
0	0	1	250 ns
0	1	0	500 ns
0	1	1	1 μs
1	0	0	2 μs
Other than the above			Setting prohibited

(**Notes**, **Cautions,** and **Remarks** are listed on the next page.)

Notes 1. If OAEN = 1 (bit 7 of the programmable gain amplifier control register (OAM)) and the CnEN bit is set to 1, a programmable gain amplifier output signal will be input to the positive-side input of comparator n.

2. There is no positive-side input pin for comparator 1 in the 78K0R/KC3-L (40-pin). Only the signal output from the programmable gain amplifier can be used for the input voltage.

3. An interrupt will occur if the CnINV bit is set (CnINV = 1) while operation is stopped (CnEN = 0) or when output is prohibited (CnOE = 0). It is therefore necessary to mask the interrupt (CMPMKn = 1), and then enable operation (CnEN = 1) and output (CnOE = 1). After operation and output have been enabled, se t reverse output (CnINV = 1), clear the interrupt request flag (CMPIFn = 0), and then unmask the interru pt (CMPMKn = 0). While reverse output is in progress, be sure to mask the interrupt (CMPMKn = 1) bef ore stopping operation (CnEN = 0) or prohibiting output (CnOE = 0).

Cautions 1. Rewrite the CnINV and CnDFS2 to CnDFS0 bits after setting the comparator output to the disabled state (CnOE = 0).

2. With the noise elimination width, an extra CPU clock (f_{CLK}) may be eliminated from the setting value.
(Example: When f_{CLK} = 20 MHz, CnDFS2 to CnDFS0 = 001, noise elimination width = 250 to 300 ns)

3. To operate the comparator in combination with a programmable gain amplifier, set the operation of the comparator after setting the operation of the programmable gain amplifier (see Figure 10-10 and Figure 10-11).

4. The negative-side external pin input of the comparator will be cutoff when the CnVRE bit of the comparator n internal reference voltage selection register (CnRVM) is set (1), regardless of the value that enables or disables the comparator operation (CnEN bit).

5. Enable interrupt signals after setting CnEN = 1 and then waiting for 1 μs by software.

Remarks 1. f_{CLK}: CPU or peripheral hardware clock frequency

2. n = 0, 1

(4) Comparator n internal reference voltage selection register (CnRVM)

This register is used to set the internal reference voltage of comparator n. The internal reference voltage can be selected from six voltages that use AV_{REF}.

The CnRVM register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-6. Format of Comparator n Internal Reference Voltage Selection Register (CnRVM)

Address: F0243H (C0RVM), F0244H (C1RVM) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CnRVM	CnVRE	0	0	0	0	CnVRS2	CnVRS1	CnVRS0

CnVRE	Internal reference voltage operation control
0	Stops operation
1	Enables operation Connects the internal reference voltage to the negative-side input of comparator n

CnVRS2	CnVRS1	CnVRS0	Reference voltage setting	
			Reference voltage settable with comparator 0 (n = 0)	Reference voltage settable with comparator 1 (n = 1)
0	0	0	Setting prohibited	
0	0	1	$2AV_{REF}/16$	$3AV_{REF}/16$
0	1	0	$4AV_{REF}/16$	$5AV_{REF}/16$
0	1	1	$6AV_{REF}/16$	$7AV_{REF}/16$
1	0	0	$8AV_{REF}/16$	$9AV_{REF}/16$
1	0	1	$10AV_{REF}/16$	$11AV_{REF}/16$
1	1	0	$12AV_{REF}/16$	$13AV_{REF}/16$
1	1	1	Setting prohibited	

Cautions 1. The operation of the comparator is controlled by the CnEN bit when the operation of the internal reference voltage is stopped (CnVRE = 0).

2. The negative-side external pin input of the comparator will be cutoff when the CnVRE bit is set (1), regardless of the value that enables or disables the comparator operation (CnEN bit).

3. Set the reference voltage before enabling the operation of the internal reference voltage (CnVRE = 1). Changing the reference voltage setting in the operation enabled state (CnVRE = 1) is prohibited.

4. Be sure to change the CnRVM register while CnEN = 0 (comparator operation stopped).

Remark n = 0, 1

(5) Port input mode register 8 (PIM8)

This register is used to enable or disable port 8 digital input in 1-bit units.

Set to digital input disable (used as analog input) to use a comparator or a programmable gain amplifier. Set to digital input enable to use the port function or the external interrupt function, because digital input disable (used as analog input) is set by default.

The PIM8 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-7. Format of Port Input Mode Register 8 (PIM8)

Address: F0048H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM8	0	0	0	0	PIM83	PIM82 Note	PIM81	PIM80

PIM8n	Selection of enabling or disabling P8n pin digital input (n = 0 to 3)
0	Disables digital input (used as analog input)
1	Enables digital input

Note PIM82 bit is not provided in the 78K0R/KC3-L (40-pin).

(6) Port mode register 8 (PM8)

This register is used to set port 8 input or output in 1-bit units.

Set the PM80 to PM83 bits to 1 to use the P80/CMP0P/INTP3/PGAI, P81/CMP0M, P82/CMP1P/INTP7, or P83/CMP1M pin as the positive-side or negative-side input function of the comparator, or the programmable gain amplifier input function.

The output latches of P80 to P83 may be 0 or 1 at this time.

The PM80 to PM83 bits can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 10-8. Format of Port Mode Register 8 (PM8)

Address: FFF28H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM8	1	1	1	1	PM83	PM82 Note	PM81	PM80

PM8n	P8n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note PM82 bit is not provided in the 78K0R/KC3-L (40-pin).

Cautions 1. The port function that is alternatively used as the CMP0M, CMP1M pin can be used in the input mode, when the CMP0P, CMP1P pin is selected as the positive-side input of the comparator, and the internal reference voltage is used on the negative side. Using the output mode, however, is prohibited.

2. 78K0R/KC3-L (40-pin) does not have a P82/CMP1P/INTP7 pin.

10.4 Operations of Comparator and Programmable Gain Amplifier

10.4.1 Starting comparator and programmable gain amplifier operation

The procedures for starting the operation of a comparator and a programmable gain amplifier are described below, separately for each use method.

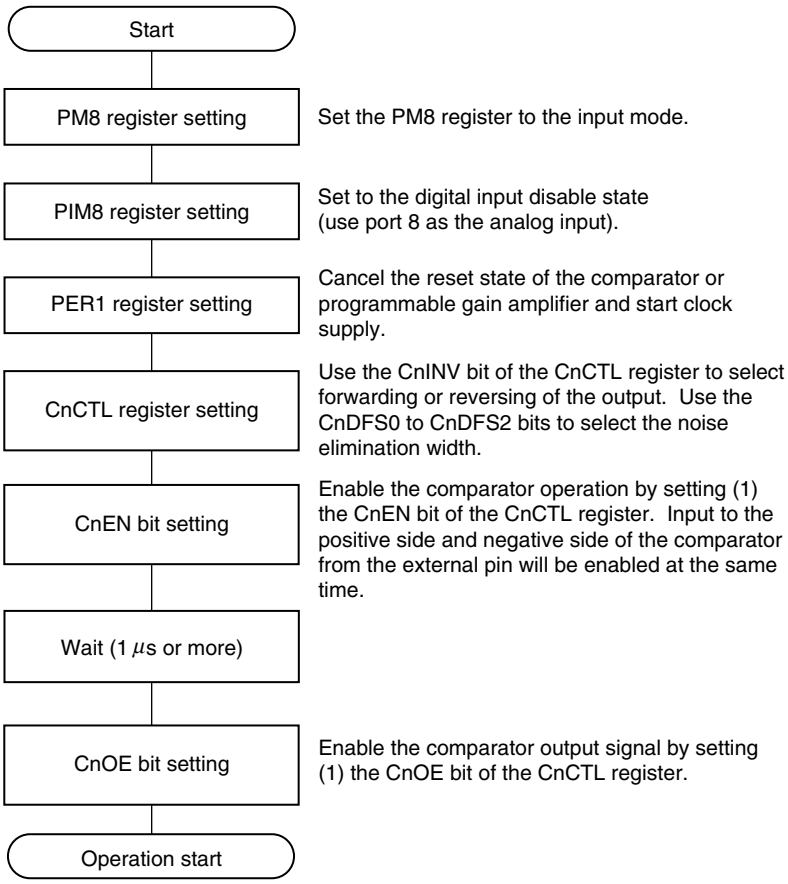
○ Using only a comparator[Note]
- Using the external pin input for the comparator reference voltage (Figure 10-9)
- Using the internal reference voltage for the comparator reference voltage (Figure 10-10)

○ Using a comparator and a programmable gain amplifier (using the programmable gain amplifier output voltage as the comparator compare voltage input)
- Using the external pin input for the comparator reference voltage (Figure 10-11)
- Using the internal reference voltage for the comparator reference voltage (Figure 10-12)

○ Using the programmable gain amplifier output voltage as the A/D converter analog input (Figure 10-13)

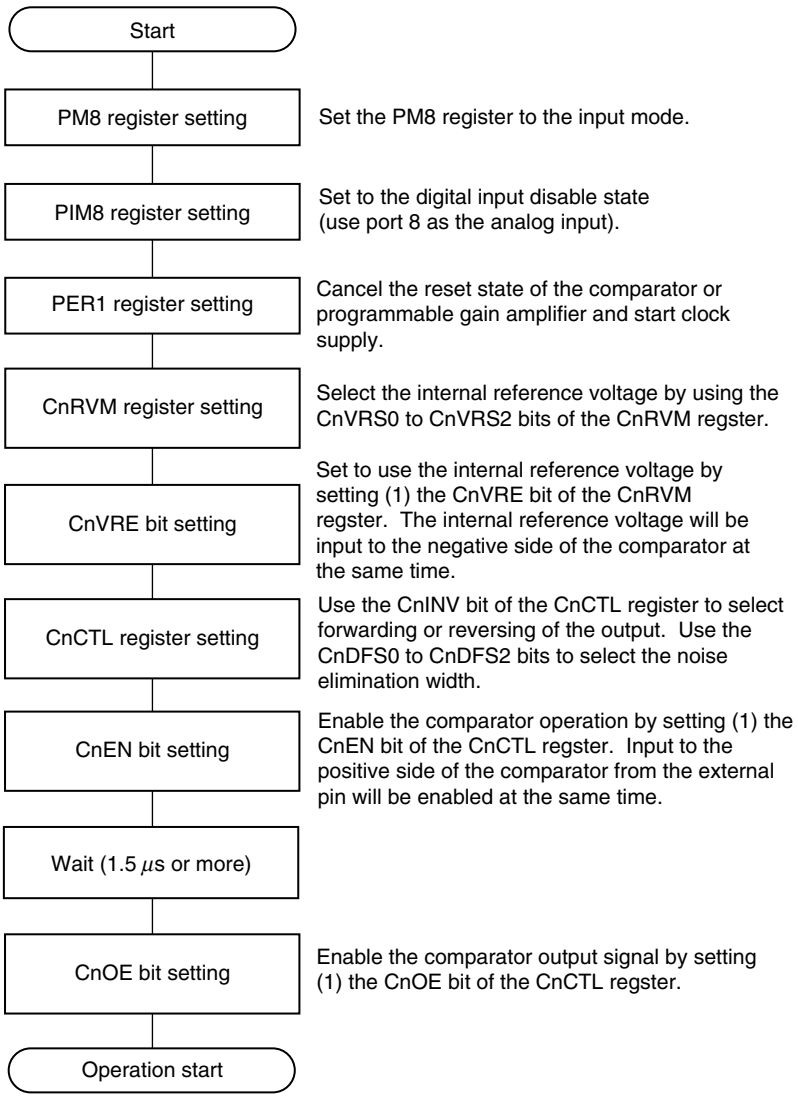
Note There is no positive-side input pin for comparator 1 in the 78K0R/KC3-L (40-pin). Only the signal output from the programmable gain amplifier can be used for the input voltage.

Figure 10-9. Using the External Pin Input for the Comparator Reference Voltage (Using Only a Comparator)



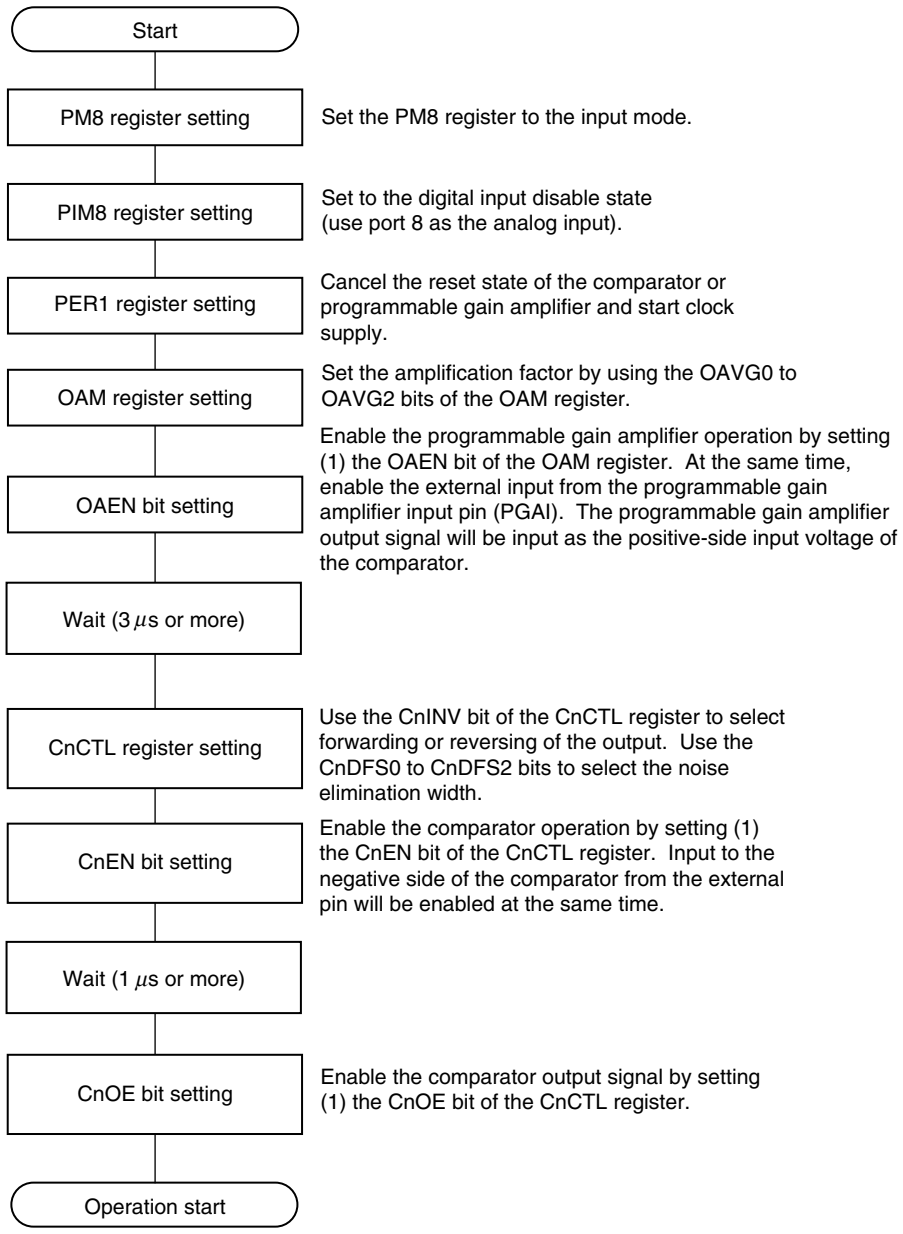
Remark n = 0 and 1 (78K0R/KC3-L (40-pin): n = 0).

Figure 10-10. Using the Internal Reference Voltage for the Comparator Reference Voltage (Using Only a Comparator)



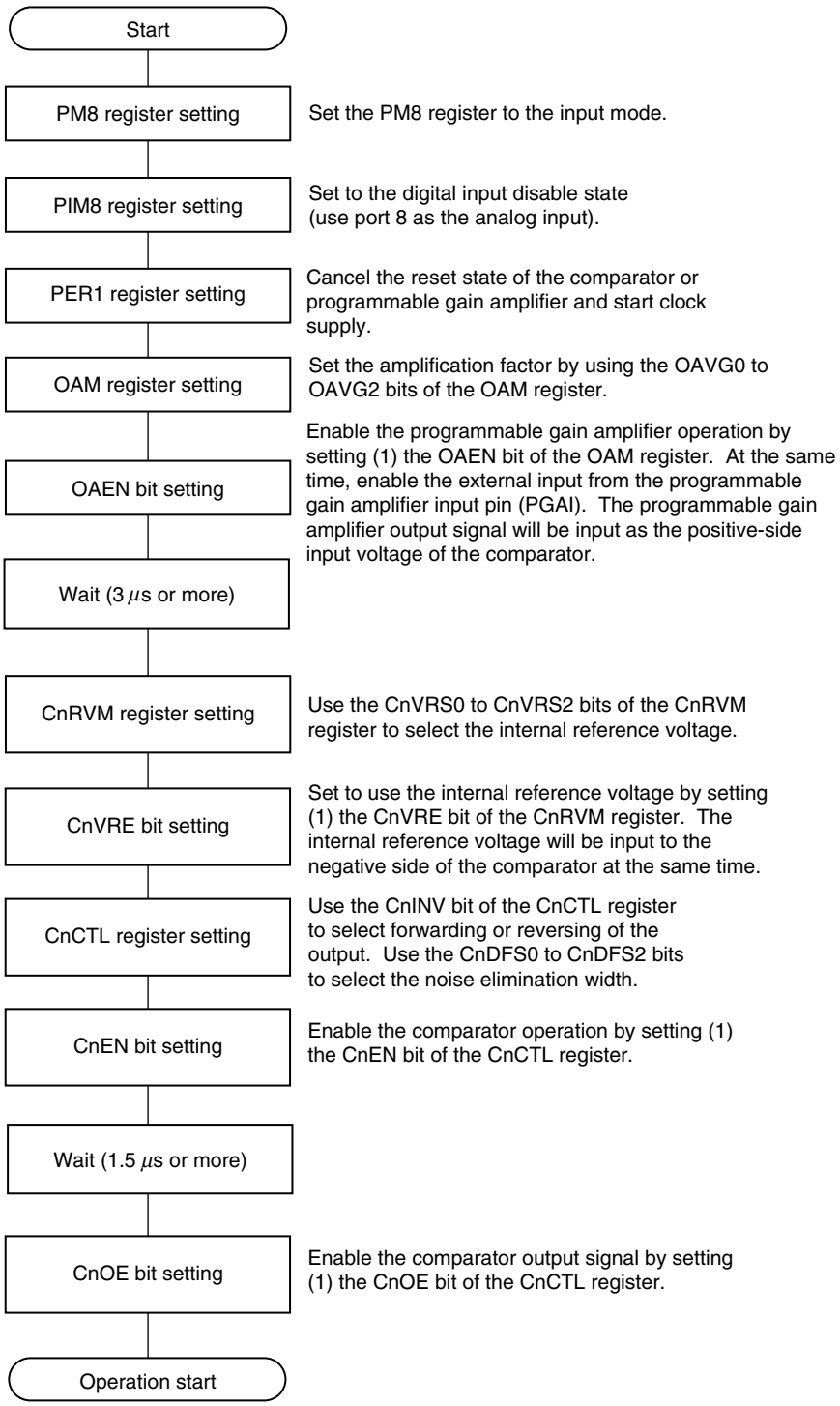
Remark n = 0 and 1 (78K0R/KC3-L (40-pin): n = 0).

Figure 10-11. Using the External Pin Input for the Comparator Reference Voltage (Using a Comparator and a Programmable Gain Amplifier)



Remark n = 0 and 1 (78K0R/KC3-L (40-pin): n = 0).

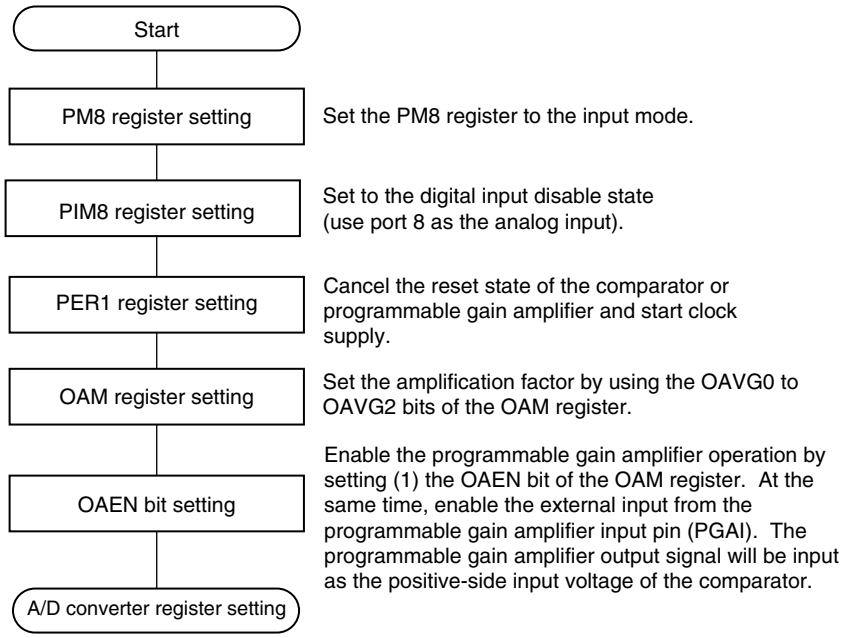
Figure 10-12. Using the Internal Reference Voltage for the Comparator Reference Voltage (Using a Comparator and a Programmable Gain Amplifier)



Remark n = 0, 1

Perform the following settings before selecting the programmable gain amplifier output signal as the analog input by using the analog input channel specification register (ADS) of the A/D converter (refer to **13.4.1 Basic operations of A/D converter**).

Figure 10-13. Using the Programmable Gain Amplifier Output Voltage as the A/D Converter Analog Input



Caution Ensure that 3 μs elapses before A/D conversion starts after setting the OAEN bit.

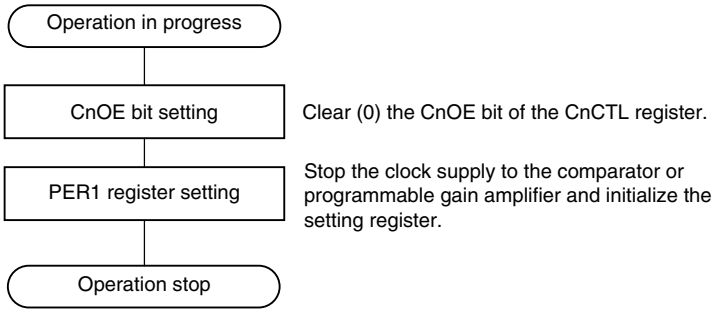
Remark n = 0, 1

10.4.2 Stopping comparator and programmable gain amplifier operation

The procedures for stopping the operation of a comparator and a programmable gain amplifier are described below, separately for each use method.

- ○ Using only a comparator (Figure 10-14)
- ○ Using the programmable gain amplifier output voltage as the comparator compare voltage input (Figure 10-15)
- ○ Using the programmable gain amplifier output voltage as the A/D converter analog input (Figure 10-16)

Figure 10-14. Using Only a Comparator



Remark n = 0 and 1 (78K0R/KC3-L (40-pin): n = 0).

Figure 10-15. Using the Programmable Gain Amplifier Output Voltage as the Comparator Compare Voltage Input

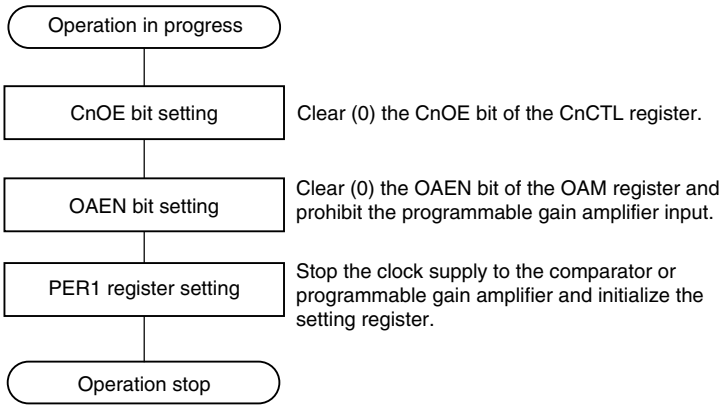
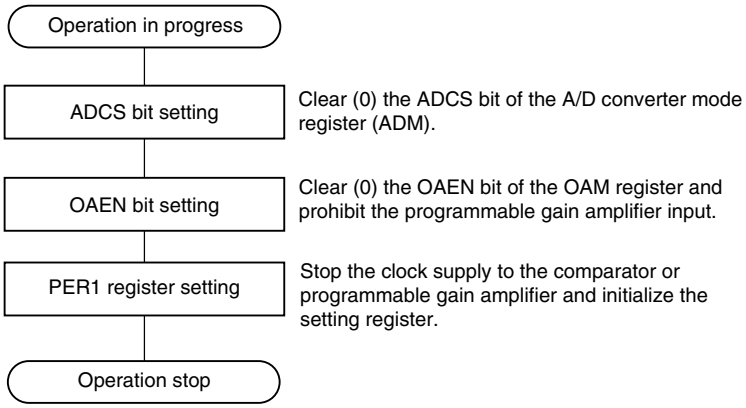


Figure 10-16. Using the Programmable Gain Amplifier Output Voltage as the A/D Converter Analog Input



Remark n = 0, 1

CHAPTER 11 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER

The number of output pins of the clock output and buzzer output controllers differs, depending on the product. Furthermore, 44-pin product of the 78K0R/KC3-L are not provided with clock output and buzzer output controllers.

Output pin	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
PCLBUZ0	–	–	√	√	√	√	√
PCLBUZ1	–	–	–	–	√	√	√

11.1 Functions of Clock Output/Buzzer Output Controller

The clock output controller is intended for carrier output during remote controlled transmission and clock output for supply to peripheral ICs.

Buzzer output is a function to output a square wave of buzzer frequency.

One pin can be used to output a clock or buzzer sound.

Two output pins, PCLBUZ0 and PCLBUZ1, are available.

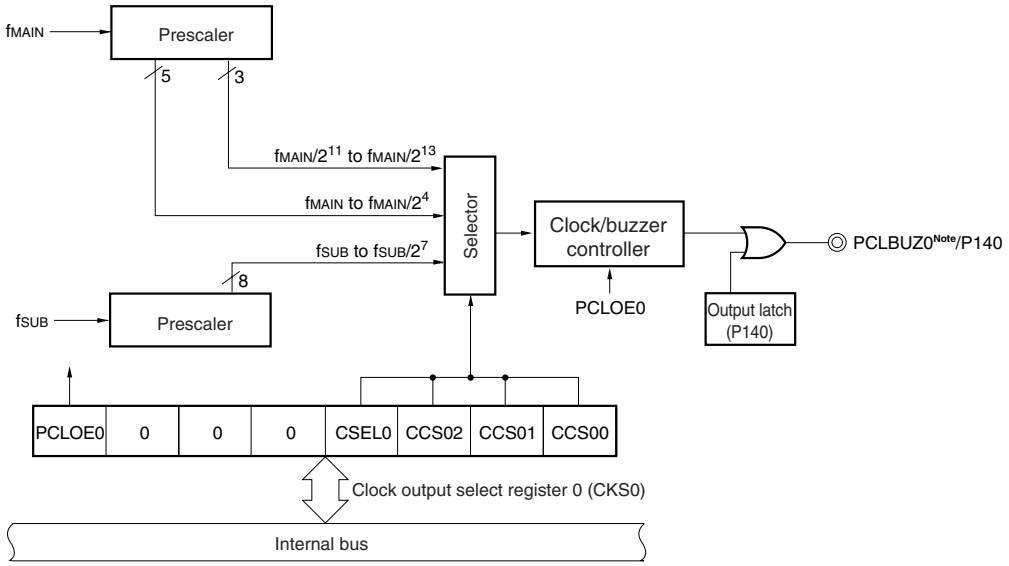
The PCLBUZn pin outputs a clock selected by clock output select register n (CKSn).

Figure 11-1 shows the block diagram of clock output/buzzer output controller.

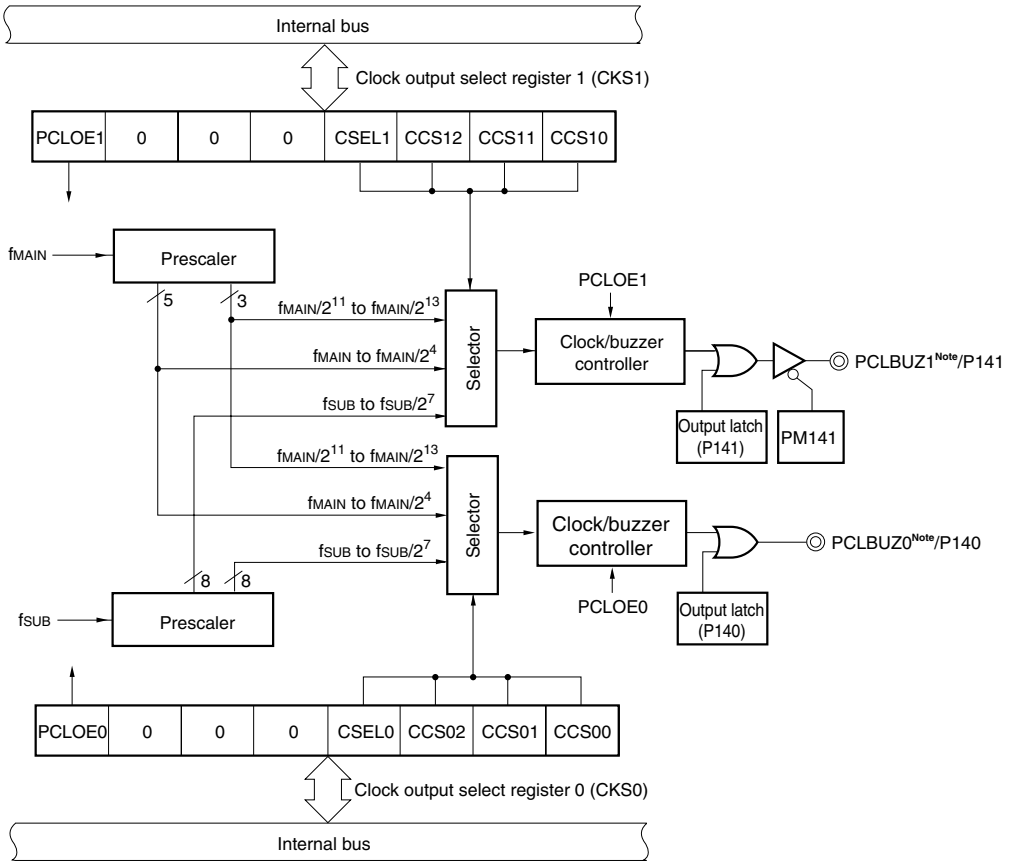
Remark n = 0: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
n = 0, 1: 78K0R/KE3-L, 78K0R/KF3-L, 78K0R/KG3-L

Figure 11-1. Block Diagram of Clock Output/Buzzer Output Controller (1/2)

- 78K0R/KC3-L (48-pin), 78K0R/KD3-L



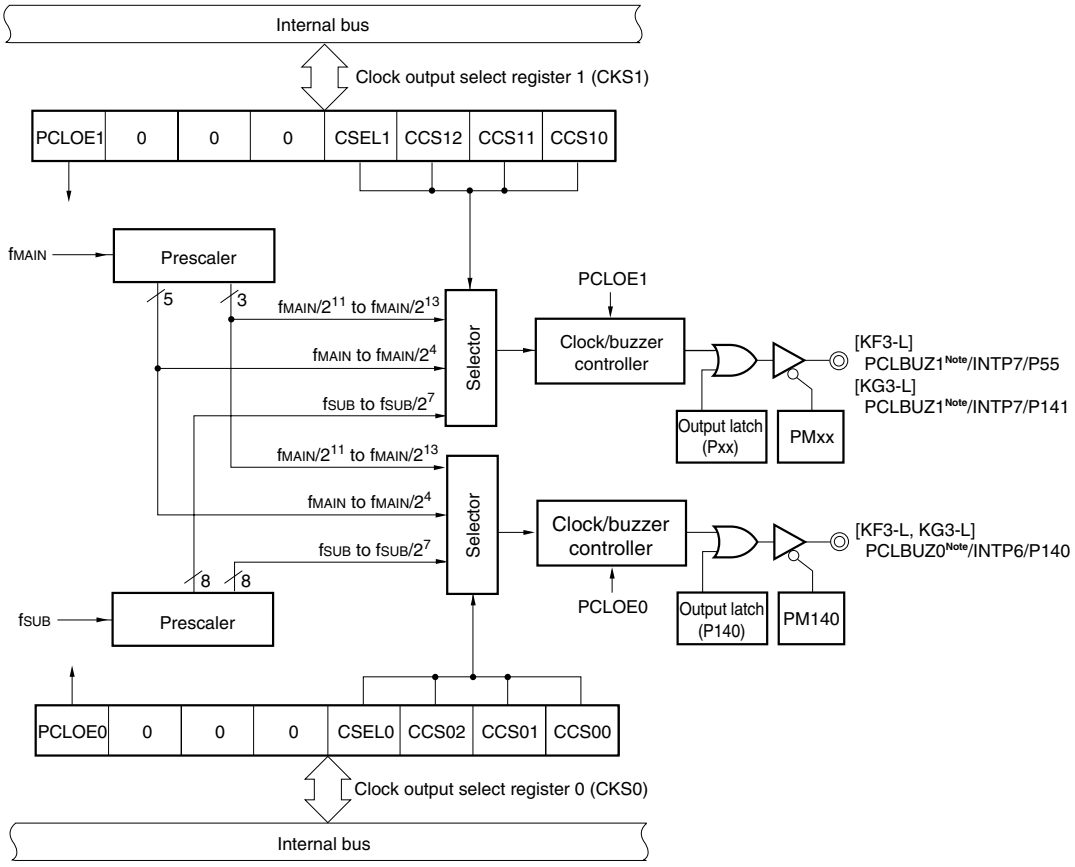
- 78K0R/KE3-L



Note The PCLBUZ0 and PCLBUZ1 pins can output a clock of up to 10 MHz at 2.7 V ≤ V_{DD}. Setting a clock exceeding 5 MHz at V_{DD} < 2.7 V is prohibited.

Figure 11-1. Block Diagram of Clock Output/Buzzer Output Controller (2/2)

- 78K0R/KF3-L, 78K0R/KG3-L



Note The PCLBUZ0 and PCLBUZ1 pins can output a clock of up to 10 MHz at 2.7 V ≤ V_{DD}. Setting a clock exceeding 5 MHz at V_{DD} < 2.7 V is prohibited.

Remark 78K0R/KE3-L: PMxx, Pxx = PM55, P55
78K0R/KG3-L: PMxx, Pxx = PM141, P141

11.2 Configuration of Clock Output/Buzzer Output Controller

The clock output/buzzer output controller includes the following hardware.

Table 11-1. Configuration of Clock Output/Buzzer Output Controller

Item	Configuration
Control registers	Clock output select registers n (CKSn) Port mode registers 5, 14 (PM5, PM14)Note Port registers 5, 14 (P5, P14) Note

Note The port mode register and port register to be set differ depending on the product.
78K0R/KC3-L (48-pin), 78K0R/KD3-L: P14
78K0R/KE3-L, 78K0R/KG3-L: PM14, P14
78K0R/KF3-L: PM5, P5, PM14, P14

Remark n = 0: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
n = 0, 1: 78K0R/KE3-L, 78K0R/KF3-L, 78K0R/KG3-L

11.3 Registers Controlling Clock Output/Buzzer Output Controller

The following two registers are used to control the clock output/buzzer output controller.

- Clock output select registers n (CKSn)
- Port mode registers 5, 14 (PM5, PM14) Note

Note The port register to be set differ depending on the product.
78K0R/KC3-L (48-pin), 78K0R/KD3-L: None
78K0R/KE3-L, 78K0R/KG3-L: PM14
78K0R/KF3-L: PM5, PM14

(1) Clock output select registers n (CKSn)

These registers set output enable/disable for clock output or for the buzzer frequency output pin (PCLBUZn), and set the output clock.

Select the clock to be output from the PCLBUZn pin by using the CKSn register.

The CKSn register are set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Remark n = 0: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
n = 0, 1: 78K0R/KE3-L, 78K0R/KF3-L, 78K0R/KG3-L

Figure 11-2. Format of Clock Output Select Register n (CKSn)

Address: FFFA5H (CKS0), FFFA6H (CKS1) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CKSn	PCLOEn	0	0	0	CSELn	CCSn2	CCSn1	CCSn0

PCLOEn	PCLBUZn pin output enable/disable specification
0	Output disable (default)
1	Output enable

CSELn	CCSn2	CCSn1	CCSn0		PCLBUZn pin output clock selection		
					f_{MAIN} = 5 MHz	f_{MAIN} = 10 MHz	f_{MAIN} = 20 MHz
0	0	0	0	f_{MAIN}	5 MHz	10 MHz[Note]	Setting prohibited[Note]
0	0	0	1	$f_{MAIN}/2$	2.5 MHz	5 MHz	10 MHz[Note]
0	0	1	0	$f_{MAIN}/2^2$	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{MAIN}/2^3$	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{MAIN}/2^4$	312.5 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{MAIN}/2^{11}$	2.44 kHz	4.88 kHz	9.76 kHz
0	1	1	0	$f_{MAIN}/2^{12}$	1.22 kHz	2.44 kHz	4.88 kHz
0	1	1	1	$f_{MAIN}/2^{13}$	610 Hz	1.22 kHz	2.44 kHz
1	0	0	0	f_{SUB}	32.768 kHz		
1	0	0	1	$f_{SUB}/2$	16.384 kHz		
1	0	1	0	$f_{SUB}/2^2$	8.192 kHz		
1	0	1	1	$f_{SUB}/2^3$	4.096 kHz		
1	1	0	0	$f_{SUB}/2^4$	2.048 kHz		
1	1	0	1	$f_{SUB}/2^5$	1.024 kHz		
1	1	1	0	$f_{SUB}/2^6$	512 Hz		
1	1	1	1	$f_{SUB}/2^7$	256 Hz		

Note Use the output clock within a range of 10 MHz. Furthermore, when using the output clock at V_{DD} < 2.7 V, use it within 5 MHz.

Cautions 1. Change the output clock after disabling clock output (PCLOEn = 0).

2. To shift to STOP mode when the main system clock is selected (CSELn = 0), set PCLOEn = 0 before executing the STOP instruction. When the subsystem clock is selected (CSELn = 1), PCLOEn = 1 can be set because the clock can be output in STOP mode.

Remarks 1. n = 0: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
n = 0, 1: 78K0R/KE3-L, 78K0R/KF3-L, 78K0R/KG3-L

2. f_{MAIN}: Main system clock frequency

3. f_{SUB}: Subsystem clock frequency

(2) Port mode registers 5, 14 (PM5, PM14) Note

These registers set input/output of ports 5 and 14 in 1-bit units.

When using the ports to be shared with the PCLBUZ0 and PCLBUZ1 pins for clock output and buzzer output, set the port mode register (PMxx) bit and port register (Pxx) bit corresponding to each port to 0.

Example: When using P140/INTP6/PCLBUZ0 for clock output and buzzer output
Set the PM140 bit of port mode register 14 to 0.
Set the P140 bit of port register 14 to 0.

The PM5 and PM14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH (the PM14 register of the 78K0R/KE3-L is set to FEH).

Note The port mode register and port register to be set differ depending on the product.
78K0R/KC3-L (48-pin), 78K0R/KD3-L: P14
78K0R/KE3-L, 78K0R/KG3-L: PM14, P14
78K0R/KF3-L: PM5, P5, PM14, P14

Figure 11-3. Format of Port Mode Registers 5, 14 (PM5, PM14) (78K0R/KF3-L)

Address: FFF25H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM5	1	1	PM55	PM54	PM53	PM52	PM51	PM50

Address: FFF2EH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM14	1	1	1	PM144	PM143	PM142	1	PM140

PMmn	Pmn pin I/O mode selection (mn = 50 to 55, 140, 142 to 144)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remarks 1. The figure shown above presents the format of port mode registers 5 and 14 of the 78K0R/KF3-L product. See below for the format of the port mode registers of other products.
78K0R/KE3-L: **5.3 (1) Port mode registers (PMxx)**.
78K0R/KF3-L, 78K0R/KG3-L: **6.3 (1) Port mode registers (PMxx)**.

2. There are no port mode registers in the 48-pin product of the 78K0R/KC3-L or in the 78K0R/KD3-L.

11.4 Operations of Clock Output/Buzzer Output Controller

One pin can be used to output a clock or buzzer sound.

The PCLBUZ0 pin outputs a clock/buzzer selected by the clock output select register 0 (CKS0).

The PCLBUZ1 pin outputs a clock/buzzer selected by the clock output select register 1 (CKS1).

11.4.1 Operation as output pin

The PCLBUZn pin is output as the following procedure.

<1> Select the output frequency with bits 0 to 3 (CCSn0 to CCSn2, CSELn) of the clock output select register (CKSn) of the PCLBUZn pin (output in disabled status).

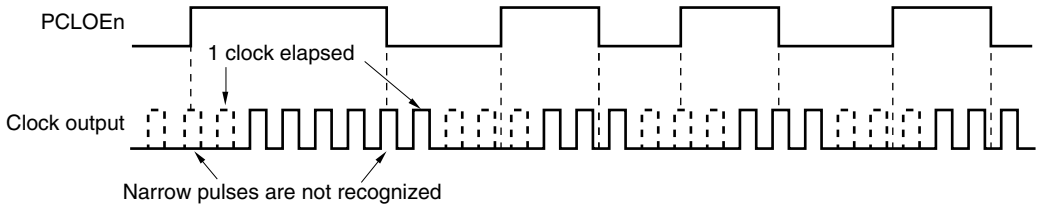
<2> Set bit 7 (PCLOEn) of the CKSn register to 1 to enable clock/buzzer output.

Remarks 1. The controller used for outputting the clock starts or stops outputting the clock one clock after enabling or disabling clock output (PCLOEn bit) is switched. At this time, pulses with a narrow width are not output. Figure 11-4 shows enabling or stopping output using the PCLOEn bit and the timing of outputting the clock.

2. n = 0: 78K0R/KC3-L (48-pin), 78K0R/KD3-L

n = 0, 1: 78K0R/KE3-L, 78K0R/KF3-L, 78K0R/KG3-L

Figure 11-4. Remote Control Output Application Example



CHAPTER 12 WATCHDOG TIMER

12.1 Functions of Watchdog Timer

The watchdog timer operates on the internal low-speed oscillation clock.

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Program loop is detected in the following cases.

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than “ACH” is written to the WDTE register
- If data is written to the WDTE register during a window close period

When a reset occurs due to the watchdog timer, bit 4 (WDRF) of the reset control flag register (RESF) is set to 1. For details of the RESF register, see **CHAPTER 21 RESET FUNCTION**.

When 75% of the overflow time is reached, an interval interrupt can be generated.

12.2 Configuration of Watchdog Timer

The watchdog timer includes the following hardware.

Table 12-1. Configuration of Watchdog Timer

Item	Configuration
Control register	Watchdog timer enable register (WDTE)

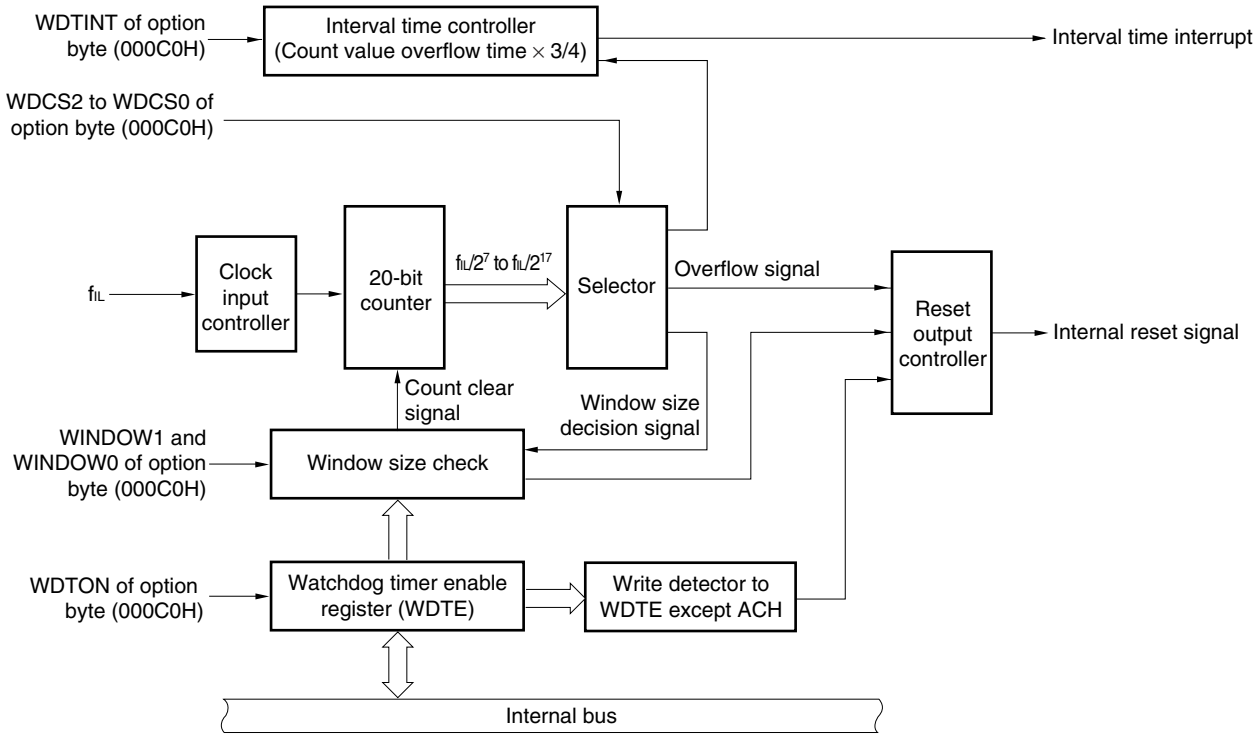
How the counter operation is controlled, overflow time, window open period, and interval interrupt are set by the option byte.

Table 12-2. Setting of Option Bytes and Watchdog Timer

Setting of Watchdog Timer	Option Byte (000C0H)
Watchdog timer interval interrupt	Bit 7 (WDTINT)
Window open period	Bits 6 and 5 (WINDOW1, WINDOW0)
Controlling counter operation of watchdog timer	Bit 4 (WDTON)
Overflow time of watchdog timer	Bits 3 to 1 (WDCS2 to WDCS0)
Controlling counter operation of watchdog timer (in HALT/STOP mode)	Bit 0 (WDSTBYON)

Remark For the option byte, see **CHAPTER 25 OPTION BYTE**.

Figure 12-1. Block Diagram of Watchdog Timer



12.3 Register Controlling Watchdog Timer

The watchdog timer is controlled by the watchdog timer enable register (WDTE).

(1) Watchdog timer enable register (WDTE)

Writing “ACH” to the WDTE register clears the watchdog timer counter and starts counting again.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 9AH or 1AH[Note].

Figure 12-2. Format of Watchdog Timer Enable Register (WDTE)

Address: FFFABH After reset: 9AH/1AH[Note] R/W

Symbol	7	6	5	4	3	2	1	0
WDTE								

Note The WDTE register reset value differs depending on the WDTON bit setting value of the option byte (000C0H). To operate watchdog timer, set the WDTON bit to 1.

WDTON Bit Setting Value	WDTE Register Reset Value
0 (watchdog timer count operation disabled)	1AH
1 (watchdog timer count operation enabled)	9AH

Cautions 1. If a value other than “ACH” is written to the WDTE register, an internal reset signal is generated.

2. If a 1-bit memory manipulation instruction is executed for the WDTE register, an internal reset signal is generated.

3. The value read from the WDTE register is 9AH/1AH (this differs from the written value (ACH)).

12.4 Operation of Watchdog Timer

12.4.1 Controlling operation of watchdog timer

1. When the watchdog timer is used, its operation is specified by the option byte (000C0H).

   - Enable counting operation of the watchdog timer by setting bit 4 (WDTON) of the option byte (000C0H) to 1 (the counter starts operating after a reset release) (for details, see **CHAPTER 25**).

WDTON	Watchdog Timer Counter
0	Counter operation disabled (counting stopped after reset)
1	Counter operation enabled (counting started after reset)

   - Set an overflow time by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H) (for details, see **12.4.2** and **CHAPTER 25**).
   - Set a window open period by using bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (000C0H) (for details, see **12.4.3** and **CHAPTER 25**).

2. After a reset release, the watchdog timer starts counting.
3. By writing “ACH” to the watchdog timer enable register (WDTE) after the watchdog timer starts counting and before the overflow time set by the option byte, the watchdog timer is cleared and starts counting again.
4. After that, write the WDTE register the second time or later after a reset release during the window open period. If the WDTE register is written during a window close period, an internal reset signal is generated.
5. If the overflow time expires without “ACH” written to the WDTE register, an internal reset signal is generated.
   An internal reset signal is generated in the following cases.

   - If a 1-bit manipulation instruction is executed on the WDTE register
   - If data other than “ACH” is written to the WDTE register

Cautions 1. When data is written to the watchdog timer enable register (WDTE) for the first time after reset release, the watchdog timer is cleared in any timing regardless of the window open time, as long as the register is written before the overflow time, and the watchdog timer starts counting again.

2. If the watchdog timer is cleared by writing “ACH” to the WDTE register, the actual overflow time may be different from the overflow time set by the option byte by up to 2/f_{IL} seconds.

3. The watchdog timer can be cleared immediately before the count value overflows.

Cautions 4. The operation of the watchdog timer in the HALT and STOP modes differs as follows depending on the set value of bit 0 (WDSTBYON) of the option byte (000C0H).

	WDSTBYON = 0	WDSTBYON = 1
In HALT mode	Watchdog timer operation stops.	Watchdog timer operation continues.
In STOP mode		

If WDSTBYON = 0, the watchdog timer resumes counting after the HALT or STOP mode is released. At this time, the counter is cleared to 0 and counting starts.
When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.
Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.
Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

5. The watchdog timer continues its operation during self-programming of the flash memory and EEPROM™ emulation. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

12.4.2 Setting overflow time of watchdog timer

Set the overflow time of the watchdog timer by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H).

If an overflow occurs, an internal reset signal is generated. The present count is cleared and the watchdog timer starts counting again by writing “ACH” to the watchdog timer enable register (WDTE) during the window open period before the overflow time.

The following overflow times can be set.

Table 12-3. Setting of Overflow Time of Watchdog Timer

WDCS2	WDCS1	WDCS0	Overflow Time of Watchdog Timer (f_{IL} = 34.5 kHz (MAX.))
0	0	0	$2^7/f_{IL}$ (3.71 ms)
0	0	1	$2^8/f_{IL}$ (7.42 ms)
0	1	0	$2^9/f_{IL}$ (14.84 ms)
0	1	1	$2^{10}/f_{IL}$ (29.68 ms)
1	0	0	$2^{12}/f_{IL}$ (118.72 ms)
1	0	1	$2^{14}/f_{IL}$ (474.90 ms)
1	1	0	$2^{15}/f_{IL}$ (949.80 ms)
1	1	1	$2^{17}/f_{IL}$ (3799.19 ms)

Caution The watchdog timer continues its operation during self-programming of the flash memory and EEPROM emulation. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

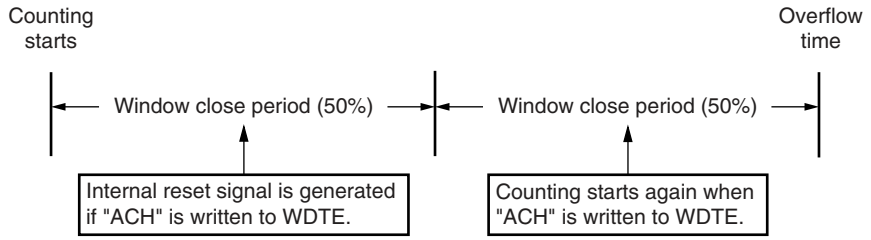
Remark f_{IL}: Internal low-speed oscillation clock frequency

12.4.3 Setting window open period of watchdog timer

Set the window open period of the watchdog timer by using bits 6 and 5 (WINDOW1, WINDOW0) of the option byte (000C0H). The outline of the window is as follows.

- If “ACH” is written to the watchdog timer enable register (WDTE) during the window open period, the watchdog timer is cleared and starts counting again.
- Even if “ACH” is written to the WDTE register during the window close period, an abnormality is detected and an internal reset signal is generated.

Example: If the window open period is 50%



Caution When data is written to the WDTE register for the first time after reset release, the watchdog timer is cleared in any timing regardless of the window open time, as long as the register is written before the overflow time, and the watchdog timer starts counting again.

The window open period can be set is as follows.

Table 12-4. Setting Window Open Period of Watchdog Timer

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	0	Setting prohibited
0	1	50%
1	0	75%
1	1	100%

Cautions 1. The watchdog timer continues its operation during self-programming of the flash memory and EEPROM emulation. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

2. When bit 0 (WDSTBYON) of the option byte (000C0H) = 0, the window open period is 100% regardless of the values of the WINDOW1 and WINDOW0 bits.

Remark If the overflow time is set to $2^{10}/f_{IL}$, the window close time and open time are as follows.

	Setting of Window Open Period		
	50%	75%	100%
Window close time	0 to 20.08 ms	0 to 10.04 ms	None
Window open time	20.08 to 29.68 ms	10.04 to 29.68 ms	0 to 29.68 ms

<When window open period is 50%>

- Overflow time:
  $2^{10}/f_{IL}$ (MAX.) = 2^{10}/34.5 kHz (MAX.) = 29.68 ms
- Window close time:
  0 to $2^{10}/f_{IL}$ (MIN.) × (1 − 0.5) = 0 to 2^{10}/25.5 kHz (MIN.) × 0.5 = 0 to 20.08 ms
- Window open time:
  $2^{10}/f_{IL}$ (MIN.) × (1 − 0.5) to $2^{10}/f_{IL}$ (MAX.) = 2^{10}/25.5 kHz (MIN.) × 0.5 to 2^{10}/34.5 kHz (MAX.) = 20.08 to 29.68 ms

12.4.4 Setting watchdog timer interval interrupt

Depending on the setting of bit 7 (WDTINT) of an option byte (000C0H), an interval interrupt (INTWDTI) can be generated when 75% of the overflow time is reached.

Table 12-5. Setting of Watchdog Timer Interval Interrupt

WDTINT	Use of Watchdog Timer Interval Interrupt
0	Interval interrupt is used.
1	Interval interrupt is generated when 75% of overflow time is reached.

Caution When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.
Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.
Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

Remark The watchdog timer continues counting even after INTWDTI is generated (until ACH is written to the watchdog timer enable register (WDTE)). If ACH is not written to the WDTE register before the overflow time, an internal reset signal is generated.

CHAPTER 13 A/D CONVERTER

The number of analog input channels of the A/D converter differs, depending on the product.

	78K0R/KC3-L (40-pin)	78K0R/KC3-L (44-pin)	78K0R/KC3-L (48-pin)	78K0R/KD3-L	78K0R/KE3-L	78K0R/KF3-L	78K0R/KG3-L
Analog input channels	10 ch (ANI0 to ANI9)	10 ch (ANI0 to ANI9)	11 ch (ANI0 to ANI10)	11 ch (ANI0 to ANI10)	12 ch (ANI0 to ANI11)	12 ch (ANI0 to ANI11)	16 ch (ANI0 to ANI15)

13.1 Function of A/D Converter

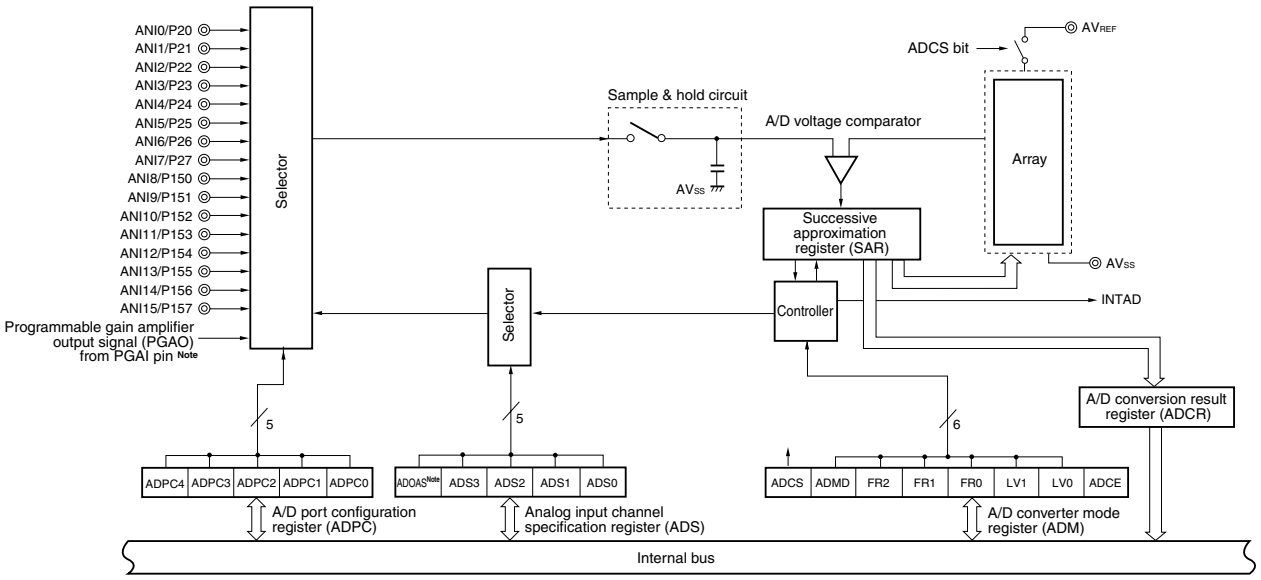
The A/D converter is a 10-bit resolution converter that converts analog input signals into digital values, and is configured to control analog inputs, including up to sixteen channels of A/D converter analog inputs (ANI0 to ANI15) and a programmable gain amplifier output (PGAO) Note.

The A/D converter has the following function.

- **10-bit resolution A/D conversion**

  10-bit resolution A/D conversion is carried out repeatedly for one analog input channel selected from ANI0 to ANI15. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated.

Figure 13-1. Block Diagram of A/D Converter



Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only.

Remark ANI0 to ANI9: 78K0R/KC3-L (40-pin, 44-pin)
ANI0 to ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
ANI0 to ANI11: 78K0R/KE3-L, 78K0R/KF3-L
ANI0 to ANI15: 78K0R/KG3-L

13.2 Configuration of A/D Converter

The A/D converter includes the following hardware.

(1) ANI0 to ANI15 pins

These are the analog input pins of the sixteen channels of the A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

Remark ANI0 to ANI9: 78K0R/KC3-L (40-pin, 44-pin)
ANI0 to ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
ANI0 to ANI11: 78K0R/KE3-L, 78K0R/KF3-L
ANI0 to ANI15: 78K0R/KG3-L

(2) PGAO (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only)

This is the programmable gain amplifier output signal from the PGAI pin. The A/D converter can perform A/D conversion by selecting the output signal of the programmable gain amplifier as the analog input.

(3) Sample & hold circuit

The sample & hold circuit samples each of the analog input voltages sequentially sent from the input circuit, and sends them to the A/D voltage comparator. This circuit also holds the sampled analog input voltage during A/D conversion.

(4) A/D voltage comparator

This A/D voltage comparator compares the voltage generated from the voltage tap of the array with the analog input voltage. If the analog input voltage is found to be greater than the reference voltage (1/2 AV_{REF}) as a result of the comparison, the most significant bit (MSB) of the successive approximation register (SAR) is set. If the analog input voltage is less than the reference voltage (1/2 AV_{REF}), the MSB bit of the SAR is reset.
After that, bit 10 of the SAR register is automatically set, and the next comparison is made. The voltage tap of the array is selected by the value of bit 11, to which the result has been already set.

Bit 11 = 0: (1/4 AV_{REF})
Bit 11 = 1: (3/4 AV_{REF})

The voltage tap of the array and the analog input voltage are compared and bit 10 of the SAR register is manipulated according to the result of the comparison.

Analog input voltage ≥ Voltage tap of array: Bit 10 = 1
Analog input voltage ≤ Voltage tap of array: Bit 10 = 0

Comparison is continued like this to bit 0 of the SAR register.

(5) Array

The array generates the comparison voltage input from an analog input pin.

(6) Successive approximation register (SAR)

The SAR register is a 12-bit register that sets voltage tap data whose values from the array match the voltage values of the analog input pins, 1 bit at a time starting from the most significant bit (MSB).

If data is set in the SAR register all the way to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register (conversion results) are held in the A/D conversion result register (ADCR). When all the specified A/D conversion operations have ended, an A/D conversion end interrupt request signal (INTAD) is generated.

(7) 10-bit A/D conversion result register (ADCR)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the A/D conversion result in its higher 10 bits (the lower 6 bits are fixed to 0).

(8) 8-bit A/D conversion result register (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

(9) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD.

(10) AV_{REF} pin

This pin inputs the reference voltage of the A/D converter, the programmable gain amplifier, the power supply pins and A/D converter of the comparator, and the comparator. When all pins of ports 2, 15, and 8 are used as the analog port pins, make the potential of AV_{REF} be such that $1.8\ V \leq AV_{REF} \leq V_{DD}$. When one or more of the pins of ports 2, 15, and 8 are used as the digital port pins, make AV_{REF} the same potential as V_{DD}.

The analog signal input to the ANI0 to ANI15 pins is converted into a digital signal, based on the voltage applied across AV_{REF} and AV_{SS}.

(11) AV_{SS} pin

This is the ground potential pin of the A/D converter. Always use this pin at the same potential as that of the V_{SS} pin even when the A/D converter is not used.

Remark ANI0 to ANI9: 78K0R/KC3-L (40-pin, 44-pin)
ANI0 to ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
ANI0 to ANI11: 78K0R/KE3-L, 78K0R/KF3-L
ANI0 to ANI15: 78K0R/KG3-L

13.3 Registers Used in A/D Converter

The A/D converter uses the following seven registers.

- Peripheral enable register 0 (PER0)
- A/D converter mode register (ADM)
- A/D port configuration register (ADPC)
- Analog input channel specification register (ADS)
- Port mode registers 2, 15, 8 Note (PM2, PM15, PM8 Note)
- 10-bit A/D conversion result register (ADCR)
- 8-bit A/D conversion result register (ADCRH)

Note Port mode register 8 is set only in the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L.

(1) Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the A/D converter is used, be sure to set bit 5 (ADCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 13-2. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN Note 1	0	ADCEN	IICAEN Note 2	SAU1EN Note 3	SAU0EN	TAU1EN Note 3	TAU0EN Note 3

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFR used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFR used by the A/D converter can be read/written.

Notes 1. That is not provided in 40-pin product of the 78K0R/KC3-L.

2. That is not provided in 40-pin and 44-pin products of the 78K0R/KC3-L.

3. 78K0R/KF3-L and 78K0R/KG3-L only.

Cautions 1. When setting the A/D converter, be sure to set the ADCEN bit to 1 first. If ADCEN = 0, writing to a control register of the A/D converter is ignored, and, even if the register is read, only the default value is read (except for port mode registers 2, 15, and 8 (PM2, PM15, and PM8)).

2. Be sure to clear the following bits to 0.

48-pin product of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: bits 0, 1, 3, 6

44-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6

40-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6, 7

78K0R/KF3-L, 78K0R/KG3-L: bit 6

(2) A/D converter mode register (ADM)

This register sets the conversion time for analog input to be A/D converted, and starts/stops conversion.

The ADM register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 13-3. Format of A/D Converter Mode Register (ADM)

Address: FFF30H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
ADM	ADCS	ADMD	FR2 Note 1	FR1 Note 1	FR0 Note 1	LV1 Note 1	LV0 Note 1	ADCE

ADCS	A/D conversion operation control
0	Stops conversion operation
1	Enables conversion operation

ADMD	A/D conversion operation mode specification
0	Select mode
1	Scan mode

ADCE	A/D voltage comparator operation control Note 2
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

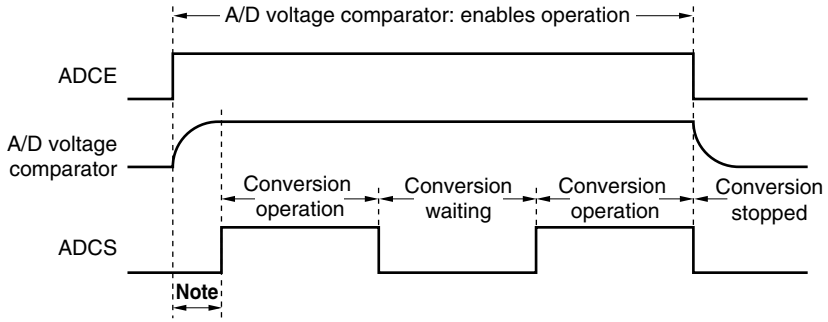
Notes 1. For details of the FR2 to FR0, LV1, LV0 bits, and A/D conversion, see **Table 13-2 A/D Conversion Time Selection**.

2. The operation of the A/D voltage comparator is controlled by the ADCS and ADCE bits, and it takes 1 μs from operation start to operation stabilization. Therefore, when the ADCS bit is set to 1 after 1 μs or more has elapsed from the time ADCE bit is set to 1, the conversion result at that time has priority over the first conversion result. Otherwise, ignore data of the first conversion.

Table 13-1. Settings of ADCS and ADCE bits

ADCS	ADCE	A/D Conversion Operation
0	0	Stop status (DC power consumption path does not exist)
0	1	Conversion waiting mode (only A/D voltage comparator consumes power))
1	0	Setting prohibited
1	1	Conversion mode (A/D voltage comparator: enables operation)

Figure 13-4. Timing Chart When A/D Voltage Comparator Is Used



Note To stabilize the internal circuit, the time from the rising of the ADCE bit to the falling of the ADCS bit must be 1 μs or longer.

Caution A/D conversion must be stopped before rewriting bits the FR0 to FR2, LV1, and LV0 bits to values other than the identical data.

<R>

Table 13-2. A/D Conversion Time Selection (1/3)

(1) 4.0 V ≤ AV_{REF} ≤ 5.5 V

A/D Converter Mode Register (ADM)					Mode	Conversion Time Selection					Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0			f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	
0	0	0	0	0	Normal	342/f_{CLK}	Setting prohibited	Setting prohibited	34.2 μs	17.1 μs	f_{CLK}/20
0	0	1				172/f_{CLK}		34.4 μs	17.2 μs	8.6 μs	f_{CLK}/10
0	1	0				138/f_{CLK}		27.6 μs	13.8 μs	6.9 μs	f_{CLK}/8
0	1	1				104/f_{CLK}	52.0 μs	20.8 μs	10.4 μs	5.2 μs	f_{CLK}/6
1	0	0				70/f_{CLK}	35.0 μs	14.0 μs	7.0 μs	Setting prohibited	f_{CLK}/4
1	0	1				53/f_{CLK}	26.5 μs	10.6 μs	5.3 μs		f_{CLK}/3
1	1	0				36/f_{CLK}	18.0 μs	7.2 μs	Setting prohibited		f_{CLK}/2
1	1	1				19/f_{CLK}	9.5 μs	Setting prohibited			f_{CLK}
×	×	×	0	1	Low-voltage	Setting prohibited					–
0	0	0	1	0	High speed 1	322/f_{CLK}	Setting prohibited	64.4 μs	32.2 μs	16.1 μs	f_{CLK}/20
0	0	1				162/f_{CLK}		32.4 μs	16.2 μs	8.1 μs	f_{CLK}/10
0	1	0				130/f_{CLK}	65.0 μs	26.0 μs	13.0 μs	6.5 μs	f_{CLK}/8
0	1	1				98/f_{CLK}	49.0 μs	19.6 μs	9.8 μs	4.9 μs	f_{CLK}/6
1	0	0				66/f_{CLK}	33.0 μs	13.2 μs	6.6 μs	3.3 μs	f_{CLK}/4
1	0	1				50/f_{CLK}	25.0 μs	10.0 μs	5.0 μs	2.5 μs	f_{CLK}/3
1	1	0				34/f_{CLK}	17.0 μs	6.8 μs	3.4 μs	Setting prohibited	f_{CLK}/2
1	1	1				18/f_{CLK}	9.0 μs	3.6 μs	Setting prohibited		f_{CLK}
0	0	0	1	1	High speed 2	342/f_{CLK}	Setting prohibited	Setting prohibited	34.2 μs	17.1 μs	f_{CLK}/20
0	0	1				172/f_{CLK}		34.4 μs	17.2 μs	8.6 μs	f_{CLK}/10
0	1	0				138/f_{CLK}		27.6 μs	13.8 μs	6.9 μs	f_{CLK}/8
0	1	1				104/f_{CLK}	52.0 μs	20.8 μs	10.4 μs	5.2 μs	f_{CLK}/6
1	0	0				70/f_{CLK}	35.0 μs	14.0 μs	7.0 μs	3.5 μs	f_{CLK}/4
1	0	1				53/f_{CLK}	26.5 μs	10.6 μs	5.3 μs	Setting prohibited	f_{CLK}/3
1	1	0				36/f_{CLK}	18.0 μs	7.2 μs	3.6 μs		f_{CLK}/2
1	1	1				19/f_{CLK}	9.5 μs	3.8 μs	Setting prohibited		f_{CLK}

Cautions 1. When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, stop A/D conversion once (ADCS = 0) beforehand.

2. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

<R>

Table 13-2. A/D Conversion Time Selection (2/3)

(2) 2.7 V ≤ AV_{REF} ≤ 5.5 V

A/D Converter Mode Register (ADM)					Mode	Conversion Time Selection					Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0			f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	
0	0	0	0	0	Normal	342/f_{CLK}	Setting prohibited	Setting prohibited	34.2 μs	17.1 μs	f_{CLK}/20
0	0	1				172/f_{CLK}		34.4 μs	17.2 μs	8.6 μs	f_{CLK}/10
0	1	0				138/f_{CLK}		27.6 μs	13.8 μs	Setting prohibited	f_{CLK}/8
0	1	1				104/f_{CLK}	52.0 μs	20.8 μs	10.4 μs		f_{CLK}/6
1	0	0				70/f_{CLK}	35.0 μs	14.0 μs	Setting prohibited		f_{CLK}/4
1	0	1				53/f_{CLK}	26.5 μs	10.6 μs			f_{CLK}/3
1	1	0				36/f_{CLK}	18.0 μs	Setting prohibited			f_{CLK}/2
1	1	1				19/f_{CLK}	9.5 μs				f_{CLK}
×	×	×	0	1	Low-voltage	Setting prohibited					–
×	×	×	1	0	High speed 1	Setting prohibited					–
0	0	0	1	1	High speed 2	342/f_{CLK}	Setting prohibited	Setting prohibited	34.2 μs	17.1 μs	f_{CLK}/20
0	0	1				172/f_{CLK}		34.4 μs	17.2 μs	8.6 μs	f_{CLK}/10
0	1	0				138/f_{CLK}		27.6 μs	13.8 μs	6.9 μs	f_{CLK}/8
0	1	1				104/f_{CLK}	52.0 μs	20.8 μs	10.4 μs	5.2 μs	f_{CLK}/6
1	0	0				70/f_{CLK}	35.0 μs	14.0 μs	7.0 μs	3.5 μs	f_{CLK}/4
1	0	1				53/f_{CLK}	26.5 μs	10.6 μs	5.3 μs	Setting prohibited	f_{CLK}/3
1	1	0				36/f_{CLK}	18.0 μs	7.2 μs	3.6 μs		f_{CLK}/2
1	1	1				19/f_{CLK}	9.5 μs	3.8 μs	Setting prohibited		f_{CLK}

Cautions 1. When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, stop A/D conversion once (ADCS = 0) beforehand.

2. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

<R>

Table 13-2. A/D Conversion Time Selection (3/3)

(3) 1.8 V ≤ AV_{REF} ≤ 4.0 V

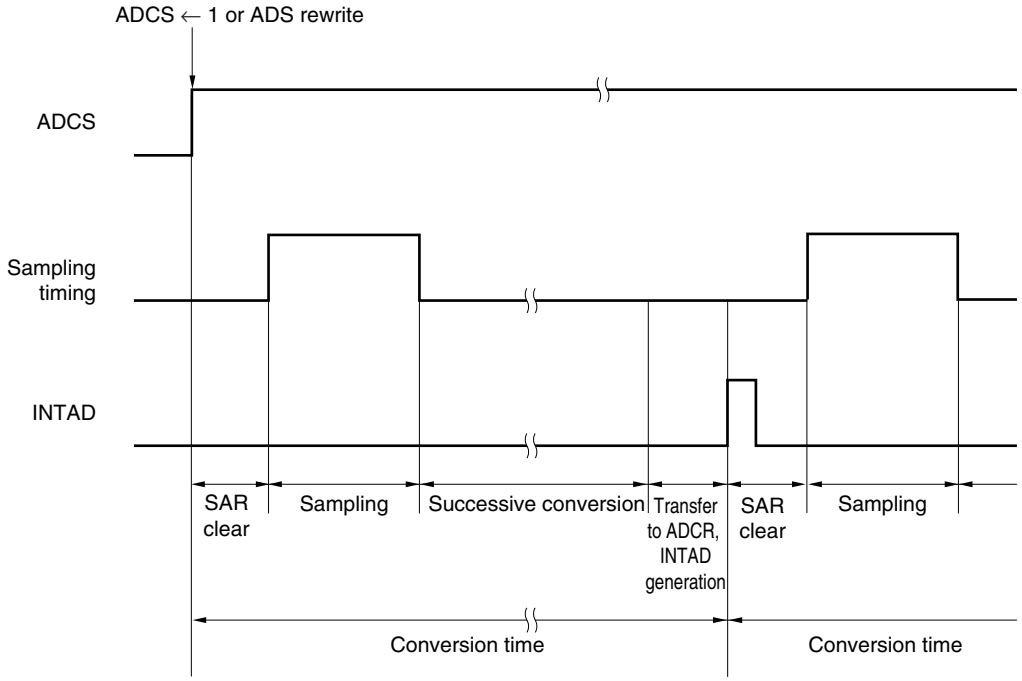
A/D Converter Mode Register (ADM)					Mode	Conversion Time Selection				Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0			f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	
×	×	×	0	0	Normal	Setting prohibited					
0	0	0	0	1	Low-voltage	482/f_{CLK}	Setting prohibited	Setting prohibited	48.2 μs	24.1 μs	f_{CLK}/20
0	0	1				242/f_{CLK}		48.4 μs	24.2 μs	Setting prohibited	f_{CLK}/10
0	1	0				194/f_{CLK}		38.8 μs	Setting prohibited		f_{CLK}/8
0	1	1				146/f_{CLK}		29.2 μs			f_{CLK}/6
1	0	0				98/f_{CLK}	49.0 μs	Setting prohibited			f_{CLK}/4
1	0	1				74/f_{CLK}	37.0 μs				f_{CLK}/3
1	1	0				50/f_{CLK}	25.0 μs				f_{CLK}/2
1	1	1				26/f_{CLK}	Setting prohibited				f_{CLK}
×	×	×	1	0	High speed 1	Setting prohibited					–
×	×	×	1	1	High speed 2	Setting prohibited					–
Other than above					Setting prohibited						

Cautions 1. When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, stop A/D conversion once (ADCS = 0) beforehand.

2. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

Figure 13-5. A/D Converter Sampling and A/D Conversion Timing



(3) 10-bit A/D conversion result register (ADCR)

This register is a 16-bit register that stores the A/D conversion result in the select mode. The lower 6 bits are fixed to 0. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register (SAR). The higher 8 bits of the conversion result are stored in FFF1FH and the lower 2 bits are stored in the higher 2 bits of FFF1EH.

The ADCR register can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 13-6. Format of 10-bit A/D Conversion Result Register (ADCR)

Address: FFF1FH, FFF1EH After reset: 0000H R

Symbol	FFF1FH								FFF1EH							
ADCR											0	0	0	0	0	0

Caution When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of the ADCR register may become undefined. Read the conversion result following conversion completion before writing to the ADM, ADS, and ADPC registers. Using timing other than the above may cause an incorrect conversion result to be read.

(4) 8-bit A/D conversion result register (ADCRH)

This register is an 8-bit register that stores the A/D conversion result. The higher 8 bits of 10-bit resolution are stored.

The ADCRH register can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 13-7. Format of 8-bit A/D Conversion Result Register (ADCRH)

Address: FFF1FH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ADCRH								

Caution When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of the ADCRH register may become undefined. Read the conversion result following conversion completion before writing to the ADM, ADS, and ADPC registers. Using timing other than the above may cause an incorrect conversion result to be read.

(5) Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

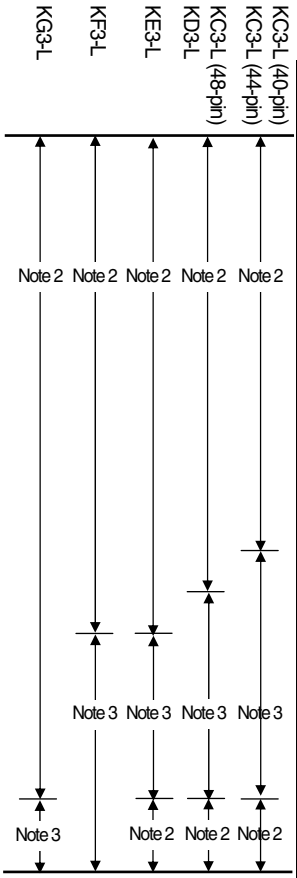
The ADS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 13-8. Format of Analog Input Channel Specification Register (ADS) (1/2)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	ADOAS Note 1	0	0	ADS3	ADS2	ADS1	ADS0



○ Select mode (ADMD = 0)

ADOAS Note 1	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	ANI0	P20/ANI0 pin
0	0	0	0	1	ANI1	P21/ANI1 pin
0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	1	0	1	ANI5	P25/ANI5 pin
0	0	1	1	0	ANI6	P26/ANI6 pin
0	0	1	1	1	ANI7	P27/ANI7 pin
0	1	0	0	0	ANI8	P150/ANI8 pin
0	1	0	0	1	ANI9	P151/ANI9 pin
0	1	0	1	0	ANI10	P152/ANI10 pin
0	1	0	1	1	ANI11	P153/ANI11 pin
0	1	1	0	0	ANI12	P154/ANI12 pin
0	1	1	0	1	ANI13	P155/ANI13 pin
0	1	1	1	0	ANI14	P156/ANI14 pin
0	1	1	1	1	ANI15	P157/ANI15 pin
1	×	×	×	×	PGAO	Programmable gain amplifier output signal
Other than the above					Setting prohibited	

Notes 1. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only.

2. Setting permitted

3. Setting prohibited

(**Cautions** and **Remarks** are listed on the next page.)

Cautions 1. Be sure to clear the following bits to 0.
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: bits 4, 5, 7
78K0R/KF3-L, 78K0R/KG3-L: bits 4 to 7

2 Set a channel to be used for A/D conversion in the input mode by using port mode registers 2, 15, and 8 (PM2, PM15, PM8).

3. Do not set the pin that is set by the A/D port configuration register (ADPC) as digital I/O by the ADS register.

4. Select the output signal (PGAO) of the programmable gain amplifier from the PGAI pin as the analog input after setting the operation of the programmable gain amplifier (refer to 13.4.1 Basic operations of A/D converter).

Remarks 1. ×: don't care

2. P20/ANI0 to P27/ANI7, P150/ANI8, P151/ANI9: 78K0R/KC3-L (40-pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L, 78K0R/KF3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P157/ANI15: 78K0R/KG3-L

Figure 13-8. Format of Analog Input Channel Specification Register (ADS) (2/2)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	ADOAS Note 1	0	0	ADS3	ADS2	ADS1	ADS0

○ Scan mode (ADMD = 1)

KF3-L, KG3-L	KE3-L	KD3-L	KC3-L (48-pin)	KC3-L (44-pin)	KC3-L (40-pin)	ADOAS Note 1	ADS3	ADS2	ADS1	ADS0	Analog input channel			
											Scan 0	Scan 1	Scan 2	Scan 3
Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	0	0	0	0	0	ANI0	ANI1	ANI2	ANI3
						0	0	0	0	1	ANI1	ANI2	ANI3	ANI4
						0	0	0	1	0	ANI2	ANI3	ANI4	ANI5
						0	0	0	1	1	ANI3	ANI4	ANI5	ANI6
						0	0	1	0	0	ANI4	ANI5	ANI6	ANI7
						0	0	1	0	1	ANI5	ANI6	ANI7	ANI8
						0	0	1	1	0	ANI6	ANI7	ANI8	ANI9
					Note 3	0	0	1	1	1	ANI7	ANI8	ANI9	ANI10
						1	0	0	0	0	PGAO	ANI0	ANI1	ANI2
						1	0	0	0	1	PGAO	ANI1	ANI2	ANI3
						1	0	0	1	0	PGAO	ANI2	ANI3	ANI4
Note 3					Note 2	1	0	0	1	1	PGAO	ANI3	ANI4	ANI5
						1	0	1	0	0	PGAO	ANI4	ANI5	ANI6
						1	0	1	0	1	PGAO	ANI5	ANI6	ANI7
						1	0	1	1	0	PGAO	ANI6	ANI7	ANI8
						1	0	1	1	1	PGAO	ANI7	ANI8	ANI9
						Other than the above					Setting prohibited			

Notes 1. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only.

2. Setting permitted

3. Setting prohibited

Cautions 1. Be sure to clear the following bits to 0.

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: bits 4, 5, 7

78K0R/KF3-L, 78K0R/KG3-L: bits 4 to 7

2 Set a channel to be used for A/D conversion in the input mode by using port mode registers 2, 15, and 8 (PM2, PM15, PM8).

3. Do not set the pin that is set by the A/D port configuration register (ADPC) as digital I/O by the ADS register.

4. Select the output signal (PGAO) of the programmable gain amplifier from the PGAI pin as the analog input after setting the operation of the programmable gain amplifier (refer to 13.4.1 Basic operations of A/D converter).

Remarks 1. ×: don't care

2. P20/ANI0 to P27/ANI7, P150/ANI8, P151/ANI9: 78K0R/KC3-L (40-pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L, 78K0R/KF3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P157/ANI15: 78K0R/KG3-L

(6) A/D port configuration register (ADPC)

This register switches the ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI15/P157 pins to analog input of A/D converter or digital I/O of port.

The ADPC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 13-9. Format of A/D Port Configuration Register (ADPC)

Address: F0017H After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	Analog Input (A)/digital I/O (D) switching															
					Port 15								Port 2							
					ANI15/P157	ANI14/P156	ANI13/P155	ANI12/P154	ANI11/P153	ANI10/P152	ANI9/P151	ANI8/P150	ANI7/P27	ANI6/P26	ANI5/P25	ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	D
0	0	0	1	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	D	D
0	0	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D
0	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D
0	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D
0	0	1	1	0	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D
0	0	1	1	1	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D
0	1	0	0	0	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D
0	1	0	0	1	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	D
0	1	0	1	0	A	A	A	A	A	A	D	D	D	D	D	D	D	D	D	D
0	1	0	1	1	A	A	A	A	A	D	D	D	D	D	D	D	D	D	D	D
0	1	1	0	0	A	A	A	A	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	0	1	A	A	A	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	1	0	A	A	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	1	1	A	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
1	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Other than above					Setting prohibited															

Cautions 1. Set a channel to be used for A/D conversion in the input mode by using port mode register 2 and 15 (PM2, PM15).

2. Do not set the pin that is set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

3. Be sure to first set the ADCEN bit of peripheral enable register 0 (PER0) to 1 when setting up the ADPC register. If ADCEN = 0, writing to the ADPC register is ignored and specified values are returned to the initial values.

Remark P20/ANI0 to P27/ANI7, P150/ANI8, P151/ANI9: 78K0R/KC3-L (40-pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L, 78K0R/KF3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P157/ANI15: 78K0R/KG3-L

(7) Port input mode register 8 (PIM8) (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only)

This register enables or disables the digital input of port 8 in 1-bit units.

Disable the digital input (used as analog input) to use the PGAI pin as the analog input. Enable the digital input to use the port function, or the external interrupt and timer Hi-Z control functions, because the digital input is disabled (used as analog input) in the initial state.

The PIM8 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 13-10. Format of Port Input Mode Register 8 (PIM8)

Address: F0048H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM8	0	0	0	0	PIM83	PIM82 Note	PIM81	PIM80

PIM8n	Selection of enabling or disabling P8n pin digital input (n = 0 to 3)
0	Disables digital input (used as analog input)
1	Enables digital input

Note PIM82 bit is not provided in the 78K0R/KC3-L (40-pin).

(8) Port mode registers 2, 15, and 8 [Note] (PM2, PM15, PM8 [Note])

When using the ANI0/P20 to ANI7/P27, ANI8/P150 to ANI15/P157, and PGAI/P80 pins for analog input port, set the PM20 to PM27, PM150 to PM157, and PM80 bits to 1. The output latches of P20 to P27, P150 to P157, and P80 at this time may be 0 or 1.

If the PM20 to PM27, PM150 to PM157, and PM80 bits are set to 0, they cannot be used as analog input port pins.

The PM2, PM15, and PM8 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Note Port mode register 8 is set only in the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L.

Caution If a pin is set as an analog input port, not the pin level but "0" is always read.

Remark P20/ANI0 to P27/ANI7, P150/ANI8, P151/ANI9: 78K0R/KC3-L (40-pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L, 78K0R/KF3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P157/ANI15: 78K0R/KG3-L

Figure 13-11. Formats of Port Mode Registers 2, 15, and 8 (PM2, PM15, PM8) (78K0R/KE3-L)

Address: FFF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

Address: FFF28H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM8	1	1	1	1	PM83	PM82	PM81	PM80

Address: FFF2FH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM15	1	1	1	1	PM153	PM152	PM151	PM150

PMmn	Pmn pin I/O mode selection (mn = 20 to 27, 150 to 153, 80 to 83)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode registers 2, 8 and 15 of the 78K0R/KE3-L product. See below for the format of the port mode registers of other products.
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: **5.3 (1) Port mode registers (PMxx)**.
78K0R/KF3-L, 78K0R/KG3-L: **6.3 (1) Port mode registers (PMxx)**.

The ANI0/P20 to ANI7/P27, ANI8/P150 to ANI15/P157, and PGAI/P80 pins are as shown below depending on the settings of the A/D port configuration register (ADPC), analog input channel specification register (ADS), PM2, PM15, and PM8 registers.

Table 13-3. Setting Functions of ANI0/P20 to ANI7/P27, ANI8/P150 to ANI15/P157, and PGAI/P80 Pins

ADPC	PM2, PM15, and PM8	ADS	ANI0/P20 to ANI7/P27, ANI8/P150 to ANI15/P157, and PGAI/P80 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

Remark P20/ANI0 to P27/ANI7, P150/ANI8, P151/ANI9: 78K0R/KC3-L (40-pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L, 78K0R/KF3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P157/ANI15: 78K0R/KG3-L

13.4 A/D Converter Operations

13.4.1 Basic operations of A/D converter

<1> Set bit 5 (ADCEN) of peripheral enable register 0 (PER0) to 1 to start the supply of the input clock to the A/D converter.

<2> Set the A/D conversion time by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of the A/D converter mode register (ADM), and set the operation mode by using bit 6 (ADMD) of the ADM register.

<3> Set bit 0 (ADCE) of the ADM register to 1 to start the operation of the A/D voltage comparator.

<4> Set the channels for A/D conversion to analog input by using the A/D port configuration register (ADPC) and set to input mode by using the port mode registers (PM2, PM15, and PM8).

<5> Set the programmable gain amplifier operation to set the programmable gain amplifier output (PGAI pin) for the analog input channel (refer to **10.4.1 Starting comparator and programmable gain amplifier operation**).

<6> Select one channel for A/D conversion using the analog input channel specification register (ADS).

<7> Start the conversion operation by setting bit 7 (ADCS) of the ADM register to 1.
(<8> to <14> are operations performed by hardware.)

<8> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<9> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.

<10> Bit 9 of the successive approximation register (SAR) is set. The series resistor string voltage tap is set to (1/2) AV_{REF} by the tap selector.

<11> The voltage difference between the series resistor string voltage tap and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{REF}, the MSB bit of the SAR register remains set to 1. If the analog input is smaller than (1/2) AV_{REF}, the MSB bit is reset to 0.

<12> Next, bit 8 of the SAR register is automatically set to 1, and the operation proceeds to the next comparison. The series resistor string voltage tap is selected according to the preset value of bit 9, as described below.

- Bit 9 = 1: (3/4) AV_{REF}
- Bit 9 = 0: (1/4) AV_{REF}

The voltage tap and sampled voltage are compared and bit 8 of the SAR register is manipulated as follows.

- Sampled voltage ≥ Voltage tap: Bit 8 = 1
- Sampled voltage < Voltage tap: Bit 8 = 0

<13> Comparison is continued in this way up to bit 0 of the SAR register.

<14> Upon completion of the comparison of 10 bits, an effective digital result value remains in the SAR register, and the result value is transferred to the A/D conversion result register (ADCR, ADCRH) and then latched.
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated.

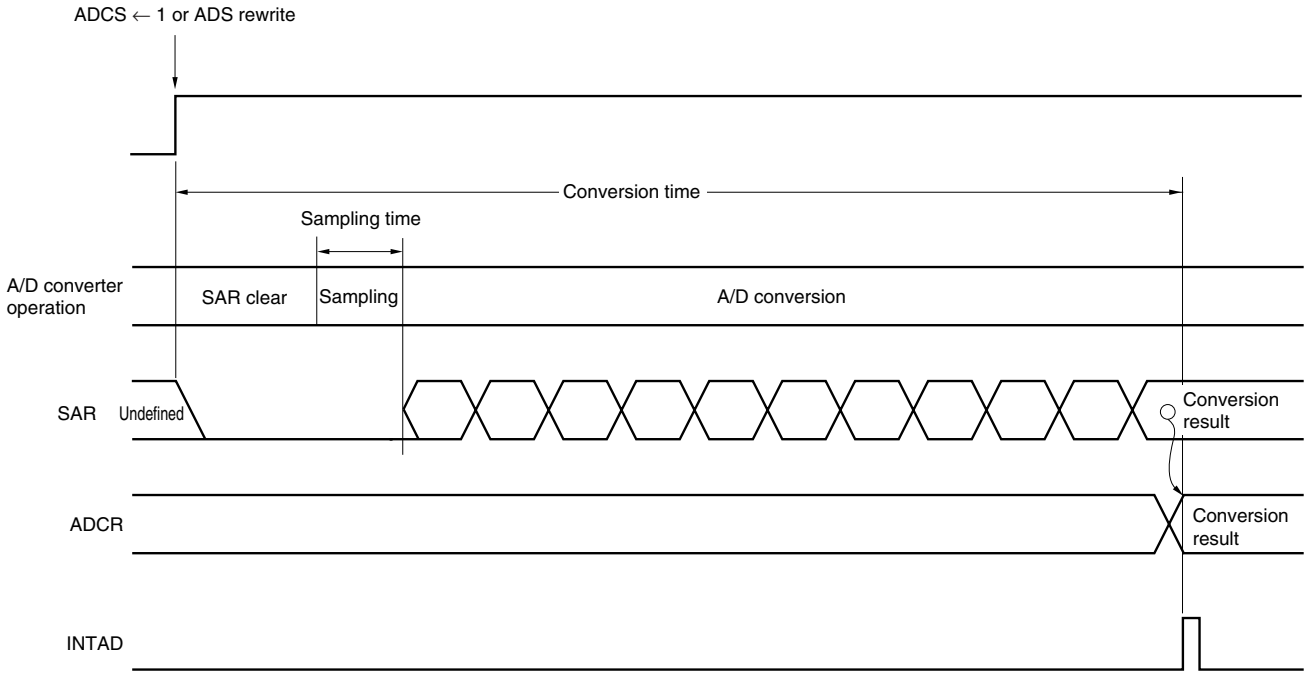
<15> Repeat steps <8> to <14>, until the ADCS bit is cleared to 0.
To stop the A/D converter, clear the ADCS bit to 0.
To restart A/D conversion from the status of ADCE = 1, start from <7>. To start A/D conversion again when ADCE = 0, set the ADCE bit to 1, wait for 1 μs or longer, and start <7>. To change a channel of A/D conversion, start from <6>.

Caution Make sure the period of <3> to <7> is 1 μs or more.

Remark Two types of the A/D conversion result registers are available.
- ADCR register (16 bits): Store 10-bit A/D conversion value
- ADCRH register (8 bits): Store 8-bit A/D conversion value

<R>

Figure 13-12. Basic Operation of A/D Converter



A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register (ADM) is reset (0) by software.

If a write operation is performed to the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH) to 0000H or 00H.

13.4.2 Input voltage and conversion results

The relationship between the analog input voltage input to the analog input pins (ANI0 to ANI15, PGAI) and the theoretical A/D conversion result (stored in the 10-bit A/D conversion result register (ADCR)) is shown by the following expression.

$$SAR = INT\left(\frac{V_{AIN}}{AV_{REF}} \times 1024 + 0.5\right)$$

$$ADCR = SAR \times 64$$

or

$$\left(\frac{ADCR}{64} - 0.5\right) \times \frac{AV_{REF}}{1024} \leq V_{AIN} < \left(\frac{ADCR}{64} + 0.5\right) \times \frac{AV_{REF}}{1024}$$

where, INT( ): Function which returns integer part of value in parentheses

V_{AIN}: Analog input voltage

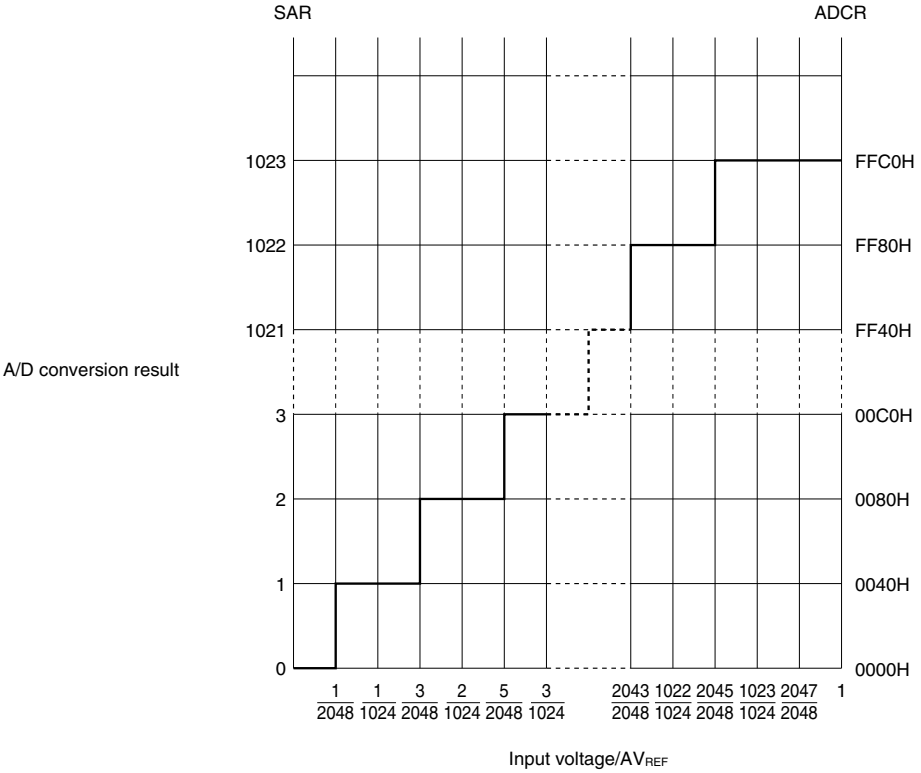
AV_{REF}: AV_{REF} pin voltage

ADCR: A/D conversion result register (ADCR) value

SAR: Successive approximation register

Figure 13-13 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 13-13. Relationship Between Analog Input Voltage and A/D Conversion Result



Remark ANI0 to ANI9: 78K0R/KC3-L (40-pin, 44-pin)
ANI0 to ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
ANI0 to ANI11: 78K0R/KE3-L, 78K0R/KF3-L
ANI0 to ANI15: 78K0R/KG3-L

13.4.3 A/D converter operation modes

The select mode and scan mode are provided as the A/D converter operation modes.

(1) Select mode

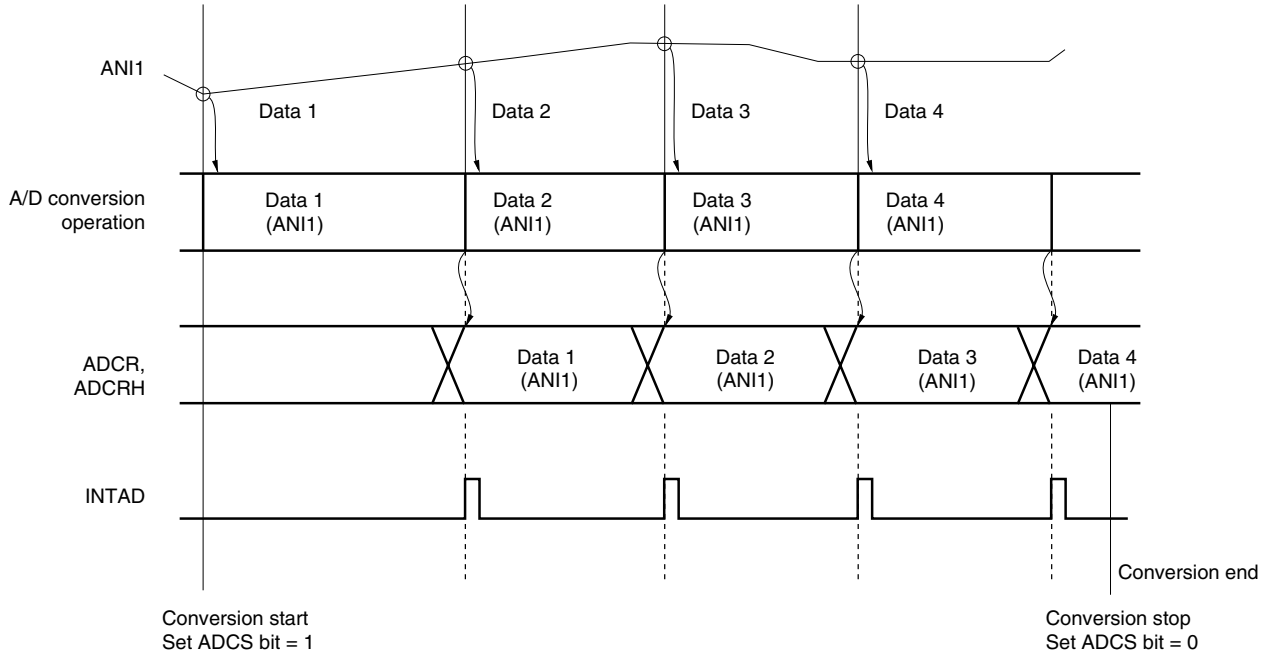
One analog input specified by the analog input channel specification register (ADS), while the ADMD bit of the A/D converter mode register (ADM) is 0, is A/D converted.

When A/D conversion is complete, the conversion result is stored in the A/D conversion result register (ADCR) and the A/D conversion end interrupt request signal (INTAD) is generated.

After A/D conversion has been completed, A/D conversion is repeated successively, unless the ADCS bit is set to 0.

If anything is written to the ADM or ADS register during conversion, A/D conversion is aborted. In this case, A/D conversion is started again from the beginning.

Figure 13-14. Example of Select Mode Operation Timing



(2) Scan mode

The four analog input channels of scans 0 to 3, which are specified by the analog input channel specification register (ADS), while the ADMD bit of the A/D converter mode register (ADM) is 1, are A/D converted successively. A/D conversion is performed in sequence, starting from the analog input channel specified by scan 0.

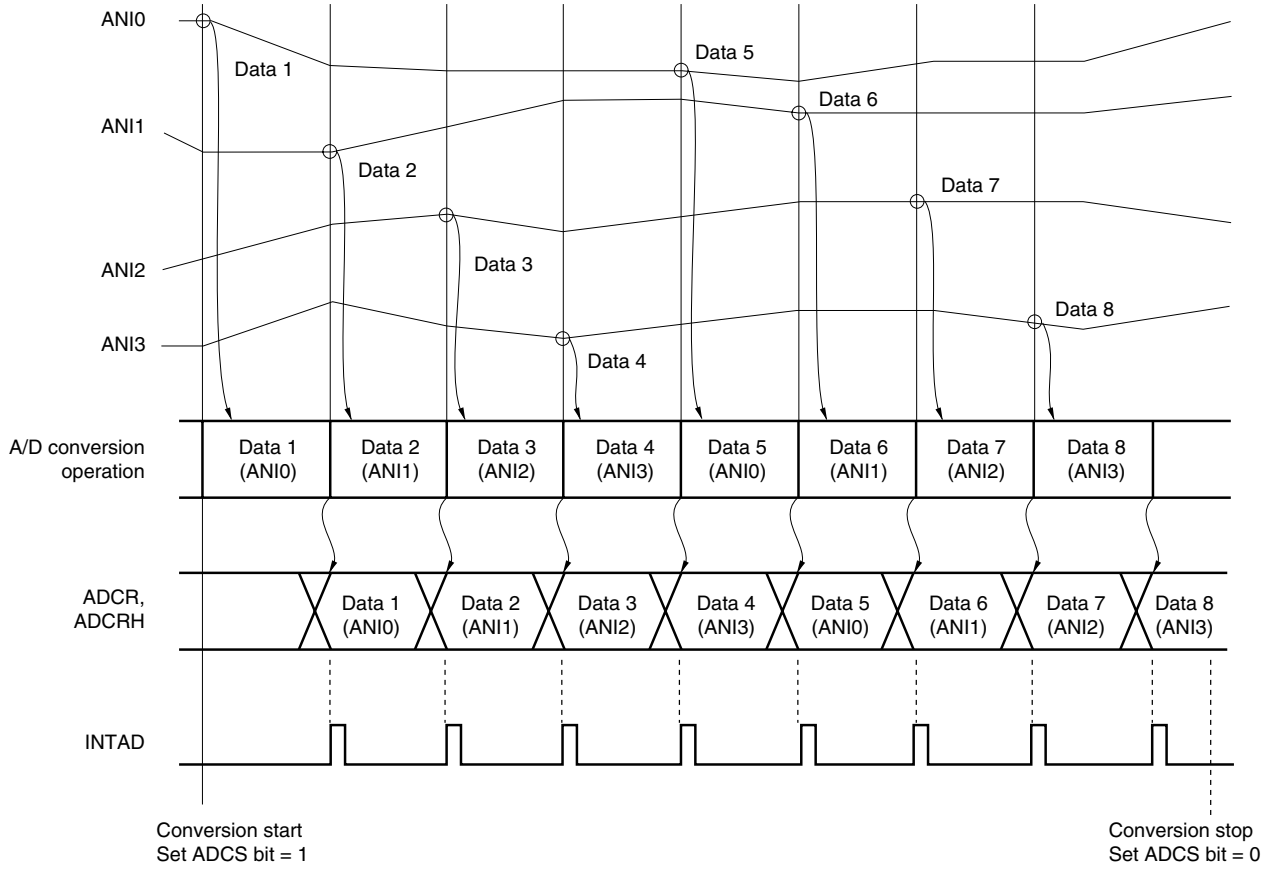
When A/D conversion of one analog input is complete, the conversion result is stored in the A/D conversion result register (ADCR) and the A/D conversion end interrupt request signal (INTAD) is generated.

The A/D conversion results of all the analog input channels are stored in the ADCR register. It is therefore recommended to save the contents of the ADCR register to RAM, once A/D conversion of one analog input channel has been completed.

After A/D conversion has been completed, A/D conversion is repeated successively, unless the ADCS bit is set to 0.

If anything is written to the ADM or ADS register during conversion, A/D conversion is aborted. In this case, A/D conversion is started again from the analog input channel of scan 0.

Figure 13-15. Example of Scan Mode Operation Timing



The setting methods are described below.

<1> Set bit 5 (ADCEN) of peripheral enable register 0 (PER0) to 1.
<2> Select the conversion time by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of the A/D converter mode register (ADM), and select the operation mode by using bit 6 (ADMD) of the ADM register.
<3> Set bit 0 (ADCE) of the ADM register to 1.
<4> Set the channel to be used in the analog input mode by using bits 4 to 0 (ADPC4 to ADPC0) of the A/D port configuration register (ADPC), bits 7 to 0 (PM27 to PM20) of port mode register 2 (PM2), bits 7 to 0 (PM157 to PM150) of port mode register 15 (PM15), and bit 0 (PM80) of port mode register 8 (PM8).
<5> Set the programmable gain amplifier operation to set the programmable gain amplifier output (PGAI pin) for the analog input channel (refer to **10.4.1 Starting comparator and programmable gain amplifier operation**).
<6> Select a channel to be used by using bits 6 and 3 to 0 (ADOAS, ADS3 to ADS0) of the analog input channel specification register (ADS).
<7> Set bit 7 (ADCS) of the ADM register to 1 to start A/D conversion.
<8> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<9> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH).

<Change the channel>

<10> Change the channel using bits 6 and 3 to 0 (ADOAS, ADS3 to ADS0) of the ADS register to start A/D conversion.
<11> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<12> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH).

<Complete A/D conversion>

<13> Clear the ADCS bit to 0.
<14> Clear the ADCE bit to 0.
<15> Clear bit 5 (ADCEN) of peripheral enable register 0 (PER0) to 0.

Cautions 1. Make sure the period of <3> to <7> is 1 μs or more.
2. <3> may be done between <4> and <6>.
3. <3> can be omitted. However, ignore data of the first conversion after <7> in this case.
4. The period from <8> to <11> differs from the conversion time set using bits 5 to 1 (FR2 to FR0, LV1, LV0) of the ADM register. The period from <10> to <11> is the conversion time set using the FR2 to FR0, LV1, and LV0 bits.

13.5 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 10 bits.

$1LSB = 1/2^{10} = 1/1024$
$= 0.098\%FSR$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.
Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a ±1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.
Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 13-16. Overall Error

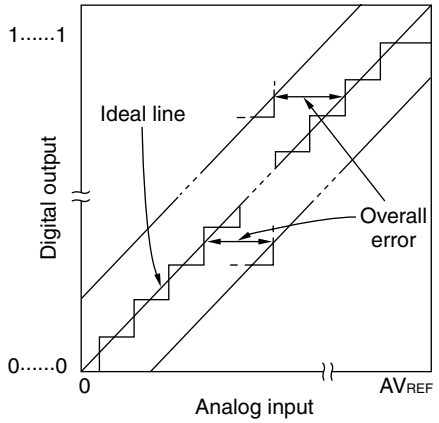
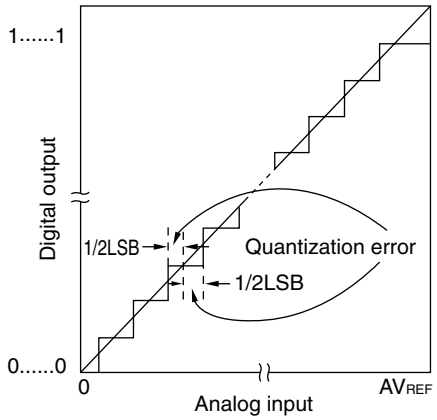


Figure 13-17. Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2LSB) when the digital output changes from 0.....000 to 0.....001.
If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value (3/2LSB) when the digital output changes from 0……001 to 0……010.

(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale – 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

(7) Differential linearity error

While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

Figure 13-18. Zero-Scale Error

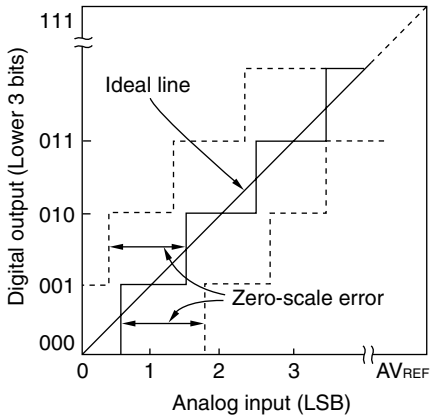


Figure 13-19. Full-Scale Error

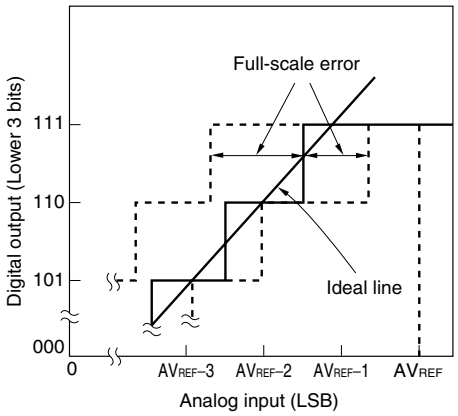


Figure 13-20. Integral Linearity Error

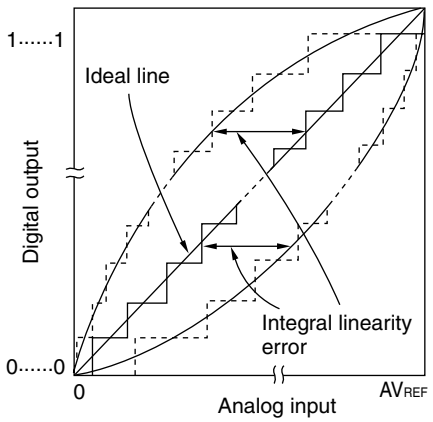
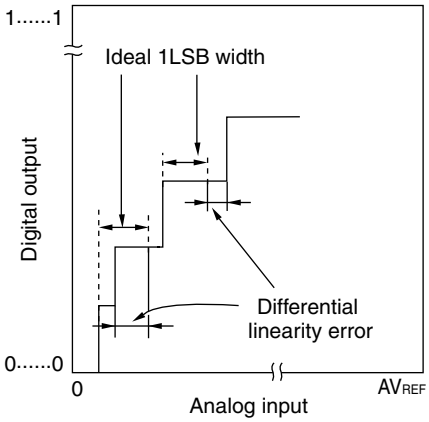


Figure 13-21. Differential Linearity Error



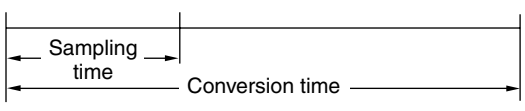
(8) Conversion time

This expresses the time from the start of sampling to when the digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.



13.6 Cautions for A/D Converter

(1) Operating current in STOP mode

Shift to STOP mode after stopping the A/D converter (by setting bit 7 (ADCS) of the A/D converter mode register (ADM) to 0). The operating current can be reduced by setting bit 0 (ADCE) of the ADM register to 0 at the same time. To restart from the standby status, clear bit 0 (ADIF) of interrupt request flag register 1L (IF1L) to 0 and start operation.

(2) Input range of ANI0 to ANI15 pins

Observe the rated range of the ANI0 to ANI15 pins input voltage. If a voltage of AV_{REF} or higher and AV_{SS} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

(3) Conflicting operations

<1> Conflict between the A/D conversion result register (ADCR, ADCRH) write and the ADCR or ADCRH register read by instruction upon the end of conversion

The ADCR or ADCRH register read has priority. After the read operation, the new conversion result is written to the ADCR or ADCRH registers.

<2> Conflict between the ADCR or ADCRH register write and the A/D converter mode register (ADM) write, the analog input channel specification register (ADS), or A/D port configuration register (ADPC) write upon the end of conversion

The ADM, ADS, or ADPC registers write has priority. The ADCR or ADCRH register write is not performed, nor is the conversion end interrupt signal (INTAD) generated.

(4) Noise countermeasures

To maintain the 10-bit resolution, attention must be paid to noise input to the AV_{REF} pin and ANI0 to ANI15 pins.

<1> Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

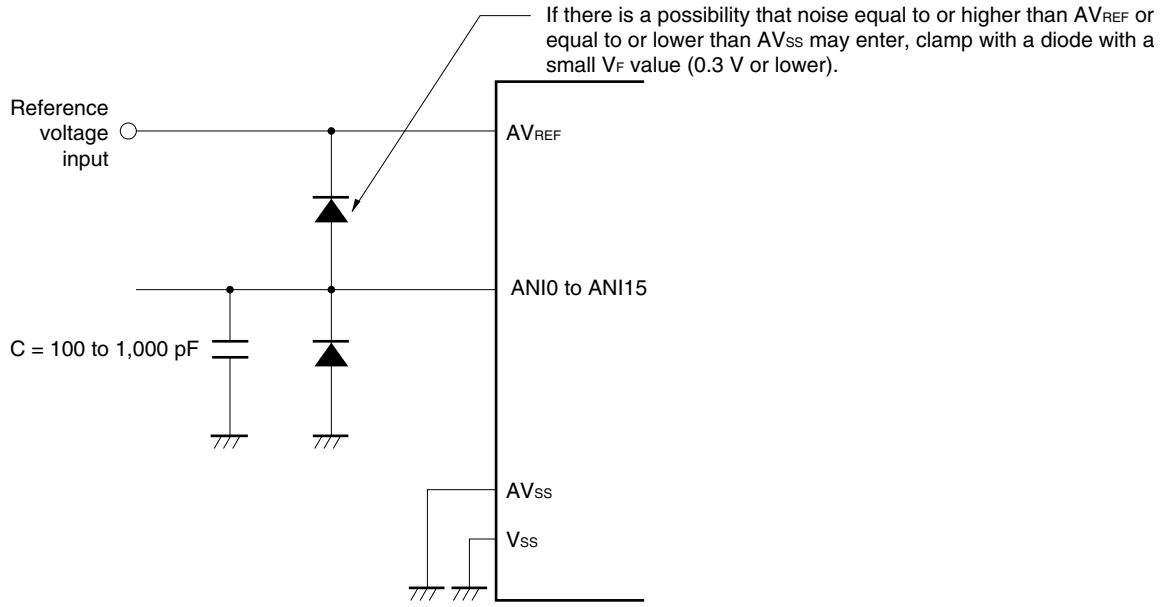
<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external C as shown in Figure 13-22 is recommended.

<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

Remark ANI0 to ANI9: 78K0R/KC3-L (40-pin, 44-pin)
ANI0 to ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
ANI0 to ANI11: 78K0R/KE3-L, 78K0R/KF3-L
ANI0 to ANI15: 78K0R/KG3-L

Figure 13-22. Analog Input Pin Connection



(5) ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI15/P157 pins

<1> The analog input pins (ANI0 to AN15) are also used as input port pins (P20 to P27, P150 to P157). When A/D conversion is performed with any of the ANI0 to ANI15 pins selected, do not access P20 to P27 and P150 to P157 while conversion is in progress; otherwise the conversion resolution may be degraded. It is recommended to select pins used as P20 to P27 and P150 to P157 starting with the ANI0/P20 pin that is the furthest from AV_{REF}.

<2> If a digital pulse is applied to the pins adjacent to the pins currently used for A/D conversion, the expected value of the A/D conversion may not be obtained due to coupling noise. Therefore, do not apply a pulse to the pins adjacent to the pin undergoing A/D conversion.

(6) Input impedance of ANI0 to ANI15 pins

This A/D converter charges a sampling capacitor for sampling during sampling time.

Therefore, only a leakage current flows when sampling is not in progress, and a current that charges the capacitor flows during sampling. Consequently, the input impedance fluctuates depending on whether sampling is in progress, and on the other states.

To make sure that sampling is effective, however, it is recommended to keep the output impedance of the analog input source to within 1 kΩ, and to connect a capacitor of about 100 pF to the ANI0 to ANI15 pins (see **Figure 13-22**).

(7) AV_{REF} pin input impedance

A series resistor string of several tens of kΩ is connected between the AV_{REF} and AV_{SS} pins.

Therefore, if the output impedance of the reference voltage source is high, this will result in a series connection to the series resistor string between the AV_{REF} and AV_{SS} pins, resulting in a large reference voltage error.

Remark P20/ANI0 to P27/ANI7, P150/ANI8, P151/ANI9: 78K0R/KC3-L (40-pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L, 78K0R/KF3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P157/ANI15: 78K0R/KG3-L

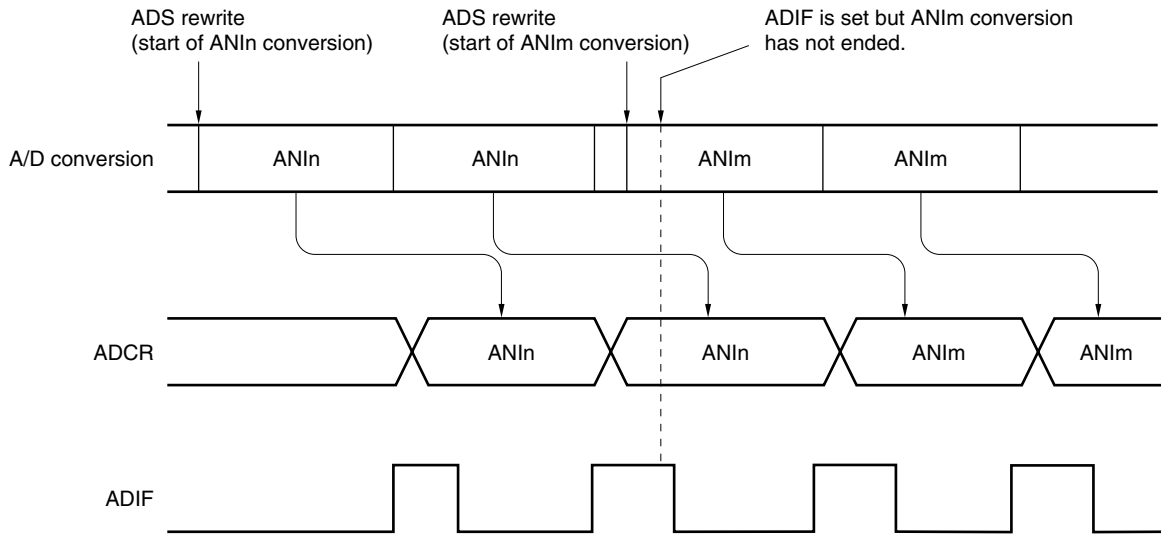
(8) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.

Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF flag for the pre-change analog input may be set just before the ADS register rewrite. Caution is therefore required since, at this time, when ADIF flag is read immediately after the ADS register rewrite, ADIF flag is set despite the fact A/D conversion for the post-change analog input has not ended.

When A/D conversion is stopped and then resumed, clear ADIF flag before the A/D conversion operation is resumed.

Figure 13-23. Timing of A/D Conversion End Interrupt Request Generation



Remark n = 0 to 9, m = 0 to 9: 78K0R/KC3-L (40-pin, 44-pin), 78K0R/KC3-L (48-pin)
n = 0 to 10, m = 0 to 10: 78K0R/KD3-L
n = 0 to 11, m = 0 to 11: 78K0R/KE3-L, 78K0R/KF3-L
n = 0 to 11, m = 0 to 15: 78K0R/KG3-L

(9) Conversion results just after A/D conversion start

The first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μs after the ADCE bit was set to 1. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.

(10) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of the ADCR and ADCRH registers may become undefined. Read the conversion result following conversion completion before writing to the ADM, ADS, or ADPC register. Using a timing other than the above may cause an incorrect conversion result to be read.

(11) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 13-24. Internal Equivalent Circuit of ANIn Pin

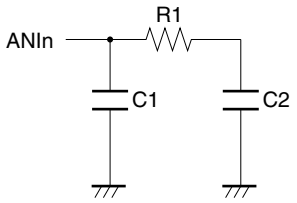


Table 13-4. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AV_{REF}	Mode	R1	C1	C2
4.0 V ≤ V_{DD} ≤ 5.5 V	Normal	5.2 kΩ	8 pF	6.3 pF
	High speed 1	5.2 kΩ		
	High speed 2	7.8 kΩ		
2.7 V ≤ V_{DD} < 4.0 V	Normal	18.6 kΩ		
	High speed 2	7.8 kΩ		
1.8 V ≤ V_{DD} < 4.0 V	Low-voltage	169.8 kΩ		

Remarks 1. The resistance and capacitance values shown in Table 13-4 are not guaranteed values.

2. 78K0R/KC3-L (40-pin, 44-pin): n = 0 to 9
78K0R/KC3-L (48-pin), 78K0R/KD3-L: n = 0 to 10
78K0R/KE3-L, 78K0R/KF3-L: n = 0 to 11
78K0R/KG3-L: n = 0 to 15

(12) Starting the A/D converter

Start the A/D converter after the AV_{REF} voltage stabilize.

CHAPTER 14 SERIAL ARRAY UNIT

Each serial array unit has four serial channels, each of which can be used for 3-wire serial (CSI), UART, and simplified I2C communication.

Function assignment of each channel supported by the 78K0R/Kx3-L is as shown below.

- 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0 (supporting LIN-bus)	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–

- 78K0R/KF3-L, 78K0R/KG3-L

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	CSI20	UART2	IIC20
	1	–		–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–
2 Note	0	CSI40	UART4	–
	1	CSI41		–

Note Serial array unit 2 is only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

When “UART0” is used for channels 0 and 1 of the unit 0, CSI00 and CSI01 cannot be used, but CSI10, UART1, or IIC10 can be used.

14.1 Functions of Serial Array Unit

Each serial interface supported by the 78K0R/Kx3-L has the following features.

14.1.1 3-wire serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41)

Data is transmitted or received in synchronization with the serial clock ($\overline{SCK}$) output from the master channel.

3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock ($\overline{SCK}$), one for transmitting serial data (SO), one for receiving serial data (SI).

For details about the settings, see **14.5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) Communication.**

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

  During master communication: Max. $f_{CLK}/4$, during slave communication: Max. $f_{MCK}/6$ Note

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

Note Use the clocks within a range satisfying the $\overline{SCK}$ cycle time (t_{KCY}) characteristics (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)** or **CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

14.1.2 UART (UART0 to UART4)

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using timer array unit 0 with an external interrupt (INTP0).

For details about the settings, see **14.6 Operation of UART (UART0 to UART4) Communication.**

[Data transmission/reception]

- Data length of 5, 7, or 8 bits
- Select the MSB/LSB first
- Level setting of transmit/receive data and select of reverse
- Parity bit appending and parity check functions
- Stop bit appending

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

The LIN-bus is accepted in UART0 (0 and 1 channels) of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L and UART3 (2 and 3 channels) of the 78K0R/KF3-L, 78K0R/KG3-L.

[LIN-bus functions]

- Wakeup signal detection
- Sync break field (SBF) detection
- Sync field measurement, baud rate calculation

} Using the external interrupt (INTP0) and timer array unit 0

14.1.3 Simplified I²C (IIC10, IIC20)

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I²C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master.

Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

For details about the settings, see **14.8 Operation of Simplified I²C (IIC10, IIC20)**

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function[Note] and ACK detection function
- Data length of 8 bits (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- Parity error (ACK error)

* [Functions not supported by simplified I²C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

Note When receiving the last data, ACK will not be output if 0 is written to the SOEmn bit (serial output enable register m (SOEm)) and serial communication data output is stopped. See the processing flow in **14.8.3 (2)** for details.

Remark To use an I²C bus of full function, see **CHAPTER 15 SERIAL INTERFACE IICA**.

14.2 Configuration of Serial Array Unit

The serial array unit includes the following hardware.

Table 14-1. Configuration of Serial Array Unit (1/2) (78K0R/KC3-L, KD3-L, KE3-L)

Item	Configuration
	78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L
Shift register	8 bits
Buffer register	Lower 8 bits of serial data register mn (SDRmn)[Note]
Serial clock I/O	$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$ pins (for 3-wire serial I/O), SCL10 pin (for simplified I^2C)
Serial data input	SI00, SI01, SI10 pins (for 3-wire serial I/O), RxD0 pin (for UART supporting LIN-bus), RxD1 pin (for UART)
Serial data output	SO00, SO01, SO10 pins (for 3-wire serial I/O), TxD0 pin (for UART supporting LIN-bus), TxD1 pin (for UART), output controller
Serial data I/O	SDA10 pin (for simplified I^2C)
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Serial clock select register 0 (SPS0) • Serial channel enable status register 0 (SE0) • Serial channel start register 0 (SS0) • Serial channel stop register 0 (ST0) • Serial output enable register 0 (SOE0) • Serial output register 0 (SO0) • Serial output level register 0 (SOL0) • Input switch control register (ISC) • Noise filter enable register 0 (NFEN0)
	<Registers of each channel> • Serial data register 0n (SDR0n) • Serial mode register 0n (SMR0n) • Serial communication operation setting register 0n (SCR0n) • Serial status register 0n (SSR0n) • Serial flag clear trigger register 0n (SIR0n)
	• Port input mode registers 3, 7 (PIM3, PIM7) • Port output mode registers 3, 7 (POM3, POM7) • Port mode registers 3, 7 (PM3, PM7) • Port registers 3, 7 (P3, P7)

Note The lower 8 bits of serial data register 0n (SDR0n) can be read or written as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IIC10 communication … SIO10 (IIC10 data register)

Remark n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10),
q: UART number (q = 0, 1)

Table 14-1. Configuration of Serial Array Unit (2/2) (78K0R/KF3-L, 78K0R/KG3-L)

Item	Configuration	
	μPD78F1010, 78F1011, 78F1012, 78F1013, 78F1014	μPD78F1027, 78F1028, 78F1029, 78F1030
Shift register	8 bits	
Buffer register	Lower 8 bits of serial data register mn (SDRmn)[Note]	
Serial clock I/O	$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK20}$ pins (for 3-wire serial I/O), SCL10, SCL20 pins (for simplified I^2C)	$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK20}$, $\overline{SCK40}$, $\overline{SCK41}$ pins (for 3-wire serial I/O), SCL10, SCL20 pins (for simplified I^2C)
Serial data input	SI00, SI01, SI10, SI20 pins (for 3-wire serial I/O), RxD0 to RxD2 pins (for UART), RxD3 pin (for UART supporting LIN-bus)	SI00, SI01, SI10, SI20, SI40, SI41 pins (for 3-wire serial I/O), RxD0 to RxD2, RxD4 pins (for UART), RxD3 pin (for UART supporting LIN-bus)
Serial data output	SO00, SO01, SO10, SO20 pins (for 3-wire serial I/O), TxD0 to TxD2 pins (for UART), TxD3 pin (for UART supporting LIN-bus), output controller	SO00, SO01, SO10, SO20, SO40, SO41 pins (for 3-wire serial I/O), TxD0 to TxD2, TxD4 pins (for UART), TxD3 pin (for UART supporting LIN-bus), output controller
Serial data I/O	SDA10, SDA20 pins (for simplified I^2C)	
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Serial clock select register m (SPSm) • Serial channel enable status register m (SEm) • Serial channel start register m (SSm) • Serial channel stop register m (STm) • Serial output enable register m (SOEm) • Serial output register m (SOm) • Serial output level register m (SOLm) • Input switch control register (ISC) • Noise filter enable register 0 (NFEN0)	<Registers of unit setting block> • Peripheral enable registers 0, 1 (PER0, PER1) • Serial clock select register m (SPSm) • Serial channel enable status register m (SEm) • Serial channel start register m (SSm) • Serial channel stop register m (STm) • Serial output enable register m (SOEm) • Serial output register m (SOm) • Serial output level register m (SOLm) • Input switch control register (ISC) • Noise filter enable register 0 (NFEN0)
	<Registers of each channel> • Serial data register mn (SDRmn) • Serial mode register mn (SMRmn) • Serial communication operation setting register mn (SCRmn) • Serial status register mn (SSRmn) • Serial flag clear trigger register mn (SIRmn)	
	• Port input mode registers 0, 1, 14 (PIM0, PIM1, PIM14) • Port output mode registers 0, 1, 14 (POM0, POM1, POM14) • Port mode registers 0, 1, 4, 14 (PM0, PM1, PM4, PM14) • Port registers 0, 1, 4, 14 (P0, P1, P4, P14	

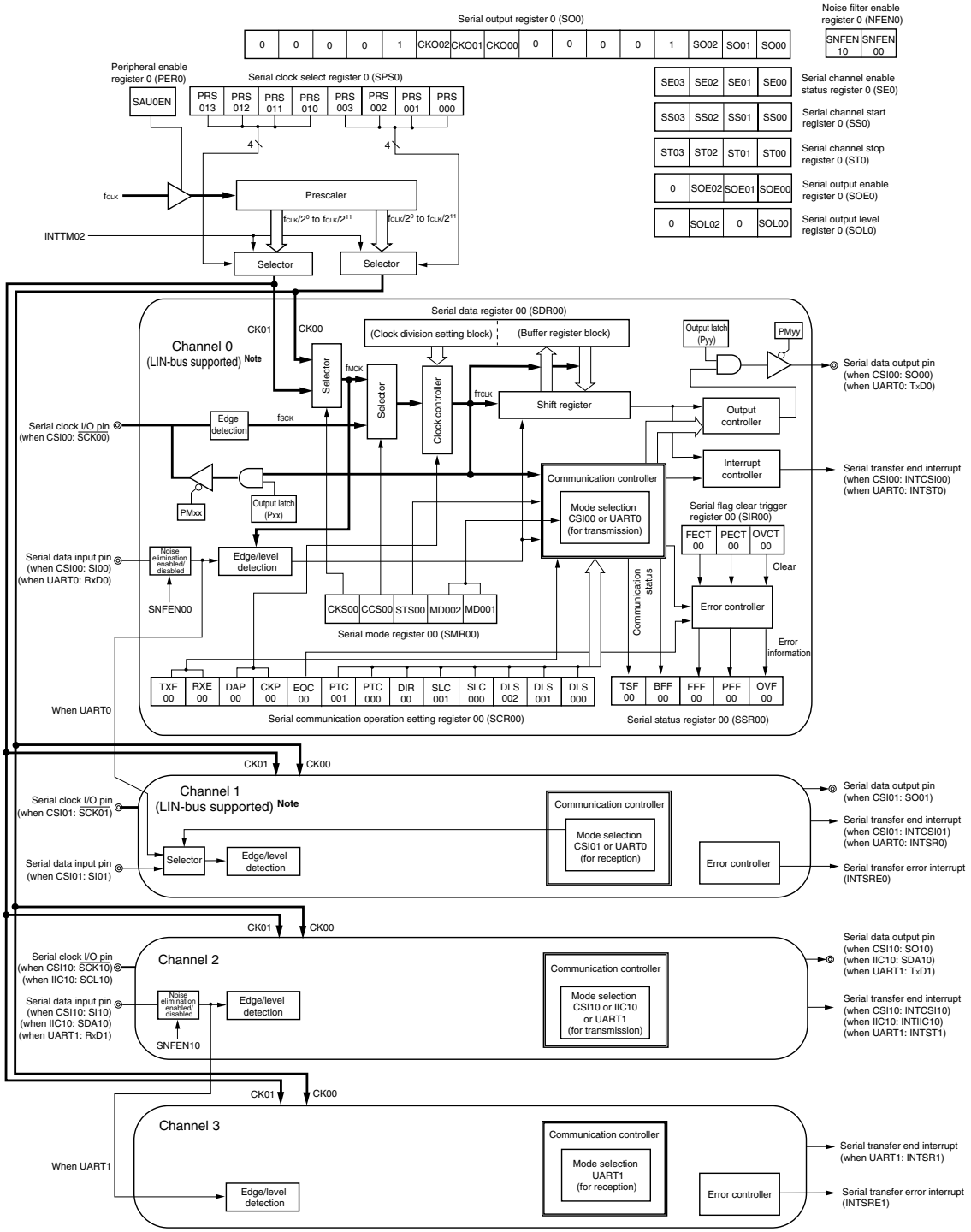
Note The lower 8 bits of serial data register mn (SDRmn) can be read or written as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IICr communication … SIOr (IICr data register)

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 20, 40, 41), q: UART number (q = 0 to 4), r: IIC number (r = 10, 20)

Figure 14-1 shows the block diagram of the serial array unit 0.

Figure 14-1. Block Diagram of Serial Array Unit 0

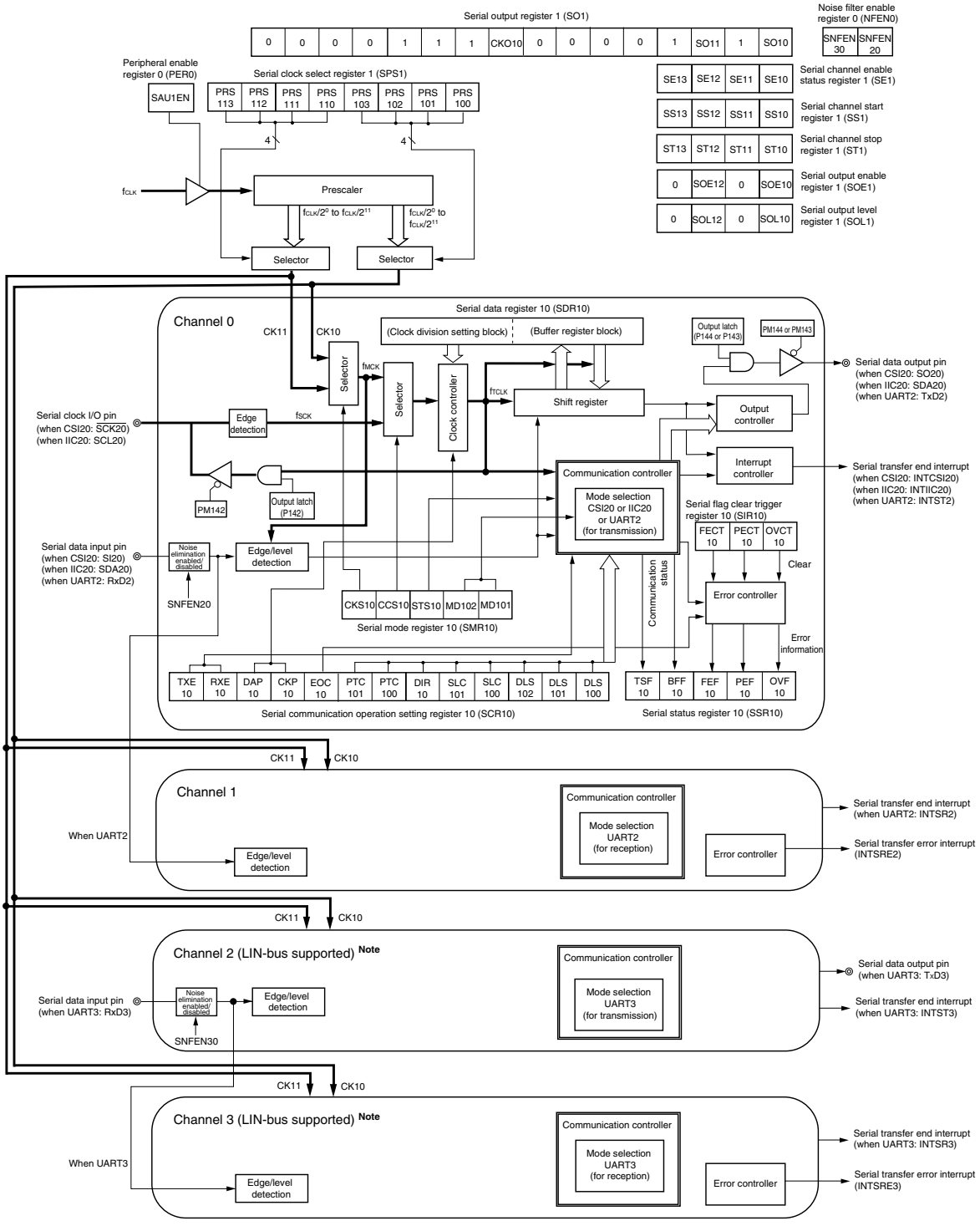


Note In the 78K0R/KF3-L and 78K0R/KG3-L, UART3 (unit 1, channels 2 and 3) is used for LIN-bus communication.

Remark 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: PMxx, Pxx = PM75, P75 PMyy, Pyy = PM73, P73
78K0R/KF3-L, 78K0R/KG3-L: PMxx, Pxx = PM10, P10 PMyy, Pyy = PM12, P12

Figure 14-2 shows the block diagram of the serial array unit 1.

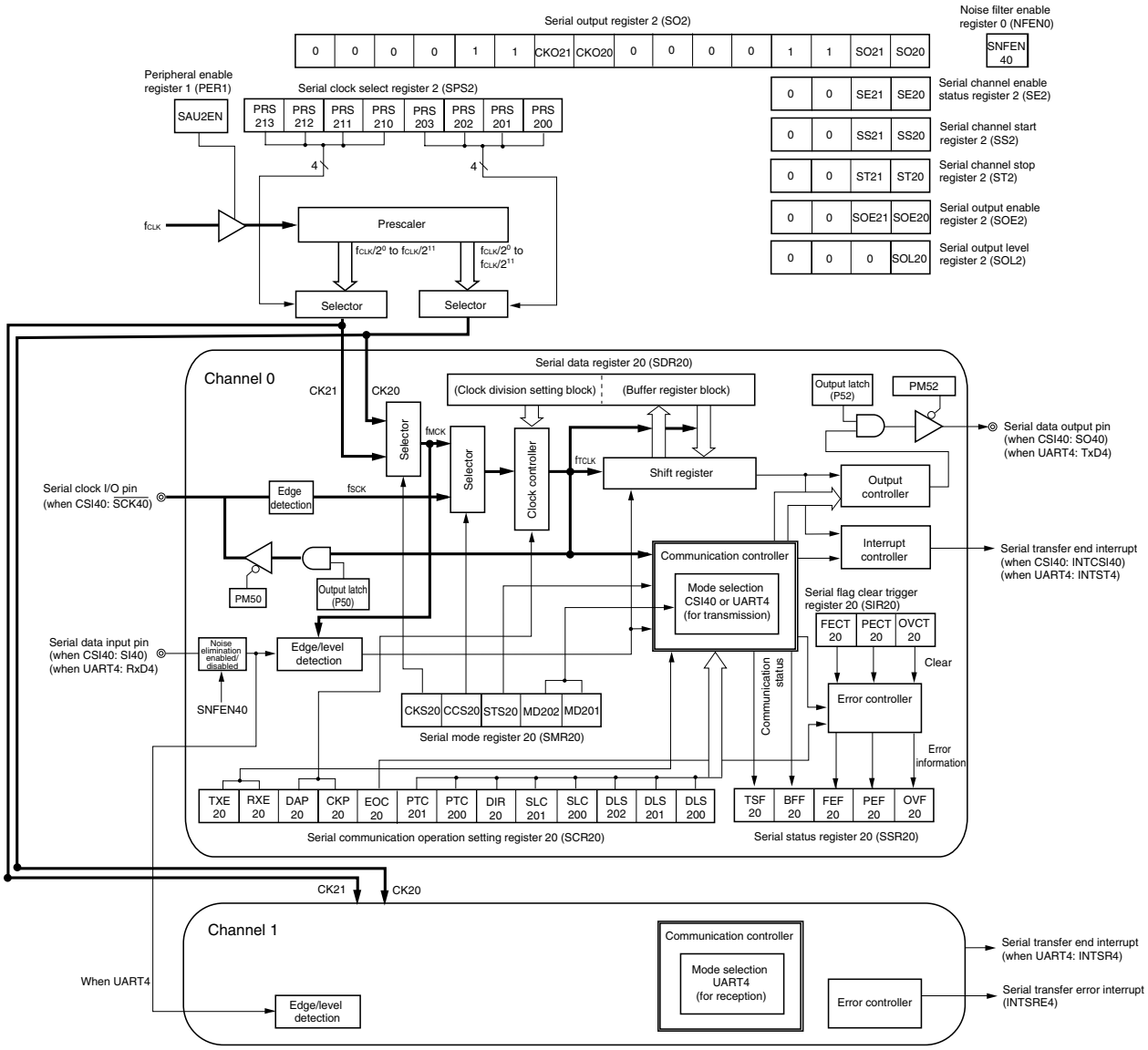
Figure 14-2. Block Diagram of Serial Array Unit 1 (78K0R/KF3-L, 78K0R/KG3-L only)



Note In the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L, UART0 (unit 0, channels 0 and 1) is used for LIN-bus communication.

Figure 14-3 shows the block diagram of the serial array unit 1.

Figure 14-3. Block Diagram of Serial Array Unit 1 (μPD78F1027, 78F1028, 78F1029, 78F1030 only)



(1) Shift register

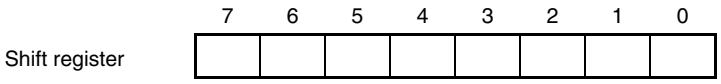
This is an 8-bit register that converts parallel data into serial data or vice versa.

During reception, it converts data input to the serial pin into parallel data.

When data is transmitted, the value set to this register is output as serial data from the serial output pin.

The shift register cannot be directly manipulated by program.

To read or write the shift register, use the lower 8 bits of serial data register mn (SDRmn).



(2) Lower 8 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 7 to 0 function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock (f_{MCK}).

When data is received, parallel data converted by the shift register is stored in the lower 8 bits. When data is to be transmitted, set transmit to be transferred to the shift register to the lower 8 bits.

The data stored in the lower 8 bits of this register is as follows, depending on the setting of bits 0 to 2 (DLSmn0 to DLSmn2) of serial communication operation setting register mn (SCRmn), regardless of the output sequence of the data.

- 5-bit data length (stored in bits 0 to 4 of SDRmn register) (settable in UART mode only)
- 7-bit data length (stored in bits 0 to 6 of SDRmn register)
- 8-bit data length (stored in bits 0 to 7 of SDRmn register)

The SDRmn register can be read or written in 16-bit units.

The lower 8 bits of the SDRmn register can be read or written[Note] as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IICr communication … SIOr (IICr data register)

Reset signal generation clears the SDRmn register to 0000H.

Note Writing in 8-bit units is prohibited when the operation is stopped (SEmn = 0).

Remarks 1. After data is received, "0" is stored in bits 0 to 7 in bit portions that exceed the data length.

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 20, 40, 41), q: UART number (q = 0 to 4), r: IIC number (r = 10, 20)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03, p = 00, 01, 10, q = 0, 1, r = 10

78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00 to 03, 10 to 13, p = 00, 01, 10, 20, q = 0 to 3, r = 10, 20

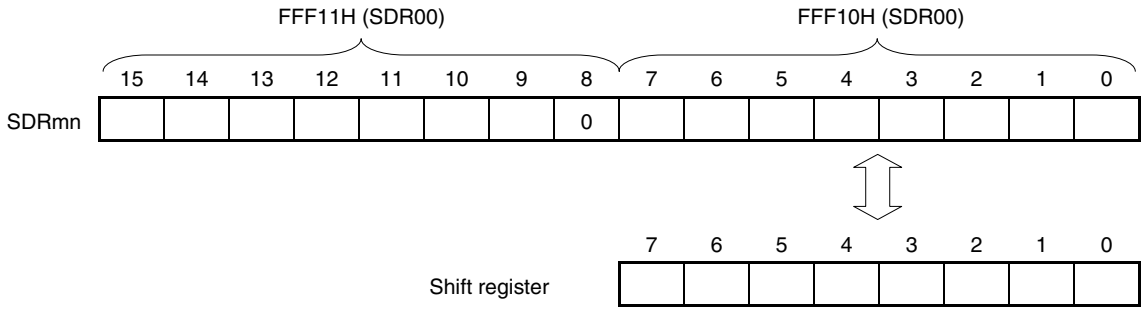
78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00 to 03, 10 to 13, 20, 21, p = 00, 01, 10, 20, 40, 41, q = 0 to 4, r = 10, 20

78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00 to 03, 10 to 13, p = 00, 01, 10, 20, q = 0 to 3, r = 10, 20

78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00 to 03, 10 to 13, 20, 21, p = 00, 01, 10, 20, 40, 41, q = 0 to 4, r = 10, 20

Figure 14-3. Format of Serial Data Register mn (SDRmn)

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01), After reset: 0000H R/W
FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03)
FFF48H, FFF49H (SDR10), FFF4AH, FFF4BH (SDR11),
FFF14H, FFF15H (SDR12), FFF16H, FFF17H (SDR13),
FFF4CH, FFF4DH (SDR20), FFF4EH, FFF4FH (SDR21)



Caution Be sure to clear bit 8 to "0".

Remarks 1. For the function of the higher 7 bits of the SDRmn register, see **14.3 Registers Controlling Serial Array Unit**.

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00-03,
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00-03, 10-13
78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00-03, 10-13, 20, 21
78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00-03, 10-13
78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00-03, 10-13, 20, 21

14.3 Registers Controlling Serial Array Unit

Serial array unit is controlled by the following registers.

- Peripheral enable registers 0, 1 (PER0, PER1)
- Serial clock select register m (SPSm)
- Serial mode register mn (SMRmn)
- Serial communication operation setting register mn (SCRmn)
- Serial data register mn (SDRmn)
- Serial flag clear trigger register mn (SIRmn)
- Serial status register mn (SSRmn)
- Serial channel start register m (SSm)
- Serial channel stop register m (STm)
- Serial channel enable status register m (SEm)
- Serial output enable register m (SOEm)
- Serial output level register m (SOLm)
- Serial output register m (SOm)
- Input switch control register (ISC)
- Noise filter enable register 0 (NFEN0)

[78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L]

- Port input mode registers 3, 7 (PIM3, PIM7)
- Port output mode registers 3, 7 (POM3, POM7)
- Port mode registers 3, 7 (PM3, PM7)
- Port registers 3, 7 (P3, P7)

[78K0R/KF3-L, 78K0R/KG3-L]

- Port input mode registers 0, 1, 14 (PIM0, PIM1, PIM14)
- Port output mode registers 0, 1, 14 (POM0, POM1, POM14)
- Port mode registers 0, 1, 4, 5Note, 14 (PM0, PM1, PM4, PM5Note, PM14)
- Port registers 0, 1, 4, 5Note, 14 (P0, P1, P4, P5Note, P14)

Note Those are only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:		mn = 00 to 03
78K0R/KF3-L	μPD78F1010, 78F1011, 78F1012 :	mn = 00 to 03, 10 to 13
78K0R/KF3-L	μPD78F1027, 78F1028 :	mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L	μPD78F1013, 78F1014 :	mn = 00 to 03, 10 to 13
78K0R/KG3-L	μPD78F1029, 78F1030 :	mn = 00 to 03, 10 to 13, 20, 21

(1) Peripheral enable registers 0, 1 (PER0, PER1)

PER0 and PER1 register are used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When serial array unit 0 is used, be sure to set bit 2 (SAU0EN) of PER0 register to 1.

In the 78K0R/KF3-L and 78K0R/KG3-L, be sure to set bit 3 (SAU1EN) of PER0 register to 1 when using serial array unit 1, in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030), be sure to set bit 0 (SAU2EN) of PER1 register to 1 when using serial array unit 2.

The PER0 and PER1 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the PER0 and PER1 register to 00H.

Figure 14-5. Format of Peripheral Enable Register 0, 1 (PER0, PER1)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN Note 1	0	ADCEN	IICAEN Note 2	SAU1EN Note 3	SAU0EN	TAU1EN Note 3	TAU0EN Note 3

Address: F00F1H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
PER1 Note	0	0	0	0	0	0	0	SAU2EN Note 4

SAUmEN	Control of serial array unit m input clock supply
0	Stops supply of input clock. • SFR used by serial array unit m cannot be written. • Serial array unit m is in the reset status.
1	Enables input clock supply. • SFR used by serial array unit m can be read/written.

Notes 1. That is not provided in 40-pin product of the 78K0R/KC3-L.

2. That is not provided in 40-pin and 44-pin products of the 78K0R/KC3-L.

3. 78K0R/KF3-L and 78K0R/KG3-L only.

4. 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030) only.

Cautions 1. When setting serial array unit m, be sure to set the SAUmEN bit to 1 first. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read.
Note that this does not apply to the following registers.
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:
ISC, NFEN0, PIM3, PIM7, POM3, POM7, PM3, PM7, P3, and P7 registers.
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012), 78K0R/KG3-L (μPD78F1013, 78F1014):
ISC, NFEN0, PIM0, PIM1, PIM14, POM0, POM1, POM14, PM0, PM1, PM4, PM14, P0, P1, P4, and P14 registers.
78K0R/KF3-L (μPD78F1027, 78F1028), 78K0R/KG3-L (μPD78F1029, 78F1030):
ISC, NFEN0, PIM0, PIM1, PIM14, POM0, POM1, POM14, PM0, PM1, PM4, PM5, PM14, P0, P1, P4, P5, and P14 registers.

2. After setting the SAUmEN bit to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

(**Caution 3** and **Remark** are listed on the next page.)

Cautions 3. Be sure to clear the following bits to 0.

48-pin product of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	**bits 0, 1, 3, 6 of PER0 register**
44-pin product of the 78K0R/KC3-L:	**bits 0, 1, 3, 4, 6 of PER0 register**
40-pin product of the 78K0R/KC3-L:	**bits 0, 1, 3, 4, 6, 7 of PER0 register**
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	**bit 6 of PER0 register**
78K0R/KF3-L (μPD78F1027, 78F1028):	**bit 6 of PER0 register, bits 1 to 7 of PER1 register**
78K0R/KG3-L (μPD78F1013, 78F1014):	**bit 6 of PER0 register**
78K0R/KG3-L (μPD78F1029, 78F1030):	**bit 6 of PER0 register, bits 1 to 7 of PER1 register**

Remark

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:		m = 0
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012	:	m = 0, 1
78K0R/KF3-L μPD78F1027, 78F1028	:	m = 0 to 2
78K0R/KG3-L μPD78F1013, 78F1014	:	m = 0, 1
78K0R/KG3-L μPD78F1029, 78F1030	:	m = 0 to 2

(2) Serial clock select register m (SPSm)

The SPSm register is a 16-bit register that is used to select two types of operation clocks (CKm0, CKm1) that are commonly supplied to each channel. CKm1 is selected by bits 7 to 4 of the SPSm register , and CKm0 is selected by bits 3 to 0.

Rewriting the SPSm register is prohibited when the register is in operation (when SEmn = 1).

The SPSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SPSm register can be set with an 8-bit memory manipulation instruction with SPSmL.

Reset signal generation clears the SPSm register to 0000H.

Figure 14-6. Format of Serial Clock Select Register m (SPSm) (1/2)

Address: F0126H, F0127H (SPS0), F0166H, F0167H (SPS1) After reset: 0000H R/W
F0216H, F0217H (SPS2)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPSm	0	0	0	0	0	0	0	0	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00

PRS mk3	PRS mk2	PRS mk1	PRS mk0	Section of operation clock (CKmk) Note 1				
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	313 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156 kHz	313 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	78.1 kHz	156 kHz	313 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	39.1 kHz	78.1 kHz	156 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.77 kHz	19.5 kHz	39.1 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	2.44 kHz	4.88 kHz	9.77 kHz
1	1	1	1	INTTM02 if m = 0 Note 2, setting prohibited if m = 1				
Other than above				Setting prohibited				

Notes 1. When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU). When selecting INTTM02 for the operation clock, also stop the timer array unit 0 (timer channel stop register 0 (TT0) = 00FFH).

2. SAU0 can be operated at a fixed division ratio of the subsystem clock, regardless of the f_{CLK} frequency (main system clock, sub system clock), by operating the interval timer for which $f_{SUB}/4$ Note 3 has been selected as the count clock (setting the TIS02 bit of timer input select register 0 (TIS0) to 1) and selecting INTTM02 by using the SPS0 register in channel 2 of TAU0. When changing f_{CLK}, however, SAU0 and TAU0 must be stopped as described in Note 1 above.

3. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Cautions 1. Be sure to clear bits 15 to 8 to "0".

2. After setting bit 2 (SAU0EN) of the PER0 register, bit 3 (SAU1EN) of the PER0 register, and bit 0 (SAU2EN) of the PER1 register to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Remarks 1. f_{CLK}: CPU/peripheral hardware clock frequency
f_{SUB}: Subsystem clock frequency

(**Remarks 2 and 3** are listed on the next page.)

Figure 14-6. Format of Serial Clock Select Register m (SPSm) (2/2)

Remarks 2. m: Unit number (m = 0, 1)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	m = 0
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	m = 0, 1
78K0R/KF3-L (μPD78F1027, 78F1028):	m = 0 to 2
78K0R/KG3-L (μPD78F1013, 78F1014):	m = 0, 1
78K0R/KG3-L(μPD78F1029, 78F1030):	m = 0 to 2

3. k = 0, 1

(3) Serial mode register mn (SMRmn)

The SMRmn register is a register that sets an operation mode of channel n. It is also used to select an operation clock (f_{MCK}), specify whether the serial clock (f_{SCK}) may be input or not, set a start trigger, an operation mode (CSI, UART, or I^2C), and an interrupt source. This register is also used to invert the level of the receive data only in the UART mode.

Rewriting the SMRmn register is prohibited when the register is in operation (when SEmn = 1). However, the MDmn0 bit can be rewritten during operation.

The SMRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets the SMRmn register to 0020H.

Figure 14-7. Format of Serial Mode Register mn (SMRmn) (1/3)

Address: F0110H, F0111H (SMR00) to F0116H, F0117H (SMR03), After reset: 0020H R/W
F0150H, F0151H (SMR10) to F0156H, F0157H (SMR13),
F0208H, F0209H (SMR20) , F020AH, F020BH (SMR21)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKS mn	CCS mn	0	0	0	0	0	STS mn	0	SIS mn0	1	0	0	MD mn2	MD mn1	MD mn0

CKS mn	Selection of operation clock (f_{MCK}) of channel n
0	Operation clock CKm0 set by the SPSm register
1	Operation clock CKm1 set by the SPSm register
Operation clock (f_{MCK}) is used by the edge detector. In addition, depending on the setting of the CCSmn bit and the higher 7 bits of the SDRmn register, a transfer clock (f_{TCLK}) is generated.	

CCS mn	Selection of transfer clock (f_{TCLK}) of channel n
0	Divided operation clock f_{MCK} specified by the CKSmn bit
1	Clock input f_{SCK} from the $\overline{SCKp}$ pin (slave transfer in CSI mode)
Transfer clock f_{TCLK} is used for the shift register, communication controller, output controller, interrupt controller, and error controller. When CCSmn = 0, the division ratio of operation clock (f_{MCK}) is set by the higher 7 bits of the SDRmn register.	

STS mn	Selection of start trigger source
0	Only software trigger is valid (selected for CSI, UART transmission, and simplified I^2C).
1	Valid edge of the RxDq pin (selected for UART reception)
Transfer is started when the above source is satisfied after 1 is set to the SSm register.	

Caution Be sure to clear bits 13 to 9, 7, 4, and 3 to "0". Be sure to set bit 5 to "1".

(**Remark** is listed on the next page.)

Figure 14-7. Format of Serial Mode Register mn (SMRmn) (2/3)

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 20, 40, 41), q: UART number (q = 0 to 4), r: IIC number (r = 10, 20)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 03, p = 00, 01, 10, q = 0, 1, r = 10
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 :	mn = 00 to 03, 10 to 13, p = 00, 01, 10, 20, q = 0 to 3, r = 10, 20
78K0R/KF3-L μPD78F1027, 78F1028 :	mn = 00 to 03, 10 to 13, 20, 21, p = 00, 01, 10, 20, 40, 41, q = 0 to 4, r = 10, 20
78K0R/KG3-L μPD78F1013, 78F1014 :	mn = 00 to 03, 10 to 13, p = 00, 01, 10, 20, q = 0 to 3, r = 10, 20
78K0R/KG3-L μPD78F1029, 78F1030 :	mn = 00 to 03, 10 to 13, 20, 21, p = 00, 01, 10, 20, 40, 41, q = 0 to 4, r = 10, 20

Figure 14-7. Format of Serial Mode Register mn (SMRmn) (3/3)

Address: F0110H, F0111H (SMR00) to F0116H, F0117H (SMR03), After reset: 0020H R/W
F0150H, F0151H (SMR10) to F0156H, F0157H (SMR13),
F0208H, F0209H (SMR20), F020AH, F020BH (SMR21)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKS mn	CCS mn	0	0	0	0	0	STS mn	0	SIS mn0	1	0	0	MD mn2	MD mn1	MD mn0

SIS mn0	Controls inversion of level of receive data of channel n in UART mode
0	Falling edge is detected as the start bit. The input communication data is captured as is.
1	Rising edge is detected as the start bit. The input communication data is inverted and captured.

MD mn2	MD mn1	Setting of operation mode of channel n
0	0	CSI mode
0	1	UART mode
1	0	Simplified I^2C mode
1	1	Setting prohibited

MD mn0	Selection of interrupt source of channel n
0	Transfer end interrupt
1	Buffer empty interrupt (Occurs when data is transferred from the SDRmn register to the shift register.)
For successive transmission, the next transmit data is written by setting the MDmn0 bit to 1 when SDRmn data has run out.	

Caution Be sure to clear bits 13 to 9, 7, 4, and 3 to "0". Be sure to set bit 5 to "1".

Remark m: Unit number (m = 0 to 2), n : Channel number (n = 0 to 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00 to 03, 10 to 13
78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00 to 03, 10 to 13
78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00 to 03, 10 to 13, 20, 21

(4) Serial communication operation setting register mn (SCRmn)

The SCRmn register is a communication operation setting register of channel n. It is used to set a data transmission/reception mode, phase of data and clock, whether an error signal is to be masked or not, parity bit, start bit, stop bit, and data length.

Rewriting the SCRmn register is prohibited when the register is in operation (when SEmn = 1).

The SCRmn register can be set by a 16-bit memory manipulation instruction.

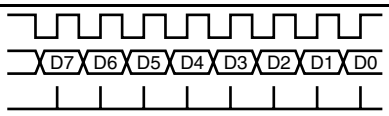
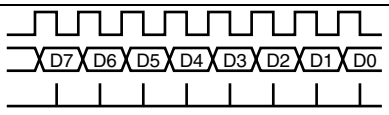
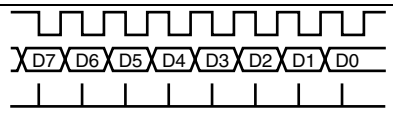
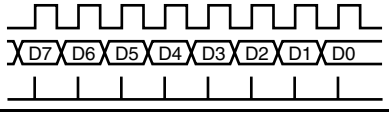
Reset signal generation sets the SCRmn register to 0087H.

Figure 14-8. Format of Serial Communication Operation Setting Register mn (SCRmn) (1/4)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), F0158H, F0159H (SCR10) to F015EH, F015FH (SCR13), F020CH, F020DH (SCR20), F020EH, F020FH (SCR21) After reset: 0087H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLC mn1	SLC mn0	0	DLS mn2	DLS mn1	DLS mn0

TXE mn	RXE mn	Setting of operation mode of channel n
0	0	Disable communication.
0	1	Reception only
1	0	Transmission only
1	1	Transmission/reception

DAP mn	CKP mn	Selection of data and clock phase in CSI mode	Type
0	0		1
0	1		2
1	0		3
1	1		4
Be sure to set DAPmn, CKPmn = 0, 0 in the UART mode and simplified I^2C mode.			

EOC mn	Selection of masking of error interrupt signal (INTSREx (x = 0 to 3))
0	Masks error interrupt INTSREx (INTSRx is not masked).
1	Enables generation of error interrupt INTSREx (INTSRx is masked if an error occurs).
Set EOCmn = 0 in the CSI mode, simplified I^2C mode, and during UART transmission[Note]. Set EOCmn = 1 during UART reception.	

Note When using CSI01 not with EOC01 = 0, error interrupt INTSRE0 may be generated.

Caution Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".

(**Remark** is listed on the next page.)

Figure 14-8. Format of Serial Communication Operation Setting Register mn (SCRmn) (2/4)

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 03, p = 00, 01, 10
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 :	mn = 00 to 03, 10 to 13, p = 00, 01, 10, 20
78K0R/KF3-L μPD78F1027, 78F1028 :	mn = 00 to 03, 10 to 13, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L μPD78F1013, 78F1014 :	mn = 00 to 03, 10 to 13, p = 00, 01, 10, 20
78K0R/KG3-L μPD78F1029, 78F1030 :	mn = 00 to 03, 10 to 13, 20, 21, p = 00, 01, 10, 20, 40, 41

Figure 14-8. Format of Serial Communication Operation Setting Register mn (SCRmn) (3/4)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), After reset: 0087H R/W
F0158H, F0159H (SCR10) to F015EH, F015FH (SCR13),
F020CH, F020DH (SCR20), F020EH, F020FH (SCR21)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLC mn1	SLC mn0	0	DLS mn2	DLS mn1	DLS mn0

PTC mn1	PTC mn0	Setting of parity bit in UART mode	
		Transmission	Reception
0	0	Does not output the parity bit.	Receives without parity
0	1	Outputs 0 parity Note.	No parity judgment
1	0	Outputs even parity.	Judged as even parity.
1	1	Outputs odd parity.	Judges as odd parity.
Be sure to set PTCmn1, PTCmn0 = 0, 0 in the CSI mode and simplified I^2C mode.			

DIR mn	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	Inputs/outputs data with LSB first.
Be sure to clear DIRmn = 0 in the simplified I^2C mode.	

SLC mn1	SLC mn0	Setting of stop bit in UART mode
0	0	No stop bit
0	1	Stop bit length = 1 bit
1	0	Stop bit length = 2 bits
1	1	Setting prohibited
When the transfer end interrupt is selected, the interrupt is generated when all stop bits have been completely transferred. Set 1 bit (SLCmn1, SLCmn0 = 0, 1) during UART reception and in the simplified I^2C mode. Set no stop bit (SLCmn1, SLCmn0 = 0, 0) in the CSI mode.		

Note 0 is always added regardless of the data contents.

Caution Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00 to 03, 10 to 13
78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00 to 03, 10 to 13
78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00 to 03, 10 to 13, 20, 21

Figure 14-8. Format of Serial Communication Operation Setting Register mn (SCRmn) (4/4)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), After reset: 0087H R/W
F0158H, F0159H (SCR10) to F015EH, F015FH (SCR13),
F020CH, F020DH (SCR20), F020EH, F020FH (SCR21)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLC mn1	SLC mn0	0	DLS mn2	DLS mn1	DLS mn0

DLS mn2	DLS mn1	DLS mn0	Setting of data length in CSI and UART modes
1	0	0	5-bit data length (stored in bits 0 to 4 of the SDRmn register) (settable in UART mode only)
1	1	0	7-bit data length (stored in bits 0 to 6 of the SDRmn register)
1	1	1	8-bit data length (stored in bits 0 to 7 of the SDRmn register)
Other than above			Setting prohibited
Be sure to set DLSmn0 = 1 in the simplified I^2C mode.			

Caution Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00 to 03, 10 to 13
78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00 to 03, 10 to 13
78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00 to 03, 10 to 13, 20, 21

(5) Higher 7 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 7 to 0 function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock (f_{MCK}).

If the CCSmn bit of serial mode register mn (SMRmn) is cleared to 0, the clock set by dividing the operating clock by the higher 7 bits of the SDRmn register is used as the transfer clock.

The lower 8 bits of the SDRmn register function as a transmit/receive buffer register. During reception, the parallel data converted by the shift register is stored in the lower 8 bits, and during transmission, the data to be transmitted to the shift register is set to the lower 8 bits.

The SDRmn register can be read or written in 16-bit units.

However, the higher 7 bits can be written or read only when the operation is stopped (SEmn = 0). During operation (SEmn = 1), a value is written only to the lower 8 bits of the SDRmn register. When the SDRmn register is read during operation, 0 is always read.

Reset signal generation clears the SDRmn register to 0000H.

Figure 14-9. Format of Serial Data Register mn (SDRmn) (1/2)

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01), FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03), FFF48H, FFF49H (SDR10), FFF4AH, FFF4BH (SDR11), FFF14H, FFF15H (SDR12), FFF16H, FFF17H (SDR13), FFF4CH, FFF4DH (SDR20), FFF4EH, FFF4FH (SDR21) After reset: 0000H R/W

FFF11H (SDR00) FFF10H (SDR00)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn								0								

SDRmn[15:9]							Transfer clock setting by dividing the operating clock (f_{MCK})
0	0	0	0	0	0	0	$f_{MCK}/2$
0	0	0	0	0	0	1	$f_{MCK}/4$
0	0	0	0	0	1	0	$f_{MCK}/6$
0	0	0	0	0	1	1	$f_{MCK}/8$
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	1	1	1	1	1	0	$f_{MCK}/254$
1	1	1	1	1	1	1	$f_{MCK}/256$

Cautions 1. Be sure to clear bit 8 to "0".

2. Setting SDRmn[15:9] = (0000000B, 0000001B) is prohibited when UART is used.

3. Setting SDRmn[15:9] = 0000000B is prohibited when simplified I^2C is used. Set SDRmn[15:9] to 0000001B or greater.

4. Do not write eight bits to the lower eight bits if operation is stopped (SEmn = 0). (If these bits are written to, the higher seven bits are cleared to 0.)

(**Remarks** are listed on the next page.)

Figure 14-9. Format of Serial Data Register mn (SDRmn) (2/2)

Remarks 1. For the function of the lower 8 bits of the SDRmn register, see **14.2 Configuration of Serial Array Unit**.

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 03
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 :	mn = 00 to 03, 10 to 13
78K0R/KF3-L μPD78F1027, 78F1028 :	mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L μPD78F1013, 78F1014 :	mn = 00 to 03, 10 to 13
78K0R/KG3-L μPD78F1029, 78F1030 :	mn = 00 to 03, 10 to 13, 20, 21

(6) Serial flag clear trigger register mn (SIRmn)

The SIRmn register is a trigger register that is used to clear each error flag of channel n.

When each bit (FECTmn, PECTmn, OVCTmn) of this register is set to 1, the corresponding bit (FEFmn, PEFmn, OVFmn) of serial status register mn is cleared to 0. Because the SIRmn register is a trigger register, it is cleared immediately when the corresponding bit of the SSRmn register is cleared.

The SIRmn register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SIRmn register can be set with an 8-bit memory manipulation instruction with SIRmnL.

Reset signal generation clears the SIRmn register to 0000H.

Figure 14-10. Format of Serial Flag Clear Trigger Register mn (SIRmn)

Address: F0108H, F0109H (SIR00) to F010EH, F010FH (SIR03), F0148H, F0149H (SIR10) to F014EH, F014FH (SIR13), F0204H, F0205H (SIR20) , F0206H, F0207H (SIR21) — After reset: 0000H — R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIRmn	0	0	0	0	0	0	0	0	0	0	0	0	0	FECTmn	PECTmn	OVCTmn

FECTmn	Clear trigger of framing error of channel n
0	Not cleared
1	Clears the FEFmn bit of the SSRmn register to 0.

PECTmn	Clear trigger of parity error flag of channel n
0	Not cleared
1	Clears the PEFmn bit of the SSRmn register to 0.

OVCTmn	Clear trigger of overrun error flag of channel n
0	Not cleared
1	Clears the OVFmn bit of the SSRmn register to 0.

Caution Be sure to clear bits 15 to 3 to "0".

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00 to 03, 10 to 13
78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00 to 03, 10 to 13
78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00 to 03, 10 to 13, 20, 21

2. When the SIRmn register is read, 0000H is always read.

(7) Serial status register mn (SSRmn)

The SSRmn register is a register that indicates the communication status and error occurrence status of channel n.
The errors indicated by this register are a framing error, parity error, and overrun error.
The SSRmn register can be read by a 16-bit memory manipulation instruction.
The lower 8 bits of the SSRmn register can be set with an 8-bit memory manipulation instruction with SSRmnL.
Reset signal generation clears the SSRmn register to 0000H.

Figure 14-11. Format of Serial Status Register mn (SSRmn) (1/2)

Address: F0100H, F0101H (SSR00) to F0106H, F0107H (SSR03), F0140H, F0141H (SSR10) to F0146H, F0147H (SSR13), F0200H, F0201H (SSR20), F0202H, F0203H (SSR21) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSRmn	0	0	0	0	0	0	0	0	0	TSF mn	BFF mn	0	0	FEF mn	PEF mn	OVF mn

TSF mn	Communication status indication flag of channel n
0	Communication is stopped or suspended.
1	Communication is in progress.
<Clear conditions> • The STmn bit of the STm register is set to 1 (communication is stopped) or the SSmn bit of the SSm register is set to 1 (communication is suspended). • Communication ends. <Set condition> • Communication starts.	

BFF mn	Buffer register status indication flag of channel n
0	Valid data is not stored in the SDRmn register.
1	Valid data is stored in the SDRmn register.
<Clear conditions> • Transferring transmit data from the SDRmn register to the shift register ends during transmission. • Reading receive data from the SDRmn register ends during reception. • The STmn bit of the STm register is set to 1 (communication is stopped) or the SSmn bit of the SSm register is set to 1 (communication is enabled). <Set conditions> • Transmit data is written to the SDRmn register while the TXEmn bit of the SCRmn register is set to 1 (transmission or transmission and reception mode in each communication mode). • Receive data is stored in the SDRmn register while the RXEmn bit of the SCRmn register is set to 1 (reception or transmission and reception mode in each communication mode). • A reception error occurs.	

Caution If data is written to the SDRmn register when BFFmn = 1, the transmit/receive data stored in the register is discarded and an overrun error (OVEmn = 1) is detected.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00 to 03, 10 to 13
78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00 to 03, 10 to 13
78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00 to 03, 10 to 13, 20, 21

Figure 14-11. Format of Serial Status Register mn (SSRmn) (2/2)

Address: F0100H, F0101H (SSR00) to F0106H, F0107H (SSR03), After reset: 0000H R
F0140H, F0141H (SSR10) to F0146H, F0147H (SSR13),
F0200H, F0201H (SSR20), F0202H, F0203H (SSR21)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSRmn	0	0	0	0	0	0	0	0	0	TSF mn	BFF mn	0	0	FEF mn	PEF mn	OVF mn

FEF mn	Framing error detection flag of channel n
0	No error occurs.
1	An error occurs (during UART reception).
<Clear condition> • 1 is written to the FECTmn bit of the SIRmn register. <Set condition> • A stop bit is not detected when UART reception ends.	

PEF mn	Parity error detection flag of channel n
0	No error occurs.
1	An error occurs (during UART reception) or ACK is not detected (during I^2C transmission).
<Clear condition> • 1 is written to the PECTmn bit of the SIRmn register. <Set condition> • The parity of the transmit data and the parity bit do not match when UART reception ends (parity error). • No ACK signal is returned from the slave channel at the ACK reception timing during I^2C transmission (ACK is not detected).	

OVF mn	Overrun error detection flag of channel n
0	No error occurs.
1	An error occurs
<Clear condition> • 1 is written to the OVCTmn bit of the SIRmn register. <Set condition> • Even though receive data is stored in the SDRmn register, that data is not read and transmit data or the next receive data is written while the RXEmn bit of the SCRmn register is set to 1 (reception or transmission and reception mode in each communication mode). • Transmit data is not ready for slave transmission or transmission and reception in CSI mode.	

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00 to 03, 10 to 13
78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00 to 03, 10 to 13
78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00 to 03, 10 to 13, 20, 21

(8) Serial channel start register m (SSm)

The SSm register is a trigger register that is used to enable starting communication/count by each channel.

When 1 is written a bit of this register (SSmn), the corresponding bit (SEmn) of serial channel enable status register m (SEm) is set to 1 (Operation is enabled). Because the SSmn bit is a trigger bit, it is cleared immediately when SEmn = 1.

The SSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSm register can be set with an 1-bit or 8-bit memory manipulation instruction with SSmL.

Reset signal generation clears the SSm register to 0000H.

Figure 14-12. Format of Serial Channel Start Register m (SSm)

Address: F0122H, F0123H (SS0), F0162H, F0163H (SS1), F0212H, F0213H (SS2) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 1	SSm2 Note 1	SSm1	SSm0

SSmn	Operation start trigger of channel n
0	No trigger operation
1	Sets the SEmn bit to 1 and enters the communication wait status Note 2.

Notes 1. Those bits are invalid while operating serial allay unit 2.

2. If a communication operation is already under execution, the operation is stopped.

Caution Be sure to clear bits 15 to 4 to "0".

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03

78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00 to 03, 10 to 13

78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00 to 03, 10 to 13, 20, 21

78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00 to 03, 10 to 13

78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00 to 03, 10 to 13, 20, 21

2. When the SSm register is read, 0000H is always read.

(9) Serial channel stop register m (STm)

The STm register is a trigger register that is used to enable stopping communication/count by each channel.

When 1 is written a bit of this register (STmn), the corresponding bit (SEmn) of serial channel enable status register m (SEm) is cleared to 0 (operation is stopped). Because the STmn bit is a trigger bit, it is cleared immediately when SEmn = 0.

The STm register can set written by a 16-bit memory manipulation instruction.

The lower 8 bits of the STm register can be set with an 1-bit or 8-bit memory manipulation instruction with STmL.

Reset signal generation clears the STm register to 0000H.

Figure 14-13. Format of Serial Channel Stop Register m (STm)

Address: F0124H, F0125H (ST0), F0164H, F0165H (ST1) After reset: 0000H R/W
F0214H, F0215H (ST2)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STm	0	0	0	0	0	0	0	0	0	0	0	0	STm3 Note 1	STm2 Note 1	STm1	STm0

STmn	Operation stop trigger of channel n
0	No trigger operation
1	Clears the SEmn bit to 0 and stops the communication operation Note 2.

Notes 1. Those bits are invalid while operating serial allay unit 2.

2. Communication stops while holding the value of the control register and shift register, and the status of the serial clock I/O pin, serial data output pin, and each error flag (FEFmn: framing error flag, PEFmn: parity error flag, OVFmn: overrun error flag).

Caution Be sure to clear bits 15 to 4 to "0".

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00 to 03, 10 to 13
78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00 to 03, 10 to 13
78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00 to 03, 10 to 13, 20, 21

2. When the STm register is read, 0000H is always read.

(10) Serial channel enable status register m (SEm)

The SEm register indicates whether data transmission/reception operation of each channel is enabled or stopped.

When 1 is written a bit of serial channel start register m (SSm), the corresponding bit of this register is set to 1.

When 1 is written a bit of serial channel stop register m (STm), the corresponding bit is cleared to 0.

Channel n that is enabled to operate cannot rewrite by software the value of the CKOmn bit (serial clock output of channel n) of serial output register m (SOm) to be described below, and a value reflected by a communication operation is output from the serial clock pin.

Channel n that stops operation can set the value of the CKOmn bit of the SOm register by software and output its value from the serial clock pin. In this way, any waveform, such as that of a start condition/stop condition, can be created by software.

The SEm register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the SEm register can be set with an 1-bit or 8-bit memory manipulation instruction with SEmL.

Reset signal generation clears the SEm register to 0000H.

Figure 14-14. Format of Serial Channel Enable Status Register m (SEm)

Address: F0120H, F0121H (SE0), F0160H, F0161H (SE1), F0210H, F0211H (SE2) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEm	0	0	0	0	0	0	0	0	0	0	0	0	SEm 3 Note	SEm 2 Note	SEm 1	SEm 0

SEm n	Indication of operation enable/stop status of channel n
0	Operation stops
1	Operation is enabled.

Note Those bits are invalid while operating serial allay unit 2.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03

78K0R/KF3-L μPD78F1010, 78F1011, 78F1012 : mn = 00 to 03, 10 to 13

78K0R/KF3-L μPD78F1027, 78F1028 : mn = 00 to 03, 10 to 13, 20, 21

78K0R/KG3-L μPD78F1013, 78F1014 : mn = 00 to 03, 10 to 13

78K0R/KG3-L μPD78F1029, 78F1030 : mn = 00 to 03, 10 to 13, 20, 21

(11) Serial output enable register m (SOEm)

The SOEm register is a register that is used to enable or stop output of the serial communication operation of each channel.

Channel n that enables serial output cannot rewrite by software the value of the SOmn bit of serial output register m (SOm) to be described below, and a value reflected by a communication operation is output from the serial data output pin.

For channel n, whose serial output is stopped, the SOmn bit value of the SOm register can be set by software, and that value can be output from the serial data output pin. In this way, any waveform of the start condition and stop condition can be created by software.

The SOEm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SOEm register can be set with an 1-bit or 8-bit memory manipulation instruction with SOEmL.

Reset signal generation clears the SOEm register to 0000H.

Figure 14-15. Format of Serial Output Enable Register m (SOEm)

Address: F012AH, F012BH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE02	SOE01	SOE00

Address: F016AH, F016BH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE1	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE12	0	SOE10

Address: F021AH, F021BH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE2 Note	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE21	SOE20

SOEmn	Serial output enable/stop of channel n
0	Stops output by serial communication operation.
1	Enables output by serial communication operation.

Note SOE2 register is only mounted in the 78K0R/KF3-L (μ PD78F1027, 78F1028) and 78K0R/KG3-L (μ PD78F1029, 78F1030).

Caution Be sure to clear bits 15 to 3 of the SOE0 register, bits 1 and 15 to 3 of the SOE1 register, and bits 15 to 2 of the SOE2 registers to "0".

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L μ PD78F1010, 78F1011, 78F1012 : mn = 00 to 02, 10, 12
78K0R/KF3-L μ PD78F1027, 78F1028 : mn = 00 to 02, 10, 12, 20, 21
78K0R/KG3-L μ PD78F1013, 78F1014 : mn = 00 to 02, 10, 12
78K0R/KG3-L μ PD78F1029, 78F1030 : mn = 00 to 02, 10, 12, 20, 21

(12) Serial output register m (SOm)

The SOm register is a buffer register for serial output of each channel.

The value of the SOmn bit of this register is output from the serial data output pin of channel n.

The value of the CKOmn bit of this register is output from the serial clock output pin of channel n.

The SOmn bit of this register can be rewritten by software only when serial output is disabled (SOEmn = 0). When serial output is enabled (SOEmn = 1), rewriting by software is ignored, and the value of the register can be changed only by a serial communication operation.

The CKOmn bit of this register can be rewritten by software only when the channel operation is stopped (SEmn = 0). While channel operation is enabled (SEmn = 1), rewriting by software is ignored, and the value of the CKOmn bit can be changed only by a serial communication operation.

When using the following pins as port function pins, set the corresponding CKOmn and SOmn bits to “1”.

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:

P30/SO10/TxD1, P31/SI10/RxD1/SDA10/INTP1, P32/$\overline{\text{SCK10}}$/SCL10/INTP2, P70/KR0/SO01/INTP4, P72/KR2/$\overline{\text{SCK01}}$/INTP6, P73/KR3/SO00/TxD0, P75/KR5/$\overline{\text{SCK00}}$

78K0R/KF3-L, 78K0R/KG3-L:

P02/SO10/TxD1, P03/SI10/SDA10/RxD1, P04/$\overline{\text{SCK10}}$/SCL10, P10/$\overline{\text{SCK00}}$, P12/SO00/TxD0, P13/TxD3, P43/$\overline{\text{SCK01}}$, P45/SO01, P142/$\overline{\text{SCK20}}$/SCL20, P143/SI20/SDA20/RxD2, P144/SO20/TxD2

μPD78F1027, 78F1028:

P02/SO10/TxD1, P03/SI10/SDA10/RxD1, P04/$\overline{\text{SCK10}}$/SCL10, P10/$\overline{\text{SCK00}}$, P12/SO00/TxD0, P13/TxD3, P43/$\overline{\text{SCK01}}$, P45/SO01, P50/$\overline{\text{SCK40}}$/INTP1, P52/SO40/TxD4/TO00, P53/$\overline{\text{SCK41}}$/TI00, P55/SO41/PCLBUZ1/INTP7, P142/$\overline{\text{SCK20}}$/SCL20, P143/SI20/SDA20/RxD2, P144/SO20/TxD2

μPD78F1029, 78F1030:

P02/SO10/TxD1, P03/SI10/SDA10/RxD1, P04/$\overline{\text{SCK10}}$/SCL10, P10/$\overline{\text{SCK00}}$, P12/SO00/TxD0, P13/TxD3, P43/$\overline{\text{SCK01}}$, P45/SO01, P50/$\overline{\text{SCK40}}$, P52/SO40/TxD4, P53/$\overline{\text{SCK41}}$, P55/SO41, P142/$\overline{\text{SCK20}}$/SCL20, P143/SI20/SDA20/RxD2, P144/SO20/TxD2

The SOm register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears the SOm register to 0F0FH.

Figure 14-16. Format of Serial Output Register m (SOm)

Address: F0128H, F0129H After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	1	CKO 02	CKO 01	CKO 00	0	0	0	0	1	SO 02	SO 01	SO 00

Address: F0168H, F0169H After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	1	1	1	CKO 10	0	0	0	0	1	SO 12	1	SO 10

Address: F0218H, F0219H After reset: 0303H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO2 Note	0	0	0	0	1	1	CKO 21	CKO 20	0	0	0	0	1	1	SO 21	SO 20

CKO mn	Serial clock output of channel n
0	Serial clock output value is “0”.
1	Serial clock output value is “1”.

SO mn	Serial data output of channel n
0	Serial data output value is “0”.
1	Serial data output value is “1”.

Note SO2 register is only mounted in the 78K0R/KF3-L (μ PD78F1027, 78F1028) and 78K0R/KG3-L (μ PD78F1029, 78F1030).

Caution Be sure to set bits 11 and 3 of the SO0 register, bits 11 to 9, 3, and 1 of the SO1 register, and bits 11, 10, 3, and 2 of the SO2 register to “1”. And be sure to clear bits 15 to 12 and 7 to 4 of the SOm register to “0”.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L (μ PD78F1010, 78F1011, 78F1012) : mn = 00 to 02, 10, 12
78K0R/KF3-L (μ PD78F1027, 78F1028) : mn = 00 to 02, 10, 12, 20, 21
78K0R/KG3-L (μ PD78F1013, 78F1014) : mn = 00 to 02, 10, 12
78K0R/KG3-L (μ PD78F1029, 78F1030) : mn = 00 to 02, 10, 12, 20, 21

(13) Serial output level register m (SOLm)

The SOLm register is a register that is used to set inversion of the data output level of each channel.

This register can be set only in the UART mode. Be sure to set 0000H in the CSI mode and simplifies I^2C mode.

Inverting channel n by using this register is reflected on pin output only when serial output is enabled (SOEmn = 1). When serial output is disabled (SOEmn = 0), the value of the SOmn bit is output as is.

Rewriting the SOLm register is prohibited when the register is in operation (when SEmn = 1).

The SOLm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SOLm register can be set with an 8-bit memory manipulation instruction with SOLmL.

Reset signal generation clears the SOLm register to 0000H.

Figure 14-17. Format of Serial Output Level Register m (SOLm)

Address: F0134H, F0135H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOL0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOL02	0	SOL00

Address: F0174H, F0175H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOL1	0	0	0	0	0	0	0	0	0	0	0	0	0	SOL12	0	SOL10

Address: F0220H, F0221H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOL2 Note	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOL20

SOLmn	Selects inversion of the level of the transmit data of channel n in UART mode
0	Communication data is output as is.
1	Communication data is inverted and output.

Note SOL2 register is only mounted in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

Caution Be sure to clear bits 15 to 3, and 1 of the SOL0 and SOL1 registers, bits 15 to 1 of the SOL2 register to "0".

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012) : mn = 00 to 02, 10, 12
78K0R/KF3-L (μPD78F1027, 78F1028) : mn = 00 to 02, 10, 12, 20
78K0R/KG3-L (μPD78F1013, 78F1014) : mn = 00 to 02, 10, 12
78K0R/KG3-L (μPD78F1029, 78F1030) : mn = 00 to 02, 10, 12, 20

(14) Input switch control register (ISC)

The ISC1 and ISC0 bits of the ISC register are used to realize a LIN-bus communication operation by UARTk in coordination with an external interrupt and the timer array unit 0.

When bit 0 is set to 1, the input signal of the serial data input (RxDk) pin is selected as an external interrupt (INTP0) that can be used to detect a wakeup signal.

When bit 1 is set to 1, the input signal of the serial data input (RxDk) pin is selected as a timer input, so that wake up signal can be detected, the low width of the sync break field, and the pulse width of the sync field can be measured by the timer.

The ISC2 bit is set to select the P52/SLTI/SLTO pin as the timer I/O pin of timer channels 0 and 1 (78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, 78K0R/KE3-L only).

The ISC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the ISC register to 00H.

Figure 14-18. Format of Input Switch Control Register (ISC)

Address: FFF3CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	0	0	0	ISC2 Note 1	ISC1	ISC0

ISC2 Note 1	Selecting P52/SLTI/SLTO Pin as Timer I/O Pin			
	Channel 0		Channel 1	
	Input pin	Output pin	Input pin	Output pin
0	P00/TI00 Note 2	P01/TO00 Note 2	P52/SLTI	P52/SLTO
1	P52/SLTI	P52/SLTO	–	–
Other than the above	Setting prohibited			

ISC1	Switching channel 7 input of timer array unit 0
0	Uses the input signal of the TI07 pin as a timer input (normal operation).
1	Input signal of the RxDk pin is used as timer input (detects the wakeup signal and measures the low width of the sync break field and the pulse width of the sync field).

ISC0	Switching external interrupt (INTP0) input
0	Uses the input signal of the INTP0 pin as an external interrupt (normal operation).
1	Uses the input signal of the RxDk pin as an external interrupt (detects the wakeup signal).

Notes 1. 78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, 78K0R/KE3-L only.

2. 78K0R/KD3-L and 78K0R/KE3-L only. Only the P52/SLTI/SLTO pin can be assigned to channels 0 and 1 in the 78K0R/KC3-L (44-pin, 48-pin).

Caution Be sure to clear bits 7 to 3 to "0" in the 78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, and 78K0R/KE3-L. Be sure to clear bits 7 to 2 to "0" in the 78K0R/KC3-L (40-pin).
Be sure to clear bits 7 to 2 to "0" in the 78K0R/KF3-L and 78K0R/KG3-L.

Remark 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: k = 0 (RxD0)
78K0R/KF3-L, 78K0R/KG3-L: k = 3 (RxD3)

(15) Noise filter enable register 0 (NFEN0)

The NFEN0 register is used to set whether the noise filter can be used for the input signal from the serial data input pin to each channel.

Disable the noise filter of the pin used for CSI or simplified I^2C communication, by clearing the corresponding bit of this register to 0.

Enable the noise filter of the pin used for UART communication, by setting the corresponding bit of this register to 1.

When the noise filter is enabled, CPU/ peripheral hardware clock (f_{CLK}) is synchronized with 2-clock match detection.

The NFEN0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the NFEN0 register to 00H.

Figure 14-19. Format of Noise Filter Enable Register 0 (NFEN0) (1/2)

Address: F0060H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN0	0	SNFEN30 Note 1	0	SNFEN20 Note 1	0	SNFEN10	SNFEN40 Note 2	SNFEN00

SNFEN40	Use of noise filter of RxD4 pin (RxD4/SI40/INTP2/P51 Note 2)
0	Noise filter OFF
1	Noise filter ON
Set SNFEN40 to 1 to use the RxD4 pin. Clear SNFEN40 to 0 to use the other than RxD4 pin.	

SNFEN30 Note 1	Use of noise filter of RxD3 pin (RxD3/P14)
0	Noise filter OFF
1	Noise filter ON
Set SNFEN30 to 1 to use the RxD3 pin. Clear SNFEN30 to 0 to use the other than RxD3 pin.	

SNFEN20 Note 1	Use of noise filter of RxD2 pin (RxD2/SDA20/SI20/P143)
0	Noise filter OFF
1	Noise filter ON
Set SNFEN20 to 1 to use the RxD2 pin. Clear SNFEN20 to 0 to use the other than RxD2 pin.	

SNFEN10	Use of noise filter of RxD1 pin 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: RxD1/SDA10/SI10/INTP1/P31 pin 78K0R/KF3-L, 78K0R/KG3-L: RxD1/SDA10/SI10/P03 pin
0	Noise filter OFF
1	Noise filter ON
Set the SNFEN10 bit to 1 to use the RxD1 pin. Clear the SNFEN10 bit to 0 to use the other than RxD1 pin.	

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. 78K0R/KF3-L (μPD78F1027, 78F1028), 78K0R/KG3-L (μPD78F1029, 78F1030) only.

Caution Be sure to clear bits 7 to 3, and 1 to "0" in the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L. Be sure to clear bits 7, 5, 3, and 1 to "0" in the 78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012) and 78K0R/KG3-L (μPD78F1013, 78F1014). Be sure to clear bits 7, 5, and 3 to "0" in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

Figure 14-19. Format of Noise Filter Enable Register 0 (NFEN0) (1/2)

Address: F0060H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN0	0	SNFEN30[Note 1]	0	SNFEN20[Note 1]	0	SNFEN10	SNFEN40[Note 2]	SNFEN00

SNFEN00	Use of noise filter of RxD0 pin 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: RxD0/SI00/KR4/P74 pin 78K0R/KF3-L, 78K0R/KG3-L: RxD0/SI00/P11 pin
0	Noise filter OFF
1	Noise filter ON
Set the SNFEN00 bit to 1 to use the RxD0 pin. Clear the SNFEN00 bit to 0 to use the other than RxD0 pin.	

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. 78K0R/KF3-L (μPD78F1027, 78F1028), 78K0R/KG3-L (μPD78F1029, 78F1030) only.

Caution Be sure to clear bits 7 to 3, and 1 to "0" in the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L. Be sure to clear bits 7, 5, 3, and 1 to "0" in the 78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012) and 78K0R/KG3-L (μPD78F1013, 78F1014). Be sure to clear bits 7, 5, and 3 to "0" in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

(16) Port input mode registers 0, 1, 3, 7, 14 (PIM0, PIM1, PIM3, PIM7, PIM14)

These registers set the input buffer of ports 0, 1, 3, 7, and 14 in 1-bit units.

The port input mode registers to be set differ depending on the product.

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: PIM3, PIM7

78K0R/KF3-L, 78K0R/KG3-L: PIM0, PIM1, PIM14

The PIM0, PIM1, PIM3, PIM7, and PIM14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the PIM0, PIM1, PIM3, PIM7, and PIM14 registers to 00H.

Figure 14-20. Format of Port Input Mode Registers 3 and 7 (PIM3 and PIM7)
(78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

Address F0043H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM3	0	0	0	0	0	PIM32	PIM31	0

Address F0047H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM7	0	0	PIM75	PIM74	0	PIM72	PIM71	0

PIMmn	Pmn pin input buffer selection (m = 3, 7; n = 1, 2, 4, 5)
0	Normal input buffer
1	TTL input buffer

Figure 14-21. Format of Port Input Mode Registers 0, 1, and 14 (PIM0, PIM1, PIM14)
(78K0R/KF3-L, 78K0R/KG3-L)

Address F0040H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM0	0	0	0	PIM04	PIM03	0	0	0

Address F0041H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM1	0	0	0	0	0	0	PIM11	PIM10

Address F004EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM14	0	0	0	0	PIM143	PIM142	0	0

PIMmn	Pmn pin input buffer selection (m = 0, 1, 14; n = 0 to 4)
0	Normal input buffer
1	TTL input buffer

(17) Port output mode registers 0, 1, 3, 7, 14 (POM0, POM1, POM3, POM7, POM14)

These registers set the output mode of ports 0, 1, 3, 7, and 14 in 1-bit units.

The port output mode registers to be set differ depending on the product.

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: POM3, POM7
78K0R/KF3-L, 78K0R/KG3-L: POM0, POM1, POM14

The POM0, POM1, POM3, POM7, and POM14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the POM0, POM1, POM3, POM7, and POM14 registers to 00H.

Figure 14-22. Format of Port Output Mode Registers 3 and 7 (POM3 and POM7)
(78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

Address F0053H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
POM3	0	0	0	0	0	POM32	POM31	POM30

Address F0057H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
POM7	0	0	POM75	0	POM73	POM72	0	POM70

POMmn	Pmn pin output buffer selection (m = 3, 7; n = 0 to 3, 5)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance) mode

Figure 14-23. Format of Port Output Mode Registers 0, 1, and 14 (POM0, POM1, POM14)
(78K0R/KF3-L, 78K0R/KG3-L)

Address F0050H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
POM0	0	0	0	POM04	POM03	POM02	0	0

Address F0051H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
POM1	0	0	0	0	0	POM12	0	POM10

Address F005EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
POM14	0	0	0	POM144	POM143	POM142	0	0

POMmn	Pmn pin output buffer selection (m = 0, 1, 14; n = 0, 2 to 4)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance) mode

(18) Port mode registers 0, 1, 3, 4, 5, 7, and 14 (PM0, PM1, PM3, PM4, PM5, PM7, PM14)

These registers set input/output of ports 0, 1, 3, 4, 5, 7, and 14 in 1-bit units.

The port pins that are shared with the serial data I/O pin or serial clock output I/O pin differ depending on the product. When using the serial array unit, set the following port mode registers according to the product used.

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L	: PM3, PM7
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012)	: PM0, PM1, PM4, PM14
78K0R/KF3-L (μPD78F1027, 78F1028)	: PM0, PM1, PM4, PM5, PM14
78K0R/KG3-L (μPD78F1013, 78F1014)	: PM0, PM1, PM4, PM14
78K0R/KF3-L (μPD78F1029, 78F1030)	: PM0, PM1, PM4, PM5, PM14

When using the ports (such as P30/SO10/TxD1, P31/SI10/RxD1/SDA10/INTP1) to be shared with the serial data output pin or serial clock output pin for serial data output or serial clock output, set the port mode register (PMxx) bit corresponding to each port to 0. And set the port register (Pxx) bit corresponding to each port to 1

Example: When using P30/SO10/TxD1 for serial data output or serial clock output
Set the PM30 bit of the port mode register 3 to 0.
Set the P30 bit of the port register 3 to 0.

When using the ports (such as P31/SI10/RxD1/SDA10/INTP1, P32/$\overline{\text{SCK10}}$/SCL10/INTP2) to be shared with the serial data input pin or serial clock input pin for serial data input or serial clock input, set the port mode register (PMxx) bit corresponding to each port to 1. At this time, the port register (Pxx) bit may be 0 or 1.

Example: When using P31/SI10/RxD1/SDA10/INTP1 for serial data input or serial clock input
Set the PM31 bit of port mode register 3 to 1.
Set the P31 bit of port register 3 to 0 or 1.

The PM0, PM1, PM3, PM4, PM5, PM7, and PM14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the PM0, PM1, PM3, PM4, PM5, PM7, and PM14 registers to FFH.

Figure 14-24. Format of Port Mode Registers 3 and 7 (PM3 and PM7)
(78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

Address: FFF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	1	PM32	PM31	PM30

Address: FFF27H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM7	1	1	PM75	PM74	PM73	PM72	PM71	PM70

PMmn	Pmn pin I/O mode selection (m = 3, 7; n = 0 to 5)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 14-25. Format of Port Mode Registers 0, 1, 4, 5, and 14 (PM0, PM1, PM4, PM5, PM14)
(78K0R/KF3-L, 78K0R/KG3-L)

Address: FFF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01 Note	PM00 Note

Address: FFF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40

Address: FFF25H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM5	PM57 Note	PM56 Note	PM55	PM54	PM53	PM52	PM51	PM50

Address: FFF2EH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM14	1	1	PM145 Note	PM144	PM143	PM142	PM141 Note	PM140

PMmn	Pmn pin I/O mode selection (m = 0, 1, 4, 14; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note 78K0R/KG3-L only.

14.4 Operation stop mode

Each serial interface of serial array unit has the operation stop mode.

In this mode, serial communication cannot be executed, thus reducing the power consumption.

In addition, the following pins can be used as port function pins in this mode.

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:

P30/SO10/TxD1, P31/SI10/RxD1/SDA10/INTP1, P32/$\overline{\text{SCK10}}$/SCL10/INTP2, P70/KR0/SO01/INTP4, P71/KR1/SI01/INTP5, P72/KR2/$\overline{\text{SCK01}}$/INTP6, P73/KR3/SO00/TxD0, P74/KR4/SI00/RxD0, P75/KR5/$\overline{\text{SCK00}}$

78K0R/KF3-L, 78K0R/KG3-L:

P02/SO10/TxD1, P03/SI10/SDA10/RxD1, P04/$\overline{\text{SCK10}}$/SCL10, P10/$\overline{\text{SCK00}}$, P11/SI00/RxD0, P12/SO00/TxD0, P13/TxD3, P14/RxD3, P43/$\overline{\text{SCK01}}$, P44/SI01, P45/SO01, P142/$\overline{\text{SCK20}}$/SCL20, P143/SI20/SDA20/RxD2, P144/SO20/TxD2

μPD78F1027, 78F1028

P02/SO10/TxD1, P03/SI10/SDA10/RxD1, P04/$\overline{\text{SCK10}}$/SCL10, P10/$\overline{\text{SCK00}}$, P11/SI00/RxD0, P12/SO00/TxD0, P13/TxD3, P14/RxD3, P43/$\overline{\text{SCK01}}$, P44/SI01, P45/SO01, P50/$\overline{\text{SCK40}}$/INTP1,P51/SI40/RxD4/INTP2, P52/SO40/TxD4/TO00, P53/$\overline{\text{SCK41}}$/TI00, P54/SI41/TI07/TO07, P55/SO41/PCLBUZ1/INTP7, P142/$\overline{\text{SCK20}}$/SCL20, P143/SI20/SDA20/RxD2, P144/SO20/TxD2

μPD78F1029, 78F1030

P02/SO10/TxD1, P03/SI10/SDA10/RxD1, P04/$\overline{\text{SCK10}}$/SCL10, P10/$\overline{\text{SCK00}}$, P11/SI00/RxD0, P12/SO00/TxD0, P13/TxD3, P14/RxD3, P43/$\overline{\text{SCK01}}$, P44/SI01, P45/SO01, P50/$\overline{\text{SCK40}}$, P51/SI40/RxD4, P52/SO40/TxD4, P53/$\overline{\text{SCK41}}$, P54/SI41, P55/SO41, P142/$\overline{\text{SCK20}}$/SCL20, P143/SI20/SDA20/RxD2, P144/SO20/TxD2

14.4.1 Stopping the operation by units

The stopping of the operation by units is set by using peripheral enable registers 0 and 1 (PER0, PER1).

The PER0 register and the PER1 register are used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

To stop the operation of serial array unit 0, clear bit 2 (SAU0EN) of the PER0 register to 0. In the 78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012) and 78K0R/KG3-L (μPD78F1013, 78F1014), to stop the operation of serial array unit 1, clear bit 3 (SAU1EN) of the PER0 register to 0.

Furthermore, in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030), to stop the operation of serial array unit 2, clear bit 0 (SAU2EN) of the PER1 register to 0.

Figure 14-26. Peripheral Enable Register 0 (PER0) Setting When Stopping the Operation by Units

(a) Peripheral enable register 0 (PER0) … Set only the bit of SAUm to be stopped to 0.

	7	6	5	4	3	2	1	0
PER0	RTCEN Note 1		ADCEN	IICAEN Note 2	SAU1EN Note 3	SAU0EN	TAU1EN Note 3	TAU0EN Note 3
	×	0	×	×	0/1	0/1	×	×

Control of SAUm input clock
0: Stops supply of input clock
1: Supplies input clock

Notes 1. That is not provided in 40-pin product of the 78K0R/KC3-L.

2. That is not provided in 40-pin and 44-pin products of the 78K0R/KC3-L.

3. 78K0R/KF3-L and 78K0R/KG3-L only.

(b) Peripheral enable register 1 (PER1) … Set only the bit of SAU2 to be stopped to 0.

	7	6	5	4	3	2	1	0
PER1								SAU2EN
	0	0	0	0	0	0	0	0/1

Control of SAU2 input clock
0: Stops supply of input clock
1: Supplies input clock

Cautions 1. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read
Note that this does not apply to the following registers.
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:
ISC, NFEN0, PIM3, PIM7, POM3, POM7, PM3, PM7, P3, and P7 registers.
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012), 78K0R/KG3-L (μPD78F1013, 78F1014):
ISC, NFEN0, PIM0, PIM1, PIM14, POM0, POM1, POM14, PM0, PM1, PM4, PM14, P0, P1, P4, and P14 registers.
78K0R/KF3-L (μPD78F1027, 78F1028), 78K0R/KG3-L (μPD78F1029, 78F1030):
ISC, NFEN0, PIM0, PIM1, PIM14, POM0, POM1, POM14, PM0, PM1, PM4, PM5, PM14, P0, P1, P4, P5, and P14 registers.

(**Caution 2** and **Remark** is listed on the next page.)

Cautions 2. Be sure to clear the following bits to 0.

48-pin product of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	**bits 0, 1, 3, 6 of PER0 register**
44-pin product of the 78K0R/KC3-L:	**bits 0, 1, 3, 4, 6 of PER0 register**
40-pin product of the 78K0R/KC3-L:	**bits 0, 1, 3, 4, 6, 7 of PER0 register**
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	**bit 6 of PER0 register**
78K0R/KF3-L (μPD78F1027, 78F1028):	**bit 6 of PER0 register, bits 1 to 7 of PER1 register**
78K0R/KG3-L (μPD78F1013, 78F1014):	**bit 6 of PER0 register**
78K0R/KG3-L (μPD78F1029, 78F1030):	**bit 6 of PER0 register, bits 1 to 7 of PER1 register**

Remarks 1. ☐ : Setting disabled (fixed by hardware)

×: Bits not used with serial array units (depending on the settings of other peripheral functions)

0/1: Set to 0 or 1 depending on the usage of the user

2. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: m = 0

78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): m = 0, 1

78K0R/KF3-L (μPD78F1027, 78F1028): m = 0 to 2

78K0R/KG3-L (μPD78F1013, 78F1014): m = 0, 1

78K0R/KF3-L (μPD78F1029, 78F1030): m = 0 to 2

14.4.2 Stopping the operation by channels

The stopping of the operation by channels is set using each of the following registers.

Figure 14-27. Each Register Setting When Stopping the Operation by Channels (1/2)

(a) Serial channel stop register m (STm) … This register is a trigger register that is used to enable stopping communication/count by each channel.

STm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	STm3 Note 0/1	STm2 Note 0/1	STm1 0/1	STm0 0/1

1: Clears the SEmn bit to 0 and stops the communication operation

* Because the STmn bit is a trigger bit, it is cleared immediately when Semn = 0.

(b) Serial Channel Enable Status Register m (SEm) … This register indicates whether data transmission/reception operation of each channel is enabled or stopped.

SEm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SEm3 Note 0/1	SEm2 Note 0/1	SEm1 0/1	SEm0 0/1

0: Operation stops

* The SEm register is a read-only status register, whose operation is stopped by using the STm register. With a channel whose operation is stopped, the value of the CKOmn bit of the SOm register can be set by software.

(c) Serial output enable register m (SOEm) … This register is a register that is used to enable or stop output of the serial communication operation of each channel.

SOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	SOE02 0/1	SOE01 0/1	SOE00 0/1

0: Stops output by serial communication operation

* For channel n, whose serial output is stopped, the SO0n bit value of the SO0 register can be set by software.

SOE1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	SOE12 0/1	0	SOE10 0/1

0: Stops output by serial communication operation

* For channel n, whose serial output is stopped, the SO10 and SO12 bits value of the SO1 register can be set by software.

SOE2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE21 0/1	SOE20 0/1

0: Stops output by serial communication operation

* For channel n, whose serial output is stopped, the SO20, SO21 bits value of the SO2 register can be set by software.

Note Those bits are invalid while operating serial allay unit 2.

(**Remark** is listed on the next page.)

Figure 14-27. Each Register Setting When Stopping the Operation by Channels (2/2)

(d) Serial output register m (SOm) …This register is a buffer register for serial output of each channel.

SO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	CKO02 0/1	CKO01 0/1	CKO00 0/1	0	0	0	0	1	SO02 0/1	SO01 0/1	SO00 0/1

1: Serial clock output value is “1” 1: Serial data output value is “1”

* When using pins corresponding to each channel as port function pins, set the corresponding CKO0n and SO0n bits to “1”.

SO1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	CKO10 0/1	0	0	0	0	1	SO12 0/1	1	SO10 0/1

1: Serial clock output value is “1” 1: Serial data output value is “1”

* When using pins corresponding to each channel as port function pins, set the corresponding CKO10, SO12 and SO10 bits to “1”.

SO2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	CKO21 0/1	CKO20 0/1	0	0	0	0	1	1	SO21 0/1	SO20 0/1

1: Serial clock output value is “1” 1: Serial data output value is “1”

* When using pins corresponding to each channel as port function pins, set the corresponding CKO21, CKO20, SO21 and SO20 bits to “1”.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L (μ PD78F1010, 78F1011, 78F1012) : mn = 00 to 03, 10 to 13
78K0R/KF3-L (μ PD78F1027, 78F1028) : mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L (μ PD78F1013, 78F1014) : mn = 00 to 03, 10 to 13
78K0R/KG3-L (μ PD78F1029, 78F1030) : mn = 00 to 03, 10 to 13, 20, 21

2. ☐ : Setting disabled (fixed by hardware), 0/1: Set to 0 or 1 depending on the usage of the user

14.5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) Communication

This is a clocked communication function that uses three lines: serial clock ($\overline{SCK}$) and serial data (SI and SO) lines.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

  During master communication: Max. $f_{CLK}/4$, during slave communication: Max. $f_{MCK}/6$ Note

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

Note Use the clocks within a range satisfying the $\overline{SCK}$ cycle time (t_{KCY}) characteristics (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

The channels supporting 3-wire serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) are channels 0 to 2 of SAU0, channel 0 of SAU1 (78K0R/KF3-L, 78K0R/KG3-L only), and channel 0 and 1 of SAU2 (78K0R/KF3-L (μPD78F1027, 78F1028), 78K0R/KG3-L (μPD78F1029, 78F1030) only).

- 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0 (supporting LIN-bus)	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–

- 78K0R/KF3-L, 78K0R/KG3-L

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	CSI20	UART2	IIC20
	1	–		–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–
2 Note	0	CSI40	UART4	–
	1	CSI41		–

Note Serial array unit 2 is only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

3-wire serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) performs the following six types of communication operations.

- Master transmission (See **14.5.1**.)
- Master reception (See **14.5.2**.)
- Master transmission/reception (See **14.5.3**.)
- Slave transmission (See **14.5.4**.)
- Slave reception (See **14.5.5**.)
- Slave transmission/reception (See **14.5.6**.)

14.5.1 Master transmission

Master transmission is that the 78K0R/Kx3-L outputs a transfer clock and transmits data to another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20 Note 1	CSI40 Note 2	CSI41 Note 2
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1	Channel 0 of SAU2	Channel 1 of SAU2
Pins used	$\overline{\text{SCK00}}$, SO00	$\overline{\text{SCK01}}$, SO01	$\overline{\text{SCK10}}$, SO10	$\overline{\text{SCK20}}$, SO20	$\overline{\text{SCK40}}$, SO40	$\overline{\text{SCK41}}$, SO41
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20	INTCSI40	INTCSI41
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.					
Error detection flag	None					
Transfer data length	7 or 8 bits					
Transfer rate	Max. $f_{CLK}/4$ [Hz], Min. $f_{CLK}/(2 \times 2^{11} \times 128)$ [Hz] Note 3 f_{CLK}: System clock frequency					
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data output starts from the start of the operation of the serial clock. • DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Forward • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. CSI40 and CSI41 are only mounted in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

3. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

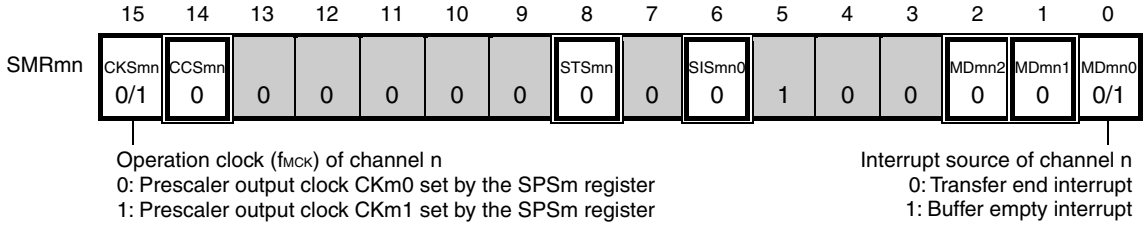
Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21

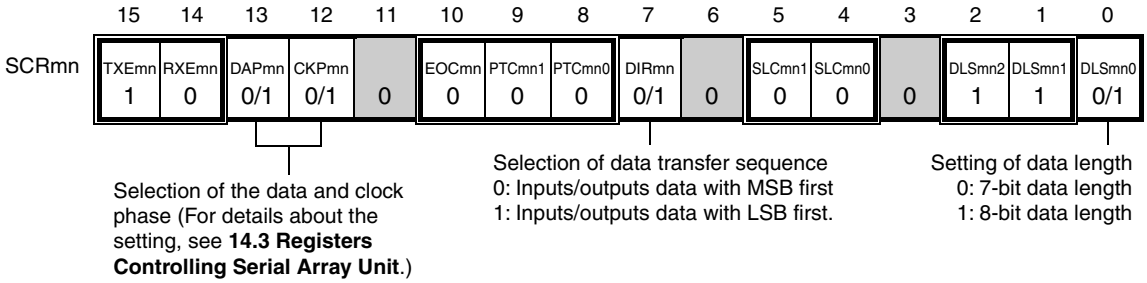
(1) Register setting

Figure 14-28. Example of Contents of Registers for Master Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (1/2)

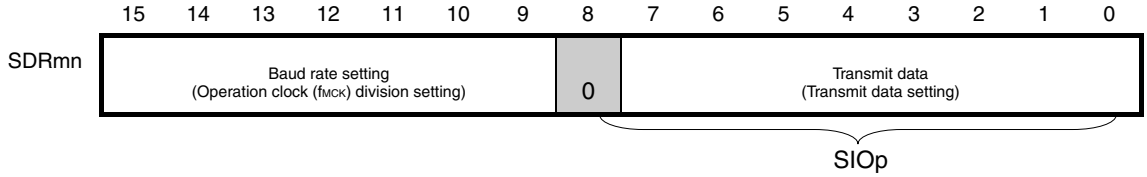
(a) Serial mode register mn (SMRmn)



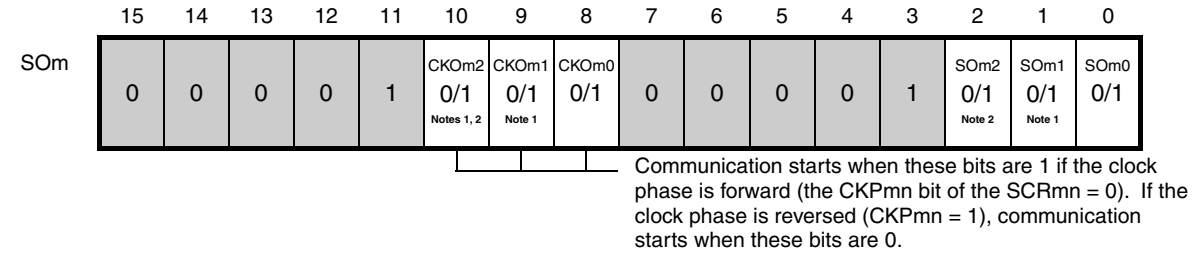
(b) Serial communication operation setting register mn (SCRmn)



(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOm) … Sets only the bits of the target channel.



Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

(**Remark** is listed on the next page.)

Figure 14-28. Example of Contents of Registers for Master Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (2/2)

(e) Serial output enable register m (SOEm) … Sets only the bits of the target channel to 1.

SOEm	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 0/1 Note 2	SOEm1 0/1 Note 1	SOEm0 0/1

(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

<R>

SSm	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 2	SSm1 0/1	SSm0 0/1

Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

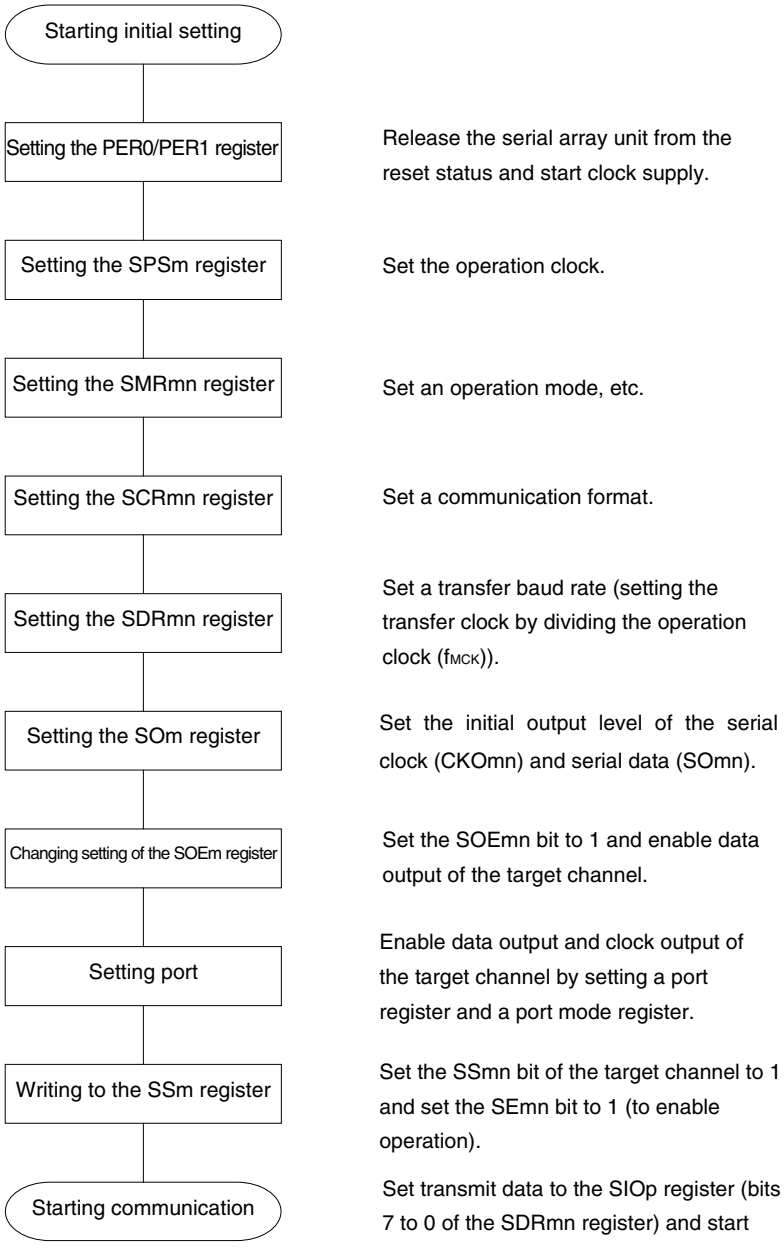
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

2. □: Setting is fixed in the CSI master transmission mode, ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

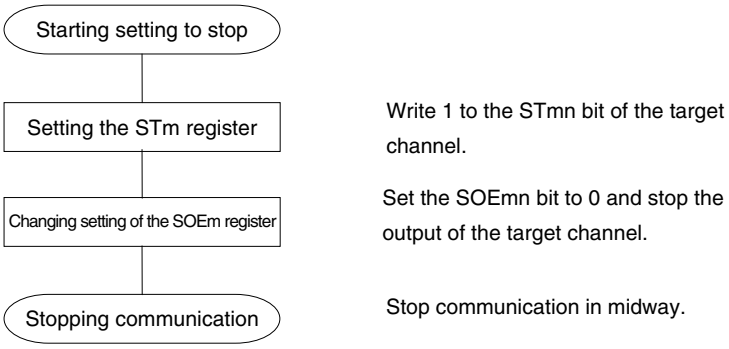
(2) Operation procedure

Figure 14-29. Initial Setting Procedure for Master Transmission



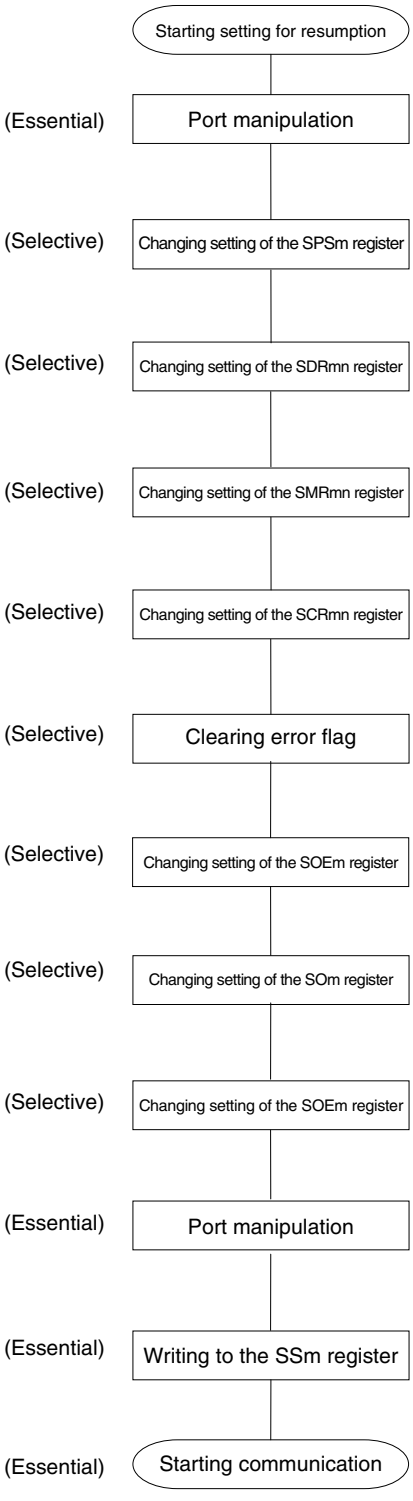
Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Figure 14-30. Procedure for Stopping Master Transmission



Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set serial output register m (SOm) (see **Figure 14-31 Procedure for Resuming Master Transmission**).

Figure 14-31. Procedure for Resuming Master Transmission



Disable data output and clock output of the target channel by setting a port register and a port mode register.

Re-set the register to change the operation clock setting.

Re-set the register to change the transfer baud rate setting (setting the transfer clock by dividing the operation clock (f_{MCK})).

Re-set the register to change serial mode register mn (SMRmn) setting.

Re-set the register to change serial communication operation setting register mn (SCRmn) setting.

If the FEF, PEF, and OVF flags remain set, clear them using serial flag clear trigger register mn (SIRmn).

Set the SOEmn bit to 0 to stop output from the target channel.

Set the initial output level of the serial clock (CKOmn) and serial data (SOmn).

Set the SOEmn bit to 1 and enable output from the target channel.

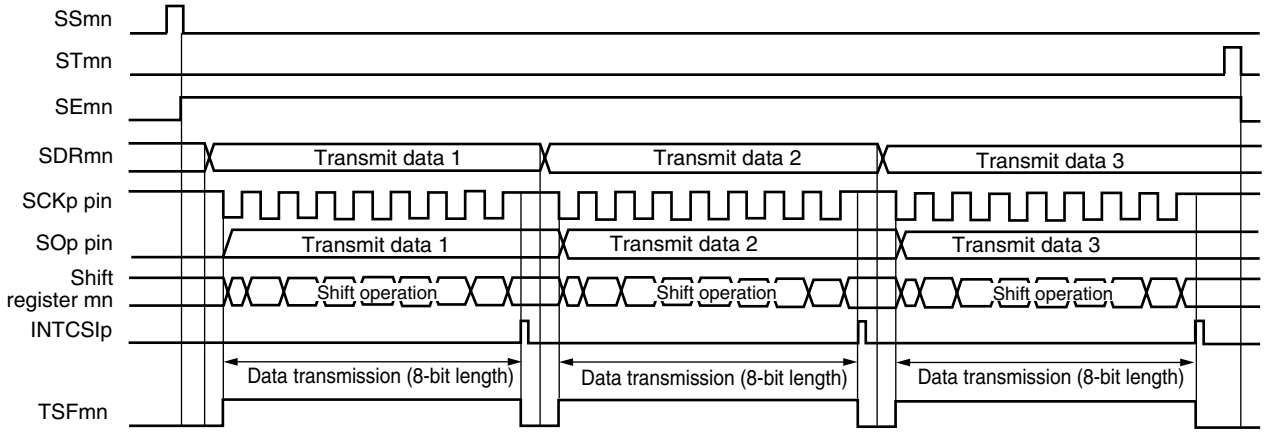
Enable data output and clock output of the target channel by setting a port register and a port mode register.

Set the SSmn bit of the target channel to 1 and set the SEmn bit to 1 (to enable operation).

Sets transmit data to the SIOp register (bits 7 to 0 of the SDRmn register) and start communication.

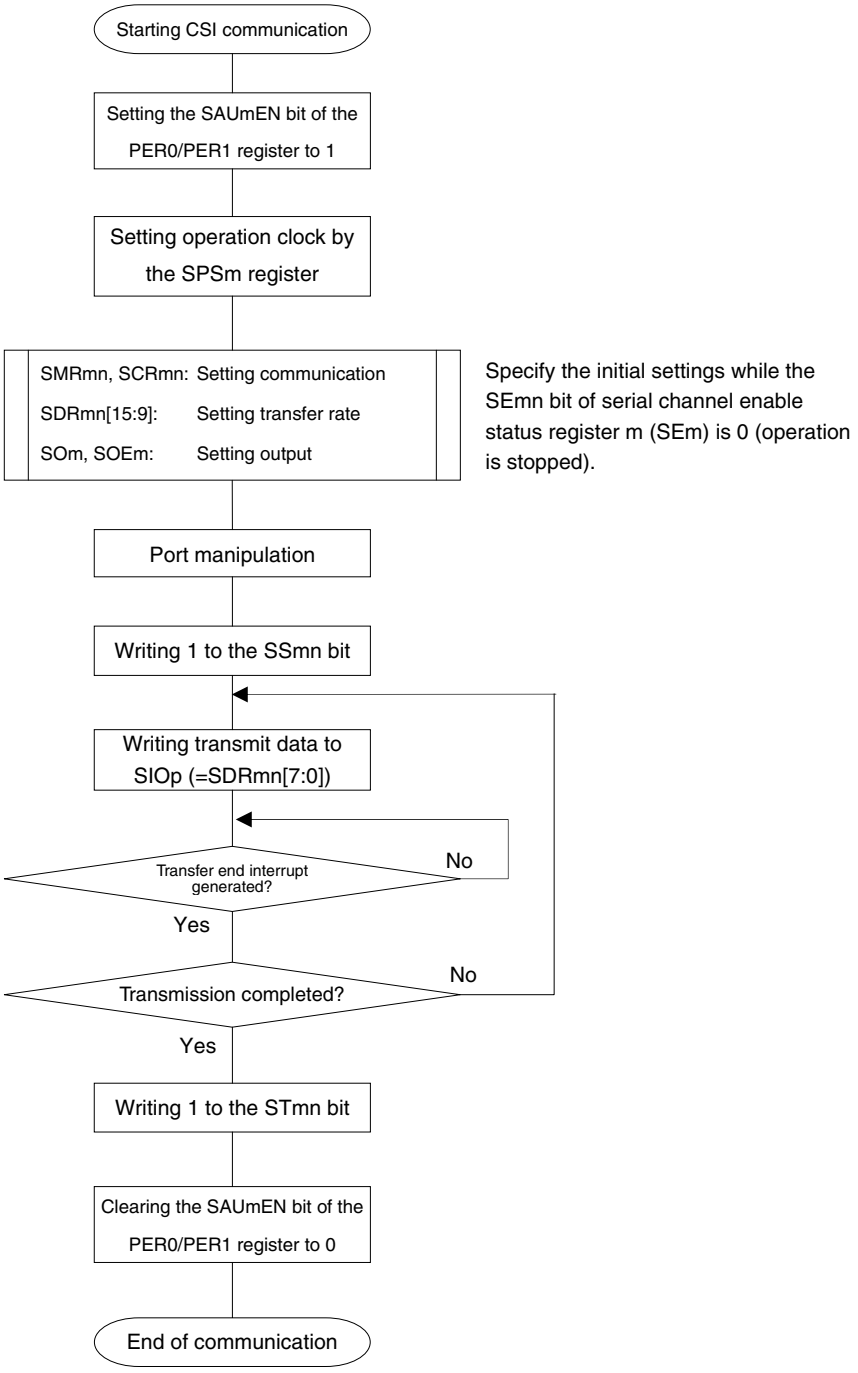
(3) Processing flow (in single-transmission mode)

Figure 14-32. Timing Chart of Master Transmission (in Single-Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

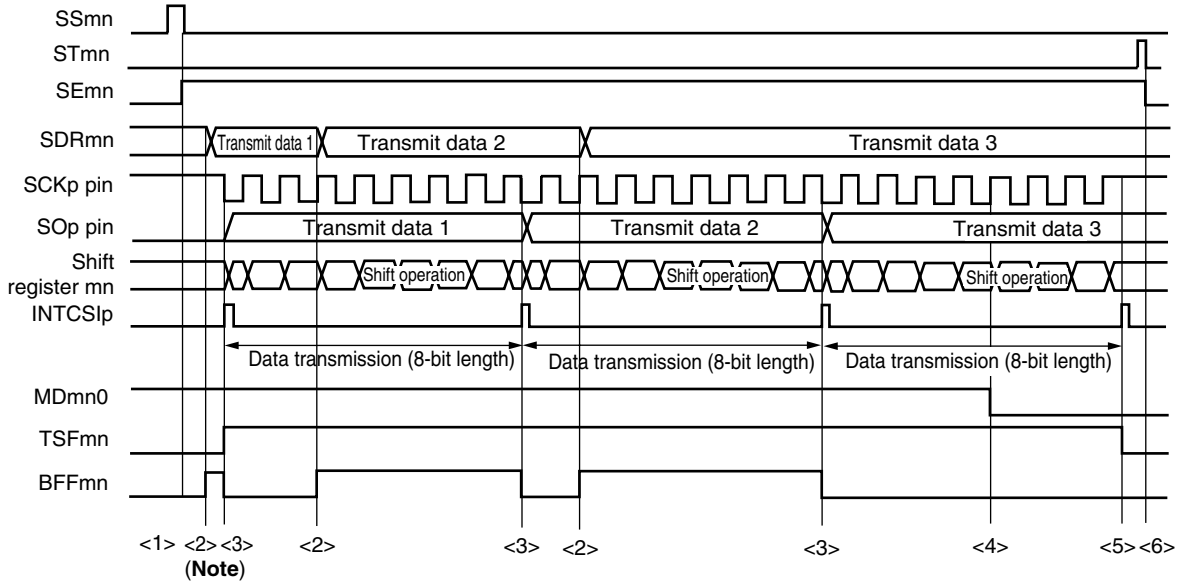
Figure 14-33. Flowchart of Master Transmission (in Single-Transmission Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

(4) Processing flow (in continuous transmission mode)

Figure 14-34. Timing Chart of Master Transmission (in Continuous Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)

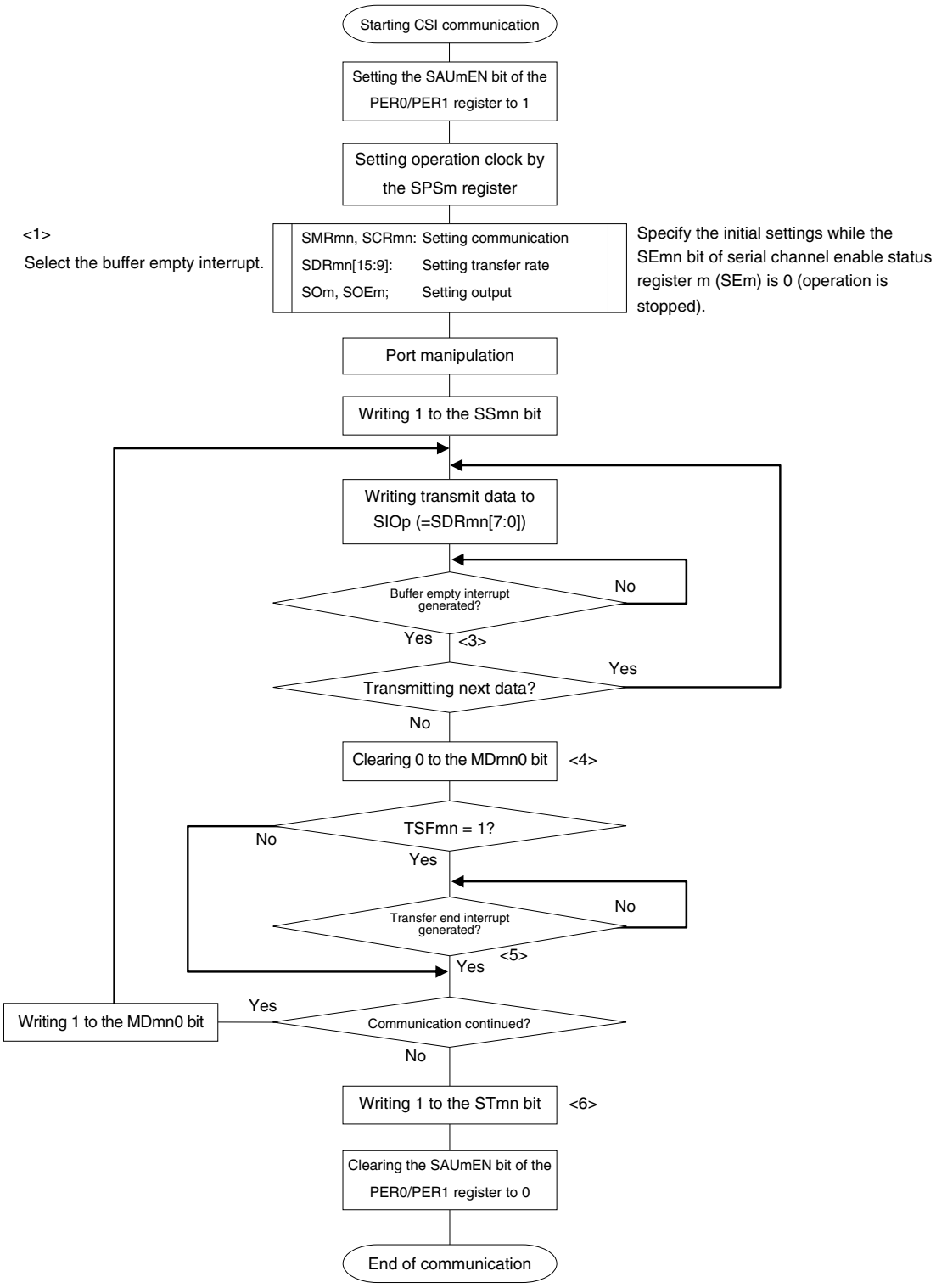


Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

Figure 14-35. Flowchart of Master Transmission (in Continuous Transmission Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Remark <1> to <6> in the figure correspond to <1> to <6> in **Figure 14-34 Timing Chart of Master Transmission (in Continuous Transmission Mode)**.

14.5.2 Master reception

Master reception is that the 78K0R/Kx3-L outputs a transfer clock and receives data from other device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20 Note 1	CSI40 Note 2	CSI41 Note 2
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1	Channel 0 of SAU2	Channel 1 of SAU2
Pins used	$\overline{SCK00}$, SI00	$\overline{SCK01}$, SI01	$\overline{SCK10}$, SI10	$\overline{SCK20}$, SI20	$\overline{SCK40}$, SI40	$\overline{SCK41}$, SI41
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20	INTCSI40	INTCSI41
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. $f_{CLK}/4$ [Hz], Min. $f_{CLK}/(2 \times 2^{11} \times 128)$ [Hz] Note 3 f_{CLK}: System clock frequency					
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data input starts from the start of the operation of the serial clock. • DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Forward • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. CSI40 and CSI41 are only mounted in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

3. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

(1) Register setting

Figure 14-36. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (1/2)

(a) Serial mode register mn (SMRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn	CCSmn						STSmn		SISmn0				MDmn2	MDmn1	MDmn0
	0/1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0/1

Operation clock (f_{MCK}) of channel n
0: Prescaler output clock CKm0 set by the SPSm register
1: Prescaler output clock CKm1 set by the SPSm register

Interrupt source of channel n
0: Transfer end interrupt
1: Buffer empty interrupt

(b) Serial communication operation setting register mn (SCRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn		EOCmn	PTCmn1	PTCmn0	DIRmn		SLCmn1	SLCmn0		DLSmn2	DLSmn1	DLSmn0
	0	1	0/1	0/1	0	0	0	0	0/1	0	0	0	0	1	1	0/1

Selection of the data and clock phase (For details about the setting, see **14.3 Registers Controlling Serial Array Unit**.)

Selection of data transfer sequence
0: Inputs/outputs data with MSB first
1: Inputs/outputs data with LSB first.

Setting of data length
0: 7-bit data length
1: 8-bit data length

(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	Baud rate setting (Operation clock (f_{MCK}) division setting)							0	Receive data (Write FFH as dummy data.)							

SIOp

(d) Serial output register m (SOm) … Sets only the bits of the target channel.

<R>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm						CKOm2	CKOm1	CKOm0						SOm2	SOm1	SOm0
	0	0	0	0	1	0/1 Notes 1, 2	0/1 Note 1	0/1	0	0	0	0	1	×	×	×

Communication starts when these bits are 1 if the clock phase is forward (the CKPmn bit of the SCRmn = 0). If the clock phase is reversed (CKPmn = 1), communication starts when these bits are 0.

Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

(**Remarks** are listed on the next page.)

Figure 14-36. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (2/2)

(e) Serial output enable register m (SOEm) …The register that not used in this mode.

<R>

SOEm	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 ×	SOEm1 ×	SOEm0 ×

(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

<R>

SSm	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 2	SSm1 0/1	SSm0 0/1

Notes 1. Those bits are invalid while operating serial allay unit 1.

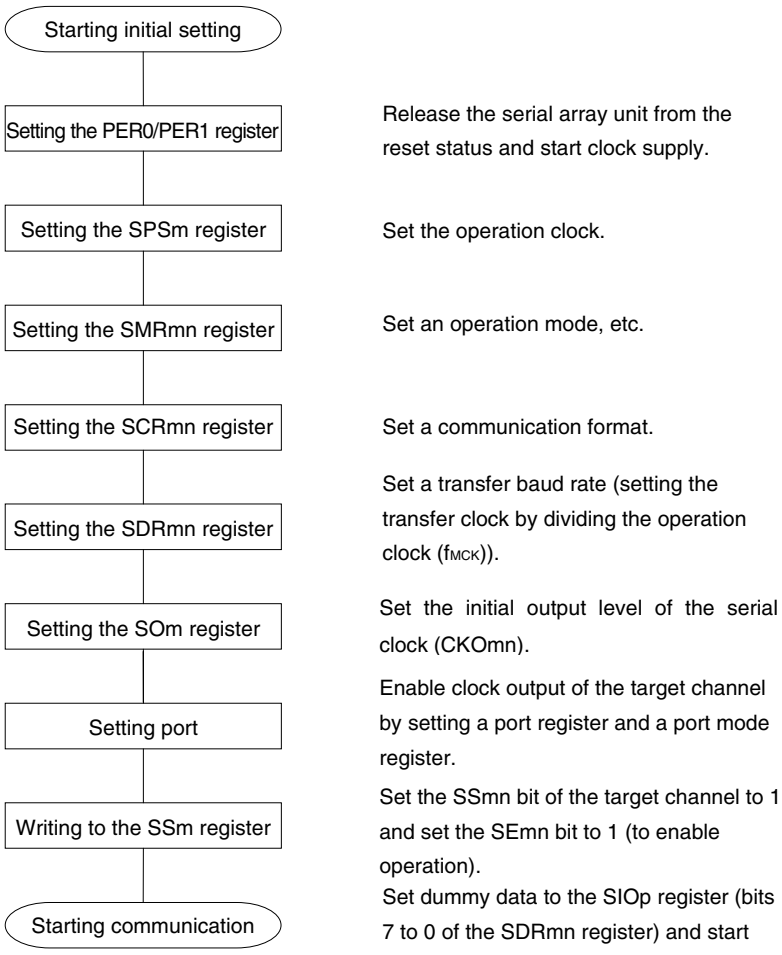
2. Those bits are invalid while operating serial allay unit 2.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

2. □: Setting is fixed in the CSI master transmission mode, ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

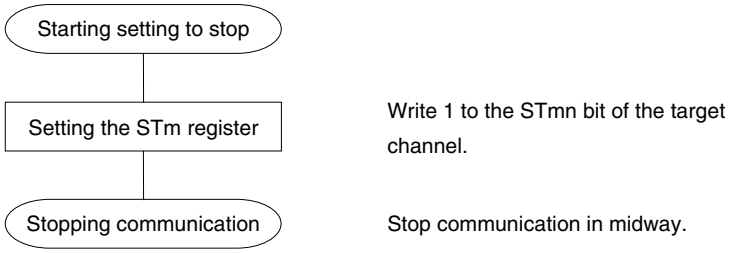
(2) Operation procedure

Figure 14-37. Initial Setting Procedure for Master Reception



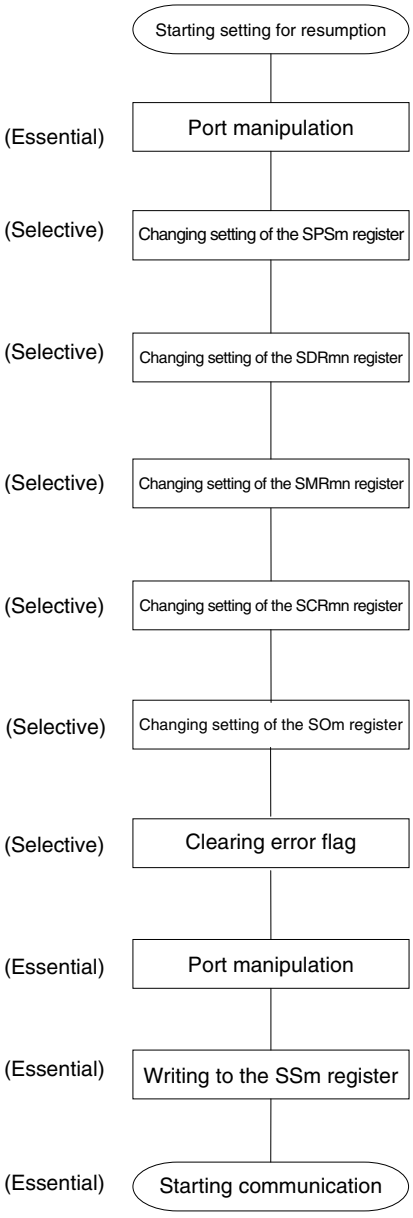
Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Figure 14-38. Procedure for Stopping Master Reception



Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set serial output register m (SOm) (see **Figure 14-39 Procedure for Resuming Master Reception**).

Figure 14-39. Procedure for Resuming Master Reception



Disable clock output of the target channel by setting a port register and a port mode register.

Re-set the register to change the operation clock setting.

Re-set the register to change the transfer baud rate setting (setting the transfer clock by dividing the operation clock (f_{MCK})).

Re-set the register to change serial mode register mn (SMRmn) setting.

Re-set the register to change serial communication operation setting register mn (SCRmn) setting.

Set the initial output level of the serial clock (CKOmn).

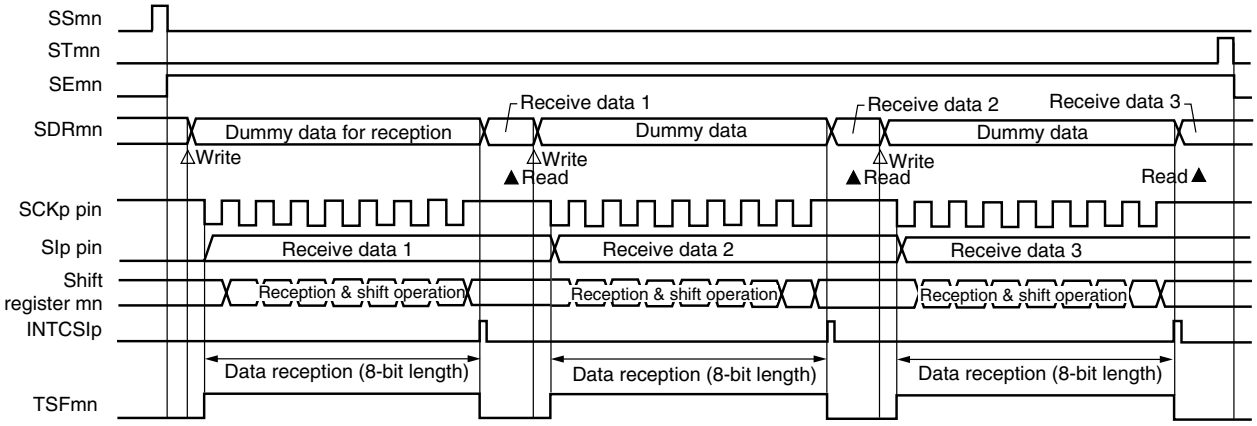
If the FEF, PEF, and OVF flags remain set, clear them using serial flag clear trigger register mn (SIRmn).

Enable clock output of the target channel by setting a port register and a port mode register.

Set the SSmn bit of the target channel to 1 and set the SEmn bit to 1 (to enable operation).
Sets dummy data to the SIOp register (bits 7 to 0 of the SDRmn register) and start communication.

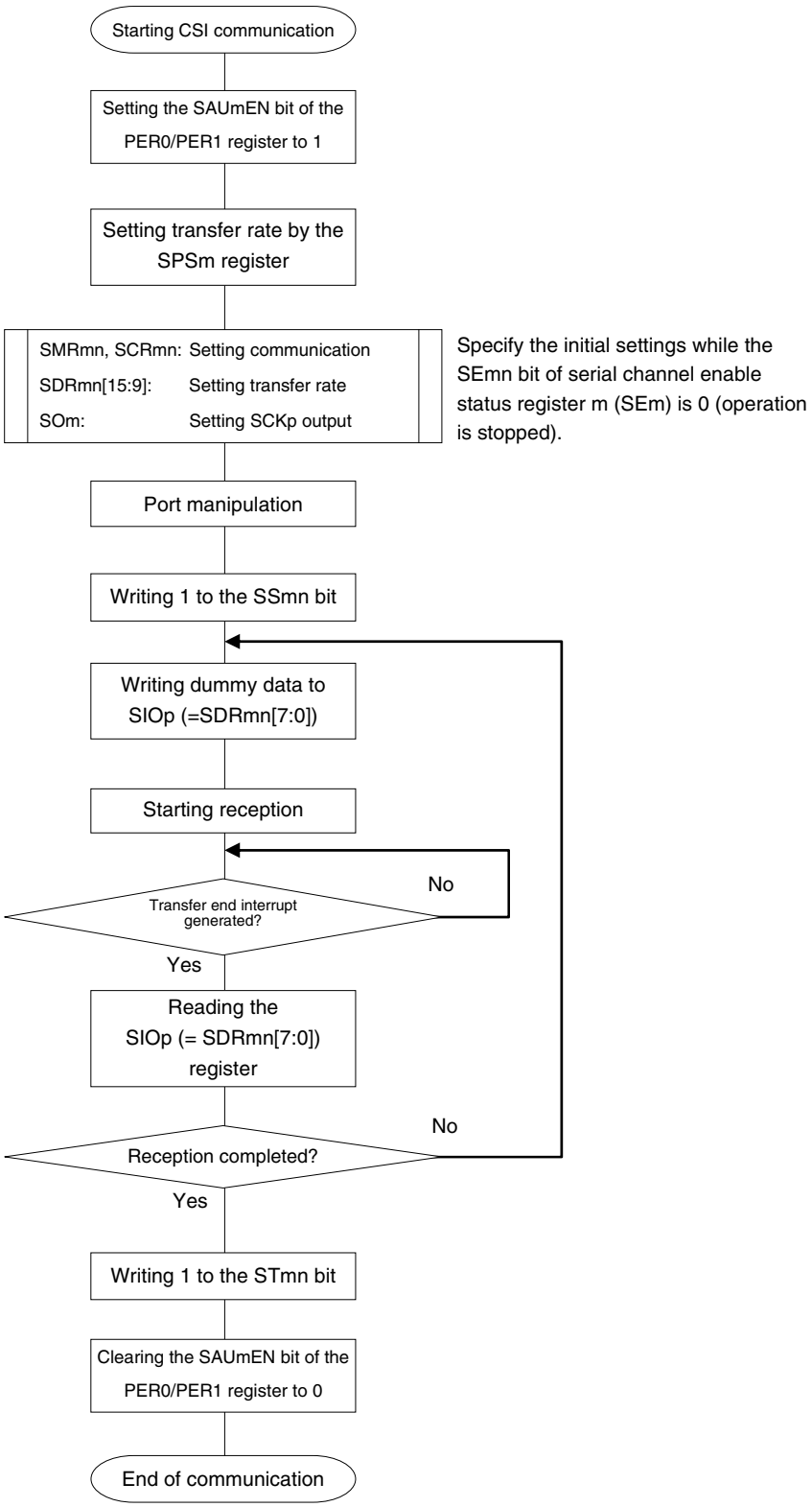
(3) Processing flow (in single-reception mode)

Figure 14-40. Timing Chart of Master Reception (in Single-Reception Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

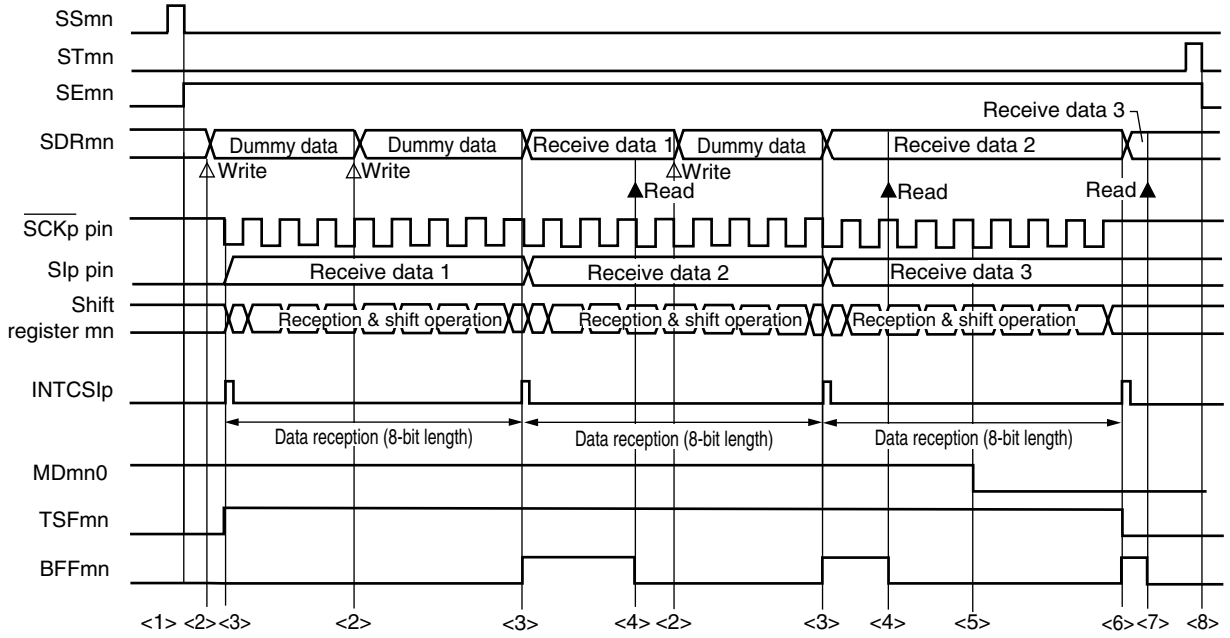
Figure 14-41. Flowchart of Master Reception (in Single-Reception Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

(4) Processing flow (in continuous reception mode)

Figure 14-42. Timing Chart of Master Reception (in Continuous Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



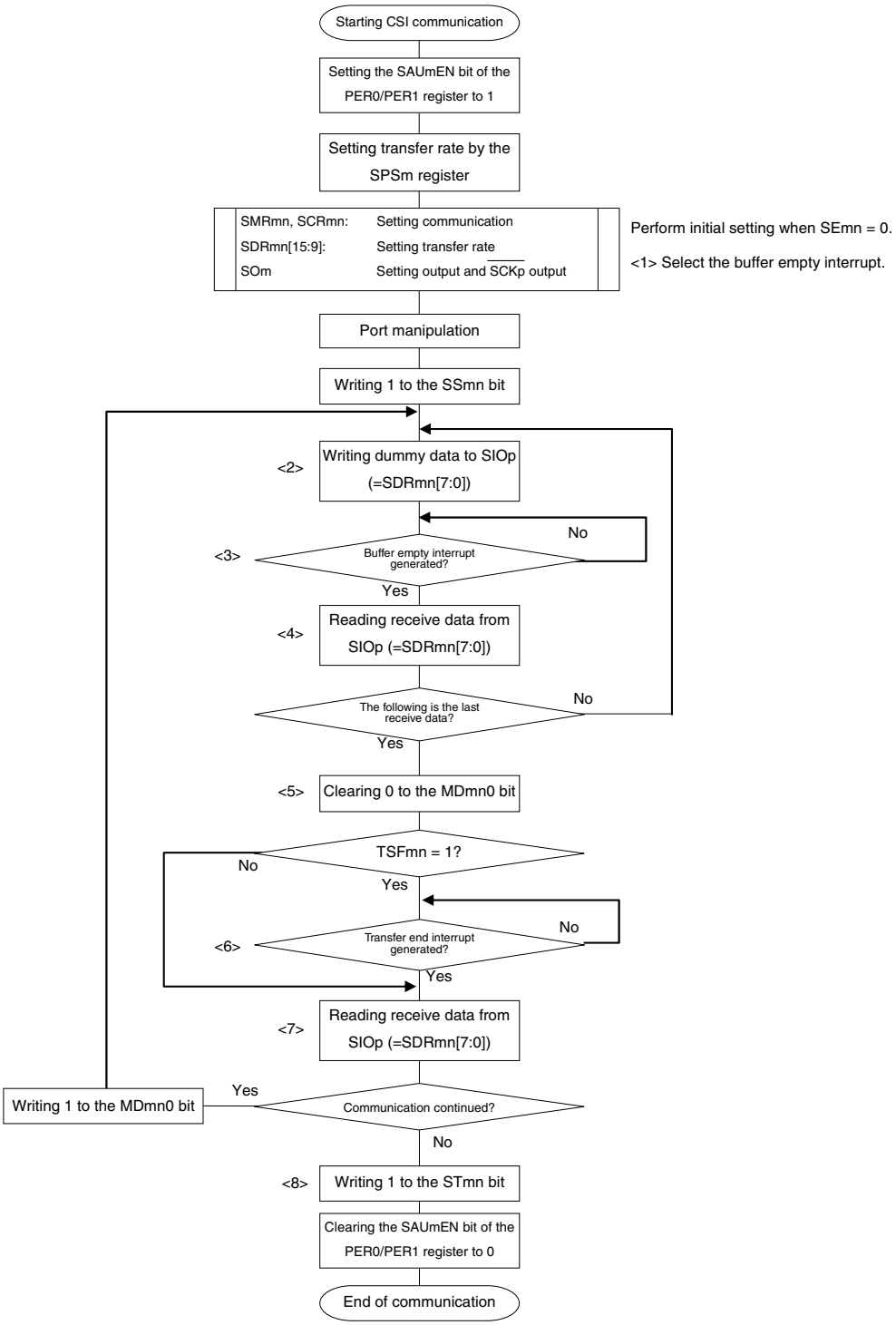
Caution The MDmn0 bit can be rewritten even during operation.
However, rewrite it before receive of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last receive data.

Remarks 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 13-43 Flowchart of Master Reception (in Continuous Reception Mode)**.

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

Figure 14-43. Flowchart of Master Reception (in Continuous Reception Mode)



Caution After setting the PER0/PER1 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 14-42 Timing Chart of Master Reception (in Continuous Reception Mode)**.

14.5.3 Master transmission/reception

Master transmission/reception is that the 78K0R/Kx3-L outputs a transfer clock and transmits/receives data to/from other device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20 Note 1	CSI40 Note 2	CSI41 Note 2
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1	Channel 0 of SAU2	Channel 1 of SAU2
Pins used	$\overline{SCK00}$, SI00, SO00	$\overline{SCK01}$, SI01, SO01	$\overline{SCK10}$, SI10, SO00	$\overline{SCK20}$, SI20, SO20	$\overline{SCK40}$, SI40, SO40	$\overline{SCK41}$, SI41, SO41
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20	INTCSI40	INTCSI41
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. $f_{CLK}/4$ [Hz], Min. $f_{CLK}/(2 \times 2^{11} \times 128)$ [Hz] Note 3 f_{CLK}: System clock frequency					
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data I/O starts at the start of the operation of the serial clock. • DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Forward • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. CSI40 and CSI41 are only mounted in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

3. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

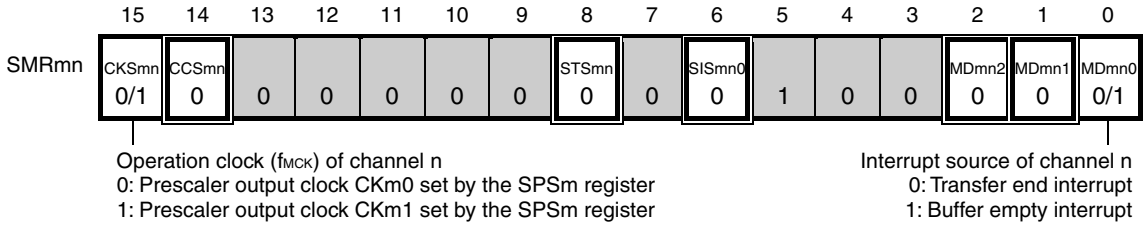
Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

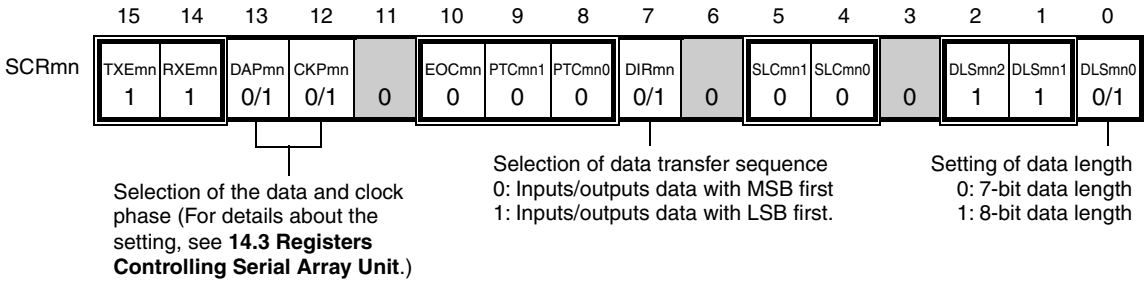
(1) Register setting

Figure 14-44. Example of Contents of Registers for Master Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (1/2)

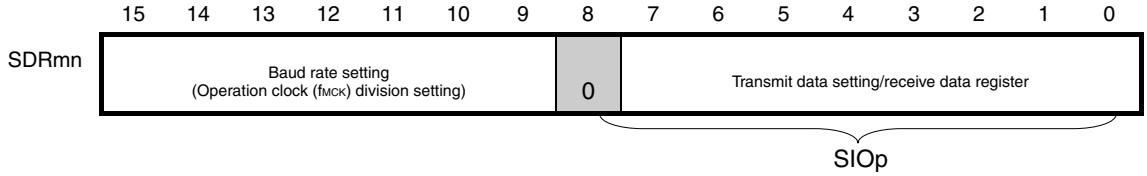
(a) Serial mode register mn (SMRmn)



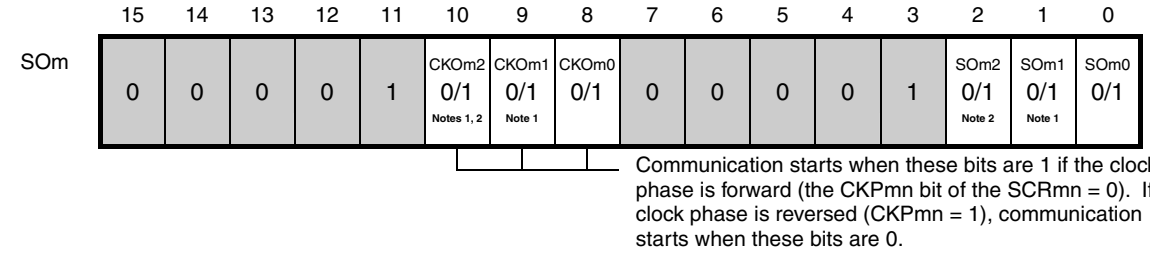
(b) Serial communication operation setting register mn (SCRmn)



(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOm) … Sets only the bits of the target channel.



Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

(**Remark** is listed on the next page.)

Figure 14-44. Example of Contents of Registers for Master Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (2/2)

(e) Serial output enable register m (SOEm) … Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 0/1 Note 1	SOEm1 0/1 Note 2	SOEm0 0/1

(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

<R>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 2	SSm1 0/1	SSm0 0/1

Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

2. ☐ : Setting is fixed in the CSI master transmission/reception mode

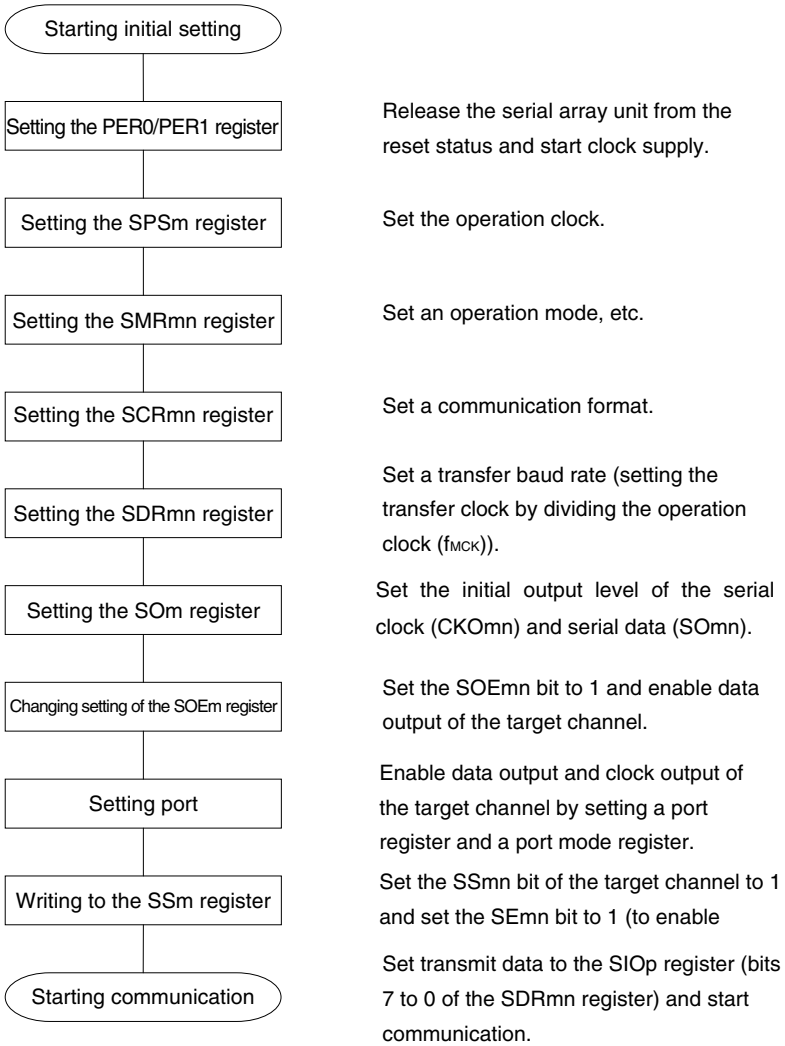
■ : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

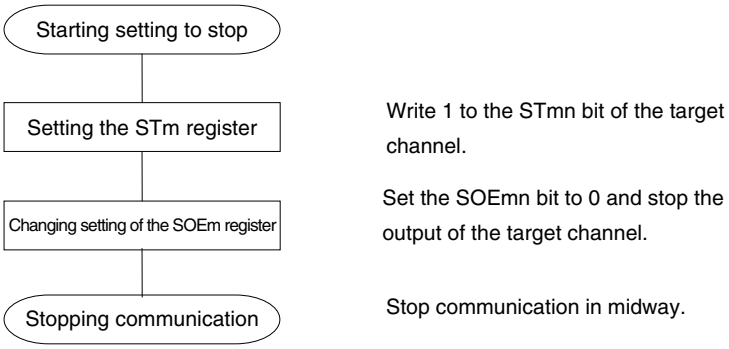
(2) Operation procedure

Figure 14-45. Initial Setting Procedure for Master Transmission/Reception



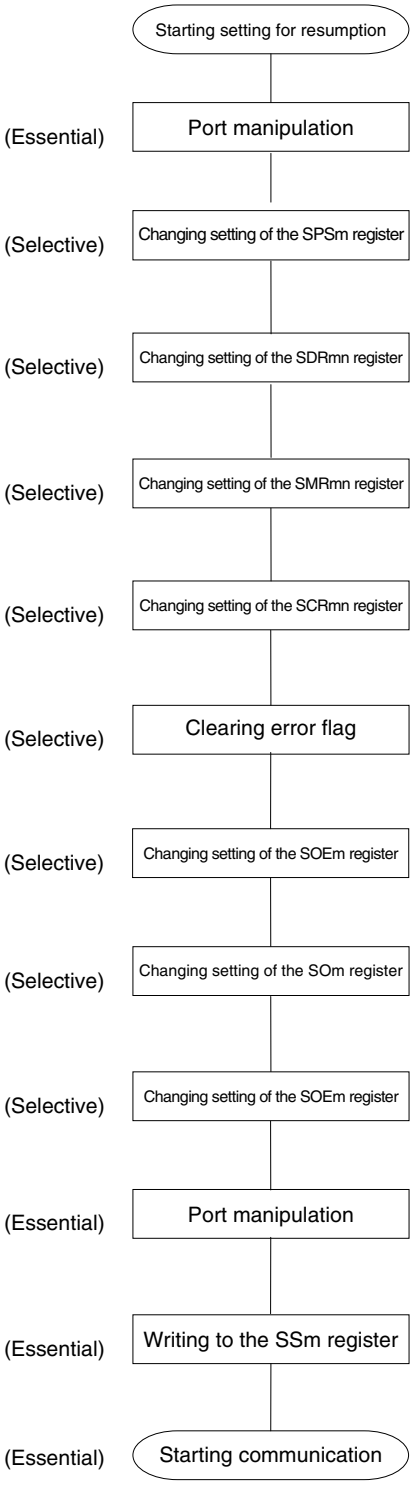
Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Figure 14-46. Procedure for Stopping Master Transmission/Reception



Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set serial output register m (SOm) (see **Figure 14-47 Procedure for Resuming Master Transmission**).

Figure 14-47. Procedure for Resuming Master Transmission/Reception



Disable data output and clock output of the target channel by setting a port register and a port mode register.

Re-set the register to change the operation clock setting.

Re-set the register to change the transfer baud rate setting (setting the transfer clock by dividing the operation clock (f_{MCK})).

Re-set the register to change serial mode register mn (SMRmn) setting.

Re-set the register to change serial communication operation setting register mn (SCRmn) setting.

If the FEF, PEF, and OVF flags remain set, clear them using serial flag clear trigger register mn (SIRmn).

Set the SOEmn bit to 0 to stop output from the target channel.

Set the initial output level of the serial clock (CKOmn) and serial data (SOmn).

Set the SOEmn bit to 1 and enable output from the target channel.

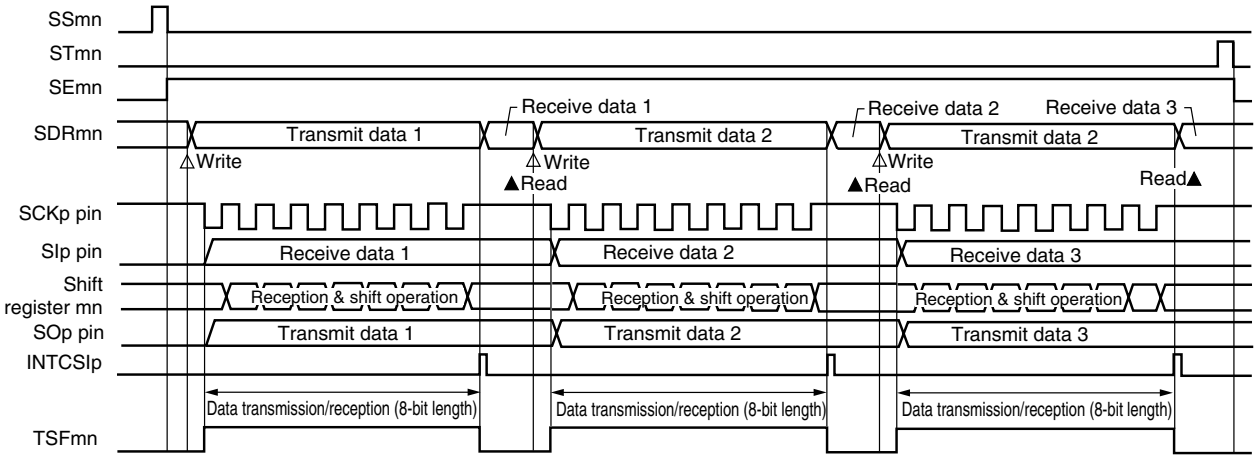
Enable data output and clock output of the target channel by setting a port register and a port mode register.

Set the SSmn bit of the target channel to 1 and set the SEmn bit to 1 (to enable operation).

Sets transmit data to the SIOp register (bits 7 to 0 of the SDRmn register) and start communication.

(3) Processing flow (in single-transmission/reception mode)

Figure 14-48. Timing Chart of Master Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

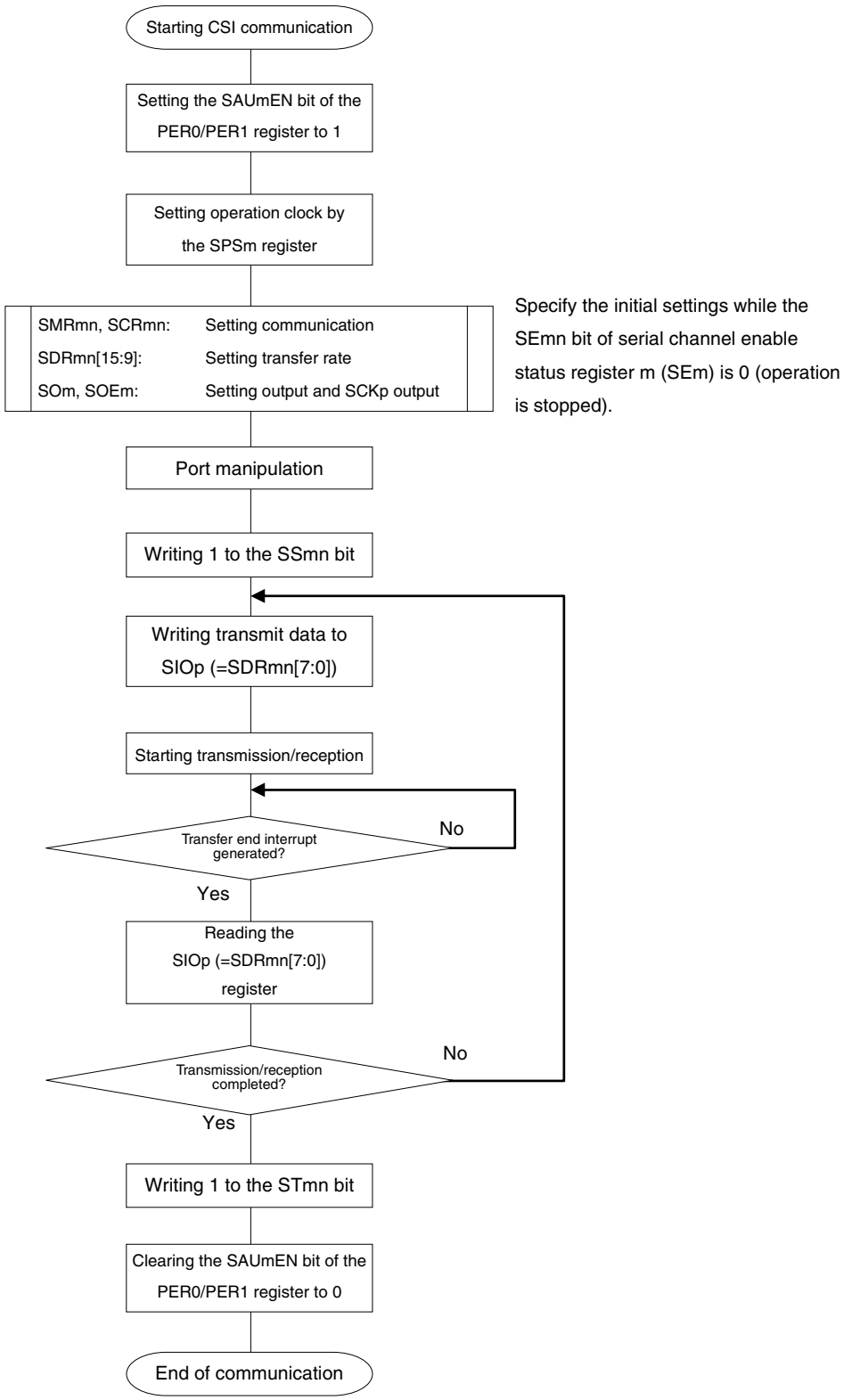
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

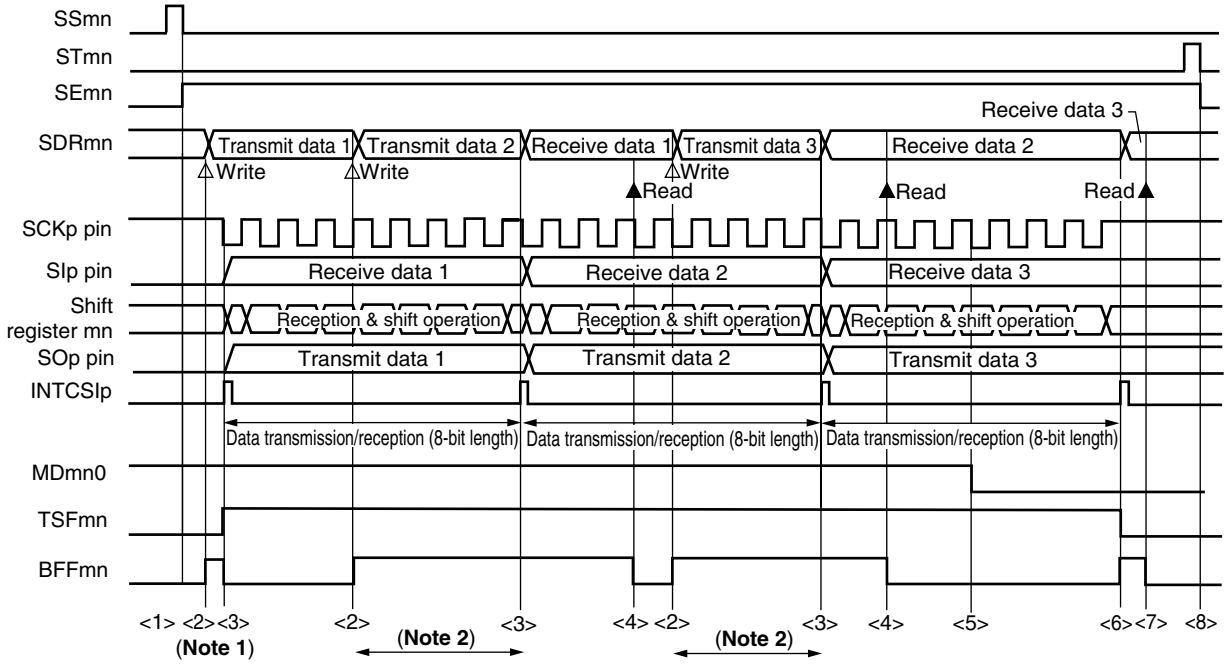
Figure 14-49. Flowchart of Master Transmission/Reception (in Single- Transmission/Reception Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

(4) Processing flow (in continuous transmission/reception mode)

Figure 14-50. Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Notes 1. If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

2. The transmit data can be read by reading the SDRmn register during this period. At this time, the transfer operation is not affected.

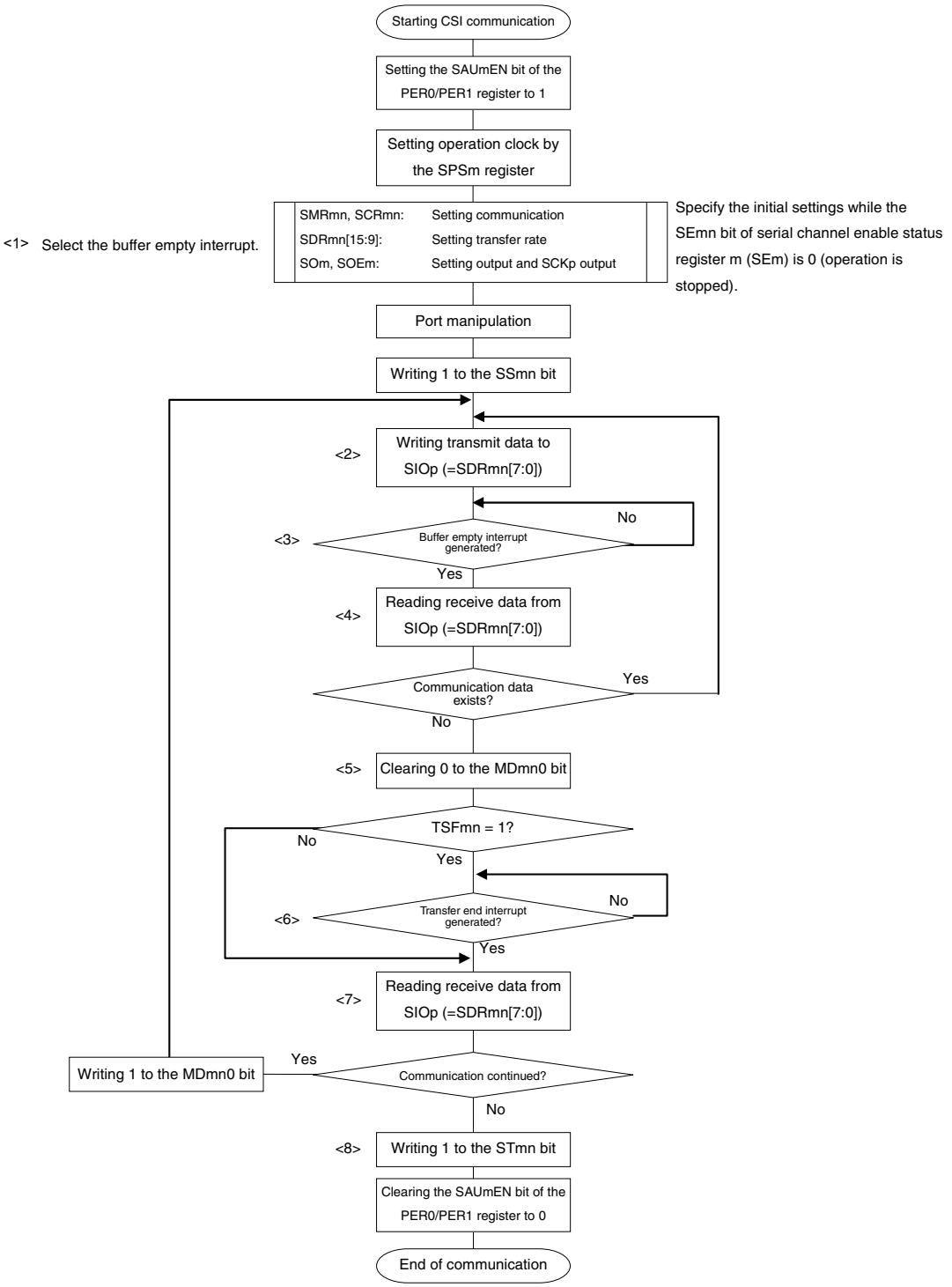
Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last transmit data.

Remarks 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 14-51 Flowchart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)**.

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

Figure 14-51. Flowchart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 14-50 Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)**.

14.5.4 Slave transmission

Slave transmission is that the 78K0R/Kx3-L transmits data to another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20 Note 1	CSI40 Note 2	CSI41 Note 2
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1	Channel 0 of SAU2	Channel 1 of SAU2
Pins used	$\overline{SCK00}$, SO00	$\overline{SCK01}$, SO01	$\overline{SCK10}$, SO10	$\overline{SCK20}$, SO20	$\overline{SCK40}$, SO40	$\overline{SCK41}$, SO41
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20	INTCSI40	INTCSI41
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 3, 4.					
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data output starts from the start of the operation of the serial clock. • DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Forward • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. CSI40 and CSI41 are only mounted in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

3. Because the external serial clock input to the $\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK20}$, $\overline{SCK40}$, and $\overline{SCK41}$ pins is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [Hz].

4. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

Remarks 1. f_{MCK}: Operation clock frequency of target channel

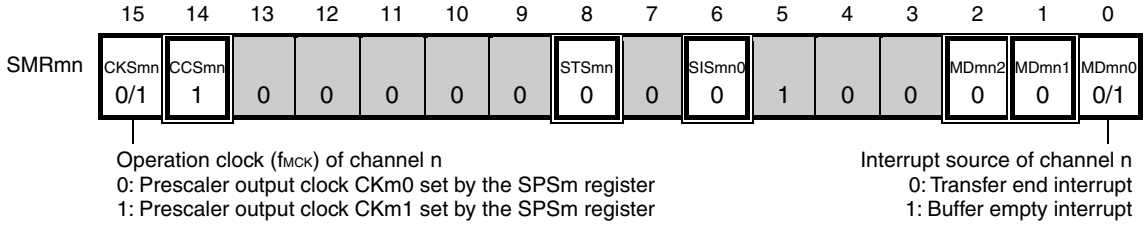
2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p : CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

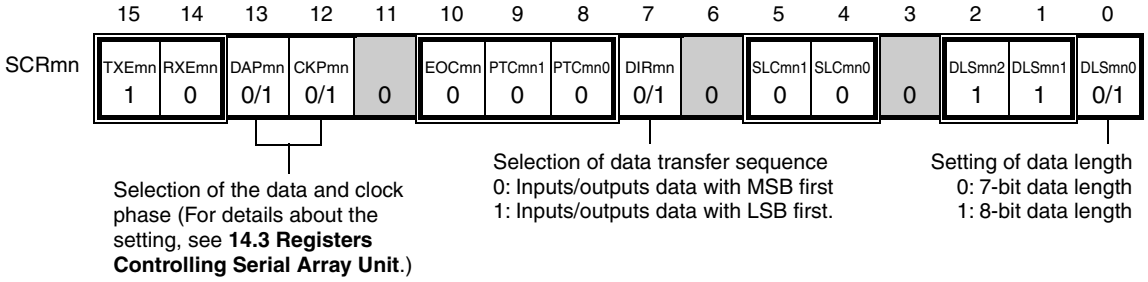
(1) Register setting

Figure 14-52. Example of Contents of Registers for Slave Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (1/2)

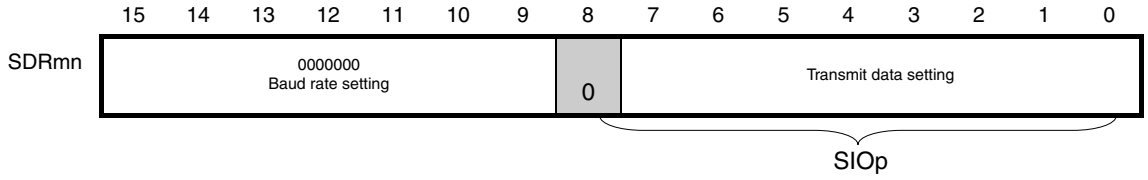
(a) Serial mode register mn (SMRmn)



(b) Serial communication operation setting register mn (SCRmn)

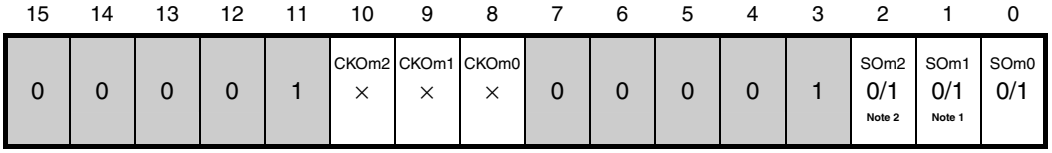


(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOm) … Sets only the bits of the target channel.

<R>



Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

(**Remark** is listed on the next page.)

Figure 14-52. Example of Contents of Registers for Slave Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (2/2)

(e) Serial output enable register m (SOEm) … Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 0/1 Note 1	SOEm1 0/1 Note 2	SOEm0 0/1

(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

<R>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 2	SSm1 0/1	SSm0 0/1

Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

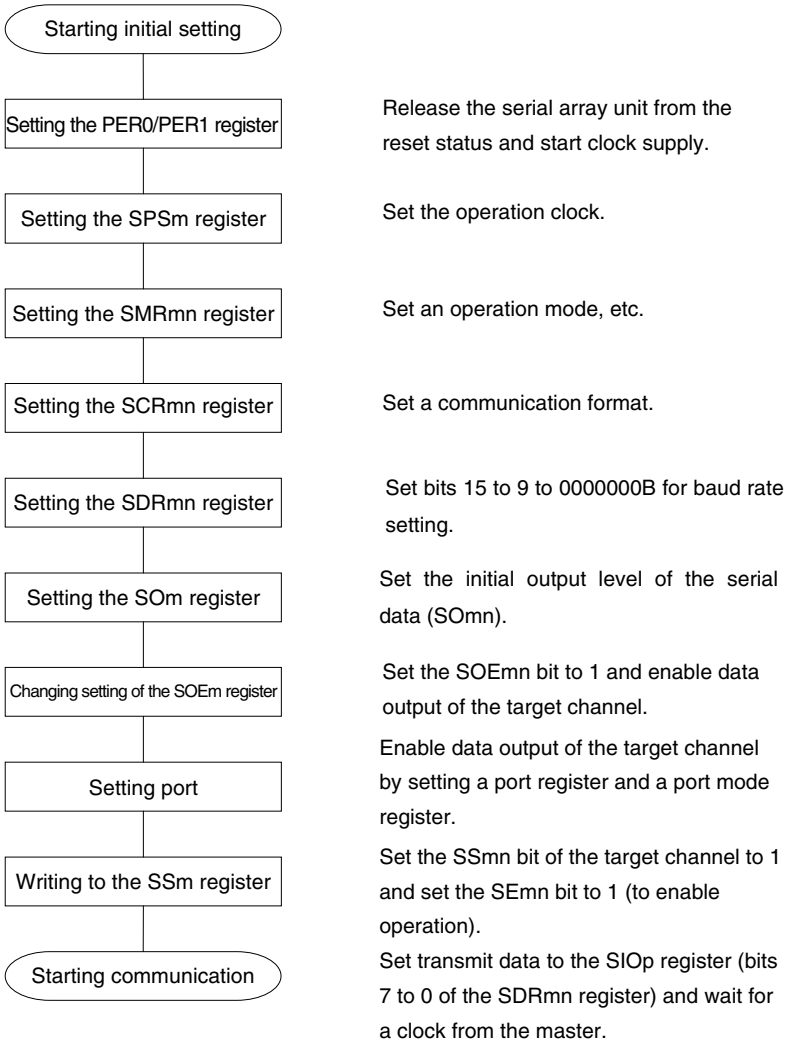
2. □: Setting is fixed in the CSI master transmission mode, ■: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

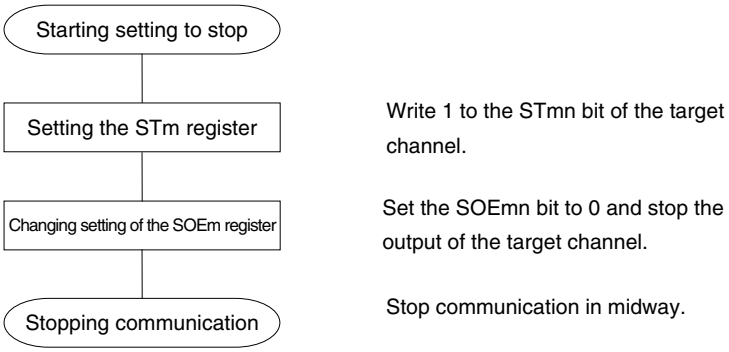
(2) Operation procedure

Figure 14-53. Initial Setting Procedure for Slave Transmission



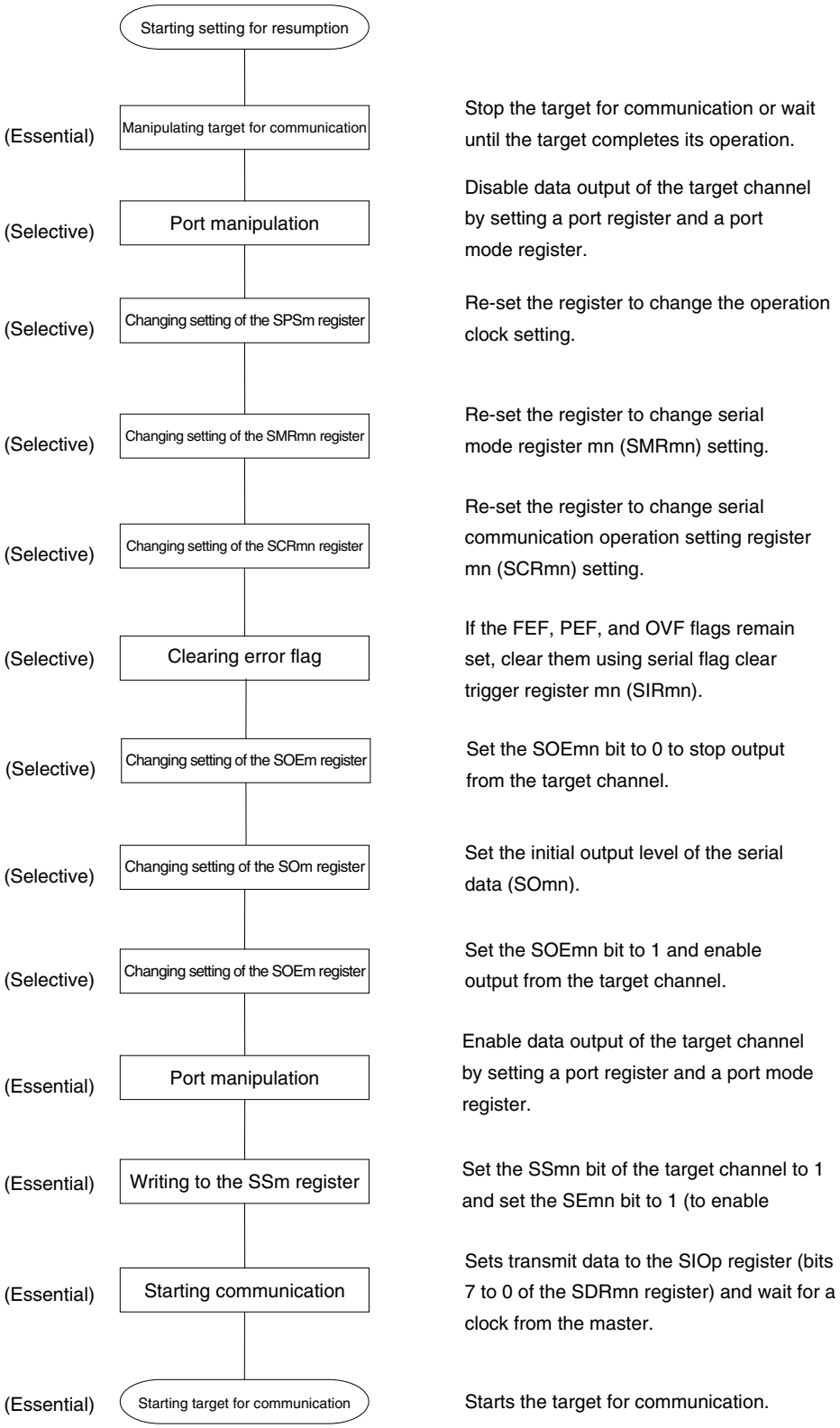
Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Figure 14-54. Procedure for Stopping Slave Transmission



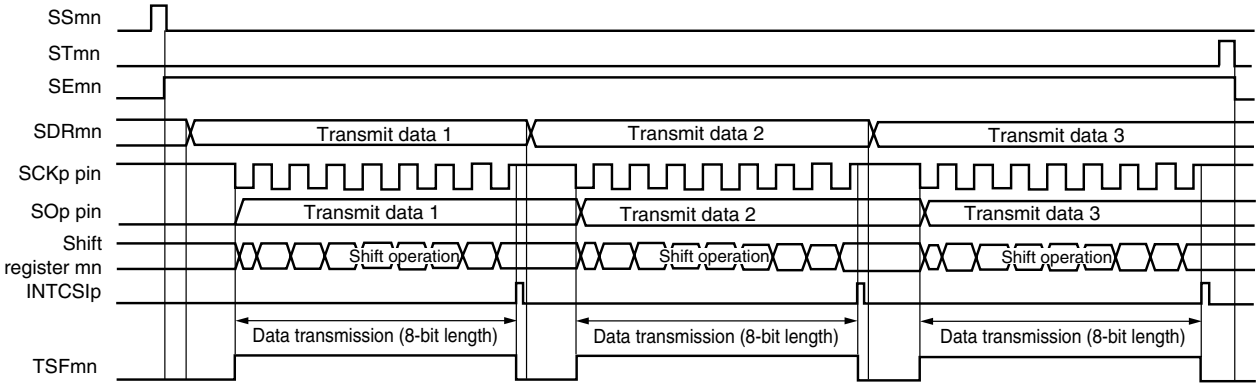
Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set the SOm register (see **Figure 14-55 Procedure for Resuming Slave Transmission**).

Figure 14-55. Procedure for Resuming Slave Transmission



(3) Processing flow (in single-transmission mode)

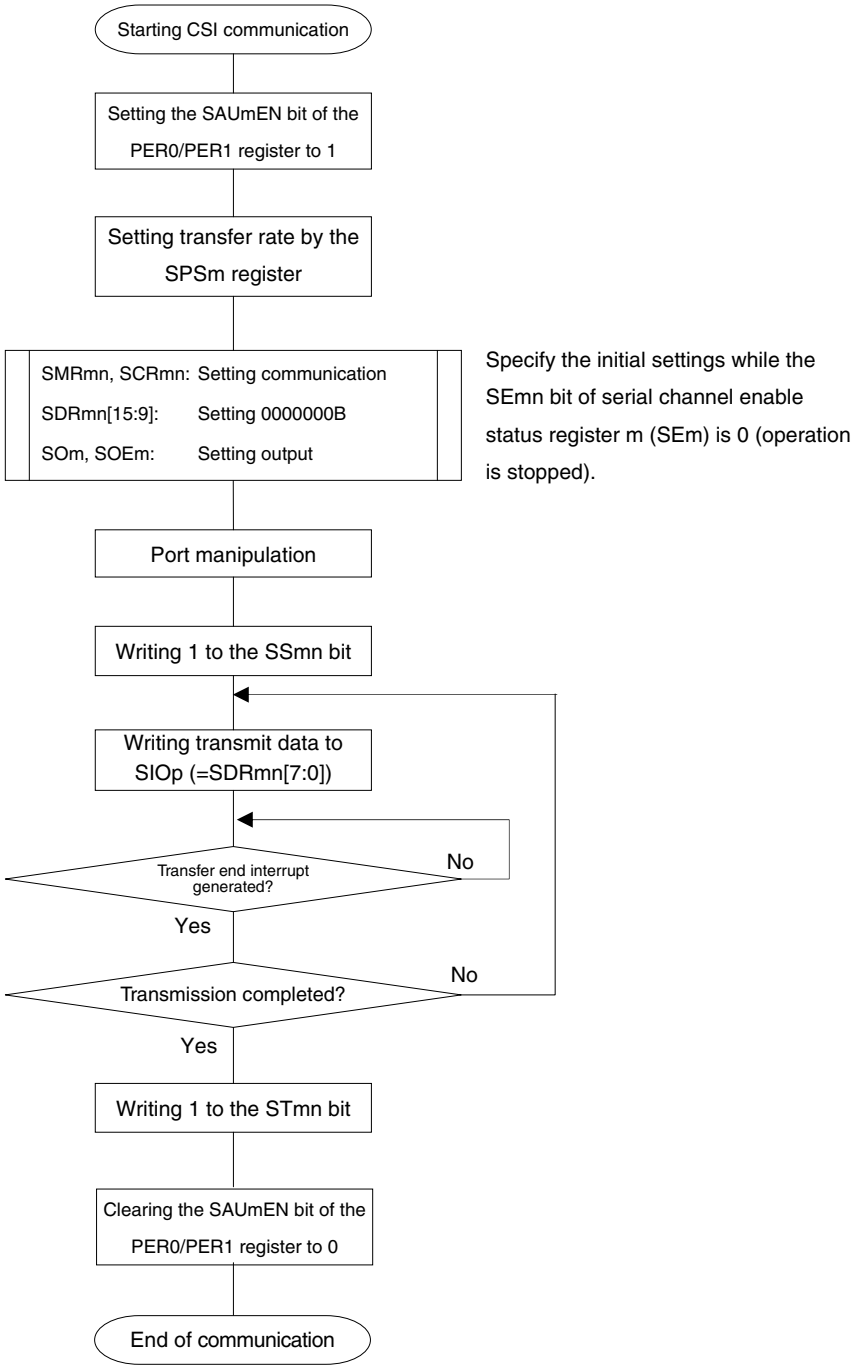
Figure 14-56. Timing Chart of Slave Transmission (in Single-Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L(μPD78F1010, 78F1011, 78F1012):	mn = 00 to 02, 10 p = 00, 01, 10, 20
78K0R/KF3-L(μPD78F1027, 78F1028):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L(μPD78F1013, 78F1014):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L(μPD78F1029, 78F1030):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

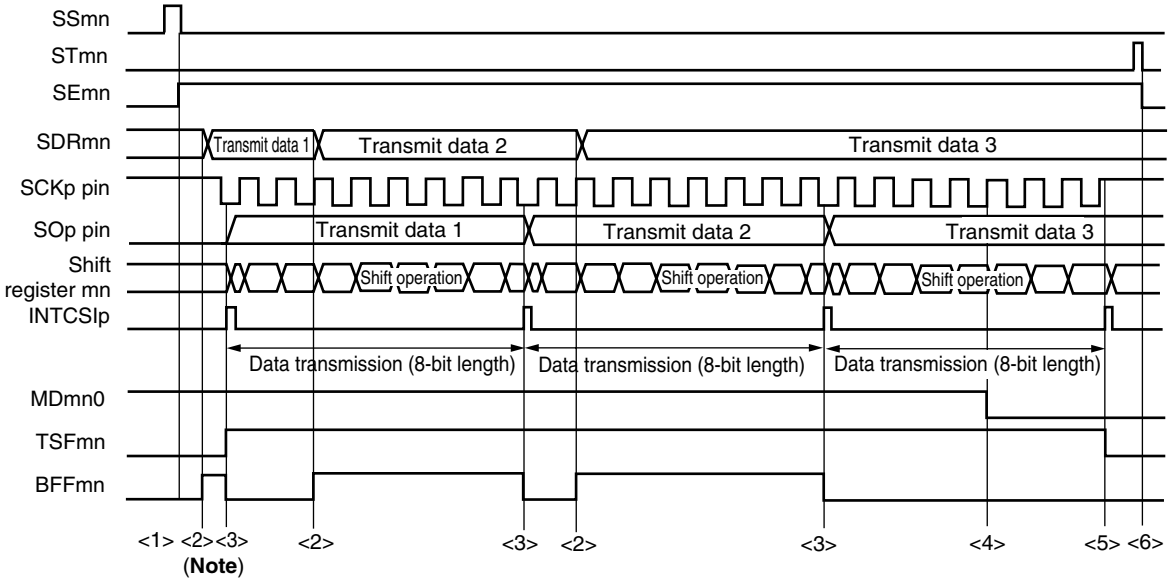
Figure 14-57. Flowchart of Slave Transmission (in Single-Transmission Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

(4) Processing flow (in continuous transmission mode)

Figure 14-58. Timing Chart of Slave Transmission (in Continuous Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



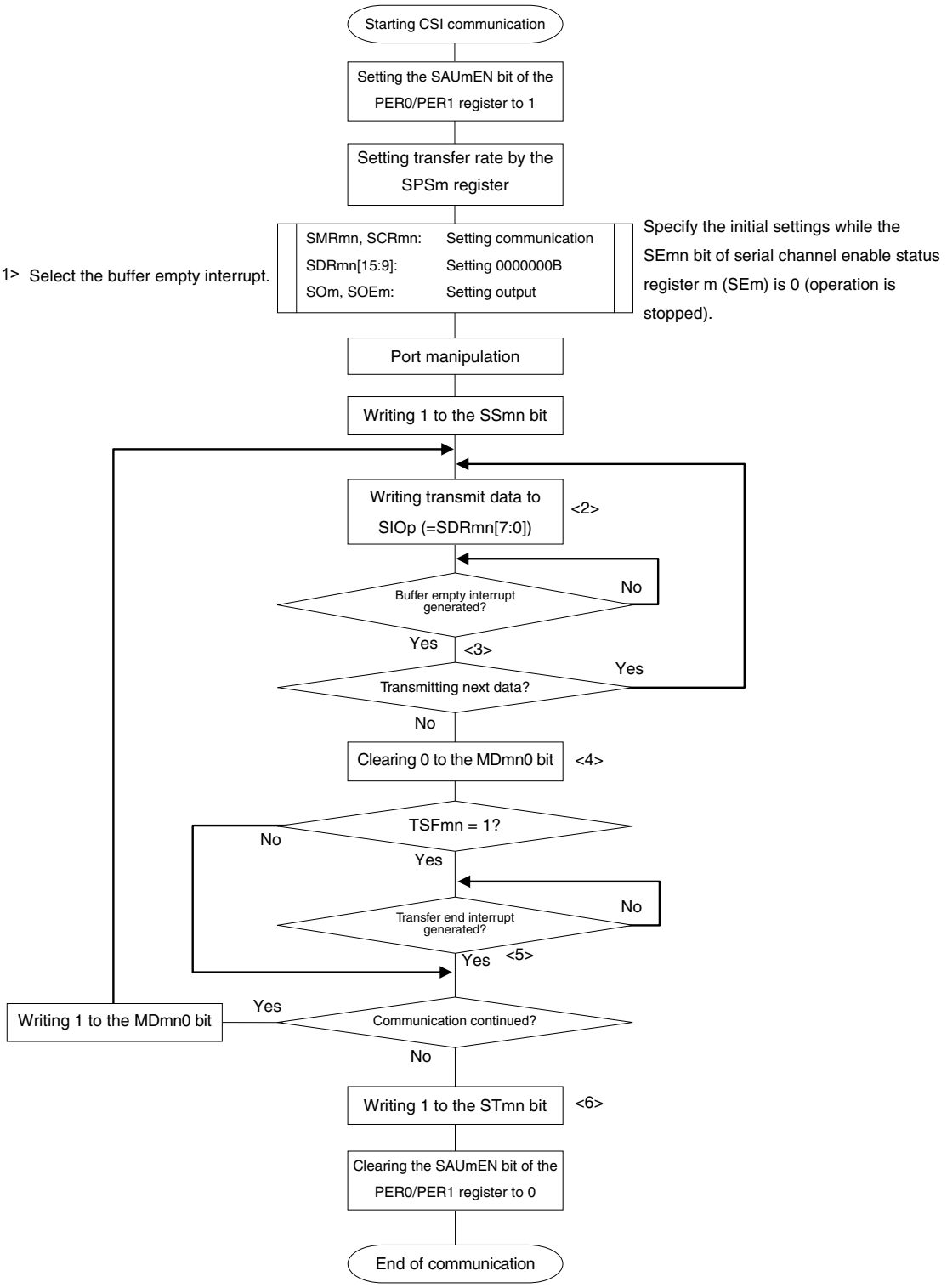
Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

Figure 14-59. Flowchart of Slave Transmission (in Continuous Transmission Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Remark <1> to <6> in the figure correspond to <1> to <6> in **Figure 14-58 Timing Chart of Slave Transmission (in Continuous Transmission Mode)**.

14.5.5 Slave reception

Slave reception is that the 78K0R/Kx3-L receives data from another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20 Note 1	CSI40 Note 2	CSI41 Note 2
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1	Channel 0 of SAU2	Channel 1 of SAU2
Pins used	$\overline{SCK00}$, SI00	$\overline{SCK01}$, SI01	$\overline{SCK10}$, SI10	$\overline{SCK20}$, SI20	$\overline{SCK40}$, SI40	$\overline{SCK41}$, SI41
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20	INTCSI40	INTCSI41
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 3, 4					
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data input starts from the start of the operation of the serial clock. • DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Forward • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. CSI40 and CSI41 are only mounted in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

3. Because the external serial clock input to the $\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK20}$, $\overline{SCK40}$, and $\overline{SCK41}$ pins is sampled internally and used, the fastest transfer rate is the f_{MCK}/6 [Hz] .

4. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

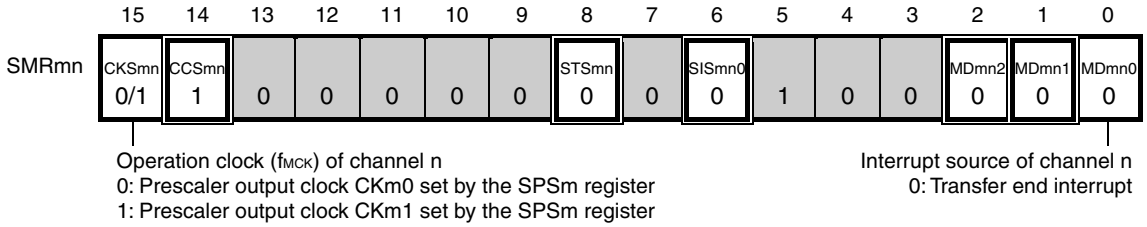
Remarks 1. f_{MCK}: Operation clock frequency of target channel

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21

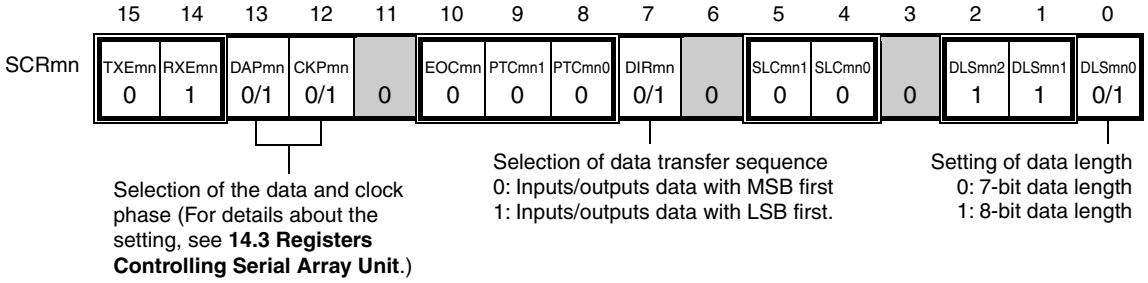
(1) Register setting

Figure 14-60. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (1/2)

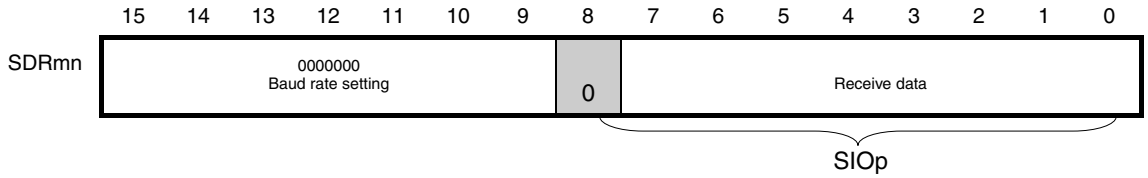
(a) Serial mode register mn (SMRmn)



(b) Serial communication operation setting register mn (SCRmn)

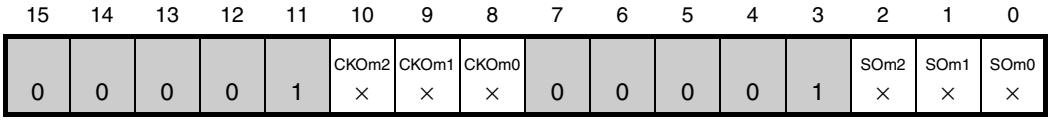


(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOm) …The Register that not used in this mode.

<R>



Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

(**Remark** is listed on the next page.)

Figure 14-60. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (2/2)

(e) Serial output enable register m (SOEm) …The Register that not used in this mode.

<R>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 ×	SOEm1 ×	SOEm0 ×

(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

<R>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 2	SSm1 0/1	SSm0 0/1

Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

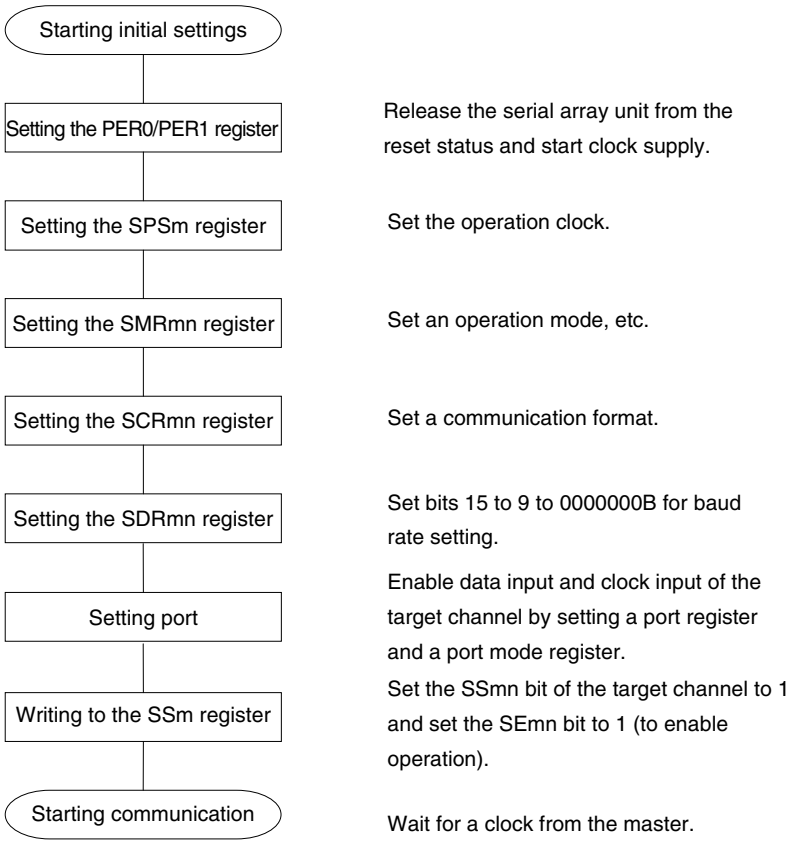
2. □ : Setting is fixed in the CSI master transmission mode, ■ : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 14-61. Initial Setting Procedure for Slave Reception



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Figure 14-62. Procedure for Stopping Slave Reception

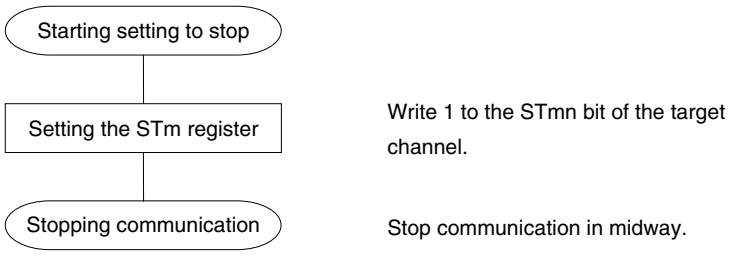
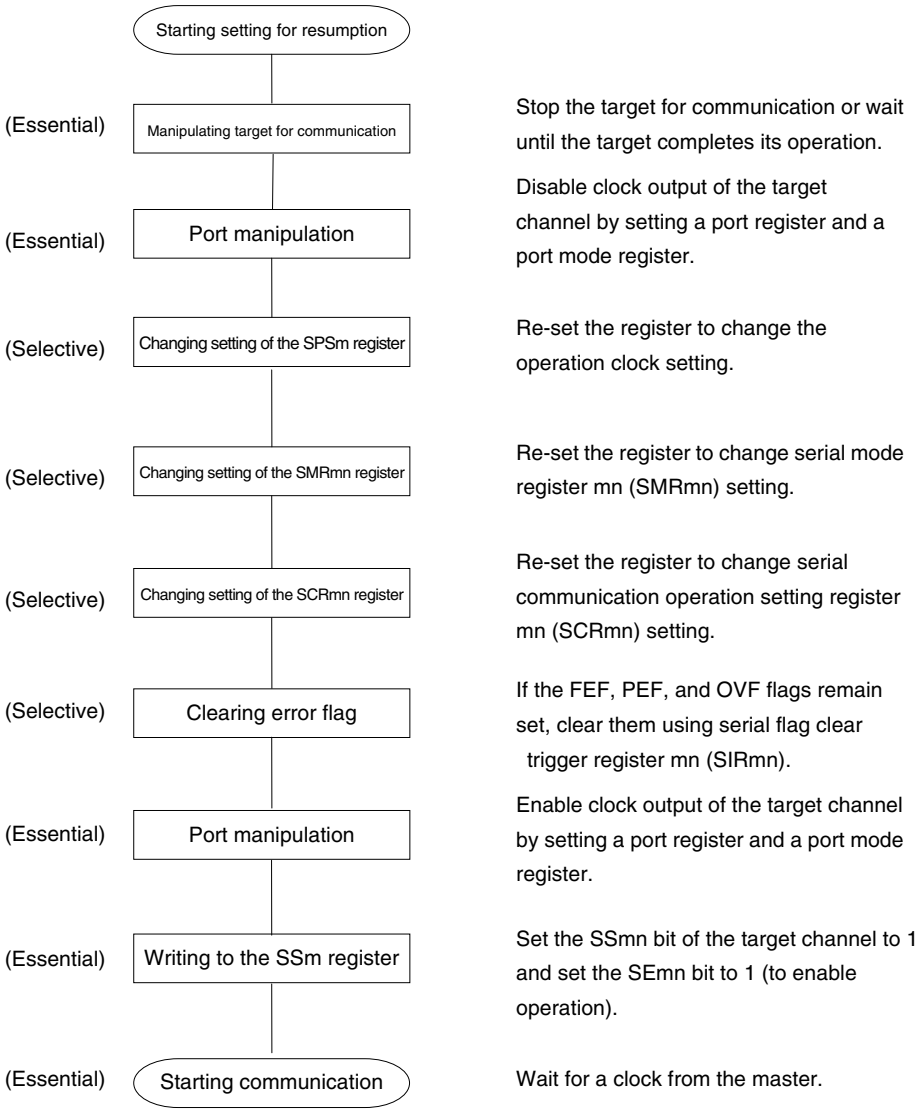
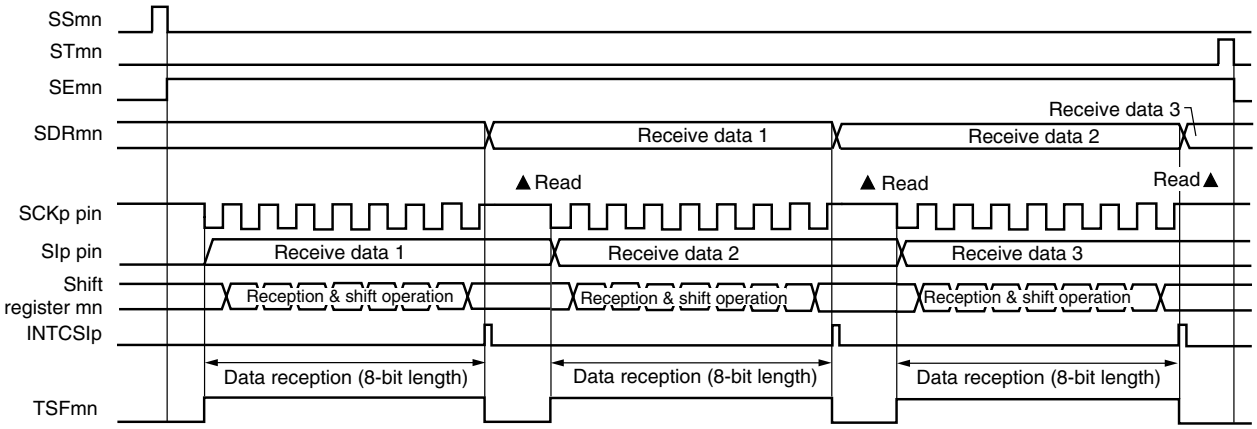


Figure 14-63. Procedure for Resuming Slave Reception



(3) Processing flow (in single-reception mode)

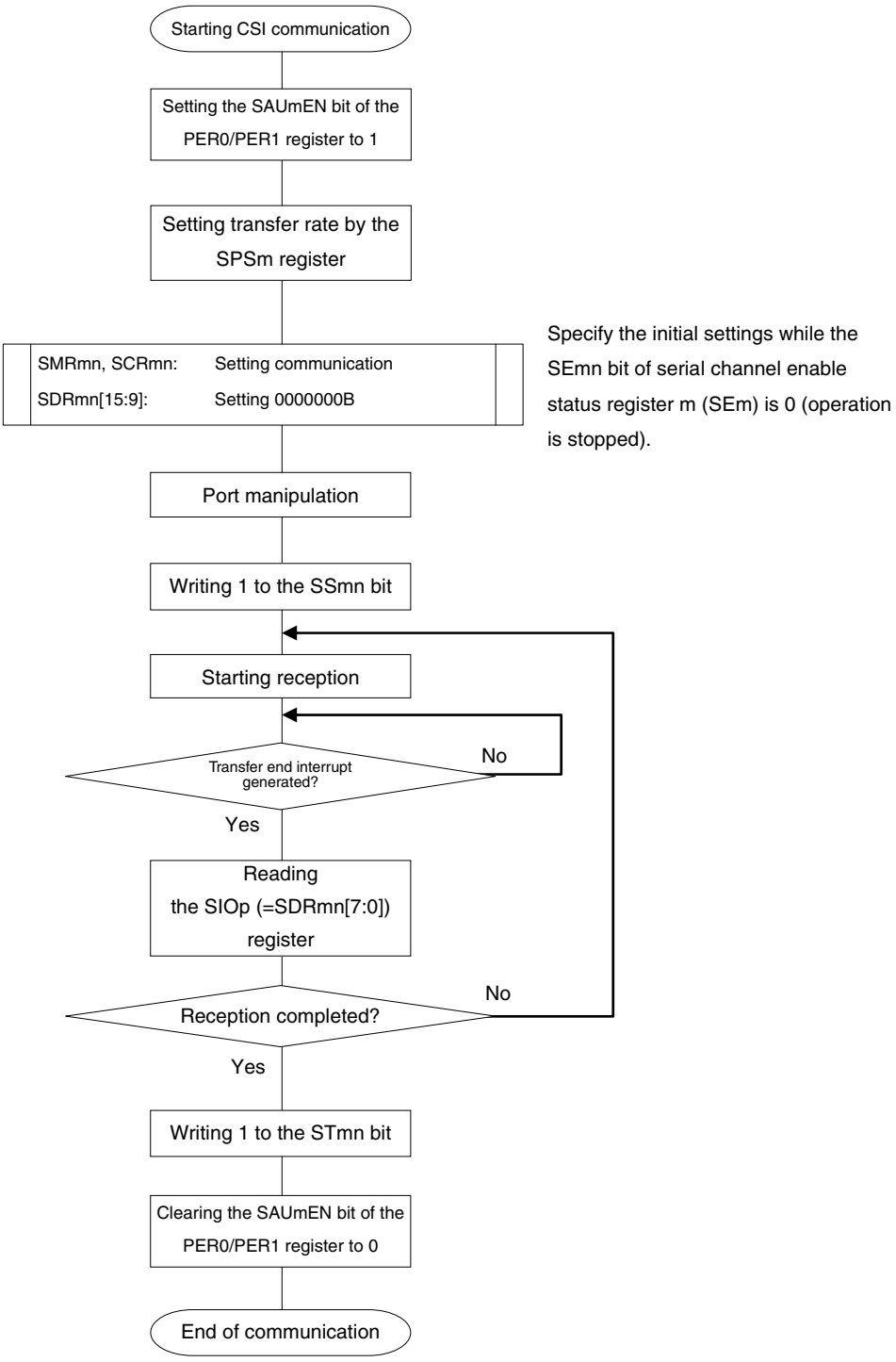
Figure 14-64. Timing Chart of Slave Reception (in Single-Reception Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

Figure 14-65. Flowchart of Slave Reception (in Single-Reception Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

14.5.6 Slave transmission/reception

Slave transmission/reception is that the 78K0R/Kx3-L transmits/receives data to/from another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20 Note 1	CSI40 Note 2	CSI41 Note 2
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1	Channel 0 of SAU2	Channel 1 of SAU2
Pins used	$\overline{\text{SCK00}}$, SI00, SOm0	$\overline{\text{SCK01}}$, SI01, SOm1	$\overline{\text{SCK10}}$, SI10, SO10	$\overline{\text{SCK20}}$, SI20, SO20	$\overline{\text{SCK40}}$, SI40, SO40	$\overline{\text{SCK41}}$, SI41, SO41
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20	INTCSI40	INTCSI41
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 3,4					
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data I/O starts from the start of the operation of the serial clock. • DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Forward • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. CSI40 and CSI41 are only mounted in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

2. Because the external serial clock input to the $\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK10}}$, $\overline{\text{SCK20}}$, $\overline{\text{SCK40}}$, and $\overline{\text{SCK41}}$ pins is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [Hz].

3. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

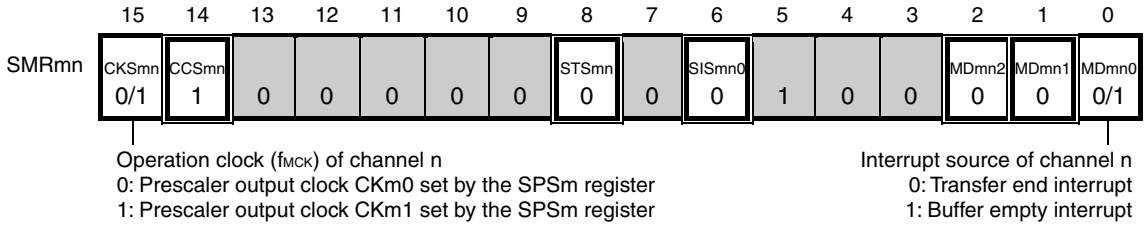
Remarks 1. f_{MCK}: Operation clock frequency of target channel

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21

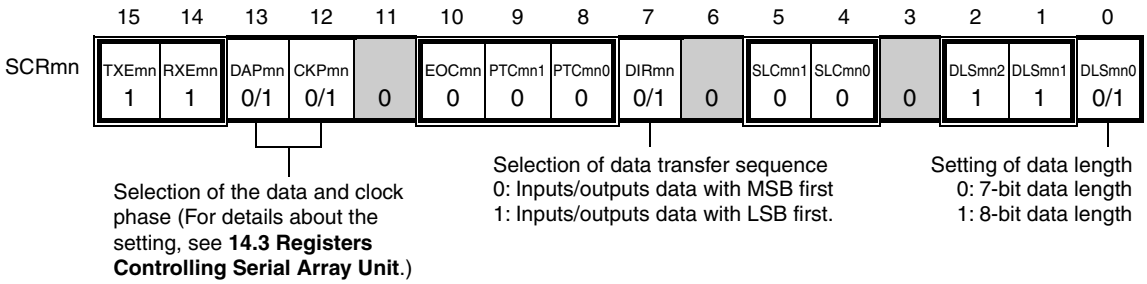
(1) Register setting

Figure 14-66. Example of Contents of Registers for Slave Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSK40, CSK41) (1/2)

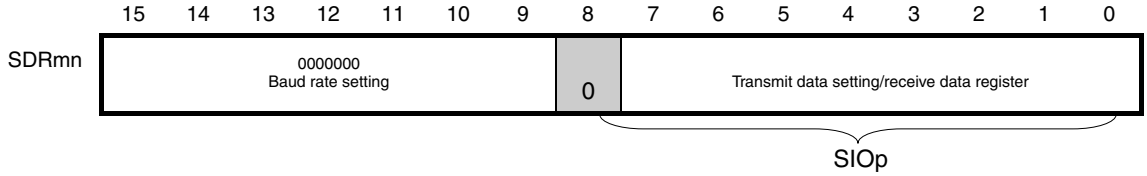
(a) Serial mode register mn (SMRmn)



(b) Serial communication operation setting register mn (SCRmn)

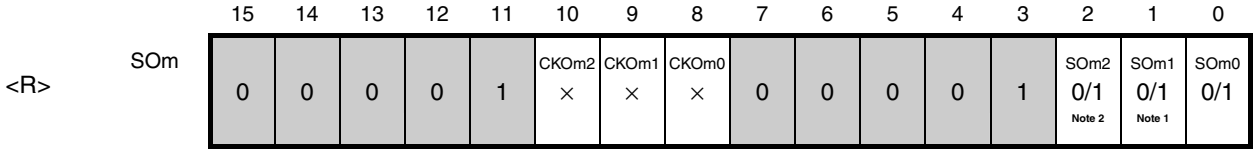


(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOm) … Sets only the bits of the target channel.

<R>



Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

(**Remark** is listed on the next page.)

Figure 14-66. Example of Contents of Registers for Slave Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (2/2)

(e) Serial output enable register m (SOEm) … Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 0/1 Note 2	SOEm1 0/1 Note 1	SOEm0 0/1

(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

<R>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 2	SSm1 0/1	SSm0 0/1

Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

78K0R/KF3-L (μ PD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KF3-L (μ PD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

78K0R/KG3-L (μ PD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KG3-L (μ PD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

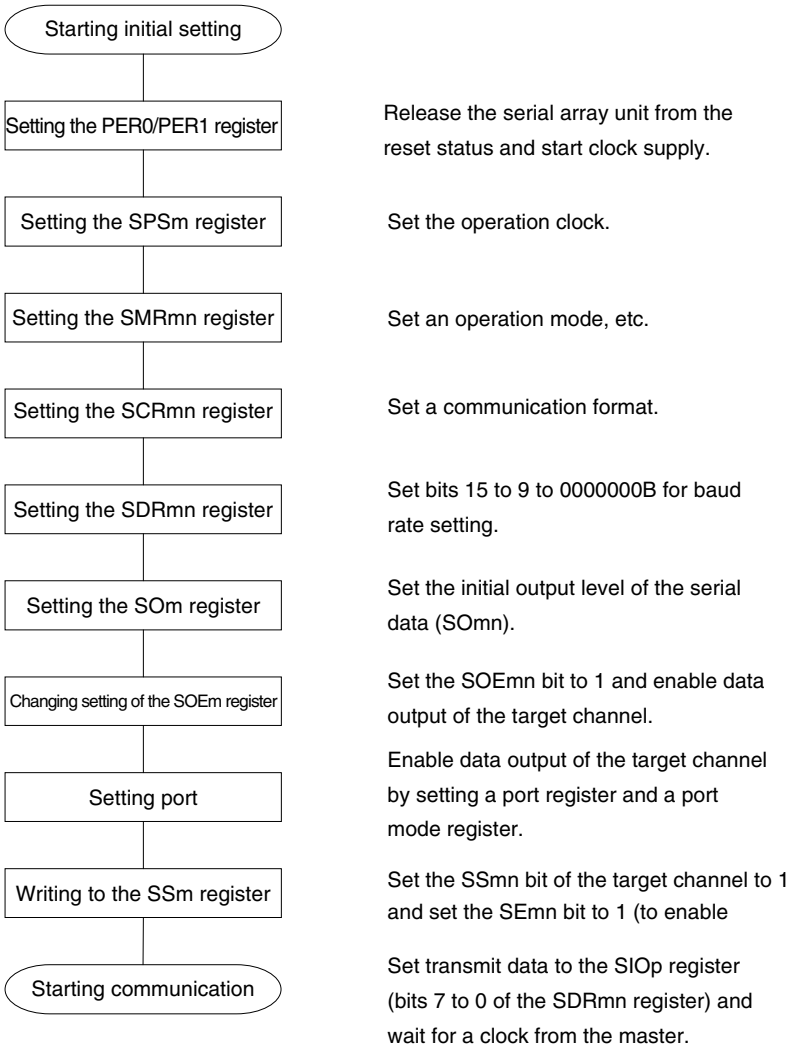
2. ☐ : Setting is fixed in the CSI master transmission mode, ▒ : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

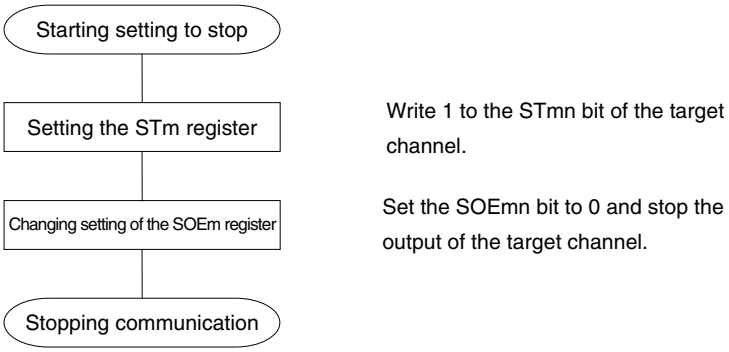
Figure 14-67. Initial Setting Procedure for Slave Transmission/Reception



Cautions 1. After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

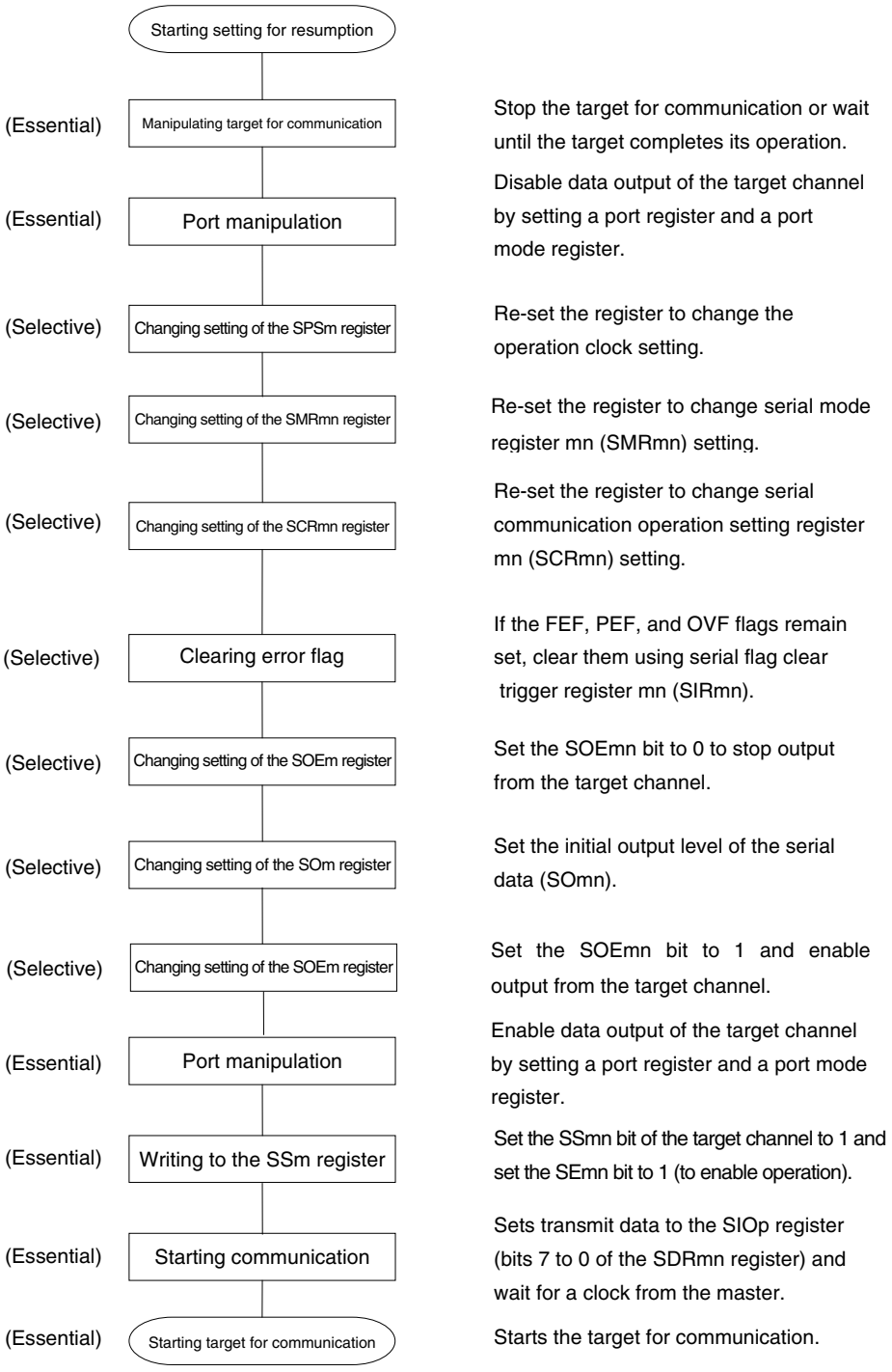
2. Be sure to set transmit data to the SIOp register before the clock from the master is started.

Figure 14-68. Procedure for Stopping Slave Transmission/Reception



Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set serial output register m (SOm) (see **Figure 14-69 Procedure for Resuming Slave Transmission/Reception**).

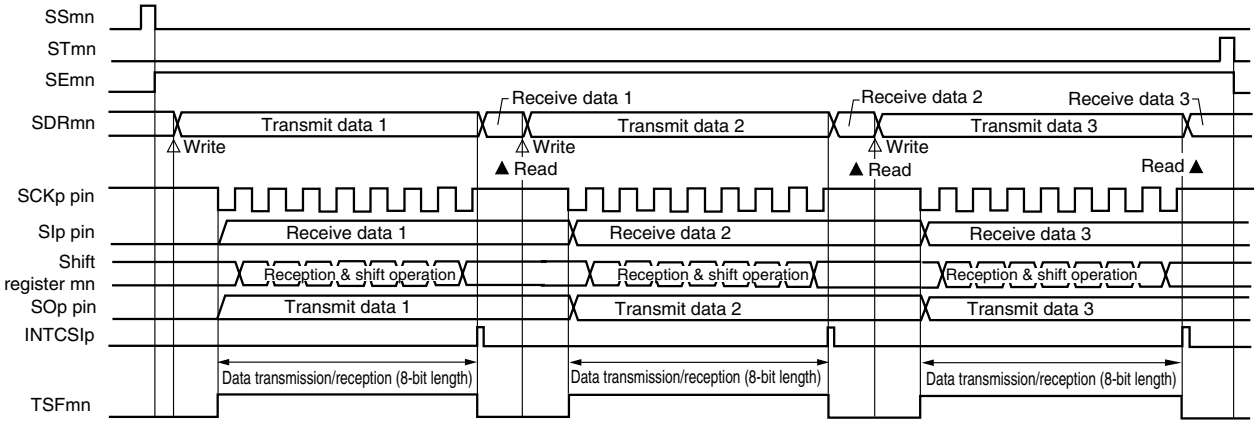
Figure 14-69. Procedure for Resuming Slave Transmission/Reception



Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

(3) Processing flow (in single-transmission/reception mode)

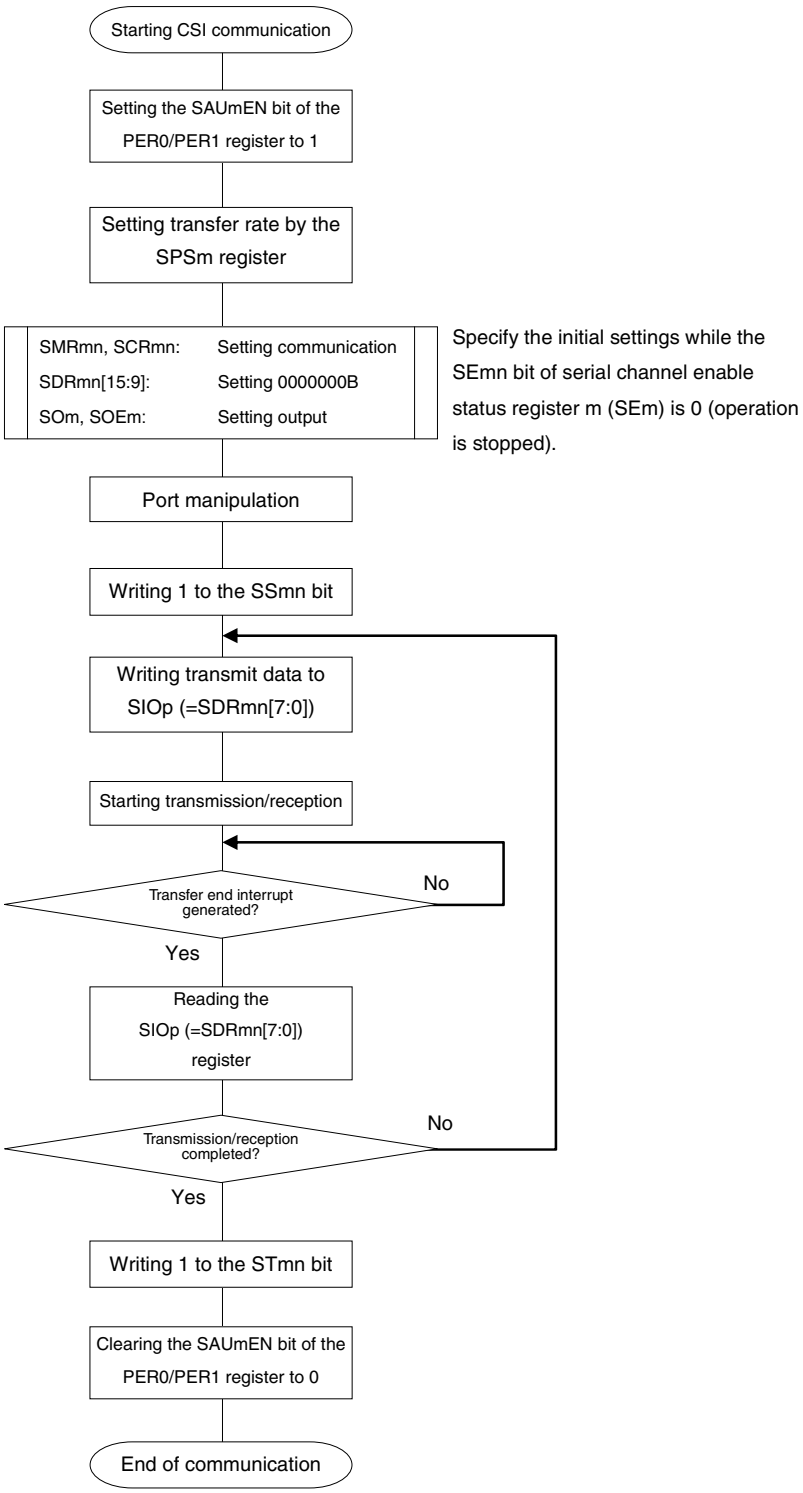
Figure 14-70. Timing Chart of Slave Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

Figure 14-71. Flowchart of Slave Transmission/Reception (in Single- Transmission/Reception Mode)

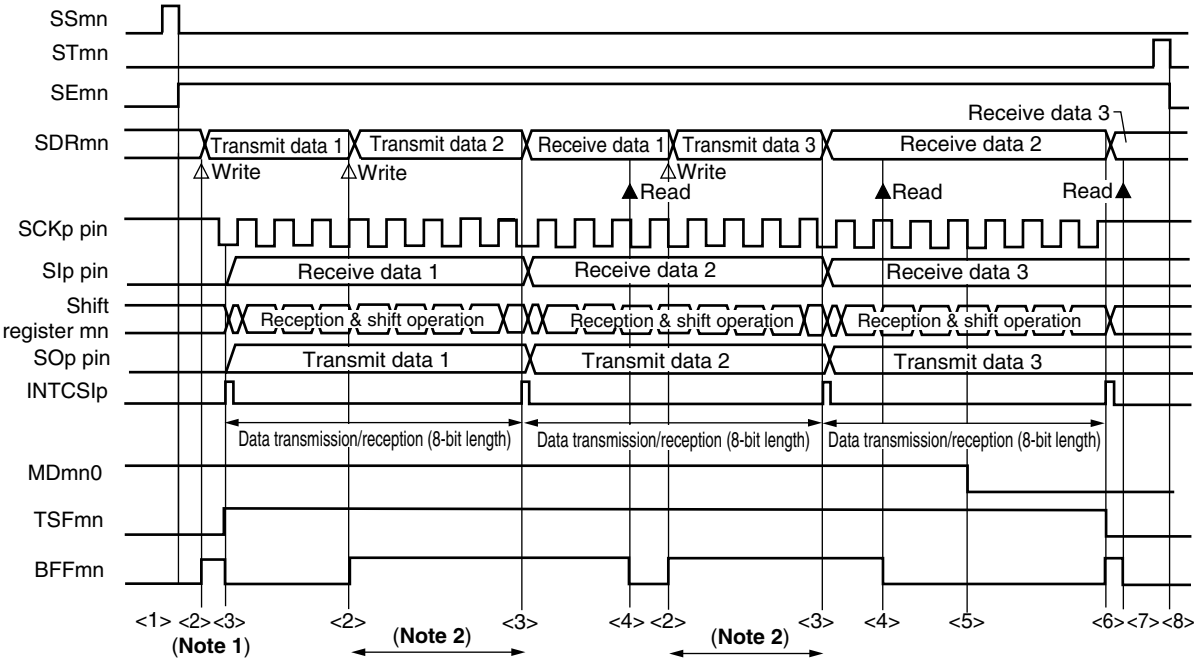


Cautions 1. After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

2. Be sure to set transmit data to the SIOp register before the clock from the master is started.

(4) Processing flow (in continuous transmission/reception mode)

Figure 14-72. Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Notes 1. If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

2. The transmit data can be read by reading the SDRmn register during this period. At this time, the transfer operation is not affected.

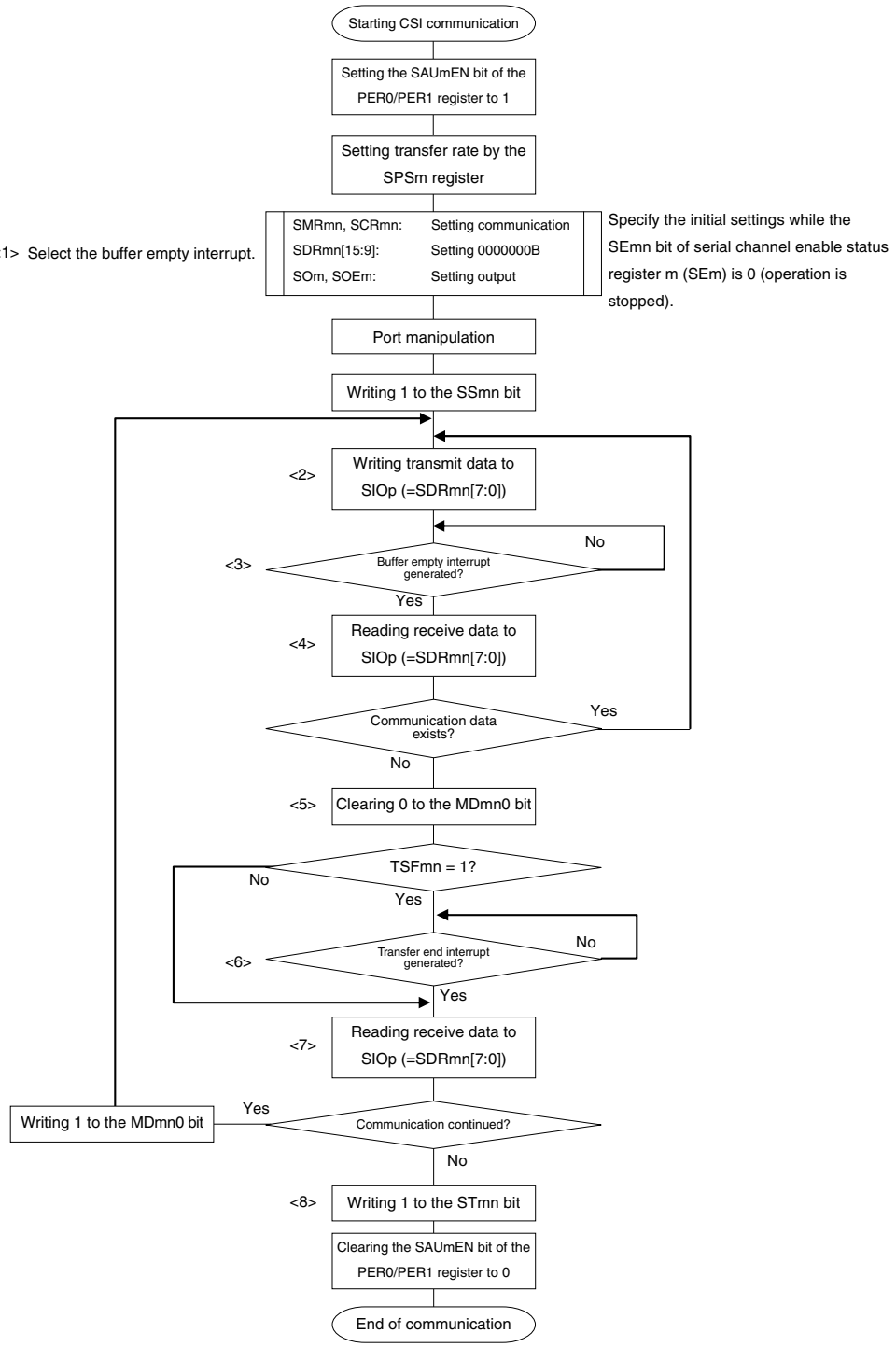
Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last transmit data.

Remarks 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 14-73 Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**.

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

Figure 14-73. Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)



Cautions 1. After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

2. Be sure to set transmit data to the SIOp register before the clock from the master is started.

Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 14-72 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**.

14.5.7 Calculating transfer clock frequency

The transfer clock frequency for 3-wire serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) communication can be calculated by the following expressions.

(1) Master

(Transfer clock frequency) = {Operation clock (f_{MCK}) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2 [Hz]

(2) Slave

(Transfer clock frequency) = {Frequency of serial clock ($\overline{SCK}$) supplied by master}[Note] [Hz]

Note The permissible maximum transfer clock frequency is f_{MCK}/6.

Remark The value of SDRmn[15:9] is the value of bits 15 to 9 of serial data register mn (SDRmn) (0000000B to 1111111B) and therefore is 0 to 127.

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 14-2. Selection of Operation Clock For 3-Wire Serial I/O

SMRmn Register	SPSm Register								Operation Clock (f_{MCK}) Note 1	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		f_{CLK} = 20 MHz
0	X	X	X	X	0	0	0	0	f_{CLK}	20 MHz
	X	X	X	X	0	0	0	1	$f_{CLK}/2$	10 MHz
	X	X	X	X	0	0	1	0	$f_{CLK}/2^2$	5 MHz
	X	X	X	X	0	0	1	1	$f_{CLK}/2^3$	2.5 MHz
	X	X	X	X	0	1	0	0	$f_{CLK}/2^4$	1.25 MHz
	X	X	X	X	0	1	0	1	$f_{CLK}/2^5$	625 kHz
	X	X	X	X	0	1	1	0	$f_{CLK}/2^6$	313 kHz
	X	X	X	X	0	1	1	1	$f_{CLK}/2^7$	156 kHz
	X	X	X	X	1	0	0	0	$f_{CLK}/2^8$	78.1 kHz
	X	X	X	X	1	0	0	1	$f_{CLK}/2^9$	39.1 kHz
	X	X	X	X	1	0	1	0	$f_{CLK}/2^{10}$	19.5 kHz
	X	X	X	X	1	0	1	1	$f_{CLK}/2^{11}$	9.77 kHz
	X	X	X	X	1	1	1	1	INTTM02 if m = 0 Note 2, setting prohibited if m = 1	
1	0	0	0	0	X	X	X	X	f_{CLK}	20 MHz
	0	0	0	1	X	X	X	X	$f_{CLK}/2$	10 MHz
	0	0	1	0	X	X	X	X	$f_{CLK}/2^2$	5 MHz
	0	0	1	1	X	X	X	X	$f_{CLK}/2^3$	2.5 MHz
	0	1	0	0	X	X	X	X	$f_{CLK}/2^4$	1.25 MHz
	0	1	0	1	X	X	X	X	$f_{CLK}/2^5$	625 kHz
	0	1	1	0	X	X	X	X	$f_{CLK}/2^6$	313 kHz
	0	1	1	1	X	X	X	X	$f_{CLK}/2^7$	156 kHz
	1	0	0	0	X	X	X	X	$f_{CLK}/2^8$	78.1 kHz
	1	0	0	1	X	X	X	X	$f_{CLK}/2^9$	39.1 kHz
	1	0	1	0	X	X	X	X	$f_{CLK}/2^{10}$	19.5 kHz
	1	0	1	1	X	X	X	X	$f_{CLK}/2^{11}$	9.77 kHz
	1	1	1	1	X	X	X	X	INTTM02 if m = 0 Note 2, setting prohibited if m = 1	
Other than above									Setting prohibited	

Notes 1. When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU). When selecting INTTM02 for the operation clock, also stop the timer array unit 0 (timer channel stop register 0 (TT0) = 00FFH).

2. SAU0 can be operated at a fixed division ratio of the subsystem clock, regardless of the f_{CLK} frequency (main system clock, sub system clock), by operating the interval timer for which $f_{SUB}/4$ Note 3 has been selected as the count clock (setting the TIS02 bit of timer input select register 0 (TIS0) to 1) and selecting INTTM02 by using the SPS0 register in channel 2 of TAU0. When changing f_{CLK}, however, SAU0 and TAU0 must be stopped as described in Note 1 above.

3. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Remarks 1. X: Don't care

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21

14.5.8 Procedure for processing errors that occurred during 3-wire serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) communication

The procedure for processing errors that occurred during 3-wire serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) communication is described in Figure 14-74.

Figure 14-74. Processing Procedure in Case of Overrun Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21

14.6 Operation of UART (UART0 to UART4) Communication

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using timer array unit 0 with an external interrupt (INTP0).

[Data transmission/reception]

- Data length of 5, 7, or 8 bits
- Select the MSB/LSB first
- Level setting of transmit/receive data and select of reverse
- Parity bit appending and parity check functions
- Stop bit appending

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

The LIN-bus is accepted in UART0 of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L and UART3 of the 78K0R/KF3-L, 78K0R/KG3-L.

[LIN-bus functions]

- Wakeup signal detection
- Sync break field (SBF) detection
- Sync field measurement, baud rate calculation

} Using the external interrupt (INTP0) and timer array unit 0

UART0 uses channels 0 and 1 of SAU0.
UART1 uses channels 2 and 3 of SAU0.
UART2 uses channels 0 and 1 of SAU1.
UART3 uses channels 2 and 3 of SAU1.
UART4 uses channels 0 and 1 of SAU2.

- 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0 (supporting LIN-bus)	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–

- 78K0R/KF3-L, 78K0R/KG3-L

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	CSI20	UART2	IIC20
	1	–		–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–
2 Note	0	CSI40	UART4	–
	1	CSI41		–

Note Serial array unit 2 is only mounted in the μPD78F1027 to 78F1030.

Caution When using serial array unit as UARTs, the channels of both the transmitting side (even-number channel) and the receiving side (odd-number channel) can be used only as UARTs.

UART performs the following four types of communication operations.

- UART transmission (See **14.6.1**.)
- UART reception (See **14.6.2**.)
- LIN transmission (UART0 or UART3 only) (See **14.7.1**.)
- LIN reception (UART0 or UART3 only) (See **14.7.2**.)

14.6.1 UART transmission

UART transmission is an operation to transmit data from the 78K0R/Kx3-L to another device asynchronously (start-stop synchronization).

Of two channels used for UART, the even channel is used for UART transmission.

UART	UART0	UART1	UART2 Note 1	UART3 Note 1	UART4 Note 2
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1	Channel 2 of SAU1	Channel 0 of SAU2
Pins used	TxD0	TxD1	TxD2	TxD3	TxD4
Interrupt	INTST0	INTST1	INTST2	INTST3	INTST4
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.				
Error detection flag	None				
Transfer data length	5, 7, or 8 bits				
Transfer rate	Max. $f_{MCK}/6$ [bps] (SDRmn [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{11} \times 128)$ [bps] Note 3				
Data phase	Forward output (default: high level) Reverse output (default: low level)				
Parity bit	The following selectable • No parity bit • Appending 0 parity • Appending even parity • Appending odd parity				
Stop bit	The following selectable • Appending 1 bit • Appending 2 bits				
Data direction	MSB or LSB first				

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. UART4 is only mounted in the 78K0R/KF3-L (μ PD78F1027, 78F1028) and 78K0R/KG3-L (μ PD78F1029, 78F1030).

3. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

Remarks 1. f_{MCK}: Operation clock frequency of target channel
f_{CLK}: System clock frequency

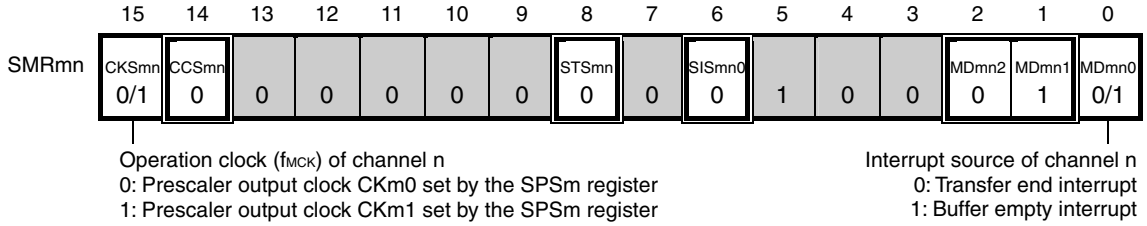
2. m: Unit number (m = 0 to 2), n: Channel number (n = 0, 2)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02
78K0R/KF3-L (μ PD78F1010, 78F1011, 78F1012): mn = 00, 02, 10, 12
78K0R/KF3-L (μ PD78F1027, 78F1028): mn = 00, 02, 10,12, 20
78K0R/KG3-L (μ PD78F1013, 78F1014): mn = 00, 02, 10, 12
78K0R/KG3-L (μ PD78F1029, 78F1030): mn = 00, 02, 10,12, 20

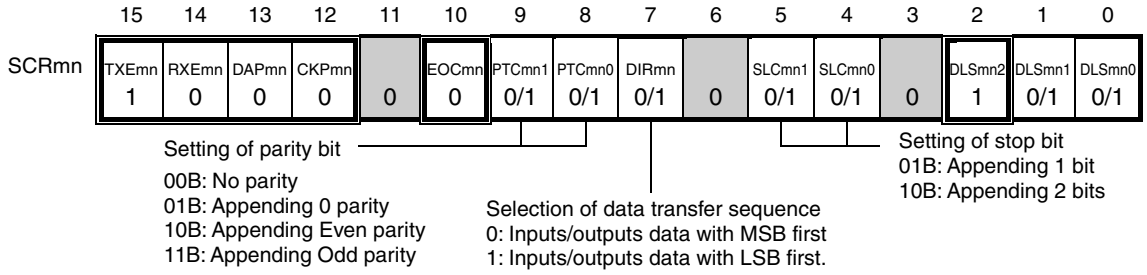
(1) Register setting

Figure 14-75. Example of Contents of Registers for UART Transmission of UART (UART0 to UART4) (1/2)

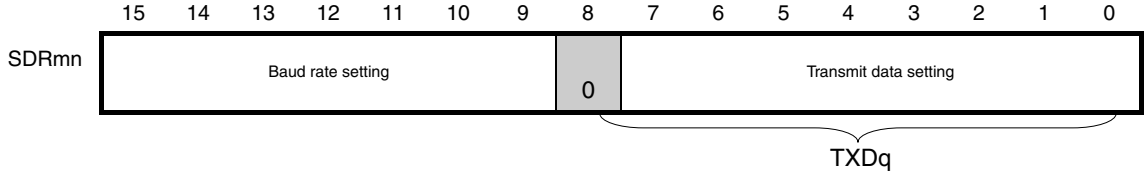
(a) Serial mode register mn (SMRmn)



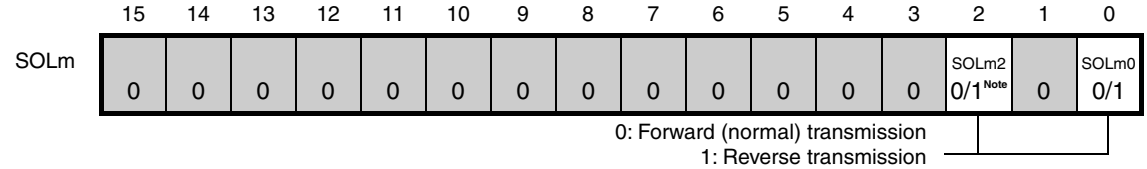
(b) Serial communication operation setting register mn (SCRmn)



(c) Serial data register mn (SDRmn) (lower 8 bits: TXDq)



(d) Serial output level register m (SOLm) … Sets only the bits of the target channel.



Note This bit is invalid while operating serial allay unit 2.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0, 2), q: UART number (p = 0 to 4)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00, 02, q = 0, 1
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 00, 02, 10, 12, q = 0 to 3
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 00, 02, 10, 12, 20, q = 0 to 4
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 00, 02, 10, 12, q = 0 to 3
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 00, 02, 10, 12, 20, q = 0 to 4

2. □ : Setting is fixed in the CSI master transmission mode, ▒ : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

Figure 14-75. Example of Contents of Registers for UART Transmission of UART (UART0 to UART4) (2/2)

(e) Serial output register m (SOm) … Sets only the bits of the target channel.

<R>

SOm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	CKOm2 ×	CKOm1 ×	CKOm0 ×	0	0	0	0	1	SOm2 0/1 Notes 2, 3	SOm1 ×	SOm0 0/1 Note 3

0: Serial data output value is “0”
1: Serial data output value is “1”

(f) Serial output enable register m (SOEm) … Sets only the bits of the target channel to 1.

<R>

SOEm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 0/1	SOEm1 ×	SOEm0 0/1

(g) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

<R>

SSm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 2	SSm1 ×	SSm0 0/1

Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

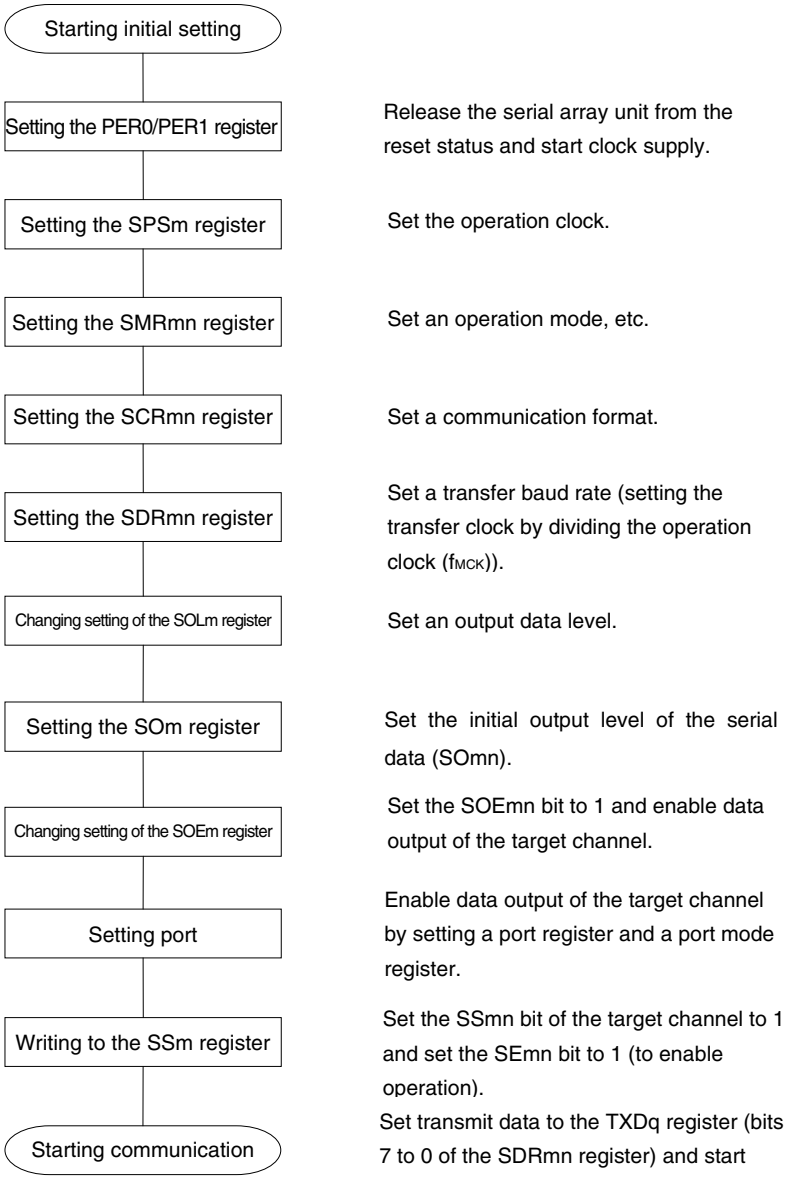
3. Before transmission is started, be sure to set to 1 when the SOLmn bit of the target channel is set to 0, and set to 0 when the SOLmn bit of the target channel is set to 1. The value varies depending on the communication data during communication operation.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0, 2), q: UART number (p = 0 to 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, q = 0, 1
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00, 02, 10, 12, q = 0 to 3
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00, 02, 10, 12, 20, q = 0 to 4
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00, 02, 10, 12, q = 0 to 3
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00, 02, 10, 12, 20, q = 0 to 4

2. ☐: Setting is fixed in the CSI master transmission mode, ▒: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

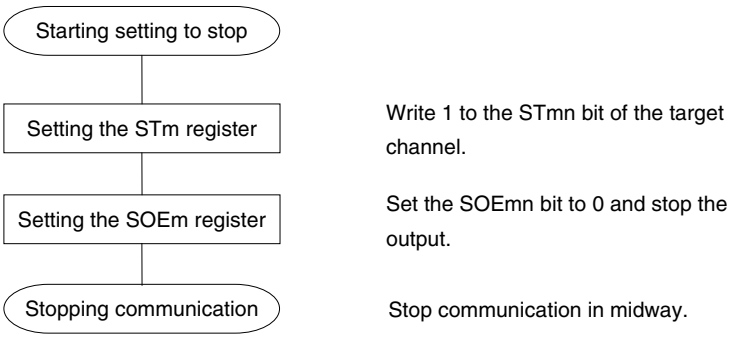
(2) Operation procedure

Figure 14-76. Initial Setting Procedure for UART Transmission



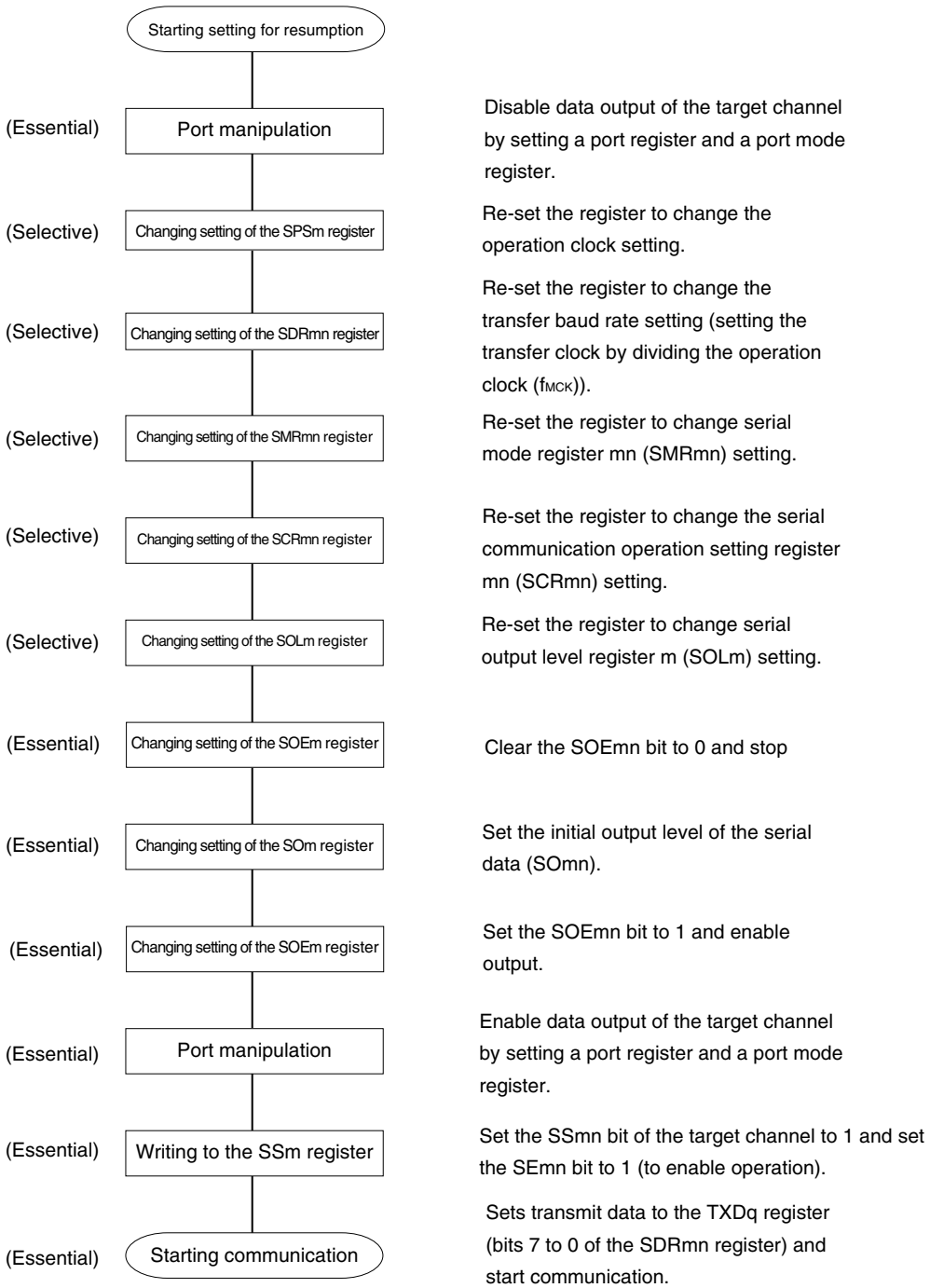
Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Figure 14-77. Procedure for Stopping UART Transmission



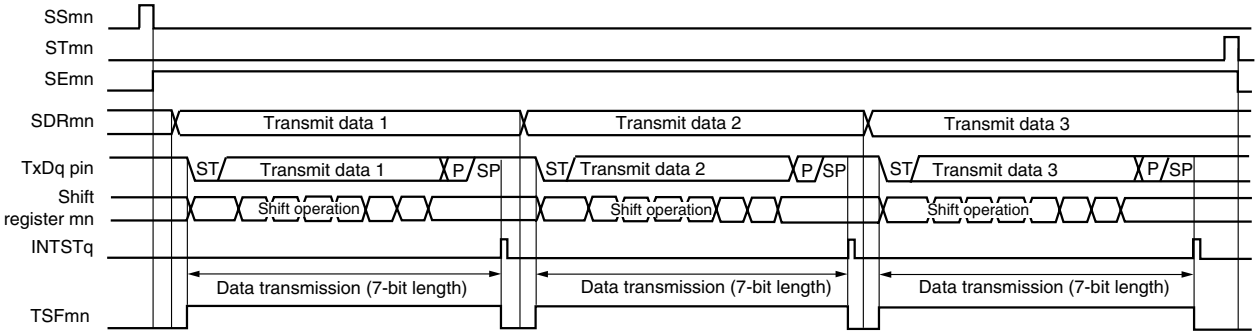
Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set serial output register m (SOm) (see **Figure 14-78 Procedure for Resuming UART Transmission**).

Figure 14-78. Procedure for Resuming UART Transmission



(3) Processing flow (in single-transmission mode)

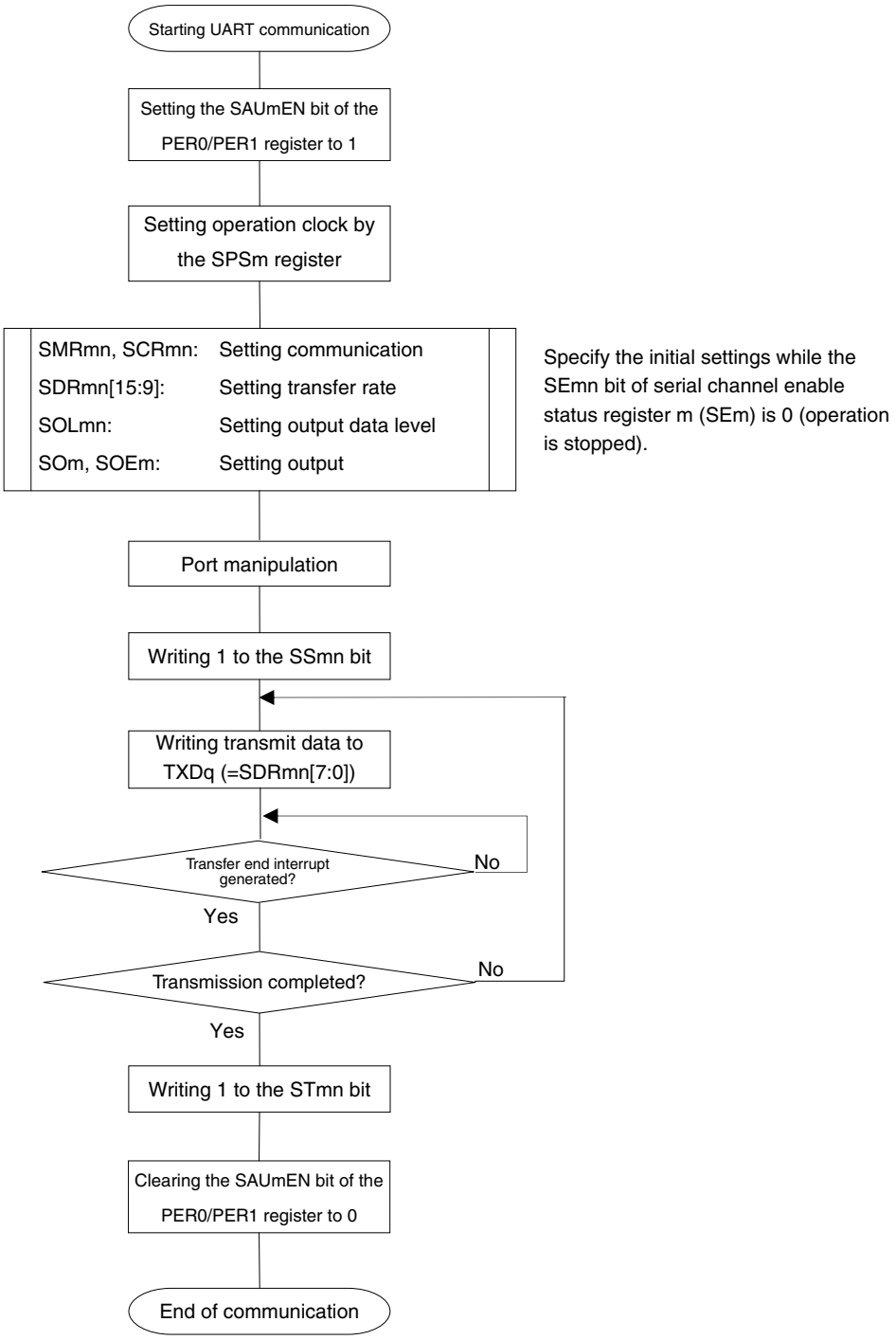
Figure 14-79. Timing Chart of UART Transmission (in Single-Transmission Mode)



Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), q: UART number (p = 0 to 4)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00, 02, q = 0, 1
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 00, 02, 10, 12, q = 0 to 3
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 00, 02, 10, 12, 20, q = 0 to 4
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 00, 02, 10, 12, q = 0 to 3
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 00, 02, 10, 12, 20, p = 0 to 4

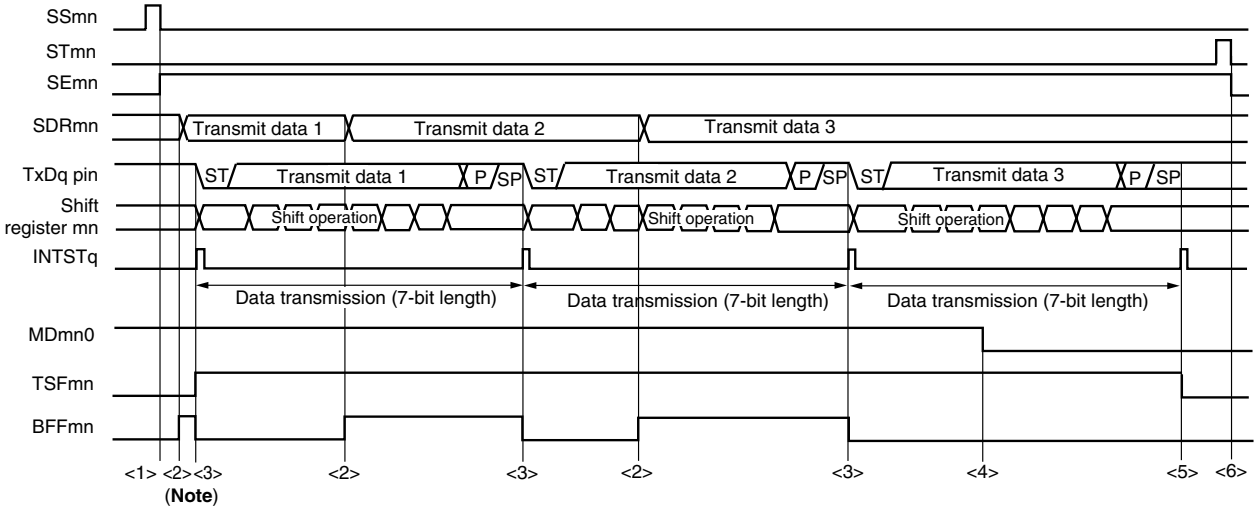
Figure 14-80. Flowchart of UART Transmission (in Single-Transmission Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

(4) Processing flow (in continuous transmission mode)

Figure 14-81. Timing Chart of UART Transmission (in Continuous Transmission Mode)

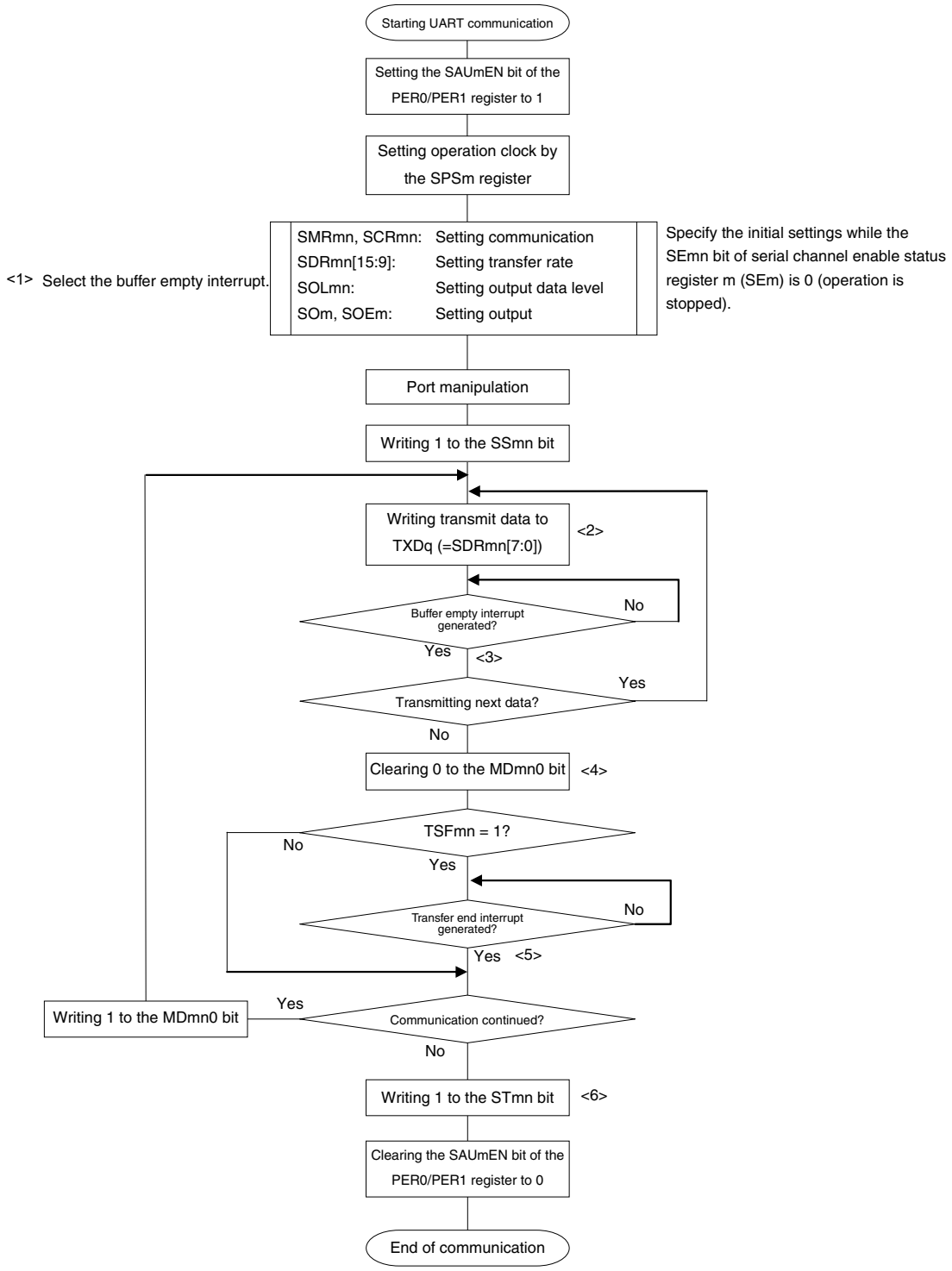


Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution The MDmn0 bit of serial mode register mn (SSRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), q: UART number (p = 0 to 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, q = 0, 1
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00, 02, 10, 12, p = 0 to 3
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00, 02, 10, 12, 20, q = 0 to 4
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00, 02, 10, 12, p = 0 to 3
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00, 02, 10, 12, 20, p = 0 to 4

Figure 14-82. Flowchart of UART Transmission (in Continuous Transmission Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Remark <1> to <6> in the figure correspond to <1> to <6> in **Figure 14-81 Timing Chart of UART Transmission (in Continuous Transmission Mode)**.

14.6.2 UART reception

UART reception is an operation wherein the 78K0R/Kx3-L asynchronously receives data from another device (start-stop synchronization).

For UART reception, the odd-number channel of the two channels used for UART is used. The SMR register of both the odd- and even-numbered channels must be set.

UART	UART0	UART1	UART2 Note 1	UART3 Note 1	UART4 Note 2
Target channel	Channel 1 of SAU0	Channel 3 of SAU0	Channel 1 of SAU1	Channel 3 of SAU1	Channel 1 of SAU2
Pins used	RxD0	RxD1	RxD2	RxD3	RxD4
Interrupt	INTSR0	INTSR1	INTSR2	INTSR3	INTSR4
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)				
Error interrupt	INTSRE0	INTSRE1	INTSRE2	INTSRE3	INTSRE4
Error detection flag	• Framing error detection flag (FEFmn) • Parity error detection flag (PEFmn) • Overrun error detection flag (OVFmn)				
Transfer data length	5, 7 or 8 bits				
Transfer rate	Max. $f_{MCK}/6$ [bps] (SDRmn [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{11} \times 128)$ [bps] Note 3				
Data phase	Forward output (default: high level) Reverse output (default: low level)				
Parity bit	The following selectable • No parity bit (no parity check) • Appending 0 parity (no parity check) • Appending even parity • Appending odd parity				
Stop bit	Appending 1 bit				
Data direction	MSB or LSB first				

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. UART4 is only mounted in the 78K0R/KF3-L (μ PD78F1027, 78F1028) and 78K0R/KG3-L (μ PD78F1029, 78F1030).

3. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

Remarks 1. f_{MCK}: Operation clock frequency of target channel
f_{CLK}: System clock frequency

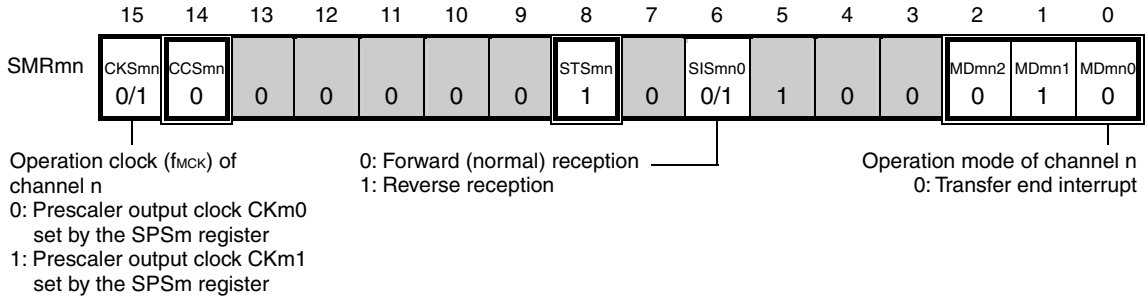
2. m: Unit number (m = 0 to 2), n: Channel number (n = 1, 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 01, 03
78K0R/KF3-L (μ PD78F1010, 78F1011, 78F1012): mn = 01, 03, 11, 13
78K0R/KF3-L (μ PD78F1027, 78F1028): mn = 01, 03, 11, 13, 21
78K0R/KG3-L (μ PD78F1013, 78F1014): mn = 01, 03, 11, 13
78K0R/KG3-L (μ PD78F1029, 78F1030): mn = 01, 03, 11, 13, 21

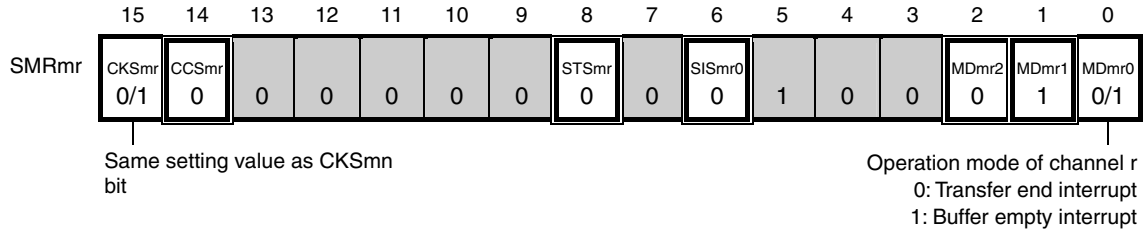
(1) Register setting

Figure 14-83. Example of Contents of Registers for UART Reception of UART (UART0 to UART4) (1/2)

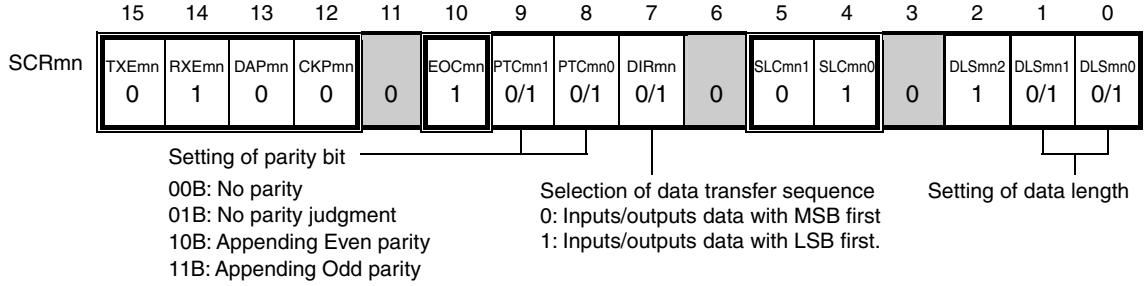
(a) Serial mode register mn (SMRmn)



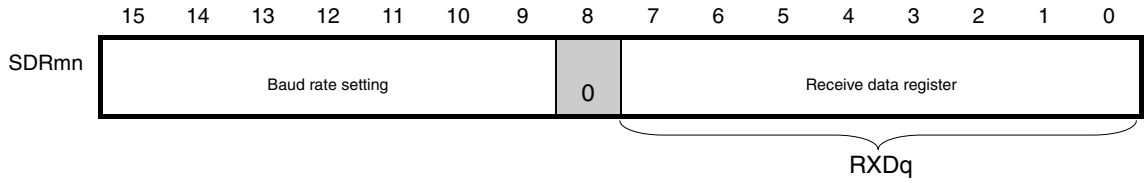
(b) Serial mode register mr (SMRmr)



(c) Serial communication operation setting register mn (SCRmn)



(d) Serial data register mn (SDRmn) (lower 8 bits: RXDq)



Caution For the UART reception, be sure to set SMRmr of channel r that is to be paired with channel n.

(**Remarks** are listed on the next page.)

Figure 14-83. Example of Contents of Registers for UART Reception of UART (UART0 to UART4) (2/2)

(e) Serial output register m (SOm) … The register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm						CKOm2	CKOm1	CKOm0						SOm2	SOm1	SOm0
	0	0	0	0	1	×	×	×	0	0	0	0	1	×	×	×

(f) Serial output enable register m (SOEm) …The register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm														SOEm2	SOEm1	SOEm0
	0	0	0	0	0	0	0	0	0	0	0	0	0	×	×	×

(g) Serial channel start register m (SSm) … Sets only the bits of the target channel is 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm													SSm3	SSm2	SSm1	SSm0
	0	0	0	0	0	0	0	0	0	0	0	0	0/1 Note	×	0/1	×

Note This bit is invalid while operating serial allay unit 2.

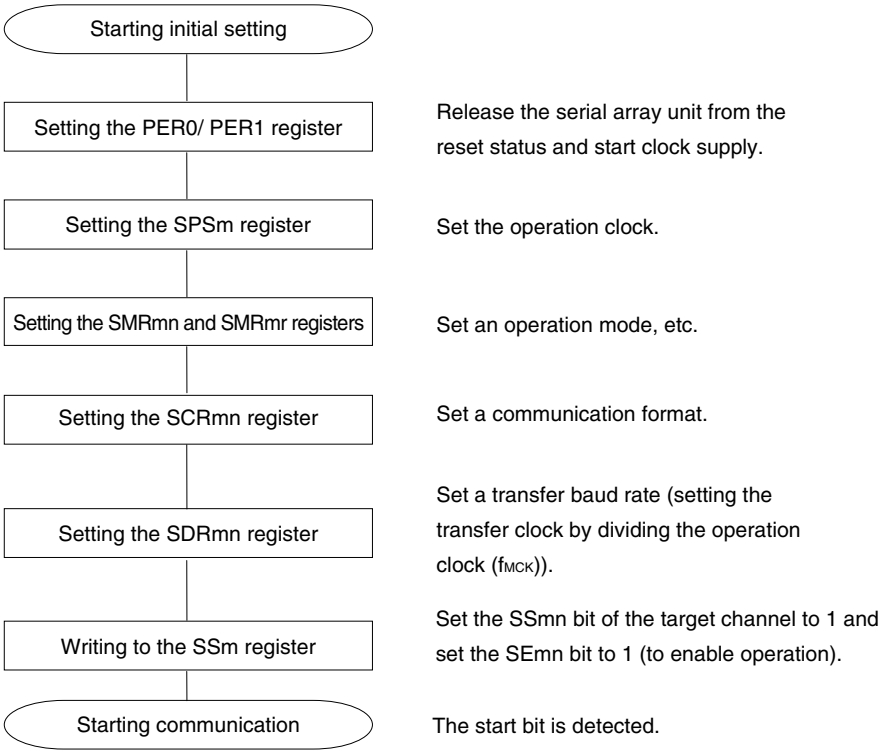
Caution For the UART reception, be sure to set SMRmr of channel r that is to be paired with channel n.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 1, 3),
r: Channel number (r = n – 1), q: UART number (q = 0 to 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 01, 03, q = 0, 1
78K0R/KF3-L(μ PD78F1010, 78F1011, 78F1012): mn = 01, 03, 11, 13, q = 0 to 3
78K0R/KF3-L(μ PD78F1027, 78F1028): mn = 01, 03, 11,13, 21, q = 0 to 4
78K0R/KG3-L(μ PD78F1013, 78F1014): mn = 01, 03, 11, 13, q = 0 to 3
78K0R/KG3-L(μ PD78F1029, 78F1030): mn = 01, 03, 11,13, 21, q = 0 to 4

2. □: Setting is fixed in the CSI master transmission mode, ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 14-84. Initial Setting Procedure for UART Reception



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Figure 14-85. Procedure for Stopping UART Reception

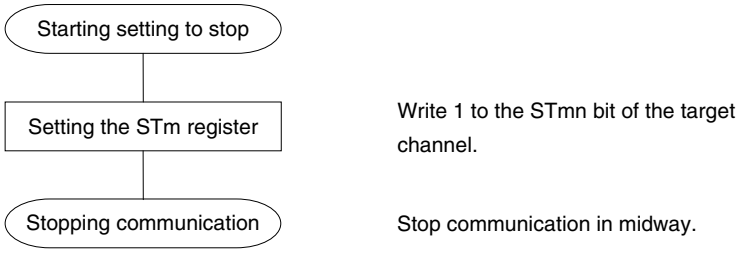
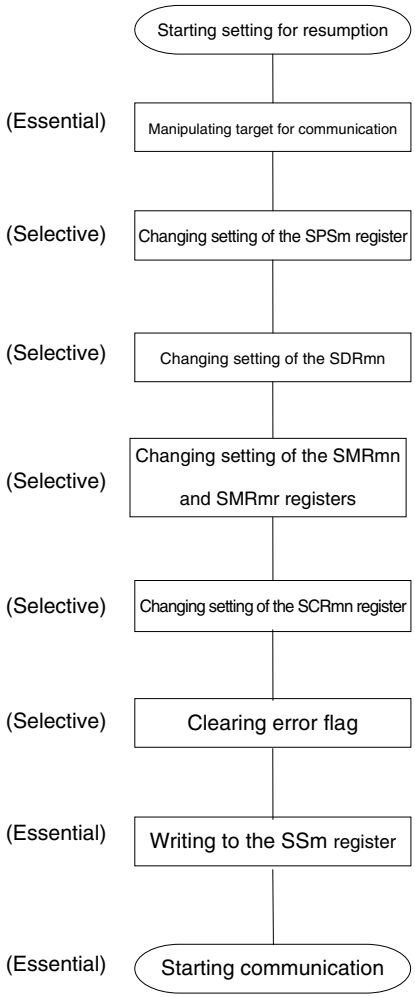


Figure 14-86. Procedure for Resuming UART Reception



Stop the target for communication or wait until the target completes its operation.

Re-set the register to change the operation clock setting.

Re-set the register to change the transfer baud rate setting (setting the transfer clock by dividing the operation clock (f_{MCK})).

Re-set the registers to change serial mode registers mn, mr (SMRmn, SMRmr) setting.

Re-set the register to change serial communication operation setting register mn (SCRmn) setting.

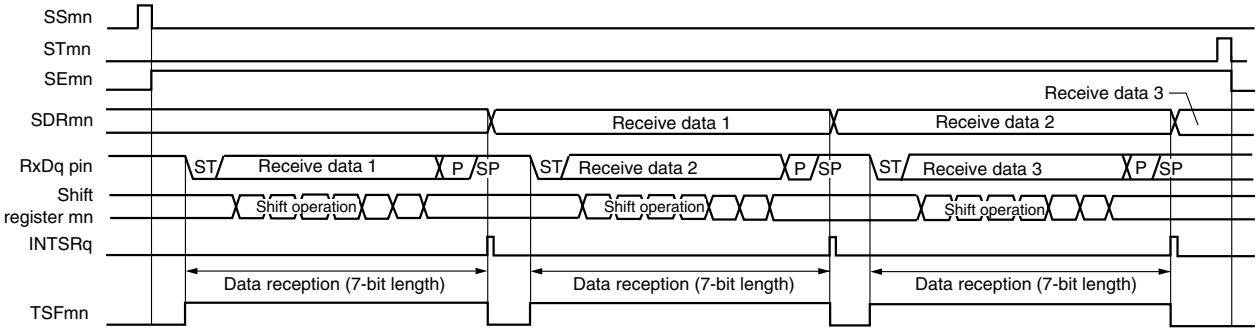
If the FEF, PEF, and OVF flags remain set, clear them using serial flag clear trigger register mn (SIRmn).

Set the SSmn bit of the target channel to 1 and set the SEmn bit to 1 (to enable operation).

The start bit is detected.

(3) Processing flow

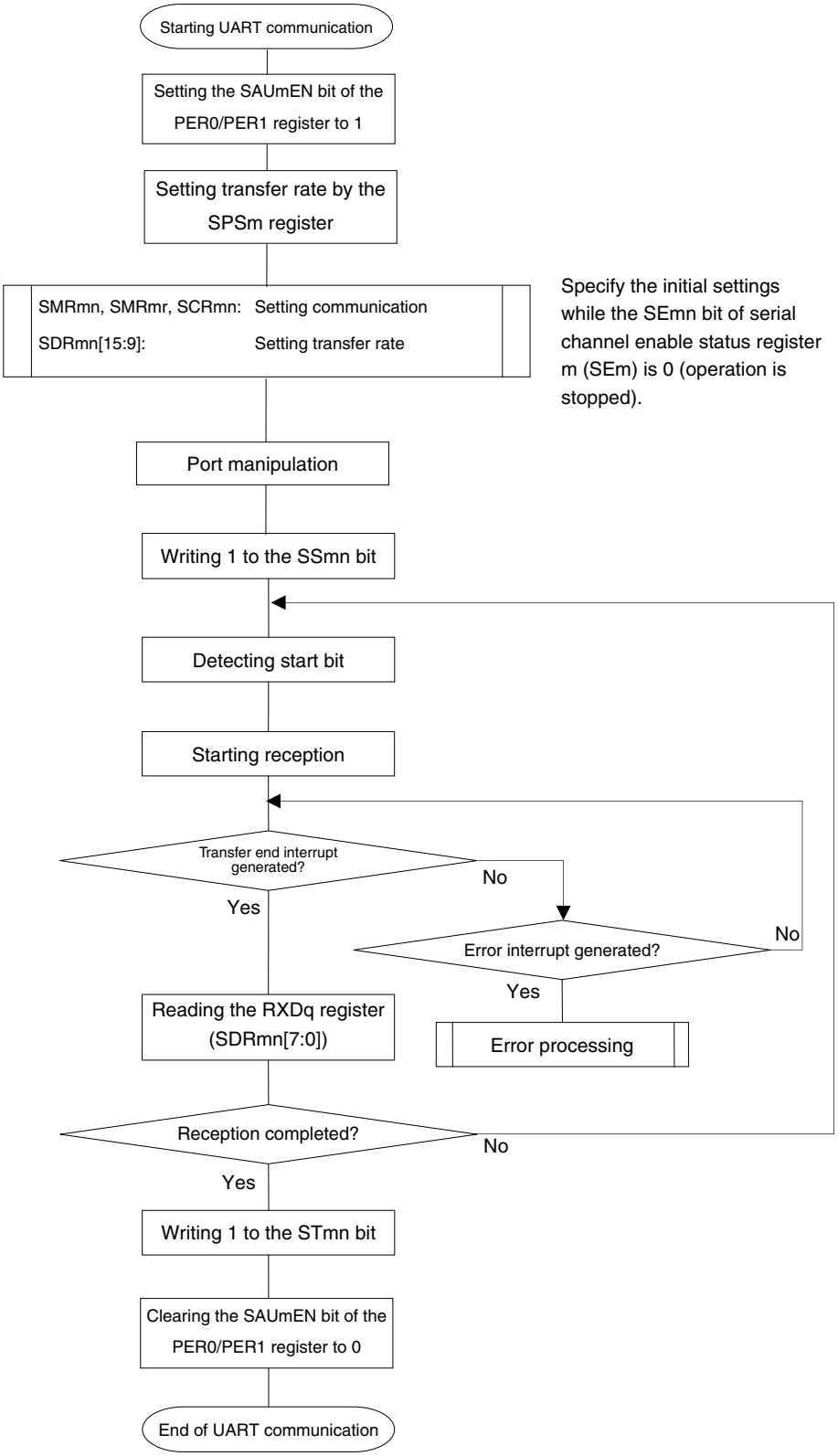
Figure 14-87. Timing Chart of UART Reception



Remark m: Unit number (m = 0 to 2), n: Channel number (n = 1, 3),
r: Channel number (r = n – 1), q: UART number (q = 0 to 4)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 01, 03, q = 0, 1
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 01, 03, 11, 13, q = 0 to 3
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 01, 03, 11, 13, 21, q = 0 to 4
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 01, 03, 11, 13, q = 0 to 3
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 01, 03, 11, 13, 21, q = 0 to 4

Figure 14-88. Flowchart of UART Reception



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

14.6.3 Calculating baud rate

(1) Baud rate calculation expression

The baud rate for UART (UART0 to UART4) communication can be calculated by the following expressions.

(Baud rate) = {Operation clock (f_{MCK}) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2 [bps]

Caution Setting serial data register mn (SDRmn) SDRmn[15:9] = (0000000B, 0000001B) is prohibited.

Remarks 1. When UART is used, the value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000010B to 1111111B) and therefore is 2 to 127.

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 00 to 03
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 00 to 03, 10 to 13
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 00 to 03, 10 to 13
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 00 to 03, 10 to 13, 20, 21

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 14-3. Selection of Operation Clock For UART

SMRmn Register	SPSm Register								Operation Clock (f_{MCK}) Note 1	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		f_{CLK} = 20 MHz
0	X	X	X	X	0	0	0	0	f_{CLK}	20 MHz
	X	X	X	X	0	0	0	1	$f_{CLK}/2$	10 MHz
	X	X	X	X	0	0	1	0	$f_{CLK}/2^2$	5 MHz
	X	X	X	X	0	0	1	1	$f_{CLK}/2^3$	2.5 MHz
	X	X	X	X	0	1	0	0	$f_{CLK}/2^4$	1.25 MHz
	X	X	X	X	0	1	0	1	$f_{CLK}/2^5$	625 kHz
	X	X	X	X	0	1	1	0	$f_{CLK}/2^6$	313 kHz
	X	X	X	X	0	1	1	1	$f_{CLK}/2^7$	156 kHz
	X	X	X	X	1	0	0	0	$f_{CLK}/2^8$	78.1 kHz
	X	X	X	X	1	0	0	1	$f_{CLK}/2^9$	39.1 kHz
	X	X	X	X	1	0	1	0	$f_{CLK}/2^{10}$	19.5 kHz
	X	X	X	X	1	0	1	1	$f_{CLK}/2^{11}$	9.77 kHz
	X	X	X	X	1	1	1	1	INTTM02 if m = 0 Note 2, setting prohibited if m = 1	
1	0	0	0	0	X	X	X	X	f_{CLK}	20 MHz
	0	0	0	1	X	X	X	X	$f_{CLK}/2$	10 MHz
	0	0	1	0	X	X	X	X	$f_{CLK}/2^2$	5 MHz
	0	0	1	1	X	X	X	X	$f_{CLK}/2^3$	2.5 MHz
	0	1	0	0	X	X	X	X	$f_{CLK}/2^4$	1.25 MHz
	0	1	0	1	X	X	X	X	$f_{CLK}/2^5$	625 kHz
	0	1	1	0	X	X	X	X	$f_{CLK}/2^6$	313 kHz
	0	1	1	1	X	X	X	X	$f_{CLK}/2^7$	156 kHz
	1	0	0	0	X	X	X	X	$f_{CLK}/2^8$	78.1 kHz
	1	0	0	1	X	X	X	X	$f_{CLK}/2^9$	39.1 kHz
	1	0	1	0	X	X	X	X	$f_{CLK}/2^{10}$	19.5 kHz
	1	0	1	1	X	X	X	X	$f_{CLK}/2^{11}$	9.77 kHz
	1	1	1	1	X	X	X	X	INTTM02 if m = 0 Note 2, setting prohibited if m = 1	
Other than above									Setting prohibited	

Notes 1. When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU). When selecting INTTM02 for the operation clock, also stop the timer array unit 0 (timer channel stop register 0 (TT0) = 00FFH).

2. SAU0 can be operated at a fixed division ratio of the subsystem clock, regardless of the f_{CLK} frequency (main system clock, sub system clock), by operating the interval timer for which $f_{SUB}/4$ Note 3 has been selected as the count clock (setting the TIS02 bit of timer input select register 0 (TIS0) to 1) and selecting INTTM02 by using the SPS0 register in channel 2 of TAU0. When changing f_{CLK}, however, SAU0 and TAU0 must be stopped as described in Note 1 above.

3. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Remarks 1. X: Don't care

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 03, 10 to 13
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 03, 10 to 13
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 03, 10 to 13, 20, 211

(2) Baud rate error during transmission

The baud rate error of UART (UART0 to UART4) communication during transmission can be calculated by the following expression. Make sure that the baud rate at the transmission side is within the permissible baud rate range at the reception side.

(Baud rate error) = (Calculated baud rate value) ÷ (Target baud rate) × 100 − 100 [%]

Here is an example of setting a UART baud rate at f_{CLK} = 20 MHz.

UART Baud Rate (Target Baud Rate)	f_{CLK} = 20 MHz			
	Operation Clock (f_{MCK})	SDRmn[15:9]	Calculated Baud Rate	Error from Target Baud Rate
300 bps	$f_{CLK}/2^9$	64	300.48 bps	+0.16 %
600 bps	$f_{CLK}/2^8$	64	600.96 bps	+0.16 %
1200 bps	$f_{CLK}/2^7$	64	1201.92 bps	+0.16 %
2400 bps	$f_{CLK}/2^6$	64	2403.85 bps	+0.16 %
4800 bps	$f_{CLK}/2^5$	64	4807.69 bps	+0.16 %
9600 bps	$f_{CLK}/2^4$	64	9615.38 bps	+0.16 %
19200 bps	$f_{CLK}/2^3$	64	19230.8 bps	+0.16 %
31250 bps	$f_{CLK}/2^3$	39	31250.0 bps	±0.0 %
38400 bps	$f_{CLK}/2^2$	64	38461.5 bps	+0.16 %
76800 bps	$f_{CLK}/2$	64	76923.1 bps	+0.16 %
153600 bps	f_{CLK}	64	153846 bps	+0.16 %
312500 bps	f_{CLK}	31	312500 bps	±0.0 %

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0, 2)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00, 02, 10, 12
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00, 02, 10, 12, 20
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00, 02, 10, 12
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00, 02, 10, 12, 20

(3) Permissible baud rate range for reception

The permissible baud rate range for reception during UART (UART0 to UART4) communication can be calculated by the following expression. Make sure that the baud rate at the transmission side is within the permissible baud rate range at the reception side.

$$\text{(Maximum receivable baud rate)} = \frac{2 \times k \times Nfr}{2 \times k \times Nfr - k + 2} \times Brate$$

$$\text{(Minimum receivable baud rate)} = \frac{2 \times k \times (Nfr - 1)}{2 \times k \times Nfr - k - 2} \times Brate$$

Brate: Calculated baud rate value at the reception side (See **14.6.3 (1) Baud rate calculation expression**.)

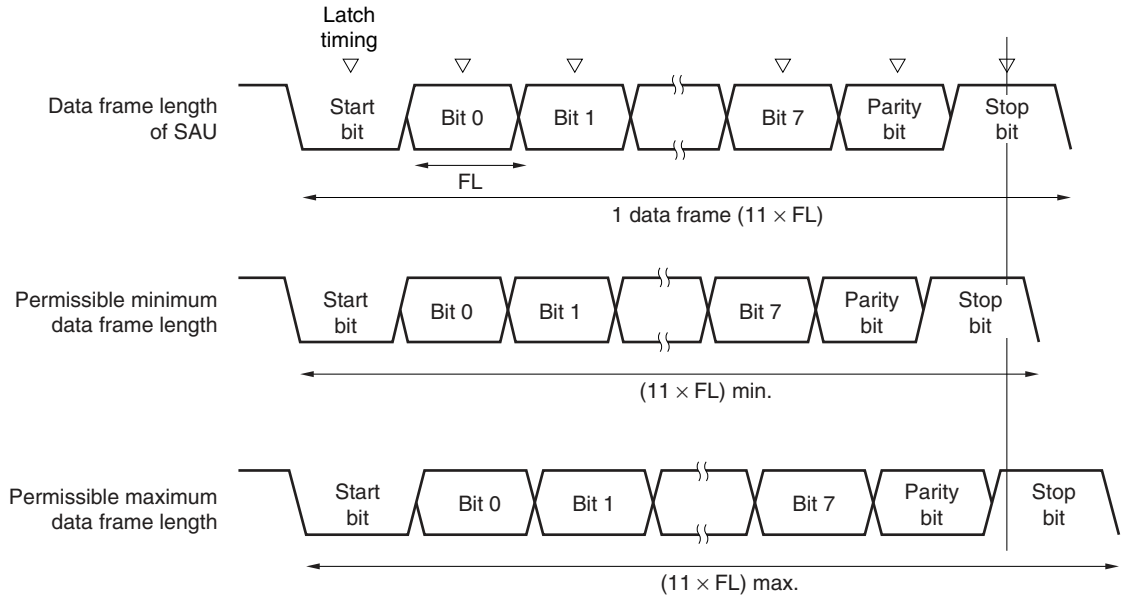
k: SDRmn[15:9] + 1

Nfr: 1 data frame length [bits]
= (Start bit) + (Data length) + (Parity bit) + (Stop bit)

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 1, 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 01, 03
78K0R/KF3-L(μPD78F1010, 78F1011, 78F1012):	mn = 01, 03, 11, 13
78K0R/KF3-L(μPD78F1027, 78F1028):	mn = 01, 03, 11, 13, 21
78K0R/KG3-L(μPD78F1013, 78F1014):	mn = 01, 03, 11, 13
78K0R/KG3-L(μPD78F1029, 78F1030):	mn = 01, 03, 11, 13, 21

Figure 14-89. Permissible Baud Rate Range for Reception (1 Data Frame Length = 11 Bits)



As shown in Figure 14-89, the timing of latching receive data is determined by the division ratio set by bits 15 to 9 of serial data register mn (SDRmn) after the start bit is detected. If the last data (stop bit) is received before this latch timing, the data can be correctly received.

14.6.4 Procedure for processing errors that occurred during UART (UART0 to UART4) communication

The procedure for processing errors that occurred during UART (UART0 to UART4) communication is described in Figures 14-90 and 14-91.

Figure 14-90. Processing Procedure in Case of Parity Error or Overrun Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

Figure 14-91. Processing Procedure in Case of Framing Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.
Sets the STmn bit of serial channel stop register m (STm) to 1. →	The SEmn bit of serial channel enable status register m (SEm) is set to 0 and channel n stops operating.	
Synchronization with other party of communication		Synchronization with the other party of communication is re-established and communication is resumed because it is considered that a framing error has occurred because the start bit has been shifted.
Sets the SSmn bit of serial channel start register m (SSm) to 1. →	The SEmn bit of serial channel enable status register m (SEm) is set to 1 and channel n is enabled to operate.	

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 03, 10 to 13
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 03, 10 to 13
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 03, 10 to 13, 20, 21

14.7 LIN Communication Operation

14.7.1 LIN transmission

Of UART transmission, UART0 of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L and UART3 of the 78K0R/KF3-L, 78K0R/KG3-L support LIN communication.

The following UART channels are used for LIN transmission.

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: Channel 0 of SAU0

78K0R/KF3-L, 78K0R/KG3-L: Channel 2 of SAU1

UART	UART0 Note 1	UART1	UART2	UART3 Note 1	UART4 Note 2
Support of LIN communication	Supported	Not supported	Not supported	Supported	Not supported
Target channel	Channel 0 of SAU0	–	–	Channel 2 of SAU1	–
Pins used	TxD0	–	–	TxD3	–
Interrupt	INTST0	–	–	INTST3	–
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.				
Error detection flag	None				
Transfer data length	8 bits				
Transfer rate	Max. f_{MCK}/6 [bps] (SDRmn [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{11} \times 128)$ [bps] Note 3				
Data phase	Forward output (default: high level) Reverse output (default: low level)				
Parity bit	The following selectable • No parity bit • Appending 0 parity • Appending even parity • Appending odd parity				
Stop bit	The following selectable • Appending 1 bit • Appending 2 bits				
Data direction	MSB or LSB first				

Notes 1. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: UART0
78K0R/KF3-L, 78K0R/KG3-L: UART3

2. UART4 is only mounted in the 78K0R/KF3-L (μ PD78F1027, 78F1028) and 78K0R/KG3-L (μ PD78F1029, 78F1030).

3. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

Remarks 1. f_{MCK}: Operation clock frequency of target channel
f_{CLK}: System clock frequency

2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00
78K0R/KF3-L, 78K0R/KG3-L: mn = 12

LIN stands for Local Interconnect Network and is a low-speed (1 to 20 kbps) serial communication protocol designed to reduce the cost of an automobile network.

Communication of LIN is single-master communication and up to 15 slaves can be connected to one master.

The slaves are used to control switches, actuators, and sensors, which are connected to the master via LIN.

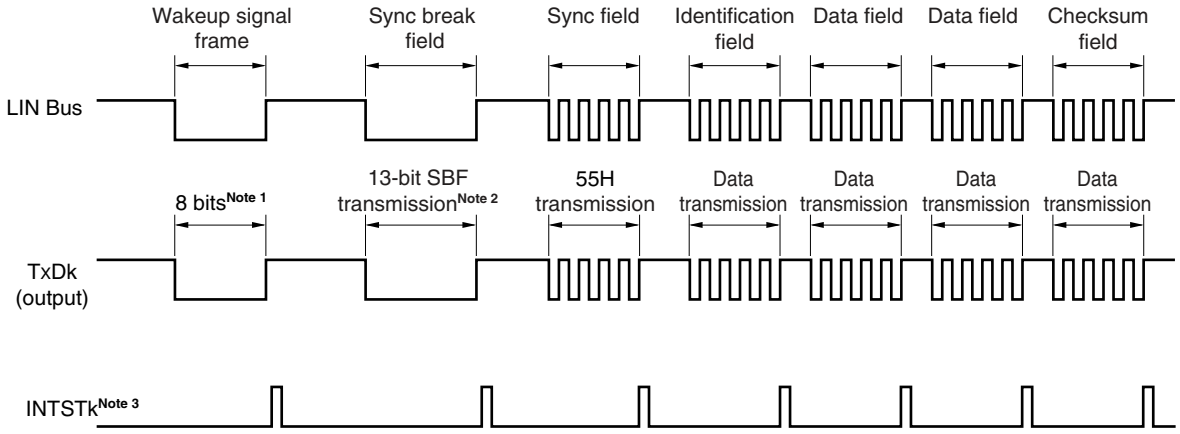
Usually, the master is connected to a network such as CAN (Controller Area Network).

A LIN bus is a single-wire bus to which nodes are connected via transceiver conforming to ISO9141.

According to the protocol of LIN, the master transmits a frame by attaching baud rate information to it. A slave receives this frame and corrects a baud rate error from the master. If the baud rate error of a slave is within ±15%, communication can be established.

Figure 14-92 outlines a transmission operation of LIN.

Figure 14-92. Transmission Operation of LIN



Notes 1. The baud rate is set so as to satisfy the standard of the wakeup signal and data of 00H is transmitted.

2. A sync break field is defined to have a width of 13 bits and output a low level. Where the baud rate for main transfer is N [bps], therefore, the baud rate of the sync break field is calculated as follows.

(Baud rate of sync break field) = 9/13 × N

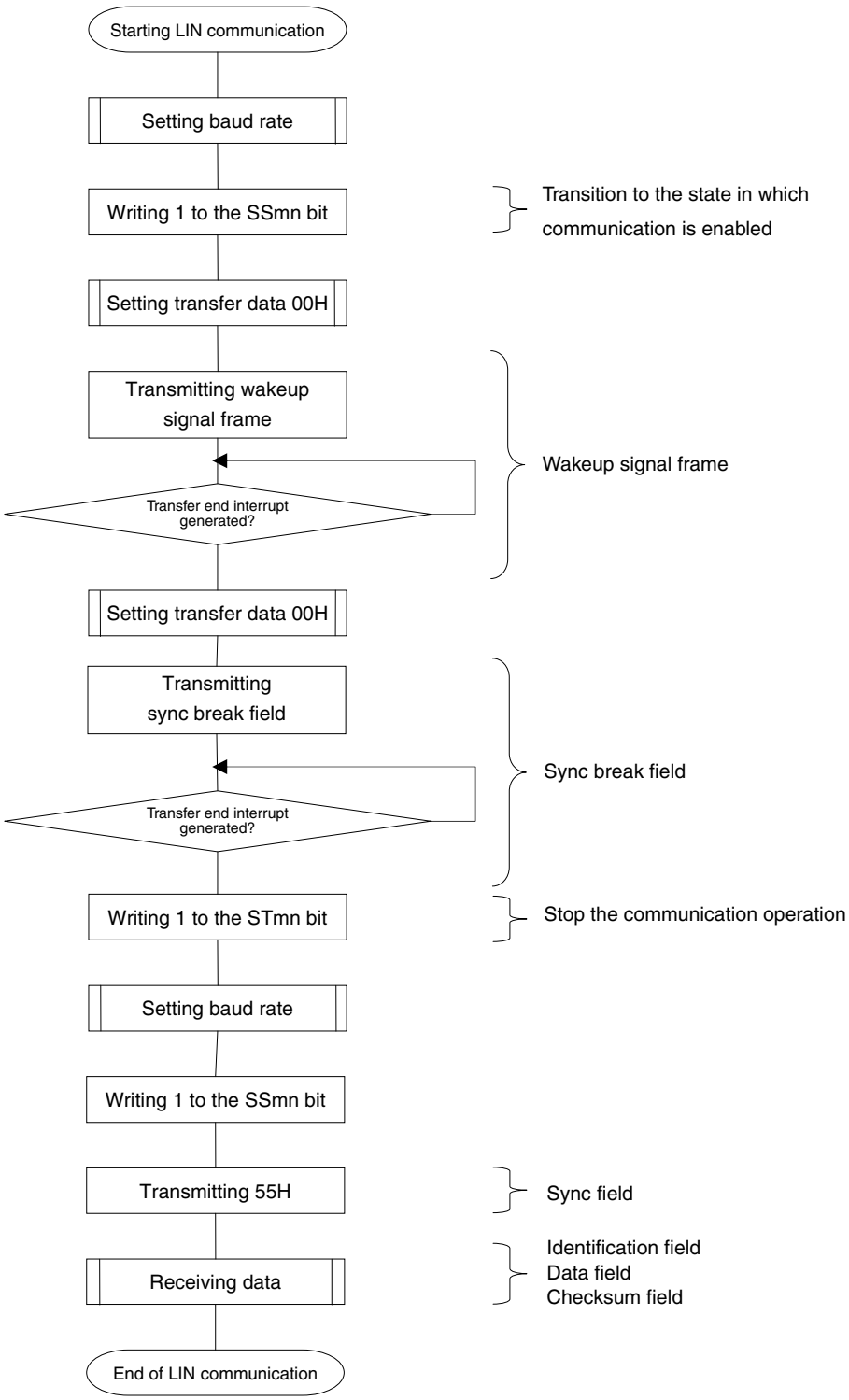
By transmitting data of 00H at this baud rate, a sync break field is generated.

3. INTSTk is output upon completion of transmission. INTSTk is also output when SBF transmission is executed.

Remarks 1. The interval between fields is controlled by software.

2. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: k = 0
78K0R/KF3-L, 78K0R/KG3-L: k = 3

Figure 14-93. Flowchart for LIN Transmission



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00
78K0R/KF3-L, 78K0R/KG3-L: mn = 12

14.7.2 LIN reception

Of UART reception, UART0 of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L and UART3 of the 78K0R/KF3-L, 78K0R/KG3-L support LIN communication.

The following UART channels are used for LIN reception.

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: Channel 1 of SAU0

78K0R/KF3-L, 78K0R/KG3-L: Channel 3 of SAU1

UART	UART0 Note 1	UART1	UART2	UART3 Note 1	UART4 Note 2
Support of LIN communication	Supported	Not supported	Not supported	Supported	Not supported
Target channel	Channel 1 of SAU0	–	–	Channel 3 of SAU1	–
Pins used	RxD0	–	–	RxD3	–
Interrupt	INTSR0	–	–	INTSR3	–
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)				
Error interrupt	INTSRE0	–	–	INTSRE3	
Error detection flag	• Framing error detection flag (FEFmn) • Parity error detection flag (PEFmn) • Overrun error detection flag (OVFmn)				
Transfer data length	8 bits				
Transfer rate	Max. $f_{MCK}/6$ [bps] (SDRmn [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{11} \times 128)$ [bps] Note 3				
Data phase	Forward output (default: high level) Reverse output (default: low level)				
Parity bit	The following selectable • No parity bit (The parity bit is not checked.) • Appending 0 parity (The parity bit is not checked.) • Even-parity check • Odd-parity check				
Stop bit	The following selectable • Appending 1 bit • Appending 2 bits				
Data direction	MSB or LSB first				

Notes 1. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: UART0
78K0R/KF3-L, 78K0R/KG3-L: UART3

2. UART4 is only mounted in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

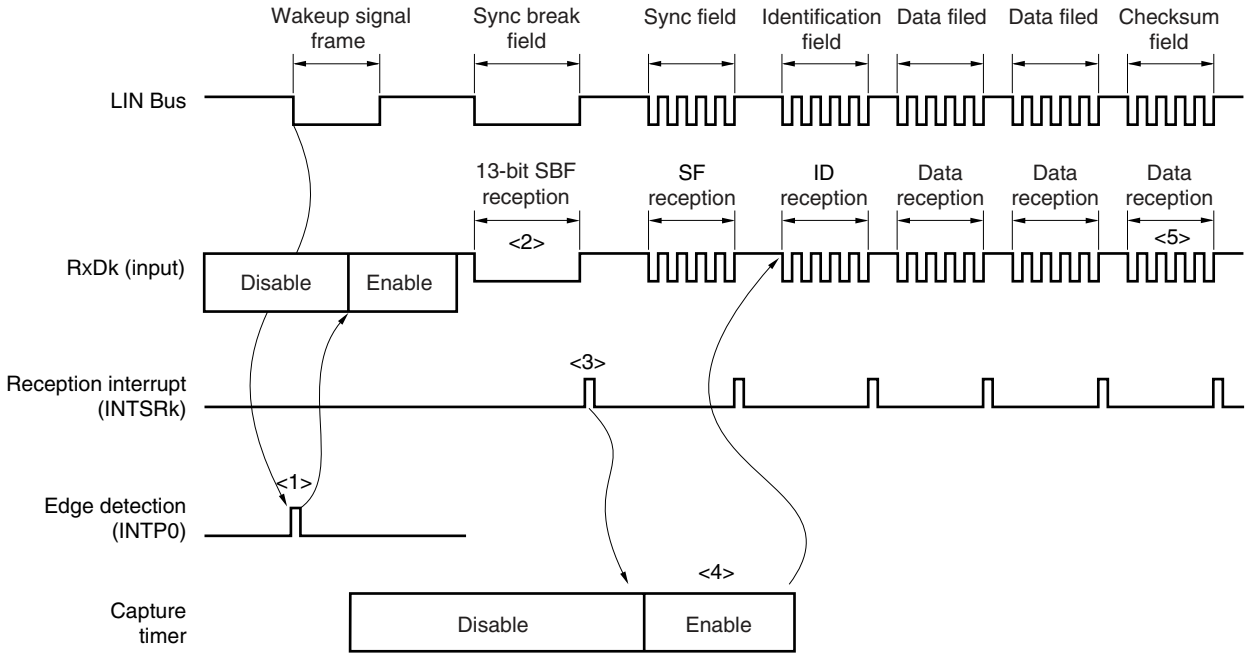
3. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

Remarks 1. f_{MCK}: Operation clock frequency of target channel
f_{CLK}: System clock frequency

2. m: Unit number (m = 0, 1), n: Channel number (n = 1, 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 01
78K0R/KF3-L, 78K0R/KG3-L: mn = 13

Figure 14-94 outlines a reception operation of LIN.

Figure 14-94. Reception Operation of LIN



Here is the flow of signal processing.

<1> The wakeup signal is detected by detecting an interrupt edge (INTP0) on a pin. When the wakeup signal is detected, enable reception of UARTk (RXEmn = 1) and wait for SBF reception.

<2> When the start bit of SBF is detected, reception is started and serial data is sequentially stored in the RXDk register (= bits 7 to 0 of serial data register mn (SDRmn)) at the set baud rate. When the stop bit is detected, the reception end interrupt request (INTSRk) is generated. When data of low levels of 11 bits or more is detected as SBF, it is judged that SBF reception has been correctly completed. If data of low levels of less than 11 bits is detected as SBF, it is judged that an SBF reception error has occurred, and the system returns to the SBF reception wait status.

<3> When SBF reception has been correctly completed, start channel 7 of the timer array unit 0 and measure the bit interval (pulse width) of the sync field (see **8.7.5 Operation as input signal high-/low-level width measurement**).

<4> Calculate a baud rate error from the bit interval of sync field (SF). Stop UARTk once and adjust (re-set) the baud rate.

<5> The checksum field should be distinguished by software. In addition, processing to initialize UARTk after the checksum field is received and to wait for reception of SBF should also be performed by software.

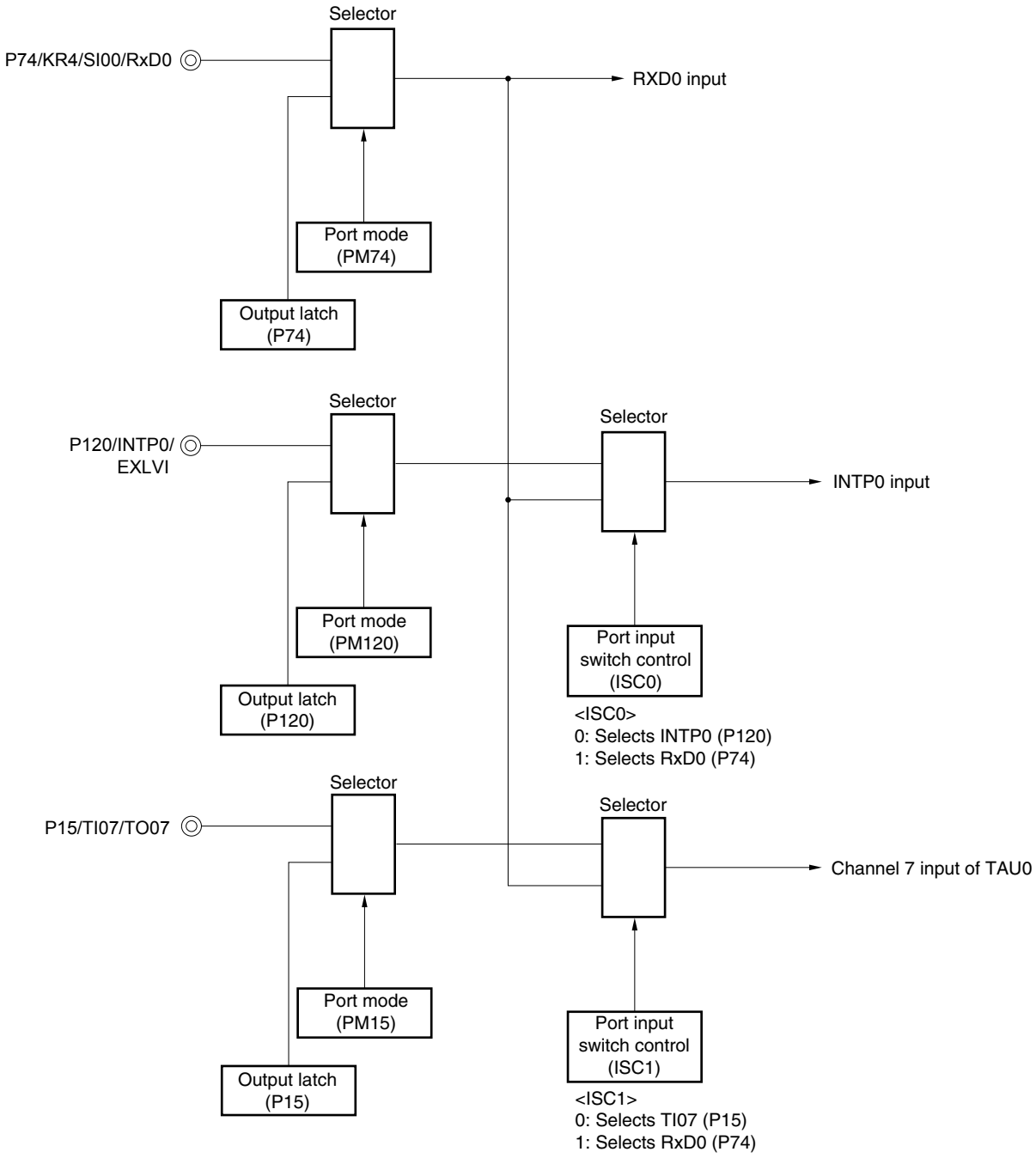
Remark m: Unit number (m = 0, 1), n: Channel number (n = 1, 3),
k: Number of UART used for LIN communication (k = 0, 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 01, k = 0
78K0R/KF3-L, 78K0R/KG3-L: mn = 13, k = 3

Figure 14-95 and figure 14-96 show the configuration of a port that manipulates reception of LIN.

The wakeup signal transmitted from the master of LIN is received by detecting an edge of an external interrupt (INTP0). The length of the sync field transmitted from the master can be measured by using the external event capture operation of the timer array unit 0 to calculate a baud-rate error.

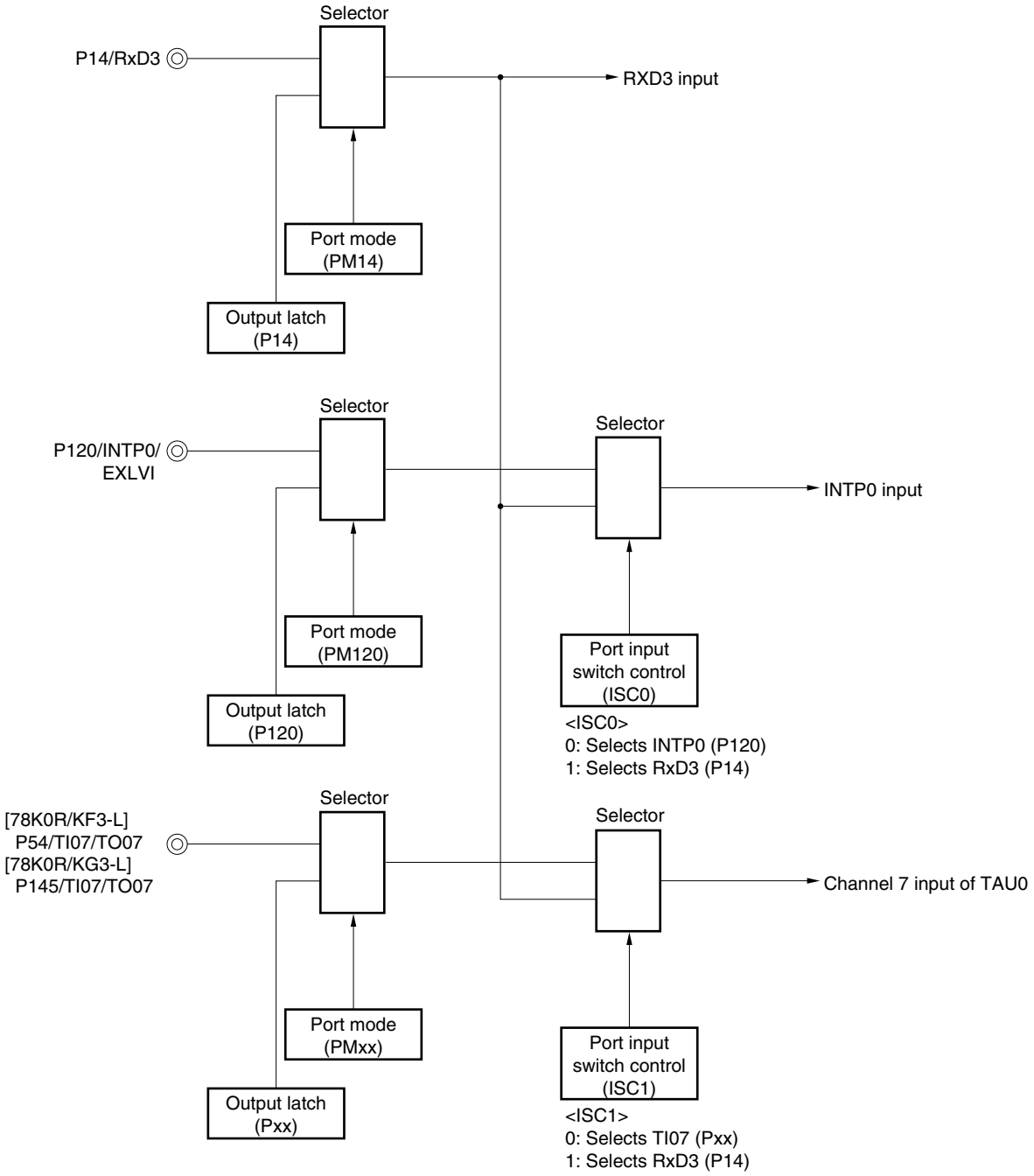
By controlling switch of port input (ISC0/ISC1), the input source of port input (RxDk) for reception can be input to the external interrupt pin (INTP0) and timer array unit 0

Figure 14-95 Port Configuration for Manipulating Reception of LIN (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)



Remark ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (See **Figure 14-17**.)

Figure 14-96 Port Configuration for Manipulating Reception of LIN (78K0R/KF3-L, 78K0R/KG3-L)



Remarks 1. ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (See **Figure 14-18**.)

2. 78K0R/KF3-L: xx = 54 (P54, PM54)
78K0R/KG3-L:xx = 145 (P145, PM145)

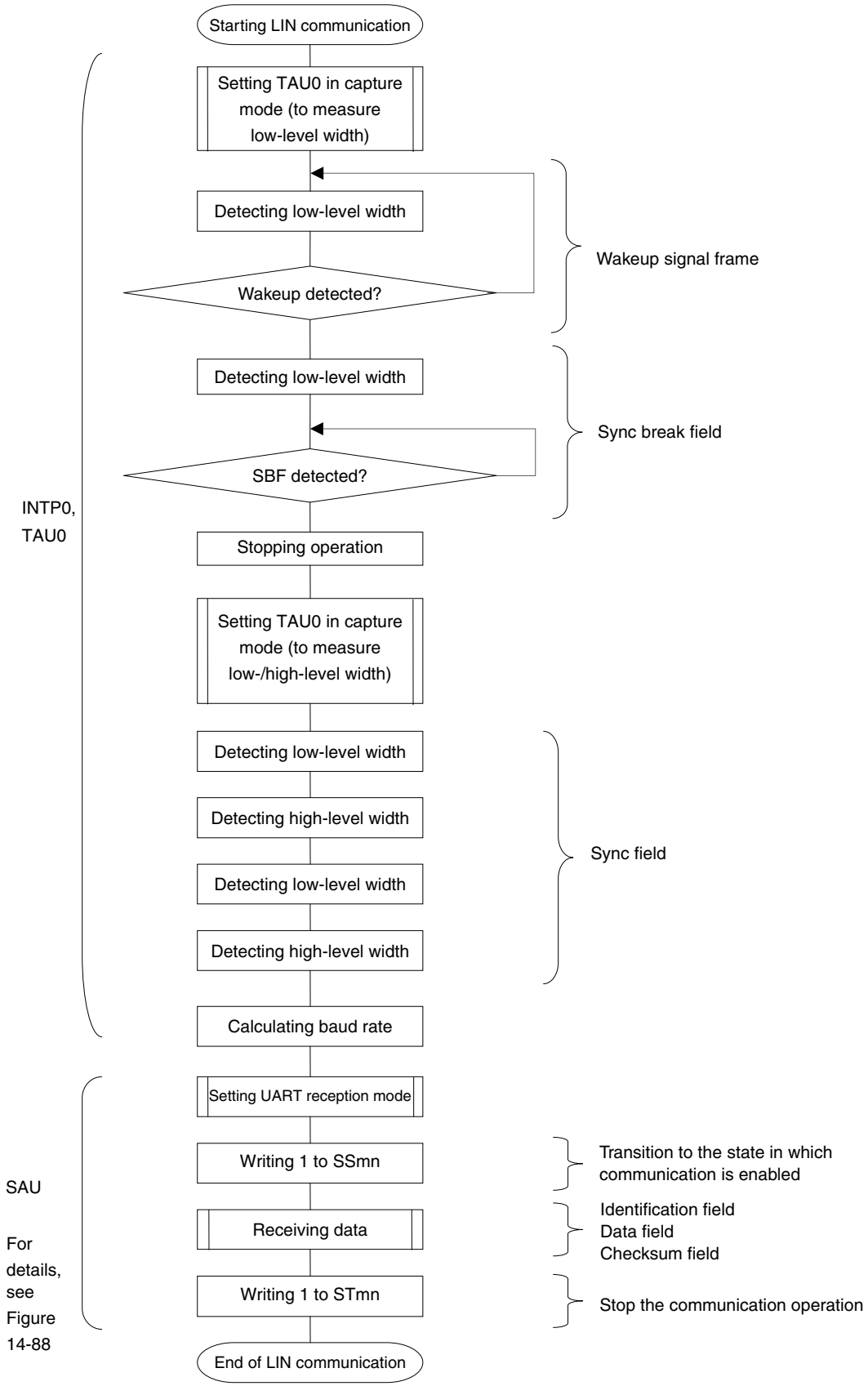
The peripheral functions used for the LIN communication operation are as follows.

<Peripheral functions used>

- External interrupt (INTP0); Wakeup signal detection
  Usage: To detect an edge of the wakeup signal and the start of communication
- Channel 7 of timer array unit 0; Baud rate error detection
  Usage: To detect the length of the sync field (SF) and divide it by the number of bits in order to detect an error (The interval of the edge input to RxDk is measured in the capture mode.)
- Channels 0 and 1 (UART0) or channels 2 and 3 (UART3) of serial array unit (SAU)

Remark 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: k = 0
78K0R/KF3-L, 78K0R/KG3-L: k = 3

Figure 14-97. Flowchart of LIN Reception



14.8 Operation of Simplified I²C (IIC10, IIC20) Communication

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This communication function is designed to execute single communication with devices such as EEPROM, flash memory, and A/D converter, and therefore, can be used only by the master.

Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function[Note] and ACK detection function
- Data length of 8 bits
  (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- Overrun error
- Parity error (ACK error)

* [Functions not supported by simplified I²C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection function

Note When receiving the last data, ACK will not be output if 0 is written to the SOEmn (SOEm register) bit and serial communication data output is stopped. See the processing flow in **14.8.3 (2)** for details.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10

2. To use an I²C bus of full function, see **CHAPTER 15 SERIAL INTERFACE IICA**.

The channel supporting simplified I²C (IIC10, IIC20) is channel 2 of SAU0 and channel 0 of SAU1.

- 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I²C
0	0	CSI00	UART0 (supporting LIN-bus)	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–

- 78K0R/KF3-L, 78K0R/KG3-L

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I²C
0	0	CSI00	UART0	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	CSI20	UART2	IIC20
	1	–		–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–
2 Note	0	CSI40	UART4	–
	1	CSI41		–

Note Serial array unit 2 is only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

Simplified I²C (IIC10, IIC20) performs the following four types of communication operations.

- Address field transmission (See **14.8.1**.)
- Data transmission (See **14.8.2**.)
- Data reception (See **14.8.3**.)
- Stop condition generation (See **14.8.4**.)

14.8.1 Address field transmission

Address field transmission is a transmission operation that first executes in I^2C communication to identify the target for transfer (slave). After a start condition is generated, an address (7 bits) and a transfer direction (1 bit) are transmitted in one frame.

Simplified I^2C	IIC10	IIC20 Note 1
Target channel	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCL10, SDA10 Note 2	SCL20, SDA20 Note 2
Interrupt	INTIIC10	INTIIC20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)	
Error detection flag	Parity error detection flag (PEFmn)	
Transfer data length	8 bits (transmitted with specifying the higher 7 bits as address and the least significant bit as R/W control)	
Transfer rate	Max. f_{MCK}/4 [Hz] (SDRmn[15:9] = 1 or more) f_{MCK}: Operation clock frequency of target channel However, the following condition must be satisfied in each mode of I^2C. • Max. 400 kHz (first mode) • Max. 100 kHz (standard mode)	
Data level	Forward output (default: high level)	
Parity bit	No parity bit	
Stop bit	Appending 1 bit (for ACK reception timing)	
Data direction	MSB first	

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. • 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L
To perform communication via simplified I^2C, set the N-ch open-drain output (V_{DD} tolerance) mode (POM31 = 1) for the port output mode registers (POM3) (see **5.3 Registers Controlling Port Function** for details). When communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance) mode (POM32 = 1) also for the clock input/output pins (SCL10) (see **5.4.4 Connecting to external device with different potential (2.5 V, 3 V)** for details).

• 78K0R/KF3-L, 78K0R/KG3-L
To perform communication via simplified I^2C, set the N-ch open-drain output (V_{DD} tolerance) mode (POM03, POM143 = 1) for the port output mode registers (POM0, POM14) (see **6.3 Registers Controlling Port Function** for details). When communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance) mode (POM04, POM142 = 1) also for the clock input/output pins (SCL10, SCL20) (see **6.4.4 Connecting to external device with different potential (2.5 V, 3 V)** for details).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10

(1) Register setting

Figure 14-98. Example of Contents of Registers for Address Field Transmission of Simplified I²C (IIC10, IIC20)(1/2)

(a) Serial mode register mn (SMRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn	CCSmn	0	0	0	0	0	STSmn	0	SISmn0	1	0	0	MDmn2	MDmn1	MDmn0
	0/1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Operation clock (f_{MCK}) of channel n
0: Prescaler output clock CKm0 set by the SPSm register
1: Prescaler output clock CKm1 set by the SPSm register

Operation mode of channel n
0: Transfer end interrupt

(b) Serial communication operation setting register mn (SCRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn		EOCmn	PTCmn1	PTCmn0	DIRmn		SLCmn1	SLCmn0		DLSmn2	DLSmn1	DLSmn0
	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

Setting of parity bit
00B: No parity

Setting of stop bit
01B: Appending 1 bit (ACK)

(c) Serial data register mn (SDRmn) (lower 8 bits: SIOr)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	Baud rate setting							0	Transmit data setting (address + R/W)							

SIOr

(d) Serial output register m (SOm)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm	0	0	0	0	1	CKOm2	CKOm1	CKOm0	0	0	0	0	1	SOm2	SOm1	SOm0
<R>						0/1 Notes 1, 3	×	0/1 Notes 2, 3						0/1 Notes 1, 3	×	0/1 Notes 2, 3

Start condition is generated by manipulating the SOmn bit.

(e) Serial output enable register m (SOEm)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2	SOEm1	SOEm0
<R>														0/1 Note 1	×	0/1 Note 2

SOEmn = 0 until the start condition is generated, and SOEmn = 1 after generation.

Notes 1. Serial array unit 0 only.

<R> **2.** Serial array unit 1 only.

<R> **3.** The value varies depending on the communication data during communication operation.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10, r = 10, 20

2. ☐: Setting is fixed in the CSI master transmission mode, ▒: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

Figure 14-98. Example of Contents of Registers for Address Field Transmission of Simplified I^2C (IIC10, IIC20)(2/2)

(f) Serial channel start register m (SSm) … Sets only the bits of the target channel is 1.

<R>

SSm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 1	SSm1 ×	SSm0 0/1 Note 2

Notes 1. Serial array unit 0 only.

<R> **2.** Serial array unit 1 only.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10

78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10, r = 10, 20

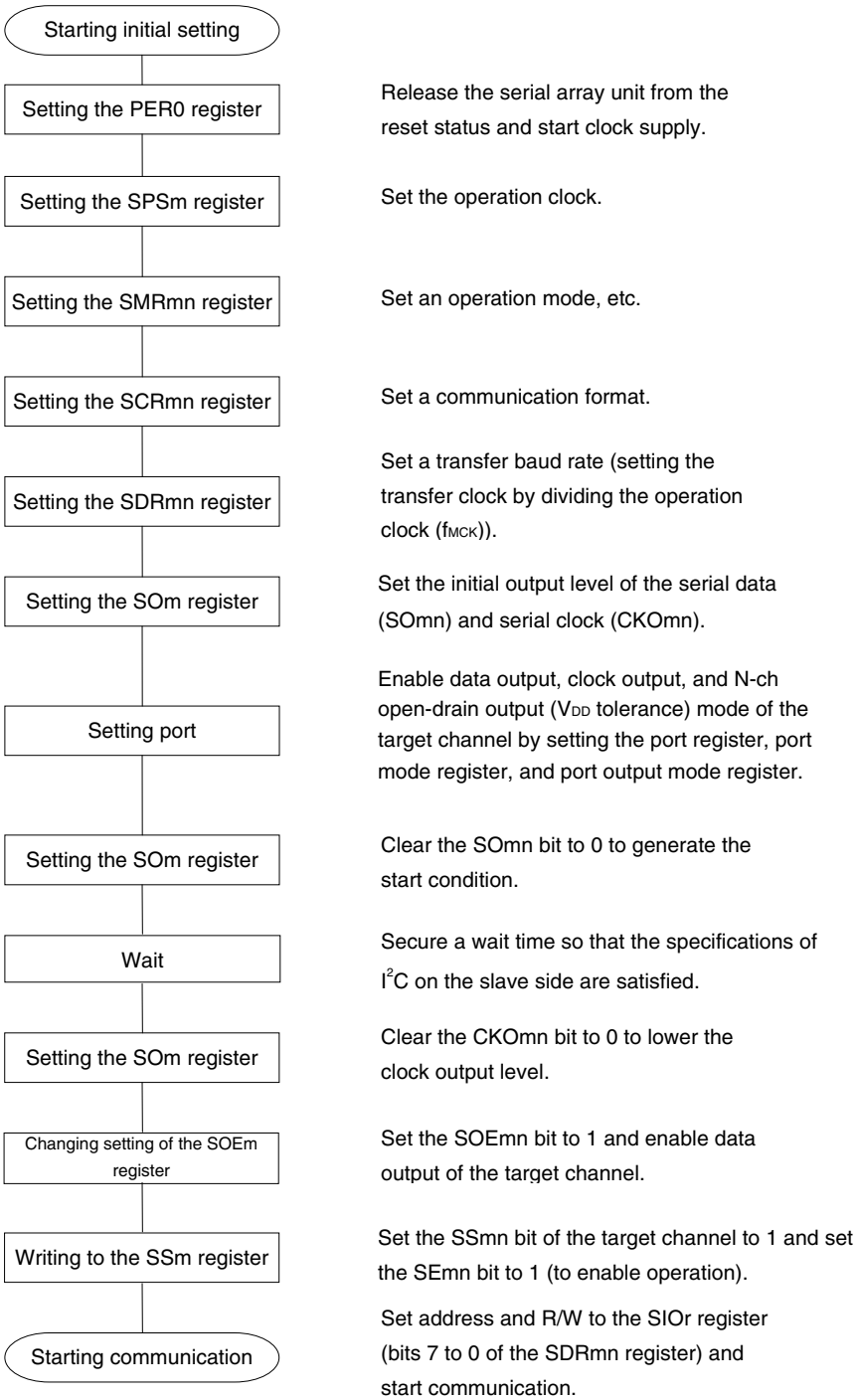
2. ☐ : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

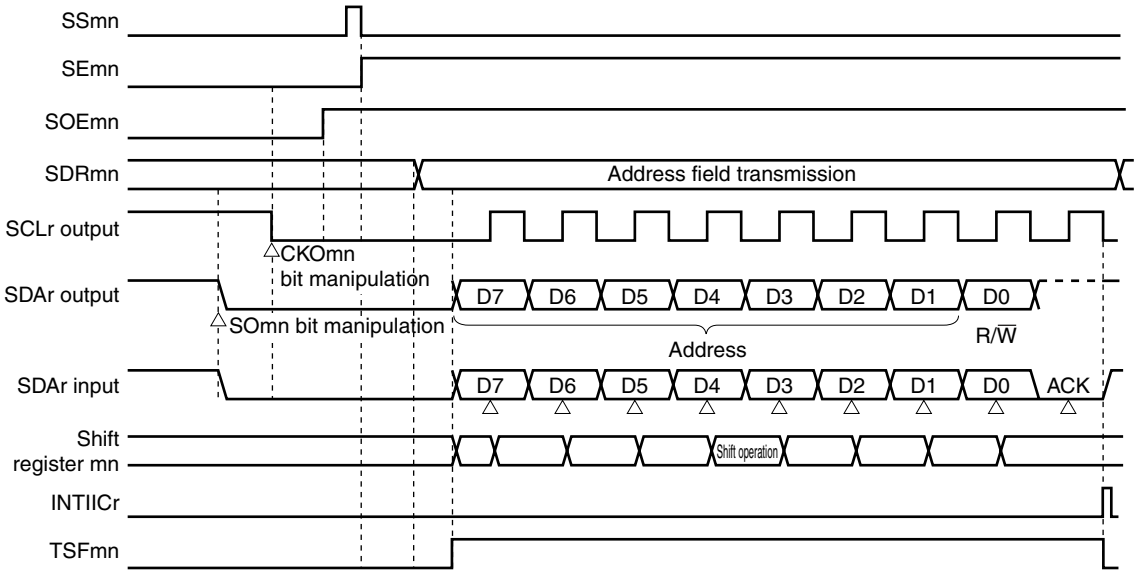
Figure 14-99. Initial Setting Procedure for Address Field Transmission



Caution After setting the SAUmEN bit of peripheral enable register 0 (PER0) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

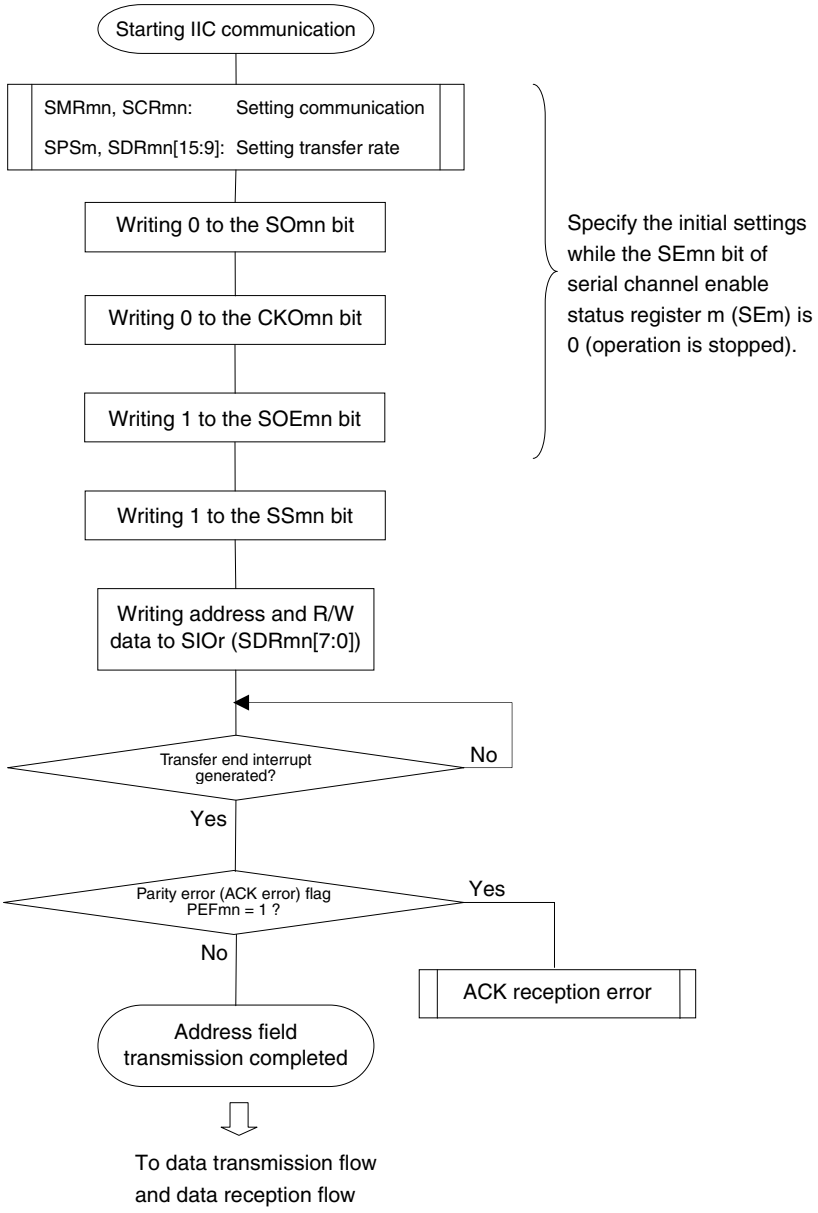
(3) Processing flow

Figure 14-100. Timing Chart of Address Field Transmission



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10,r = 10, 20

Figure 14-101. Flowchart of Address Field Transmission



14.8.2 Data transmission

Data transmission is an operation to transmit data to the target for transfer (slave) after transmission of an address field. After all data are transmitted to the slave, a stop condition is generated and the bus is released.

Simplified I^2C	IIC10	IIC20 Note 1
Target channel	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCL10, SDA10 Note 2	SCL20, SDA20 Note 2
Interrupt	INTIIC10	INTIIC20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)	
Error detection flag	Parity error detection flag (PEFmn)	
Transfer data length	8 bits	
Transfer rate	Max. f_{MCK}/4 [Hz] (SDRmn[15:9] = 1 or more) f_{MCK}: Operation clock frequency of target channel However, the following condition must be satisfied in each mode of I^2C. • Max. 400 kHz (first mode) • Max. 100 kHz (standard mode)	
Data level	Forward output (default: high level)	
Parity bit	No parity bit	
Stop bit	Appending 1 bit (for ACK reception timing)	
Data direction	MSB first	

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. • 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L

To perform communication via simplified I^2C, set the N-ch open-drain output (V_{DD} tolerance) mode (POM31 = 1) for the port output mode registers (POM3) (see **5.3 Registers Controlling Port Function** for details). When communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance) mode (POM32 = 1) also for the clock input/output pins (SCL10) (see **5.4.4 Connecting to external device with different potential (2.5 V, 3 V)** for details).

• 78K0R/KF3-L, 78K0R/KG3-L

To perform communication via simplified I^2C, set the N-ch open-drain output (V_{DD} tolerance) mode (POM03, POM143 = 1) for the port output mode registers (POM0, POM14) (see **6.3 Registers Controlling Port Function** for details). When communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance) mode (POM04, POM142 = 1) also for the clock input/output pins (SCL10, SCL20) (see **6.4.4 Connecting to external device with different potential (2.5 V, 3 V)** for details).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10

(1) Register setting

Figure 14-102. Example of Contents of Registers for Data Transmission of Simplified I²C (IIC10, IIC20)(1/2)

(a) Serial mode register mn (SMRmn) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn	CCSmn						STSmn		SISmn0				MDmn2	MDmn1	MDmn0
	0/1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

(b) Serial communication operation setting register mn (SCRmn) … Do not manipulate the bits of this register, except the TXEmn and RXEmn bits, during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn		EOCmn	PTCmn1	PTCmn0	DIRmn		SLCmn1	SLCmn0		DLSmn2	DLSmn1	DLSmn0
	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

(c) Serial data register mn (SDRmn) (lower 8 bits: SIOr)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	Baud rate setting							0	Transmit data setting							

SIOr

(d) Serial output register m (SOm) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm						CKOm2	CKOm1	CKOm0						SOm2	SOm1	SOm0
<R>	0	0	0	0	1	0/1 Notes 1, 3	×	0/1 Notes 2, 3	0	0	0	0	1	0/1 Notes 1, 3	×	0/1 Notes 2, 3

(e) Serial output enable register m (SOEm) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm														SOEm2	SOEm1	SOEm0
<R>	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1 Note 1	×	0/1 Note 2

Notes 1. Serial array unit 0 only.

<R> **2.** Serial array unit 1 only.

3. The value varies depending on the communication data during communication operation.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10, r = 10, 20

2. □: Setting is fixed in the CSI master transmission mode, ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

Figure 14-102. Example of Contents of Registers for Data Transmission of Simplified I^2C (IIC10, IIC20)(2/2)

(f) Serial channel start register m (SSm) … Do not manipulate this register during data transmission/reception.

<R>

SSm	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 1	SSm1 ×	SSm0 0/1 Note 2

Notes 1. Serial array unit 0 only.

2. The value varies depending on the communication data during communication operation.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10, r = 10, 20

2. ☐ : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Processing flow

Figure 14-103. Timing Chart of Data Transmission

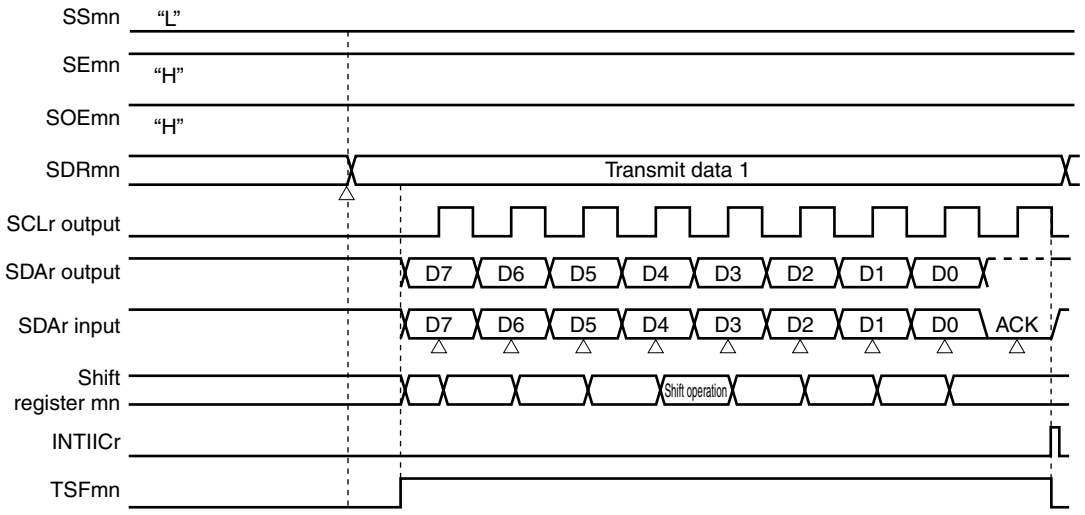
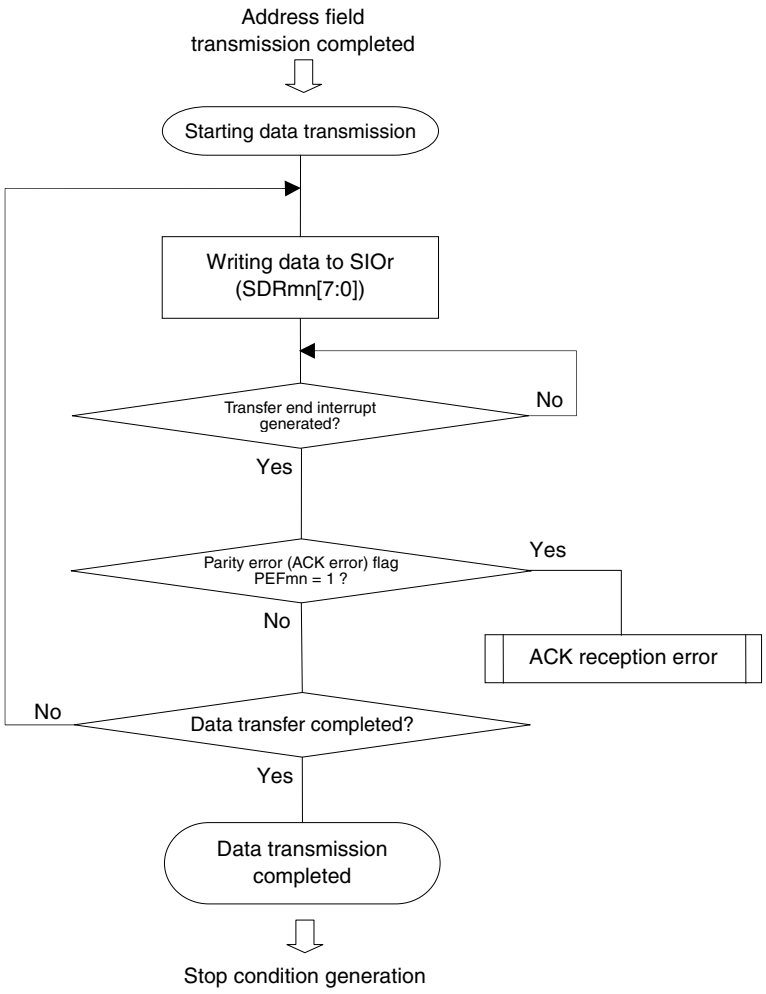


Figure 14-104. Flowchart of Data Transmission



14.8.3 Data reception

Data reception is an operation to receive data to the target for transfer (slave) after transmission of an address field. After all data are received to the slave, a stop condition is generated and the bus is released.

Simplified I^2C	IIC10	IIC20 Note 1
Target channel	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCL10, SDA10 Note 2	SCL20, SDA20 Note 2
Interrupt	INTIIC10	INTIIC20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)	
Error detection flag	Overrun error detection flag (OVFmn) only	
Transfer data length	8 bits	
Transfer rate	Max. f_{MCK}/4 [Hz] (SDRmn[15:9] = 1 or more) f_{MCK}: Operation clock frequency of target channel However, the following condition must be satisfied in each mode of I^2C. • Max. 400 kHz (first mode) • Max. 100 kHz (standard mode)	
Data level	Forward output (default: high level)	
Parity bit	No parity bit	
Stop bit	Appending 1 bit (ACK transmission)	
Data direction	MSB first	

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. • 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L

To perform communication via simplified I^2C, set the N-ch open-drain output (V_{DD} tolerance) mode (POM31 = 1) for the port output mode registers (POM3) (see **5.3 Registers Controlling Port Function** for details). When communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance) mode (POM32 = 1) also for the clock input/output pins (SCL10) (see **5.4.4 Connecting to external device with different potential (2.5 V, 3 V)** for details).

• 78K0R/KF3-L, 78K0R/KG3-L

To perform communication via simplified I^2C, set the N-ch open-drain output (V_{DD} tolerance) mode (POM03, POM143 = 1) for the port output mode registers (POM0, POM14) (see **6.3 Registers Controlling Port Function** for details). When communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance) mode (POM04, POM142 = 1) also for the clock input/output pins (SCL10, SCL20) (see **6.4.4 Connecting to external device with different potential (2.5 V, 3 V)** for details).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10

(1) Register setting

Figure 14-105. Example of Contents of Registers for Data Reception of Simplified I²C (IIC10, IIC20) (1/2)

(a) Serial mode register mn (SMRmn) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn	CCSmn						STSmn		SISmn0				MDmn2	MDmn1	MDmn0
	0/1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

(b) Serial communication operation setting register mn (SCRmn) … Do not manipulate the bits of this register, except the TXEmn and RXEmn bits, during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn		EOCmn	PTCmn1	PTCmn0	DIRmn		SLCmn1	SLCmn0		DLSmn2	DLSmn1	DLSmn0
	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1

(c) Serial data register mn (SDRmn) (lower 8 bits: SIOr)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	Baud rate setting							0	Dummy transmit data setting (FFH)							

SIOr

(d) Serial output register m (SOm) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<R> SOm	0	0	0	0	1	CKOm2	CKOm1	CKOm0	0	0	0	0	1	SOm2	SOm1	SOm0
						0/1 Notes 1, 2	×	0/1 Notes 2, 3						0/1 Notes 1, 2	×	0/1 Notes 2, 3

(e) Serial output enable register m (SOEm) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<R> SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2	SOEm1	SOEm0
														0/1 Note 1	×	0/1 Note 2

Notes 1. Serial array unit 0 only.

<R> **2.** Serial array unit 1 only.

3. The value varies depending on the communication data during communication operation.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10, r = 10, 20

2. □: Setting is fixed in the CSI master transmission mode, ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

Figure 14-105. Example of Contents of Registers for Data Reception of Simplified I²C (IIC10, IIC20) (2/2)

(f) Serial channel start register m (SSm) … Do not manipulate this register during data transmission/reception.

<R>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 1	SSm1 ×	SSm0 0/1 Note 2

Notes 1. Serial array unit 0 only.

<R> **2.** Serial array unit 1 only.

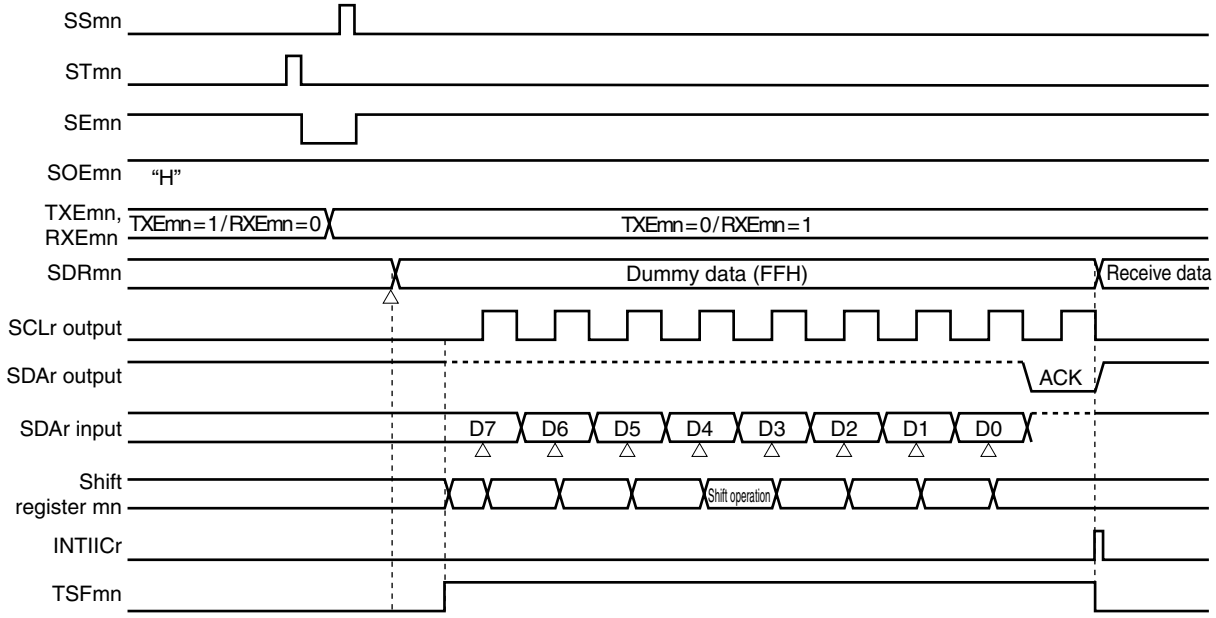
Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10, r = 10, 20

2. ☐ : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

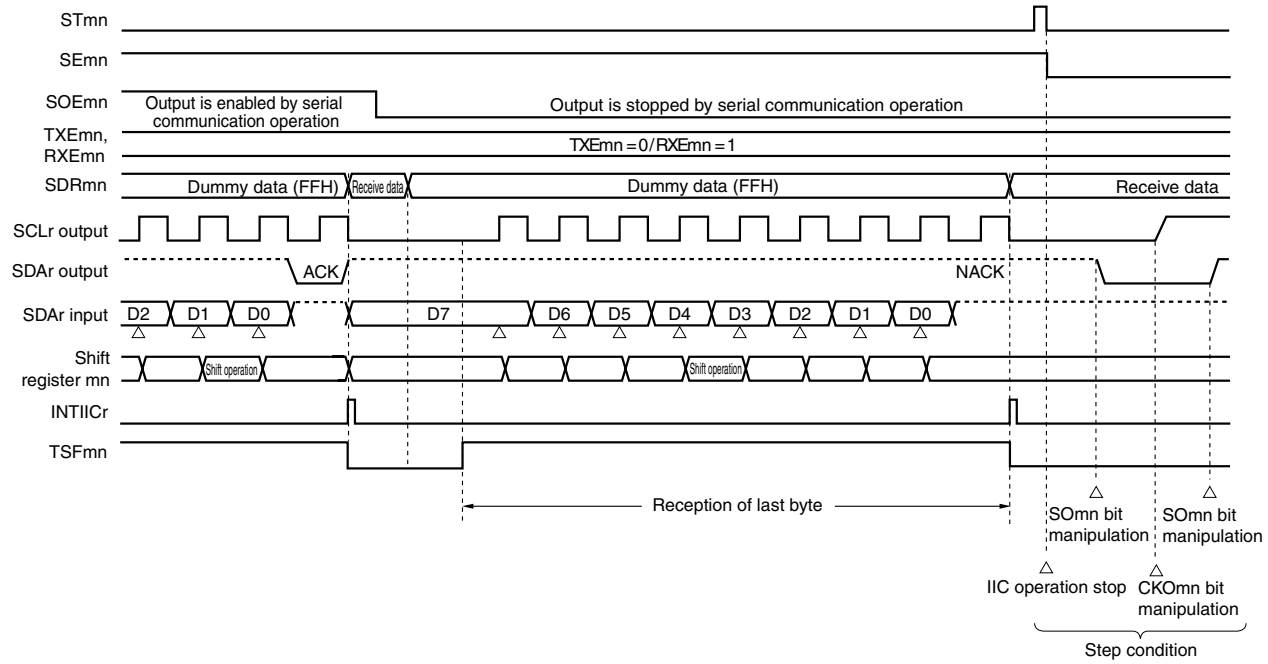
(2) Processing flow

Figure 14-106. Timing Chart of Data Reception

(a) When starting data reception

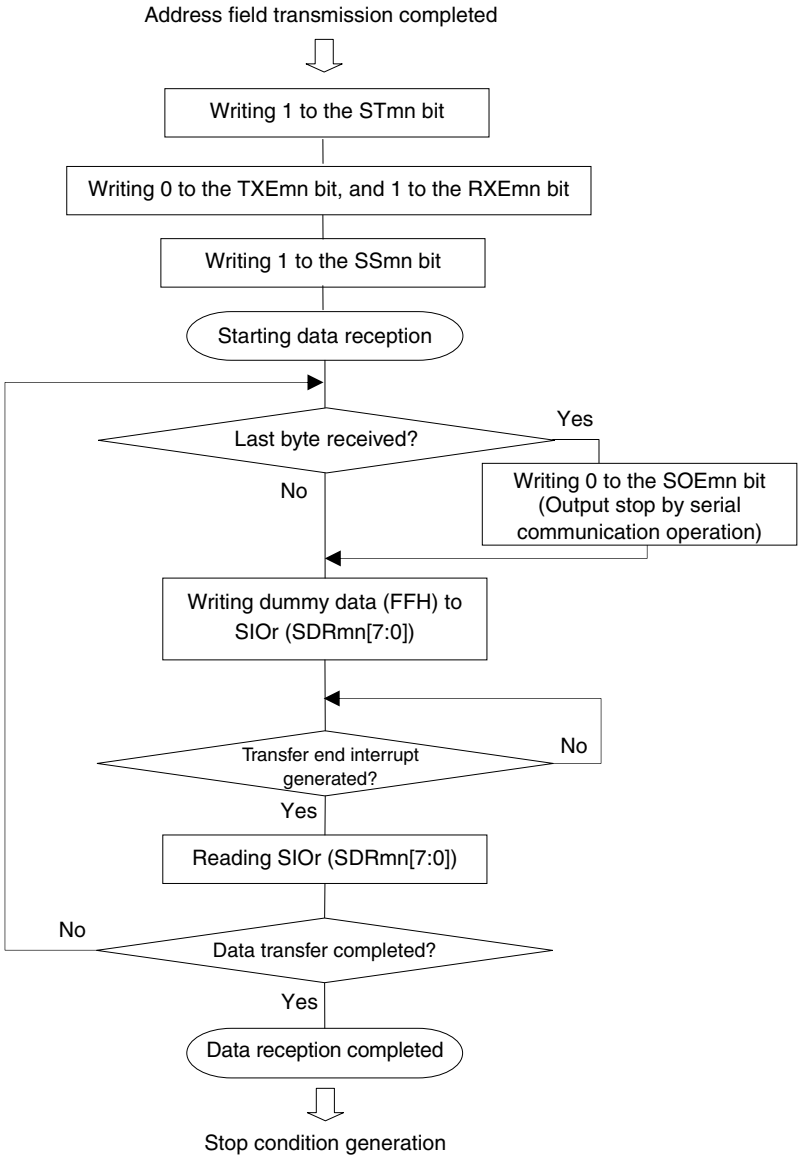


(b) When receiving last data



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2) , r: IIC number (r = 10, 20)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10, r = 10, 20

Figure 14-107. Flowchart of Data Reception



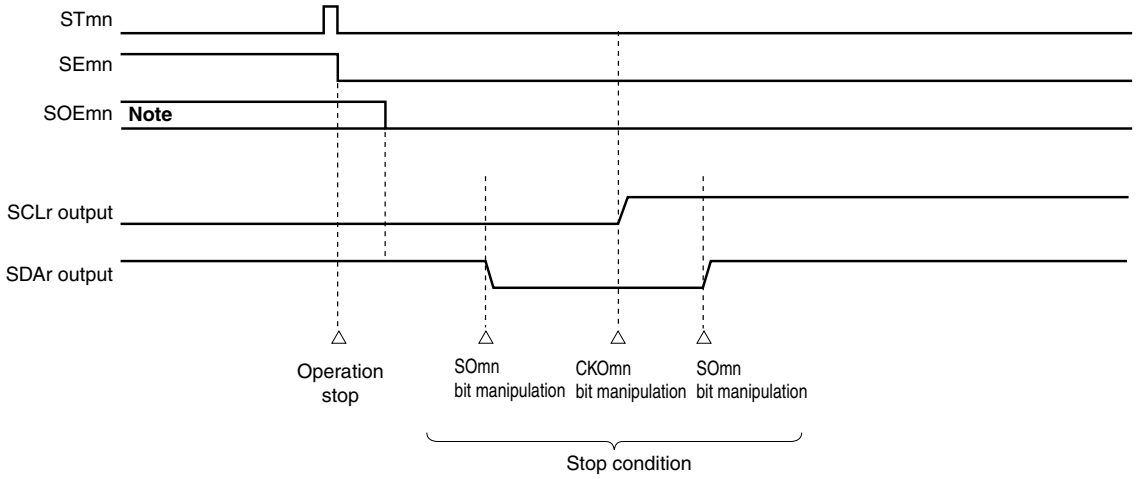
Caution ACK is not output when the last data is received (NACK). Communication is then completed by setting "1" to the STmn bit of serial channel stop register m (STm) to stop operation and generating a stop condition.

14.8.4 Stop condition generation

After all data are transmitted to or received from the target slave, a stop condition is generated and the bus is released.

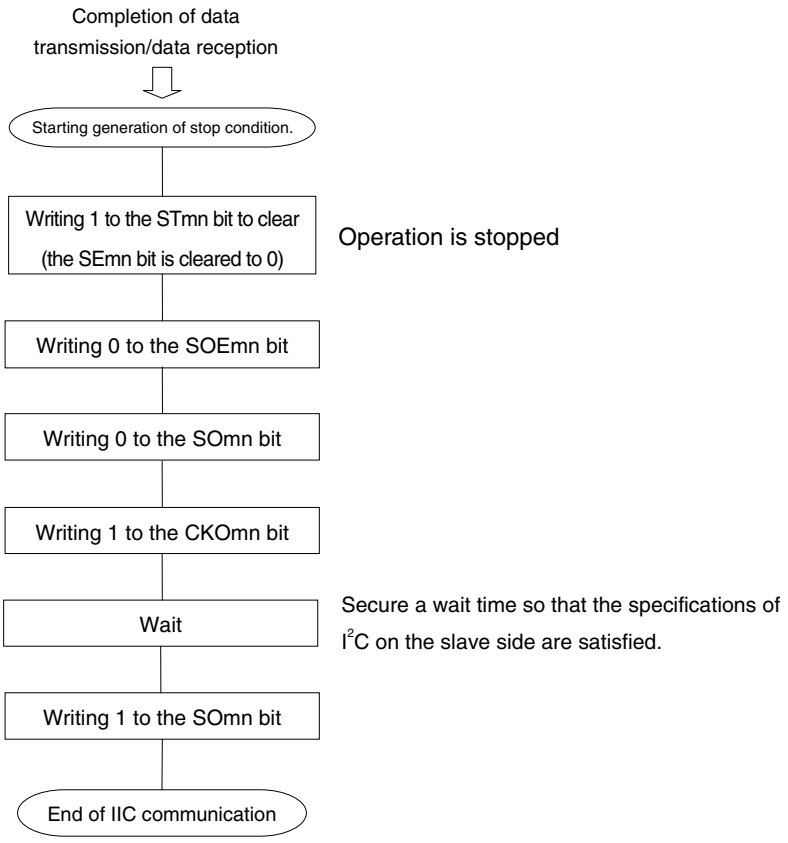
(1) Processing flow

Figure 14-108. Timing Chart of Stop Condition Generation



Note During a receive operation, the SOEmn bit of serial output enable register m (SOEm) is cleared to 0 before receiving the last data.

Figure 14-109. Flowchart of Stop Condition Generation



14.8.5 Calculating transfer rate

The transfer rate for simplified I^2C (IIC10, IIC20) communication can be calculated by the following expressions.

(Transfer rate) = {Operation clock (f_{MCK}) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2

Caution Setting SDRmn[15:9] = 0000000B is prohibited. Setting SDRmn[15:9] = 0000001B or more.

Remarks 1. The value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000001B to 1111111B) and therefore is 1 to 127.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02

78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 14-4. Selection of Operation Clock For Simplified I^2C

SMRmn Register	SPSm Register								Operation Clock (f_{MCK}) Note 1	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		f_{CLK} = 20 MHz
0	X	X	X	X	0	0	0	0	f_{CLK}	20 MHz
	X	X	X	X	0	0	0	1	$f_{CLK}/2$	10 MHz
	X	X	X	X	0	0	1	0	$f_{CLK}/2^2$	5 MHz
	X	X	X	X	0	0	1	1	$f_{CLK}/2^3$	2.5 MHz
	X	X	X	X	0	1	0	0	$f_{CLK}/2^4$	1.25 MHz
	X	X	X	X	0	1	0	1	$f_{CLK}/2^5$	625 kHz
	X	X	X	X	0	1	1	0	$f_{CLK}/2^6$	313 kHz
	X	X	X	X	0	1	1	1	$f_{CLK}/2^7$	156 kHz
	X	X	X	X	1	0	0	0	$f_{CLK}/2^8$	78.1 kHz
	X	X	X	X	1	0	0	1	$f_{CLK}/2^9$	39.1 kHz
	X	X	X	X	1	0	1	0	$f_{CLK}/2^{10}$	19.5 kHz
	X	X	X	X	1	0	1	1	$f_{CLK}/2^{11}$	9.77 kHz
	X	X	X	X	1	1	1	1	INTTM02 if m = 0 Note 2, setting prohibited if m = 1	
1	0	0	0	0	X	X	X	X	f_{CLK}	20 MHz
	0	0	0	1	X	X	X	X	$f_{CLK}/2$	10 MHz
	0	0	1	0	X	X	X	X	$f_{CLK}/2^2$	5 MHz
	0	0	1	1	X	X	X	X	$f_{CLK}/2^3$	2.5 MHz
	0	1	0	0	X	X	X	X	$f_{CLK}/2^4$	1.25 MHz
	0	1	0	1	X	X	X	X	$f_{CLK}/2^5$	625 kHz
	0	1	1	0	X	X	X	X	$f_{CLK}/2^6$	313 kHz
	0	1	1	1	X	X	X	X	$f_{CLK}/2^7$	156 kHz
	1	0	0	0	X	X	X	X	$f_{CLK}/2^8$	78.1 kHz
	1	0	0	1	X	X	X	X	$f_{CLK}/2^9$	39.1 kHz
	1	0	1	0	X	X	X	X	$f_{CLK}/2^{10}$	19.5 kHz
	1	0	1	1	X	X	X	X	$f_{CLK}/2^{11}$	9.77 kHz
	1	1	1	1	X	X	X	X	INTTM02 if m = 0 Note 2, setting prohibited if m = 1	
Other than above									Setting prohibited	

Notes 1. When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU). When selecting INTTM02 for the operation clock, also stop the timer array unit 0 (timer channel stop register 0 (TT0) = 00FFH).

2. SAU0 can be operated at a fixed division ratio of the subsystem clock, regardless of the f_{CLK} frequency (main system clock, sub system clock), by operating the interval timer for which $f_{SUB}/4$ Note 3 has been selected as the count clock (setting TIS02 bit of timer input select register 0 (TIS0) to 1) and selecting INTTM02 by using the SPS0 register in channel 2 of TAU0. When changing f_{CLK}, however, SAU0 and TAU0 must be stopped as described in Note 1 above.

3. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Remarks 1. X: Don't care

2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02

78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10

Here is an example of setting an IIC transfer rate where $f_{MCK} = f_{CLK} = 20$ MHz.

IIC Transfer Mode (Desired Transfer Rate)	f_{CLK} = 20 MHz			
	Operation Clock (f_{MCK})	SDRmn[15:9]	Calculated Transfer Rate	Error from Desired Transfer Rate
100 kHz	f_{CLK}	99	100 kHz	0.0%
400 kHz	f_{CLK}	24	400 kHz	0.0%

14.8.6 Procedure for processing errors that occurred during simplified I²C (IIC10, IIC20) communication

The procedure for processing errors that occurred during simplified I²C (IIC10, IIC20) communication is described in Figure 14-110 and 14-111.

Figure 14-110. Processing Procedure in Case of Overrun Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

Figure 14-111. Processing Procedure in Case of Parity Error (ACK error) in Simplified I²C Mode

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.
Sets the STmn bit of serial channel stop register m (STm) to 1. →	The SEmn bit of serial channel enable status register m (SEm) is set to 0 and channel n stops operation.	Slave is not ready for reception because ACK is not returned. Therefore, a stop condition is created, the bus is released, and communication is started again from the start condition. Or, a restart condition is generated and transmission can be redone from address transmission.
Creates stop condition.		
Creates start condition.		
Sets the SSmn bit of serial channel start register m (SSm) to 1. →	The SEmn bit of serial channel enable status register m (SEm) is set to 1 and channel n is enabled to operate.	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10, r = 10, 20

14.9 Relationship Between Register Settings and Pins

Tables 14-5 to 14-16 show the relationship between register settings and pins for each channel of the serial array unit. See Tables 14-5 to 14-8 if using the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L, and see Tables 14-9 to 14-16 if using the 78K0R/KF3-L and 78K0R/KG3-L.

14.9.1 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L

Table 14-5. Relationship Between Register Settings and Pins (Channel 0: CSI00, UART0 Transmission)

SE 00 Note 1	MD 0mn	MD0 01	SOE 00	SO0 0	CKO 00	TXE 00	RXE 00	PM 75	P75	PM 74 Note 2	P74 Note 2	PM 73	P73	Operation mode	Pin Function		
															$\overline{\text{SCK00}}$/ KR5/P75	SI00/ RxD0/KR4/ P74 Note 2	SO00/ TxD0/KR3/ P73
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	KR5/P75	KR4/P74	KR3/P73
	0	1														KR4/P74/ RxD0	
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	Slave CSI00 reception	$\overline{\text{SCK00}}$ (input)	SI00	KR3/P73
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	Slave CSI00 transmission	$\overline{\text{SCK00}}$ (input)	KR4/P74	SO00
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	Slave CSI00 transmission /reception	$\overline{\text{SCK00}}$ (input)	SI00	SO00
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	Master CSI00 reception	$\overline{\text{SCK00}}$ (output)	SI00	KR3/P73
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	Master CSI00 transmission	$\overline{\text{SCK00}}$ (output)	KR4/P74	SO00
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	Master CSI00 transmission /reception	$\overline{\text{SCK00}}$ (output)	SI00	SO00
	0	1	1	0/1 Note 4	1	1	0	× Note 3	× Note 3	× Note 3	× Note 3	0	1	UART0 transmission Note 5	KR5/P75	KR4/P74/ RxD0	TxD0

Notes 1. Serial channel enable register 0 (SE0) is a read-only status register which is set using serial channel start register 0 (SS0) and serial channel stop register 0 (ST0).

2. When channel 1 is set to UART0 reception, this pin becomes an RxD0 function pin (refer to **Table 14-6**). In this case, operation stop mode or UART0 transmission must be selected for channel 0.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART0 transmission and reception in a pair, set channel 1 to UART0 reception (refer to **Table 14-6**).

Remark X: Don't care

Table 14-6. Relationship Between Register Settings and Pins (Channel 1: CSI01, UART0 Reception)

SE01 Note 1	MD012	MD011	SOE01	SO01	CKO01	TXE01	RXE01	PM72	P72	PM71	P71	PM70	P70	PM74 Note 2	P74 Note 2	Operation mode	Pin Function			
																	$\overline{SCK01}$/KR2/INTP6/P72	SI01/KR1/INTP5/P71	SO01/KR0/INTP4/P70	SI00/RxD0/KR4/P74 Note 2
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	KR2/INTP6/P72	KR1/INTP5/P71	KR0/INTP4/P70	KR4/P74
	0	1																		
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	× Note 3	× Note 3	Slave CSI01 reception	$\overline{SCK01}$ (input)	SI01	KR0/INTP4/P70	SI00/KR4/P74
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	× Note 3	× Note 3	Slave CSI01 transmission	$\overline{SCK01}$ (input)	KR1/INTP5/P71	SO01	SI00/KR4/P74
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	× Note 3	× Note 3	Slave CSI01 transmission /reception	$\overline{SCK01}$ (input)	SI01	SO01	SI00/KR4/P74
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	× Note 3	× Note 3	Master CSI01 reception	$\overline{SCK01}$ (output)	SI01	KR0/INTP4/P70	SI00/KR4/P74
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	× Note 3	× Note 3	Master CSI01 transmission	$\overline{SCK01}$ (output)	KR1/INTP5/P71	SO01	SI00/KR4/P74
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	× Note 3	× Note 3	Master CSI01 transmission /reception	$\overline{SCK01}$ (output)	SI01	SO01	SI00/KR4/P74
	0	1	0	1	1	0	1	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	1	×	UART0 reception Notes 5, 6	KR2/INTP6/P72	KR1/INTP5/P71	KR0/INTP4/P70	RxD0

Notes 1. Serial channel enable status register 0 (SE0) is a read-only status register which is set using serial channel statrt register 0 (SS0) and serial channel stop register 0 (ST0).

2. When channel 1 is set to UART0 reception, this pin becomes an RxD0 function pin. In this case, set channel 0 to operation stop mode or UART0 transmission (refer to **Table 14-5**).
When channel 0 is set to CSI00, this pin cannot be used as an RxD0 function pin. In this case, set channel 1 to operation stop mode or CSI01.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART0 transmission and reception in a pair, set channel 0 to UART0 transmission (refer to **Table 14-5**).

6. Serial mode register 00 (SMR00) of channel 0 must also be set during UART0 reception. For details, refer to **14.6.2 (1) Register setting**.

Remark X: Don't care

Table 14-7. Relationship Between Register Settings and Pins (Channel 2: CSI10, UART1 Transmission, IIC10)

SE02 Note 1	MD022	MD021	SOE02	SO02	CKO02	TXE02	RXE02	PM32	P32	PM31 Note 2	P31 Note 2	PM30	P30	Operation mode	Pin Function		
															$\overline{SCK10}$/SCL10/INTP2/P32	SI10/SDA10/RxD1/INTP1/P31 Note 2	SO10/TxD1/P30
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	INTP2/P32	INTP1/P31	P30
	0	1														RxD1/INTP1/P31	
	1	0														INTP1/P31	
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	Slave CSI10 reception	$\overline{SCK10}$ (input)	SI10	P30
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	Slave CSI10 transmission	$\overline{SCK10}$ (input)	INTP1/P31	SO10
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	Slave CSI10 transmission /reception	$\overline{SCK10}$ (input)	SI10	SO10
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	Master CSI10 reception	$\overline{SCK10}$ (output)	SI10	P30
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	Master CSI10 transmission	$\overline{SCK10}$ (output)	INTP1/P31	SO10
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	Master CSI10 transmission /reception	$\overline{SCK10}$ (output)	SI10	SO10
	0	1	1	0/1 Note 4	1	1	0	× Note 3	× Note 3	× Note 3	× Note 3	0	1	UART1 transmission Note 5	INTP2/P32	RxD1/INTP1/P31	TxD1
0	1	0	0	0/1 Note 6	0/1 Note 6	0	0	0	1	0	1	× Note 3	× Note 3	IIC10 start condition	SCL10	SDA10	P30
						1	0										
						0	1										
1			1	0/1 Note 4	0/1 Note 4	1	0	0	1	0	1	× Note 3	× Note 3	IIC10 address field transmission	SCL10	SDA10	P30
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	0	1	× Note 3	× Note 3	IIC10 data transmission	SCL10	SDA10	P30
			1	0/1 Note 4	0/1 Note 4	0	1	0	1	0	1	× Note 3	× Note 3	IIC10 data reception	SCL10	SDA10	P30
0			0	0/1 Note 7	0/1 Note 7	0	0	0	1	0	1	× Note 3	× Note 3	IIC10 stop condition	SCL10	SDA10	P30
						1	0										
						0	1										

Notes 1. Serial channel enable status register 0 (SE0) is a read-only status register which is set using serial channel start register 0 (SS0) and serial channel stop register 0 (ST0).

2. When channel 3 is set to UART1 reception, this pin becomes an RxD1 function pin (refer to **Table 14-8**). In this case, operation stop mode or UART1 transmission must be selected for channel 2.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART1 transmission and reception in a pair, set channel 3 to UART1 reception (refer to **Table 14-8**).

6. Set the CKO02 bit to 1 before a start condition is generated. Clear the SO02 bit from 1 to 0 when the start condition is generated.

7. Set the CKO02 bit to 1 before a stop condition is generated. Clear the SO02 bit from 0 to 1 when the stop condition is generated.

Remark X: Don't care

Table 14-8. Relationship Between Register Settings and Pins (Channel 3: UART1 Reception)

SE03[Note 1]	MD032	MD031	TXE03	RXE03	PM31[Note 2]	P31[Note 2]	Operation mode	Pin Function
								SI10/SDA10/RxD1/INTP1/P31[Note 2]
0	0	1	0	0	×[Note 3]	×[Note 3]	Operation stop mode	SI10/SDA10/INTP1/P31[Note 2]
1	0	1	0	1	1	×	UART1 reception Notes 4, 5	RxD1

Notes 1. Serial channel enable status register 0 (SE0) is a read-only status register which is set using serial channel start register 0 (SS0) and serial channel stop register 0 (ST0).

2. When channel 3 is set to UART1 reception, this pin becomes an RxD1 function pin. In this case, set channel 2 to operation stop mode or UART1 transmission (refer to **Table 14-7**).
When channel 2 is set to CSI10 or IIC10, this pin cannot be used as an RxD1 function pin. In this case, set channel 3 to operation stop mode.

3. This pin can be set as a port function pin.

4. When using UART1 transmission and reception in a pair, set channel 2 to UART1 transmission (refer to **Table 14-7**).

5. Serial mode register 02 (SMR02) of channel 2 must also be set during UART1 reception. For details, refer to **14.6.2 (1) Register setting**.

Remark X: Don't care

14.9.2 78K0R/KF3-L, 78K0R/KG3-L

Table 14-9. Relationship between register settings and pins (Channel 0 of unit 0: CSI00, UART0 transmission)

SE00 Note 1	MD002	MD001	SOE00	SO00	CKO00	TXE00	RXE00	PM10	P10	PM11 Note 2	P11 Note 2	PM12	P12	Operation mode	Pin Function		
															$\overline{\text{SCK00}}$/P10	SI00/RxD0/P11 Note 2	SO00/TxD0/P12
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	P10	P11	P12
	0	1														P11/RxD0	
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	Slave CSI00 reception	$\overline{\text{SCK00}}$ (input)	SI00	P12
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	Slave CSI00 transmission	$\overline{\text{SCK00}}$ (input)	P11	SO00
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	Slave CSI00 transmission/ reception	$\overline{\text{SCK00}}$ (input)	SI00	SO00
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	Master CSI00 reception	$\overline{\text{SCK00}}$ (output)	SI00	P12
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	Master CSI00 transmission	$\overline{\text{SCK00}}$ (output)	P11	SO00
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	Master CSI00 transmission/ reception	$\overline{\text{SCK00}}$ (output)	SI00	SO00
	0	1	1	0/1 Note 4	1	1	0	× Note 3	× Note 3	× Note 3	× Note 3	0	1	UART0 transmission Note 5	P10	P11/RxD0	TxD0

Notes 1. Serial channel enable register 0 (SE0) is a read-only status register which is set using serial channel start register 0 (SS0) and serial channel stop register 0 (ST0).

2. When channel 1 of unit 0 is set to UART0 reception, this pin becomes an RxD0 function pin (refer to **Table 14-10**). In this case, operation stop mode or UART0 transmission must be selected for channel 0 of unit 0.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART0 transmission and reception in a pair, set channel 1 of unit 0 to UART0 reception (refer to **Table 14-10**).

Remark X: Don't care

Table 14-10. Relationship between register settings and pins (Channel 1 of unit 0: CSI01, UART0 reception)

SE01 Note 1	MD012	MD011	SOE01	SO01	CKO01	TXE01	RXE01	PM43	P43	PM44	P44	PM45	P45	PM11 Note 2	P11 Note 2	Operation mode	Pin Function			
																	$\overline{SCK01}$/P43	SI01/P44	SO01/P45	SI00/RxD0/P11 Note 2
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	P43	P44	P45	SI00/P11
	0	1																		
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	× Note 3	× Note 3	Slave CSI01 reception	$\overline{SCK01}$ (input)	SI01	P45	SI00/P11
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	× Note 3	× Note 3	Slave CSI01 transmission	$\overline{SCK01}$ (input)	P44	SO01	SI00/P11
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	× Note 3	× Note 3	Slave CSI01 transmission /reception	$\overline{SCK01}$ (input)	SI01	SO01	SI00/P11
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	× Note 3	× Note 3	Master CSI01 reception	$\overline{SCK01}$ (output)	SI01	P45	SI00/P11
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	× Note 3	× Note 3	Master CSI01 transmission	$\overline{SCK01}$ (output)	P44	SO01	SI00/P11
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	× Note 3	× Note 3	Master CSI01 transmission /reception	$\overline{SCK01}$ (output)	SI01	SO01	SI00/P11
	0	1	0	1	1	0	1	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	1	×	UART0 reception Notes 5, 6	P43	P44	P45	RxD0

Notes 1. Serial channel enable register 0 (SE0) is a read-only status register which is set using serial channel statrt register 0 (SS0) and serial channel stop register 0 (ST0).

2. When channel 1 of unit 0 is set to UART0 reception, this pin becomes an RxD0 function pin. In this case, set channel 0 of unit 0 to operation stop mode or UART0 transmission (refer to **Table 14-9**).
When channel 0 of unit 0 is set to CSI00, this pin cannot be used as an RxD0 function pin. In this case, set channel 1 of unit 0 to operation stop mode or CSI01.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART0 transmission and reception in a pair, set channel 0 of unit 0 to UART0 transmission (refer to **Table 14-9**).

6. Serial mode register 00 (SMR00) of channel 0 of unit 0 must also be set during UART0 reception. For details, refer to **14.6.2 (1) Register setting**.

Remark X: Don't care

Table 14-11. Relationship between register settings and pins
(Channel 2 of unit 0: CSI10, UART1 transmission, IIC10)

SE 02 Note 1	MD 022	MD 021	SOE 02	SO 02	CKO 02	TXE 02	RXE 02	PM 04	P04	PM03 Note 2	P03 Note 2	PM02	P02	Operation mode	Pin Function		
															$\overline{\text{SCK10}}$/ SCL10/P04	SI10/SDA10/ RxD1/P03 Note 2	SO10/ TxD1/P02
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	P04	P03	P02
	0	1														P03/RxD1	
	1	0														P03	
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	Slave CSI10 reception	$\overline{\text{SCK10}}$ (input)	SI10	P02
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	Slave CSI10 transmission	$\overline{\text{SCK10}}$ (input)	P03	SO10
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	Slave CSI10 transmission /reception	$\overline{\text{SCK10}}$ (input)	SI10	SO10
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	Master CSI10 reception	$\overline{\text{SCK10}}$ (output)	SI10	P02
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	Master CSI10 transmission	$\overline{\text{SCK10}}$ (output)	P03	SO10
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	Master CSI10 transmission /reception	$\overline{\text{SCK10}}$ (output)	SI10	SO10
	0	1	1	0/1 Note 4	1	1	0	× Note 3	× Note 3	× Note 3	× Note 3	0	1	UART1 transmission Note 5	P04	P03/RxD1	TxD1
0	1	0	0	0/1 Note 6	0/1 Note 6	0	0	0	1	0	1	× Note 3	× Note 3	IIC10 start condition	SCL10	SDA10	P02
						1	0										
						0	1										
1			1	0/1 Note 4	0/1 Note 4	1	0	0	1	0	1	× Note 3	× Note 3	IIC10 address field transmission	SCL10	SDA10	P02
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	0	1	× Note 3	× Note 3	IIC10 data transmission	SCL10	SDA10	P02
			1	0/1 Note 4	0/1 Note 4	0	1	0	1	0	1	× Note 3	× Note 3	IIC10 data reception	SCL10	SDA10	P02
0			0	0/1 Note 7	0/1 Note 7	0	0	0	1	0	1	× Note 3	× Note 3	IIC10 stop condition	SCL10	SDA10	P02
						1	0										
						0	1										

Notes 1. Serial channel enable register 0 (SE0) is a read-only status register which is set using serial channel statrt register 0 (SS0) and serial channel stop register 0 (ST0).

2. When channel 3 of unit 0 is set to UART1 reception, this pin becomes an RxD1 function pin (refer to **Table 14-12**). In this case, operation stop mode or UART1 transmission must be selected for channel 2 of unit 0.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART1 transmission and reception in a pair, set channel 3 of unit 0 to UART1 reception (refer to **Table 14-12**).

6. Set the CKO02 bit to 1 before a start condition is generated. Clear the SO02 bit from 1 to 0 when the start condition is generated.

7. Set the CKO02 bit to 1 before a stop condition is generated. Clear the SO02 bit from 0 to 1 when the stop condition is generated.

Remark X: Don't care

Table 14-12. Relationship between register settings and pins (Channel 3 of unit 0: UART1 reception)

SE03 Note 1	MD032	MD031	TXE03	RXE03	PM03 Note 2	P03 Note 2	Operation mode	Pin Function
								SI10/SDA10/RxD1/P03 Note 2
0	0	1	0	0	× Note 3	× Note 3	Operation stop mode	SI10/SDA10/P03 Note 2
1	0	1	0	1	1	×	UART1 reception Notes 4, 5	RxD1

Notes 1. Serial channel enable register 0 (SE0) is a read-only status register which is set using serial channel statrt register 0 (SS0) and serial channel stop register 0 (ST0).

2. When channel 3 of unit 0 is set to UART1 reception, this pin becomes an RxD1 function pin. In this case, set channel 2 of unit 0 to operation stop mode or UART1 transmission (refer to **Table 14-11**).
When channel 2 of unit 0 is set to CSI10 or IIC10, this pin cannot be used as an RxD1 function pin. In this case, set channel 3 of unit 0 to operation stop mode.

3. This pin can be set as a port function pin.

4. When using UART1 transmission and reception in a pair, set channel 2 of unit 0 to UART1 transmission (refer to **Table 14-11**).

5. Serial mode register 02 (SMR02) of channel 2 of unit 0 must also be set during UART1 reception. For details, refer to **14.6.2 (1) Register setting**.

Remark X: Don't care

Table 14-13. Relationship between register settings and pins
(Channel 0 of unit 1: CSI20, UART2 transmission, IIC20)

SE10 Note 1	MD102	MD101	SOE10	SO10	CKO10	TXE10	RXE10	PM142	P142	PM143 Note 2	P143 Note 2	PM144	P144	Operation mode	Pin Function		
															$\overline{SCK20}$/ SCL20/P142	SI20/SDA20/ RxD2/P143 Note 2	SO20/ TxD2/P144
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	P142	P143	P144
	0	1														P143/RxD2	
	1	0														P143	
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	Slave CSI20 reception	$\overline{SCK20}$ (input)	SI20	P144
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	Slave CSI20 transmission	$\overline{SCK20}$ (input)	P143	SO20
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	Slave CSI20 transmission/reception	$\overline{SCK20}$ (input)	SI20	SO20
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	Master CSI20 reception	$\overline{SCK20}$ (output)	SI20	P144
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	Master CSI20 transmission	$\overline{SCK20}$ (output)	P143	SO20
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	Master CSI20 transmission/reception	$\overline{SCK20}$ (output)	SI20	SO20
	0	1	1	0/1 Note 4	1	1	0	× Note 3	× Note 3	× Note 3	× Note 3	0	1	UART2 transmission Note 5	P142	P143/RxD2	TxD2
0	1	0	0	0/1 Note 6	0/1 Note 6	0	0	0	1	0	1	× Note 3	× Note 3	IIC20 start condition	SCL20	SDA20	P144
						1	0										
						0	1										
1			1	0/1 Note 4	0/1 Note 4	1	0	0	1	0	1	× Note 3	× Note 3	IIC20 address field transmission	SCL20	SDA20	P144
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	0	1	× Note 3	× Note 3	IIC20 data transmission	SCL20	SDA20	P144
			1	0/1 Note 4	0/1 Note 4	0	1	0	1	0	1	× Note 3	× Note 3	IIC20 data reception	SCL20	SDA20	P144
0			0	0/1 Note 7	0/1 Note 7	0	0	0	1	0	1	× Note 3	× Note 3	IIC20 stop condition	SCL20	SDA20	P144
						1	0										
						0	1										

Notes 1. Serial channel enable register 1 (SE1) is a read-only status register which is set using serial channel statrt register 1 (SS1) and serial channel stop register 1 (ST1).

2. When channel 1 of unit 1 is set to UART2 reception, this pin becomes an RxD2 function pin (refer to **Table 14-14**). In this case, operation stop mode or UART2 transmission must be selected for channel 0 of unit 1.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART2 transmission and reception in a pair, set channel 1 of unit 1 to UART2 reception (refer to **Table 14-14**).

6. Set the CKO10 bit to 1 before a start condition is generated. Clear the SO10 bit from 1 to 0 when the start condition is generated.

7. Set the CKO10 bit to 1 before a stop condition is generated. Clear the SO10 bit from 0 to 1 when the stop condition is generated.

Remark X: Don't care

Table 14-14. Relationship between register settings and pins (Channel 1 of unit 1: UART2 reception)

SE11 Note 1	MD112	MD111	TXE11	RXE11	PM143 Note 2	P143 Note 2	Operation mode	Pin Function
								SI20/SDA20/RxD2/P143 Note 2
0	0	1	0	0	× Note 3	× Note 3	Operation stop mode	SI20/SDA20/P143
1	0	1	0	1	1	×	UART2 reception Notes 4, 5	RxD2

Notes 1. Serial channel enable register 1 (SE1) is a read-only status register which is set using serial channel statrt register 1 (SS1) and serial channel stop register 1 (ST1).

2. When channel 1 of unit 1 is set to UART2 reception, this pin becomes an RxD2 function pin. In this case, set channel 0 of unit 1 to operation stop mode or UART2 transmission (refer to **Table 14-13**).
When channel 0 of unit 1 is set to CSI20 or IIC20, this pin cannot be used as an RxD2 function pin. In this case, set channel 1 of unit 1 to operation stop mode.

3. This pin can be set as a port function pin.

4. When using UART2 transmission and reception in a pair, set channel 0 of unit 1 to UART2 transmission (refer to **Table 14-13**).

5. Serial mode register 10 (SMR10) of channel 0 of unit 1 must also be set during UART2 reception. For details, refer to **14.6.2 (1) Register setting**.

Remark X: Don't care

Table 14-15. Relationship between register settings and pins (Channel 2 of unit 1: UART3 transmission)

SE12 Note1	MD122	MD121	SOE12	SO12	TXE12	RXE12	PM13 Note 2	P13 Note 2	Operation mode	Pin Function
										TxD3/P13
0	0	1	0	1	0	0	× Note 3	× Note 3	Operation stop mode	P13
1	0	1	1	0/1 Note 4	1	0	0	1	UART3 transmission Note 5	TxD3

Notes 1. Serial channel enable register 1 (SE1) is a read-only status register which is set using serial channel statrt register 1 (SS1) and serial channel stop register 1 (ST1)

2. When channel 3 of unit 1 is set to UART1 reception, this pin becomes an RxD3 function pin (refer to Table 14-16). In this case, set channel 2 of unit 1 to operation stop mode or UART2 transmission.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART3 transmission and reception in a pair, set channel 3 of unit 1 to UART3 reception (refer to **Table 14-16**).

Remark X: Don't care

Table 14-16. Relationship between register settings and pins (Channel 3 of unit 1: UART3 reception)

SE13 Note 1	MD132	MD131	TXE13	RXE13	PM14 Note 2	P14 Note 2	Operation mode	Pin Function
								RxD3/P14 Note 2
0	0	1	0	0	× Note 3	× Note 3	Operation stop mode	P14
1	0	1	0	1	1	×	UART3 reception Notes 4, 5	RxD3

Notes 1. Serial channel enable register 1 (SE1) is a read-only status register which is set using serial channel start register 1 (SS1) and serial channel stop register 1 (ST1)

2. When channel 1 of unit 1 is set to UART3 reception, this pin becomes an RxD3 function pin. In this case, set channel 2 of unit 1 to operation stop mode or UART3 transmission (refer to Table 14-15).

3. This pin can be set as a port function pin.

4. When using UART3 transmission and reception in a pair, set channel 2 of unit 1 to UART3 transmission (refer to **Table 14-15**).

5. Serial mode register 12 (SMR12) of channel 2 of unit 1 must also be set during UART3 reception. For details, refer to **14.6.2 (1) Register setting**.

Remark X: Don't care

Table 14-17. Relationship between register settings and pins (Channel 0 of unit 2: CSI40, UART4 transmission)

(μPD78F1027, 78F1028, 78F1029, 78F1030 only)

SE 20 Note 1	MD 202	MD 201	SOE 20	SO 20	CKO 20	TXE 20	RXE 20	PM 50	P50	PM 51 Note 2	P51 Note 2	PM 52	P52	Operation mode	Pin Function		
															$\overline{\text{SCK40}}$/ INTP1/ P50	SI40/ RxD4/ INTP2/ P51 Note 2	SO40/ TxD4/ TO00/P52
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	INTP1/ P50	INTP2/ P51	TO00/P52
	0	1														INTP2/ P51/RxD4	
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	Slave CSI40 reception	$\overline{\text{SCK40}}$ (input)	SI40	TO00/P52
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	Slave CSI40 transmission	$\overline{\text{SCK40}}$ (input)	INTP2/P51	SO40
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	Slave CSI40 transmission/ reception	$\overline{\text{SCK40}}$ (input)	SI40	SO40
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	Master CSI40 reception	$\overline{\text{SCK40}}$ (output)	SI40	TO00/P52
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	Master CSI40 transmission	$\overline{\text{SCK40}}$ (output)	INTP2/P51	SO40
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	Master CSI40 transmission/ reception	$\overline{\text{SCK40}}$ (output)	SI40	SO40
	0	1	1	0/1 Note 4	1	1	0	× Note 3	× Note 3	× Note 3	× Note 3	0	1	UART4 transmission Note 5	INTP1/ P50	INTP2/ P51/RxD4	TxD4

Notes 1. Serial channel enable register 2 (SE2) is a read-only status register which is set using serial channel start register 2 (SS2) and serial channel stop register 2 (ST2).

2. When channel 1 of unit 2 is set to UART4 reception, this pin becomes an RxD4 function pin (refer to **Table 14-18**). In this case, operation stop mode or UART4 transmission must be selected for channel 0 of unit 2.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART4 transmission and reception in a pair, set channel 1 of unit 2 to UART4 reception (refer to **Table 14-18**).

Remark X: Don't care

Table 14-18. Relationship between register settings and pins (Channel 1 of unit 2: CSI41, UART4 reception)

(μPD78F1027, 78F1028, 78F1029, 78F1030 only)

SE21 Note 1	MD212	MD211	SOE21	SO21	CKO21	TXE21	RXE21	PM53	P53	PM54	P54	PM55	P55	PM51 Note 2	P51 Note 2	Operation mode	Pin Function			
																	$\overline{\text{SCK41}}$/TI00/P53	SI41/TI07/TO07/P54	SO41/PCLBUZ1/INTP7/P55	SI40/RxD4/INTP2/P51 Note 2
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	TI00/P53	TI07/TO07/P54	PCLBUZ1/INTP7/P55	SI40/INTP2/P51
	0	1																		
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	× Note 3	× Note 3	Slave CSI41 reception	$\overline{\text{SCK41}}$ (input)	SI41	PCLBUZ1/INTP7/P55	SI40/INTP2/P51
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	× Note 3	× Note 3	Slave CSI41 transmission	$\overline{\text{SCK41}}$ (input)	TI07/TO07/P54	SO41	SI40/INTP2/P51
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	× Note 3	× Note 3	Slave CSI41 transmission /reception	$\overline{\text{SCK41}}$ (input)	SI41	SO41	SI40/INTP2/P51
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	× Note 3	× Note 3	Master CSI41 reception	$\overline{\text{SCK41}}$ (output)	SI41	PCLBUZ1/INTP7/P55	SI40/INTP2/P51
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	× Note 3	× Note 3	Master CSI41 transmission	$\overline{\text{SCK41}}$ (output)	TI07/TO07/P54	SO41	SI40/INTP2/P51
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	× Note 3	× Note 3	Master CSI41 transmission /reception	$\overline{\text{SCK41}}$ (output)	SI41	SO41	SI40/INTP2/P51
	0	1	0	1	1	0	1	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	1	×	UART4 reception Notes 5, 6	TI00/P53	TI07/TO07/P54	PCLBUZ1/INTP7/P55	RxD4

Notes 1. Serial channel enable register 2 (SE2) is a read-only status register which is set using serial channel statrt register 2 (SS2) and serial channel stop register 2 (ST2).

2. When channel 1 of unit 2 is set to UART4 reception, this pin becomes an RxD4 function pin. In this case, set channel 0 of unit 2 to operation stop mode or UART4 transmission (refer to **Table 14-17**).
When channel 0 of unit 2 is set to CSI40, this pin cannot be used as an RxD4 function pin. In this case, set channel 1 of unit 2 to operation stop mode or CSI41.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART4 transmission and reception in a pair, set channel 0 of unit 2 to UART4 transmission (refer to **Table 14-17**).

6. Serial mode register 20 (SMR20) of channel 0 of unit 2 must also be set during UART4 reception. For details, refer to **14.6.2 (1) Register setting**.

Remark X: Don't care

CHAPTER 15 SERIAL INTERFACE IICA

Remark 40-pin and 44-pin products of the 78K0R/KC3-L are not provided with serial interface IICA.

15.1 Functions of Serial Interface IICA

Serial interface IICA has the following three modes.

(1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

(2) I^2C bus mode (multimaster supported)

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCL0) line and a serial data bus (SDA0) line.

This mode complies with the I^2C bus format and the master device can generated “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I^2C bus.

Since the SCL0 and SDA0 pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.

(3) Wakeup mode

The STOP mode can be released by generating an interrupt request signal (INTIICA) when an extension code from the master device or a local address has been received while in STOP mode. This can be set by using the WUP bit of IICA control register 1 (IICCTL1).

Figure 15-1 shows a block diagram of serial interface IICA.

Figure 15-1. Block Diagram of Serial Interface IICA

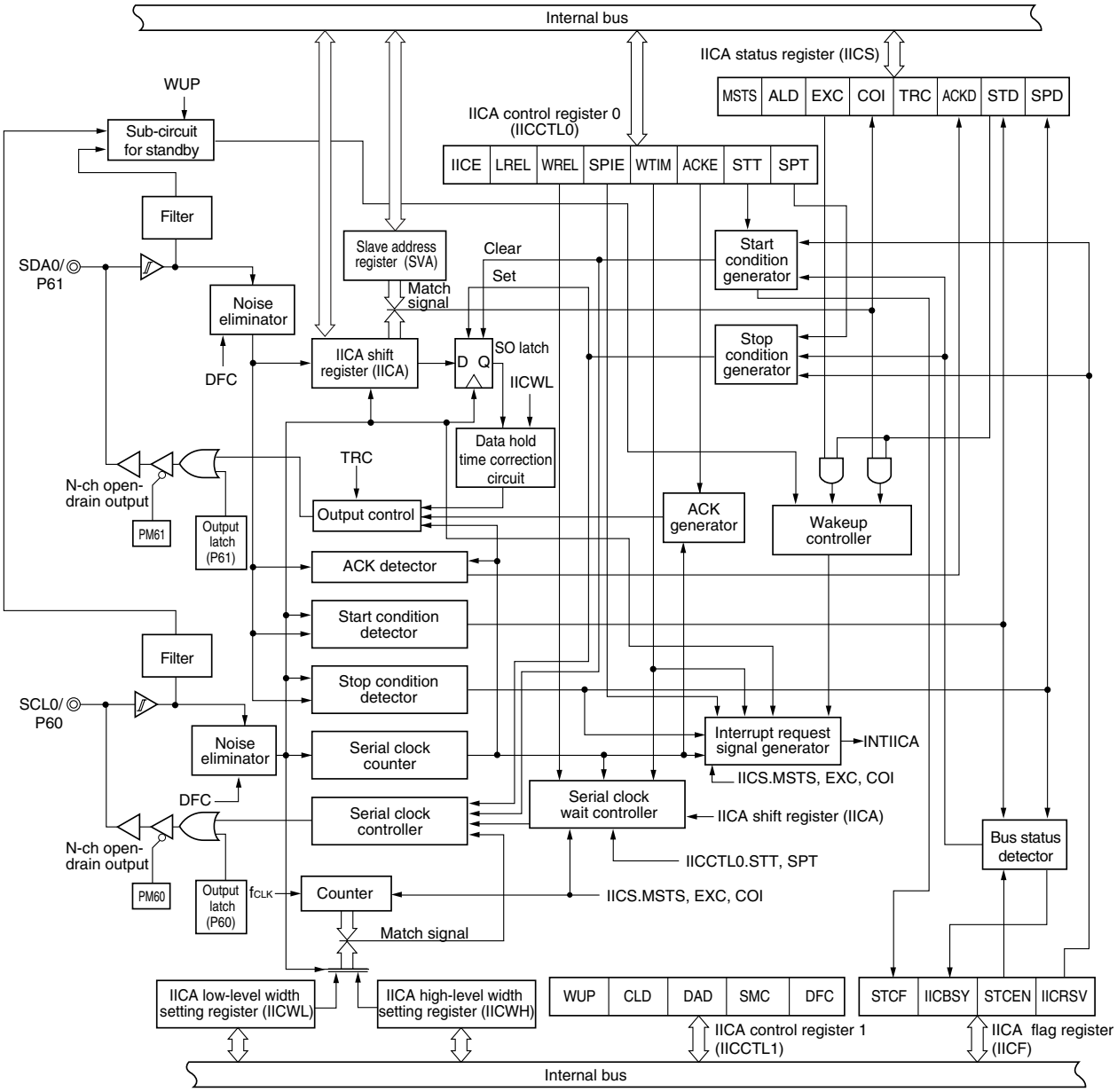
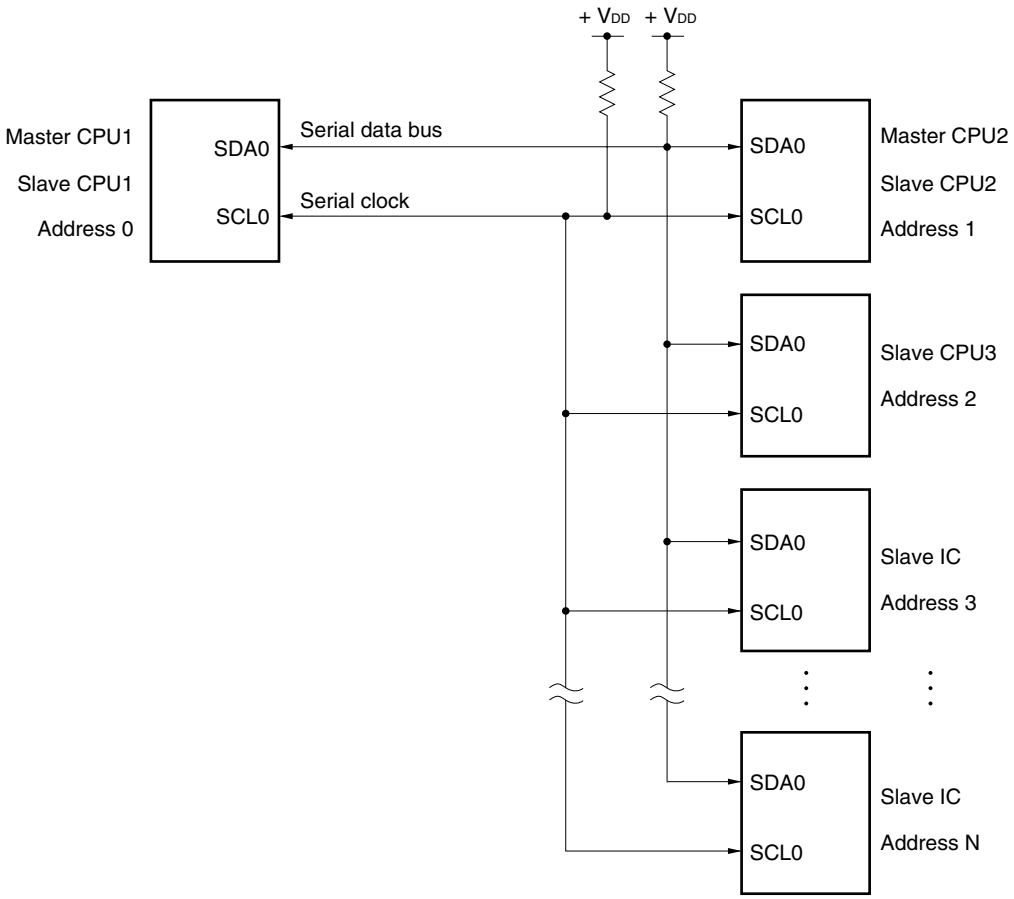


Figure 15-2 shows a serial bus configuration example.

Figure 15-2. Serial Bus Configuration Example Using I²C Bus



15.2 Configuration of Serial Interface IICA

Serial interface IICA includes the following hardware.

Table 15-1. Configuration of Serial Interface IICA

Item	Configuration
Registers	IICA shift register (IICA) Slave address register (SVA)
Control registers	Peripheral enable register 0 (PER0) IICA control register 0 (IICCTL0) IICA status register (IICS) IICA flag register (IICF) IICA control register 1 (IICCTL1) IICA low-level width setting register (IICWL) IICA high-level width setting register (IICWH) Port mode register 6 (PM6) Port register 6 (P6)

(1) IICA shift register (IICA)

The IICA register is used to convert 8-bit serial data to 8-bit parallel data and vice versa in synchronization with the serial clock. The IICA register can be used for both transmission and reception.

The actual transmit and receive operations can be controlled by writing and reading operations to the IICA register.

Cancel the wait state and start data transfer by writing data to the IICA register during the wait period.

The IICA register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears IICA to 00H.

Figure 15-3. Format of IICA Shift Register (IICA)

Address: FFF50H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IICA								

Cautions 1. Do not write data to the IICA register during data transfer.

2. Write or read the IICA register only during the wait period. Accessing the IICA register in a communication state other than during the wait period is prohibited. When the device serves as the master, however, the IICA register can be written only once after the communication trigger bit (STT) is set to 1.

3. When communication is reserved, write data to the IICA register after the interrupt triggered by a stop condition is detected.

(2) Slave address register (SVA)

This register stores seven bits of local addresses {A6, A5, A4, A3, A2, A1, A0} when in slave mode.

The SVA register can be set by an 8-bit memory manipulation instruction.

However, rewriting to this register is prohibited while STD = 1 (while the start condition is detected).

Reset signal generation clears the SVA register to 00H.

Figure 15-4. Format of Slave Address Register (SVA)

Address: F0234H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SVA	A6	A5	A4	A3	A2	A1	A0	0[Note]

Note Bit 0 is fixed to 0.

(3) SO latch

The SO latch is used to retain the SDA0 pin's output level.

(4) Wakeup controller

This circuit generates an interrupt request (INTIICA) when the address received by this register matches the address value set to the slave address register (SVA) or when an extension code is received.

(5) Serial clock counter

This counter counts the serial clocks that are output or input during transmit/receive operations and is used to verify that 8-bit data was transmitted or received.

(6) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIICA).

An I^2C interrupt request is generated by the following two triggers.

- Falling edge of eighth or ninth clock of the serial clock (set by the WTIM bit)
- Interrupt request generated when a stop condition is detected (set by the SPIE bit)

Remark WTIM bit: Bit 3 of IICA control register 0 (IICCTL0)
SPIE bit: Bit 4 of IICA control register 0 (IICCTL0)

(7) Serial clock controller

In master mode, this circuit generates the clock output via the SCL0 pin from a sampling clock.

(8) Serial clock wait controller

This circuit controls the wait timing.

(9) ACK generator, stop condition detector, start condition detector, and ACK detector

These circuits generate and detect each status.

(10) Data hold time correction circuit

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

(11) Start condition generator

This circuit generates a start condition when the STT bit is set to 1.

However, in the communication reservation disabled status (IICRSV bit = 1), when the bus is not released (IICBSY bit = 1), start condition requests are ignored and the STCF bit is set to 1.

(12) Stop condition generator

This circuit generates a stop condition when the SPT bit is set to 1.

(13) Bus status detector

This circuit detects whether or not the bus is released by detecting start conditions and stop conditions.

However, as the bus status cannot be detected immediately following operation, the initial status is set by the STCEN bit.

Remark STT bit: Bit 1 of IICA control register 0 (IICCTL0)
SPT bit: Bit 0 of IICA control register 0 (IICCTL0)
IICRSV bit: Bit 0 of IICA flag register (IICF)
IICBSY bit: Bit 6 of IICA flag register (IICF)
STCF bit: Bit 7 of IICA flag register (IICF)
STCEN bit: Bit 1 of IICA flag register (IICF)

15.3 Registers Controlling Serial Interface IICA

Serial interface IICA is controlled by the following nine registers.

- Peripheral enable register 0 (PER0)
- IICA control register 0 (IICCTL0)
- IICA flag register (IICF)
- IICA status register (IICS)
- IICA control register 1 (IICCTL1)
- IICA low-level width setting register (IICWL)
- IICA high-level width setting register (IICWH)
- Port mode register 6 (PM6)
- Port register 6 (P6)

(1) Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When serial interface IICA is used, be sure to set bit 4 (IICAEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 15-5. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN Note 1	0	ADCEN	IICAEN Note 2	SAU1EN Note 3	SAU0EN	TAU1EN Note 3	TAU0EN Note 3

IICAEN	Control of serial interface IICA input clock supply
0	Stops input clock supply. • SFR used by serial interface IICA cannot be written. • Serial interface IICA is in the reset status.
1	Enables input clock supply. • SFR used by serial interface IICA can be read/written.

Notes 1. This is not mounted onto 40-pin product of the 78K0R/KC3-L.

2. This is not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.

3. 78K0R/KF3-L and 78K0R/KG3-L only.

Cautions 1. When setting serial interface IICA, be sure to set the IICAEN bit to 1 first. If IICAEN = 0, writing to a control register of serial interface IICA is ignored, and, even if the register is read, only the default value is read (except for port mode register 6 (PM6) and port register 6 (P6)).

2. Be sure to clear the following bits to 0.

48-pin product of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: bits 0, 1, 3, 6

44-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6

40-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6, 7

78K0R/KF3-L, 78K0R/KG3-L: bit 6

(2) IICA control register 0 (IICCTL0)

This register is used to enable/stop I^2C operations, set wait timing, and set other I^2C operations.

The IICCTL0 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, set the SPIE, WTIM, and ACKE bits while IICE = 0 or during the wait period. These bits can be set at the same time when the IICE bit is set from “0” to “1”.

Reset signal generation clears this register to 00H.

Figure 15-6. Format of IICA Control Register 0 (IICCTL0) (1/4)

Address: F0230H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICCTL0	IICE	LREL	WREL	SPIE	WTIM	ACKE	STT	SPT

IICE	I^2C operation enable
0	Stop operation. Reset the IICA status register (IICS)[Note 1]. Stop internal operation.
1	Enable operation.
Be sure to set this bit (1) while the SCL0 and SDA0 lines are at high level.	
Condition for clearing (IICE = 0)	Condition for setting (IICE = 1)
• Cleared by instruction • Reset	• Set by instruction

LREL[Notes 2, 3]	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCL0 and SDA0 lines are set to high impedance. The following flags of IICA control register 0 (IICCTL0) and the IICA status register (IICS) are cleared to 0. • STT • SPT • MSTS • EXC • COI • TRC • ACKD • STD
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL = 0)	Condition for setting (LREL = 1)
• Automatically cleared after execution • Reset	• Set by instruction

WREL[Notes 2, 3]	Wait cancellation
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared after wait is canceled.
When the WREL bit is set (wait canceled) during the wait period at the ninth clock pulse in the transmission status (TRC = 1), the SDA0 line goes into the high impedance state (TRC = 0).	
Condition for clearing (WREL = 0)	Condition for setting (WREL = 1)
• Automatically cleared after execution • Reset	• Set by instruction

Notes 1. The IICA status register (IICS), the STCF and IICBSY bits of the IICA flag register (IICF), and the CLD and DAD bits of IICA control register 1 (IICCTL1) are reset.

2. The signal of this bit is invalid while IICE0 is 0.

3. When the LREL and WREL bits are read, 0 is always read.

Caution If the operation of I^2C is enabled (IICE = 1) when the SCL0 line is high level, the SDA0 line is low level, and the digital filter is turned on (DFC bit of IICCTL1 register = 1), a start condition will be inadvertently detected immediately. In this case, set (1) the LREL bit by using a 1-bit memory manipulation instruction immediately after enabling operation of I^2C (IICE = 1).

Figure 15-6. Format of IICA Control Register 0 (IICCTL0) (2/4)

SPIE[Note 1]	Enable/disable generation of interrupt request when stop condition is detected
0	Disable
1	Enable
If the WUP bit of IICA control register 1 (IICCTL1) is 1, no stop condition interrupt will be generated even if SPIE = 1.	
Condition for clearing (SPIE = 0)	Condition for setting (SPIE = 1)
• Cleared by instruction • Reset	• Set by instruction

WTIM[Note 1]	Control of wait and interrupt request generation
0	Interrupt request is generated at the eighth clock's falling edge. Master mode: After output of eight clocks, clock output is set to low level and wait is set. Slave mode: After input of eight clocks, the clock is set to low level and wait is set for master device.
1	Interrupt request is generated at the ninth clock's falling edge. Master mode: After output of nine clocks, clock output is set to low level and wait is set. Slave mode: After input of nine clocks, the clock is set to low level and wait is set for master device.
An interrupt is generated at the falling edge of the ninth clock during address transfer independently of the setting of this bit. The setting of this bit is valid when the address transfer is completed. When in master mode, a wait is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a wait is inserted at the falling edge of the ninth clock after an acknowledge ($\overline{ACK}$) is issued. However, when the slave device has received an extension code, a wait is inserted at the falling edge of the eighth clock.	
Condition for clearing (WTIM = 0)	Condition for setting (WTIM = 1)
• Cleared by instruction • Reset	• Set by instruction

ACKE[Notes 1, 2]	Acknowledgment control
0	Disable acknowledgment.
1	Enable acknowledgment. During the ninth clock period, the SDA0 line is set to low level.
Condition for clearing (ACKE = 0)	Condition for setting (ACKE = 1)
• Cleared by instruction • Reset	• Set by instruction

Notes 1. The signal of this bit is invalid while IICE0 is 0. Set this bit during that period.

2. The set value is invalid during address transfer and if the code is not an extension code.
When the device serves as a slave and the addresses match, an acknowledgment is generated regardless of the set value.

Figure 15-6. Format of IICA Control Register 0 (IICCTL0) (3/4)

STT[Note]	Start condition trigger
0	Do not generate a start condition.
1	When bus is released (in standby state, when IICBSY = 0): If this bit is set (1), a start condition is generated (startup as the master). When a third party is communicating: • When communication reservation function is enabled (IICRSV = 0) Functions as the start condition reservation flag. When set to 1, automatically generates a start condition after the bus is released. • When communication reservation function is disabled (IICRSV = 1) Even if this bit is set (1), the STT bit is cleared and the STT clear flag (STCF) is set (1). No start condition is generated. In the wait state (when master device): Generates a restart condition after releasing the wait.

Cautions concerning set timing
- For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the waiting period when the ACKE bit has been cleared to 0 and slave has been notified of final reception.
- For master transmission: A start condition cannot be generated normally during the acknowledge period. Set to 1 during the wait period that follows output of the ninth clock.
- Cannot be set to 1 at the same time as stop condition trigger (SPT).
- Setting the STT bit to 1 and then setting it again before it is cleared to 0 is prohibited.

Condition for clearing (STT = 0)	Condition for setting (STT = 1)
• Cleared by setting the STT bit to 1 while communication reservation is prohibited. • Cleared by loss in arbitration • Cleared after start condition is generated by master device • Cleared by LREL = 1 (exit from communications) • When IICE = 0 (operation stop) • Reset	• Set by instruction

Note The signal of this bit is invalid while IICE0 is 0.

Remarks 1. Bit 1 (STT) becomes 0 when it is read after data setting.

2. IICRSV: Bit 0 of IIC flag register (IICF)
STCF: Bit 7 of IIC flag register (IICF)

Figure 15-6. Format of IICA Control Register 0 (IICCTL0) (4/4)

SPT	Stop condition trigger
0	Stop condition is not generated.
1	Stop condition is generated (termination of master device's transfer).

Cautions concerning set timing
- For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the waiting period when the ACKE bit has been cleared to 0 and slave has been notified of final reception.
- For master transmission: A stop condition cannot be generated normally during the acknowledge period. Therefore, set it during the wait period that follows output of the ninth clock.
- Cannot be set to 1 at the same time as start condition trigger (STT).
- The SPT bit can be set to 1 only when in master mode.
- When the WTIM bit has been cleared to 0, if the SPT bit is set to 1 during the wait period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock. The WTIM bit should be changed from 0 to 1 during the wait period following the output of eight clocks, and the SPT bit should be set to 1 during the wait period that follows the output of the ninth clock.
- Setting the SPT bit to 1 and then setting it again before it is cleared to 0 is prohibited.

Condition for clearing (SPT = 0)	Condition for setting (SPT = 1)
• Cleared by loss in arbitration • Automatically cleared after stop condition is detected • Cleared by LREL = 1 (exit from communications) • When IICE = 0 (operation stop) • Reset	• Set by instruction

Caution When bit 3 (TRC) of the IICA status register (IICS) is set to 1 (transmission status), bit 5 (WREL) of IICA control register 0 (IICCTL0) is set to 1 during the ninth clock and wait is canceled, after which the TRC bit is cleared (reception status) and the SDA0 line is set to high impedance. Release the wait performed while the TRC bit is 1 (transmission status) by writing to the IICA shift register.

Remark Bit 0 (SPT) becomes 0 when it is read after data setting.

(3) IICA status register (IICS)

This register indicates the status of I^2C.

The IICS register is read by a 1-bit or 8-bit memory manipulation instruction only when STT = 1 and during the wait period.

Reset signal generation clears this register to 00H.

Caution Reading the IICS register while the address match wakeup function is enabled (WUP = 1) in STOP mode is prohibited. When the WUP bit is changed from 1 to 0 (wakeup operation is stopped), regardless of the INTIICA interrupt request, the change in status is not reflected until the next start condition or stop condition is detected. To use the wakeup function, therefore, enable (SPIE = 1) the interrupt generated by detecting a stop condition and read the IICS register after the interrupt has been detected.

Remark STT: bit 1 of IICA control register 0 (IICCTL0)
WUP: bit 7 of IICA control register 1 (IICCTL1)

Figure 15-7. Format of IICA Status Register (IICS) (1/3)

Address: FFF51H After reset: 00H R

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICS	MSTS	ALD	EXC	COI	TRC	ACKD	STD	SPD

MSTS	Master status check flag
0	Slave device status or communication standby status
1	Master device communication status

Condition for clearing (MSTS = 0)	Condition for setting (MSTS = 1)
• When a stop condition is detected • When ALD = 1 (arbitration loss) • Cleared by LREL = 1 (exit from communications) • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is generated

ALD	Detection of arbitration loss
0	This status means either that there was no arbitration or that the arbitration result was a “win”.
1	This status indicates the arbitration result was a “loss”. The MSTS bit is cleared.

Condition for clearing (ALD = 0)	Condition for setting (ALD = 1)
• Automatically cleared after the IICS register is read[Note] • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• When the arbitration result is a “loss”.

Note This register is also cleared when a 1-bit memory manipulation instruction is executed for bits other than the IICS register. Therefore, when using the ALD bit, read the data of this bit before the data of the other bits.

Remark LREL: Bit 6 of IICA control register 0 (IICCTL0)
IICE: Bit 7 of IICA control register 0 (IICCTL0)

Figure 15-7. Format of IICA Status Register (IICS) (2/3)

EXC	Detection of extension code reception
0	Extension code was not received.
1	Extension code was received.

Condition for clearing (EXC = 0)	Condition for setting (EXC = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LREL = 1 (exit from communications) • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• When the higher four bits of the received address data is either “0000” or “1111” (set at the rising edge of the eighth clock).

COI	Detection of matching addresses
0	Addresses do not match.
1	Addresses match.

Condition for clearing (COI = 0)	Condition for setting (COI = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LREL = 1 (exit from communications) • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• When the received address matches the local address (slave address register (SVA)) (set at the rising edge of the eighth clock).

TRC	Detection of transmit/receive status
0	Receive status (other than transmit status). The SDA0 line is set for high impedance.
1	Transmit status. The value in the SO0 latch is enabled for output to the SDA0 line (valid starting at the falling edge of the first byte’s ninth clock).

Condition for clearing (TRC = 0)	Condition for setting (TRC = 1)
<Both master and slave> • When a stop condition is detected • Cleared by LREL = 1 (exit from communications) • When the IICE bit changes from 1 to 0 (operation stop) • Cleared by WREL = 1[Note] (wait cancel) • When the ALD bit changes from 0 to 1 (arbitration loss) • Reset • When not used for communication (MSTS, EXC, COI = 0) <Master> • When “1” is output to the first byte’s LSB (transfer direction specification bit) <Slave> • When a start condition is detected • When “0” is input to the first byte’s LSB (transfer direction specification bit)	<Master> • When a start condition is generated • When 0 (master transmission) is output to the LSB (transfer direction specification bit) of the first byte (during address transfer) <Slave> • When 1 (slave transmission) is input to the LSB (transfer direction specification bit) of the first byte from the master (during address transfer)

Note When bit 3 (TRC) of the IICA status register (IICS) is set to 1 (transmission status), bit 5 (WREL) of IICA control register 0 (IICCTL0) is set to 1 during the ninth clock and wait is canceled, after which the TRC bit is cleared (reception status) and the SDA0 line is set to high impedance. Release the wait performed while the TRC bit is 1 (transmission status) by writing to the IICA shift register.

Remark LREL: Bit 6 of IICA control register 0 (IICCTL0)
IICE: Bit 7 of IICA control register 0 (IICCTL0)

Figure 15-7. Format of IICA Status Register (IICS) (3/3)

ACKD	Detection of acknowledge ($\overline{ACK}$)
0	Acknowledge was not detected.
1	Acknowledge was detected.

Condition for clearing (ACKD = 0)	Condition for setting (ACKD = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by LREL = 1 (exit from communications) • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• After the SDA0 line is set to low level at the rising edge of SCL0 line's ninth clock

STD	Detection of start condition
0	Start condition was not detected.
1	Start condition was detected. This indicates that the address transfer period is in effect.

Condition for clearing (STD = 0)	Condition for setting (STD = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by LREL = 1 (exit from communications) • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is detected

SPD	Detection of stop condition
0	Stop condition was not detected.
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

Condition for clearing (SPD = 0)	Condition for setting (SPD = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• When a stop condition is detected

Remark LREL: Bit 6 of IICA control register 0 (IICCTL0)
IICE: Bit 7 of IICA control register 0 (IICCTL0)

(4) IICA flag register (IICF)

This register sets the operation mode of I^2C and indicates the status of the I^2C bus.

The IICF register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the STT clear flag (STCF) and I^2C bus status flag (IICBSY) bits are read-only.

The IICRSV bit can be used to enable/disable the communication reservation function.

The STCEN bit can be used to set the initial value of the IICBSY bit.

The IICRSV and STCEN bits can be written only when the operation of I^2C is disabled (bit 7 (IICE) of IICA control register 0 (IICCTL0) = 0). When operation is enabled, the IICF register can be read.

Reset signal generation clears this register to 00H.

Figure 15-8. Format of IICA Flag Register (IICF)

Address: FFF52H After reset: 00H R/W[Note]

Symbol	<7>	<6>	5	4	3	2	<1>	<0>
IICF	STCF	IICBSY	0	0	0	0	STCEN	IICRSV

STCF	STT clear flag
0	Generate start condition
1	Start condition generation unsuccessful: clear the STT flag

Condition for clearing (STCF = 0)	Condition for setting (STCF = 1)
• Cleared by STT = 1 • When IICE = 0 (operation stop) • Reset	• Generating start condition unsuccessful and the STT bit cleared to 0 when communication reservation is disabled (IICRSV = 1).

IICBSY	I^2C bus status flag
0	Bus release status (communication initial status when STCEN = 1)
1	Bus communication status (communication initial status when STCEN = 0)

Condition for clearing (IICBSY = 0)	Condition for setting (IICBSY = 1)
• Detection of stop condition • When IICE = 0 (operation stop) • Reset	• Detection of start condition • Setting of the IICE bit when STCEN = 0

STCEN	Initial start enable trigger
0	After operation is enabled (IICE = 1), enable generation of a start condition upon detection of a stop condition.
1	After operation is enabled (IICE = 1), enable generation of a start condition without detecting a stop condition.

Condition for clearing (STCEN = 0)	Condition for setting (STCEN = 1)
• Cleared by instruction • Detection of start condition • Reset	• Set by instruction

IICRSV	Communication reservation function disable bit
0	Enable communication reservation
1	Disable communication reservation

Condition for clearing (IICRSV = 0)	Condition for setting (IICRSV = 1)
• Cleared by instruction • Reset	• Set by instruction

Note Bits 6 and 7 are read-only.

Cautions 1. Write to the STCEN bit only when the operation is stopped (IICE = 0).

2. As the bus release status (IICBSY = 0) is recognized regardless of the actual bus status when STCEN = 1, when generating the first start condition (STT = 1), it is necessary to verify that no third party communications are in progress in order to prevent such communications from being destroyed.

3. Write to IICRSV only when the operation is stopped (IICE = 0).

Remark STT: Bit 1 of IICA control register 0 (IICCTL0)
IICE: Bit 7 of IICA control register 0 (IICCTL0)

(5) IICA control register 1 (IICCTL1)

This register is used to set the operation mode of I^2C and detect the statuses of the SCL0 and SDA0 pins.

The IICCTL1 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the CLD and DAD bits are read-only.

Set the IICCTL1 register, except the WUP bit, while operation of I^2C is disabled (bit 7 (IICE) of IICA control register 0 (IICCTL0) is 0).

Reset signal generation clears this register to 00H.

Figure 15-9. Format of IICA Control Register 1 (IICCTL1) (1/2)

Address: F0231H After reset: 00H R/W[Note 1]

Symbol	7	6	<5>	<4>	<3>	<2>	1	0
IICCTL1	WUP	0	CLD	DAD	SMC	DFC	0	0

WUP	Control of address match wakeup
0	Stops operation of address match wakeup function in STOP mode.
1	Enables operation of address match wakeup function in STOP mode.

To shift to STOP mode when WUP = 1, execute the STOP instruction at least three clocks after setting (1) the WUP bit (see **Figure 15-22 Flow When Setting WUP = 1**).

Clear (0) the WUP bit after the address has matched or an extension code has been received. The subsequent communication can be entered by the clearing (0) WUP bit. (The wait must be released and transmit data must be written after the WUP bit has been cleared (0).)

The interrupt timing when the address has matched or when an extension code has been received, while WUP = 1, is identical to the interrupt timing when WUP = 0. (A delay of the difference of sampling by the clock will occur.) Furthermore, when WUP = 1, a stop condition interrupt is not generated even if the SPIE bit is set to 1.

When WUP = 0 is set by a source other than an interrupt from serial interface IICA, operation as the master device cannot be performed until the subsequent start condition or stop condition is detected. Do not output a start condition by setting (1) the STT bit, without waiting for the detection of the subsequent start condition or stop condition.

Condition for clearing (WUP = 0)	Condition for setting (WUP = 1)
• Cleared by instruction (after address match or extension code reception)	• Set by instruction (when the MSTS, EXC, and COI bits are “0”, and the STD bit also “0” (communication not entered))[Note 2]

Notes 1. Bits 4 and 5 are read-only.

2. The status of the IICA status register (IICS) must be checked and the WUP bit must be set during the period shown below.

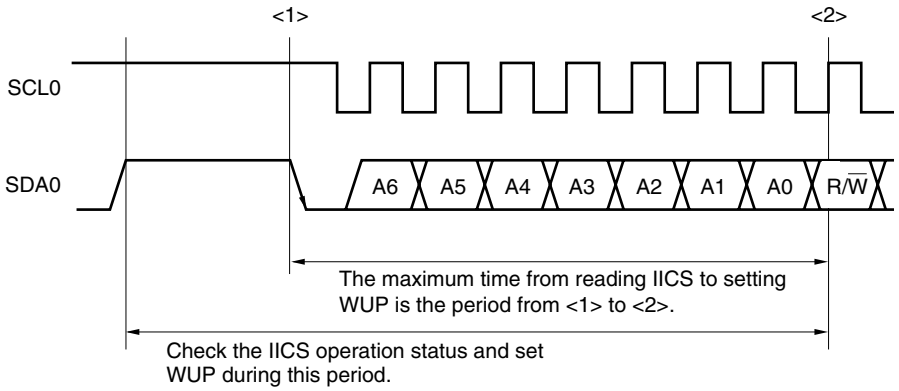


Figure 15-9. Format of IICA Control Register 1 (IICCTL1) (2/2)

CLD	Detection of SCL0 pin level (valid only when IICE = 1)
0	The SCL0 pin was detected at low level.
1	The SCL0 pin was detected at high level.

Condition for clearing (CLD = 0)	Condition for setting (CLD = 1)
• When the SCL0 pin is at low level • When IICE = 0 (operation stop) • Reset	• When the SCL0 pin is at high level

DAD	Detection of SDA0 pin level (valid only when IICE = 1)
0	The SDA0 pin was detected at low level.
1	The SDA0 pin was detected at high level.

Condition for clearing (DAD = 0)	Condition for setting (DAD = 1)
• When the SDA0 pin is at low level • When IICE = 0 (operation stop) • Reset	• When the SDA0 pin is at high level

SMC	Operation mode switching
0	Operates in standard mode.
1	Operates in fast mode.

DFC	Digital filter operation control
0	Digital filter off.
1	Digital filter on.
Digital filter can be used only in fast mode. In fast mode, the transfer clock does not vary, regardless of the DFC bit being set (1) or cleared (0). The digital filter is used for noise elimination in fast mode.	

Remark IICE: Bit 7 of IICA control register 0 (IICCTL0)

(6) IICA low-level width setting register (IICWL)

This register is used to set the low-level width of the SCL0 pin signal that is output by serial interface IICA.

The IICWL register can be set by an 8-bit memory manipulation instruction.

Set the IICWL register while operation of I^2C is disabled (bit 7 (IICE) of IICA control register 0 (IICCTL0) is 0).

Reset signal generation sets this register to FFH.

Figure 15-10. Format of IICA Low-Level Width Setting Register (IICWL)

Address: F0232H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
IICWL								

(7) IICA high-level width setting register (IICWH)

This register is used to set the high-level width of the SCL0 pin signal that is output by serial interface IICA.

The IICWH register can be set by an 8-bit memory manipulation instruction.

Set the IICWL register while operation of I^2C is disabled (bit 7 (IICE) of IICA control register 0 (IICCTL0) is 0).

Reset signal generation sets this register to FFH.

Figure 15-11. Format of IICA High-Level Width Setting Register (IICWH)

Address: F0233H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
IICWH								

Remark For how to set the transfer clock by using the IICWL and IICWH registers, see **15.4.2 Setting transfer clock by using IICWL and IICWH registers**.

(8) Port mode register 6 (PM6)

This register sets the input/output of port 6 in 1-bit units.

When using the P60/SCL0 pin as clock I/O and the P61/SDA0 pin as serial data I/O, clear PM60 and PM61, and the output latches of P60 and P61 to 0.

Set the IICE bit (bit 7 of IICA control register 0 (IICCTL0)) to 1 before setting the output mode because the P60/SCL0 and P61/SDA0 pins output a low level (fixed) when the IICE bit is 0.

The PM6 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 15-12. Format of Port Mode Register 6 (PM6)

Address: FFF26H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM6	1	1	1	1	1	1	PM61	PM60

PM6n	P6n pin I/O mode selection (n = 0, 1)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

15.4 I^2C Bus Mode Functions

15.4.1 Pin configuration

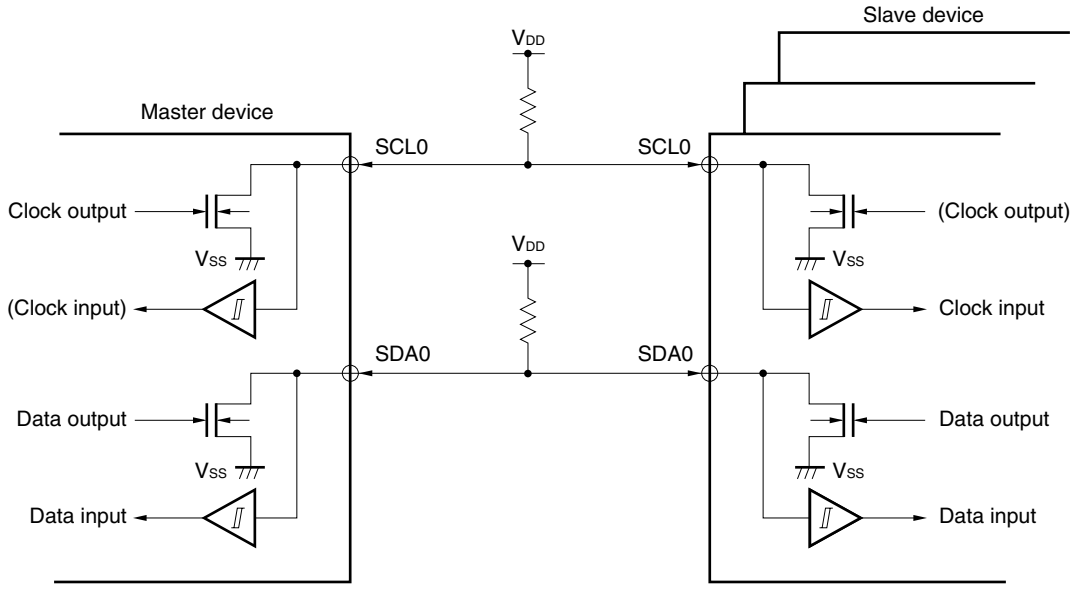
The serial clock pin (SCL0) and the serial data bus pin (SDA0) are configured as follows.

(1) SCL0..... This pin is used for serial clock input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

(2) SDA0 ..... This pin is used for serial data input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

Since outputs from the serial clock line and the serial data bus line are N-ch open-drain outputs, an external pull-up resistor is required.

Figure 15-13. Pin Configuration Diagram



15.4.2 Setting transfer clock by using IICWL and IICWH registers

(1) Setting transfer clock on master side

$$\text{Transfer clock} = \frac{f_{CLK}}{IICWL + IICWH + f_{CLK}(t_R + t_F)}$$

At this time, the optimal setting values of the IICWL and IICWH registers are as follows.
(The fractional parts of all setting values are rounded up.)

- When the fast mode

$$IICWL = \frac{0.52}{\text{Transfer clock}} \times f_{CLK}$$
$$IICWH = \left(\frac{0.48}{\text{Transfer clock}} - t_R - t_F\right) \times f_{CLK}$$

- When the normal mode

$$IICWL = \frac{0.47}{\text{Transfer clock}} \times f_{CLK}$$
$$IICWH = \left(\frac{0.53}{\text{Transfer clock}} - t_R - t_F\right) \times f_{CLK}$$

(2) Setting IICWL and IICWH registers on slave side

(The fractional parts of all setting values are truncated.)

- When the fast mode

$$IICWL = 1.3\ \mu s \times f_{CLK}$$
$$IICWH = (1.2\ \mu s - t_R - t_F) \times f_{CLK}$$

- When the normal mode

$$IICWL = 4.7\ \mu s \times f_{CLK}$$
$$IICWH = (5.3\ \mu s - t_R - t_F) \times f_{CLK}$$

Caution Note the minimum f_{CLK} operation frequency when setting the transfer clock. The minimum f_{CLK} operation frequency for serial interface IICA is determined according to the mode.

Fast mode: f_{CLK} = 3.5 MHz (MIN.)

Normal mode: f_{CLK} = 1 MHz (MIN.)

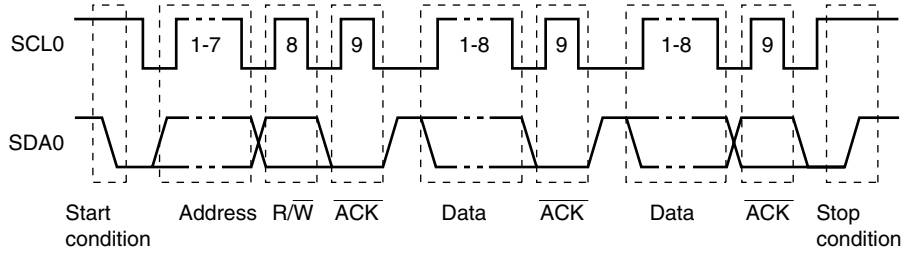
Remarks 1. Calculate the rise time (t_R) and fall time (t_F) of the SDA0 and SCL0 signals separately, because they differ depending on the pull-up resistance and wire load.

2. IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDA0 and SCL0 signal falling times
t_R: SDA0 and SCL0 signal rising times
f_{CLK}: CPU/peripheral hardware clock frequency

15.5 I^2C Bus Definitions and Control Methods

The following section describes the I^2C bus's serial data communication format and the signals used by the I^2C bus. Figure 15-14 shows the transfer timing for the "start condition", "address", "data", and "stop condition" output via the I^2C bus's serial data bus.

Figure 15-14. I^2C Bus Serial Data Transfer Timing



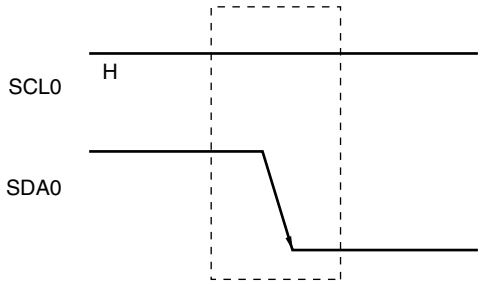
The master device generates the start condition, slave address, and stop condition.
The acknowledge ($\overline{ACK}$) can be generated by either the master or slave device (normally, it is output by the device that receives 8-bit data).

The serial clock (SCL0) is continuously output by the master device. However, in the slave device, the SCL0 pin low level period can be extended and a wait can be inserted.

15.5.1 Start conditions

A start condition is met when the SCL0 pin is at high level and the SDA0 pin changes from high level to low level. The start conditions for the SCL0 pin and SDA0 pin are signals that the master device generates to the slave device when starting a serial transfer. When the device is used as a slave, start conditions can be detected.

Figure 15-15. Start Conditions



A start condition is output when bit 1 (STT) of IICA control register 0 (IICCTL0) is set (1) after a stop condition has been detected (SPD: Bit 0 of the IICA status register (IICS) = 1). When a start condition is detected, bit 1 (STD) of the IICS register is set (1).

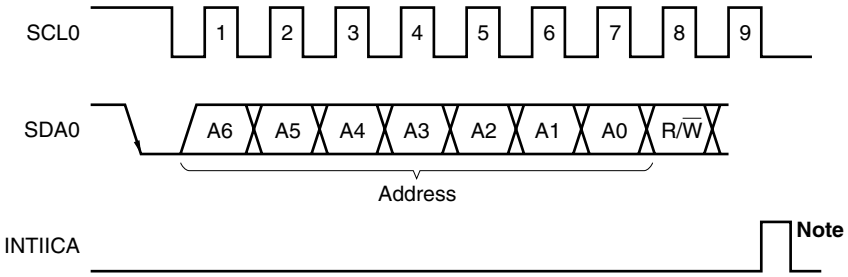
15.5.2 Addresses

The address is defined by the 7 bits of data that follow the start condition.

An address is a 7-bit data segment that is output in order to select one of the slave devices that are connected to the master device via the bus lines. Therefore, each slave device connected via the bus lines must have a unique address.

The slave devices include hardware that detects the start condition and checks whether or not the 7-bit address data matches the data values stored in the slave address register (SVA). If the address data matches the SVA register values, the slave device is selected and communicates with the master device until the master device generates a start condition or stop condition.

Figure 15-16. Address



Note INTIICA is not issued if data other than a local address or extension code is received during slave device operation.

Addresses are output when a total of 8 bits consisting of the slave address and the transfer direction described in **15.5.3 Transfer direction specification** are written to the IICA shift register (IICA). The received addresses are written to the IICA register.

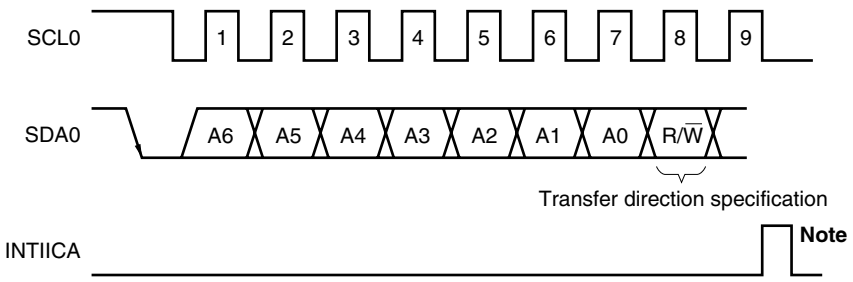
The slave address is assigned to the higher 7 bits of the IICA register.

15.5.3 Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction.

When this transfer direction specification bit has a value of “0”, it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of “1”, it indicates that the master device is receiving data from a slave device.

Figure 15-17. Transfer Direction Specification



Note INTIICA is not issued if data other than a local address or extension code is received during slave device operation.

15.5.4 Acknowledge ($\overline{ACK}$)

$\overline{ACK}$ is used to check the status of serial data at the transmission and reception sides.

The reception side returns $\overline{ACK}$ each time it has received 8-bit data.

The transmission side usually receives $\overline{ACK}$ after transmitting 8-bit data. When $\overline{ACK}$ is returned from the reception side, it is assumed that reception has been correctly performed and processing is continued. Whether $\overline{ACK}$ has been detected can be checked by using bit 2 (ACKD) of the IICA status register (IICS).

When the master receives the last data item, it does not return $\overline{ACK}$ and instead generates a stop condition. If a slave does not return $\overline{ACK}$ after receiving data, the master outputs a stop condition or restart condition and stops transmission. If $\overline{ACK}$ is not returned, the possible causes are as follows.

<1> Reception was not performed normally.
<2> The final data item was received.
<3> The reception side specified by the address does not exist.

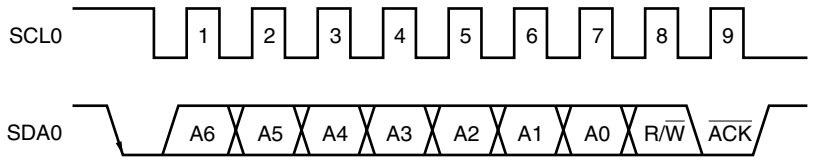
To generate $\overline{ACK}$, the reception side makes the SDA0 line low at the ninth clock (indicating normal reception).

Automatic generation of $\overline{ACK}$ is enabled by setting bit 2 (ACKE) of IICA control register 0 (IICCTL0) to 1. Bit 3 (TRC) of the IICS register is set by the data of the eighth bit that follows 7-bit address information. Usually, set the ACKE bit to 1 for reception (TRC = 0).

If a slave can receive no more data during reception (TRC = 0) or does not require the next data item, then the slave must inform the master, by clearing the ACKE bit to 0, that it will not receive any more data.

When the master does not require the next data item during reception (TRC = 0), it must clear the ACKE bit to 0 so that $\overline{ACK}$ is not generated. In this way, the master informs a slave at the transmission side that it does not require any more data (transmission will be stopped).

Figure 15-18. $\overline{ACK}$



When the local address is received, $\overline{ACK}$ is automatically generated, regardless of the value of the ACKE bit. When an address other than that of the local address is received, $\overline{ACK}$ is not generated (NACK).

When an extension code is received, $\overline{ACK}$ is generated if the ACKE bit is set to 1 in advance.

How $\overline{ACK}$ is generated when data is received differs as follows depending on the setting of the wait timing.

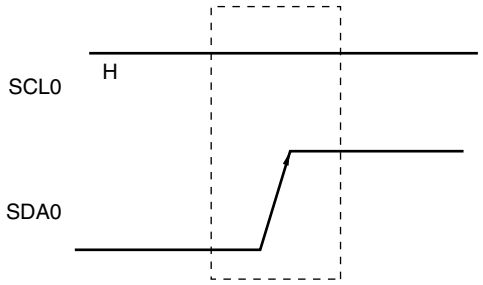
- When 8-clock wait state is selected (bit 3 (WTIM) of IICCTL0 register = 0):
  By setting the ACKE bit to 1 before releasing the wait state, $\overline{ACK}$ is generated at the falling edge of the eighth clock of the SCL0 pin.
- When 9-clock wait state is selected (bit 3 (WTIM) of IICCTL0 register = 1):
  $\overline{ACK}$ is generated by setting the ACKE bit to 1 in advance.

15.5.5 Stop condition

When the SCL0 pin is at high level, changing the SDA0 pin from low level to high level generates a stop condition.

A stop condition is a signal that the master device generates to the slave device when serial transfer has been completed. When the device is used as a slave, stop conditions can be detected.

Figure 15-19. Stop Condition



A stop condition is generated when bit 0 (SPT) of IICA control register 0 (IICCTL0) is set to 1. When the stop condition is detected, bit 0 (SPD) of the IICA status register (IICS) is set to 1 and INTIICA is generated when bit 4 (SPIE) of the IICCTL0 register is set to 1.

15.5.6 Wait

The wait is used to notify the communication partner that a device (master or slave) is preparing to transmit or receive data (i.e., is in a wait state).

Setting the SCL0 pin to low level notifies the communication partner of the wait state. When wait state has been canceled for both the master and slave devices, the next data transfer can begin.

Figure 15-20. Wait (1/2)

(1) When master device has a nine-clock wait and slave device has an eight-clock wait (master transmits, slave receives, and ACKE = 1)

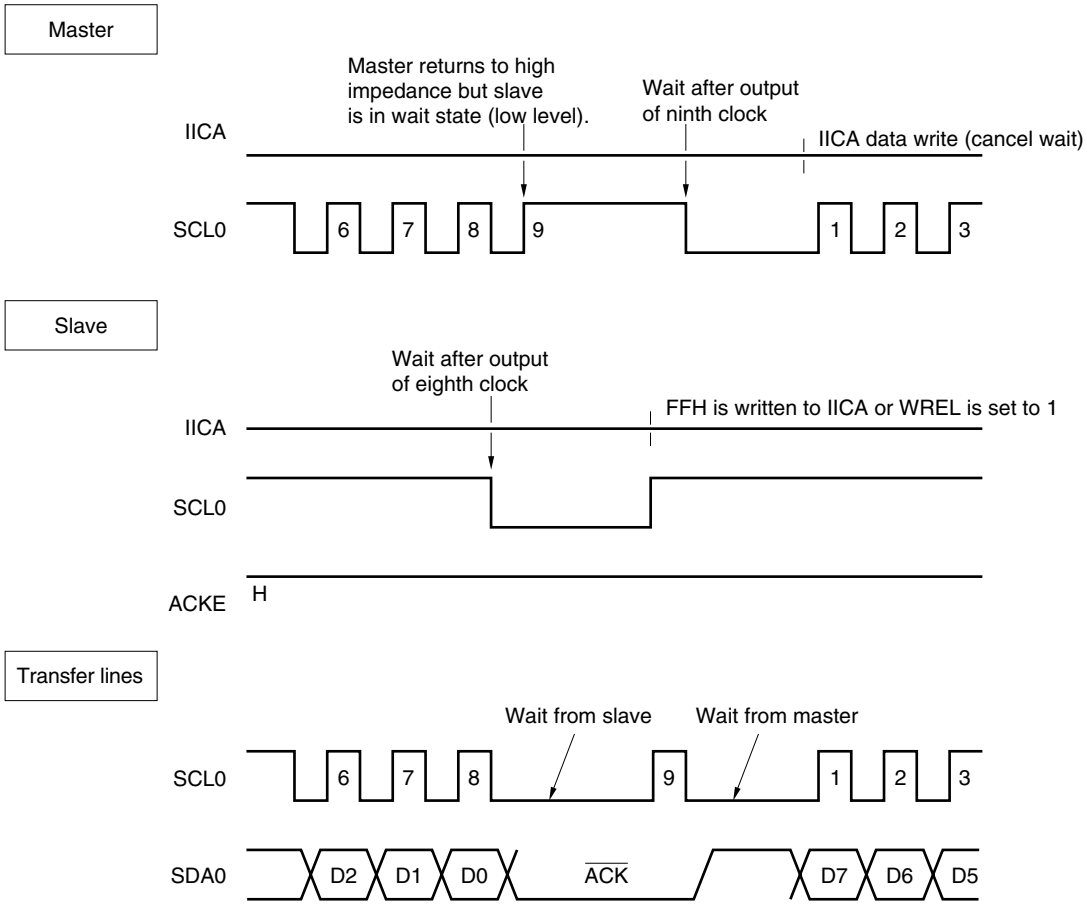
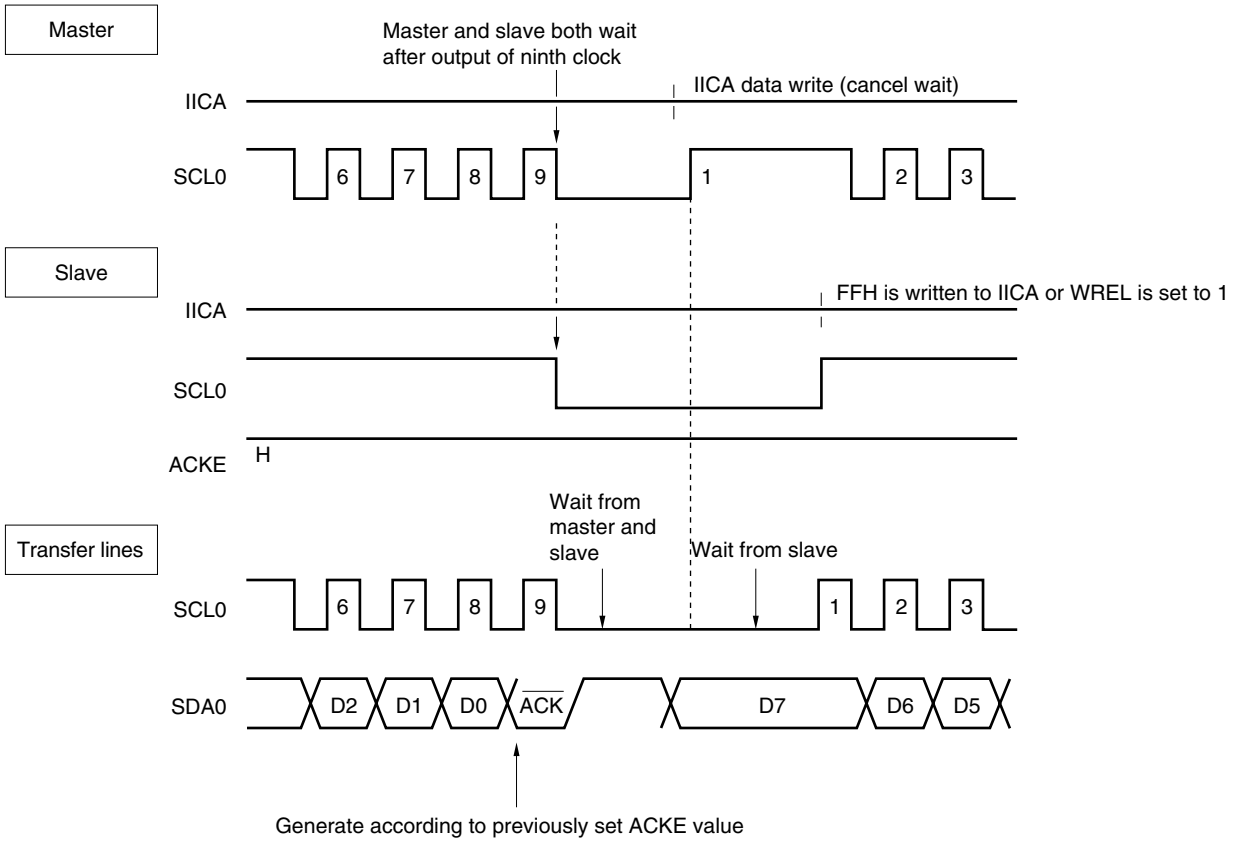


Figure 15-20. Wait (2/2)

(2) When master and slave devices both have a nine-clock wait (master transmits, slave receives, and ACKE = 1)



Remark ACKE: Bit 2 of IICA control register 0 (IICCTL0)
WREL: Bit 5 of IICA control register 0 (IICCTL0)

A wait may be automatically generated depending on the setting of bit 3 (WTIM) of IICA control register 0 (IICCTL0).

Normally, the receiving side cancels the wait state when bit 5 (WREL) of the IICCTL0 register is set to 1 or when FFH is written to the IICA shift register (IICA), and the transmitting side cancels the wait state when data is written to the IICA register.

The master device can also cancel the wait state via either of the following methods.

- By setting bit 1 (STT) of the IICCTL0 register to 1
- By setting bit 0 (SPT) of the IICCTL0 register to 1

15.5.7 Canceling wait

The I^2C usually cancels a wait state by the following processing.

- Writing data to the IICA shift register (IICA)
- Setting bit 5 (WREL) of IICA control register 0 (IICCTL0) (canceling wait)
- Setting bit 1 (STT) of the IICCTL0 register (generating start condition)[Note]
- Setting bit 0 (SPT) of the IICCTL0 register (generating stop condition)[Note]

Note Master only

When the above wait canceling processing is executed, the I^2C cancels the wait state and communication is resumed.

To cancel a wait state and transmit data (including addresses), write the data to the IICA register.

To receive data after canceling a wait state, or to complete data transmission, set bit 5 (WREL) of the IICCTL0 register to 1.

To generate a restart condition after canceling a wait state, set bit 1 (STT) of the IICCTL0 register to 1.

To generate a stop condition after canceling a wait state, set bit 0 (SPT) of the IICCTL0 register to 1.

Execute the canceling processing only once for one wait state.

If, for example, data is written to the IICA register after canceling a wait state by setting the WREL bit to 1, an incorrect value may be output to SDA0 line because the timing for changing the SDA0 line conflicts with the timing for writing the IICA register.

In addition to the above, communication is stopped if the IICE bit is cleared to 0 when communication has been aborted, so that the wait state can be canceled.

If the I^2C bus has deadlocked due to noise, processing is saved from communication by setting bit 6 (LREL) of the IICCTL0 register, so that the wait state can be canceled.

Caution If a processing to cancel a wait state is executed when WUP = 1, the wait state will not be canceled.

15.5.8 Interrupt request (INTIICA) generation timing and wait control

The setting of bit 3 (WTIM) of IICA control register 0 (IICCTL0) determines the timing by which INTIICA is generated and the corresponding wait control, as shown in Table 15-2.

Table 15-2. INTIICA Generation Timing and Wait Control

WTIM	During Slave Device Operation			During Master Device Operation		
	Address	Data Reception	Data Transmission	Address	Data Reception	Data Transmission
0	9 Notes 1, 2	8 Note 2	8 Note 2	9	8	8
1	9 Notes 1, 2	9 Note 2	9 Note 2	9	9	9

Notes 1. The slave device's INTIICA signal and wait period occurs at the falling edge of the ninth clock only when there is a match with the address set to the slave address register (SVA).
At this point, $\overline{ACK}$ is generated regardless of the value set to the IICCTL0 register's bit 2 (ACKE). For a slave device that has received an extension code, INTIICA occurs at the falling edge of the eighth clock.
However, if the address does not match after restart, INTIICA is generated at the falling edge of the 9th clock, but wait does not occur.

2. If the received address does not match the contents of the slave address register (SVA) and extension code is not received, neither INTIICA nor a wait occurs.

Remark The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and wait control are both synchronized with the falling edge of these clock signals.

(1) During address transmission/reception

- Slave device operation: Interrupt and wait timing are determined depending on the conditions described in Notes 1 and 2 above, regardless of the WTIM bit.
- Master device operation: Interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIM bit.

(2) During data reception

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM bit.

(3) During data transmission

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM bit.

(4) Wait cancellation method

The four wait cancellation methods are as follows.

- Writing data to the IICA shift register (IICA)
- Setting bit 5 (WREL) of IICA control register 0 (IICCTL0) (canceling wait)
- Setting bit 1 (STT) of IICCTL0 register (generating start condition)Note
- Setting bit 0 (SPT) of IICCTL0 register (generating stop condition)Note

Note Master only.

When an 8-clock wait has been selected (WTIM = 0), the presence/absence of $\overline{ACK}$ generation must be determined prior to wait cancellation.

(5) Stop condition detection

INTIICA is generated when a stop condition is detected (only when SPIE = 1).

15.5.9 Address match detection method

In I^2C bus mode, the master device can select a particular slave device by transmitting the corresponding slave address.

Address match can be detected automatically by hardware. An interrupt request (INTIICA) occurs when the address set to the slave address register (SVA) matches the slave address sent by the master device, or when an extension code has been received.

15.5.10 Error detection

In I^2C bus mode, the status of the serial data bus (SDA0) during data transmission is captured by the IICA shift register (IICA) of the transmitting device, so the IICA data prior to transmission can be compared with the transmitted IICA data to enable detection of transmission errors. A transmission error is judged as having occurred when the compared data values do not match.

15.5.11 Extension code

(1) When the higher 4 bits of the receive address are either “0000” or “1111”, the extension code reception flag (EXC) is set to 1 for extension code reception and an interrupt request (INTIICA) is issued at the falling edge of the eighth clock. The local address stored in the slave address register (SVA) is not affected.

(2) The settings below are specified if 11110xx0 is transferred from the master by using a 10-bit address transfer when the SVA register is set to 11110xx0. Note that INTIICA occurs at the falling edge of the eighth clock.

- Higher four bits of data match: EXC = 1
- Seven bits of data match: COI = 1

Remark EXC: Bit 5 of IICA status register (IICS)
COI: Bit 4 of IICA status register (IICS)

(3) Since the processing after the interrupt request occurs differs according to the data that follows the extension code, such processing is performed by software.
If the extension code is received while a slave device is operating, then the slave device is participating in communication even if its address does not match.
For example, after the extension code is received, if you do not wish to operate the target device as a slave device, set bit 6 (LREL) of IICA control register 0 (IICCTL0) to 1 to set the standby mode for the next communication operation.

Table 15-3. Bit Definitions of Major Extension Codes

Slave Address	R/W Bit	Description
0 0 0 0 0 0 0	0	General call address
1 1 1 1 0 x x	0	10-bit slave address specification (during address authentication)
1 1 1 1 0 x x	1	10-bit slave address specification (after address match, when read command is issued)

Remark See the I^2C bus specifications issued by NXP Semiconductors for details of extension codes other than those described above.

15.5.12 Arbitration

When several master devices simultaneously generate a start condition (when the STT bit is set to 1 before the STD bit is set to 1), communication among the master devices is performed as the number of clocks are adjusted until the data differs. This kind of operation is called arbitration.

When one of the master devices loses in arbitration, an arbitration loss flag (ALD) in the IICA status register (IICS) is set (1) via the timing by which the arbitration loss occurred, and the SCL0 and SDA0 lines are both set to high impedance, which releases the bus.

The arbitration loss is detected based on the timing of the next interrupt request (the eighth or ninth clock, when a stop condition is detected, etc.) and the ALD = 1 setting that has been made by software.

For details of interrupt request timing, see **15.5.8 Interrupt request (INTIICA) generation timing and wait control**.

Remark STD: Bit 1 of IICA status register (IICS)
STT: Bit 1 of IICA control register 0 (IICCTL0)

Figure 15-21. Arbitration Timing Example

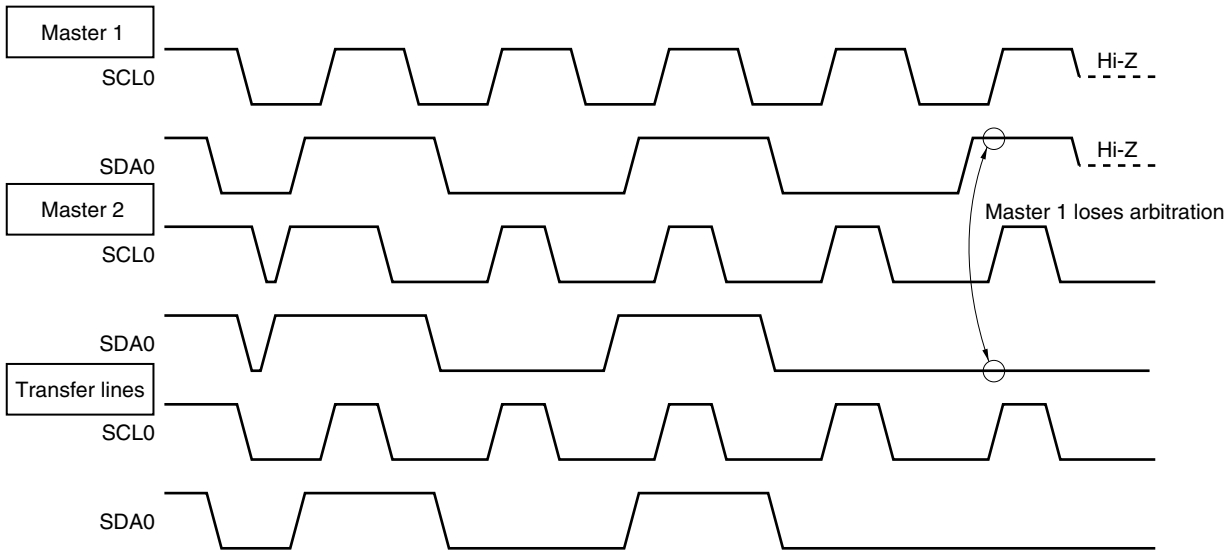


Table 15-4. Status During Arbitration and Interrupt Request Generation Timing

Status During Arbitration	Interrupt Request Generation Timing
During address transmission	At falling edge of eighth or ninth clock following byte transfer[Note 1]
Read/write data after address transmission	
During extension code transmission	
Read/write data after extension code transmission	
During data transmission	
During $\overline{\text{ACK}}$ transfer period after data transmission	
When restart condition is detected during data transfer	
When stop condition is detected during data transfer	When stop condition is generated (when SPIE = 1)[Note 2]
When data is at low level while attempting to generate a restart condition	At falling edge of eighth or ninth clock following byte transfer[Note 1]
When stop condition is detected while attempting to generate a restart condition	When stop condition is generated (when SPIE = 1)[Note 2]
When data is at low level while attempting to generate a stop condition	At falling edge of eighth or ninth clock following byte transfer[Note 1]
When SCL0 is at low level while attempting to generate a restart condition	

Notes 1. When the WTIM bit (bit 3 of IICA control register 0 (IICCTL0)) = 1, an interrupt request occurs at the falling edge of the ninth clock. When WTIM = 0 and the extension code's slave address is received, an interrupt request occurs at the falling edge of the eighth clock.

2. When there is a chance that arbitration will occur, set SPIE = 1 for master device operation.

Remark SPIE: Bit 4 of IICA control register 0 (IICCTL0)

15.5.13 Wakeup function

The I^2C bus slave function is a function that generates an interrupt request signal (INTIICA) when a local address and extension code have been received.

This function makes processing more efficient by preventing unnecessary INTIICA signal from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has generated a start condition) to a slave device.

However, when a stop condition is detected, bit 4 (SPIE) of IICA control register 0 (IICCTL0) is set regardless of the wakeup function, and this determines whether interrupt requests are enabled or disabled.

To use the wakeup function in the STOP mode, set the WUP bit to 1. Addresses can be received regardless of the operation clock. An interrupt request signal (INTIICA) is also generated when a local address and extension code have been received. Operation returns to normal operation by using an instruction to clear (0) the WUP bit after this interrupt has been generated.

Figure 15-22 shows the flow for setting WUP = 1 and Figure 15-23 shows the flow for setting WUP = 0 upon an address match.

Figure 15-22. Flow When Setting WUP = 1

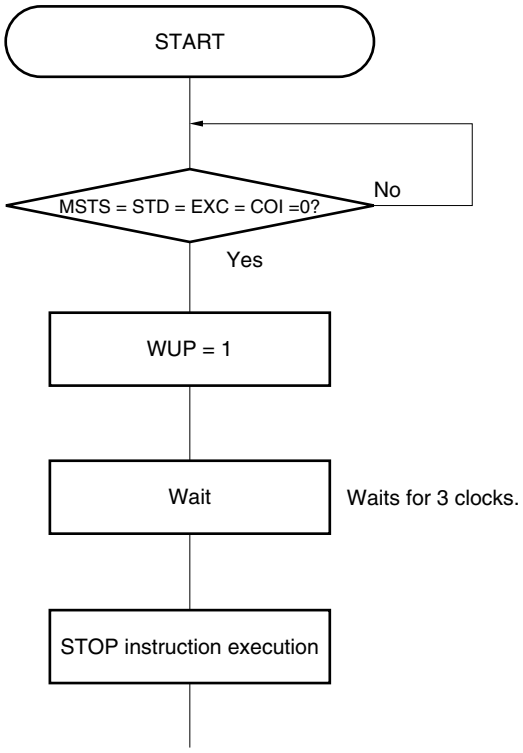
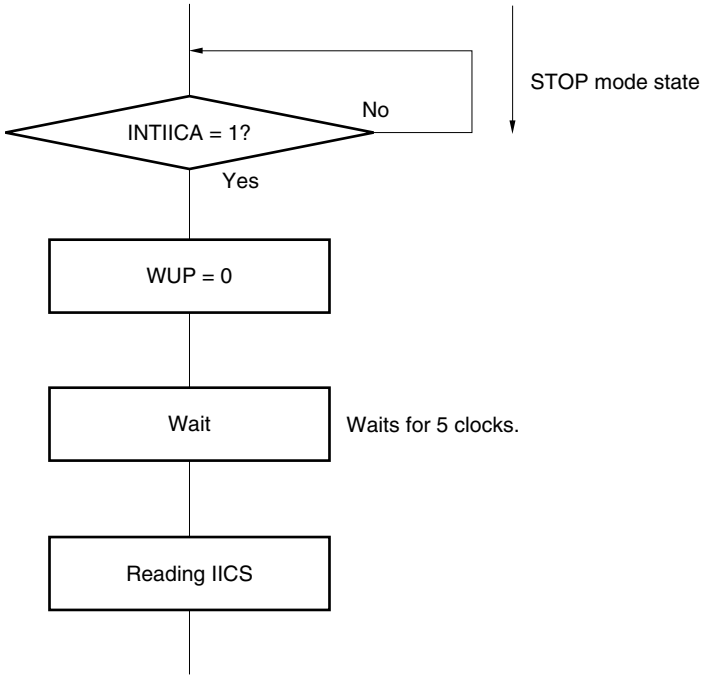


Figure 15-23. Flow When Setting WUP = 0 upon Address Match (Including Extension Code Reception)

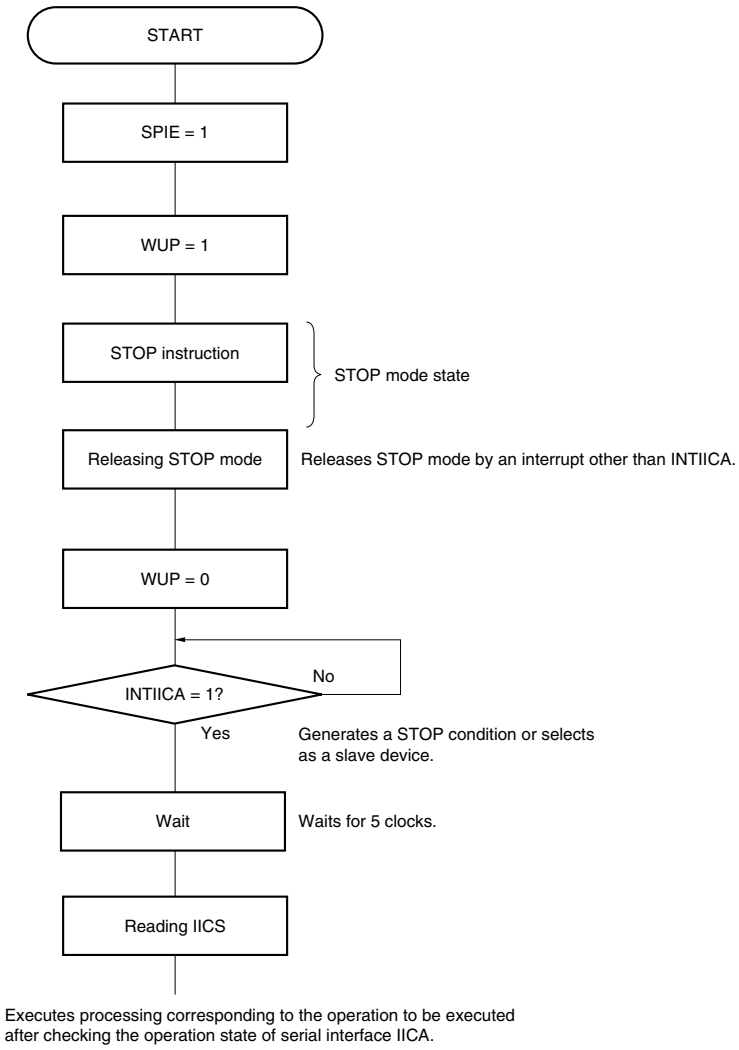


Executes processing corresponding to the operation to be executed after checking the operation state of serial interface IICA.

Use the following flows to perform the processing to release the STOP mode other than by an interrupt request (INTIICA) generated from serial interface IICA.

- Master device operation: Flow shown in Figure 15-24
- Slave device operation: Same as the flow in Figure 15-23

Figure 15-24. When Operating as Master Device after Releasing STOP Mode other than by INTIICA



15.5.14 Communication reservation

(1) When communication reservation function is enabled (bit 0 (IICRSV) of IICA flag register (IICF) = 0)

To start master device communications when not currently using a bus, a communication reservation can be made to enable transmission of a start condition when the bus is released. There are two modes under which the bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ is not returned and the bus was released by setting bit 6 (LREL) of IICA control register 0 (IICCTL0) to 1 and saving communication).

If bit 1 (STT) of the IICCTL0 register is set to 1 while the bus is not used (after a stop condition is detected), a start condition is automatically generated and wait state is set.
If an address is written to the IICA shift register (IICA) after bit 4 (SPIE) of the IICCTL0 register was set to 1, and it was detected by generation of an interrupt request signal (INTIICA) that the bus was released (detection of the stop condition), then the device automatically starts communication as the master. Data written to the IICA register before the stop condition is detected is invalid.
When the STT bit has been set to 1, the operation mode (as start condition or as communication reservation) is determined according to the bus status.

- If the bus has been released ..... a start condition is generated
- If the bus has not been released (standby mode)..... communication reservation

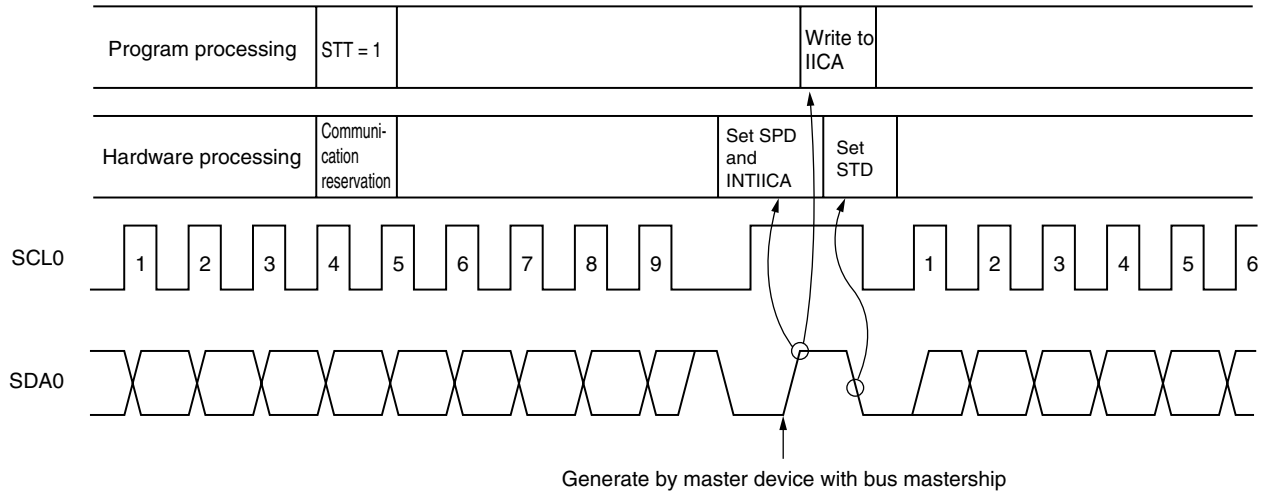
Check whether the communication reservation operates or not by using the MSTS bit (bit 7 of the IICA status register (IICS)) after the STT bit is set to 1 and the wait time elapses.
Use software to secure the wait time calculated by the following expression.

Wait time from setting STT = 1 to checking the MSTS flag: (IICWL setting value + IICWH setting value + 4) + $t_F \times 2 \times f_{CLK}$ [clocks]

Remark IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDA0 and SCL0 signal falling times
f_{CLK}: CPU/peripheral hardware clock frequency

Figure 15-25 shows the communication reservation timing.

Figure 15-25. Communication Reservation Timing



Remark IICA: IICA shift register
STT: Bit 1 of IICA control register 0 (IICCTL0)
STD: Bit 1 of IICA status register (IICS)
SPD: Bit 0 of IICA status register (IICS)

Communication reservations are accepted via the timing shown in Figure 15-26. After bit 1 (STD) of the IICA status register (IICS) is set to 1, a communication reservation can be made by setting bit 1 (STT) of IICA control register 0 (IICCTL0) to 1 before a stop condition is detected.

Figure 15-26. Timing for Accepting Communication Reservations

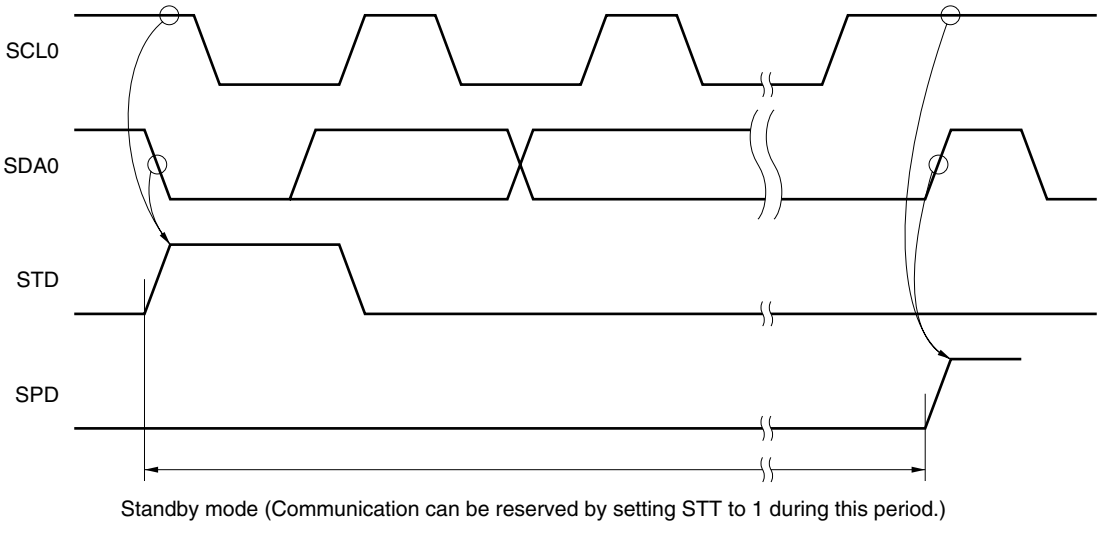
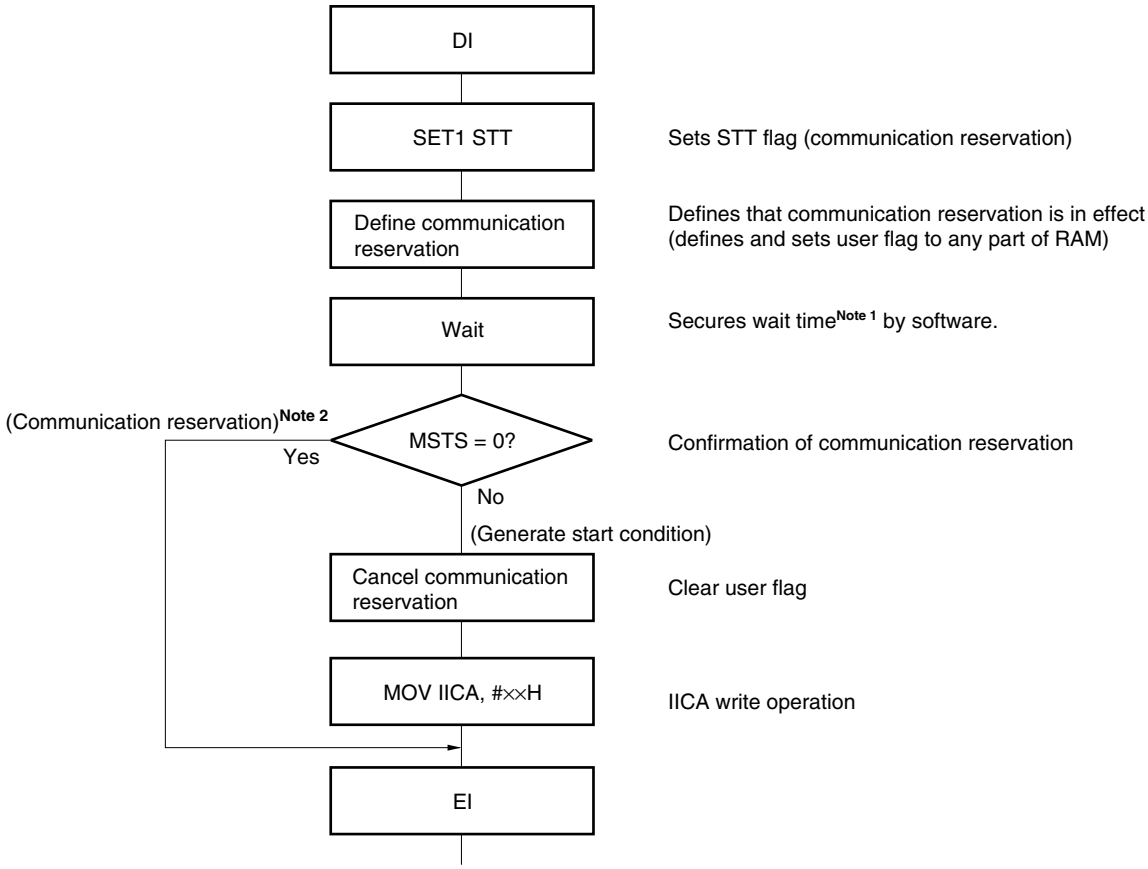


Figure 15-27 shows the communication reservation protocol.

Figure 15-27. Communication Reservation Protocol



Notes 1. The wait time is calculated as follows.
(IICWL setting value + IICWH setting value + 4) + $t_F \times 2 \times f_{CLK}$ [clocks]

2. The communication reservation operation executes a write to the IICA shift register (IICA) when a stop condition interrupt request occurs.

Remark STT: Bit 1 of IICA control register 0 (IICCTL0)
MSTS: Bit 7 of IICA status register (IICS)
IICA: IICA shift register
IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDA0 and SCL0 signal falling times
f_{CLK}: CPU/peripheral hardware clock frequency

(2) When communication reservation function is disabled (bit 0 (IICRSV) of IICA flag register (IICF) = 1)

When bit 1 (STT) of IICA control register 0 (IICCTL0) is set to 1 when the bus is not used in a communication during bus communication, this request is rejected and a start condition is not generated. The following two statuses are included in the status where bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ is not returned and the bus was released by setting bit 6 (LREL) of the IICCTL0 register to 1 and saving communication)

To confirm whether the start condition was generated or request was rejected, check STCF (bit 7 of the IICF register). It takes up to 5 clocks until the STCF bit is set to 1 after setting STT = 1. Therefore, secure the time by software.

15.5.15 Cautions

(1) When STCEN = 0

Immediately after I^2C operation is enabled (IICE = 1), the bus communication status (IICBSY = 1) is recognized regardless of the actual bus status. When changing from a mode in which no stop condition has been detected to a master device communication mode, first generate a stop condition to release the bus, then perform master device communication.

When using multiple masters, it is not possible to perform master device communication when the bus has not been released (when a stop condition has not been detected).

Use the following sequence for generating a stop condition.

<1> Set IICA control register 1 (IICCTL1).
<2> Set bit 7 (IICE) of IICA control register 0 (IICCTL0) to 1.
<3> Set bit 0 (SPT) of the IICCTL0 register to 1.

(2) When STCEN = 1

Immediately after I^2C operation is enabled (IICE = 1), the bus released status (IICBSY = 0) is recognized regardless of the actual bus status. To generate the first start condition (STT = 1), it is necessary to confirm that the bus has been released, so as to not disturb other communications.

(3) If other I^2C communications are already in progress

If I^2C operation is enabled and the device participates in communication already in progress when the SDA0 pin is low and the SCL0 pin is high, the macro of I^2C recognizes that the SDA0 pin has gone low (detects a start condition). If the value on the bus at this time can be recognized as an extension code, $\overline{ACK}$ is returned, but this interferes with other I^2C communications. To avoid this, start I^2C in the following sequence.

<1> Clear bit 4 (SPIE) of the IICCTL0 register to 0 to disable generation of an interrupt request signal (INTIICA) when the stop condition is detected.
<2> Set bit 7 (IICE) of the IICCTL0 register to 1 to enable the operation of I^2C.
<3> Wait for detection of the start condition.
<4> Set bit 6 (LREL) of the IICCTL0 register to 1 before $\overline{ACK}$ is returned (4 to 80 clocks after setting the IICE bit to 1), to forcibly disable detection.

(4) Setting the STT and SPT bits (bits 1 and 0 of the IICCTL0 register) again after they are set and before they are cleared to 0 is prohibited.

(5) When transmission is reserved, set the SPIE bit (bit 4 of the IICTL0 register) to 1 so that an interrupt request is generated when the stop condition is detected. Transfer is started when communication data is written to the IICA shift register (IICA) after the interrupt request is generated. Unless the interrupt is generated when the stop condition is detected, the device stops in the wait state because the interrupt request is not generated when communication is started. However, it is not necessary to set the SPIE bit to 1 when the MSTS bit (bit 7 of the IICA status register (IICS)) is detected by software.

15.5.16 Communication operations

The following shows three operation procedures with the flowchart.

(1) Master operation in single master system

The flowchart when using the 78K0R/Kx3-L as the master in a single master system is shown below.

This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

(2) Master operation in multimaster system

In the I^2C bus multimaster system, whether the bus is released or used cannot be judged by the I^2C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the 78K0R/Kx3-L takes part in a communication with bus released state.

This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the 78K0R/Kx3-L looses in arbitration and is specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

(3) Slave operation

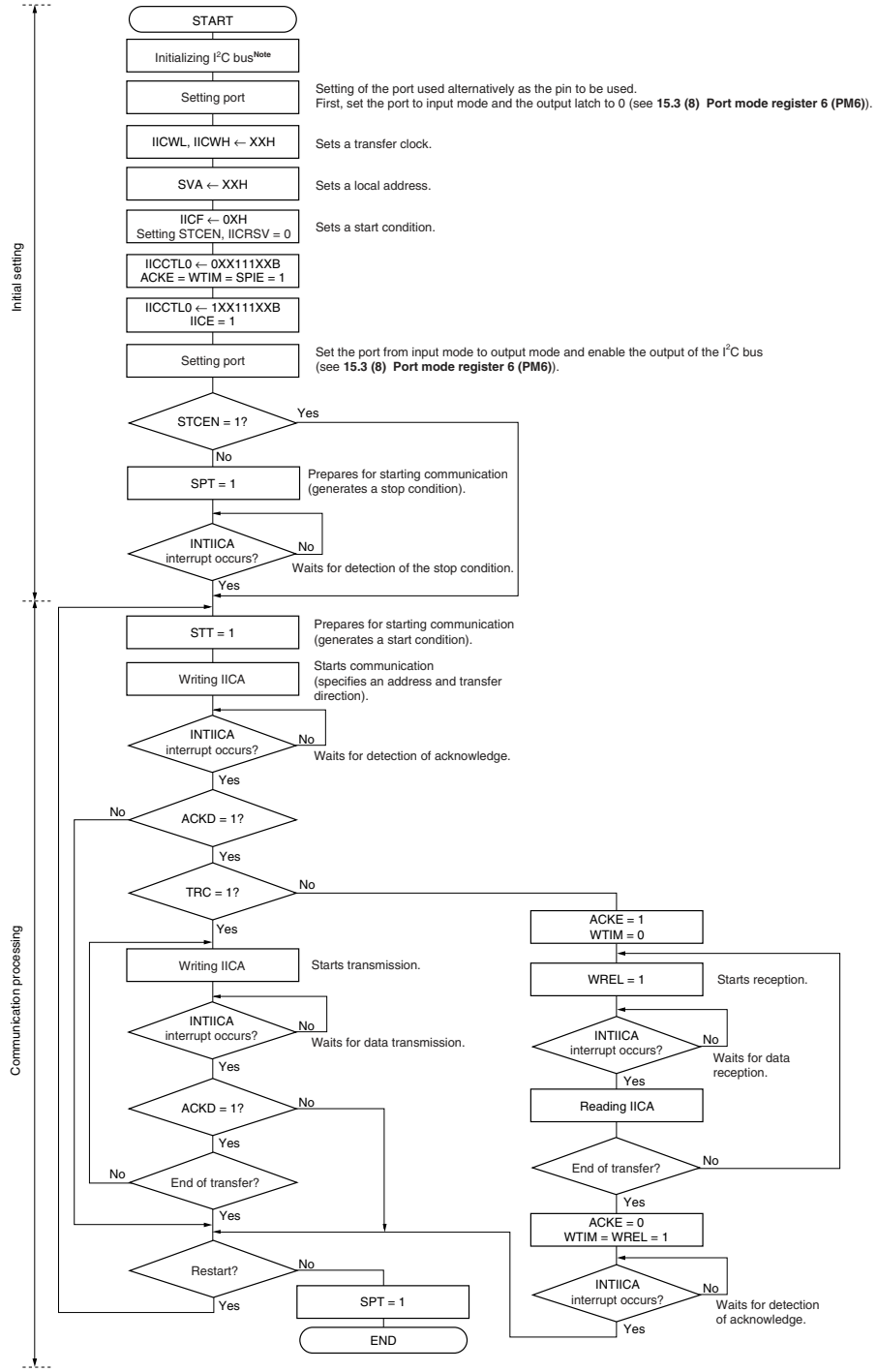
An example of when the 78K0R/Kx3-L is used as the I^2C bus slave is shown below.

When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIICA interrupt occurrence (communication waiting). When an INTIICA interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.

By checking the flags, necessary communication processing is performed.

(1) Master operation in single-master system

Figure 15-28. Master Operation in Single-Master System

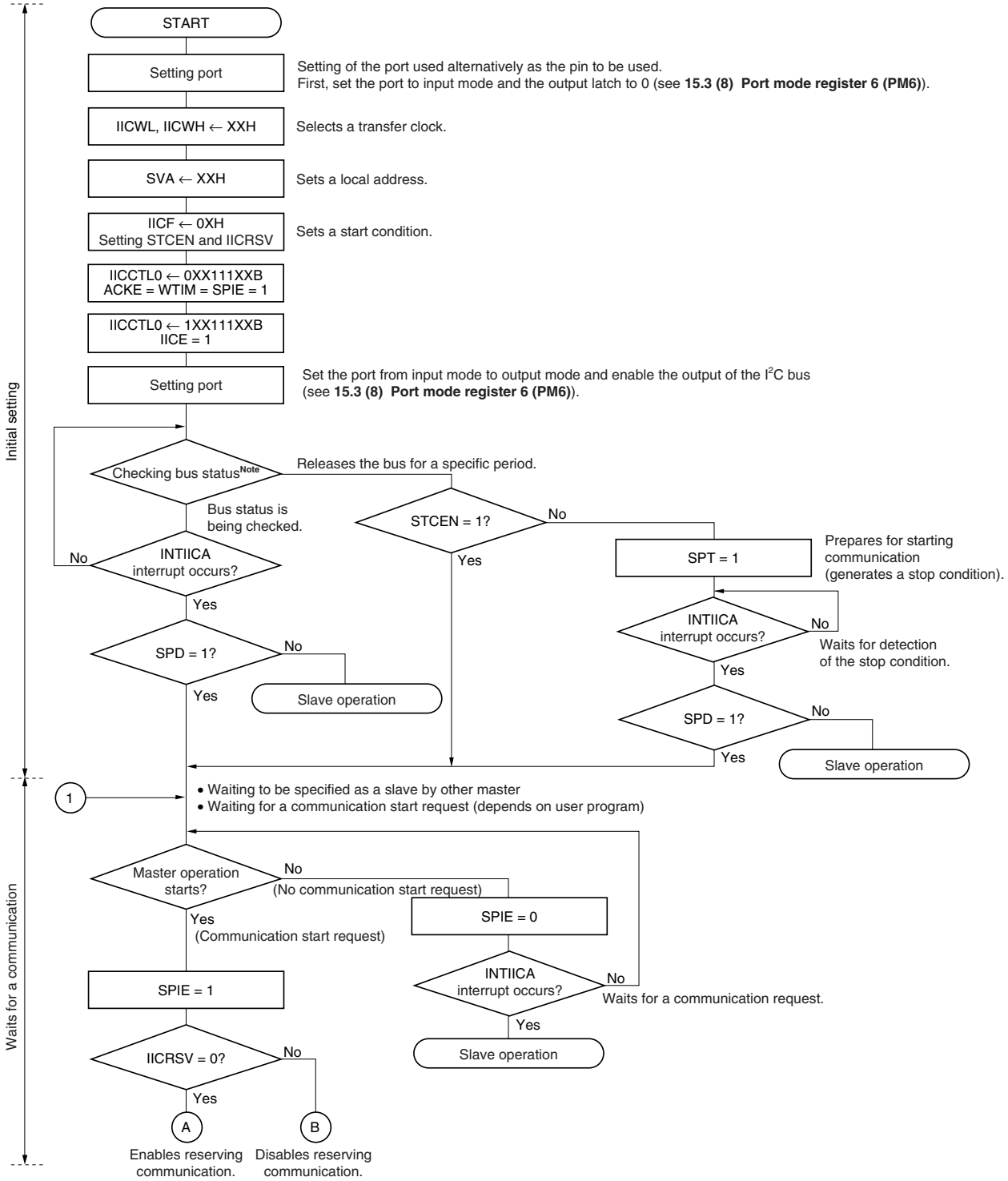


Note Release (SCL0 and SDA0 pins = high level) the I^2C bus in conformance with the specifications of the product that is communicating. If EEPROM is outputting a low level to the SDA0 pin, for example, set the SCL0 pin in the output port mode, and output a clock pulse from the output port until the SDA0 pin is constantly at high level.

Remark Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

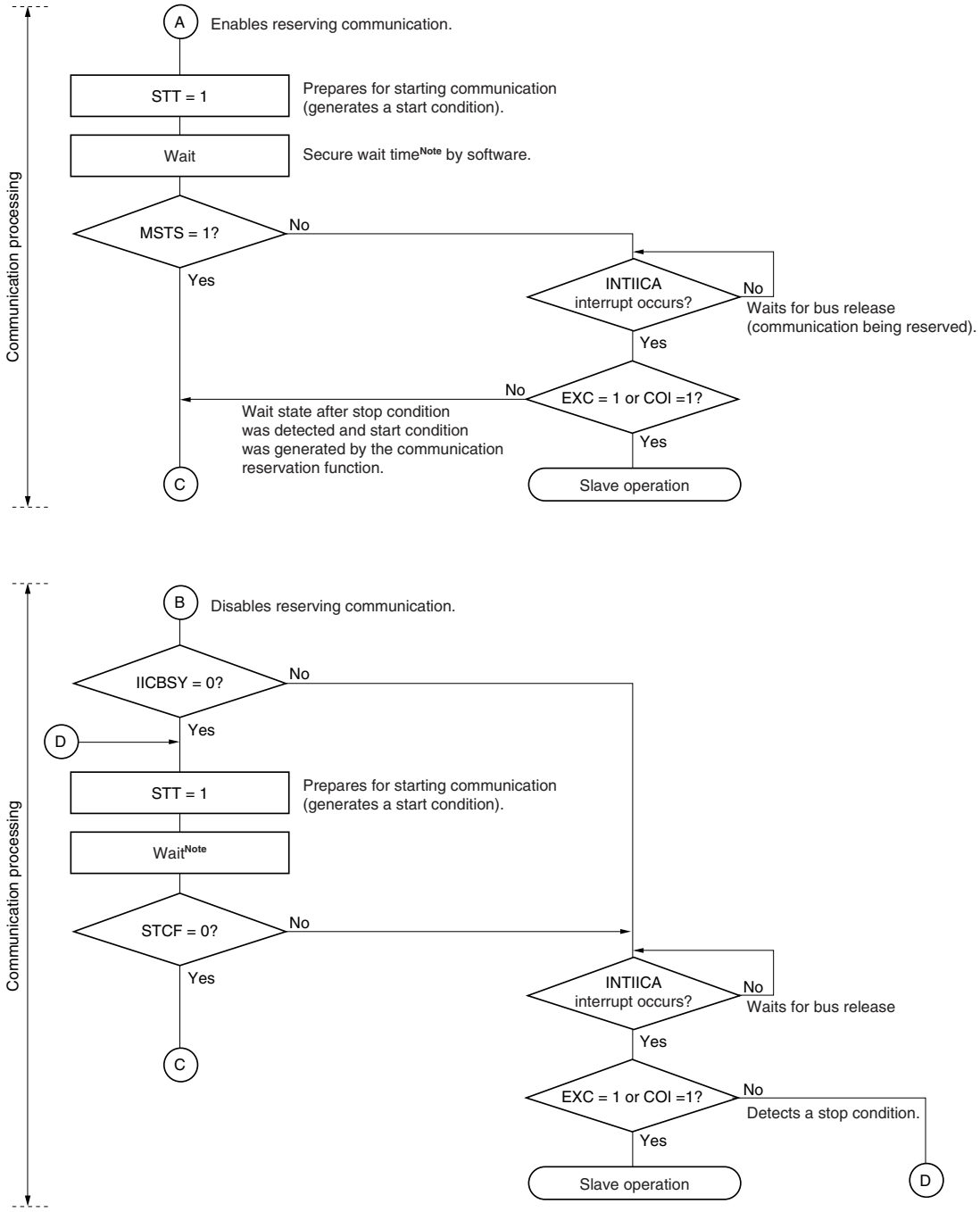
(2) Master operation in multi-master system

Figure 15-29. Master Operation in Multi-Master System (1/3)



Note Confirm that the bus is released (CLD bit = 1, DAD bit = 1) for a specific period (for example, for a period of one frame). If the SDA0 pin is constantly at low level, decide whether to release the I²C bus (SCL0 and SDA0 pins = high level) in conformance with the specifications of the product that is communicating.

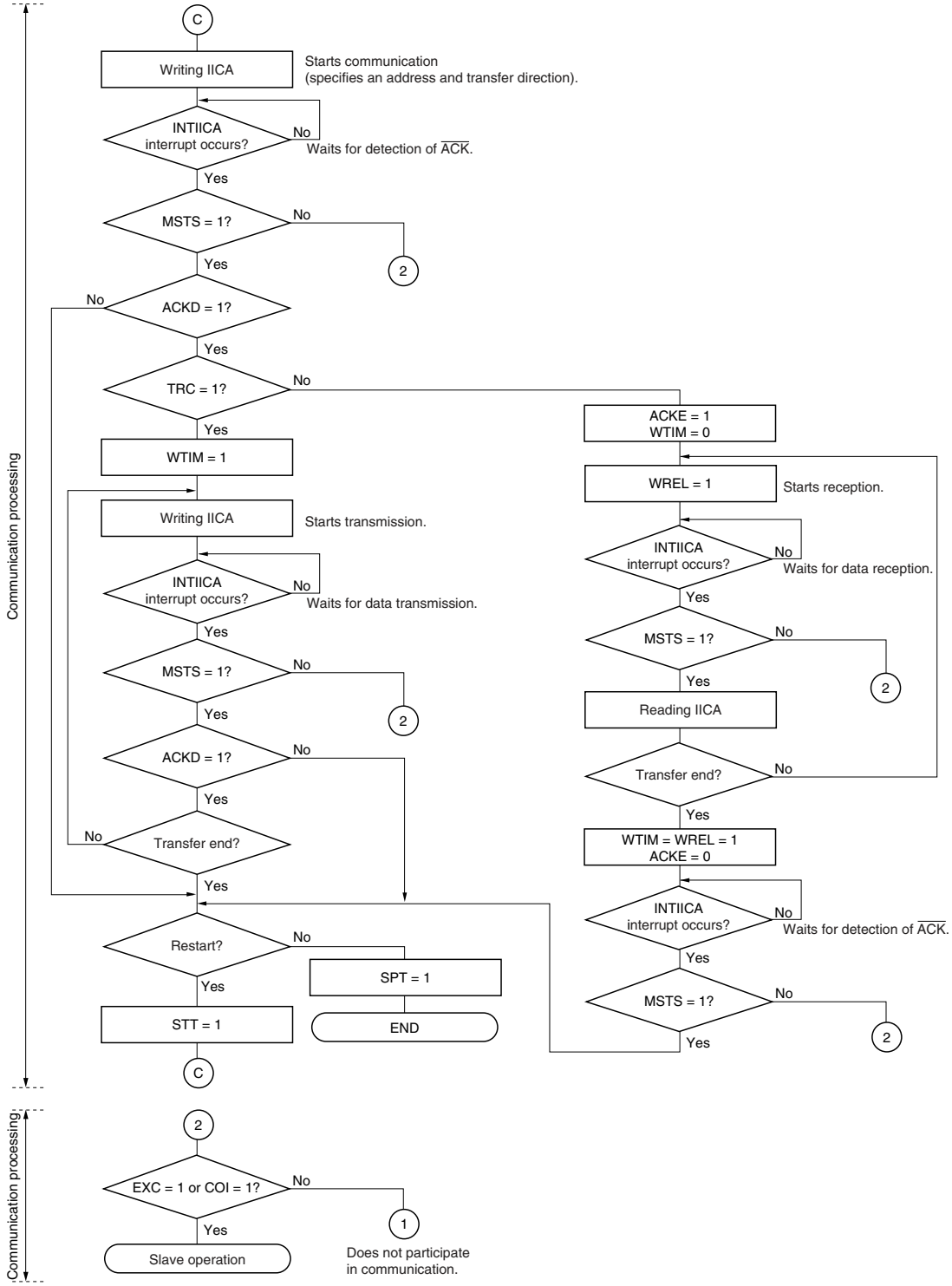
Figure 15-29. Master Operation in Multi-Master System (2/3)



Note The wait time is calculated as follows.
(IICWL setting value + IICWH setting value + 4 clocks) / f_{CLK} + $t_F \times 2$

Remark IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDA0 and SCL0 signal falling times
f_{CLK}: CPU/peripheral hardware clock frequency

Figure 15-29. Master Operation in Multi-Master System (3/3)



Remarks 1. Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

2. To use the device as a master in a multi-master system, read the MSTS bit each time interrupt INTIICA has occurred to check the arbitration result.

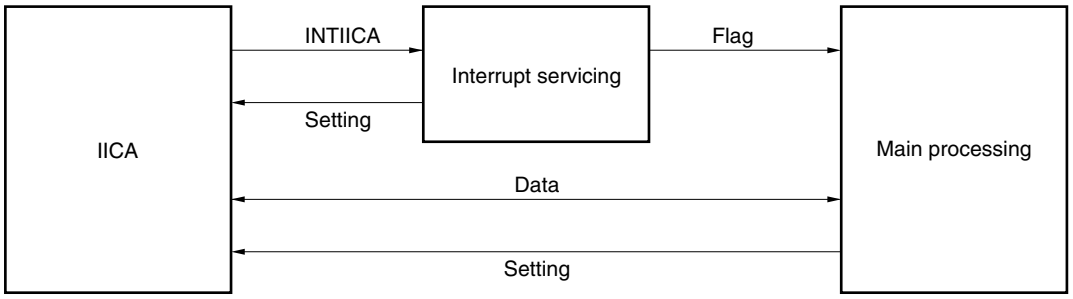
3. To use the device as a slave in a multi-master system, check the status by using the IICA status register (IICS) and IICA flag register (IICF) each time interrupt INTIICA has occurred, and determine the processing to be performed next.

(3) Slave operation

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIICA interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICA interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICA.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

<2> Ready flag

This flag indicates that data communication is enabled. Its function is the same as the INTIICA interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as the TRC bit.

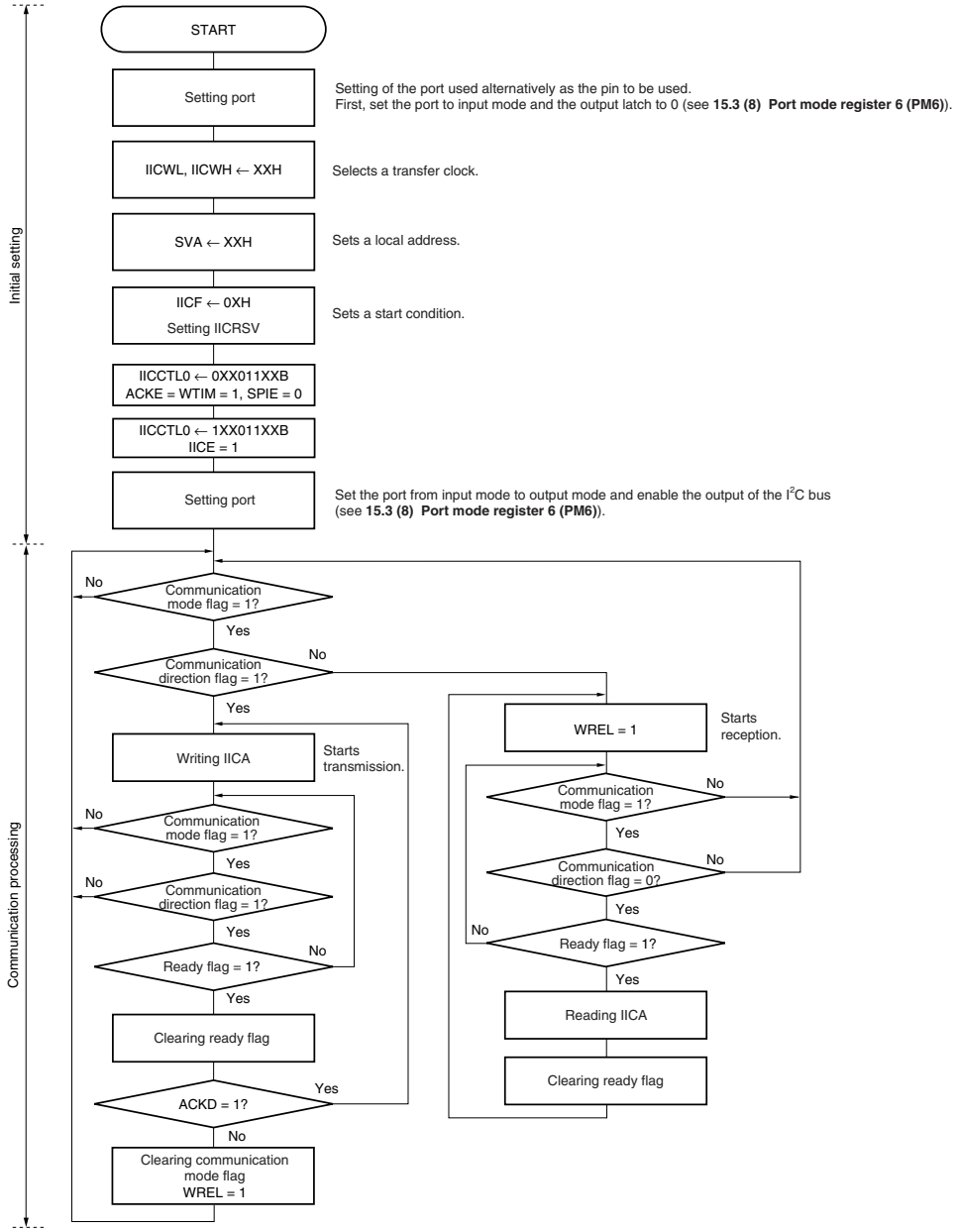
The main processing of the slave operation is explained next.

Start serial interface IICA and wait until communication is enabled. When communication is enabled, execute communication by using the communication mode flag and ready flag (processing of the stop condition and start condition is performed by an interrupt. Here, check the status by using the flags).

The transmission operation is repeated until the master no longer returns $\overline{ACK}$. If $\overline{ACK}$ is not returned from the master, communication is completed.

For reception, the necessary amount of data is received. When communication is completed, $\overline{ACK}$ is not returned as the next data. After that, the master generates a stop condition or restart condition. Exit from the communication status occurs in this way.

Figure 15-30. Slave Operation Flowchart (1)



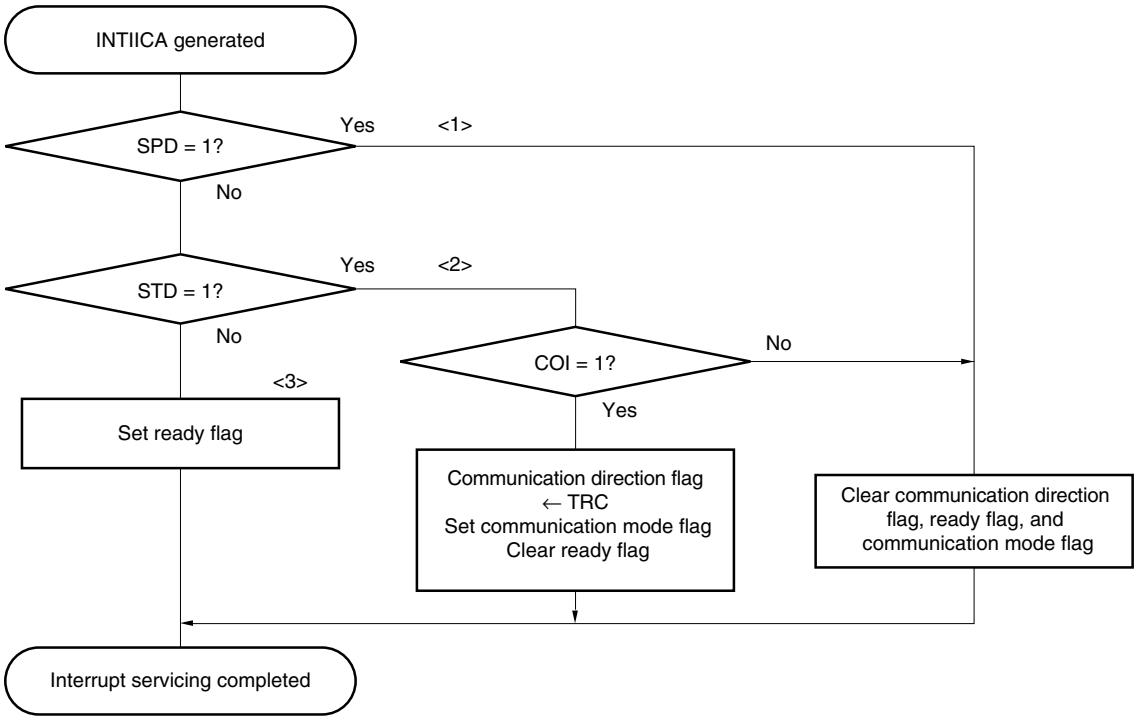
Remark Conform to the specifications of the product that is in communication, regarding the transmission and reception formats.

An example of the processing procedure of the slave with the INTIICA interrupt is explained below (processing is performed assuming that no extension code is used). The INTIICA interrupt checks the status, and the following operations are performed.

<1> Communication is stopped if the stop condition is issued.
<2> If the start condition is issued, the address is checked and communication is completed if the address does not match. If the address matches, the communication mode is set, wait is cancelled, and processing returns from the interrupt (the ready flag is cleared).
<3> For data transmit/receive, only the ready flag is set. Processing returns from the interrupt with the I^2C bus remaining in the wait state.

Remark <1> to <3> above correspond to <1> to <3> in Figure 15-31 Slave Operation Flowchart (2).

Figure 15-31. Slave Operation Flowchart (2)



15.5.17 Timing of I^2C interrupt request (INTIICA) occurrence

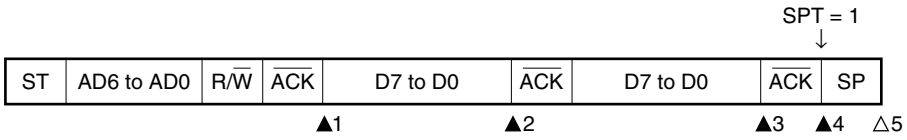
The timing of transmitting or receiving data and generation of interrupt request signal INTIICA, and the value of the IICA status register (IICS) when the INTIICA signal is generated are shown below.

Remark ST: Start condition
AD6 to AD0: Address
R/$\overline{W}$: Transfer direction specification
$\overline{ACK}$: Acknowledge
D7 to D0: Data
SP: Stop condition

(1) Master device operation

(a) Start ~ Address ~ Data ~ Data ~ Stop (transmission/reception)

(i) When WTIM = 0

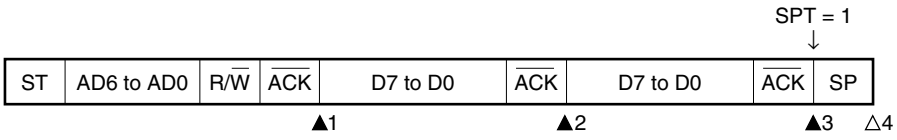


▲1: IICS = 1000×110B
▲2: IICS = 1000×000B
▲3: IICS = 1000×000B (Sets the WTIM bit to 1)[Note]
▲4: IICS = 1000××00B (Sets the SPT bit to 1)[Note]
△5: IICS = 00000001B

Note To generate a stop condition, set the WTIM bit to 1 and change the timing for generating the INTIICA interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1

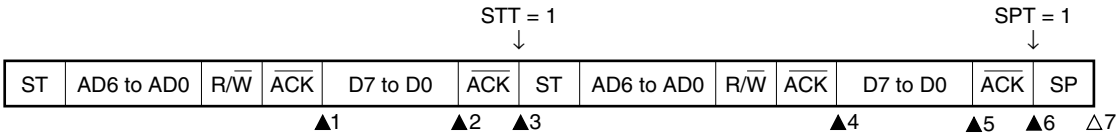


▲1: IICS = 1000×110B
▲2: IICS = 1000×100B
▲3: IICS = 1000××00B (Sets the SPT bit to 1)
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

(i) When WTIM = 0

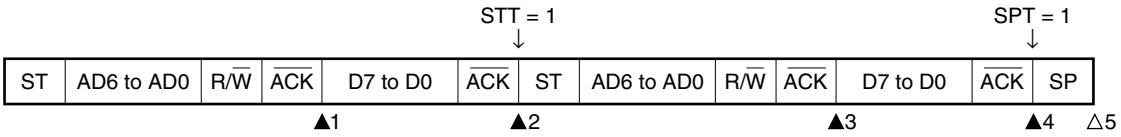


▲1: IICS = 1000×110B
▲2: IICS = 1000×000B (Sets the WTIM bit to 1)[Note 1]
▲3: IICS = 1000××00B (Clears the WTIM bit to 0[Note 2], sets the STT bit to 1)
▲4: IICS = 1000×110B
▲5: IICS = 1000×000B (Sets the WTIM bit to 1)[Note 3]
▲6: IICS = 1000××00B (Sets the SPT bit to 1)
△7: IICS = 00000001B

Notes 1. To generate a start condition, set the WTIM bit to 1 and change the timing for generating the INTIICA interrupt request signal.
2. Clear the WTIM bit to 0 to restore the original setting.
3. To generate a stop condition, set the WTIM bit to 1 and change the timing for generating the INTIICA interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1

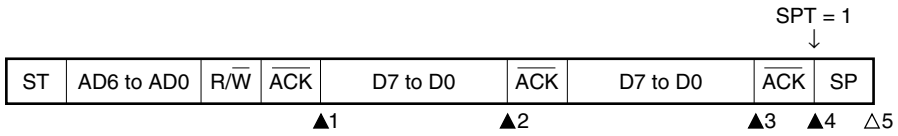


▲1: IICS = 1000×110B
▲2: IICS = 1000××00B (Sets the STT bit to 1)
▲3: IICS = 1000×110B
▲4: IICS = 1000××00B (Sets the SPT bit to 1)
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

(i) When WTIM = 0

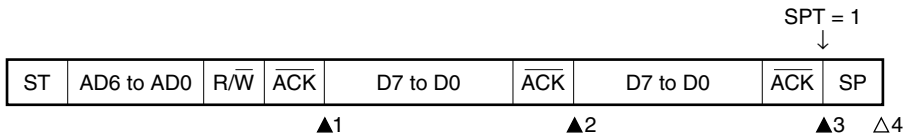


▲1: IICS = 1010×110B
▲2: IICS = 1010×000B
▲3: IICS = 1010×000B (Sets the WTIM bit to 1)[Note]
▲4: IICS = 1010××00B (Sets the SPT bit to 1)
△5: IICS = 00000001B

Note To generate a stop condition, set the WTIM bit to 1 and change the timing for generating the INTIICA interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1



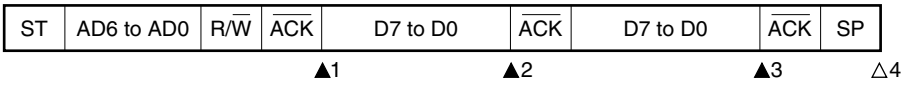
▲1: IICS = 1010×110B
▲2: IICS = 1010×100B
▲3: IICS = 1010××00B (Sets the SPT bit to 1)
△4: IICS = 00001001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(2) Slave device operation (slave address data reception)

(a) Start ~ Address ~ Data ~ Data ~ Stop

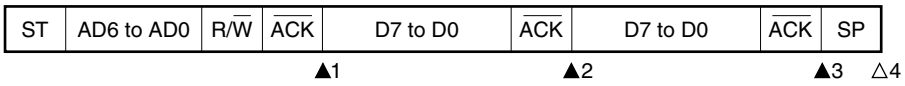
(i) When WTIM = 0



▲1: IICS = 0001×110B
▲2: IICS = 0001×000B
▲3: IICS = 0001×000B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1

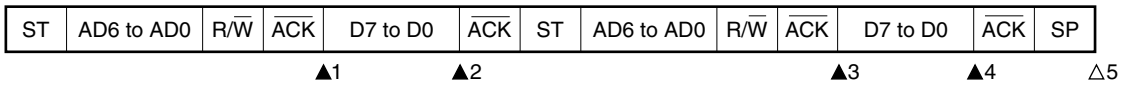


▲1: IICS = 0001×110B
▲2: IICS = 0001×100B
▲3: IICS = 0001××00B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

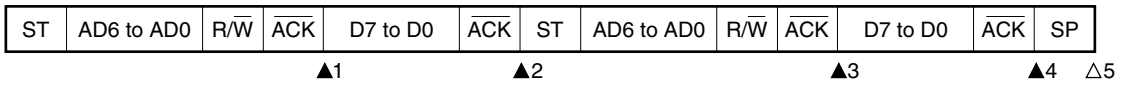
(i) When WTIM = 0 (after restart, matches with SVA)



▲1: IICS = 0001×110B
▲2: IICS = 0001×000B
▲3: IICS = 0001×110B
▲4: IICS = 0001×000B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, matches with SVA)

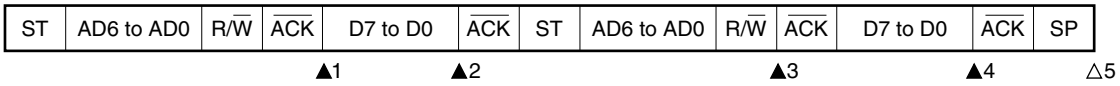


▲1: IICS = 0001×110B
▲2: IICS = 0001××00B
▲3: IICS = 0001×110B
▲4: IICS = 0001××00B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(c) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

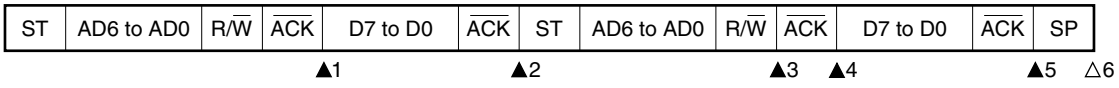
(i) When WTIM = 0 (after restart, does not match address (= extension code))



▲1: IICS = 0001×110B
▲2: IICS = 0001×000B
▲3: IICS = 0010×010B
▲4: IICS = 0010×000B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, does not match address (= extension code))

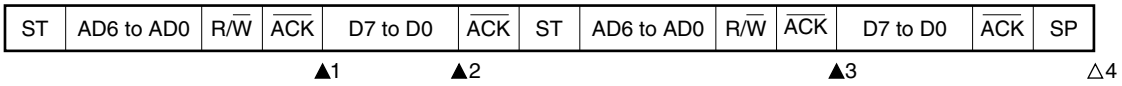


▲1: IICS = 0001×110B
▲2: IICS = 0001××00B
▲3: IICS = 0010×010B
▲4: IICS = 0010×110B
▲5: IICS = 0010××00B
△6: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(d) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

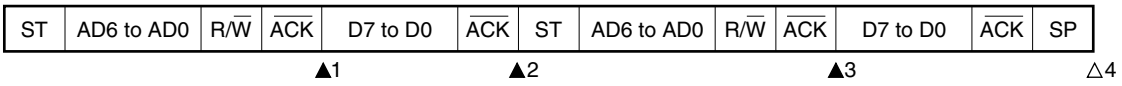
(i) When WTIM = 0 (after restart, does not match address (= not extension code))



▲1: IICS = 0001×110B
▲2: IICS = 0001×000B
▲3: IICS = 00000110B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, does not match address (= not extension code))



▲1: IICS = 0001×110B
▲2: IICS = 0001××00B
▲3: IICS = 00000110B
△4: IICS = 00000001B

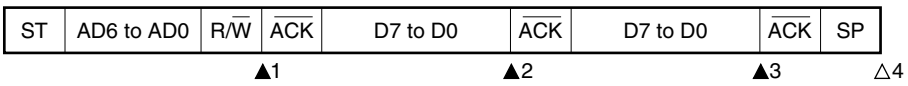
Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(3) Slave device operation (when receiving extension code)

The device is always participating in communication when it receives an extension code.

(a) Start ~ Code ~ Data ~ Data ~ Stop

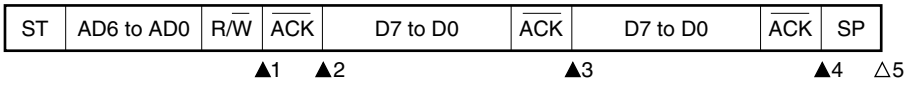
(i) When WTIM = 0



▲1: IICS = 0010×010B
▲2: IICS = 0010×000B
▲3: IICS = 0010×000B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1

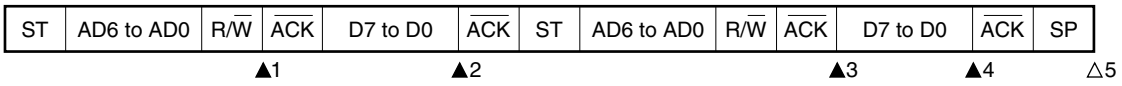


▲1: IICS = 0010×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010×100B
▲4: IICS = 0010××00B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(b) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

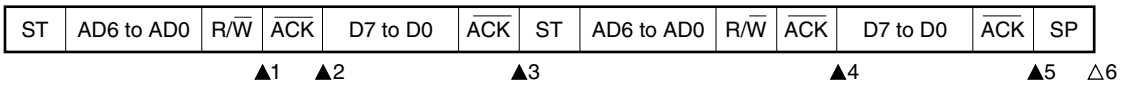
(i) When WTIM = 0 (after restart, matches SVA)



▲1: IICS = 0010×010B
▲2: IICS = 0010×000B
▲3: IICS = 0001×110B
▲4: IICS = 0001×000B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, matches SVA)

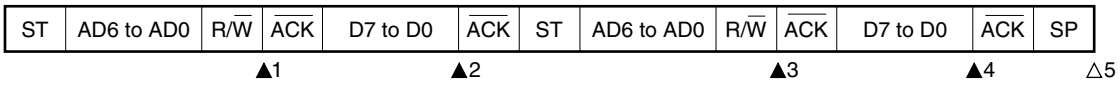


▲1: IICS = 0010×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010××00B
▲4: IICS = 0001×110B
▲5: IICS = 0001××00B
△6: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(c) Start ~ Code ~ Data ~ Start ~ Code ~ Data ~ Stop

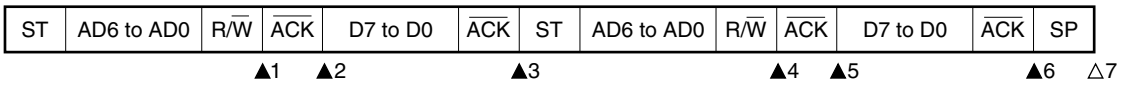
(i) When WTIM = 0 (after restart, extension code reception)



▲1: IICS = 0010×010B
▲2: IICS = 0010×000B
▲3: IICS = 0010×010B
▲4: IICS = 0010×000B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, extension code reception)



▲1: IICS = 0010×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010××00B
▲4: IICS = 0010×010B
▲5: IICS = 0010×110B
▲6: IICS = 0010××00B
△7: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

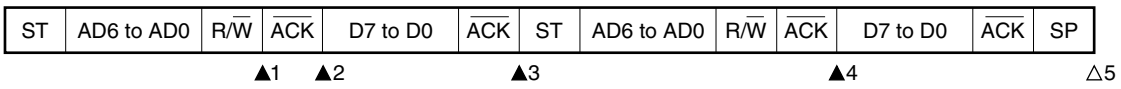
(d) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIM = 0 (after restart, does not match address (= not extension code))

▲1: IICS = 00100010B
▲2: IICS = 00100000B
▲3: IICS = 00000110B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, does not match address (= not extension code))

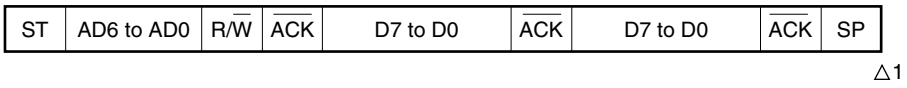


▲1: IICS = 00100010B
▲2: IICS = 00100110B
▲3: IICS = 00100×00B
▲4: IICS = 00000110B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(4) Operation without communication

(a) Start ~ Code ~ Data ~ Data ~ Stop



△1: IICS = 00000001B

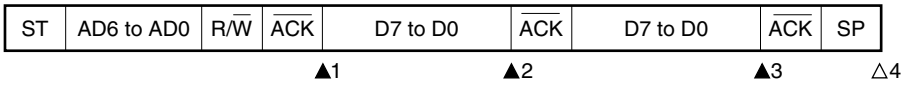
Remark △: Generated only when SPIE = 1

(5) Arbitration loss operation (operation as slave after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTS bit each time interrupt request signal INTIICA has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data

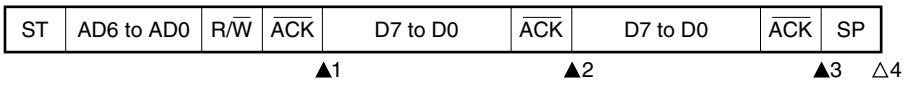
(i) When WTIM = 0



▲1: IICS = 0101×110B
▲2: IICS = 0001×000B
▲3: IICS = 0001×000B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1

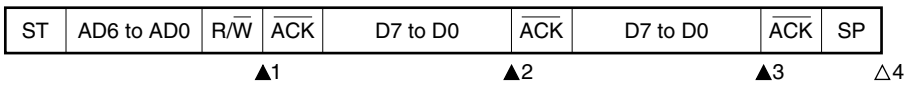


▲1: IICS = 0101×110B
▲2: IICS = 0001×100B
▲3: IICS = 0001××00B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(b) When arbitration loss occurs during transmission of extension code

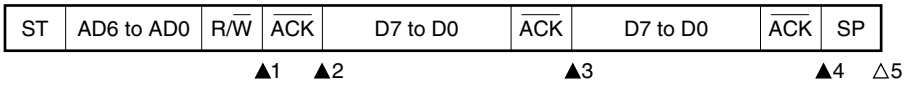
(i) When WTIM = 0



▲1: IICS = 0110×010B
▲2: IICS = 0010×000B
▲3: IICS = 0010×000B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1



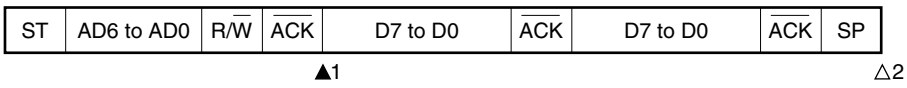
▲1: IICS = 0110×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010×100B
▲4: IICS = 0010××00B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(6) Operation when arbitration loss occurs (no communication after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTS bit each time interrupt request signal INTIICA has occurred to check the arbitration result.

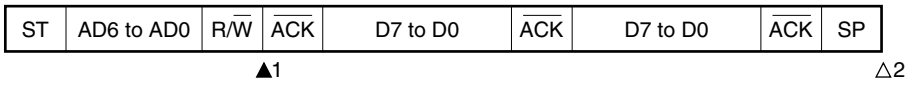
(a) When arbitration loss occurs during transmission of slave address data (when WTIM = 1)



▲1: IICS = 01000110B
△2: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1

(b) When arbitration loss occurs during transmission of extension code



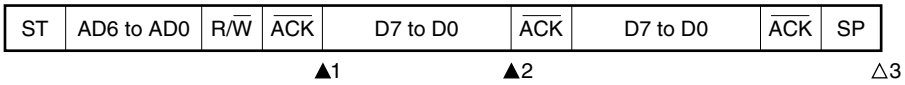
▲1 △2

▲1: IICS = 0110×010B
Sets LREL = 1 by software
△2: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(c) When arbitration loss occurs during transmission of data

(i) When WTIM = 0

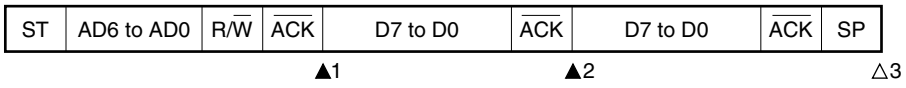


▲1 ▲2 △3

▲1: IICS = 10001110B
▲2: IICS = 01000000B
△3: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1

(ii) When WTIM = 1

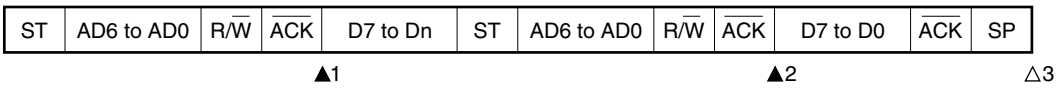


▲1: IICS = 10001110B
▲2: IICS = 01000100B
△3: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1

(d) When loss occurs due to restart condition during data transfer

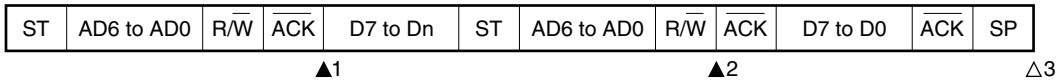
(i) Not extension code (Example: unmatches with SVA)



▲1: IICS = 1000×110B
▲2: IICS = 01000110B
△3: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care
n = 6 to 0

(ii) Extension code



▲1: IICS = 1000×110B
▲2: IICS = 01100010B
Sets LREL = 1 by software
△3: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care
n = 6 to 0

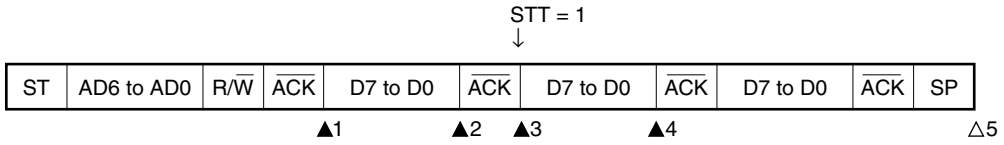
(e) When loss occurs due to stop condition during data transfer

▲1: IICS = 10000110B
△2: IICS = 01000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care
n = 6 to 0

(f) When arbitration loss occurs due to low-level data when attempting to generate a restart condition

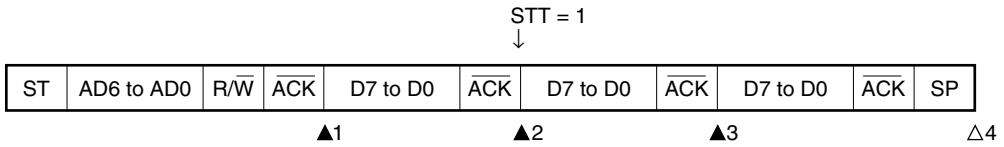
(i) When WTIM = 0



▲1: IICS = 1000×110B
▲2: IICS = 1000×000B (Sets the WTIM bit to 1)
▲3: IICS = 1000×100B (Clears the WTIM bit to 0)
▲4: IICS = 01000000B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1

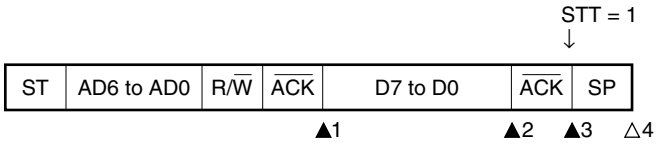


▲1: IICS = 1000×110B
▲2: IICS = 1000×100B (Sets the STT bit to 1)
▲3: IICS = 01000100B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(g) When arbitration loss occurs due to a stop condition when attempting to generate a restart condition

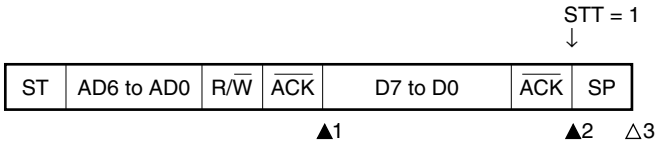
(i) When WTIM = 0



▲1: IICS = 1000×110B
▲2: IICS = 1000×000B (Sets the WTIM bit to 1)
▲3: IICS = 1000××00B (Sets the STT bit to 1)
△4: IICS = 01000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1

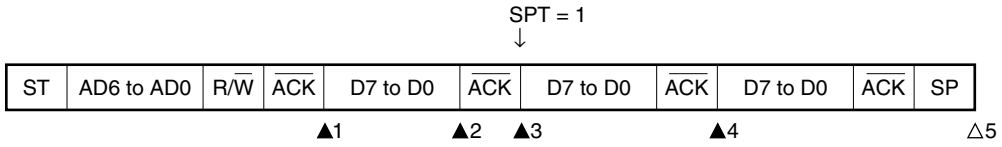


▲1: IICS = 1000×110B
▲2: IICS = 1000××00B (Sets the STT bit to 1)
△3: IICS = 01000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(h) When arbitration loss occurs due to low-level data when attempting to generate a stop condition

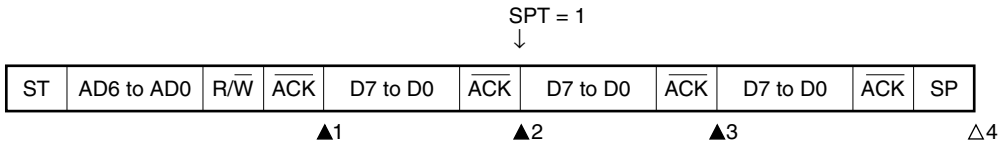
(i) When WTIM = 0



▲1: IICS = 1000×110B
▲2: IICS = 1000×000B (Sets the WTIM bit to 1)
▲3: IICS = 1000×100B (Clears the WTIM bit to 0)
▲4: IICS = 01000100B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1



▲1: IICS = 1000×110B
▲2: IICS = 1000×100B (Sets the SPT bit to 1)
▲3: IICS = 01000100B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

15.6 Timing Charts

When using the I^2C bus mode, the master device outputs an address via the serial bus to select one of several slave devices as its communication partner.

After outputting the slave address, the master device transmits the TRC bit (bit 3 of the IICA status register (IICS)), which specifies the data transfer direction, and then starts serial communication with the slave device.

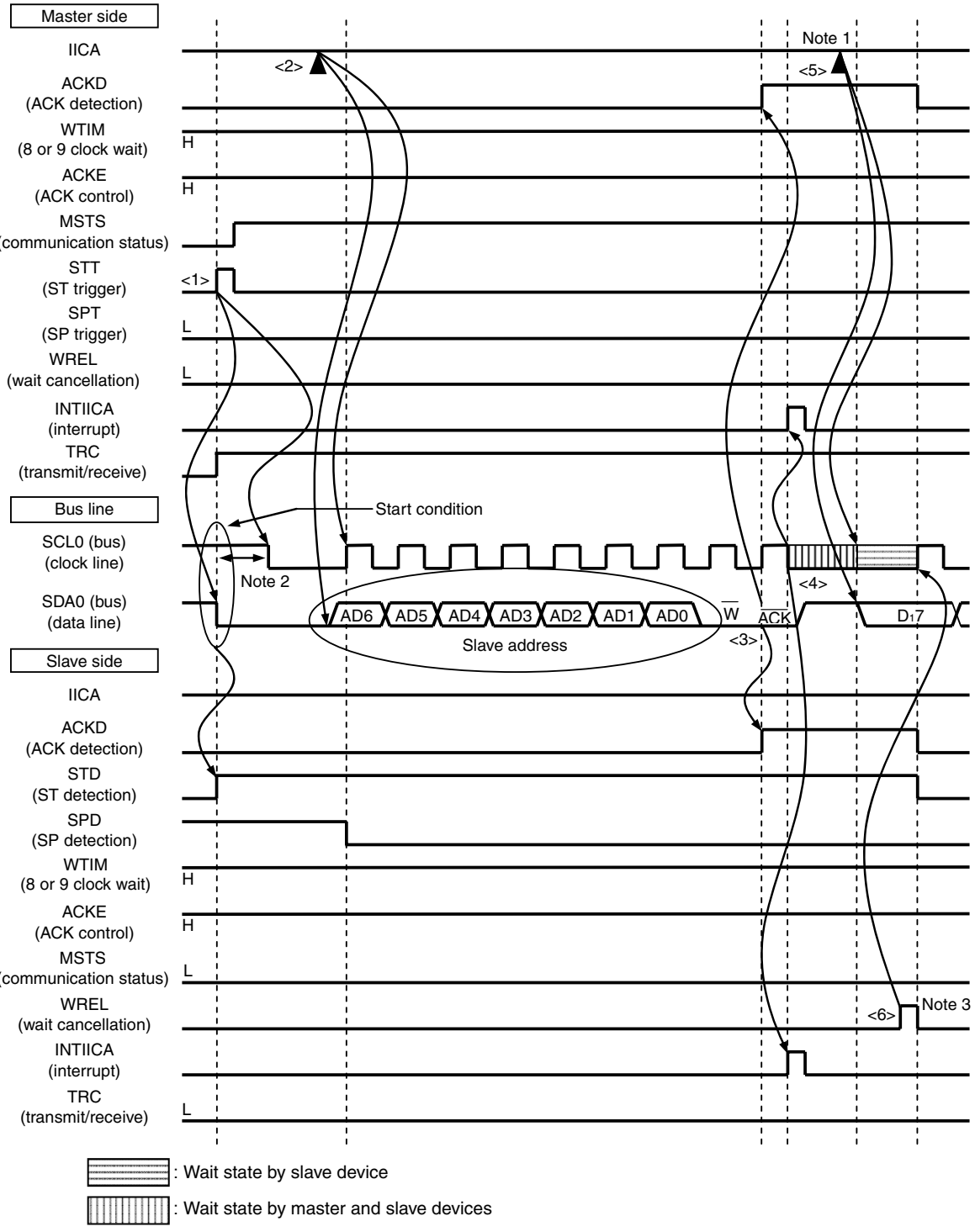
Figures 15-32 and 15-33 show timing charts of the data communication.

The IICA shift register (IICA)'s shift operation is synchronized with the falling edge of the serial clock (SCL0). The transmit data is transferred to the SO latch and is output (MSB first) via the SDA0 pin.

Data input via the SDA0 pin is captured into IICA at the rising edge of SCL0.

Figure 15-32. Example of Master to Slave Communication (9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/4)

(1) Start condition ~ address ~ data



<R> **Notes 1.** Write data to IICA, not setting the WREL bit, in order to cancel a wait state during transmission by a master device.

2. Make sure that the time between the fall of the SDA0 pin signal and the fall of the SCL0 pin signal is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

<R> **3.** For releasing wait state during reception of a slave device, write “FFH” to IICA or set the WREL bit.

The meanings of <1> to <6> in (1) Start condition ~ address ~ data in Figure 15-32 are explained below.

<R> <1> The start condition trigger is set by the master device (STT = 1) and a start condition (i.e. SCL0 = 1 changes SDA0 from 1 to 0) is generated once the bus data line goes low (SDA0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS = 1). The master device is ready to communicate once the bus clock line goes low (SCL0 = 0) after the hold time has elapsed.

<2> The master device writes the address + W (transmission) to the IICA shift register (IICA) and transmits the slave address.

<R> <3> In the slave device if the address received matches the address (SVA value) of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<R> <4> The master device issues an interrupt (INTIICA: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCL0 = 0) and issues an interrupt (INTIICA: address match)[Note].

<5> The master device writes the data to transmit to the IICA register and releases the wait status that it set by the master device.

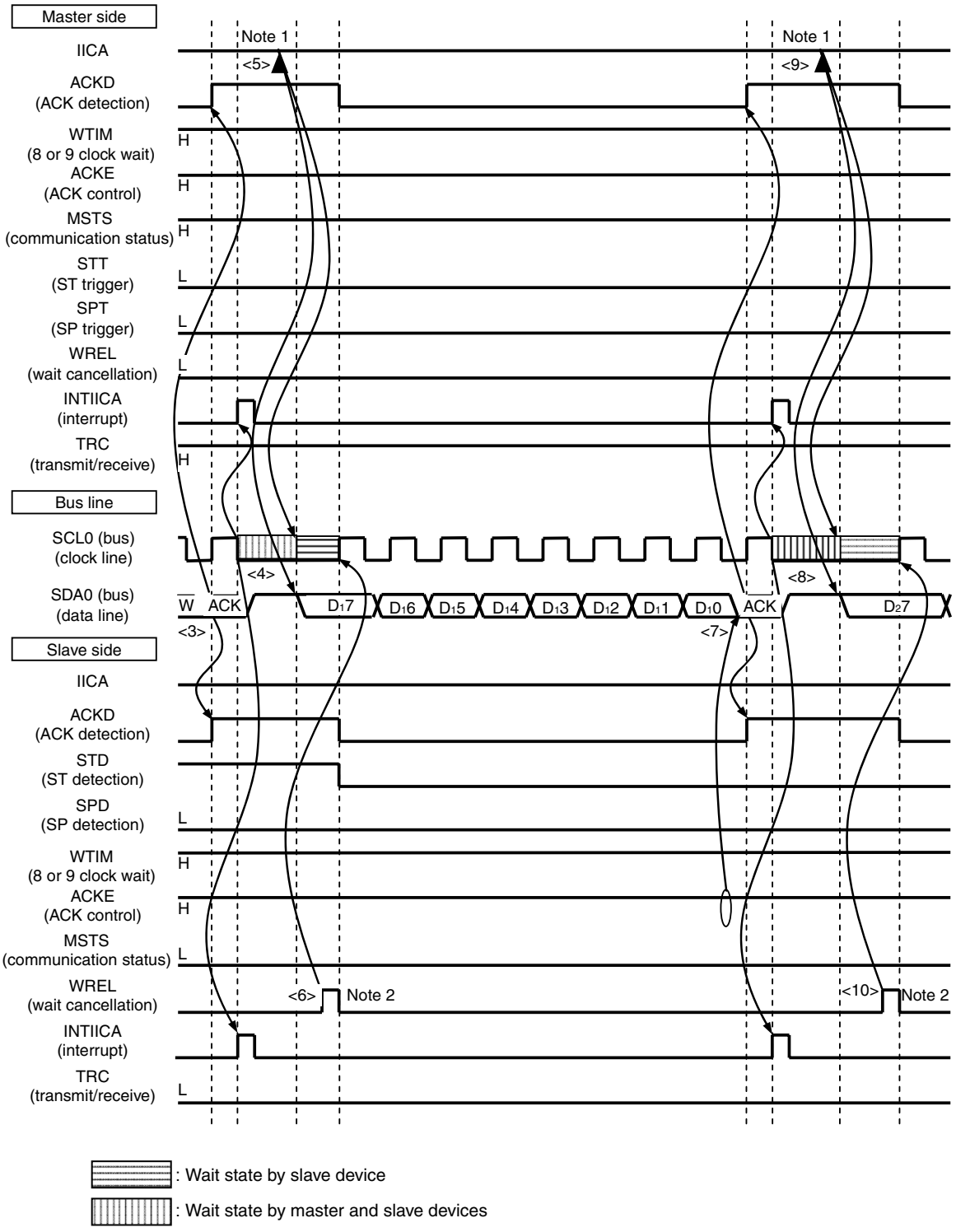
<6> If the slave device releases the wait status (WREL = 1), the master device starts transferring data to the slave device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDA0 = 1). The slave device also does not issue the INTIICA interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <15> in Figure 15-32 represent the entire procedure for communicating data using the I^2C bus. Figure 15-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 15-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 15-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

Figure 15-32. Example of Master to Slave Communication
(9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/4)

(2) Address ~ data ~ data



Notes 1. Write data to IICA, not setting the WREL bit, in order to cancel a wait state during transmission by a master device.

2. For releasing wait state during reception of a slave device, write “FFH” to IICA or set the WREL bit.

The meanings of <3> to <10> in (2) Address ~ data ~ data in Figure 15-32 are explained below.

<R> <3> In the slave device if the address received matches the address (SVA value) of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<R> <4> The master device issues an interrupt (INTIICA: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCL0 = 0) and issues an interrupt (INTIICA: address match)[Note].

<5> The master device writes the data to transmit to the IICA shift register (IICA) and releases the wait status that it set by the master device.

<6> If the slave device releases the wait status (WREL = 1), the master device starts transferring data to the slave device.

<R> <7> After data transfer is completed, because of ACKE = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA: end of transfer).

<9> The master device writes the data to transmit to the IICA register and releases the wait status that it set by the master device.

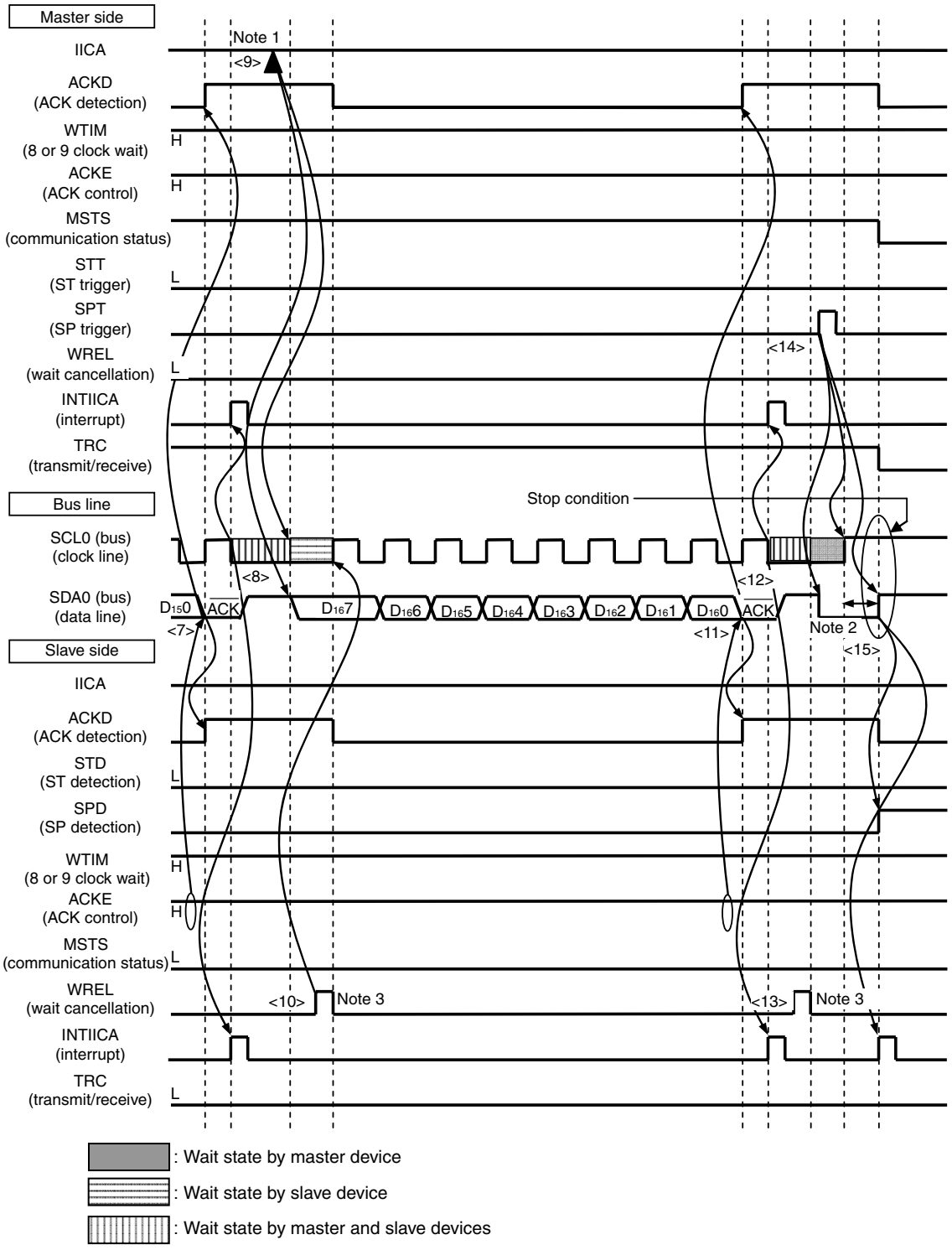
<10> The slave device reads the received data and releases the wait status (WREL = 1). The master device then starts transferring data to the slave device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDA0 = 1). The slave device also does not issue the INTIICA interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <15> in Figure 15-32 represent the entire procedure for communicating data using the I^2C bus. Figure 15-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 15-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 15-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

Figure 15-32. Example of Master to Slave Communication (9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/4)

(3) Data ~ data ~ Stop condition



Notes 1. Write data to IICA, not setting the WREL bit, in order to cancel a wait state during transmission by a master device.

2. Make sure that the time between the rise of the SCL0 pin signal and the generation of the stop condition after a stop condition has been issued is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

3. For releasing wait state during reception of a slave device, write “FFH” to IICA or set the WREL bit.

The meanings of <7> to <15> in (3) Data ~ data ~ stop condition in Figure 15-32 are explained below.

<R> <7> After data transfer is completed, because of ACKE = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA: end of transfer).

<9> The master device writes the data to transmit to the IICA shift register (IICA) and releases the wait status that it set by the master device.

<10> The slave device reads the received data and releases the wait status (WREL = 1). The master device then starts transferring data to the slave device.

<R> <11> When data transfer is complete, the slave device (ACKE =1) sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<12> The master device and slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA: end of transfer).

<13> The slave device reads the received data and releases the wait status (WREL = 1).

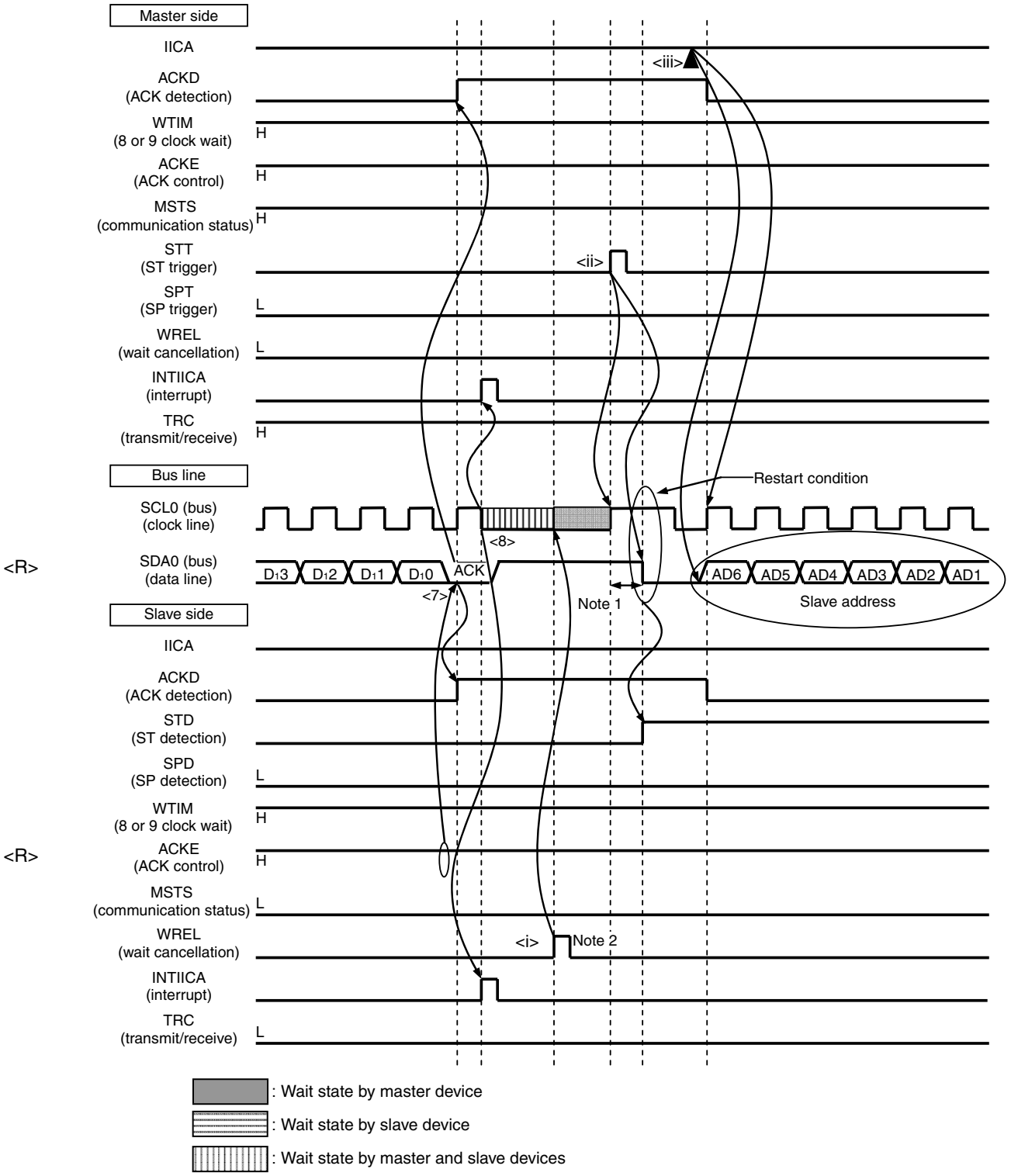
<R> <14> By the master device setting a stop condition trigger (SPT = 1), the bus data line is cleared (SDA0 = 0) and the bus clock line is set (SCL0 = 1). After the stop condition setup time has elapsed, by setting the bus data line (SDA0 = 1), the stop condition is then generated (i.e. SCL0 =1 changes SDA0 from 0 to 1).

<R> <15> When a stop condition is generated, the slave device detects the stop condition and issues an interrupt (INTIICA: stop condition).

Remark <1> to <15> in Figure 15-32 represent the entire procedure for communicating data using the I^2C bus. Figure 15-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 15-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 15-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

Figure 15-32. Example of Master to Slave Communication (9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (4/4)

(4) Data ~ restart condition ~ address



Notes 1. Make sure that the time between the rise of the SCL0 pin signal and the generation of the start condition after a restart condition has been issued is at least 4.7 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

<R> **2.** For releasing wait state during reception of a slave device, write “FFH” to IICA or set the WREL bit.

The following describes the operations in Figure 15-32 (4) Data ~ restart condition ~ address. After the operations in steps <7> and <8>, the operations in steps <i> to <iii> are performed. These steps return the processing to step <3>, the data transmission step.

<R> <7> After data transfer is completed, because of ACKE = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA: end of transfer).

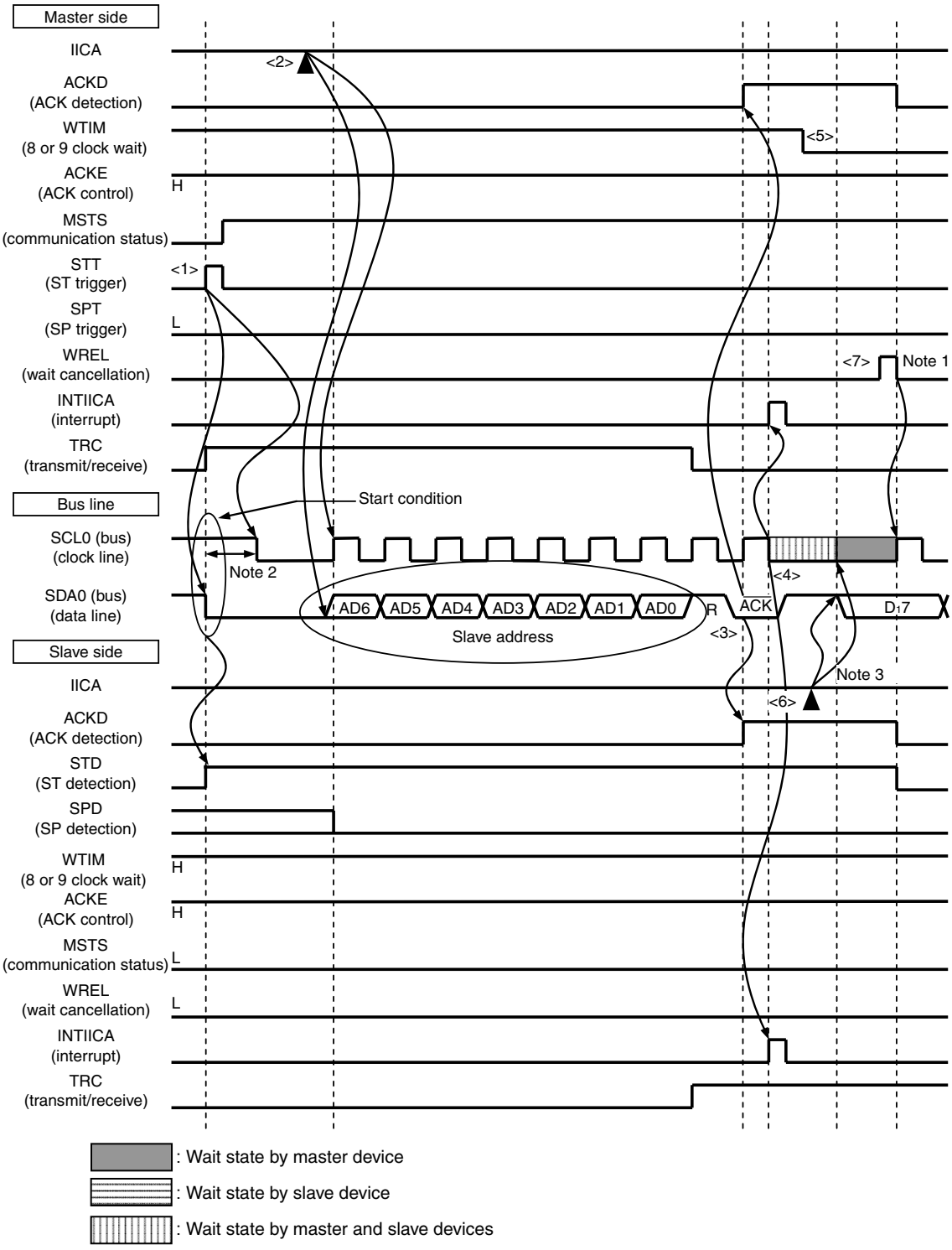
<i> The slave device reads the received data and releases the wait status (WREL = 1).

<R> <ii> The start condition trigger is set again by the master device (STT = 1) and a start condition (i.e. SCL0 =1 changes SDA0 from 1 to 0) is generated once the bus clock line goes high (SCL0 = 1) and the bus data line goes low (SDA0 = 0) after the restart condition setup time has elapsed. When the start condition is subsequently detected, the master device is ready to communicate once the bus clock line goes low (SCL0 = 0) after the hold time has elapsed.

<R> <iii> The master device writing the address + R/W (transmission) to the IICA shift register (IICA) enables the slave address to be transmitted.

Figure 15-33. Example of Slave to Master Communication (8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)

(1) Start condition ~ address ~ data



<R> **Notes 1.** For releasing wait state during reception of a master device, write “FFH” to IICA or set the WREL bit.

2. Make sure that the time between the fall of the SDA0 pin signal and the fall of the SCL0 pin signal is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

<R> **3.** Write data to IICA, not setting the WREL bit, in order to cancel a wait state during transmission by a slave device.

The meanings of <1> to <7> in (1) Start condition ~ address ~ data in Figure 15-33 are explained below.

<R> <1> The start condition trigger is set by the master device (STT = 1) and a start condition (i.e. SCL0 =1 changes SDA0 from 1 to 0) is generated once the bus data line goes low (SDA0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS = 1). The master device is ready to communicate once the bus clock line goes low (SCL0 = 0) after the hold time has elapsed.

<2> The master device writes the address + W (transmission) to the IICA shift register (IICA) and transmits the slave address.

<R> <3> In the slave device if the address received matches the address (SVA value) of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<R> <4> The master device issues an interrupt (INTIICA: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCL0 = 0) and issues an interrupt (INTIICA: address match)[Note].

<5> The timing at which the master device sets the wait status changes to the 8th clock (WTIM = 0).

<6> The slave device writes the data to transmit to the IICA register and releases the wait status that it set by the slave device.

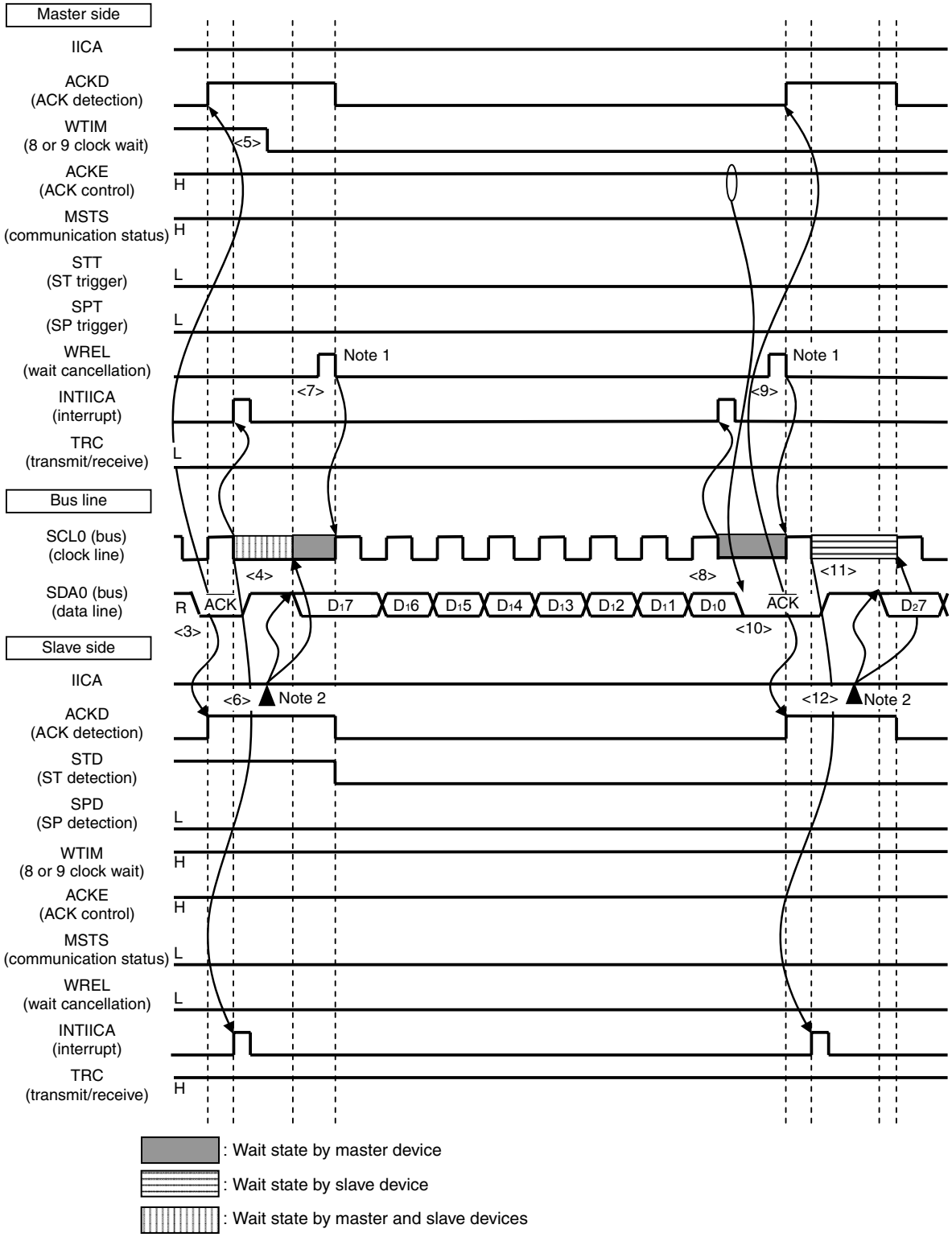
<R> <7> The master device releases the wait status (WREL = 1) and starts transferring data from the slave device to the master device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDA0 = 1). The slave device also does not issue the INTIICA interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <19> in Figure 15-33 represent the entire procedure for communicating data using the I^2C bus. Figure 15-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 15-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 15-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

Figure 15-33. Example of Slave to Master Communication (8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/3)

(2) Address ~ data ~ data



<R> **Notes 1.** For releasing wait state during reception of a master device, write “FFH” to IICA or set the WREL bit.

<R> **2.** Write data to IICA, not setting the WREL bit, in order to cancel a wait state during transmission by a slave device.

The meanings of <3> to <12> in (2) Address ~ data ~ data in Figure 15-33 are explained below.

<R> <3> In the slave device if the address received matches the address (SVA value) of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<R> <4> The master device issues an interrupt (INTIICA: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCL0 = 0) and issues an interrupt (INTIICA: address match)[Note].

<R> <5> The master device changes the timing of the wait status to the 8th clock (WTIM = 0).

<6> The slave device writes the data to transmit to the IICA shift register (IICA) and releases the wait status that it set by the slave device.

<R> <7> The master device releases the wait status (WREL = 1) and starts transferring data from the slave device to the master device.

<R> <8> The master device sets a wait status (SCL0 = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICA: end of transfer). Because of ACKE = 1 in the master device, the master device then sends an ACK by hardware to the slave device.

<9> The master device reads the received data and releases the wait status (WREL = 1).

<10> The ACK is detected by the slave device (ACKD = 1) at the rising edge of the 9th clock.

<11> The slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and the slave device issue an interrupt (INTIICA: end of transfer).

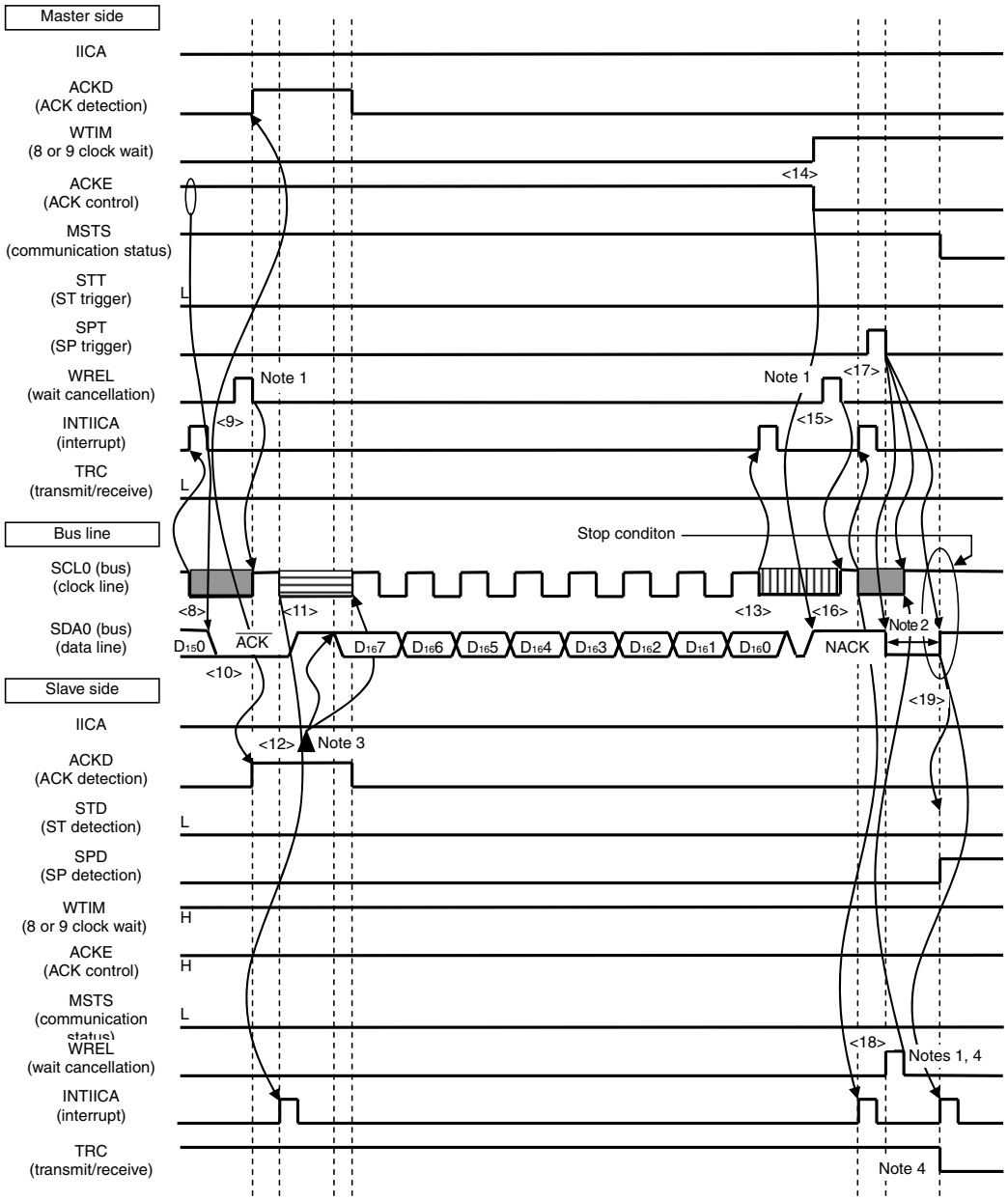
<R> <12> By the slave device writing the data to transmit to the IICA register, the wait status set by the slave device is released. The slave device then starts transferring data to the master device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDA0 = 1). The slave device also does not issue the INTIICA interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <19> in Figure 15-33 represent the entire procedure for communicating data using the I^2C bus. Figure 15-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 15-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 15-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

Figure 15-33. Example of Slave to Master Communication (8-Clock and 9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/3)

(3) Data ~ data ~ stop condition



Notes 1. To cancel a wait state, write "FFH" to IICA or set the WREL bit.

2. Make sure that the time between the rise of the SCL0 pin signal and the generation of the stop condition after a stop condition has been issued is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

<R> **3.** Write data to IICA, not setting the WREL bit, in order to cancel a wait state during transmission by a slave device.

<R> **4.** If a wait state during transmission by a slave device is canceled by setting the WREL bit, the TRC bit will be cleared.

The meanings of <8> to <19> in (3) Data ~ data ~ stop condition in Figure 15-33 are explained below.

<R> <8> The master device sets a wait status (SCL0 = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICA: end of transfer). Because of ACKE = 0 in the master device, the master device then sends an ACK by hardware to the slave device.

<9> The master device reads the received data and releases the wait status (WREL = 1).

<10> The ACK is detected by the slave device (ACKD = 1) at the rising edge of the 9th clock.

<11> The slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and the slave device issue an interrupt (INTIICA: end of transfer).

<R> <12> By the slave device writing the data to transmit to the IICA register, the wait status set by the slave device is released. The slave device then starts transferring data to the master device.

<13> The master device issues an interrupt (INTIICA: end of transfer) at the falling edge of the 8th clock, and sets a wait status (SCL0 = 0). Because ACK control (ACKE = 1) is performed, the bus data line is at the low level (SDA0 = 0) at this stage.

<R> <14> The master device sets NACK as the response (ACKE = 0) and changes the timing at which it sets the wait status to the 9th clock (WTIM = 1).

<15> If the master device releases the wait status (WREL = 1), the slave device detects the NACK (ACK = 0) at the rising edge of the 9th clock.

<16> The master device and slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA: end of transfer).

<17> When the master device issues a stop condition (SPT = 1), the bus data line is cleared (SDA0 = 0) and the master device releases the wait status. The master device then waits until the bus clock line is set (SCL0 = 1).

<18> The slave device acknowledges the NACK, halts transmission, and releases the wait status (WREL = 1) to end communication. Once the slave device releases the wait status, the bus clock line is set (SCL0 = 1).

<R> <19> Once the master device recognizes that the bus clock line is set (SCL0 = 1) and after the stop condition setup time has elapsed, the master device sets the bus data line (SDA0 = 1) and issues a stop condition (i.e. SCL0 =1 changes SDA0 from 0 to 1). The slave device detects the generated stop condition and slave device issue an interrupt (INTIICA: stop condition).

Remark <1> to <19> in Figure 15-33 represent the entire procedure for communicating data using the I^2C bus. Figure 15-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 15-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 15-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

CHAPTER 16 MULTIPLIER/DIVIDER

16.1 Functions of Multiplier/Divider

The multiplier/divider has the following functions.

- 16 bits × 16 bits = 32 bits (multiplication)
- 32 bits ÷ 32 bits = 32 bits, 32-bit remainder (division)

16.2 Configuration of Multiplier/Divider

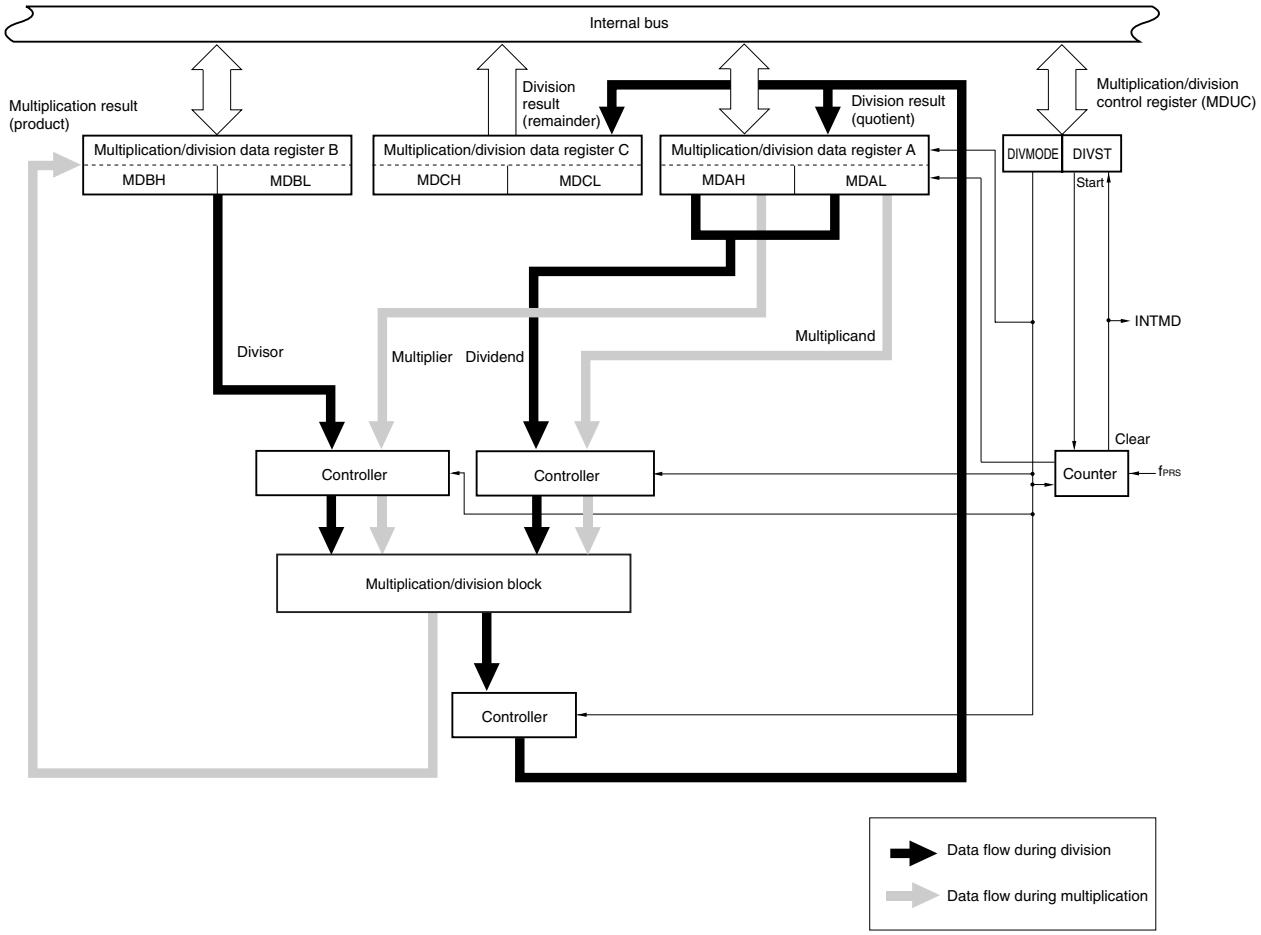
The multiplier/divider consists of the following hardware.

Table 16-1. Configuration of Multiplier/Divider

Item	Configuration
Registers	Multiplication/division data register A (L) (MDAL) Multiplication/division data register A (H) (MDAH) Multiplication/division data register B (L) (MDBL) Multiplication/division data register B (H) (MDBH) Multiplication/division data register C (L) (MDCL) Multiplication/division data register C (H) (MDCH)
Control register	Multiplication/division control register (MDUC)

Figure 16-1 shows a block diagram of the multiplier/divider.

Figure 16-1. Block Diagram of Multiplier/Divider



(1) Multiplication/division data register A (MDAH, MDAL)

The MDAH and MDAL registers set the values that are used for a multiplication or division operation and store the operation result. They set the multiplier and multiplicand data in the multiplication mode, and set the dividend data in the division mode. Furthermore, the operation result (quotient) is stored in the MDAH and MDAL registers in the division mode.

The MDAH and MDAL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 16-2. Format of Multiplication/Division Data Register A (MDAH, MDAL)

Address: FFFF0H, FFFF1H, FFFF2H, FFFF3H After reset: 0000H, 0000H R/W

Symbol FFFF3H FFFF2H

MDAH	MDAH 15	MDAH 14	MDAH 13	MDAH 12	MDAH 11	MDAH 10	MDAH 9	MDAH 8	MDAH 7	MDAH 6	MDAH 5	MDAH 4	MDAH 3	MDAH 2	MDAH 1	MDAH 0

Symbol FFFF1H FFFF0H

MDAL	MDAL 15	MDAL 14	MDAL 13	MDAL 12	MDAL 11	MDAL 10	MDAL 9	MDAL 8	MDAL 7	MDAL 6	MDAL 5	MDAL 4	MDAL 3	MDAL 2	MDAL 1	MDAL 0

Cautions 1. Do not rewrite the MDAH and MDAL registers values during division operation processing (while the multiplication/division control register (MDUC) is 81H). The operation will be executed in this case, but the operation result will be an undefined value.

2. The MDAH and MDAL registers values read during division operation processing (while MDUC is 81H) will not be guaranteed.

The following table shows the functions of the MDAH and MDAL registers during operation execution.

Table 16-2. Functions of MDAH and MDAL Registers During Operation Execution

DIVMODE	Operation Mode	Setting	Operation Result
0	Multiplication mode	MDAH: Multiplier MDAL: Multiplicand	–
1	Division mode	MDAH: Divisor (higher 16 bits) MDAL: Dividend (lower 16 bits)	MDAH: Division result (quotient) Higher 16 bits MDAL: Division result (quotient) Lower 16 bits

Remark DIVMODE: Bit 7 of the multiplication/division control register (MDUC)

(2) Multiplication/division data register B (MDBL, MDBH)

The MDBH and MDBL registers set the values that are used for multiplication or division operation and store the operation result. They store the operation result (product) in the multiplication mode and set the divisor data in the division mode.

The MDBH and MDBL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 16-3. Format of Multiplication/Division Data Register B (MDBH, MDBL)

Address: FFFF4H, FFFF5H, FFFF6H, FFFF7H After reset: 0000H, 0000H R/W

Symbol	FFFF7H								FFFF6H							
MDBH	MDBH 15	MDBH 14	MDBH 13	MDBH 12	MDBH 11	MDBH 10	MDBH 9	MDBH 8	MDBH 7	MDBH 6	MDBH 5	MDBH 4	MDBH 3	MDBH 2	MDBH 1	MDBH 0

Symbol	FFFF5H								FFFF4H							
MDBL	MDBL 15	MDBL 14	MDBL 13	MDBL 12	MDBL 11	MDBL 10	MDBL 9	MDBL 8	MDBL 7	MDBL 6	MDBL 5	MDBL 4	MDBHL 3	MDBL 2	MDBL 1	MDBL 0

Cautions 1. Do not rewrite the MDBH and MDBL registers values during division operation processing (while the multiplication/division control register (MDUC) is 81H). The operation result will be an undefined value.

2. Do not set the MDBH and MDBL registers to 0000H in the division mode. If they are set, the operation result will be an undefined value.

The following table shows the functions of the MDBH and MDBL registers during operation execution.

Table 16-3. Functions of MDBH and MDBL Registers During Operation Execution

DIVMODE	Operation Mode	Setting	Operation Result
0	Multiplication mode	–	MDBH: Multiplication result (product) Higher 16 bits MDBL: Multiplication result (product) Lower 16 bits
1	Division mode	MDBH: Divisor (higher 16 bits) MDBL: Dividend (lower 16 bits)	–

Remark DIVMODE: Bit 7 of the multiplication/division control register (MDUC)

(3) Multiplication/division data register C (MDCL, MDCH)

The MDCH and MDCL registers store remainder value of the operation result in the division mode. They are not used in the multiplication mode.

The MDCH and MDCL registers can be read by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 16-4. Format of Multiplication/Division Data Register C (MDCH, MDCL)

Address: F00E0H, F00E1H, F00E2H, F00E3H After reset: 0000H, 0000H R

Symbol F00E3H F00E2H

MDCH	MDCH 15	MDCH 14	MDCH 13	MDCH 12	MDCH 11	MDCH 10	MDCH 9	MDCH 8	MDCH 7	MDCH 6	MDCH 5	MDCH 4	MDCH 3	MDCH 2	MDCH 1	MDCH 0

Symbol F00E1H F00E0H

MDCL	MDCL 15	MDCL 14	MDCL 13	MDCL 12	MDCL 11	MDCL 10	MDCL 9	MDCL 8	MDCL 7	MDCL 6	MDCL 5	MDCL 4	MDCL 3	MDCL 2	MDCL 1	MDCL 0

Caution The MDCH and MDCL registers values read during division operation processing (while the multiplication/division control register (MDUC) is 81H) will not be guaranteed.

Table 16-4. Functions of MDCH and MDCL Registers During Operation Execution

DIVMODE	Operation Mode	Setting	Operation Result
0	Multiplication mode	–	–
1	Division mode	–	MDCH: Remainder (higher 16 bits) MDCL: Remainder (lower 16 bits)

Remark DIVMODE: Bit 7 of the multiplication/division control register (MDUC)

The register configuration differs between when multiplication is executed and when division is executed, as follows.

- Register configuration during multiplication

<Multiplier A> <Multiplier B> <Product>

MDAL (bits 15 to 0) × MDAH (bits 15 to 0) = [MDBH (bits 15 to 0), MDBL (bits 15 to 0)]

- Register configuration during division

<Dividend> <Divisor>

[MDAH (bits 15 to 0), MDAL (bits 15 to 0)] ÷ [MDBH (bits 15 to 0), MDBL (bits 15 to 0)] =

<Quotient> <Remainder>

[MDAH (bits 15 to 0), MDAL (bits 15 to 0)] ··· [MDCH (bits 15 to 0), MDCL (bits 15 to 0)]

16.3 Register Controlling Multiplier/Divider

The multiplier/divider is controlled by using the multiplication/division control register (MDUC).

(1) Multiplication/division control register (MDUC)

The MDUC register is an 8-bit register that controls the operation of the multiplier/divider.

The MDUC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16-5. Format of Multiplication/Division Control Register (MDUC)

Address: F00E8H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
MDUC	DIVMODE	0	0	0	0	0	0	DIVST

DIVMODE	Operation mode (multiplication/division) selection
0	Multiplication mode
1	Division mode

DIVST[Note]	Division operation start/stop
0	Division operation processing complete
1	Starts division operation/division operation processing in progress

Note The DIVST bit can only be set (1) in the division mode. In the division mode, division operation is started by setting (1) the DIVST bit. The DIVST bit is automatically cleared (0) when the operation ends. In the multiplication mode, operation is automatically started by setting the multiplier and multiplicand to multiplication/division data register A (MDAH, MDAL), respectively.

Cautions 1. Do not rewrite the DIVMODE bit during operation processing (while the DIVST bit is 1). If it is rewritten, the operation result will be an undefined value.

2. The DIVST bit cannot be cleared (0) by using software during division operation processing (while the DIVST bit is 1).

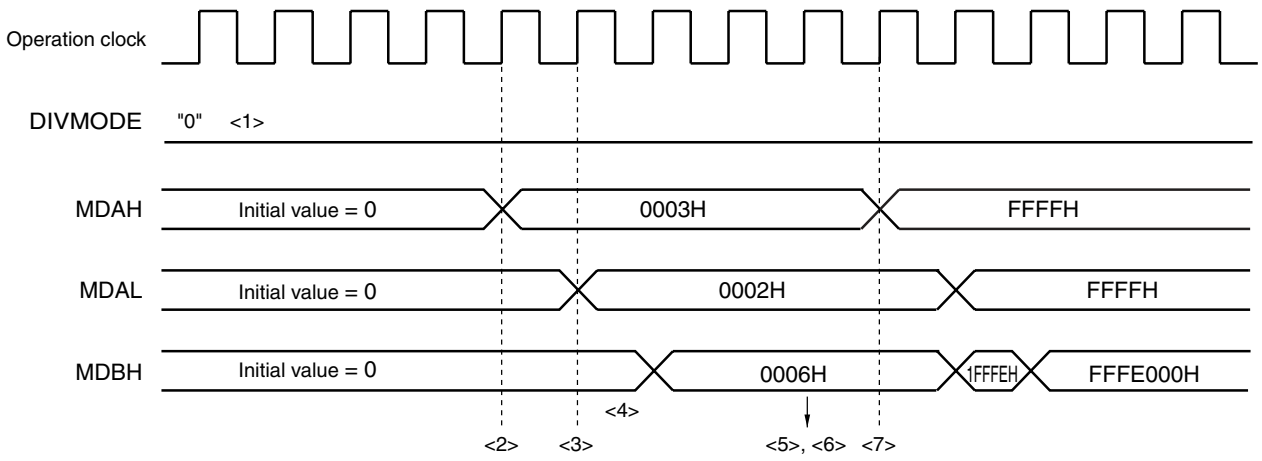
16.4 Operations of Multiplier/Divider

16.4.1 Multiplication operation

- Initial setting
  - <1> Set bit 7 (DIVMODE) of the multiplication/division control register (MDUC) to 0.
  - <2> Set the multiplicand to multiplication/division data register A (L) (MDAL).
  - <3> Set the multiplier to multiplication/division data register A (H) (MDAH).
    (There is no preference in the order of executing steps <2> and <3>. Multiplication operation is automatically started when the multiplier and multiplicand are set to the MDAH and MDAL registers, respectively.)
- During operation processing
  - <4> Wait for at least one clock. The operation will end when one clock has been issued.
- Operation end
  - <5> Read the product (lower 16 bits) from multiplication/division data register B (L) (MDBL).
  - <6> Read the product (higher 16 bits) from multiplication/division data register B (H) (MDBH).
    (There is no preference in the order of executing steps <5> and <6>.)
- Next operation
  - <7> To execute multiplication operation next, start from the “Initial setting” for multiplication operation.
  - <8> To execute division operation next, start from the “Initial setting” in **16.4.2 Division operation**.

Remark Steps <1> to <7> correspond to <1> to <7> in Figure 16-6.

Figure 16-6. Timing Diagram of Multiplication Operation (0003H × 0002H)



16.4.2 Division operation

- Initial setting
  - <1> Set bit 7 (DIVMODE) of the multiplication/division control register (MDUC) to 1.
  - <2> Set the dividend (higher 16 bits) to multiplication/division data register A (H) (MDAH).
  - <3> Set the dividend (lower 16 bits) to multiplication/division data register A (L) (MDAL).
  - <4> Set the divisor (higher 16 bits) to multiplication/division data register B (H) (MDBH).
  - <5> Set the divisor (lower 16 bits) to multiplication/division data register B (L) (MDBL).
  - <6> Set bit 0 (DIVST) of the MDUC register to 1.

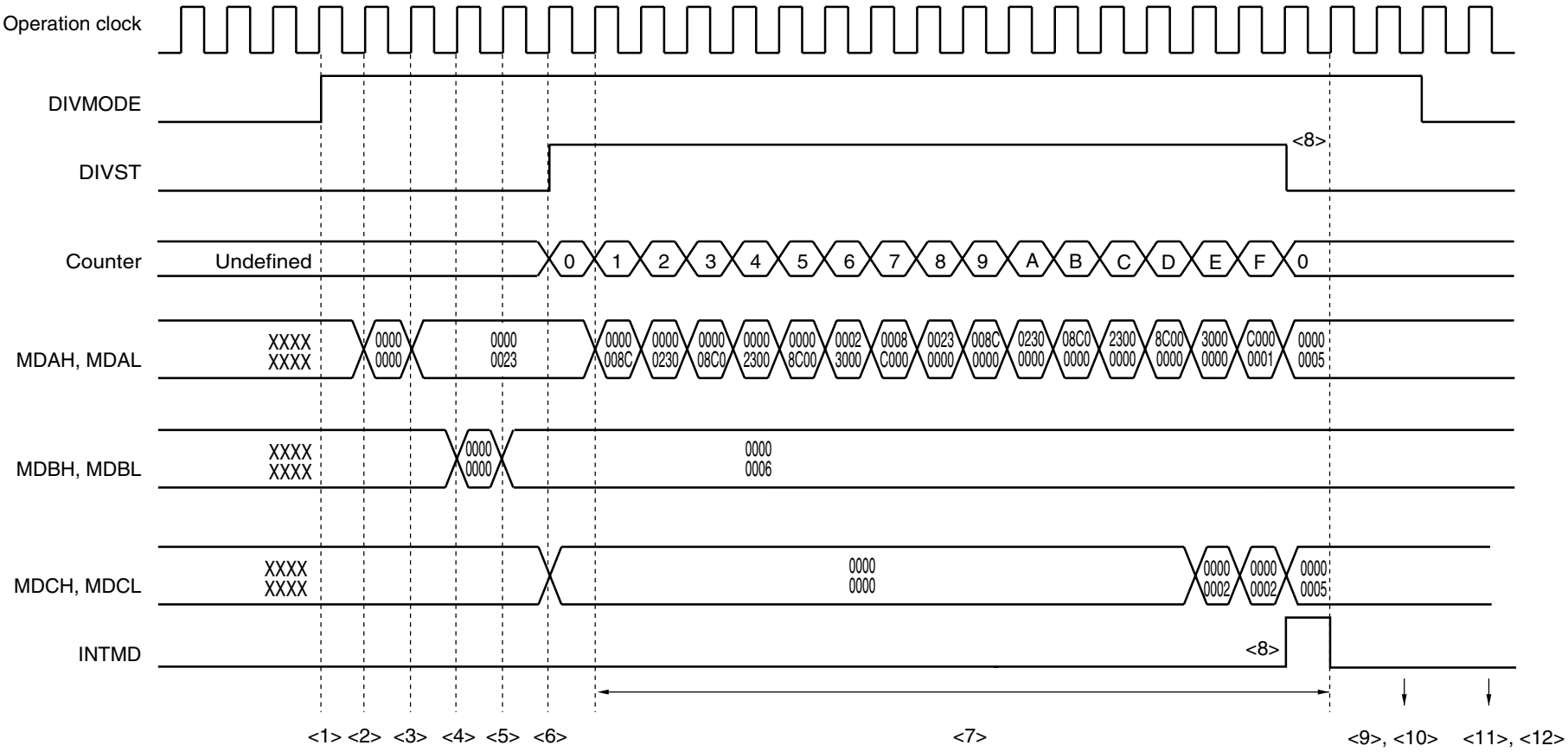
    (There is no preference in the order of executing steps <2> to <5>.)
- During operation processing
  - <7> The operation will end when one of the following processing is completed.
    - A wait of at least 16 clocks (The operation will end when 16 clocks have been issued.)
    - A check whether the DIVST bit has been cleared
    - Generation of a division completion interrupt (INTMD)

    (The read values of the MDBL, MDBH, MDCL, and MDCH registers during operation processing are not guaranteed.)
- Operation end
  - <8> The DIVST bit is cleared (0) and an interrupt request signal (INTMD) is generated (end of operation).
  - <9> Read the quotient (lower 16 bits) from the MDAL register.
  - <10> Read the quotient (higher 16 bits) from the MDAH register.
  - <11> Read the remainder (lower 16 bits) from multiplication/division data register C (L) (MDCL).
  - <12> Read the remainder (higher 16 bits) from multiplication/division data register C (H) (MDCH).

    (There is no preference in the order of executing steps <9> to <12>.)
- Next operation
  - <13> To execute multiplication operation next, start from the “Initial setting” in **16.4.1 Multiplication operation**.
  - <14> To execute division operation next, start from the “Initial setting” for division operation.

Remark Steps <1> to <12> correspond to <1> to <12> in Figure 16-7.

Figure 16-7. Timing Diagram of Division Operation (Example: 35 ÷ 6 = 5, Remainder 5)



CHAPTER 17 DMA CONTROLLER

The 78K0R/Kx3-L has an internal DMA (Direct Memory Access) controller.

Data can be automatically transferred between the peripheral hardware supporting DMA, SFRs, and internal RAM without via CPU.

As a result, the normal internal operation of the CPU and data transfer can be executed in parallel with transfer between the SFR and internal RAM, and therefore, a large capacity of data can be processed. In addition, real-time control using communication, timer, and A/D can also be realized.

17.1 Functions of DMA Controller

- Number of DMA channels: 2
- Transfer unit: 8 or 16 bits
- Maximum transfer unit: 1024 times
- Transfer type: 2-cycle transfer (One transfer is processed in 2 clocks and the CPU stops during that processing.)
- Transfer mode: Single-transfer mode
- Transfer request: Selectable from the following peripheral hardware interrupts
  - A/D converter
  - Serial interface (CSI00, CSI01, CSI10, UART0, UART1, UART3[Note], or IIC10)
  - Timer (channel 0, 1, 4, or 5)
- Transfer target: Between SFR and internal RAM

Note 78K0R/KF3-L, 78K0R/KG3-L only.

Here are examples of functions using DMA.

- Successive transfer of serial interface
- Batch transfer of analog data
- Capturing A/D conversion result at fixed interval
- Capturing port value at fixed interval

17.2 Configuration of DMA Controller

The DMA controller includes the following hardware.

Table 17-1. Configuration of DMA Controller

Item	Configuration
Address registers	• DMA SFR address registers 0, 1 (DSA0, DSA1) • DMA RAM address registers 0, 1 (DRA0, DRA1)
Count register	• DMA byte count registers 0, 1 (DBC0, DBC1)
Control registers	• DMA mode control registers 0, 1 (DMC0, DMC1) • DMA operation control register 0, 1 (DRC0, DRC1)

(1) DMA SFR address register n (DSAn)

This is an 8-bit register that is used to set an SFR address that is the transfer source or destination of DMA channel n.

Set the lower 8 bits of the SFR addresses FFF00H to FFFFFH.

This register is not automatically incremented but fixed to a specific value.

In the 16-bit transfer mode, the least significant bit is ignored and is treated as an even address.

The DSAn register can be read or written in 8-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 00H.

Figure 17-1. Format of DMA SFR Address Register n (DSAn)

Address: FFFB0H (DSA0), FFFB1H (DSA1) After reset: 00H R/W

	7	6	5	4	3	2	1	0
DSAn								

Remark n: DMA channel number (n = 0, 1)

(2) DMA RAM address register n (DRAn)

This is a 16-bit register that is used to set a RAM address that is the transfer source or destination of DMA channel n.

Addresses of the internal RAM area other than the general-purpose registers (FF900H to FFEDFH in the case of the μPD78F1001, 78F1004, and 78F1007) can be set to this register.

Set the lower 16 bits of the RAM address.

This register is automatically incremented when DMA transfer has been started. It is incremented by +1 in the 8-bit transfer mode and by +2 in the 16-bit transfer mode. DMA transfer is started from the address set to this DRAn register. When the data of the last address has been transferred, the DRAn register stops with the value of the last address +1 in the 8-bit transfer mode, and the last address +2 in the 16-bit transfer mode.

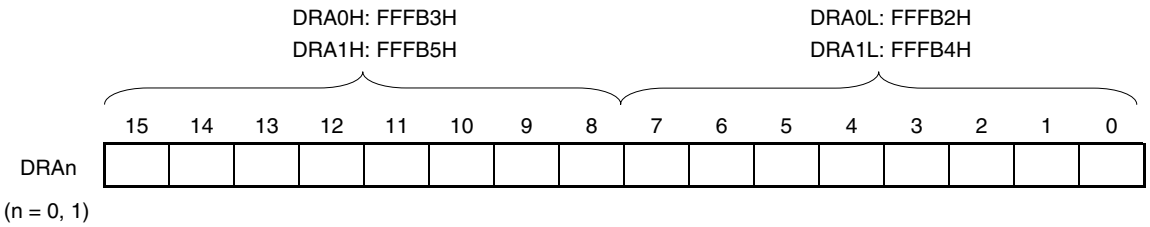
In the 16-bit transfer mode, the least significant bit is ignored and is treated as an even address.

The DRAn register can be read or written in 8-bit or 16-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 0000H.

Figure 17-2. Format of DMA RAM Address Register n (DRAn)

Address: FFFB2H, FFFB3H (DRA0), FFFB4H, FFFB5H (DRA1) After reset: 0000H R/W



Remark n: DMA channel number (n = 0, 1)

(3) DMA byte count register n (DBCn)

This is a 10-bit register that is used to set the number of times DMA channel n executes transfer. Be sure to set the number of times of transfer to this DBCn register before executing DMA transfer (up to 1024 times).

Each time DMA transfer has been executed, this register is automatically decremented. By reading this DBCn register during DMA transfer, the remaining number of times of transfer can be learned.

The DBCn register can be read or written in 8-bit or 16-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 0000H.

Figure 17-3. Format of DMA Byte Count Register n (DBCn)

Address: FFFB6H, FFFB7H (DBC0), FFFB8H, FFFB9H (DBC1) After reset: 0000H R/W

DBC0H: FFFB7H
DBC1H: FFFB9H

DBC0L: FFFB6H
DBC1L: FFFB8H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBCn	0	0	0	0	0	0										

(n = 0, 1)

DBCn[9:0]	Number of Times of Transfer (When DBCn is Written)	Remaining Number of Times of Transfer (When DBCn is Read)
000H	1024	Completion of transfer or waiting for 1024 times of DMA transfer
001H	1	Waiting for remaining one time of DMA transfer
002H	2	Waiting for remaining two times of DMA transfer
003H	3	Waiting for remaining three times of DMA transfer
•	•	•
•	•	•
•	•	•
3FEH	1022	Waiting for remaining 1022 times of DMA transfer
3FFH	1023	Waiting for remaining 1023 times of DMA transfer

Cautions 1. Be sure to clear bits 15 to 10 to "0".

2. If the general-purpose register is specified or the internal RAM space is exceeded as a result of continuous transfer, the general-purpose register or SFR space are written or read, resulting in loss of data in these spaces. Be sure to set the number of times of transfer that is within the internal RAM space.

Remark n: DMA channel number (n = 0, 1)

17.3 Registers Controlling DMA Controller

DMA controller is controlled by the following registers.

- DMA mode control register n (DMCn)
- DMA operation control register n (DRCn)

Remark n: DMA channel number (n = 0, 1)

(1) DMA mode control register n (DMCn)

The DMCn register is a register that is used to set a transfer mode of DMA channel n. It is used to select a transfer direction, data size, setting of pending, and start source. Bit 7 (STGn) is a software trigger that starts DMA.

Rewriting bits 6, 5, and 3 to 0 of the DMCn register is prohibited during operation (when DSTn = 1).

The DMCn register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17-4. Format of DMA Mode Control Register n (DMCn) (1/2)

Address: FFFBAH (DMC0), FFFBBH (DMC1) After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
DMCn	STGn	DRSn	DSn	DWAITn	IFCn3	IFCn2	IFCn1	IFCn0

STGn[Note 1]	DMA transfer start software trigger
0	No trigger operation
1	DMA transfer is started when DMA operation is enabled (DENn = 1).
DMA transfer is performed once by writing 1 to the STGn bit when DMA operation is enabled (DENn = 1). When this bit is read, 0 is always read.	

DRSn	Selection of DMA transfer direction
0	SFR to internal RAM
1	Internal RAM to SFR

DSn	Specification of transfer data size for DMA transfer
0	8 bits
1	16 bits

DWAITn[Note 2]	Pending of DMA transfer
0	Executes DMA transfer upon DMA start request (not held pending).
1	Holds DMA start request pending if any.
DMA transfer that has been held pending can be started by clearing the value of the DWAITn bit to 0. It takes 2 clocks to actually hold DMA transfer pending when the value of the DWAITn bit is set to 1.	

Notes 1. The software trigger (STGn) can be used regardless of the IFCn0 to IFCn3 bits values.

2. When DMA transfer is held pending while using both DMA channels, be sure to hold the DMA transfer pending for both channels (by setting the DWAIT0 and DWAIT1 bits to 1).

Remark n: DMA channel number (n = 0, 1)

Figure 17-4. Format of DMA Mode Control Register n (DMCn) (2/2)

Address: FFFBAH (DMC0), FFFBBH (DMC1) After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
DMCn	STGn	DRSn	DSn	DWAITn	IFCn3	IFCn2	IFCn1	IFCn0

IFCn 3	IFCn 2	IFCn 1	IFCn 0	Selection of DMA start source[Note 1]	
				Trigger signal	Trigger contents
0	0	0	0	–	Disables DMA transfer by interrupt. (Only software trigger is enabled.)
0	0	1	0	INTTM00	End of timer channel 0 count or capture end interrupt
0	0	1	1	INTTM01	End of timer channel 1 count or capture end interrupt
0	1	0	0	INTTM04	End of timer channel 4 count or capture end interrupt
0	1	0	1	INTTM05	End of timer channel 5 count or capture end interrupt
0	1	1	0	INTST0/INTCSI00	UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt
0	1	1	1	INTSR0/INTCSI01	UART0 reception transfer end interrupt/CSI01 transfer end or buffer empty interrupt
1	0	0	0	INTST1/INTCSI10/INTIIC10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt/IIC10 transfer end interrupt
1	0	0	1	INTSR1	UART1 reception transfer end interrupt
1	0	1	0	INTST3[Note 2]	UART3 transmission transfer end or buffer empty interrupt
1	0	1	1	INTSR3[Note 2]	UART3 reception transfer end interrupt
1	1	0	0	INTAD	A/D conversion end interrupt
Other than above				Setting prohibited	

Notes 1. The software trigger (STGn) can be used regardless of the IFCn0 to IFCn3 bits values.

2. 78K0R/KF3-L, 78K0R/KG3-L only.

Remark n: DMA channel number (n = 0, 1)

(2) DMA operation control register n (DRCn)

The DRCn register is a register that is used to enable or disable transfer of DMA channel n.

Rewriting bit 7 (DENn) of this register is prohibited during operation (when DSTn = 1).

The DRCn register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17-5. Format of DMA Operation Control Register n (DRCn)

Address: FFFBCH (DRC0), FFFBDH (DRC1) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
DRCn	DENn	0	0	0	0	0	0	DSTn

DENn	DMA operation enable flag
0	Disables operation of DMA channel n (stops operating cock of DMA).
1	Enables operation of DMA channel n.
DMAC waits for a DMA trigger when DSTn = 1 after DMA operation is enabled (DENn = 1).	

DSTn	DMA transfer mode flag
0	DMA transfer of DMA channel n is completed.
1	DMA transfer of DMA channel n is not completed (still under execution).
DMAC waits for a DMA trigger when DSTn = 1 after DMA operation is enabled (DENn = 1). When a software trigger (STGn) or the start source trigger set by the IFCn3 to IFCn0 bits is input, DMA transfer is started. When DMA transfer is completed after that, this bit is automatically cleared to 0. Write 0 to this bit to forcibly terminate DMA transfer under execution.	

Cautions 1. The DSTn flag is automatically cleared to 0 when a DMA transfer is completed. Writing the DENn flag is enabled only when DSTn = 0. When a DMA transfer is terminated without waiting for generation of the interrupt (INTDMAn) of DMAn, therefore, set the DSTn bit to 0 and then the DENn bit to 0 (for details, refer to 17.5.5 Forced termination by software).

2. When the FSEL bit of the OSMC register has been set to 1, do not enable (DENn = 1) DMA operation for at least three clocks after the setting.

Remark n: DMA channel number (n = 0, 1)

17.4 Operation of DMA Controller

17.4.1 Operation procedure

<1> The DMA controller is enabled to operate when DENn = 1. Before writing the other registers, be sure to set the DENn bit to 1. Use 80H to write with an 8-bit manipulation instruction.

<2> Set an SFR address, a RAM address, the number of times of transfer, and a transfer mode of DMA transfer to DMA SFR address register n (DSAn), DMA RAM address register n (DRAn), DMA byte count register n (DBCn), and DMA mode control register n (DMCn).

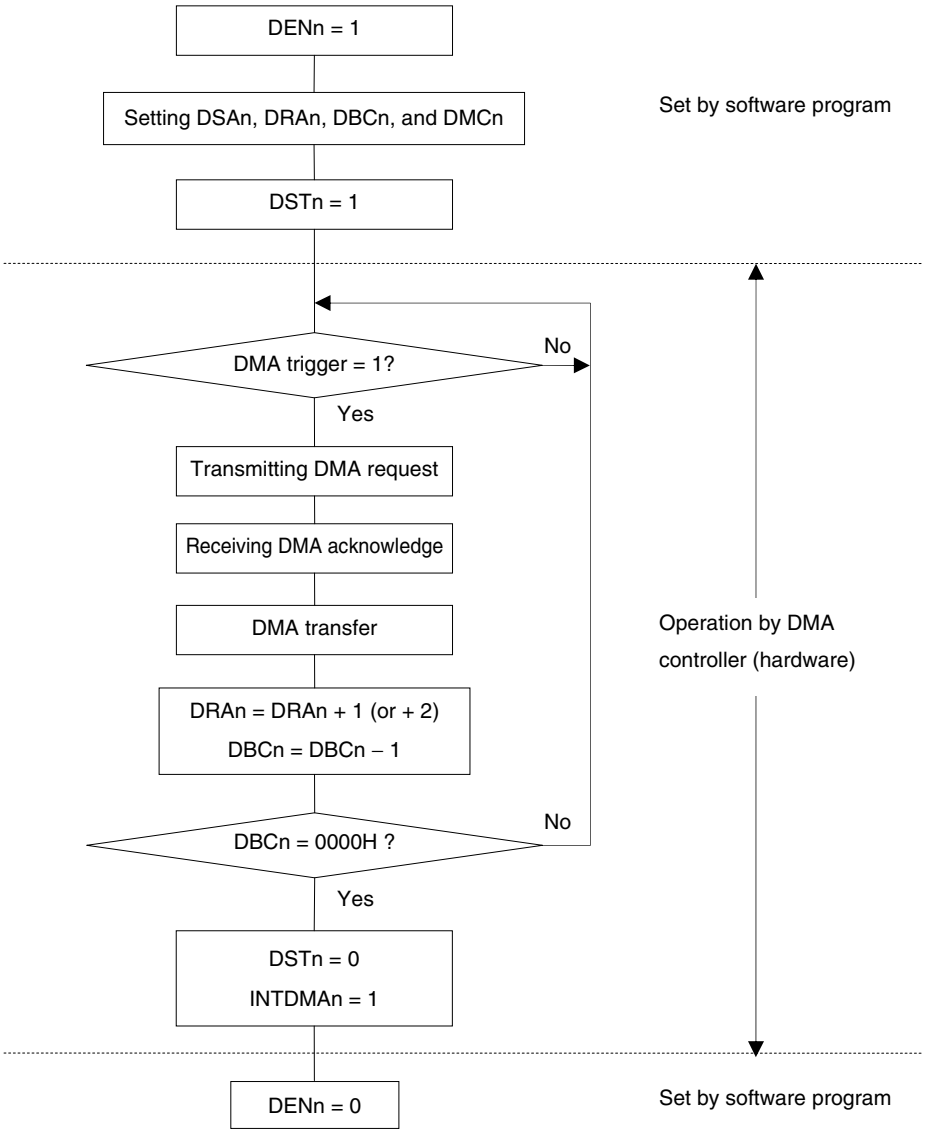
<3> The DMA controller waits for a DMA trigger when DSTn = 1. Use 81H to write with an 8-bit manipulation instruction.

<4> When a software trigger (STGn) or a start source trigger specified by the IFCn3 to IFCn0 bits is input, a DMA transfer is started.

<5> Transfer is completed when the number of times of transfer set by the DBCn register reaches 0, and transfer is automatically terminated by occurrence of an interrupt (INTDMAn).

<6> Stop the operation of the DMA controller by clearing the DENn bit to 0 when the DMA controller is not used.

Figure 17-6. Operation Procedure



Remark n: DMA channel number (n = 0, 1)

17.4.2 Transfer mode

The following four modes can be selected for DMA transfer by using bits 6 and 5 (DRSn and DSn) of DMA mode control register n (DMCn).

DRSn	DSn	DMA Transfer Mode
0	0	Transfer from SFR of 1-byte data (fixed address) to RAM (address is incremented by +1)
0	1	Transfer from SFR of 2-byte data (fixed address) to RAM (address is incremented by +2)
1	0	Transfer from RAM of 1-byte data (address is incremented by +1) to SFR (fixed address)
1	1	Transfer from RAM of 2-byte data (address is incremented by +2) to SFR (fixed address)

By using these transfer modes, up to 1024 bytes of data can be consecutively transferred by using the serial interface, data resulting from A/D conversion can be consecutively transferred, and port data can be scanned at fixed time intervals by using a timer.

17.4.3 Termination of DMA transfer

When DBCn = 00H and DMA transfer is completed, the DSTn bit is automatically cleared to 0. An interrupt request (INTDMAn) is generated and transfer is terminated.

When the DSTn bit is cleared to 0 to forcibly terminate DMA transfer, DMA byte count register n (DBCn) and DMA RAM address register n (DRAn) hold the value when transfer is terminated.

The interrupt request (INTDMAn) is not generated if transfer is forcibly terminated.

Remark n: DMA channel number (n = 0, 1)

17.5 Example of Setting of DMA Controller

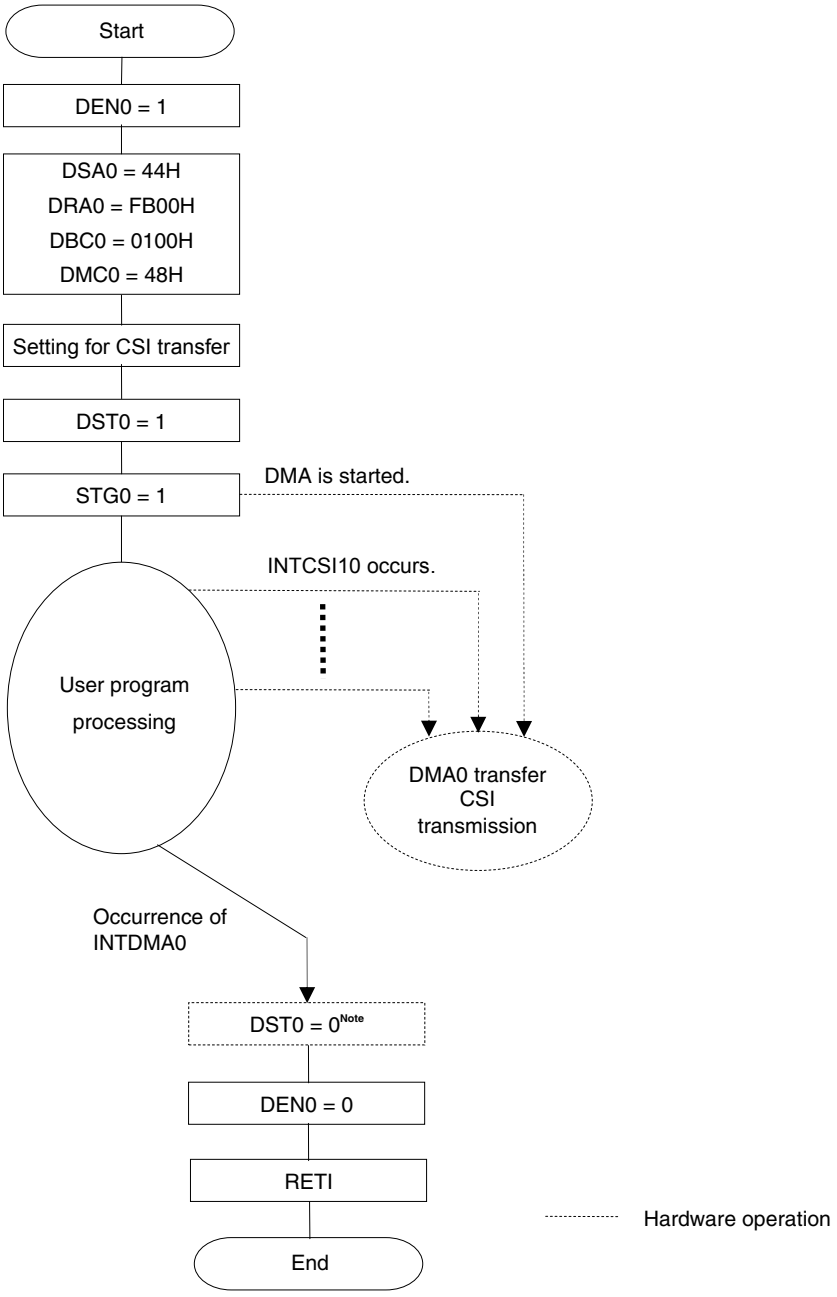
17.5.1 CSI consecutive transmission

A flowchart showing an example of setting for CSI consecutive transmission is shown below.

- Consecutive transmission of CSI10 (256 bytes)
- DMA channel 0 is used for DMA transfer.
- DMA start source: INTCSI10 (software trigger (STG0) only for the first start source)
- Interrupt of CSI10 is specified by IFC03 to IFC00 = 1000B.
- Transfers FFB00H to FFBFFH (256 bytes) of RAM to FFF44H of the data register (SIO10) of CSI.

Remark IFC03 to IFC00: Bits 3 to 0 of DMA mode control registers 0 (DMC0)

Figure 17-7. Example of Setting for CSI Consecutive Transmission



Note The DST0 flag is automatically cleared to 0 when a DMA transfer is completed.
Writing the DEN0 flag is enabled only when DST0 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA0 (INTDMA0), set the DST0 bit to 0 and then the DEN0 bit to 0 (for details, refer to **17.5.5 Forced termination by software**).

The fist trigger for consecutive transmission is not started by the interrupt of CSI. In this example, it start by a software trigger.

CSI transmission of the second time and onward is automatically executed.

A DMA interrupt (INTDMA0) occurs when the last transmit data has been written to the data register.

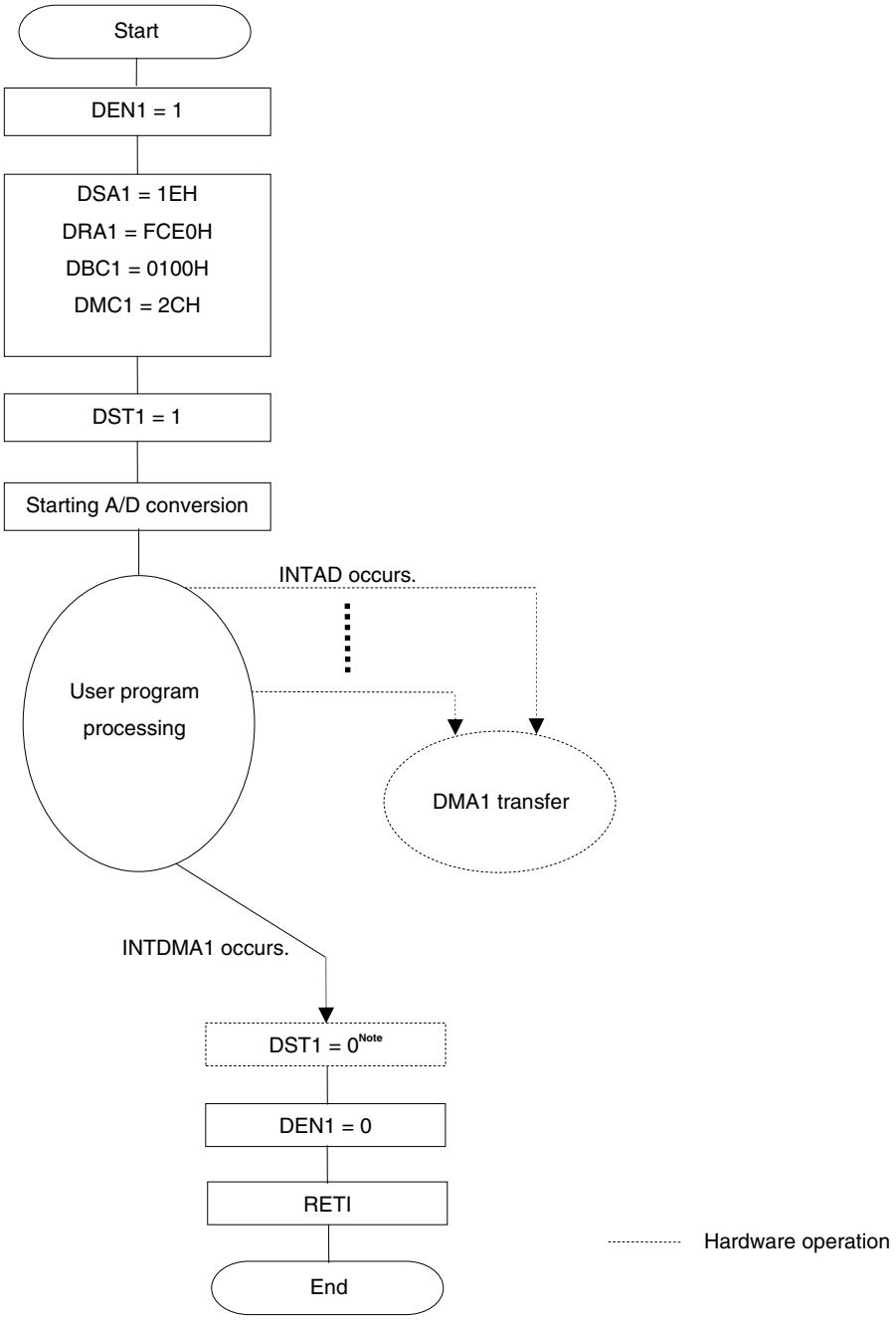
17.5.2 Consecutive capturing of A/D conversion results

A flowchart of an example of setting for consecutively capturing A/D conversion results is shown below.

- Consecutive capturing of A/D conversion results.
- DMA channel 1 is used for DMA transfer.
- DMA start source: INTAD
- Interrupt of A/D is specified by IFC13 to IFC10 = 1100B.
- Transfers FFF1EH and FFF1FH (2 bytes) of the 10-bit A/D conversion result register (ADCR) to 512 bytes of FFCE0H to FFEDFH of RAM.

Remark IFC13 to IFC10: Bits 3 to 0 of DMA mode control registers 1 (DMC1)

Figure 17-8. Example of Setting of Consecutively Capturing A/D Conversion Results



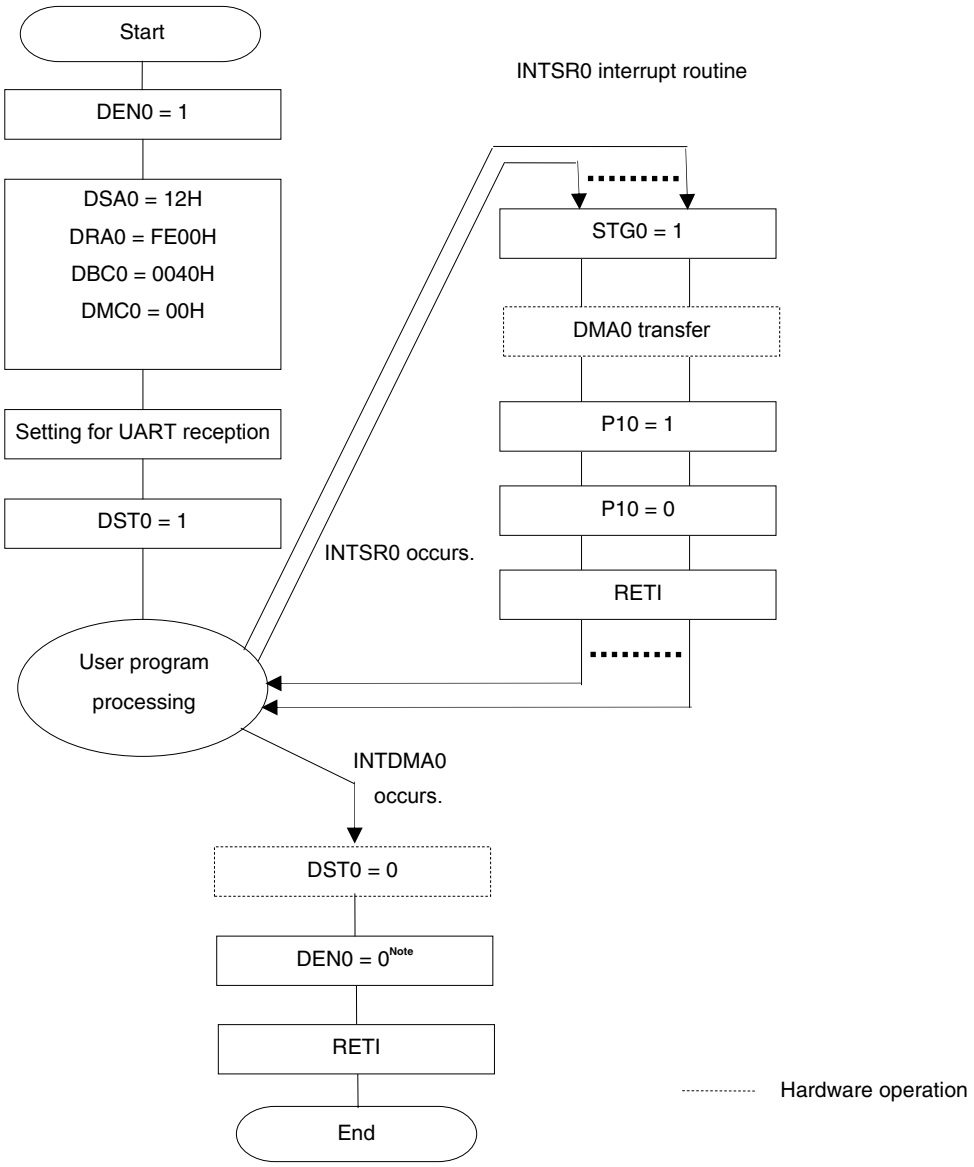
Note The DST1 flag is automatically cleared to 0 when a DMA transfer is completed.
Writing the DEN1 flag is enabled only when DST1 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA1 (INTDMA1), set the DST1 bit to 0 and then the DEN1 bit to 0 (for details, refer to **17.5.5 Forced termination by software**).

17.5.3 UART consecutive reception + ACK transmission

A flowchart illustrating an example of setting for UART consecutive reception + ACK transmission is shown below.

- Consecutively receives data from UART0 and outputs ACK to P10 on completion of reception.
- DMA channel 0 is used for DMA transfer.
- DMA start source: Software trigger (DMA transfer on occurrence of an interrupt is disabled.)
- Transfers FFF12H of UART receive data register 0 (RXD0) to 64 bytes of FFE00H to FFE3FH of RAM.

Figure 17-9. Example of Setting for UART Consecutive Reception + ACK Transmission



Note The DST0 flag is automatically cleared to 0 when a DMA transfer is completed.
Writing the DEN0 flag is enabled only when DST0 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA0 (INTDMA0), set the DST0 bit to 0 and then the DEN0 bit to 0 (for details, refer to **17.5.5 Forced termination by software**).

Remark This is an example where a software trigger is used as a DMA start source.
If ACK is not transmitted and if only data is consecutively received from UART, the UART reception end interrupt (INTSR0) can be used to start DMA for data reception.

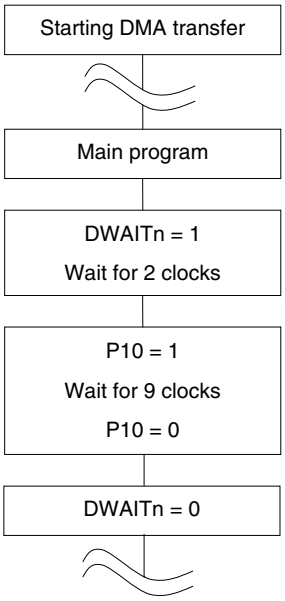
17.5.4 Holding DMA transfer pending by DWAITn bit

When DMA transfer is started, transfer is performed while an instruction is executed. At this time, the operation of the CPU is stopped and delayed for the duration of 2 clocks. If this poses a problem to the operation of the set system, a DMA transfer can be held pending by setting the DWAITn bit to 1. The DMA transfer for a transfer trigger that occurred while DMA transfer was held pending is executed after the pending status is canceled. However, because only one transfer trigger can be held pending for each channel, even if multiple transfer triggers occur for one channel during the pending status, only one DMA transfer is executed after the pending status is canceled.

To output a pulse with a width of 10 clocks of the operating frequency from the P10 pin, for example, the clock width increases to 12 if a DMA transfer is started midway. In this case, the DMA transfer can be held pending by setting the DWAITn bit to 1.

After setting the DWAITn bit to 1, it takes two clocks until a DMA transfer is held pending.

Figure 17-10. Example of Setting for Holding DMA Transfer Pending by DWAITn Bit



Caution When DMA transfer is held pending while using both DMA channels, be sure to held the DMA transfer pending for both channels (by setting DWAIT0 and DWAIT1 to 1). If the DMA transfer of one channel is executed while that of the other channel is held pending, DMA transfer might not be held pending for the latter channel.

Remarks 1. n: DMA channel number (n = 0, 1)

2. 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

17.5.5 Forced termination by software

After the DSTn bit is set to 0 by software, it takes up to 2 clocks until a DMA transfer is actually stopped and the DSTn bit is set to 0. To forcibly terminate a DMA transfer by software without waiting for occurrence of the interrupt (INTDMAn) of DMAn, therefore, perform either of the following processes.

<When using one DMA channel>

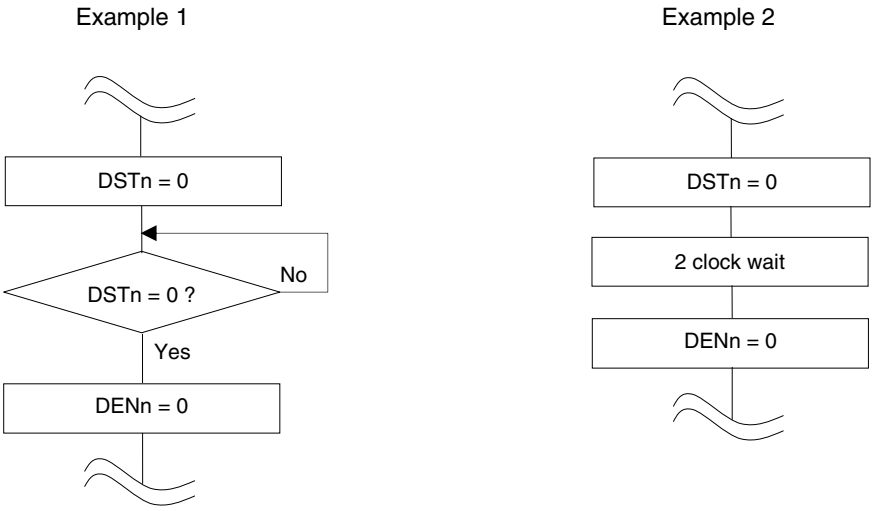
- Set the DSTn bit to 0 (use DRCn = 80H to write with an 8-bit manipulation instruction) by software, confirm by polling that the DSTn bit has actually been cleared to 0, and then set the DENn bit to 0 (use DRCn = 00H to write with an 8-bit manipulation instruction).

- Set the DSTn bit to 0 (use DRCn = 80H to write with an 8-bit manipulation instruction) by software and then set the DENn bit to 0 (use DRCn = 00H to write with an 8-bit manipulation instruction) two or more clocks after.

<When using both DMA channels>

- To forcibly terminate DMA transfer by software when using both DMA channels (by setting DSTn to 0), clear the DSTn bit to 0 after the DMA transfer is held pending by setting the DWAIT0 and DWAIT1 bits of both channels to 1. Next, clear the DWAIT0 and DWAIT1 bits of both channels to 0 to cancel the pending status, and then clear the DENn bit to 0.

Figure 17-11. Forced Termination of DMA Transfer (1/2)



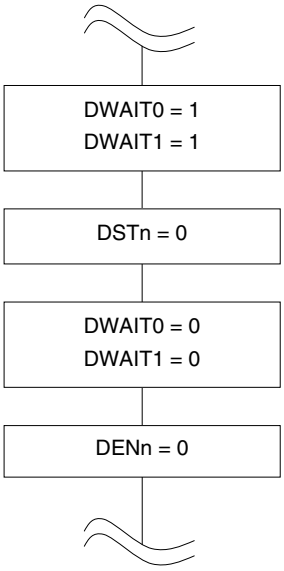
Remarks 1. n: DMA channel number (n = 0, 1)

2. 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

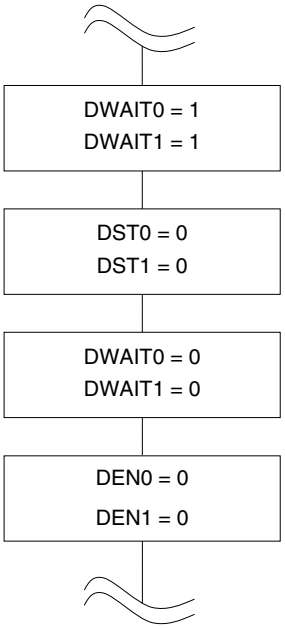
Figure 17-11. Forced Termination of DMA Transfer (2/2)

Example 3

- Procedure for forcibly terminating the DMA transfer for one channel if both channels are used



- Procedure for forcibly terminating the DMA transfer for both channels if both channels are used



Caution In example 3, the system is not required to wait two clock cycles after the DWAITn bit is set to 1. In addition, the system does not have to wait two clock cycles after clearing the DSTn bit to 0, because more than two clock cycles elapse from when the DSTn bit is cleared to 0 to when the DENn bit is cleared to 0.

Remarks 1. n: DMA channel number (n = 0, 1)

2. 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

17.6 Cautions on Using DMA Controller

(1) Priority of DMA

During DMA transfer, a request from the other DMA channel is held pending even if generated. The pending DMA transfer is started after the ongoing DMA transfer is completed. If two DMA requests are generated at the same time, however, DMA channel 0 takes priority over DMA channel 1.

If a DMA request and an interrupt request are generated at the same time, the DMA transfer takes precedence, and then interrupt servicing is executed.

(2) DMA response time

The response time of DMA transfer is as follows.

Table 17-2. Response Time of DMA Transfer

	Minimum Time	Maximum Time
Response time	3 clocks	10 clocks[Note]

Note The maximum time necessary to execute an instruction from internal RAM is 16 clock cycles.

Cautions 1. The above response time does not include the two clock cycles required for a DMA transfer.

2. When executing a DMA pending instruction (see 17.6 (4)), the maximum response time is extended by the execution time of that instruction to be held pending.

3. Do not specify successive transfer triggers for a channel within a period equal to the maximum response time plus one clock cycle, because they might be ignored.

Remark 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

(3) Operation in standby mode

The DMA controller operates as follows in the standby mode.

Table 17-3. DMA Operation in Standby Mode

Status	DMA Operation
HALT mode	Normal operation
STOP mode	Stops operation. If DMA transfer and STOP instruction execution contend, DMA transfer may be damaged. Therefore, stop DMA before executing the STOP instruction.

(4) DMA pending instruction

Even if a DMA request is generated, DMA transfer is held pending immediately after the following instructions.

- CALL !addr16
- CALL $!addr20
- CALL !!addr20
- CALL rp
- CALLT [addr5]
- BRK
- Bit manipulation instructions for registers IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H and PSW each.

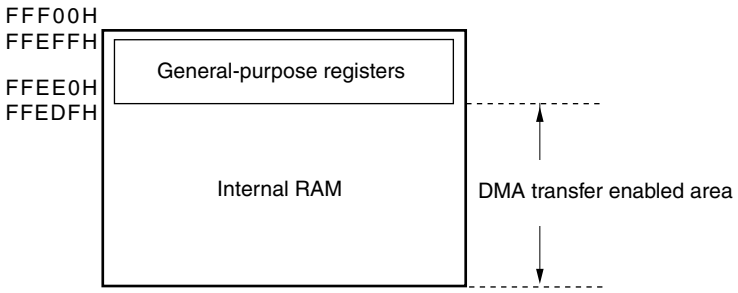
(5) Operation if address in general-purpose register area or other than those of internal RAM area is specified

The address indicated by DMA RAM address register n (DRAn) is incremented during DMA transfer. If the address is incremented to an address in the general-purpose register area or exceeds the area of the internal RAM, the following operation is performed.

- In mode of transfer from SFR to RAM
  The data of that address is lost.

- In mode of transfer from RAM to SFR
  Undefined data is transferred to SFR.

In either case, malfunctioning may occur or damage may be done to the system. Therefore, make sure that the address is within the internal RAM area other than the general-purpose register area.



CHAPTER 18 INTERRUPT FUNCTIONS

The number of interrupt sources differs, depending on the product.

<In case of the 78K0R/KC3-L, KD3-L, KE3-L>

		78K0R/KC3-L (40-pin)	78K0R/KC3-L (44-pin)	78K0R/KC3-L (48-pin)	78K0R/KD3-L	78K0R/KE3-L
Maskable interrupts	External	8	9	9	9	9
	Internal	22	24	25	25	25

<In case of the 78K0R/KF3-L, KG3-L>

		78K0R/KF3-L		78K0R/KG3-L	
		(μPD78F10xx : xx = 10, 11, 12)	(μPD78F10xx : xx = 27, 28)	(μPD78F10xx : xx = 13, 14)	(μPD78F10xx : xx = 29, 30)
Maskable interrupts	External	13			
	Internal	33	35	33	35

18.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into four priority groups by setting the priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H).

Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the priority of vectored interrupt servicing. For the priority order, see **Table 18-1**.

A standby release signal is generated and STOP and HALT modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

(2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

18.2 Interrupt Sources and Configuration

Interrupt sources include maskable interrupts and software interrupts. In addition, they also have up to five reset sources (see **Table 18-1**). The vector codes that store the program start address when branching due to the generation of a reset or various interrupt requests are two bytes each, so interrupts jump to a 64 K address of 00000H to 0FFFFH.

Table 18-1. Interrupt Source List (1/3)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
		Name	Trigger										
Maskable	0	INTWDTI	Watchdog timer interval Note 3 (75% of overflow time)	Internal	0004H	(A)	√	√	√	√	√	√	√
	1	INTLVI	Low-voltage detection Note 4		0006H		√	√	√	√	√	√	√
	2	INTP0	Pin input edge detection	External	0008H	(B)	√	√	√	√	√	√	√
	3	INTP1			000AH		√	√	√	√	√	√	√
	4	INTP2			000CH		√	√	√	√	√	√	√
	5	INTP3			000EH		√	√	√	√	√	√	√
	6	INTP4			0010H		√	√	√	√	√	√	√
	7	INTP5			0012H		√	√	√	√	√	√	√
	8	INTST3	UART3 transmission transfer end or buffer empty interrupt	Internal	0014H	(A)	–	–	–	–	–	√	√
	9	INTCMP0	CMP0 detection		0016H		√	√	√	√	√	–	–
		INTSR3	UART3 reception transfer end				–	–	–	–	–	√	√
	10	INTCMP1	CMP1 detection		0018H		√	√	√	√	√	–	–
		INTSRE3	UART3 reception communication error occurrence				–	–	–	–	–	√	√
	11	INTDMA0	End of DMA0 transfer		001AH		√	√	√	√	√	√	√
	12	INTDMA1	End of DMA1 transfer		001CH		√	√	√	√	√	√	√
	13	INTST0/ INTCSI00	UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt		001EH		√	√	√	√	√	√	√
	14	INTSR0/ INTCSI01	UART0 reception transfer end/CSI01 transfer end or buffer empty interrupt		0020H		√	√	√	√	√	√	√
	15	INTSRE0	UART0 reception communication error occurrence		0022H		√	√	√	√	√	√	√
	16	INTST1 /INTCSI10 /INTIIC10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt/IIC10 transfer end		0024H		√	√	√	√	√	√	√
	17	INTSR1	UART1 reception transfer end		0026H		√	√	√	√	√	√	√
	18	INTSRE1	UART1 reception communication error occurrence		0028H		√	√	√	√	√	√	√
	19	INTIICA	End of IICA communication		002AH		–	–	√	√	√	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts request occur simultaneously. Zero indicates the highest priority and 47 indicate the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 18-1.

3. When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.

4. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is cleared to 0.

Table 18-1. Interrupt Source List (2/3)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
		Name	Trigger										
Maskable	20	INTTM00	End of timer channel 0 count or capture	Internal	002CH	(A)	√	√	√	√	√	√	√
	21	INTTM01	End of timer channel 1 count or capture		002EH		√	√	√	√	√	√	√
	22	INTTM02	End of timer channel 2 count or capture		0030H		√	√	√	√	√	√	√
	23	INTTM03	End of timer channel 3 count or capture		0032H		√	√	√	√	√	√	√
	24	INTAD	End of A/D conversion		0034H		√	√	√	√	√	√	√
	25	INTRTC	Fixed-cycle signal of real-time counter/alarm match detection		0036H		–	√	√	√	√	√	√
	26	INTRTCI	Interval signal detection of real-time counter		0038H		–	√	√	√	√	√	√
	27	INTKR	Key return signal detection	External	003AH	(C)	√	√	√	√	√	√	√
	28	INTST2 /INTCSI20 /INTIIC20	UART2 transmission transfer end or buffer empty interrupt/CSI20 transfer end or buffer empty interrupt/IIC20 transfer end	Internal	003CH	(A)	–	–	–	–	–	√	√
	29	INTP6	Pin input edge detection	External	003EH	(B)	–	–	–	–	–	√	√
	30	INTTM13	End of timer channel 13 count or capture	Internal	0040H	(A)	–	–	–	–	–	√	√
		INTMD	End of division operation				√	√	√	√	√	–	–
	31	INTTM04	End of timer channel 4 count or capture		0042H		√	√	√	√	√	√	√
	32	INTTM05	End of timer channel 5 count or capture		0044H		√	√	√	√	√	√	√
	33	INTTM06	End of timer channel 6 count or capture		0046H		√	√	√	√	√	√	√
	34	INTTM07	End of timer channel 7 count or capture		0048H		√	√	√	√	√	√	√
	35	INTSR2	UART2 reception transfer end		004AH		–	–	–	–	–	√	√
		INTP6	Pin input edge detection	External		(B)	√	√	√	√	√	–	–
	36	INTP7			004CH		–	√	√	√	√	√	√
	37	INTP8			004EH		–	–	–	–	–	√	√
	38	INTP9			0050H		–	–	–	–	–	√	√
	39	INTP10			0052H		–	–	–	–	–	√	√
	40	INTSRE4 Note 3	UART4 reception communication error occurrence	Internal	0054H	(A)	–	–	–	–	–	Note 3	Note 3
		INTP11	Pin input edge detection	External		(B)	–	–	–	–	–	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 47 indicate the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 18-1.

3. INTSRE4 is only mounted in the 78K0R/KF3-L (μ PD78F1027 and 78F1028) and the 78K0R/KG3-L (μ PD78F1029 and 78F1030).

Table 18-1. Interrupt Source List (3/3)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
		Name	Trigger										
Maskable	41	INTTM10	End of timer channel 10 count or capture	Internal	0056H	(A)	–	–	–	–	–	√	√
	42	INTTM11	End of timer channel 11 count or capture		0058H		–	–	–	–	–	√	√
	43	INTTM12	End of timer channel 12 count or capture		005AH		–	–	–	–	–	√	√
	44	INTSRE2	UART2 reception communication error occurrence		005CH		–	–	–	–	–	√	√
	45	INTMD	End of A/D conversion		005EH		–	–	–	–	–	√	√
	46	INTST4 /INTCSI40	UART4 transmission transfer end or buffer empty interrupt/CSI40 transfer end or buffer empty interrupt		0060H		–	–	–	–	–	Note 3	Note 3
	47	INTSR4 /INTCSI41	UART4 reception transfer end/CSI41 transfer end or buffer empty interrupt		0062H		–	–	–	–	–	Note 3	Note 3
Software	–	BRK	Execution of BRK instruction	–	007EH	(D)	√	√	√	√	√	√	√
Reset	–	RESET	$\overline{\text{RESET}}$ pin input	–	0000H	–	√	√	√	√	√	√	√
		POC	Power-on-clear				√	√	√	√	√	√	√
		LVI	Low-voltage detection Note 4				√	√	√	√	√	√	√
		WDT	Overflow of watchdog timer				√	√	√	√	√	√	√
		TRAP	Execution of illegal instruction Note 5				√	√	√	√	√	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 47 indicate the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 18-1.

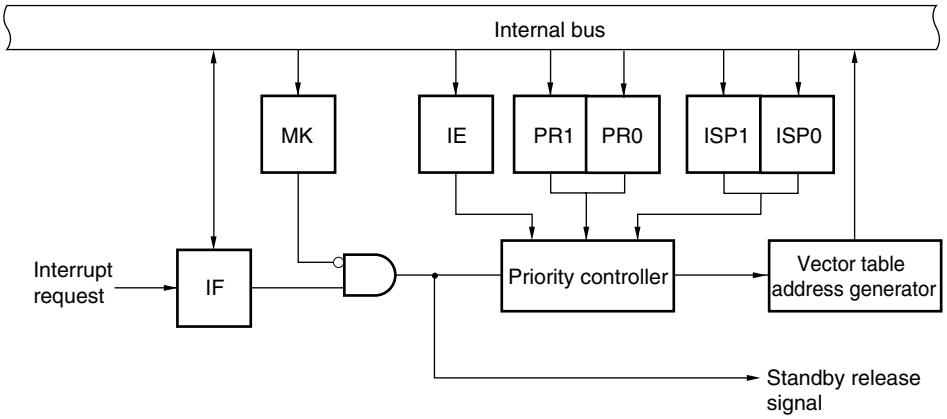
3. INTST4, INTCSI40, INTSR4, INTCSI41 are only mounted in the 78K0R/KF3-L (μPD78F1027 and 78F1028) and the 78K0R/KG3-L (μPD78F1029 and 78F1030).

4. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is set to 1.

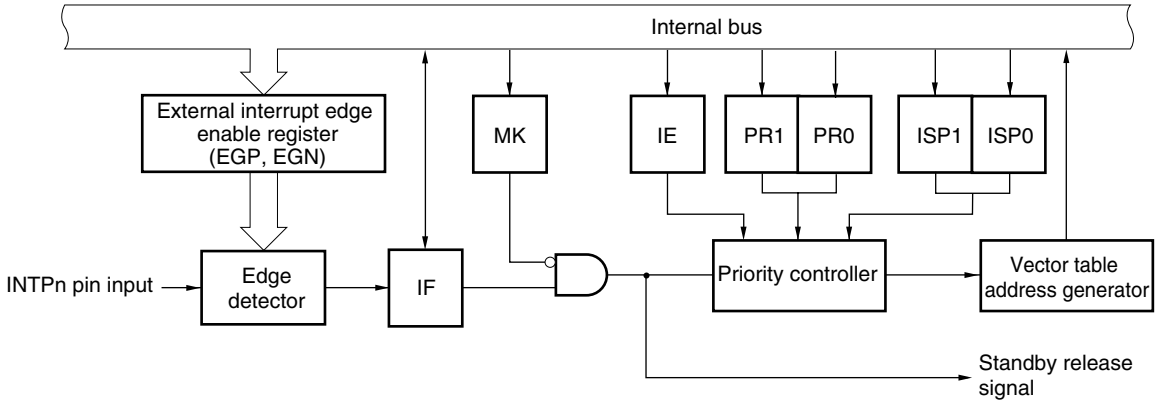
5. When the instruction code in FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Figure 18-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal maskable interrupt



(B) External maskable interrupt (INTPn)

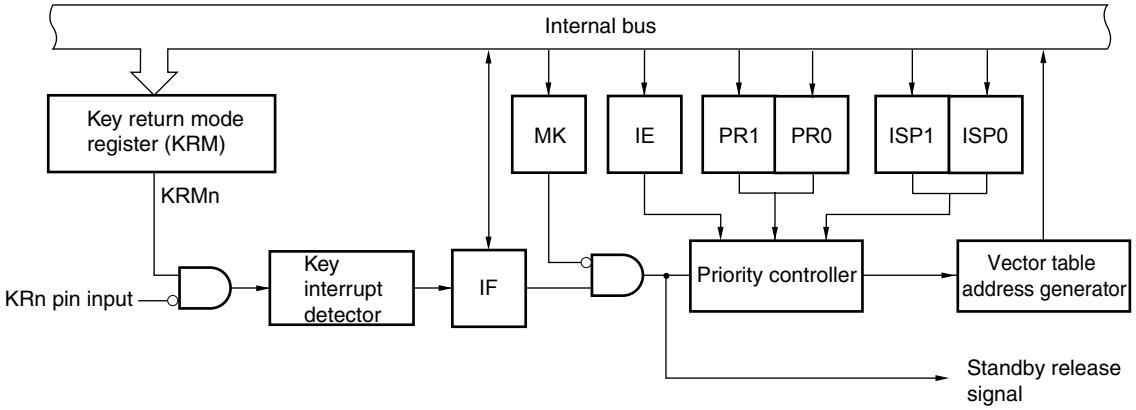


IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

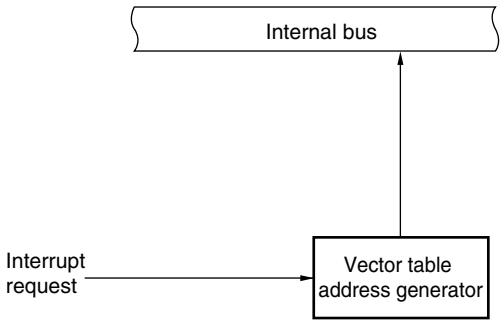
Remark 78K0R/KC3-L (40-pin): n = 0 to 6
78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, 78K0R/KE3-L: n = 0 to 7
78K0R/KF3-L, 78K0R/KG3-L: n = 0 to 11

Figure 18-1. Basic Configuration of Interrupt Function (2/2)

(C) External maskable interrupt (INTKR)



(D) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

Remark 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: n = 0 to 5
78K0R/KF3-L, 78K0R/KG3-L: n = 0 to 7

18.3 Registers Controlling Interrupt Functions (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L)
- Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L)
- Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, PR12L)
- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
- Program status word (PSW)

Table 18-2 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 18-2. Flags Corresponding to Interrupt Request Sources (1/2)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register
INTWDTI	WDTIIF	IF0L	WDTIMK	MK0L	WDTIPR0, WDTIPR1	PR00L, PR10L
INTLVI	LVIIF		LVIMK		LVIPR0, LVIPR1	
INTP0	PIF0		PMK0		PPR00, PPR10	
INTP1	PIF1		PMK1		PPR01, PPR11	
INTP2	PIF2		PMK2		PPR02, PPR12	
INTP3	PIF3		PMK3		PPR03, PPR13	
INTP4	PIF4		PMK4		PPR04, PPR14	
INTP5	PIF5		PMK5		PPR05, PPR15	
INTCMP0	CMPIF0	IF0H	CMPMK0	MK0H	CMPPR00, CMPPR10	PR00H, PR10H
INTCMP1	CMPIF1		CMPMK1		CMPPR01, CMPPR11	
INTDMA0	DMAIF0		DMAMK0		DMAPR00, DMAPR10	
INTDMA1	DMAIF1		DMAMK1		DMAPR01, DMAPR11	
INTST0[Note 1]	STIF0[Note 1]		STMK0[Note 1]		STPR00, STPR10[Note 1]	
INTCSI00[Note 1]	CSIIF00[Note 1]		CSIMK00[Note 1]		CSIPR000, CSIPR100[Note 1]	
INTSR0[Note 2]	SRIF0[Note 2]		SRMK0[Note 2]		SRPR00, SRPR10[Note 2]	
INTCSI01[Note 2]	CSIIF01[Note 2]		CSIMK01[Note 2]		CSIPR001, CSIPR101[Note 2]	
INTSRE0	SREIF0		SREMK0		SREPR00, SREPR10	

Notes 1. Do not use UART0 and CSI00 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INST0 and INTCSI00 is generated, bit 5 of the IF0H register is set to 1. Bit 5 of the MK0H, PR00H, and PR10H registers supports these two interrupt sources.

2. Do not use UART0 and CSI01 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INSR0 and INTCSI01 is generated, bit 6 of the IF0H register is set to 1. Bit 6 of the MK0H, PR00H, and PR10H registers supports these two interrupt sources.

Table 18-2. Flags Corresponding to Interrupt Request Sources (2/2)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register
INTST1 Note 1	STIF1 Note 1	IF1L	STMK1 Note 1	MK1L	STPR01, STPR11 Note 1	PR01L, PR11L
INTCSI10 Note 1	CSIIF10 Note 1		CSIMK10 Note 1		CSIPR010, CSIPR110 Note 1	
INTIIC10 Note 1	IICIF10 Note 1		IICMK10 Note 1		IICPR010, IICPR110 Note 1	
INTSR1	SRIF1		SRMK1		SRPR01, SRPR11	
INTSRE1	SREIF1		SREMK1		SREPR01, SREPR11	
INTIICA Note 2	IICAIF Note 2		IICAMK Note 2		IICAPR0, IICAPR1 Note 2	
INTTM00	TMIF00		TMMK00		TMPR000, TMPR100	
INTTM01	TMIF01		TMMK01		TMPR001, TMPR101	
INTTM02	TMIF02		TMMK02		TMPR002, TMPR102	
INTTM03	TMIF03		TMMK03		TMPR003, TMPR103	
INTAD	ADIF	IF1H	ADMK	MK1H	ADPR0, ADPR1	PR01H, PR11H
INTRTC Note 3	RTCIF Note 3		RTCMK Note 3		RTCPR0, RTCPR1 Note 3	
INTRTCI Note 3	RTCIIF Note 3		RTCIMK Note 3		RTCIPR0, RTCIPR1 Note 3	
INTKR	KRIF		KRMK		KRPR0, KRPR1	
INTMD	MDIF		MDMK		MDPR0, MDPR1	
INTTM04	TMIF04		TMMK04		TMPR004, TMPR104	
INTTM05	TMIF05	IF2L	TMMK05	MK2L	TMPR005, TMPR105	PR02L, PR12L
INTTM06	TMIF06		TMMK06		TMPR006, TMPR106	
INTTM07	TMIF07		TMMK07		TMPR007, TMPR107	
INTP6	PIF6		PMK6		PPR06, PPR16	
INTP7 Note 3	PIF7 Note 3		PMK7 Note 3		PPR07, PPR17 Note 3	

Notes 1. Do not use UART1, CSI10, and IIC10 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTST1, INTCSI10, and INTIIC10 is generated, bit 0 of the IF1L register is set to 1. Bit 0 of the MK1L, PR01L, and PR11L registers supports these three interrupt sources.

2. Those interrupt sources are not provided in the 40-pin and 44-pin products of the 78K0R/KC3-L.

3. Those interrupt sources are not provided in the 40-pin product of the 78K0R/KC3-L.

(1) Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L)

The interrupt request flags are set to 1 when the corresponding interrupt request is generated or an instruction is executed. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is entered.

The IF0L, IF0H, IF1L, IF1H, and IF2L registers can be set by a 1-bit or 8-bit memory manipulation instruction. When the IF0L and IF0H, and IF1L and IF1H registers are combined to form 16-bit registers IF0 and IF1, they can be set by a 16-bit memory manipulation instruction. Using the IF2L register as the IF2 register can be set also by using a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 18-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L) (1/2)

Address: FFFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF

Address: FFFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	0
IF0H	SREIF0	SRIF0 CSIIF01	STIF0 CSIIF00	DMAIF1	DMAIF0	CMPIF1	CMPIF0	0

Address: FFFE2H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF1L	TMIF03	TMIF02	TMIF01	TMIF00	IICAIF Note 1	SREIF1	SRIF1	STIF1 CSIIF10 IICIF10

Address: FFFE3H After reset: 00H R/W

Symbol	<7>	<6>	5	4	<3>	<2>	<1>	<0>
IF1H	TMIF04	MDIF	0	0	KRIF	RTCIIF Note 2	RTCIF Note 2	ADIF

Address: FFFD0H After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
IF2L	0	0	0	PIF7 Note 2	PIF6	TMIF07	TMIF06	TMIF05

Notes 1. That bit is not provided in the 40-pin and 44-pin products of the 78K0R/KC3-L.

2. Those bits are not provided in the 40-pin product of the 78K0R/KC3-L.

(**Caution** is listed on the next page.)

Figure 18-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L) (2/2)

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Cautions 1. Be sure to clear bit 0 of the IF0H register, bits 4 and 5 of the IF1H register (in case of 78K0R/KC3-L (40-pin), bits 1, 2, 4, and 5), and bits 5 to 7 of the IF2L register (in case of 78K0R/KC3-L (40-pin), bits 4 to 7) to 0.

2. When operating a timer, serial interface, or A/D converter after standby release, operate it once after clearing the interrupt request flag. An interrupt request flag may be set by noise.

3. When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as "IF0L.0 = 0;" or "_asm("clr1 IF0L, 0");" because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).

If a program is described in C language using an 8-bit memory manipulation instruction such as "IF0L &= 0xfe;" and compiled, it becomes the assembler of three instructions.

```
mov a, IF0L
and a, #0FEH
mov IF0L, a
```

In this case, even if the request flag of another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between "mov a, IF0L" and "mov IF0L, a", the flag is cleared to 0 at "mov IF0L, a". Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.

(2) Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L)

The interrupt mask flags are used to enable/disable the corresponding maskable interrupt servicing.

The MK0L, MK0H, MK1L, MK1H, and MK2L registers can be set by a 1-bit or 8-bit memory manipulation instruction.

When the MK0L and MK0H, and MK1L and MK1H registers are combined to form 16-bit registers MK0 and MK1, they can be set by a 16-bit memory manipulation instruction. Using the MK2L register as the MK2 register can be set also by using a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 18-3. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L)

Address: FFFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	0
MK0H	SREMK0	SRMK0 CSIMK01	STMK0 CSIMK00	DMAMK1	DMAMK0	CMPMK1	CMPMK0	1

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	IICAMK Note 1	SREMK1	SRMK1	STMK1 CSIMK10 IICMK10

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	<6>	5	4	<3>	<2>	<1>	<0>
MK1H	TMMK04	MDMK	1	1	KRMK	RTCIMK Note 2	RTCMK Note 2	ADMK

Address: FFFD4H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
MK2L	1	1	1	PMK7 Note 2	PMK6	TMMK07	TMMK06	TMMK05

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Notes 1. That bit is not provided in the 40-pin and 44-pin products of the 78K0R/KC3-L.

2. Those bits are not provided in the 40-pin product of the 78K0R/KC3-L.

Caution Be sure to set bit 0 of the MK0H register, bits 4 and 5 of the MK1H register (in case of 78K0R/KC3-L (40-pin), bits 1, 2, 4, and 5), and bits 5 to 7 of the MK2L register (in case of 78K0R/KC3-L (40-pin), bits 4 to 7) to 1.

(3) Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, PR12L)

The priority specification flag registers are used to set the corresponding maskable interrupt priority level.

A priority level is set by using the PR0xy and PR1xy registers in combination (xy = 0L, 0H, 1L, 1H, or 2L).

The PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, and PR12L registers can be set by a 1-bit or 8-bit memory manipulation instruction. If the PR00L and PR00H, PR01L and PR01H, PR10L and PR10H, and PR11L and PR11H registers are combined to form 16-bit registers PR00, PR01, PR10, and PR11, they can be set by a 16-bit memory manipulation instruction. Using the PR02L register as the PR02 register and the PR12L register as the PR12 register can be set also by using a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 18-4. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, PR12L) (1/2)

Address: FFFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00L	PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10L	PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	0
PR00H	SREPR00	SRPR00 CSIPR001	STPR00 CSIPR000	DMAPR01	DMAPR00	CMPPR01	CMPPR00	1

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	0
PR10H	SREPR10	SRPR10 CSIPR101	STPR10 CSIPR100	DMAPR11	DMAPR10	CMPPR11	CMPPR10	1

Figure 18-4. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, PR12L) (2/2)

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	IICAPR0 Note 1	SREPR01	SRPR01	STPR01 CSIPR010 IICPR010

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	IICAPR1 Note 1	SREPR11	SRPR11	STPR11 CSIPR110 IICPR110

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	<6>	5	4	<3>	<2>	<1>	<0>
PR01H	TMPR004	MDPR0	1	1	KRPR0	RTCIPR0 Note 2	RTCPR0 Note 2	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	<6>	5	4	<3>	<2>	<1>	<0>
PR11H	TMPR104	MDPR1	1	1	KRPR1	RTCIPR1 Note 2	RTCPR1 Note 2	ADPR1

Address: FFFD8H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PR02L	1	1	1	PPR07 Note 2	PPR06	TMPR007	TMPR006	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PR12L	1	1	1	PPR17 Note 2	PPR16	TMPR107	TMPR106	TMPR105

XXPR1X	XXPR0X	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Notes 1. Those bits are not provided in the 40-pin and 44-pin products of the 78K0R/KC3-L.

2. Those bits are not provided in the 40-pin product of the 78K0R/KC3-L.

Caution Be sure to set bit 0 of the PR00H and PR10H registers, bits 4 and 5 of the PR01H and PR11H registers (in case of 78K0R/KC3-L (40-pin), bits 1, 2, 4, and 5), and bits 5 to 7 of the PR02L and PR12L registers (in case of 78K0R/KC3-L (40-pin), bits 4 to 7) to 1.

(4) External interrupt rising edge enable register 0 (EGP0), external interrupt falling edge enable register 0 (EGN0)

These registers specify the valid edge for INTP0 to INTP7[Note].

The EGP0 and EGN0 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 18-5. Format of External Interrupt Rising Edge Enable Register 0 (EGP0) and External Interrupt Falling Edge Enable Register 0 (EGN0)

Address: FFF38H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP0	EGP7[Note]	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FFF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN0	EGN7[Note]	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection (n = 0 to 7[Note])
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Table 18-3 shows the ports corresponding to the EGPn and EGNn bits.

Table 18-3. Ports Corresponding to EGPn and EGNn Bits

Detection Enable Bit		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P120	INTP0
EGP1	EGN1	P31	INTP1
EGP2	EGN2	P32	INTP2
EGP3	EGN3	P80	INTP3
EGP4	EGN4	P70	INTP4
EGP5	EGN5	P71	INTP5
EGP6	EGN6	P72	INTP6
EGP7[Note]	EGN7[Note]	P82[Note]	INTP7[Note]

Note Those are not provided in the 40-pin product of the 78K0R/KC3-L.

Caution Select the port mode by clearing the EGPn and EGNn bits to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark 78K0R/KC3-L (40-pin): n = 0 to 6
78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, 78K0R/KE3-L: n = 0 to 7
78K0R/KF3-L, 78K0R/KG3-L: n = 0 to 7

(5) Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for an interrupt request. The IE flag that sets maskable interrupt enable/disable and the ISP0 and ISP1 flags that controls multiple interrupt servicing are mapped to the PSW.

Besides 8-bit read/write, this register can carry out operations using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged, if the BRK instruction is executed, the contents of the PSW are automatically saved into a stack and the IE flag is reset to 0. If a maskable interrupt request is acknowledged, the ISP1 and ISP0 flags are set according to the priority specification level of the acknowledged interrupt. The PSW contents are also saved into the stack with the PUSH PSW instruction. They are restored from the stack with the RETI, RETB, and POP PSW instructions.

Reset signal generation sets the PSW register to 06H.

Figure 18-6. Configuration of Program Status Word

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	0	After reset
PSW	IE	Z	RBS1	AC	RBS0	ISP1	ISP0	CY	06H

Used when normal instruction is executed

ISP1	ISP0	Priority of interrupt currently being serviced
0	0	Enables interrupt of level 0 (while interrupt of level 1 or 0 is being serviced).
0	1	Enables interrupt of level 0 and 1 (while interrupt of level 2 is being serviced).
1	0	Enables interrupt of level 0 to 2 (while interrupt of level 3 is being serviced).
1	1	Enables all interrupts (waits for acknowledgment of an interrupt).

IE	Interrupt request acknowledgment enable/disable
0	Disabled
1	Enabled

18.4 Registers Controlling Interrupt Functions (78K0R/KF3-L, 78K0R/KG3-L)

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)
- Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)
- Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H)
- External interrupt rising edge enable registers (EGP0, EGP1)
- External interrupt falling edge enable registers (EGN0, EGN1)
- Program status word (PSW)

Table 18-4 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 18-4. Flags Corresponding to Interrupt Request Sources (1/3)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDTI	WDTIIF	IF0L	WDTIMK	MK0L	WDTIPR0, WDTIPR1	PR00L, PR10L
INTLVI	LVIIF		LVIMK		LVIPR0, LVIPR1	
INTP0	PIF0		PMK0		PPR00, PPR10	
INTP1	PIF1		PMK1		PPR01, PPR11	
INTP2	PIF2		PMK2		PPR02, PPR12	
INTP3	PIF3		PMK3		PPR03, PPR13	
INTP4	PIF4		PMK4		PPR04, PPR14	
INTP5	PIF5		PMK5		PPR05, PPR15	
INTST3	STIF3	IF0H	STMK3	MK0H	STPR03, STPR13	PR00H, PR10H
INTSR3	SRIF3		SRMK3		SRPR03, SRPR13	
INTSRE3	SREIF3		SREMK3		SREPR03, SREPR13	
INTDMA0	DMAIF0		DMAMK0		DMAPR00, DMAPR10	
INTDMA1	DMAIF1		DMAMK1		DMAPR01, DMAPR11	
INTST0[Note 1]	STIF0[Note 1]		STMK0[Note 1]		STPR00, STPR10[Note 1]	
INTCSI00[Note 1]	CSIIF00[Note 1]		CSIMK00[Note 1]		CSIPR000, CSIPR100[Note 1]	
INTSR0[Note 2]	SRIF0[Note 2]		SRMK0[Note 2]		SRPR00, SRPR10[Note 2]	
INTCSI01[Note 2]	CSIIF01[Note 2]		CSIMK01[Note 2]		CSIPR001, CSIPR101[Note 2]	
INTSRE0	SREIF0		SREMK0		SREPR00, SREPR10	

Notes 1. Do not use UART0 and CSI00 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTST0 and INTCSI00 is generated, bit 5 of the IF0H register is set to 1. Bit 5 of the MK0H, PR00H, and PR10H registers supports these three interrupt sources.

2. Do not use UART0 and CSI01 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTSR0 and INTCSI01 is generated, bit 6 of the IF0H register is set to 1. Bit 6 of the MK0H, PR00H, and PR10H registers supports these three interrupt sources.

Table 18-4. Flags Corresponding to Interrupt Request Sources (2/3)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register
INTST1[Note 1]	STIF1[Note 1]	IF1L	STMK1[Note 1]	MK1L	STPR01, STPR11[Note 1]	PR01L, PR11L
INTCSI10[Note 1]	CSIIF10[Note 1]		CSIMK10[Note 1]		CSIPR010, CSIPR110[Note 1]	
INTIIC10[Note 1]	IICIF10[Note 1]		IICMK10[Note 1]		IICPR010, IICPR110[Note 1]	
INTSR1	SRIF1		SRMK1		SRPR01, SRPR11	
INTSRE1	SREIF1		SREMK1		SREPR01, SREPR11	
INTIICA	IICAIF		IICAMK		IICAPR0, IICAPR1	
INTTM00	TMIF00		TMMK00		TMPR000, TMPR100	
INTTM01	TMIF01		TMMK01		TMPR001, TMPR101	
INTTM02	TMIF02		TMMK02		TMPR002, TMPR102	
INTTM03	TMIF03		TMMK03		TMPR003, TMPR103	
INTAD	ADIF	IF1H	ADMK	MK1H	ADPR0, ADPR1	PR01H, PR11H
INTRTC	RTCIF		RTCMK		RTCPR0, RTCPR1	
INTRTCI	RTCIIF		RTCIMK		RTCIPR0, RTCIPR1	
INTKR	KRIF		KRMK		KRPR0, KRPR1	
INTST2[Note 2]	STIF2[Note 2]		STMK2[Note 2]		STPR02, STPR12[Note 2]	
INTCSI20[Note 2]	CSIIF20[Note 2]		CSIMK20[Note 2]		CSIPR020, CSIPR120[Note 2]	
INTIIC20[Note 2]	IICIF20[Note 2]		IICMK20[Note 2]		IICPR020, IICPR120[Note 2]	
INTP6	PIF6		PMK6		PPR06, PPR16	
INTTM13	TMIF13		TMMK13		TMPR013, TMPR113	
INTTM04	TMIF04		TMMK04		TMPR004, TMPR104	
INTTM05	TMIF05	IF2L	TMMK05	MK2L	TMPR005, TMPR105	PR02L, PR12L
INTTM06	TMIF06		TMMK06		TMPR006, TMPR106	
INTTM07	TMIF07		TMMK07		TMPR007, TMPR107	
INTSR2	SRIF2		SRMK2		SRPR02, SRPR12	
INTP7	PIF7		PMK7		PPR07, PPR17	
INTP8	PIF8		PMK8		PPR08, PPR18	
INTP9	PIF9		PMK9		PPR09, PPR19	
INTP10	PIF10		PMK10		PPR010, PPR110	

Notes 1. Do not use UART1, CSI10, and IIC10 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTST1, INTCSI10, and INTIIC10 is generated, bit 0 of the IF1L register is set to 1. Bit 0 of the MK1L, PR01L, and PR11L registers supports these three interrupt sources.

2. Do not use UART2, CSI20, and IIC20 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTST2, INTCSI20, and INTIIC20 is generated, bit 4 of the IF1H register is set to 1. Bit 4 of the MK1H, PR01H, and PR11H registers supports these three interrupt sources.

Table 18-4. Flags Corresponding to Interrupt Request Sources (3/3)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTP11	PIF11	IF2H	PMK11	MK2H	PPR011, PPR111	PR02H, PR12H
INTSRE4[Note]	SREIF4[Note]		SREMK4[Note]		SREPR04, SREPR14[Note]	
INTTM10	TMIF10		TMMK10		TMPR010, TMPR110	
INTTM11	TMIF11		TMMK11		TMPR011, TMPR111	
INTTM12	TMIF12		TMMK12		TMPR012, TMPR112	
INTSRE2	SREIF2		SREMK2		SREPR02, SREPR12	
INTMD	MDIF		MDMK		MDPR0, MDPR1	
INTST4[Note]	STIF4[Note]		STMK4[Note]		STPR04, STPR14[Note]	
INTCSI40[Note]	CSIIF40[Note]		CSIMK40[Note]		CSIPR040, CSIPR140[Note]	
INTSR4[Note]	SRIF4[Note]		SRMK4[Note]		SRPR04, SRPR14[Note]	
INTCSI41[Note]	CSIIF41[Note]		CSIMK41[Note]		CSIPR041, CSIPR141[Note]	

Note Those are only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

(1) Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)

The interrupt request flags are set to 1 when the corresponding interrupt request is generated or an instruction is executed. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is entered.

The IF0L, IF0H, IF1L, IF1H, IF2L, and IF2H registers can be set by a 1-bit or 8-bit memory manipulation instruction. When the IF0L and IF0H registers, the IF1L and IF1H registers, and the IF2L and IF2H registers are combined to form 16-bit registers IF0, IF1, and IF2, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 18-7. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H) (1/2)

Address: FFFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF

Address: FFFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	SREIF0	SRIF0 CSIIF01	STIF0 CSIIF00	DMAIF1	DMAIF0	SREIF3	SRIF3	STIF3

Address: FFFE2H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF1L	TMIF03	TMIF02	TMIF01	TMIF00	IICAIF	SREIF1	SRIF1	STIF1 CSIIF10 IICIF10

Address: FFFE3H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF1H	TMIF04	TMIF13	PIF6	STIF2 CSIIF20 IICIF20	KRIF	RTCIIF	RTCIF	ADIF

Address: FFFD0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF2L	PIF10	PIF9	PIF8	PIF7	SRIF2	TMIF07	TMIF06	TMIF05

Figure 18-7. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H) (2/2)

Address: FFFD1H After reset: 00H R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
IF2H	SRIF4 CSIIF41[Note]	STIF4 CSIIF40[Note]	MDIF	SREIF2	TMIF12	TMIF11	TMIF10	PIF11 SREIF4[Note]

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Note Those are only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

Cautions 1. Be sure to clear bits 6 and 7 of the IF2H register to 0 (except for μPD78F1027, 78F1028, 78F1029, 78F1030).

2. When operating a timer, serial interface, or A/D converter after standby release, operate it once after clearing the interrupt request flag. An interrupt request flag may be set by noise.

3. When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as "IF0L.0 = 0;" or "_asm("clr1 IF0L, 0");" because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).

If a program is described in C language using an 8-bit memory manipulation instruction such as "IF0L &= 0xfe;" and compiled, it becomes the assembler of three instructions.

```
mov a, IF0L
and a, #0FEH
mov IF0L, a
```

In this case, even if the request flag of the another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between "mov a, IF0L" and "mov IF0L, a", the flag is cleared to 0 at "mov IF0L, a". Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.

(2) Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)

The interrupt mask flags are used to enable/disable the corresponding maskable interrupt servicing.

The MK0L, MK0H, MK1L, MK1H, MK2L, and MK2H registers can be set by a 1-bit or 8-bit memory manipulation instruction. When the MK0L and MK0H registers, the MK1L and MK1H registers, and the MK2L and MK2H registers are combined to form 16-bit registers MK0, MK1, and MK2, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 18-8. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)

Address: FFFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	SREMK0	SRMK0 CSIMK01	STMK0 CSIMK00	DMAMK1	DMAMK0	SREMK3	SRMK3	STMK3

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	IICAMK	SREMK1	SRMK1	STMK1 CSIMK10 IICMK10

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1H	TMMK04	TMMK13	PMK6	STMK2 CSIMK20 IICMK20	KRMK	RTCIMK	RTCMK	ADMK

Address: FFFD4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK2L	PMK10	PMK9	PMK8	PMK7	SRMK2	TMMK07	TMMK06	TMMK05

Address: FFFD5H After reset: FFH R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
MK2H	SRMK4[Note] CSIMK41[Note]	STMK4[Note] CSIMK40[Note]	MDMK	SREMK2	TMMK12	TMMK11	TMMK10	PMK11 SREMK4[Note]

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note Those are only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

Caution Be sure to set bits 6 and 7 of the MK2H register to 1 (except for μPD78F1027, 78F1028, 78F1029, 78F1030).

(3) Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H)

The priority specification flag registers are used to set the corresponding maskable interrupt priority level.

A priority level is set by using the PR0xy and PR1xy registers in combination (xy = 0L, 0H, 1L, 1H, 2L, or 2H).

The PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, and the PR12H registers can be set by a 1-bit or 8-bit memory manipulation instruction. If the PR00L and PR00H registers, the PR01L and PR01H registers, the PR02L and PR02H registers, the PR10L and PR10H registers, the PR11L and PR11H registers, and the PR12L and PR12H registers are combined to form 16-bit registers PR00, PR01, PR02, PR10, PR11, and PR12, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 18-9. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H) (1/2)

Address: FFFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00L	PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10L	PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	SREPR00	SRPR00 CSIPR001	STPR00 CSIPR000	DMAPR01	DMAPR00	SREPR03	SRPR03	STPR03

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	SREPR10	SRPR10 CSIPR101	STPR10 CSIPR100	DMAPR11	DMAPR10	SREPR13	SRPR13	STPR13

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	IICAPR0	SREPR01	SRPR01	STPR01 CSIPR010 IICPR010

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	IICAPR1	SREPR11	SRPR11	STPR11 CSIPR110 IICPR110

Figure 18-9. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H) (2/2)

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR01H	TMPR004	TMPR013	PPR06	STPR02 CSIPR020 IICPR020	KRPR0	RTCIPR0	RTCPR0	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR11H	TMPR104	TMPR113	PPR16	STPR12 CSIPR120 IICPR120	KRPR1	RTCIPR1	RTCPR1	ADPR1

Address: FFFD8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR02L	PPR010	PPR09	PPR08	PPR07	SRPR02	TMPR007	TMPR006	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR12L	PPR110	PPR19	PPR18	PPR17	SRPR12	TMPR107	TMPR106	TMPR105

Address: FFFD9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR02H	SRPR04 CSIPR041Note	STPR04 CSIPR040Note	MDPR0	SREPR02	TMPR012	TMPR011	TMPR010	PPR011 SREPER04 Note

Address: FFFDDH After reset: FFH R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
PR12H	SRPR14 CSIPR141Note	STPR14 CSIPR140Note	MDPR1	SREPR12	TMPR112	TMPR111	TMPR110	PPR111 SREPER14 Note

XXPR1X	XXPR0X	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Note Those are only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

Caution Be sure to set bits 6 and 7 of the PR02H and PR12H registers to 1 (except for μPD78F1027, 78F1028, 78F1029, 78F1030).

(4) External interrupt rising edge enable registers (EGP0, EGP1), external interrupt falling edge enable registers (EGN0, EGN1)

These registers specify the valid edge for INTP0 to INTP11.

The EGP0, EGP1, EGN0, and EGN1 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 18-10. Format of External Interrupt Rising Edge Enable Registers (EGP0, EGP1) and External Interrupt Falling Edge Enable Registers (EGN0, EGN1)

Address: FFF38H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP0	EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FFF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN0	EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

Address: FFF3AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP1	0	0	0	0	EGP11	EGP10	EGP9	EGP8

Address: FFF3BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN1	0	0	0	0	EGN11	EGN10	EGN9	EGN8

EGPn	EGNn	INTPn pin valid edge selection (n = 0 to 11)
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Table 18-5 shows the ports corresponding to the EGPn and EGNn bits.

Table 18-5. Ports Corresponding to EGPn and EGNn bits

Detection Enable Bit		Edge Detection Port		Interrupt Request Signal
		78K0R/KF3-L	78K0R/KG3-L	
EGP0	EGN0	P120	P120	INTP0
EGP1	EGN1	P50	P46	INTP1
EGP2	EGN2	P51	P47	INTP2
EGP3	EGN3	P30	P30	INTP3
EGP4	EGN4	P31	P31	INTP4
EGP5	EGN5	P16	P16	INTP5
EGP6	EGN6	P140	P140	INTP6
EGP7	EGN7	P55	P141	INTP7
EGP8	EGN8	P74	P74	INTP8
EGP9	EGN9	P75	P75	INTP9
EGP10	EGN10	P76	P76	INTP10
EGP11	EGN11	P77	P77	INTP11

Caution Select the port mode by clearing the EGPn and EGNn bits to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0 to 11

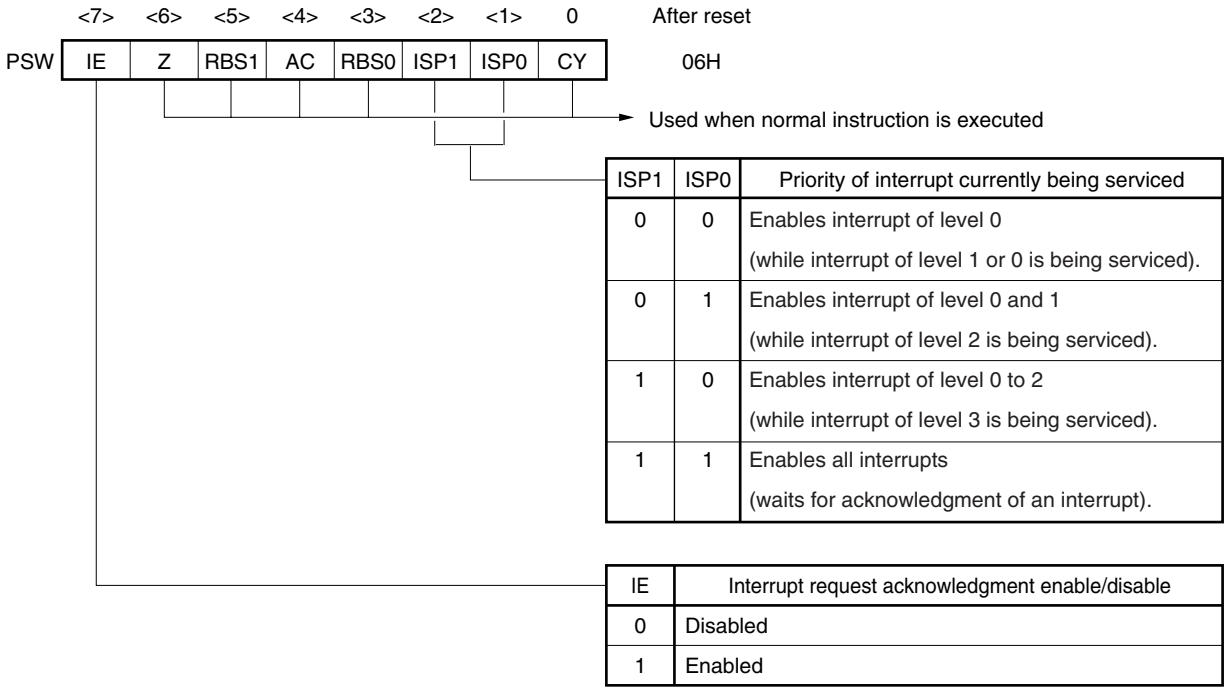
(5) Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for an interrupt request. The IE flag that sets maskable interrupt enable/disable and the ISP0 and ISP1 flags that controls multiple interrupt servicing are mapped to the PSW.

Besides 8-bit read/write, this register can carry out operations using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged, if the BRK instruction is executed, the contents of the PSW are automatically saved into a stack and the IE flag is reset to 0. If a maskable interrupt request is acknowledged, the contents of the priority specification flag of the acknowledged interrupt are transferred to the ISP0 and ISP1 flags. The PSW contents are also saved into the stack with the PUSH PSW instruction. They are restored from the stack with the RETI, RETB, and POP PSW instructions.

Reset signal generation sets PSW to 06H.

Figure 18-11. Configuration of Program Status Word



ISP1	ISP0	Priority of interrupt currently being serviced
0	0	Enables interrupt of level 0 (while interrupt of level 1 or 0 is being serviced).
0	1	Enables interrupt of level 0 and 1 (while interrupt of level 2 is being serviced).
1	0	Enables interrupt of level 0 to 2 (while interrupt of level 3 is being serviced).
1	1	Enables all interrupts (waits for acknowledgment of an interrupt).

IE	Interrupt request acknowledgment enable/disable
0	Disabled
1	Enabled

18.5 Interrupt Servicing Operations

18.5.1 Maskable interrupt request acknowledgment

A maskable interrupt request becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request.

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 18-6 below.

For the interrupt request acknowledgment timing, see **Figures 18-13** and **18-14**.

Table 18-6. Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time[Note]
Servicing time	9 clocks	14 clocks

Note If an interrupt request is generated just before the RET instruction, the wait time becomes longer.

Remark 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

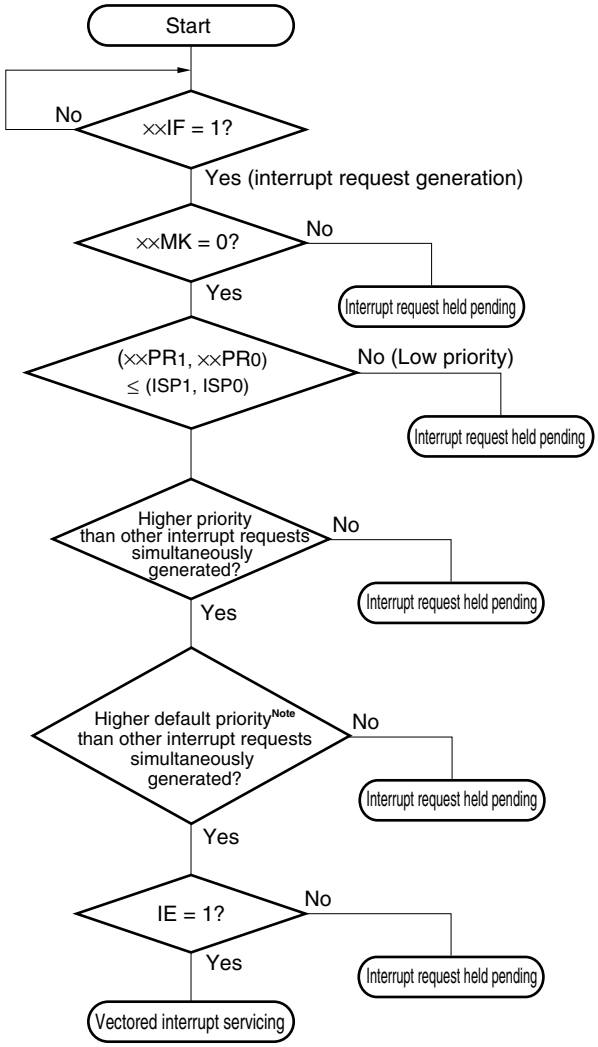
An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

Figure 18-12 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP1 and ISP0 flags. The vector table data determined for each interrupt request is the loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

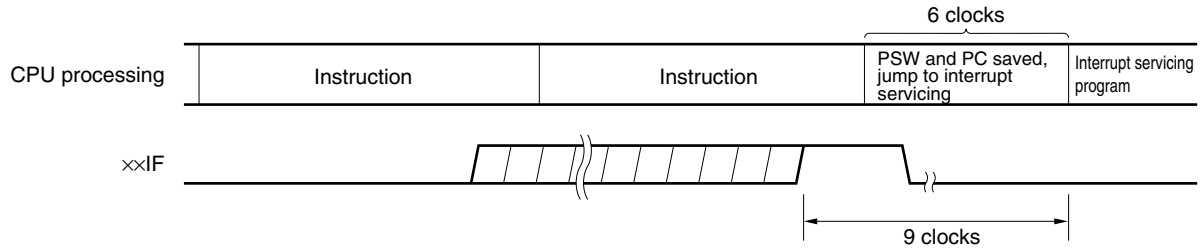
Figure 18-12. Interrupt Request Acknowledgment Processing Algorithm



××IF: Interrupt request flag
××MK: Interrupt mask flag
××PR0: Priority specification flag 0
××PR1: Priority specification flag 1
IE: Flag that controls acknowledgment of maskable interrupt request (1 = Enable, 0 = Disable)
ISP0, ISP1: Flag that indicates the priority level of the interrupt currently being serviced (see **Figure 18-6** and **18-11**)

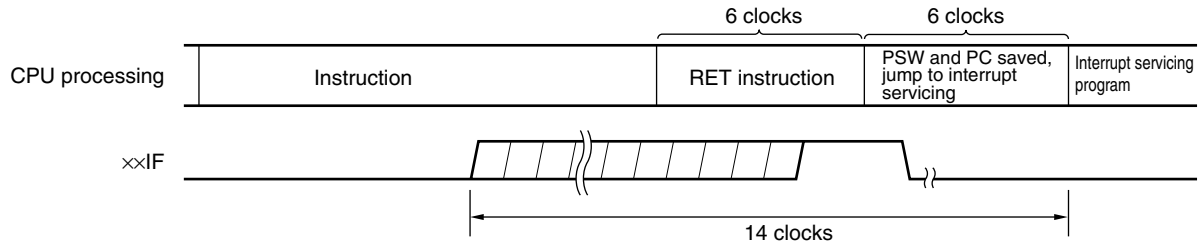
Note For the default priority, refer to **Table 18-1 Interrupt Source List**.

Figure 18-13. Interrupt Request Acknowledgment Timing (Minimum Time)



Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

Figure 18-14. Interrupt Request Acknowledgment Timing (Maximum Time)



Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

18.5.2 Software interrupt request acknowledgment

A software interrupt request is acknowledged by BRK instruction execution. Software interrupts cannot be disabled.

If a software interrupt request is acknowledged, the contents are saved into the stacks in the order of the program status word (PSW), then program counter (PC), the IE flag is reset (0), and the contents of the vector table (0007EH, 0007FH) are loaded into the PC and branched.

Restoring from a software interrupt is possible by using the RETB instruction.

Caution Do not use the RETI instruction for restoring from the software interrupt.

18.5.3 Multiple interrupt servicing

Multiple interrupt servicing occurs when another interrupt request is acknowledged during execution of an interrupt.

Multiple interrupt servicing does not occur unless the interrupt request acknowledgment enabled state is selected (IE = 1). When an interrupt request is acknowledged, interrupt request acknowledgment becomes disabled (IE = 0). Therefore, to enable multiple interrupt servicing, it is necessary to set (1) the IE flag with the EI instruction during interrupt servicing to enable interrupt acknowledgment.

Moreover, even if interrupts are enabled, multiple interrupt servicing may not be enabled, this being subject to interrupt priority control. Two types of priority control are available: default priority control and programmable priority control. Programmable priority control is used for multiple interrupt servicing.

In the interrupt enabled state, if an interrupt request with a priority equal to or higher than that of the interrupt currently being serviced is generated, it is acknowledged for multiple interrupt servicing. If an interrupt with a priority lower than that of the interrupt currently being serviced is generated during interrupt servicing, it is not acknowledged for multiple interrupt servicing. Interrupt requests that are not enabled because interrupts are in the interrupt disabled state or because they have a lower priority are held pending. When servicing of the current interrupt ends, the pending interrupt request is acknowledged following execution of at least one main processing instruction execution.

Table 18-5 shows relationship between interrupt requests enabled for multiple interrupt servicing and Figure 18-15 shows multiple interrupt servicing examples.

Table 18-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0, ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0, ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1, ISP0 = 0	○	×	○	×	○	×	×	×	○
	ISP1 = 1, ISP0 = 1	○	×	○	×	○	×	○	×	○
Software interrupt		○	×	○	×	○	×	○	×	○

Remarks 1. ○: Multiple interrupt servicing enabled

2. ×: Multiple interrupt servicing disabled

3. ISP0, ISP1, and IE are flags contained in the PSW.

ISP1 = 0, ISP0 = 0: An interrupt of level 1 or level 0 is being serviced.

ISP1 = 0, ISP0 = 1: An interrupt of level 2 is being serviced.

ISP1 = 1, ISP0 = 0: An interrupt of level 3 is being serviced.

ISP1 = 1, ISP0 = 1: Wait for An interrupt acknowledgment.

IE = 0: Interrupt request acknowledgment is disabled.

IE = 1: Interrupt request acknowledgment is enabled.

4. PR is a flag contained in the PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, and PR12H registers.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)

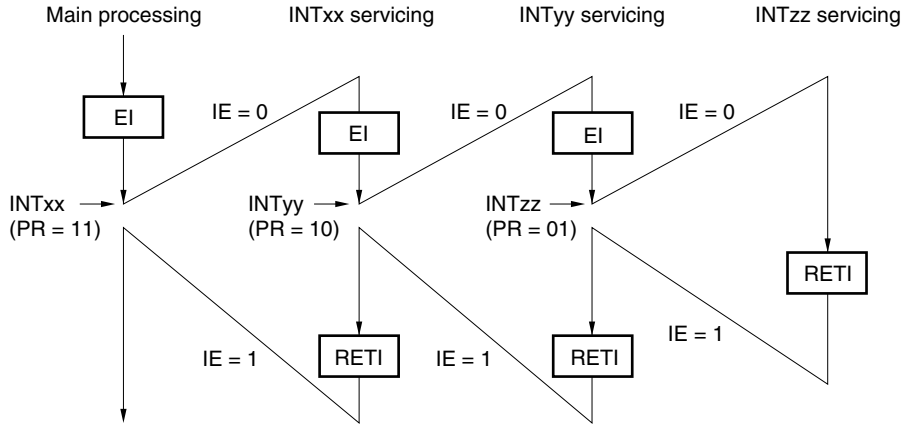
PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1

PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0

PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)

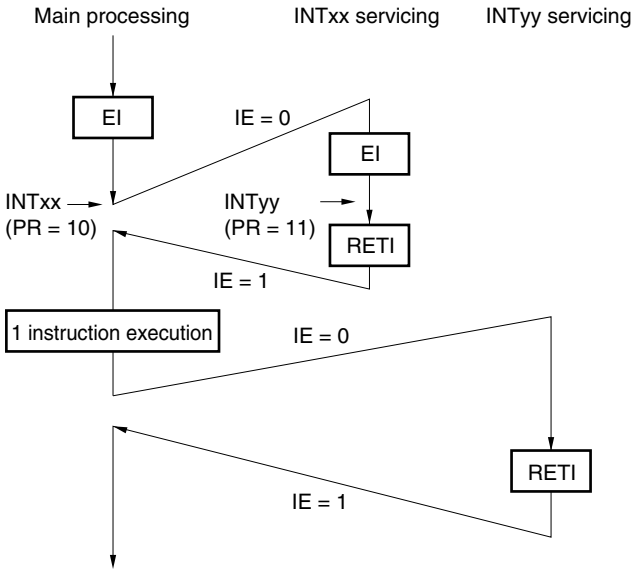
Figure 18-15. Examples of Multiple Interrupt Servicing (1/2)

Example 1. Multiple interrupt servicing occurs twice



During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

Example 2. Multiple interrupt servicing does not occur due to priority control

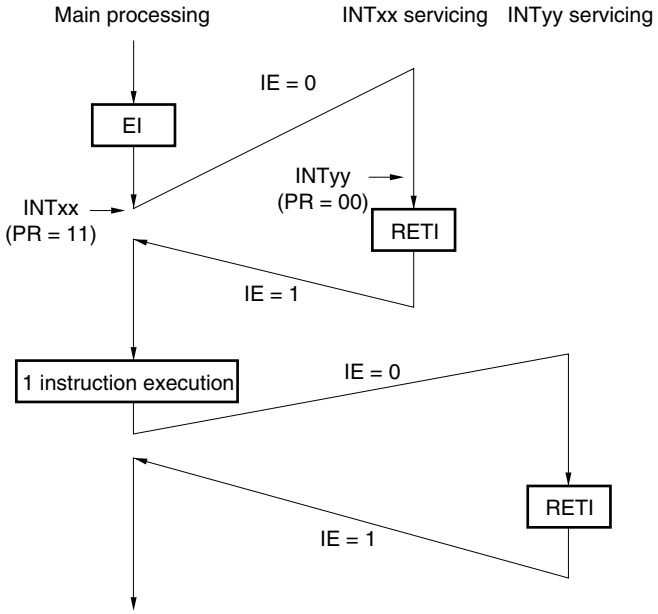


Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)
PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1
PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0
PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)
IE = 0: Interrupt request acknowledgment is disabled
IE = 1: Interrupt request acknowledgment is enabled.

Figure 18-15. Examples of Multiple Interrupt Servicing (2/2)

Example 3. Multiple interrupt servicing does not occur because interrupts are not enabled



Interrupts are not enabled during servicing of interrupt INTxx (EI instruction is not issued), therefore, interrupt request INTyy is not acknowledged and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)
PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1
PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0
PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)
IE = 0: Interrupt request acknowledgment is disabled
IE = 1: Interrupt request acknowledgment is enabled.

18.5.4 Interrupt request hold

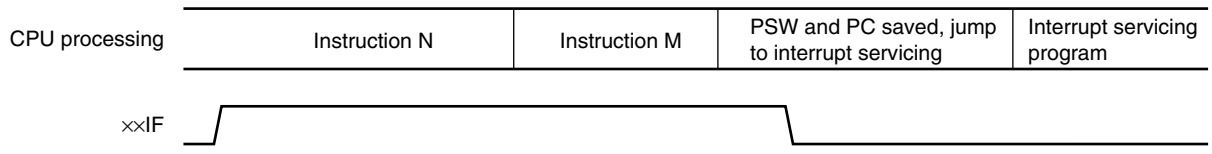
There are instructions where, even if an interrupt request is issued while the instructions are being executed, interrupt request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV PSW, A
- MOV1 PSW. bit, CY
- SET1 PSW. bit
- CLR1 PSW. bit
- RETB
- RETI
- POP PSW
- BTCLR PSW. bit, $addr20
- EI
- DI
- SKC
- SKNC
- SKZ
- SKNZ
- SKH
- SKNH
- Manipulation instructions for the IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, and PR12H registers

Caution The BRK instruction is not one of the above-listed interrupt request hold instructions. However, the software interrupt activated by executing the BRK instruction causes the IE flag to be cleared. Therefore, even if a maskable interrupt request is generated during execution of the BRK instruction, the interrupt request is not acknowledged.

Figure 18-16 shows the timing at which interrupt requests are held pending.

Figure 18-16. Interrupt Request Hold



Remarks 1. Instruction N: Interrupt request hold instruction

2. Instruction M: Instruction other than interrupt request hold instruction

3. The ××PR (priority level) values do not affect the operation of ××IF (interrupt request).

CHAPTER 19 KEY INTERRUPT FUNCTION

The number of key interrupt input channels differs, depending on the product.

	78K0R/KC3-L	78K0R/KD3-L	78K0R/KE3-L	78K0R/KF3-L	78K0R/KG3-L
Key interrupt input channels	6 ch	8 ch			

19.1 Functions of Key Interrupt

A key interrupt (INTKR) can be generated by setting the key return mode register (KRM) and inputting a falling edge to the key interrupt input pins (KR0 to KR7).

Table 19-1. Assignment of Key Interrupt Detection Pins

Flag	Description
KRM0	Controls KR0 signal in 1-bit units.
KRM1	Controls KR1 signal in 1-bit units.
KRM2	Controls KR2 signal in 1-bit units.
KRM3	Controls KR3 signal in 1-bit units.
KRM4	Controls KR4 signal in 1-bit units.
KRM5	Controls KR5 signal in 1-bit units.
KRM6	Controls KR6 signal in 1-bit units.
KRM7	Controls KR7 signal in 1-bit units.

19.2 Configuration of Key Interrupt

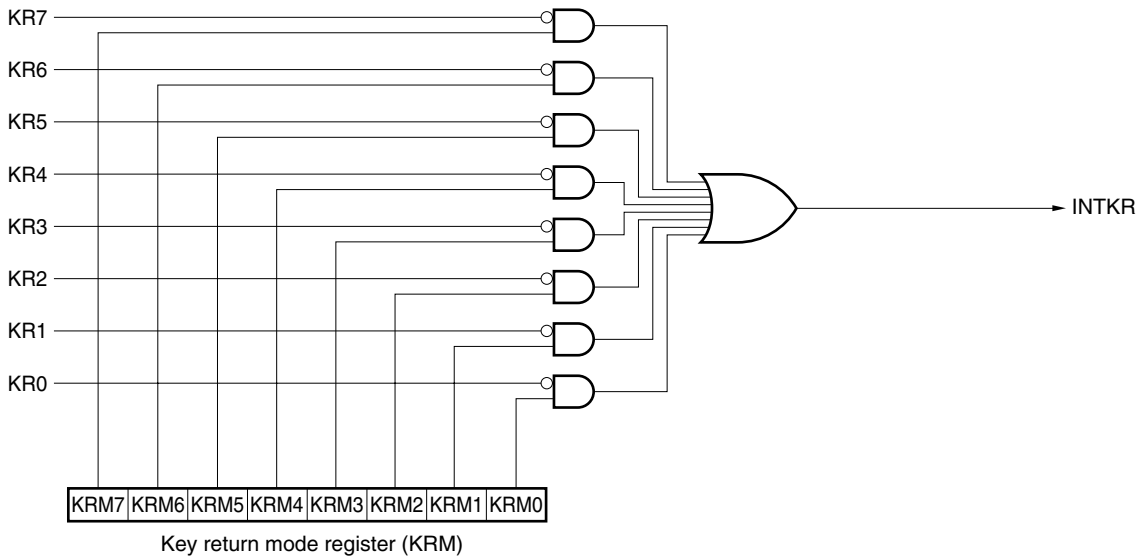
The key interrupt includes the following hardware.

Table 19-2. Configuration of Key Interrupt

Item	Configuration
Control register	Key return mode register (KRM)

Remark KR0 to KR5: 78K0R/KC3-L
KR0 to KR7: 78K0R/KD3-L, 78K0R/KE3-L, 78K0R/KF3-L, and 78K0R/KG3-L

Figure 19-1. Block Diagram of Key Interrupt



Remark KR0 to KR5: 78K0R/KC3-L
KR0 to KR7: 78K0R/KD3-L, 78K0R/KE3-L, 78K0R/KF3-L, and 78K0R/KG3-L

19.3 Register Controlling Key Interrupt

(1) Key return mode register (KRM)

This register controls the KRM0 to KRM7 bits using the KR0 to KR7 signals, respectively.

The KRM register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 19-2. Format of Key Return Mode Register (KRM)

Address: FFF37H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0

KRMn	Key interrupt mode control
0	Does not detect key interrupt signal
1	Detects key interrupt signal

Cautions 1. If any of the KRM0 to KRM7 bits used is set to 1, set bits 0 to 7 (PU70 to PU77) of the corresponding pull-up resistor register 7 (PU7) to 1.

2. An interrupt will be generated if the target bit of the KRM register is set while a low level is being input to the key interrupt input pin. To ignore this interrupt, set the KRM register after disabling interrupt servicing by using the interrupt mask flag. Afterward, clear the interrupt request flag and enable interrupt servicing after waiting for the key interrupt input low-level width (250 ns or more).

3. The bits not used in the key interrupt mode can be used as normal ports.

Remarks 1. n = 0 to 7

2. KR0 to KR5: 78K0R/KC3-L

KR0 to KR7: 78K0R/KD3-L, 78K0R/KE3-L, 78K0R/KF3-L, and 78K0R/KG3-L

CHAPTER 20 STANDBY FUNCTION

20.1 Standby Function and Configuration

20.1.1 Standby function

The standby function reduces the operating current of the system, and the following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, internal high-speed oscillator, 20 MHz internal high-speed oscillator, or subsystem clock oscillator[Note] is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and internal high-speed oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Cautions 1. The STOP mode can be used only when the CPU is operating on the main system clock. The STOP mode cannot be set while the CPU operates with the subsystem clock. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.

2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction.

3. The following sequence is recommended for operating current reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

4. The following sequence is recommended for operating current reduction of the comparator when the standby function is used: First clear bit 7 (CnEN) of the comparator n control register (CnCTL) and bit 7 (CnVRE) of the comparator n internal reference voltage selection register to 0 to stop the comparator operation, and then execute the STOP instruction.

5. The following sequence is recommended for operating current reduction of the programmable gain amplifier when the standby function is used: First clear bit 7 (OAEN) of the programmable gain amplifier control register (OAM) to 0 to stop the programmable gain amplifier operation, and then execute the STOP instruction.

Remark n = 0, 1

Cautions 6. It can be selected by the option byte whether the internal low-speed oscillator continues oscillating or stops in the HALT or STOP mode. For details, see CHAPTER 25 OPTION BYTE.

7. The STOP instruction cannot be executed when the CPU operates on the 20 MHz internal high-speed oscillation clock. Be sure to execute the STOP instruction after shifting to internal high-speed oscillation clock operation.

20.1.2 Registers controlling standby function

The standby function is controlled by the following two registers.

- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

Remark For the registers that start, stop, or select the clock, see **CHAPTER 7 CLOCK GENERATOR**.

(1) Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter.

The X1 clock oscillation stabilization time can be checked in the following case.

- If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock[Note] is being used as the CPU clock.
- If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating.

The OSTC register can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POC, LVI, WDT, and executing an illegal instruction), the STOP instruction and MSTOP bit (bit 7 of clock operation status control register (CSC)) = 1 clear this register to 00H.

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Figure 20-1. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFFA2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18

MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18	Oscillation stabilization time status		
									fx = 10 MHz	fx = 20 MHz
0	0	0	0	0	0	0	0	2^8/fx max.	25.6 μs max.	12.8 μs max.
1	0	0	0	0	0	0	0	2^8/fx min.	25.6 μs min.	12.8 μs min.
1	1	0	0	0	0	0	0	2^9/fx min.	51.2 μs min.	25.6 μs min.
1	1	1	0	0	0	0	0	2^{10}/fx min.	102.4 μs min.	51.2 μs min.
1	1	1	1	0	0	0	0	2^{11}/fx min.	204.8 μs min.	102.4 μs min.
1	1	1	1	1	0	0	0	2^{13}/fx min.	819.2 μs min.	409.6 μs min.
1	1	1	1	1	1	0	0	2^{15}/fx min.	3.27 ms min.	1.64 ms min.
1	1	1	1	1	1	1	0	2^{17}/fx min.	13.11 ms min.	6.55 ms min.
1	1	1	1	1	1	1	1	2^{18}/fx min.	26.21 ms min.	13.11 ms min.

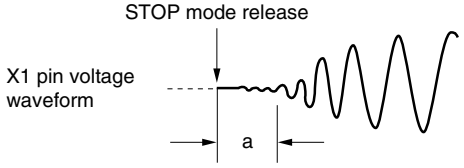
Cautions 1. After the above time has elapsed, the bits are set to 1 in order from the MOST8 bit and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the oscillation stabilization time select register (OSTS). If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC register oscillation stabilization time ≤ Oscillation stabilization time set by OSTS register**

Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after STOP mode is released.

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

(2) Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using the OSTS register after the STOP mode is released.

When the internal high-speed oscillation clock is selected as the CPU clock, confirm with the oscillation stabilization time counter status register (OSTC) that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using the OSTC register.

The OSTS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 07H.

Figure 20-2. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFFA3H After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				f_X = 10 MHz	f_X = 20 MHz
0	0	0	$2^8/f_X$	25.6 μs	Setting prohibited
0	0	1	$2^9/f_X$	51.2 μs	25.6 μs
0	1	0	$2^{10}/f_X$	102.4 μs	51.2 μs
0	1	1	$2^{11}/f_X$	204.8 μs	102.4 μs
1	0	0	$2^{13}/f_X$	819.2 μs	409.6 μs
1	0	1	$2^{15}/f_X$	3.27 ms	1.64 ms
1	1	0	$2^{17}/f_X$	13.11 ms	6.55 ms
1	1	1	$2^{18}/f_X$	26.21 ms	13.11 ms

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.

2. Setting the oscillation stabilization time to 20 μs or less is prohibited.

3. Before changing the setting of the OSTS register, confirm that the count operation of the OSTC register is completed.

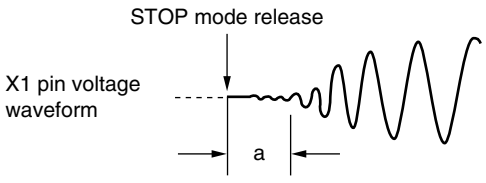
4. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

5. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the OSTS register. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC register oscillation stabilization time ≤ Oscillation stabilization time set by OSTS register**

Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after STOP mode is released.

6. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_X: X1 clock oscillation frequency

20.2 Standby Function Operation

20.2.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock, internal high-speed oscillation clock, 20 MHz internal high-speed oscillation clock, or subsystem clock[Note].

The operating statuses in the HALT mode are shown below.

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Table 20-1. Operating Statuses in HALT Mode (1/2)

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{IH}) or 20 MHz Internal High-Speed Oscillation Clock (f_{IH20})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}, f_{IH20}	Operation continues (cannot be stopped)	Status before HALT mode was set is retained	
		f_X	Status before HALT mode was set is retained	Operation continues (cannot be stopped)	Cannot operate
		f_{EX}		Cannot operate	Operation continues (cannot be stopped)
	Subsystem clock[Note 1]	f_{XT}		Status before HALT mode was set is retained	
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WTON) of option byte (000C0H) • WTON = 0: Stops • WTON = 1 and WDSTBYON = 1: Oscillates • WTON = 1 and WDSTBYON = 0: Stops		
CPU			Operation stopped		
Flash memory			Operation stopped		
RAM			The value is retained		
Port (latch)			Status before HALT mode was set is retained		
Timer array unit			Operable		
Real-time counter (RTC) [Note 1]					
Watchdog timer			Set by bits 0 (WDSTBYON) and 4 (WTON) of option byte (000C0H) • WTON = 0: Stops • WTON = 1 and WDSTBYON = 1: Operates • WTON = 1 and WDSTBYON = 0: Stops		
Clock output/buzzer output [Note 2]			Operable		
A/D converter					
Programmable gain amplifier [Note 3]					
Comparator [Note 3]					
Serial array unit (SAU)					
Serial interface (IICA) [Note 2]					
Multiplier/divider					
DMA controller					
Power-on-clear function					
Low-voltage detection function					
External interrupt					
Key interrupt function					

Notes 1. That os not mounted onto 40-pin product of the 78K0R/KC3-L.
2. Those are not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.
3. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only.

Remark f_{IH}: Internal high-speed oscillation clock
f_{IH20}: 20 MHz internal high-speed oscillation clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{IL}: Internal low-speed oscillation clock

Table 20-1. Operating Statuses in HALT Mode (2/2)

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock
			When CPU Is Operating on XT1 Clock (f_{XT})
System clock			Clock supply to the CPU is stopped
	Main system clock	f_{IH}, f_{IH20}	Status before HALT mode was set is retained
		f_X	
		f_{EX}	
	Subsystem clock[Note 1]	f_{XT}	Operation continues (cannot be stopped)
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H) • WDTON = 0: Stops • WDTON = 1 and WDSTBYON = 1: Oscillates • WDTON = 1 and WDSTBYON = 0: Stops
CPU			Operation stopped
Flash memory			Operation stopped (wait state in low-current consumption mode)
RAM			The value is retained
Port (latch)			Status before HALT mode was set is retained
Timer array unit			Operable
Real-time counter (RTC)[Note 1]			
Watchdog timer			Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H) • WDTON = 0: Stops • WDTON = 1 and WDSTBYON = 1: Operates • WDTON = 1 and WDSTBYON = 0: Stops
Clock output/buzzer output[Note 2]			Operable
A/D converter			Cannot operate
Programmable gain amplifier[Note 3]			Operable
Comparator[Note 3]			
Serial array unit (SAU)			
Serial interface (IICA)[Note 2]			Cannot operate
Multiplier/divider			Operable
DMA controller			
Power-on-clear function			
Low-voltage detection function			
External interrupt			
Key interrupt function			

Notes 1. That is not mounted onto 40-pin product of the 78K0R/KC3-L.
2. Those are not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.
3. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only.

Remark f_{IH}: Internal high-speed oscillation clock
f_{IH20}: 20 MHz internal high-speed oscillation clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{IL}: Internal low-speed oscillation clock

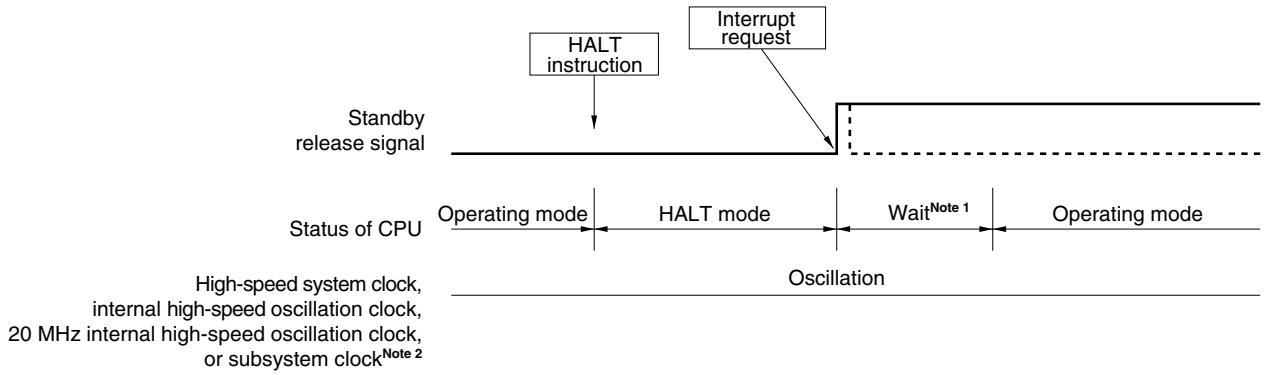
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 20-3. HALT Mode Release by Interrupt Request Generation



Notes 1. The wait time is as follows:

- When vectored interrupt servicing is carried out
  - When main system clock is used: 10 to 12 clocks
  - When subsystem clock is used: 8 to 10 clocks
- When vectored interrupt servicing is not carried out
  - When main system clock is used: 5 or 6 clocks
  - When subsystem clock is used: 3 or 4 clocks

2. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

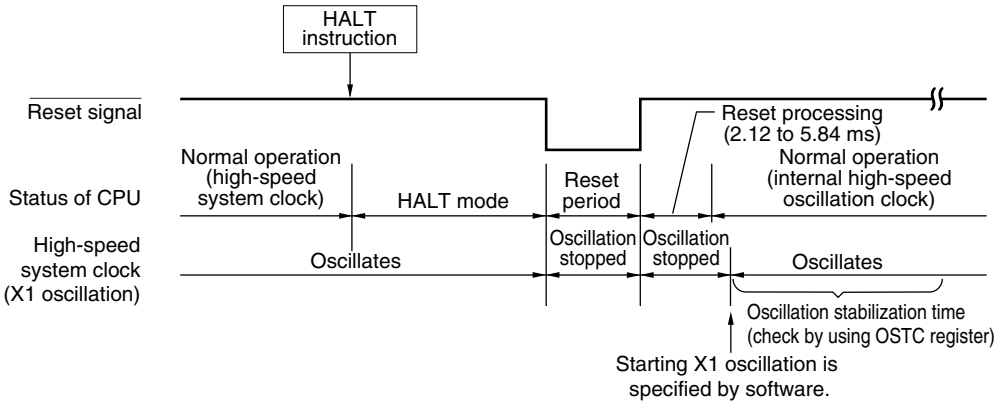
Remark The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

(b) Release by reset signal generation

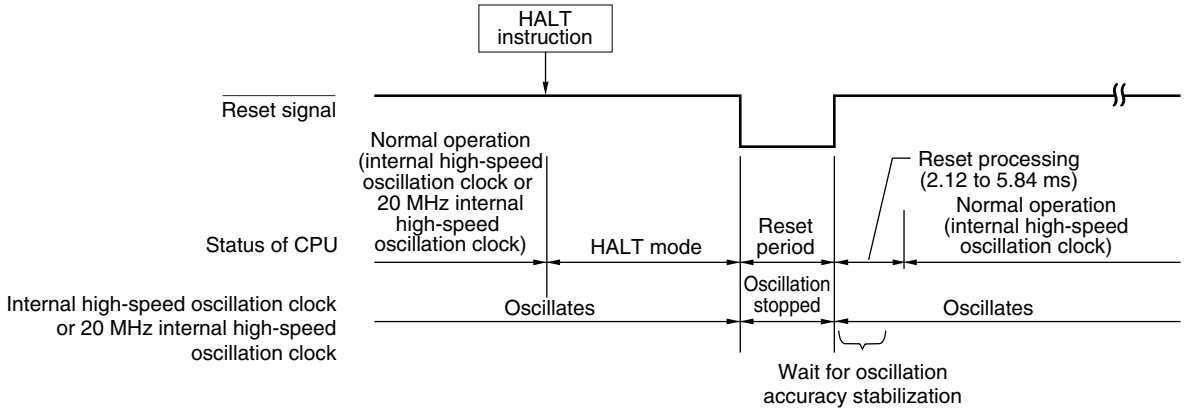
When the reset signal is generated, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 20-4. HALT Mode Release by Reset

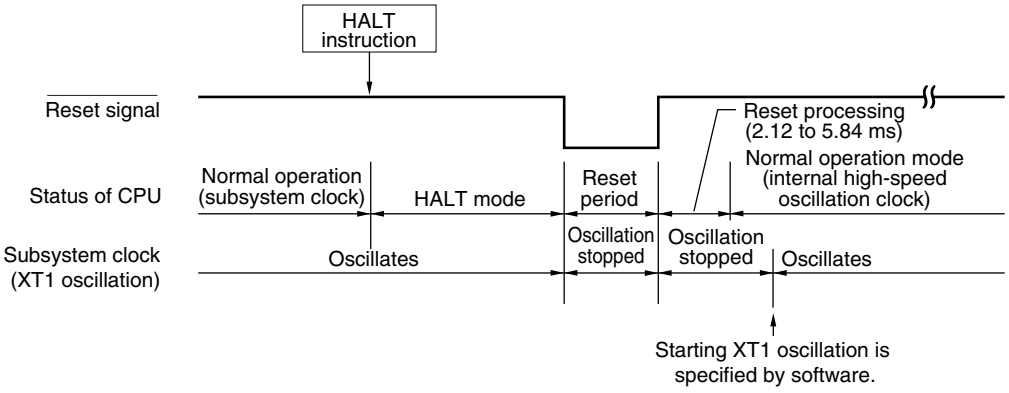
(1) When high-speed system clock is used as CPU clock



(2) When internal high-speed oscillation clock or 20 MHz internal high-speed oscillation clock is used as CPU clock



(3) When subsystem clock is used as CPU clock[Note]



Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Remark fx: X1 clock oscillation frequency

20.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the internal high-speed oscillation clock, X1 clock, or external main system clock.

Cautions 1. Because the interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.

2. The STOP instruction cannot be executed when the CPU operates on the 20 MHz internal high-speed oscillation clock. Be sure to execute the STOP instruction after shifting to internal high-speed oscillation clock operation.

The operating statuses in the STOP mode are shown below.

Table 20-2. Operating Statuses in STOP Mode

STOP Mode Setting / Item	When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
	When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
System clock	Clock supply to the CPU is stopped		
Main system clock (f_{IH})	Stopped		
Main system clock (f_X)	Stopped		
Main system clock (f_{EX})	Stopped		
Subsystem clock[Note 1] (f_{XT})	Status before STOP mode was set is retained		
f_{IL}	Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H) • WDTON = 0: Stops • WDTON = 1 and WDSTBYON = 1: Oscillates • WDTON = 1 and WDSTBYON = 0: Stops		
CPU	Operation stopped		
Flash memory	Operation stopped		
RAM	The value is retained		
Port (latch)	Status before STOP mode was set is retained		
Timer array unit	Operation disabled		
Real-time counter (RTC)[Note 1]	Operable		
Watchdog timer	Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H) • WDTON = 0: Stops • WDTON = 1 and WDSTBYON = 1: Operates • WDTON = 1 and WDSTBYON = 0: Stops		
Clock output/buzzer output[Note 2]	Operable only when subsystem clock is selected as the count clock		
A/D converter	Operation disabled		
Programmable gain amplifier[Note 3]			
Comparator[Note 3]			
Serial array unit (SAU)			
Serial interface (IICA)[Note 2]	Wakeup by address match operable		
Multiplier/divider	Operation disabled		
DMA controller			
Power-on-clear function	Operable		
Low-voltage detection function			
External interrupt			
Key interrupt function			

Notes 1. Those are not mounted onto 40-pin product of the 78K0R/KC3-L.
2. Those are not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.
3. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only.

Remark f_{IH}: Internal high-speed oscillation clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{IL}: Internal low-speed oscillation clock

Cautions 1. To use the peripheral hardware that stops operation in the STOP mode, and the peripheral hardware for which the clock that stops oscillating in the STOP mode after the STOP mode is released, restart the peripheral hardware.

2. To stop the internal low-speed oscillation clock in the STOP mode, use an option byte to stop the watchdog timer operation in the HALT/STOP mode (bit 0 (WDSTBYON) of 000C0H = 0), and then execute the STOP instruction.

3. To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), temporarily switch the CPU clock to the internal high-speed oscillation clock before the execution of the STOP instruction. Before changing the CPU clock from the internal high-speed oscillation clock to the high-speed system clock (X1 oscillation) after the STOP mode is released, check the oscillation stabilization time with the oscillation stabilization time counter status register (OSTC).

4. The STOP instruction cannot be executed when the CPU operates on the 20 MHz internal high-speed oscillation clock. Be sure to execute the STOP instruction after shifting to internal high-speed oscillation clock operation.

(2) STOP mode release

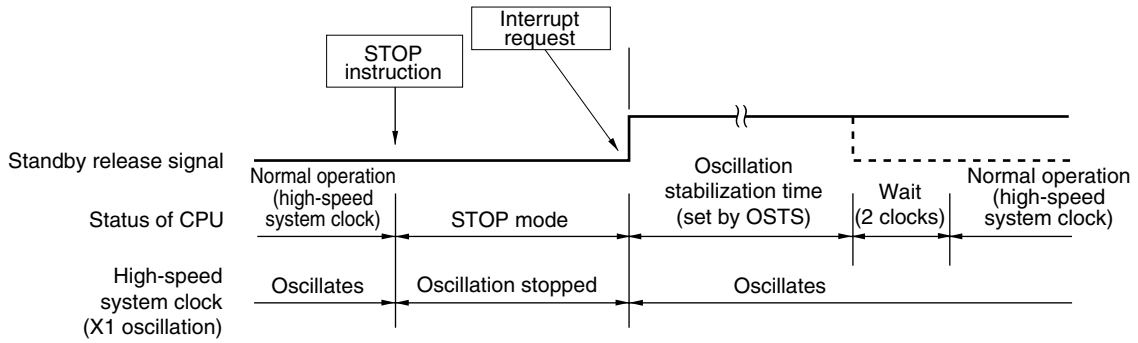
The STOP mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the STOP mode is released. After the oscillation stabilization time has elapsed, if interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 20-5. STOP Mode Release by Interrupt Request Generation (1/2)

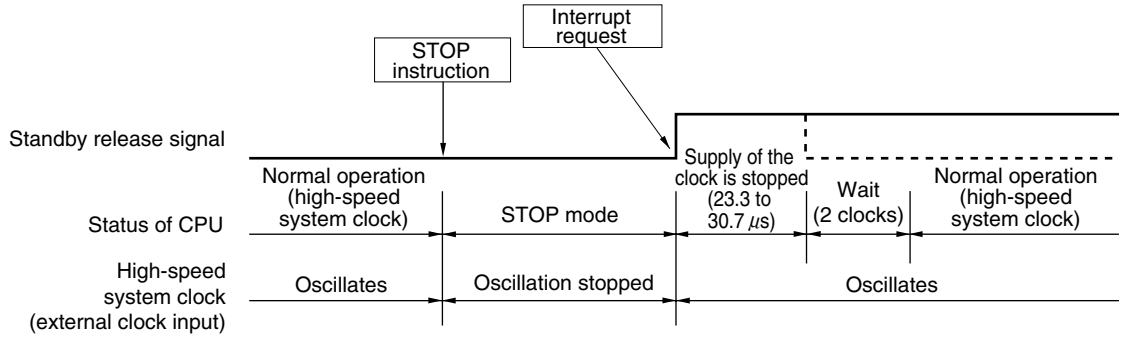
(1) When high-speed system clock (X1 oscillation) is used as CPU clock



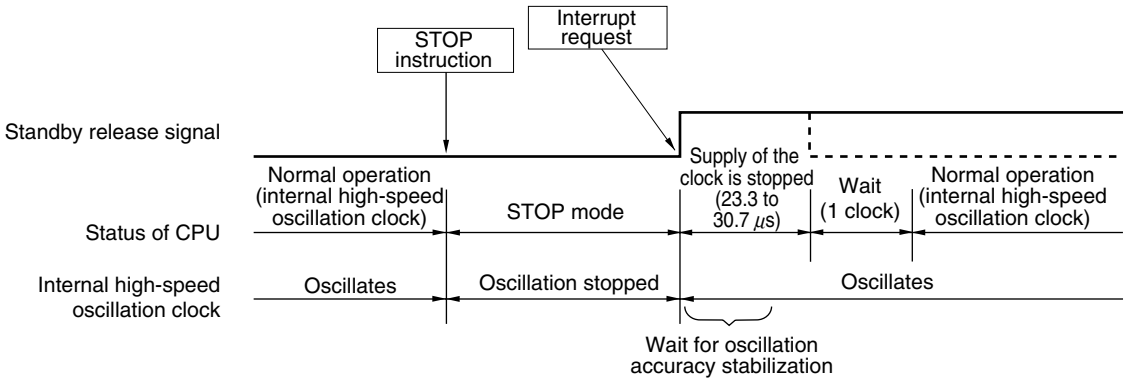
Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Figure 20-5. STOP Mode Release by Interrupt Request Generation (2/2)

(2) When high-speed system clock (external clock input) is used as CPU clock



(3) When internal high-speed oscillation clock is used as CPU clock



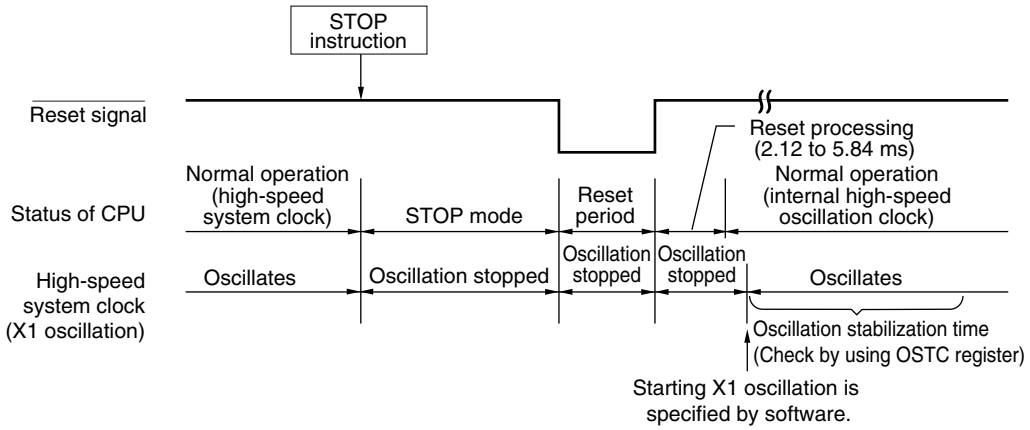
Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

(b) Release by reset signal generation

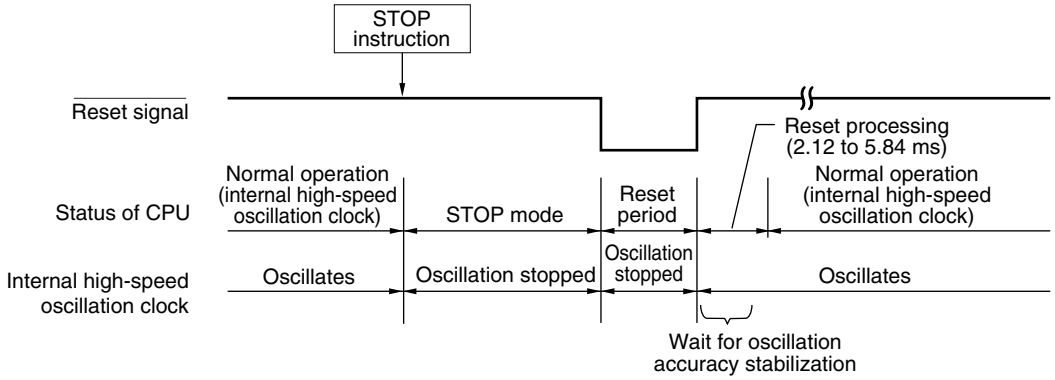
When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 20-6. STOP Mode Release by Reset

(1) When high-speed system clock is used as CPU clock



(2) When internal high-speed oscillation clock is used as CPU clock



Remark fx: X1 clock oscillation frequency

CHAPTER 21 RESET FUNCTION

The following five operations are available to generate a reset signal.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
(4) Internal reset by comparison of supply voltage of the low-voltage detector (LVI) or input voltage (EXLVI) from external input pin, and detection voltage
(5) Internal reset by execution of illegal instruction[Note]
(6) Internal reset by a reset processing check error

External and internal resets start program execution from the address at 0000H and 0001H when the reset signal is generated.

A reset is effected when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POC and LVI circuit voltage detection or execution of illegal instruction[Note 1], and each item of hardware is set to the status shown in Tables 21-1 and 21-2. Each pin is high impedance during reset signal generation or during the oscillation stabilization time just after a reset release, except for P140[Notes 2, 3], which is low-level output.

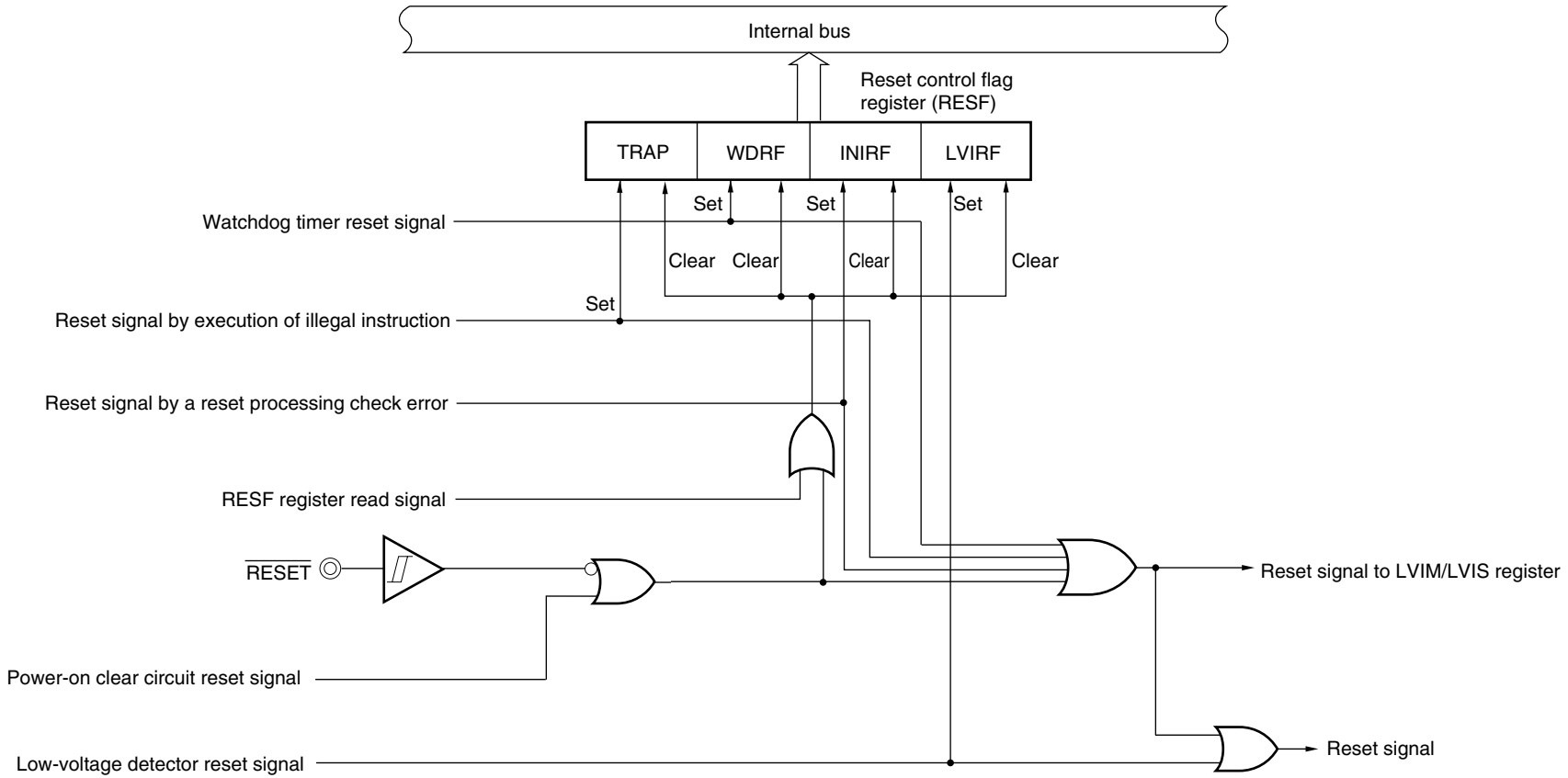
When a low level is input to the $\overline{\text{RESET}}$ pin, the device is reset. It is released from the reset status when a high level is input to the $\overline{\text{RESET}}$ pin and program execution is started with the internal high-speed oscillation clock after reset processing. A reset by the watchdog timer is automatically released, and program execution starts using the internal high-speed oscillation clock (see **Figures 21-2** to **21-4**) after reset processing. Reset by POC and LVI circuit supply voltage detection is automatically released when $V_{DD} \geq V_{POR}$ or $V_{DD} \geq V_{LVI}$ after the reset, and program execution starts using the internal high-speed oscillation clock (see **CHAPTER 22 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 23 LOW-VOLTAGE DETECTOR**) after reset processing.

Notes 1. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.
2. The P140 pin is not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.
3. Read P140 as P130 if using the 78K0R/KF3-L or 78K0R/KG3-L.

Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.
(To perform an external reset upon power application, a low level of at least 10 μs must be continued during the period in which the supply voltage is within the operating range ($V_{DD} \geq 1.8$ V).)
2. During reset input, the X1 clock, XT1 clock (except for 78K0R/KC3-L (40-pin)), internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input becomes invalid.
3. When the STOP mode is released by a reset, the RAM contents in the STOP mode are held during reset input.
4. When reset is effected, port pin P140 is set to low-level output and other port pins become high-impedance, because each SFR and 2nd SFR are initialized.

Remark V_{POR}: POC power supply rise detection voltage

Figure 21-1. Block Diagram of Reset Function



Caution An LVI circuit internal reset does not reset the LVI circuit.

Remarks 1. LVIM: Low-voltage detection register

2. LVIS: Low-voltage detection level select register

Figure 21-2. Timing of Reset by $\overline{\text{RESET}}$ Input

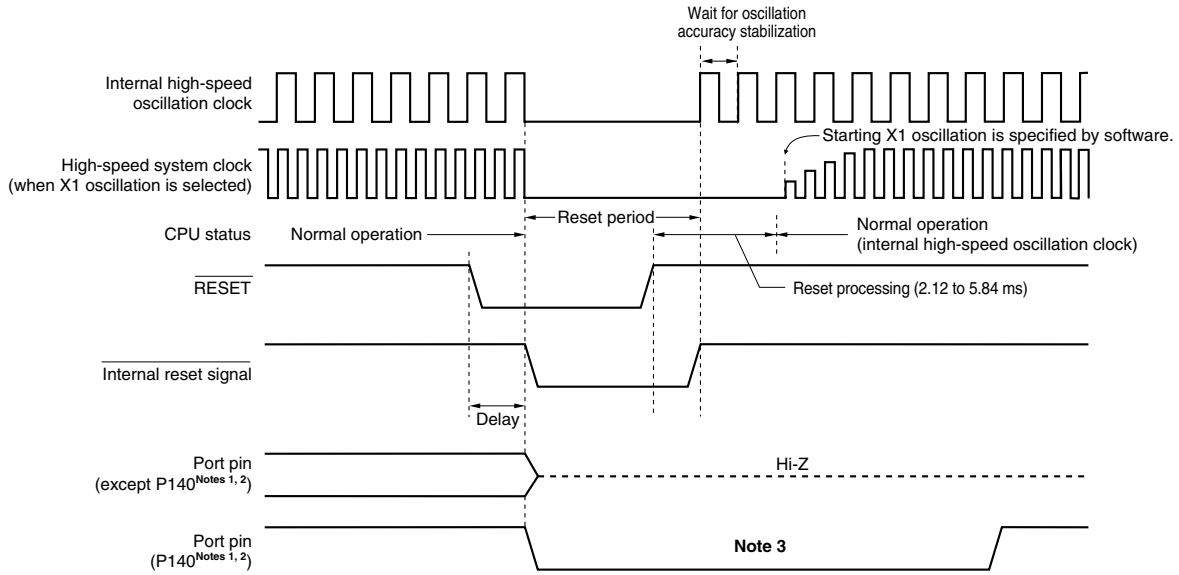
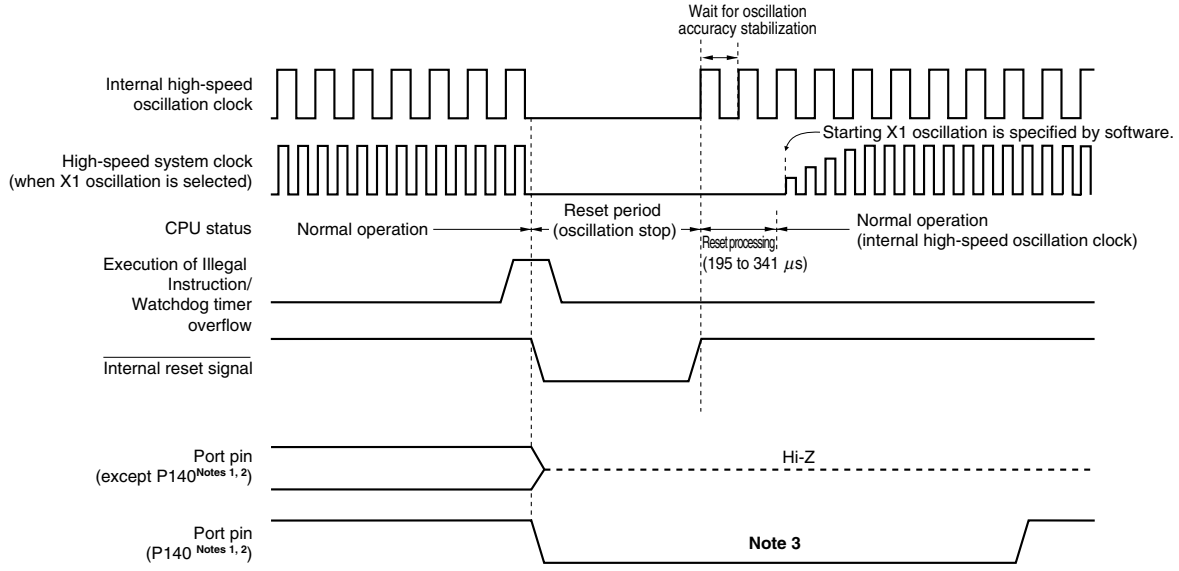


Figure 21-3. Timing of Reset Due to Execution of Illegal Instruction or Watchdog Timer Overflow



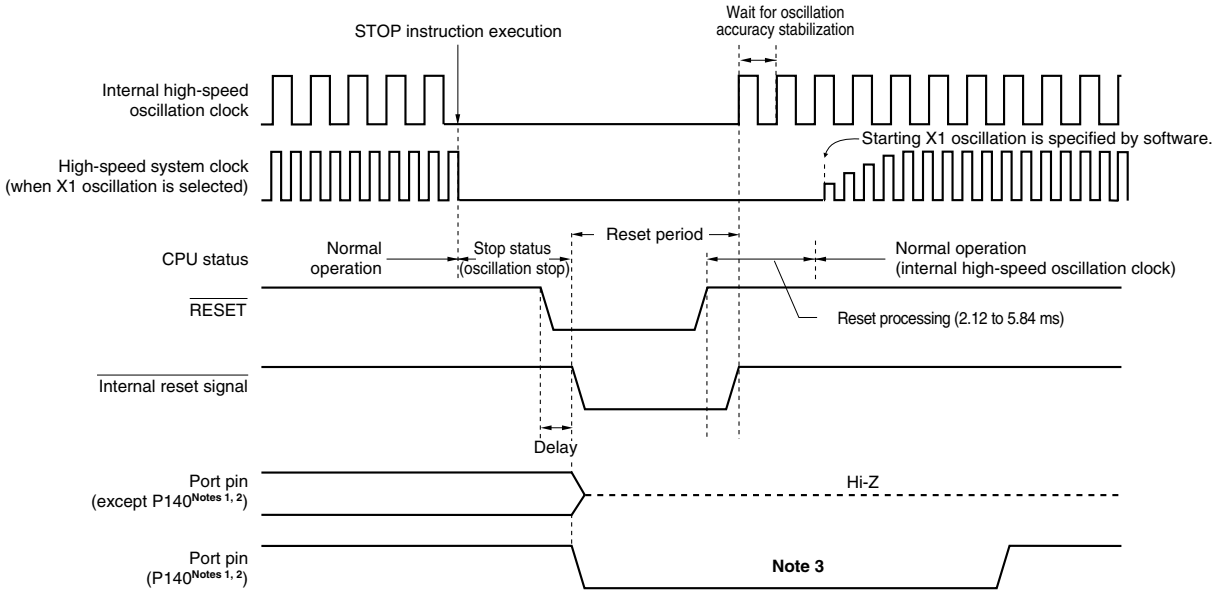
Notes 1. The P140 pin is not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.

2. Read P140 as P130 if using the 78K0R/KF3-L or 78K0R/KG3-L.

3. When P140 is set to high-level output before reset is effected, the output signal of P140 can be dummy-output as a reset signal to an external device, because P140 outputs a low level when reset is effected. To release a reset signal to an external device, set P140 to high-level output by software.

Caution A watchdog timer internal reset resets the watchdog timer.

Figure 21-4. Timing of Reset in STOP Mode by $\overline{\text{RESET}}$ Input



Notes 1. The P140 pin is not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.

2. Read P140 as P130 if using the 78K0R/KF3-L or 78K0R/KG3-L.

3. Set P140 to high-level output by software. When P140 is set to high-level output before reset is effected, the output signal of P140 can be dummy-output as a reset signal to an external device, because P140 outputs a low level when reset is effected. To release a reset signal to an external device, set P140 to high-level output by software.

Remark For the reset timing of the power-on-clear circuit and low-voltage detector, see **CHAPTER 22 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 23 LOW-VOLTAGE DETECTOR**.

Table 21-1. Operation Statuses During Reset Period

Item			During Reset Period
System clock			Clock supply to the CPU is stopped.
	Main system clock	f_{IH}	Operation stopped
		f_X	Operation stopped (the X1 and X2 pins are input port mode)
		f_{EX}	Clock input invalid (the pin is input port mode)
	Subsystem clock Note 1	f_{XT}	Operation stopped (the XT1 and XT2 pins are input port mode)
	f_{IL}		Operation stopped
CPU			
Flash memory			
RAM			Operation stopped (The value, however, is retained when the voltage is at least the power-on-clear detection voltage.)
Port (latch)			Set P140 to low-level output. The port pins except for P140 become high impedance. Note 2
Timer array unit			Operation stopped
Real-time counter (RTC) Note 1			
Watchdog timer			
Clock output/buzzer output Note 3			
A/D converter			
Programmable gain amplifier Note 4			
Comparator Note 4			
Serial array unit (SAU)			
Serial interface (IICA) Note 3			
Multiplier/divider			
DMA controller			
Power-on-clear function			Detection operation possible
Low-voltage detection function			Operation stopped (however, operation continues at LVI reset)
External interrupt			Operation stopped
Key interrupt function			

Notes 1. This is not mounted onto 40-pin product of the 78K0R/KC3-L.
2. Read P140 as P130 if using the 78K0R/KF3-L or 78K0R/KG3-L.
3. This is not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.
4. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only.

Remark f_{IH}: Internal high-speed oscillation clock
f_X: X1 oscillation clock
f_{EX}: External main system clock
f_{XT}: XT1 oscillation clock
f_{IL}: Internal low-speed oscillation clock

Table 21-2. Hardware Statuses After Reset Acknowledgment (1/4)

Hardware		After Reset Acknowledgment[Note 1]
Program counter (PC)		The contents of the reset vector table (0000H, 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		06H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Processor mode control register (PMC)		00H
Port registers (P0 to P9, P11 to P15) (output latches)		00H
Port mode registers	PM0 to PM9, PM11 to PM15[Note 3]	FFH
Port input mode registers 0, 1, 3, 7, 8, 14 (PIM0, PIM1, PIM3, PIM7, PIM8, PIM14)		00H
Port output mode registers 0, 1, 3, 7, 14 (POM0, POM1, POM3, POM7, POM14)		00H
Pull-up resistor option registers (PU0, PU1, PU3 to PU9, PU11 to PU14)		00H
Clock operation mode control register (CMC)		00H
Clock operation status control register (CSC)		C0H
System clock control register (CKC)		09H
20 MHz internal high-speed oscillation control register (DSCCTL)		00H
Oscillation stabilization time counter status register (OSTC)		00H
Oscillation stabilization time select register (OSTS)		07H
Noise filter enable registers 0, 1, 2 (NFEN0, NFEN1, NFEN2)		00H
Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2)		00H
Operation speed mode control register (OSMC)		00H
Timer array unit	Timer data registers 00 to 07, 10 to 13 (TDR00 to TDR07, TDR10 to TDR13)	0000H
	Timer mode registers 00 to 07, 10 to 13 (TMR00 to TMR07, TMR10 to TMR13)	0000H
	Timer status registers 00 to 07, 10 to 13 (TSR00 to TSR07, TSR10 to TSR13)	0000H
	Timer input select registers 0, 1 (TIS0, TIS1)	00H
	Timer counter registers 00 to 07, 10 to 13 (TCR00 to TCR07, TCR10 to TCR13)	FFFFH
	Timer channel enable status registers 0, 1 (TE0, TE1)	0000H
	Timer channel start registers 0, 1 (TS0, TS1)	0000H
	Timer channel stop registers 0, 1 (TT0, TT1)	0000H
	Timer clock select registers 0, 1 (TPS0, TPS1)	0000H
	Timer output registers 0, 1 (TO0, TO1)	0000H
	Timer output enable registers 0 , 1(TOE0, TOE1)	0000H
	Timer output level registers 0, 1 (TOL0, TOL1)	0000H
	Timer output mode registers 0, 1 (TOM0, TOM1)	0000H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. When a reset is executed in the standby mode, the pre-reset status is held even after reset.

3. In the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L, the reset value of the PM14 register is FEH. In the 78K0R/KF3-L and 78K0R/KG3-L, the reset value of the PM13 register is FEH.

Remark The special function register (SFR) mounted depend on the product. See **4.2.4 Special function registers (SFRs)** and **4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

Table 21-2. Hardware Statuses After Reset Acknowledgment (2/4)

Hardware		Status After Reset Acknowledgment[Note 1]
Real-time counter	Sub-count register (RSUBC)	0000H
	Second count register (SEC)	00H
	Minute count register (MIN)	00H
	Hour count register (HOUR)	12H
	Week count register (WEEK)	00H
	Day count register (DAY)	01H
	Month count register (MONTH)	01H
	Year count register (YEAR)	00H
	Watch error correction register (SUBCUD)	00H
	Alarm minute register (ALARMWM)	00H
	Alarm hour register (ALARMWH)	12H
	Alarm week register ALARMWW)	00H
	Control register 0 (RTCC0)	00H
	Control register 1 (RTCC1)	00H
	Control register 2 (RTCC2)	00H
Clock output/buzzer output controller	Clock output select registers 0, 1 (CKS0, CKS1)	00H
Watchdog timer	Enable register (WDTE)	1AH/9AH[Note 2]
A/D converter	10-bit A/D conversion result register (ADCR)	0000H
	8-bit A/D conversion result register (ADCRH)	00H
	Mode register (ADM)	00H
	Analog input channel specification register (ADS)	00H
	A/D port configuration register (ADPC)	10H
Serial array unit (SAU)	Serial data registers 00 to 03, 10 to 13, 20, 21 (SDR00 to SDR03, SDR10 to SDR13, SDR20, SDR21)	0000H
	Serial status registers 00 to 03, 10 to 13, 20, 21 (SSR00 to SSR03, SSR10 to SSR13, SSR20, SSR21)	0000H
	Serial flag clear trigger registers 00 to 03, 10 to 13, 20, 21 (SIR00 to SIR03, SIR10 to SIR13, SIR20, SIR21)	0000H
	Serial mode registers 00 to 03, 10 to 13, 20, 21 (SMR00 to SMR03, SMR10 to SMR13, SMR20, SMR21)	0020H
	Serial communication operation setting registers 00 to 03, 10 to 13, 20, 21 (SCR00 to SCR03, SCR10 to SCR13, SCR20, SCR21)	0087H
	Serial channel enable status registers 0, 1, 2 (SE0, SE1, SE2)	0000H
	Serial channel start registers 0, 1, 2 (SS0, SS1, SS2)	0000H
	Serial channel stop registers 0, 1, 2 (ST0, ST1, ST2)	0000H
	Serial clock select registers 0, 1, 2 (SPS0, SPS1, SPS2)	0000H
	Serial output registers 0, 1, 2 (SO0, SO1, SO2)	0F0FH
	Serial output enable registers 0, 1, 2 (SOE0, SOE1, SOE2)	0000H
	Serial output level registers 0, 1, 2 (SOL0, SOL1, SOL2)	0000H
	Input switch control register (ISC)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. The reset value of WDTE is determined by the option byte setting.

Remark The special function register (SFR) mounted depend on the product. See **4.2.4 Special function registers (SFRs)** and **4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

Table 21-2. Hardware Statuses After Reset Acknowledgment (3/4)

Hardware		Status After Reset Acknowledgment[Note 1]
Serial interface IICA	IICA shift register (IICA)	00H
	IICA status register (IICS)	00H
	IICA flag register (IICF)	00H
	IICA control register 0 (IICCTL0)	00H
	IICA control register 1 (IICCTL1)	00H
	IICA low-level width setting register (IICWL)	FFH
	IICA high-level width setting register (IICWH)	FFH
	Slave address register (SVA)	00H
Multiplier/divider	Multiplication/division data register A (L) (MDAL)	0000H
	Multiplication/division data register A (H) (MDAH)	0000H
	Multiplication/division data register B (L) (MDBL)	0000H
	Multiplication/division data register B (H) (MDBH)	0000H
	Multiplication/division data register C (L) (MDCL)	0000H
	Multiplication/division data register C (H) (MDCH)	0000H
	Multiplication/division control register (MDUC)	00H
Key interrupt	Key return mode register (KRM)	00H
Reset function	Reset control flag register (RESF)	00H[Note 2]
Low-voltage detector	Low-voltage detection register (LVIM)	00H[Note 3]
	Low-voltage detection level select register (LVIS)	0EH[Note 2]
Regulator	Regulator mode control register (RMC)	00H
DMA controller	SFR address registers 0, 1 (DSA0, DSA1)	00H
	RAM address registers 0L, 0H, 1L, 1H (DRA0L, DRA0H, DRA1L, DRA1H)	00H
	Byte count registers 0L, 0H, 1L, 1H (DBC0L, DBC0H, DBC1L, DBC1H)	00H
	Mode control registers 0, 1 (DMC0, DMC1)	00H
	Operation control registers 0, 1 (DRC0, DRC1)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. These values vary depending on the reset source.

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POC	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by INIRF	Reset by LVI
RESF	TRAP bit	Cleared (0)	Cleared (0)	Set (1)	Held	Held	Held
	WDRF bit			Held	Set (1)	Held	Held
	INIRF bit			Held	Held	Set (1)	Held
	LVIRF bit			Held	Held	Held	Set (1)
LVIS		Cleared (0EH)	Cleared (0EH)	Cleared (0EH)	Cleared (0EH)	Cleared (0EH)	Held

3. This value varies depending on the reset source and the option byte.

Remark The special function register (SFR) mounted depend on the product. See **4.2.4 Special function registers (SFRs)** and **4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

Table 21-2. Hardware Statuses After Reset Acknowledgment (4/4)

Hardware		Status After Reset Acknowledgment[Note]
Interrupt	Request flag registers 0L, 0H, 1L, 1H, 2L, 2H (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)	00H
	Mask flag registers 0L, 0H, 1L, 1H, 2L, 2H (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)	FFH
	Priority specification flag registers 00L, 00H, 01L, 01H, 02L, 02H, 10L, 10H, 11L, 11H, 12L, 12H (PR00L, PR00H, PR01L, PR01H, PR10L, PR10H, PR11L, PR11H, PR02L, PR02H, PR12L, PR12H)	FFH
	External interrupt rising edge enable registers 0, 1 (EGP0, EGP1)	00H
	External interrupt falling edge enable registers 0, 1 (EGN0, EGN1)	00H
Programmable gain amplifier	Programmable gain amplifier control register (OAM)	00H
Comparator	Comparator 0 control register (C0CTL)	00H
	Comparator 0 internal reference voltage setting register (C0RVM)	00H
	Comparator 1 control register (C1CTL)	00H
	Comparator 1 internal reference voltage setting register (C1RVM)	00H
BCD correction circuit	BCD correction result register (BCDAJ)	Undefined

Note During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

Remark The special function register (SFR) mounted depend on the product. See **4.2.4 Special function registers (SFRs)** and **4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

21.1 Register for Confirming Reset Source

Many internal reset generation sources exist in the 78K0R/Kx3-L. The reset control flag register (RESF) is used to store which source has generated the reset request.

The RESF register can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input, reset by power-on-clear (POC) circuit, and reading the RESF register clear TRAP, WDRF, INIRF, and LVIRF flags.

Figure 21-5. Format of Reset Control Flag Register (RESF)

Address: FFFA8H After reset: 00H[Note 1] R

Symbol	7	6	5	4	3	2	1	0
RESF	TRAP	0	0	WDRF	0	0	INIRF	LVIRF

TRAP	Internal reset request by execution of illegal instruction[Note 2]
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

WDRF	Internal reset request by watchdog timer (WDT)
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

INIRF	Internal rese request t by a reset processing check error
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

LVIRF	Internal reset request by low-voltage detector (LVI)
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

Notes 1. The value after reset varies depending on the reset source.

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Cautions 1. Do not read data by a 1-bit memory manipulation instruction.

2. When the LVI default start function (bit 0 (LVIOFF) of 000C1H = 0) is used, LVIRF flag may become 1 from the beginning depending on the power-on waveform.

The status of the RESF register when a reset request is generated is shown in Table 21-3.

Table 21-3. RESF Register Status When Reset Request Is Generated

Reset Source / Flag	$\overline{\text{RESET}}$ Input	Reset by POC	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by INIRF	Reset by LVI
TRAP bit	Cleared (0)	Cleared (0)	Set (1)	Held	Held	Held
WDRF bit			Held	Set (1)	Held	Held
INIRF bit			Held	Held	Set (1)	Held
LVIRF bit			Held	Held	Held	Set (1)

CHAPTER 22 POWER-ON-CLEAR CIRCUIT

22.1 Functions of Power-on-Clear Circuit

The power-on-clear circuit (POC) has the following functions.

- Generates internal reset signal at power on.
  The reset signal is released when the supply voltage (V_{DD}) exceeds 1.61 V ±0.09 V.

  Caution If the low-voltage detector (LVI) is set to ON by an option byte by default, the reset signal is not released until the supply voltage (V_{DD}) exceeds 2.07 V ±0.2 V.

- Compares supply voltage (V_{DD}) and detection voltage (V_{PDR} = 1.59 V ±0.09 V), generates internal reset signal when $V_{DD} < V_{PDR}$.

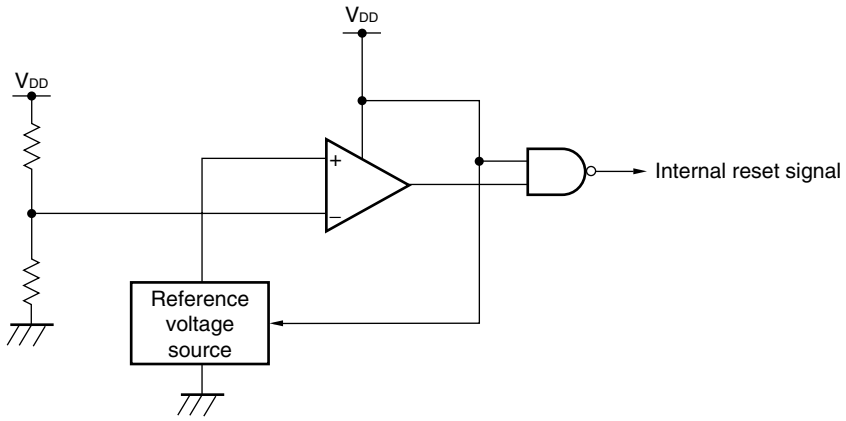
  Caution If an internal reset signal is generated in the POC circuit, TRAP, WDRF, INIRF, and LVIRF flags of the reset control flag register (RESF) is cleared.

  Remark This product incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT), low-voltage-detector (LVI), or illegal instruction execution. The RESF register is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by WDT or LVI.
  For details of the RESF register, see **CHAPTER 21 RESET FUNCTION**.

22.2 Configuration of Power-on-Clear Circuit

The block diagram of the power-on-clear circuit is shown in Figure 22-1.

Figure 22-1. Block Diagram of Power-on-Clear Circuit



22.3 Operation of Power-on-Clear Circuit

- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds the detection voltage (V_{PDR} = 1.61 V ±0.09 V), the reset status is released.

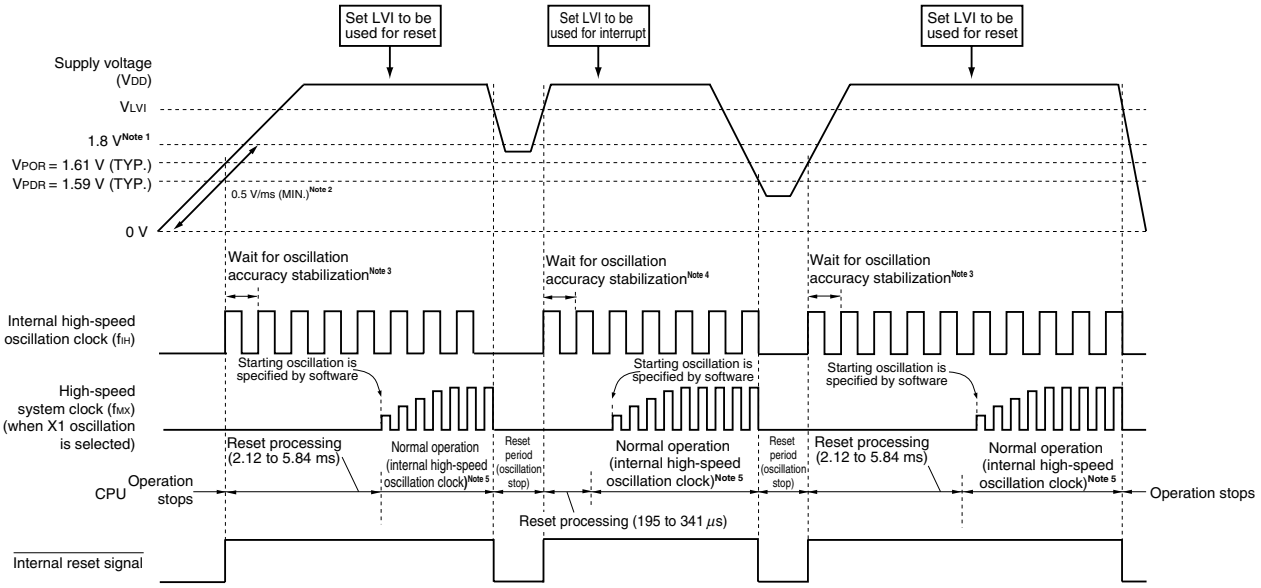
  Caution If the low-voltage detector (LVI) is set to ON by an option byte by default, the reset signal is not released until the supply voltage (V_{DD}) exceeds 2.07 V ±0.2 V.

- The supply voltage (V_{DD}) and detection voltage (V_{PDR} = 1.59 V ±0.09 V) are compared. When $V_{DD} < V_{PDR}$, the internal reset signal is generated.

The timing of generation of the internal reset signal by the power-on-clear circuit and low-voltage detector is shown below.

Figure 22-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (1/2)

(1) When LVI is OFF upon power application (option byte: LVIOFF = 1)



Notes 1. The operation guaranteed range is 1.8 V ≤ V_{DD} ≤ 5.5 V. To make the state at lower than 1.8 V reset state when the supply voltage falls, use the reset function of the low-voltage detector, or input the low level to the $\overline{\text{RESET}}$ pin.

2. If the rate at which the voltage rises to 1.8 V after power application is slower than 0.5 V/ms (MIN.), input a low level to the $\overline{\text{RESET}}$ pin before the voltage reaches to 1.8 V, or set LVI to ON by default by using an option byte (option byte: LVIOFF = 0).

3. The reset processing time, such as when waiting for internal voltage stabilization, includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

4. The internal reset processing time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

5. The internal high-speed oscillation clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock [Note 6], use the timer function for confirmation of the lapse of the stabilization time.

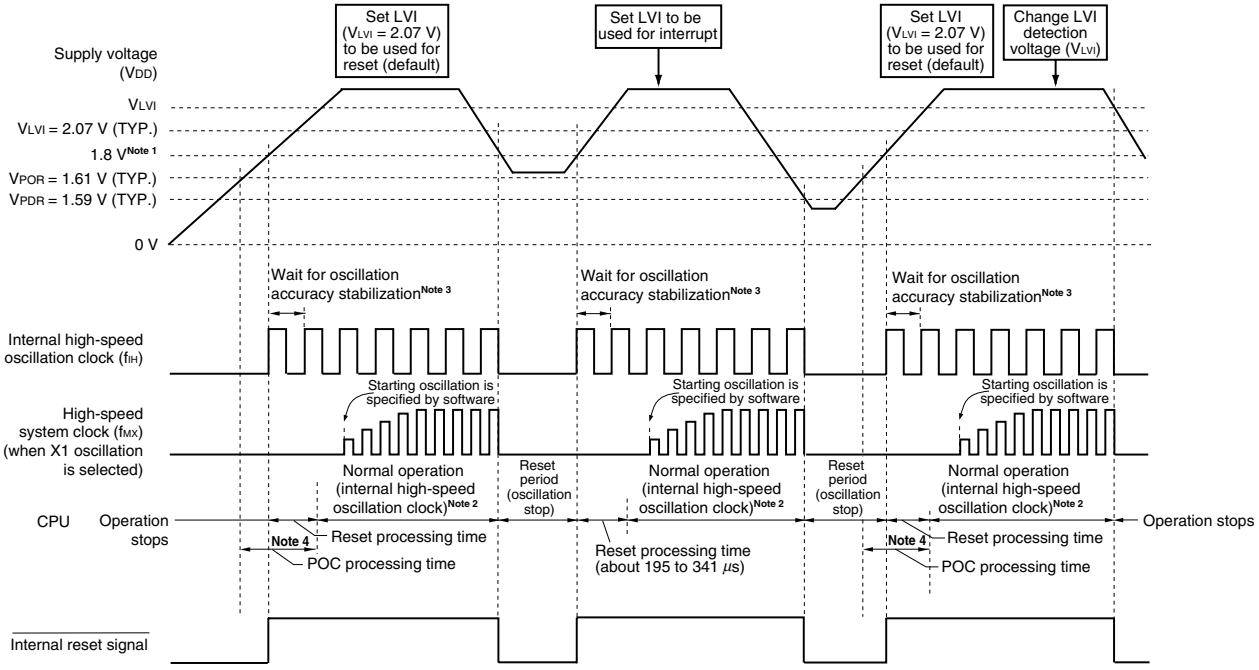
6. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Caution Set the low-voltage detector by software after the reset status is released (see CHAPTER 23 LOW-VOLTAGE DETECTOR).

Remark V_{LVI}: LVI detection voltage
V_{POR}: POC power supply rise detection voltage
V_{PDR}: POC power supply fall detection voltage

Figure 22-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2/2)

(2) When LVI is ON upon power application (option byte: LVIOFF = 0)



Notes 1. The operation guaranteed range is 1.8 V ≤ V_{DD} ≤ 5.5 V. To make the state at lower than 1.8 V reset state when the supply voltage falls, use the reset function of the low-voltage detector, or input the low level to the $\overline{\text{RESET}}$ pin.

2. The internal high-speed oscillation clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock Note 5, use the timer function for confirmation of the lapse of the stabilization time.

3. The internal reset processing time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

4. The following times are required between reaching the POC detection voltage (1.61 V (TYP.)) and starting normal operation.

- When the time to reach 2.07 V (TYP.) from 1.61 V (TYP.) is less than 5.8 ms:
  A POC processing time of 2.12 to 5.84 ms is required between reaching 1.61 V (TYP.) and starting normal operation.
- When the time to reach 2.07 V (TYP.) from 1.61 V (TYP.) is greater than 5.8 ms:
  A reset processing time of 195 to 341 μs is required between reaching 2.07 V (TYP.) and starting normal operation.

5. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Caution Set the low-voltage detector by software after the reset status is released (see CHAPTER 23 LOW-VOLTAGE DETECTOR).

Remark V_{LVI}: LVI detection voltage
V_{POR}: POC power supply rise detection voltage
V_{PDR}: POC power supply fall detection voltage

22.4 Cautions for Power-on-Clear Circuit

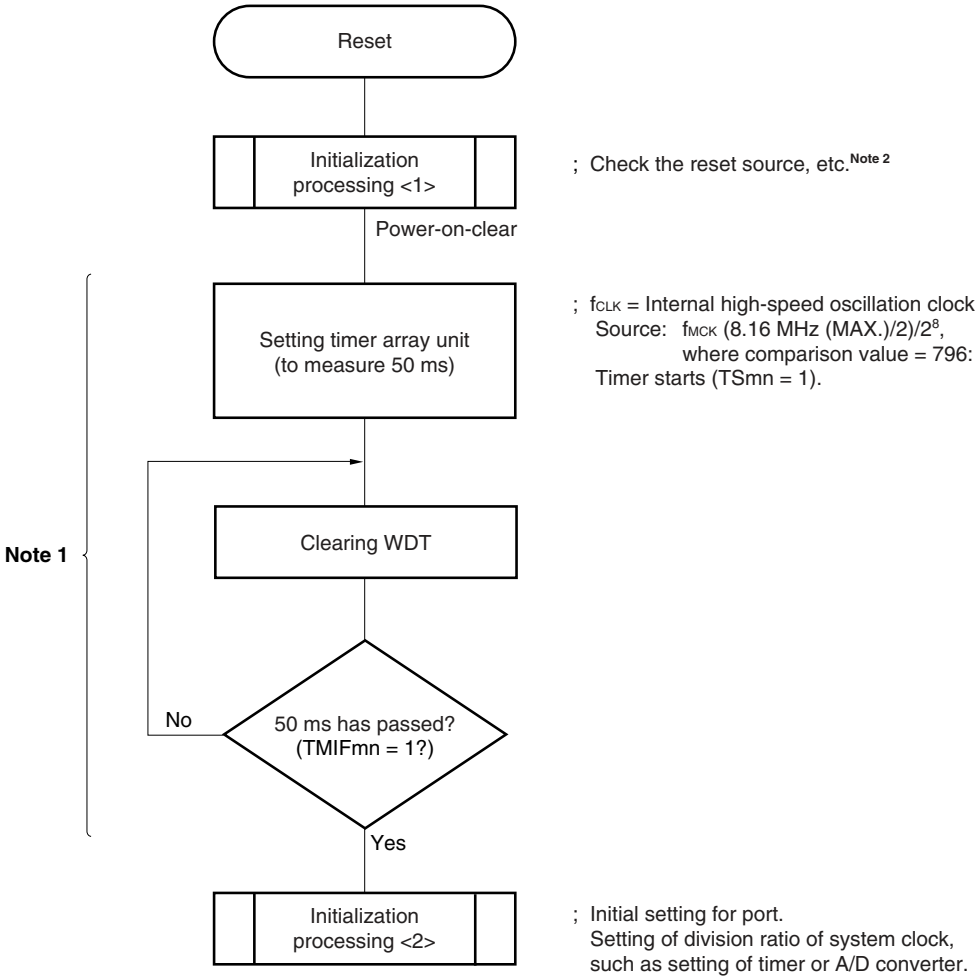
In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the POC detection voltage (V_{POR}, V_{PDR}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

Figure 22-3. Example of Software Processing After Reset Release (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of POC detection voltage



Notes 1. If reset is generated again during this period, initialization processing <2> is not started.

2. A flowchart is shown on the next page.

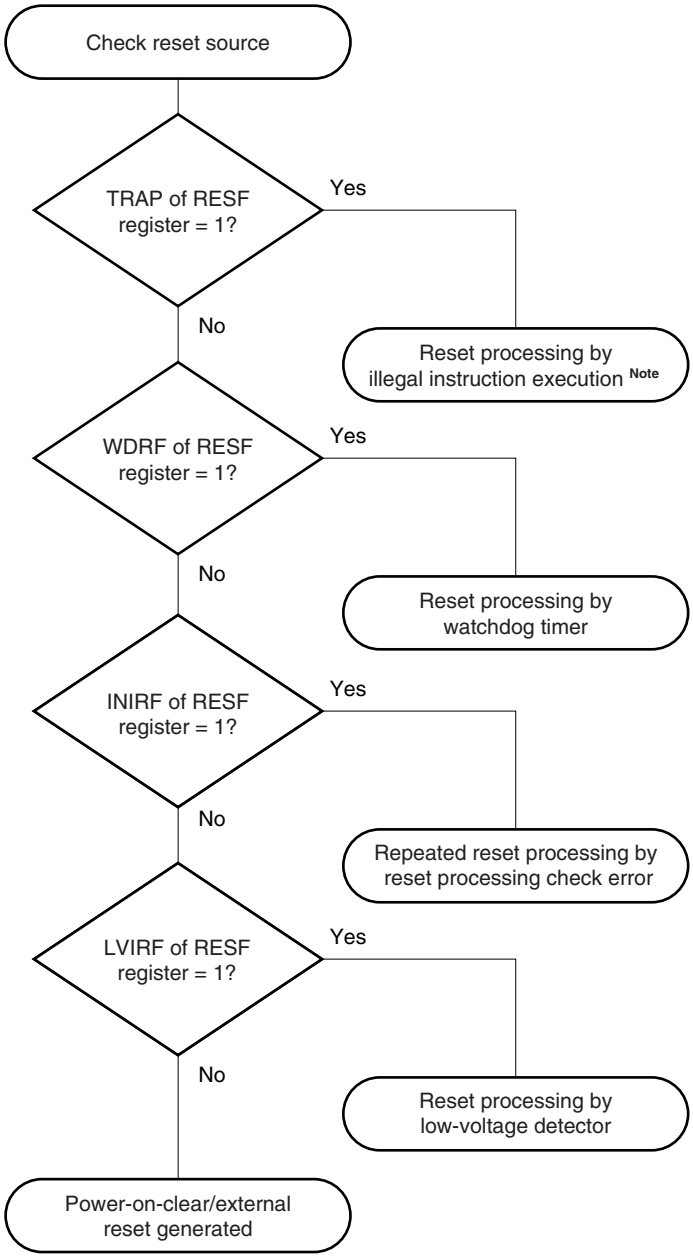
Remark m = 0, 1, n = 0 to 7

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07

78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 22-3. Example of Software Processing After Reset Release (2/2)

• Checking reset source



Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

CHAPTER 23 LOW-VOLTAGE DETECTOR

23.1 Functions of Low-Voltage Detector

The low-voltage detector (LVI) has the following functions.

- The LVI circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVI}) or the input voltage from an external input pin (EXLVI) with the detection voltage (V_{EXLVI} = 1.21 V ±0.1 V), and generates an internal reset or internal interrupt signal.
- The low-voltage detector (LVI) can be set to ON by an option byte by default. If it is set to ON to raise the power supply from the POC detection voltage (V_{POR} = 1.61 V (TYP.)) or lower, the internal reset signal is generated when the supply voltage (V_{DD}) < detection voltage (V_{LVI} = 2.07 V ±0.2 V). After that, the internal reset signal is generated when the supply voltage (V_{DD}) < detection voltage (V_{LVI} = 2.07 V ±0.1 V).
- The supply voltage (V_{DD}) or the input voltage from the external input pin (EXLVI) can be selected to be detected by software.
- A reset or an interrupt can be selected to be generated after detection by software.
- Detection levels (V_{LVI},16 levels) of supply voltage can be changed by software.
- Operable in STOP mode.

The reset and interrupt signals are generated as follows depending on selection by software.

Selection of Level Detection of Supply Voltage (V_{DD}) (LVISEL = 0)		Selection Level Detection of Input Voltage from External Input Pin (EXLVI) (LVISEL = 1)	
Selects reset (LVIMD = 1).	Selects interrupt (LVIMD = 0).	Selects reset (LVIMD = 1).	Selects interrupt (LVIMD = 0).
Generates an internal reset signal when $V_{DD} < V_{LVI}$ and releases the reset signal when $V_{DD} \geq V_{LVI}$.	Generates an internal interrupt signal when V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$).	Generates an internal reset signal when EXLVI < V_{EXLVI} and releases the reset signal when EXLVI ≥ V_{EXLVI}.	Generates an internal interrupt signal when EXLVI drops lower than V_{EXLVI} (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).

Remark LVISEL bit: Bit 2 of the low-voltage detection register (LVIM)
LVIMD bit: Bit 1 of LVIM

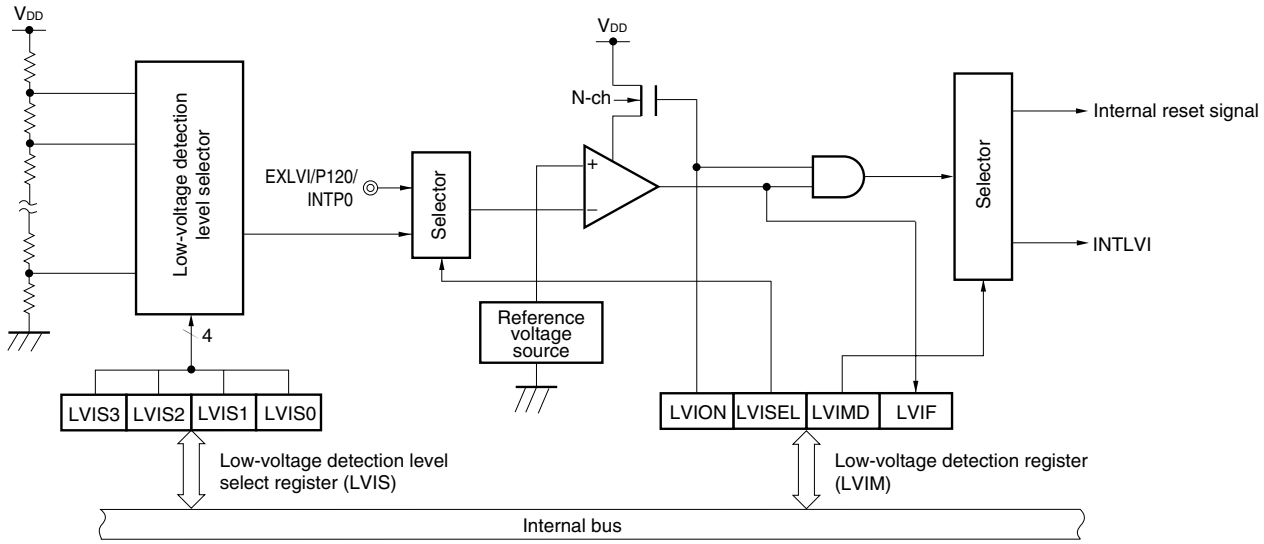
While the low-voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of the low-voltage detection register (LVIM)).

When the low-voltage detector is used to reset, bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of the RESF register, see **CHAPTER 21 RESET FUNCTION**.

23.2 Configuration of Low-Voltage Detector

The block diagram of the low-voltage detector is shown in Figure 23-1.

Figure 23-1. Block Diagram of Low-Voltage Detector



23.3 Registers Controlling Low-Voltage Detector

The low-voltage detector is controlled by the following registers.

- Low-voltage detection register (LVIM)
- Low-voltage detection level select register (LVIS)
- Port mode register 12 (PM12)

(1) Low-voltage detection register (LVIM)

This register sets low-voltage detection and the operation mode.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 23-2. Format of Low-Voltage Detection Register (LVIM)

Address: FFFA9H After reset: 00H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	<2>	<1>	<0>
LVIM	LVION	0	0	0	0	LVISEL	LVIMD	LVIF

LVION[Notes 3, 4]	Enables low-voltage detection operation
0	Disables operation
1	Enables operation

LVISEL[Note 3]	Voltage detection selection
0	Detects level of supply voltage (V_{DD})
1	Detects level of input voltage from the external input pin (EXLVI)

LVIMD	Low-voltage detection operation mode (interrupt/reset) selection
0	• LVISEL = 0: Generates an internal interrupt signal when the supply voltage (V_{DD}) drops lower than the detection voltage (V_{LVI}) ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$). • LVISEL = 1: Generates an interrupt signal when the input voltage from an external input pin (EXLVI) drops lower than the detection voltage (V_{EXLVI}) (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).
1	• LVISEL = 0: Generates an internal reset signal when the supply voltage (V_{DD}) < detection voltage (V_{LVI}) and releases the reset signal when $V_{DD} \geq V_{LVI}$. • LVISEL = 1: Generates an internal reset signal when the input voltage from an external input pin (EXLVI) < detection voltage (V_{EXLVI}) and releases the reset signal when EXLVI ≥ V_{EXLVI}.

LVIF	Low-voltage detection flag
0	• LVISEL = 0: Supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}), or when LVI operation is disabled • LVISEL = 1: Input voltage from the external input pin (EXLVI) ≥ detection voltage (V_{EXLVI}), or when LVI operation is disabled
1	• LVISEL = 0: Supply voltage (V_{DD}) < detection voltage (V_{LVI}) • LVISEL = 1: Input voltage from the external input pin (EXLVI) < detection voltage (V_{EXLVI})

Notes 1. The reset value changes depending on the reset source and the setting of the option byte.
This register is not cleared (00H) by LVI reset.
It is set to “82H” when a reset signal other than LVI is applied if option byte LVIOFF = 0, and to “00H” if option byte LVIOFF = 1.

2. Bit 0 is read-only.

3. The LVION, LVIMD, and LVISEL bits are cleared to 0 in the case of a reset other than an LVI reset. These are not cleared to 0 in the case of an LVI reset.

Note 4. When the LVION bit is set to 1, operation of the comparator in the LVI circuit is started. Use software to wait for the following periods of time, between when the LVION bit is set to 1 and when the voltage is confirmed with LVIF flag.

- Operation stabilization time (10 μs (MAX.))
- Minimum pulse width (200 μs (MIN.))

The LVIF flag value for these periods may be set/cleared regardless of the voltage level, and can therefore not be used. Also, the LVIIF interrupt request flag may be set to 1 in these periods.

Cautions 1. To stop LVI, be sure to clear (0) the LVION bit by using a 1-bit memory manipulation instruction.

2. Input voltage from the external input pin (EXLVI) must be EXLVI < V_{DD}.

3. When LVI is used in interrupt mode (LVIMD = 0) and the LVISEL bit is set to 0, an interrupt request signal (INTLVI) that disables LVI operation (clears the LVION bit) when the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}) (if LVISEL = 1, input voltage of the external input pin (EXLVI) is less than or equal to the detection voltage (V_{EXLVI})) is generated and LVIIF flag may be set to 1.

4. To read the LVIM register after writing this register, secure the time of one or more clock.

(2) Low-voltage detection level select register (LVIS)

This register selects the low-voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation input sets this register to 0EH.

Figure 23-3. Format of Low-Voltage Detection Level Select Register (LVIS)

Address: FFFAAH After reset: 0EH[Note] R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V_{LVI0} (4.22 ±0.1 V)
0	0	0	1	V_{LVI1} (4.07 ±0.1 V)
0	0	1	0	V_{LVI2} (3.92 ±0.1 V)
0	0	1	1	V_{LVI3} (3.76 ±0.1 V)
0	1	0	0	V_{LVI4} (3.61 ±0.1 V)
0	1	0	1	V_{LVI5} (3.45 ±0.1 V)
0	1	1	0	V_{LVI6} (3.30 ±0.1 V)
0	1	1	1	V_{LVI7} (3.15 ±0.1 V)
1	0	0	0	V_{LVI8} (2.99 ±0.1 V)
1	0	0	1	V_{LVI9} (2.84 ±0.1 V)
1	0	1	0	V_{LVI10} (2.68 ±0.1 V)
1	0	1	1	V_{LVI11} (2.53 ±0.1 V)
1	1	0	0	V_{LVI12} (2.38 ±0.1 V)
1	1	0	1	V_{LVI13} (2.22 ±0.1 V)
1	1	1	0	V_{LVI14} (2.07 ±0.1 V)
1	1	1	1	V_{LVI15} (1.91 ±0.1 V)

Note The reset value changes depending on the reset source.
If the LVIS register is reset by LVI, it is not reset but holds the current value. The value of this register is reset to “0EH” if a reset other than by LVI is effected.

Caution 1. Be sure to clear bits 4 to 7 to “0”.

Cautions 2. Change the low-voltage detection level select register (LVIS) value with either of the following methods.

- **When changing the value after stopping LVI**
  - **<1> Stop LVI (LVION = 0).**
  - **<2> Change the LVIS register.**
  - **<3> Set to the mode used as an interrupt (LVIMD = 0).**
  - **<4> Mask LVI interrupts (LVIMK = 1).**
  - **<5> Enable LVI operation (LVION = 1).**
  - **<6> Before cancelling the LVI interrupt mask (LVIMK = 0), clear it with software because an LVIIF flag may be set when LVI operation is enabled.**
- **When changing the value after setting to the mode used as an interrupt (LVIMD = 0)**
  - **<1> Mask LVI interrupts (LVIMK = 1).**
  - **<2> Set to the mode used as an interrupt (LVIMD = 0).**
  - **<3> Change the LVIS register.**
  - **<4> Before cancelling the LVI interrupt mask (LVIMK = 0), clear it with software because an LVIIF flag may be set when the LVIS register is changed.**

3. When an input voltage from the external input pin (EXLVI) is detected, the detection voltage (V_{EXLVI}) is fixed. Therefore, setting of the LVIS register is not necessary.

4. To read the LVIS register after writing this register, secure the time of one or more clock.

(3) Port mode register 12 (PM12)

When using the P120/EXLVI/INTP0 pin for external low-voltage detection potential input, set the PM120 bit to 1. At this time, the output latch of P120 may be 0 or 1.

The PM12 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 23-4. Format of Port Mode Register 12 (PM12)

Address: FFF2CH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM12	1	1	1	1	1	1	1	PM120

PM120	P120 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

23.4 Operation of Low-Voltage Detector

The low-voltage detector can be used in the following two modes.

(1) Used as reset (LVIMD = 1)

- If LVISEL = 0, compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}), generates an internal reset signal when $V_{DD} < V_{LVI}$, and releases internal reset when $V_{DD} \geq V_{LVI}$.
- If LVISEL = 1, compares the input voltage from the external input pin (EXLVI) and detection voltage (V_{EXLVI} = 1.21 V ±0.1 V), generates an internal reset signal when EXLVI < V_{EXLVI}, and releases internal reset when EXLVI ≥ V_{EXLVI}.

Remark The low-voltage detector (LVI) can be set to ON by an option byte by default. If it is set to ON to raise the power supply from the POC detection voltage (V_{POR} = 1.61 V (TYP.)) or lower, the internal reset signal is generated when the supply voltage (V_{DD}) < detection voltage (V_{LVI} = 2.07 V ±0.2 V). After that, the internal reset signal is generated when the supply voltage (V_{DD}) < detection voltage (V_{LVI} = 2.07 V ±0.1 V).

(2) Used as interrupt (LVIMD = 0)

- If LVISEL = 0, compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}). When V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$), generates an interrupt signal (INTLVI).
- If LVISEL = 1, compares the input voltage from the external input pin (EXLVI) and detection voltage (V_{EXLVI} = 1.21 V ±0.1 V). When EXLVI drops lower than V_{EXLVI} (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}), generates an interrupt signal (INTLVI).

While the low-voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of the low-voltage detection register (LVIM)).

Remark LVIMD bit: Bit 1 of the LVIM register
LVISEL bit: Bit 2 of the LVIM register

23.4.1 When used as reset

(1) When detecting level of supply voltage (V_{DD})

(a) When LVI default start function stopped is set (LVIOFF = 1)

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (detects level of supply voltage (V_{DD})) (default value).
  - <3> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).
  - <4> Set bit 7 (LVION) of the LVIM register to 1 (enables LVI operation).
  - <5> Use software to wait for the following periods of time (Total 210 μs).
    - Operation stabilization time (10 μs (MAX.))
    - Minimum pulse width (200 μs (MIN.))
  - <6> Wait until it is checked that (supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})) by bit 0 (LVIF) of the LVIM register.
  - <7> Set bit 1 (LVIMD) of the LVIM register to 1 (generates reset when the level is detected).

  Figure 23-5 shows the timing of the internal reset signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <7> above.

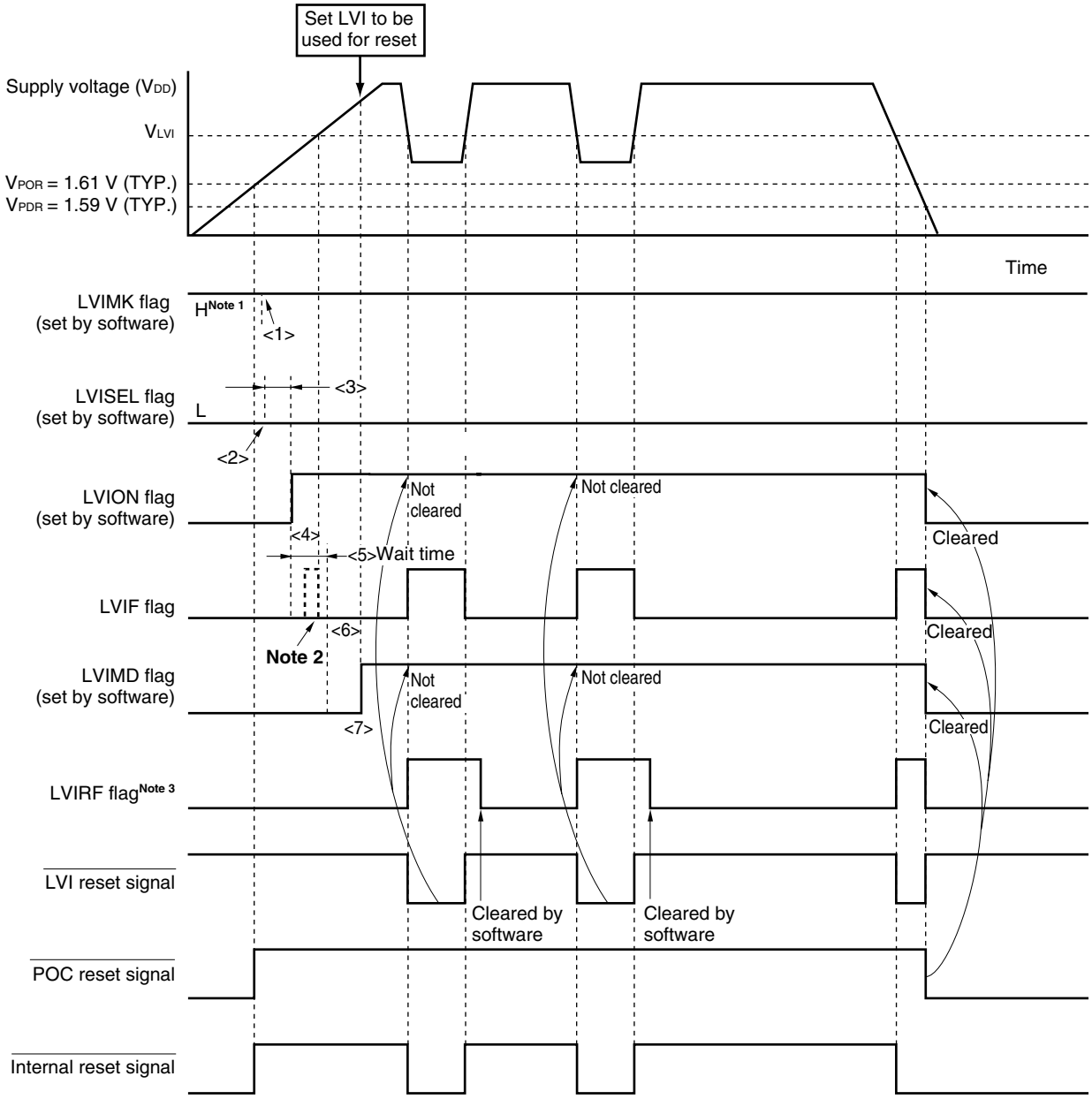
  Cautions 1. Be sure to execute <1>. When LVIMK = 0, an interrupt may occur immediately after the processing in <4>.

  2. If supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}) when the LVIMD bit is set to 1, an internal reset signal is not generated.

- When stopping operation

  Be sure to clear (0) the LVIMD bit and then the LVION bit by using a 1-bit memory manipulation instruction.

Figure 23-5. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The LVIIF flag of the interrupt request flag registers and the LVIF flag may be set (1).

3. LVIRF flag is bit 0 of the reset control flag register (RESF). For details of the RESF register, see **CHAPTER 21 RESET FUNCTION**.

Remarks 1. <1> to <7> in Figure 23-5 above correspond to <1> to <7> in the description of "When starting operation" in **23.4.1 (1) (a) When LVI default start function stopped is set (LVIOFF = 1).**

2. V_{POR}: POC power supply rise detection voltage
V_{PDR}: POC power supply fall detection voltage

(b) When LVI default start function enabled is set (LVIOFF = 0)

- When starting operation

  Start in the following initial setting state.

  - Set bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 (enables LVI operation)
  - Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (detects level of supply voltage (V_{DD}))
  - Set the low-voltage detection level selection register (LVIS) to 0EH (default value: V_{LVI} = 2.07 V ±0.1 V).
  - Set bit 1 (LVIMD) of the LVIM register to 1 (generates reset when the level is detected)
  - Set bit 0 (LVIF) of the LVIM register to 0 (“Supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})”)

  Figure 23-6 shows the timing of the internal reset signal generated by the low-voltage detector.

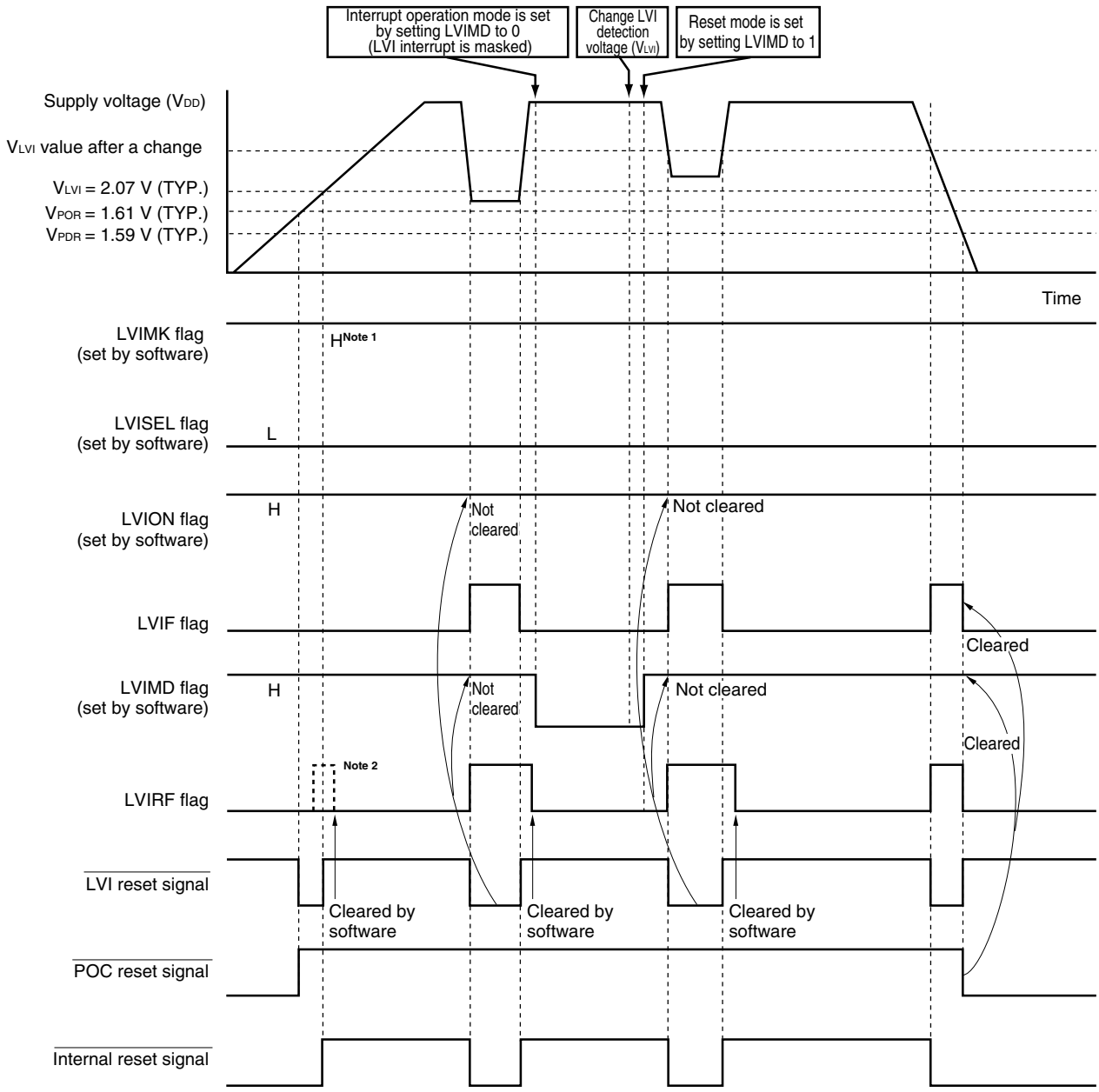
- When stopping operation

  Be sure to clear (0) the LVIMD bit and then the LVION bit by using a 1-bit memory manipulation instruction.

Caution Even when the LVI default start function is used, if it is set to LVI operation prohibition by the software (Set bit 7 (LVION) of the low-voltage detection register (LVIM) to 0), it operates as follows:

- **Does not perform low-voltage detection during LVION = 0.**
- **If a reset is generated while LVION = 0, the LVION bit will be re-set to 1 when the CPU starts after reset release. There is a period when low-voltage detection cannot be performed normally, however, when a reset occurs due to WDT and illegal instruction execution.**
  This is due to the fact that while the pulse width detected by LVI must be 200 μs max., LVION = 1 is set upon reset occurrence, and the CPU starts operating without waiting for the LVI stabilization time.

Figure 23-6. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 0)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. LVIRF flag is bit 0 of the reset control flag register (RESF).
When the LVI default start function (bit 0 (LVIOFF) of 000C1H = 0) is used, the LVIRF flag may become 1 from the beginning due to the power-on waveform.
For details of the RESF register, see **CHAPTER 21 RESET FUNCTION**.

Remark V_{POR}: POC power supply rise detection voltage
V_{PDR}: POC power supply fall detection voltage

(2) When detecting level of input voltage from external input pin (EXLVI)

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Set bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 1 (detects level of input voltage from the external input pin (EXLVI)).
  - <3> Set bit 7 (LVION) of the LVIM register to 1 (enables LVI operation).
  - <4> Use software to wait for the following periods of time (Total 210 μs).
    - Operation stabilization time (10 μs (MAX.))
    - Minimum pulse width (200 μs (MIN.))
  - <5> Wait until it is checked that (input voltage from the external input pin (EXLVI) ≥ detection voltage (V_{EXLVI} = 1.21 V (TYP.))) by bit 0 (LVIF) of the LVIM register.
  - <6> Set bit 1 (LVIMD) of the LVIM register to 1 (generates reset signal when the level is detected).

Figure 23-7 shows the timing of the internal reset signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <6> above.

Cautions 1. Be sure to execute <1>. When LVIMK = 0, an interrupt may occur immediately after the processing in <3>.

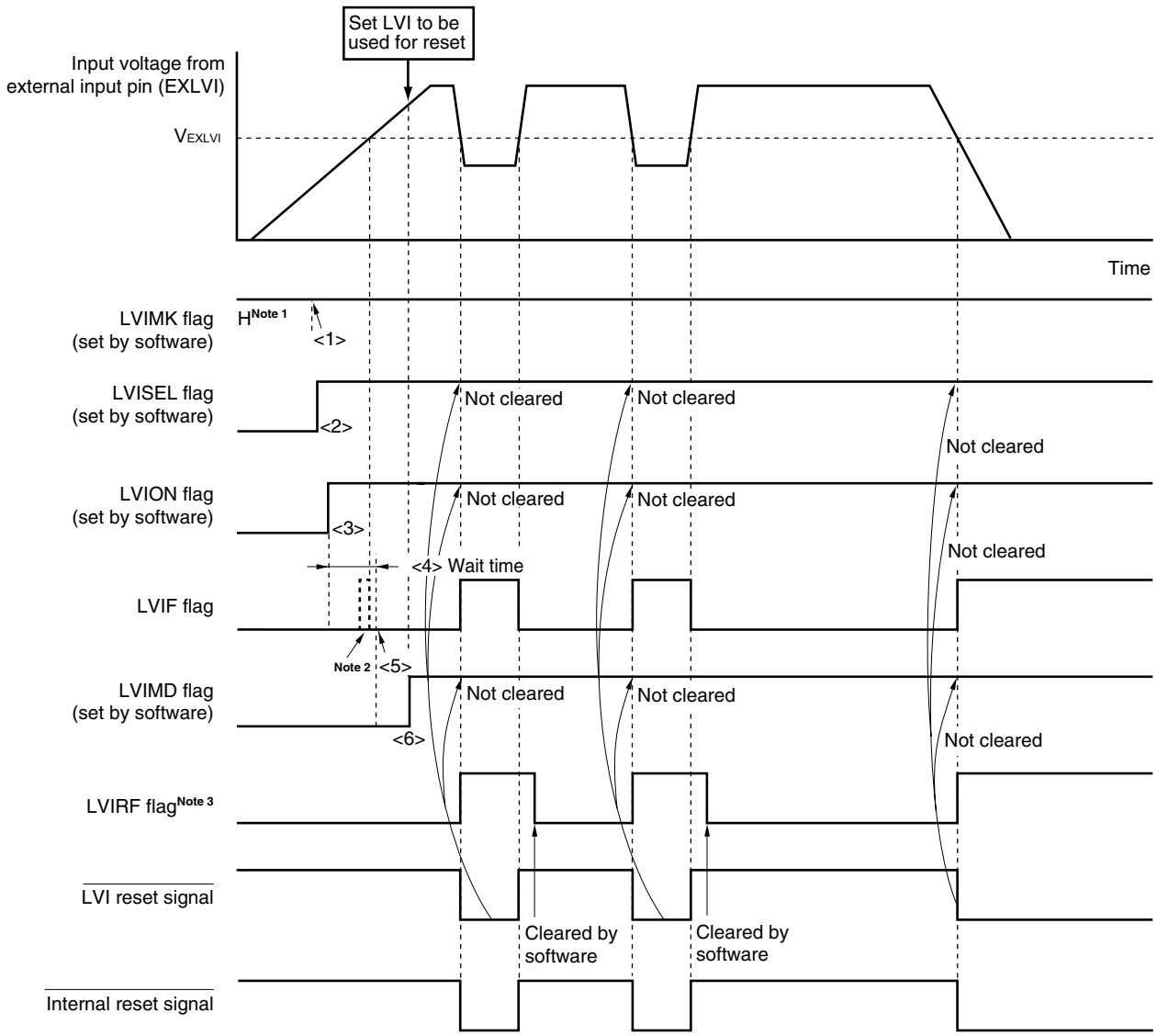
2. If input voltage from the external input pin (EXLVI) ≥ detection voltage (V_{EXLVI} = 1.21 V (TYP.)) when the LVIMD bit is set to 1, an internal reset signal is not generated.

3. Input voltage from the external input pin (EXLVI) must be EXLVI < V_{DD}.

- When stopping operation

Be sure to clear (0) the LVIMD bit and then the LVION bit by using a 1-bit memory manipulation instruction.

Figure 23-7. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The LVIIF flag of the interrupt request flag registers and the LVIF flag may be set (1).

3. LVIRF flag is bit 0 of the reset control flag register (RESF). For details of the RESF register, see **CHAPTER 21 RESET FUNCTION**.

Remark <1> to <6> in Figure 23-7 above correspond to <1> to <6> in the description of "When starting operation" in **23.4.1 (2) When detecting level of input voltage from external input pin (EXLVI)**.

23.4.2 When used as interrupt

(1) When detecting level of supply voltage (V_{DD})

(a) When LVI default start function stopped is set (LVIOFF = 1)

- When starting operation

<1> Mask the LVI interrupt (LVIMK = 1).

<2> Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (detects level of supply voltage (V_{DD})) (default value).
Clear bit 1 (LVIMD) of the LVIM register to 0 (generates interrupt signal when the level is detected) (default value).

<3> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).

<4> Set bit 7 (LVION) of the LVIM register to 1 (enables LVI operation).

<5> Use software to wait for the following periods of time (Total 210 μs).
- Operation stabilization time (10 μs (MAX.))
- Minimum pulse width (200 μs (MIN.))

<6> Confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, at bit 0 (LVIF) of the LVIM register.

<7> Clear the interrupt request flag of LVI (LVIIF) to 0.

<8> Release the interrupt mask flag of LVI (LVIMK).

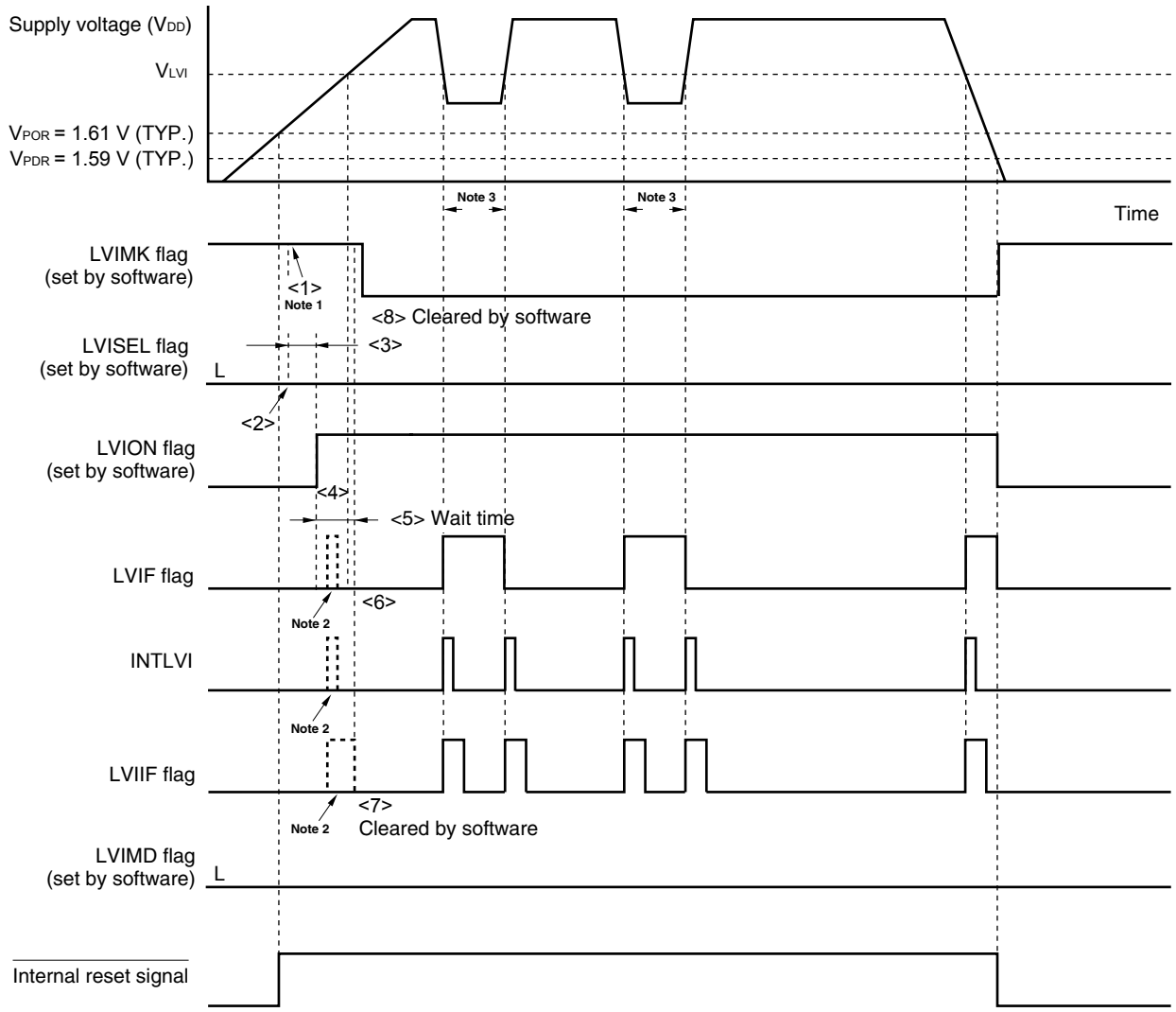
<9> Execute the EI instruction (when vector interrupts are used).

Figure 23-8 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <8> above.

- When stopping operation

Be sure to clear (0) the LVION bit by using a 1-bit memory manipulation instruction.

Figure 23-8. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVI operation is disabled (clears the LVION bit) when the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), an interrupt request signal (INTLVI) is generated and the LVIIF flag may be set to 1.

Remarks 1. <1> to <8> in Figure 23-8 above correspond to <1> to <8> in the description of "When starting operation" in **23.4.2 (1) (a) When LVI default start function stopped is set (LVIOFF = 1).**

2. V_{POR}: POC power supply rise detection voltage
V_{PDR}: POC power supply fall detection voltage

(b) When LVI default start function enabled is set (LVIOFF = 0)

- When starting operation

<1> Start in the following initial setting state.

- Set bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 (enables LVI operation)
- Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (detects level of supply voltage (V_{DD}))
- Set the low-voltage detection level selection register (LVIS) to 0EH (default value: V_{LVI} = 2.07 V ±0.1 V).
- Set bit 1 (LVIMD) of the LVIM register to 1 (generates reset when the level is detected)
- Set bit 0 (LVIF) of the LVIM register to 0 (Detects falling edge "Supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})")

<2> Clear bit 1 (LVIMD) of the LVIM register to 0 (generates interrupt signal when the level is detected) (default value).

<3> Release the interrupt mask flag of LVI (LVIMK).

<4> Execute the EI instruction (when vector interrupts are used).

Figure 23-9 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <3> above.

- When stopping operation

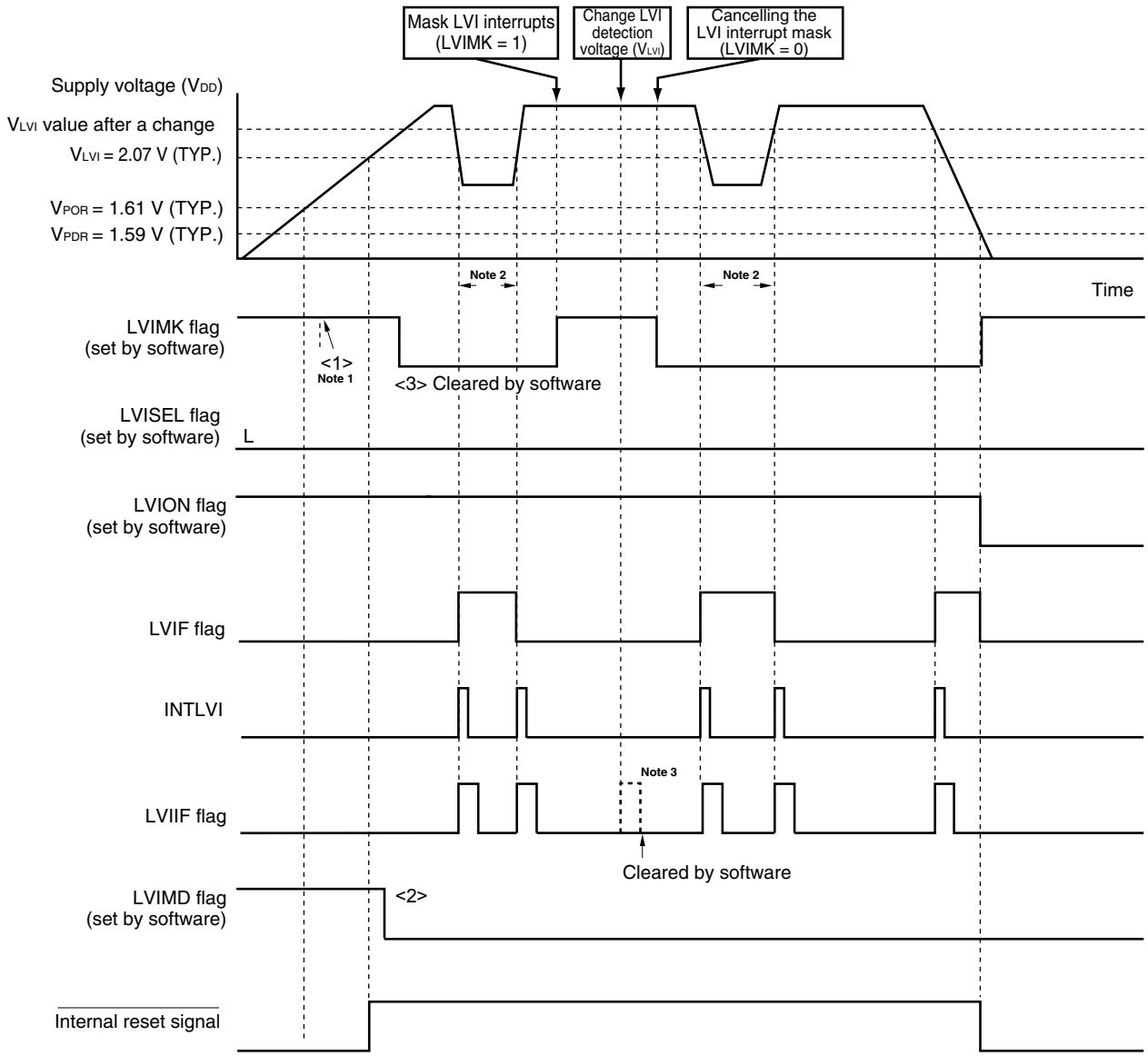
Be sure to clear (0) the LVION bit by using a 1-bit memory manipulation instruction.

Cautions 1. Even when the LVI default start function is used, if it is set to LVI operation prohibition by the software, it operates as follows:

- **Does not perform low-voltage detection during LVION = 0.**
- **If a reset is generated while LVION = 0, LVION will be re-set to 1 when the CPU starts after reset release. There is a period when low-voltage detection cannot be performed normally, however, when a reset occurs due to WDT and illegal instruction execution.**
  This is due to the fact that while the pulse width detected by LVI must be 200 μs max., LVION = 1 is set upon reset occurrence, and the CPU starts operating without waiting for the LVI stabilization time.

2. When the LVI default start function (bit 0 (LVIOFF) of 000C1H = 0) is used, the LVIRF flag may become 1 from the beginning due to the power-on waveform.
For details of the RESF register, see CHAPTER 21 RESET FUNCTION.

Figure 23-9. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 0)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. If LVI operation is disabled (clears the LVION bit) when the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), an interrupt request signal (INTLVI) is generated and the LVIIF flag may be set to 1.

3. The LVIIF flag may be set when the LVI detection voltage is changed.

Remarks 1. <1> to <3> in Figure 23-9 above correspond to <1> to <3> in the description of "When starting operation" in **23.4.2 (1) (b) When LVI default start function enabled is set (LVIOFF = 0).**

2. V_{POR}: POC power supply rise detection voltage
V_{PDR}: POC power supply fall detection voltage

(2) When detecting level of input voltage from external input pin (EXLVI)

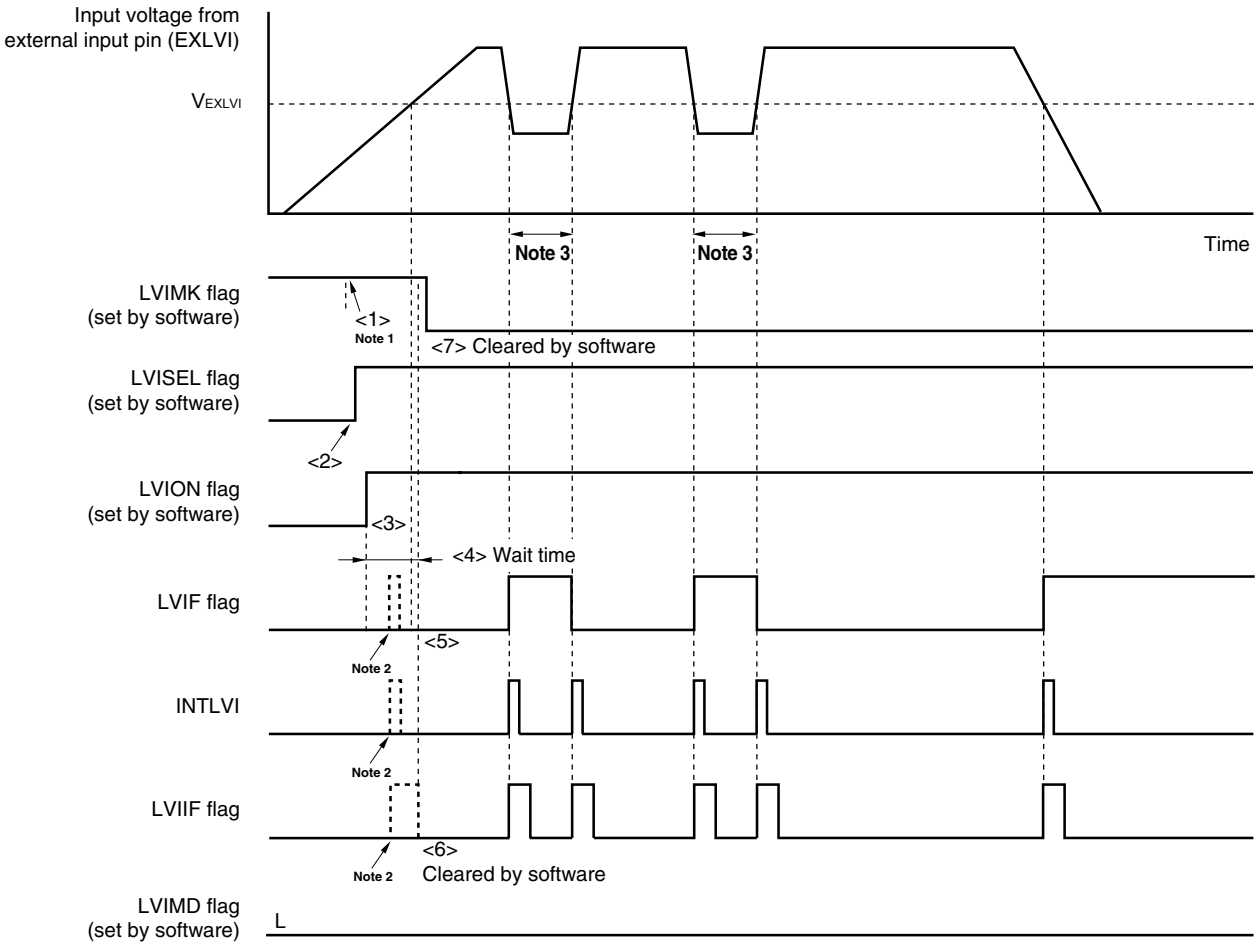
- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Set bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 1 (detects level of input voltage from the external input pin (EXLVI)).
    Clear bit 1 (LVIMD) of the LVIM register to 0 (generates interrupt signal when the level is detected) (default value).
  - <3> Set bit 7 (LVION) of the LVIM register to 1 (enables LVI operation).
  - <4> Use software to wait for the following periods of time (Total 210 μs).
    - Operation stabilization time (10 μs (MAX.))
    - Minimum pulse width (200 μs (MIN.))
  - <5> Confirm that "input voltage from the external input pin (EXLVI) ≥ detection voltage (V_{EXLVI} = 1.21 V (TYP.))" when detecting the falling edge of EXLVI, or "input voltage from the external input pin (EXLVI) < detection voltage (V_{EXLVI} = 1.21 V (TYP.))" when detecting the rising edge of EXLVI, at bit 0 (LVIF) of the LVIM register.
  - <6> Clear the interrupt request flag of LVI (LVIIF) to 0.
  - <7> Release the interrupt mask flag of LVI (LVIMK).
  - <8> Execute the EI instruction (when vector interrupts are used).

Figure 23-10 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <7> above.

Caution Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.

- When stopping operation
  Be sure to clear (0) the LVION bit by using a 1-bit memory manipulation instruction.

Figure 23-10. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 1)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVI operation is disabled (clears the LVION bit) when the input voltage of the external input pin (EXLVI) is less than or equal to the detection voltage (V_{EXLVI}), an interrupt request signal (INTLVI) is generated and the LVIIF flag may be set to 1.

Remark <1> to <7> in Figure 23-10 above correspond to <1> to <7> in the description of “When starting operation” in **23.4.2 (2) When detecting level of input voltage from external input pin (EXLVI)**.

23.5 Cautions for Low-Voltage Detector

(1) Measures method when supply voltage (V_{DD}) frequently fluctuates in the vicinity of the LVI detection voltage (V_{LVI})

In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the LVI detection voltage (V_{LVI}), the operation is as follows depending on how the low-voltage detector is used.

Operation example 1: When used as reset

The system may be repeatedly reset and released from the reset status.

The time from reset release through microcontroller operation start can be set arbitrarily by the following action.

<Action>

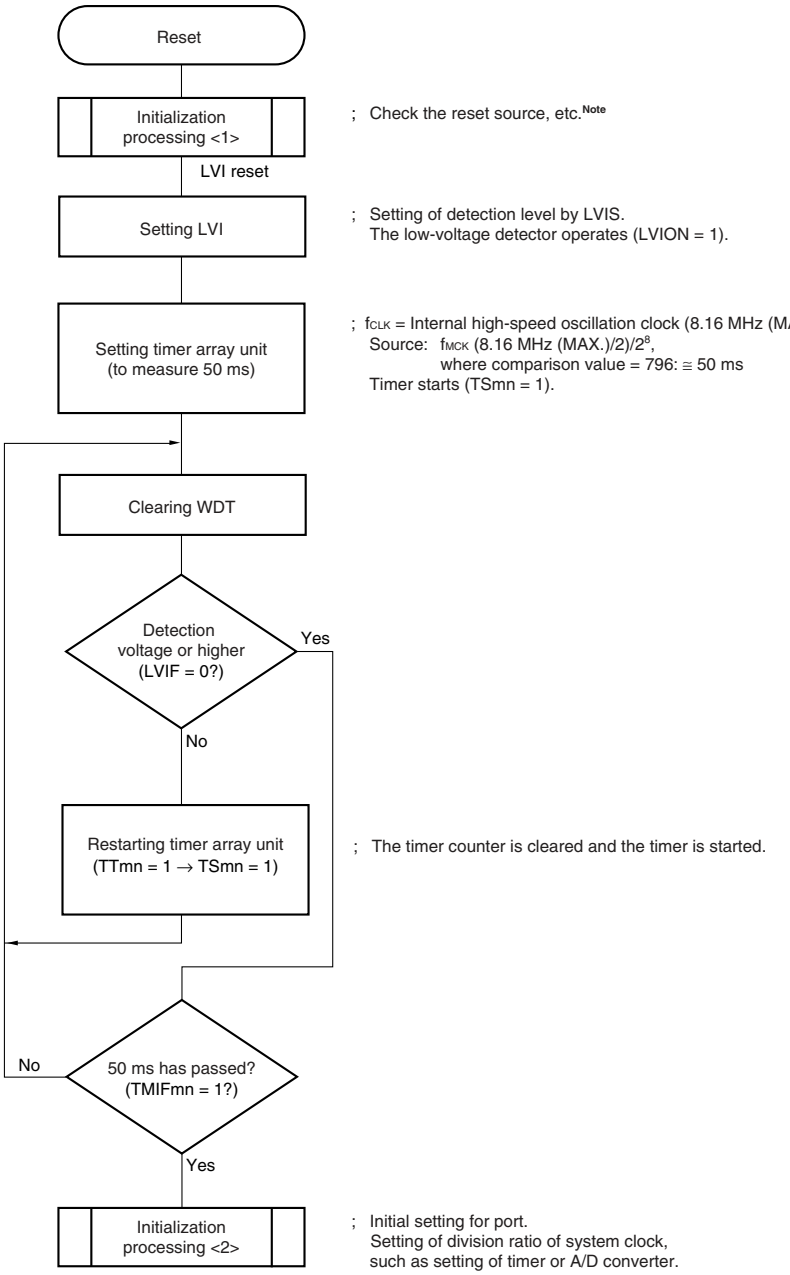
After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports (see **Figure 23-11**).

Remark If bit 2 (LVISEL) of the low voltage detection register (LVIM) is set to “1”, the meanings of the above words change as follows.

- Supply voltage (V_{DD}) → Input voltage from the external input pin (EXLVI)
- Detection voltage (V_{LVI}) → Detection voltage (V_{EXLVI} = 1.21 V)

Figure 23-11. Example of Software Processing After Reset Release (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of LVI detection voltage



Note A flowchart is shown on the next page.

Remarks 1. If bit 2 (LVISEL) of the low voltage detection register (LVIM) is set to "1", the meanings of the above words change as follows.

- Supply voltage (V_{DD}) → Input voltage from the external input pin (EXLVI)
- Detection voltage (V_{LVI}) → Detection voltage (V_{EXLVI} = 1.21 V)

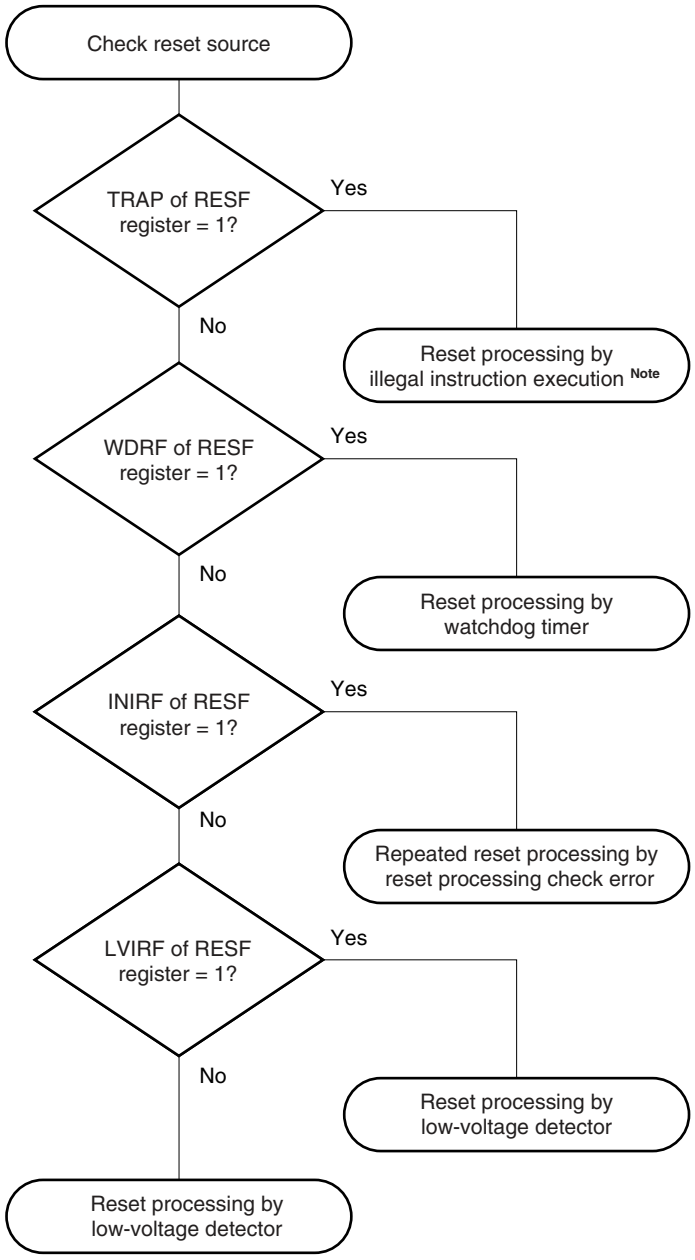
2. Remark m = 0, 1, n = 0 to 7

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07

78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 23-11. Example of Software Processing After Reset Release (2/2)

• Checking reset source



Note When instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Remark If bit 2 (LVISEL) of the low voltage detection register (LVIM) is set to "1", the meanings of the above words change as follows.

- Supply voltage (V_{DD}) → Input voltage from the external input pin (EXLVI)
- Detection voltage (V_{LVI}) → Detection voltage (V_{EXLVI} = 1.21 V)

Operation example 2: When used as interrupt

Interrupt requests may be generated frequently.

Take the following action.

<Action>

Confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, in the servicing routine of the LVI interrupt by using bit 0 (LVIF) of the low-voltage detection register (LVIM). Clear bit 1 (LVIIF) of interrupt request flag register 0L (IF0L) to 0.

For a system with a long supply voltage fluctuation period near the LVI detection voltage, take the above action after waiting for the supply voltage fluctuation time.

Remark If bit 2 (LVISEL) of the low voltage detection register (LVIM) is set to "1", the meanings of the above words change as follows.

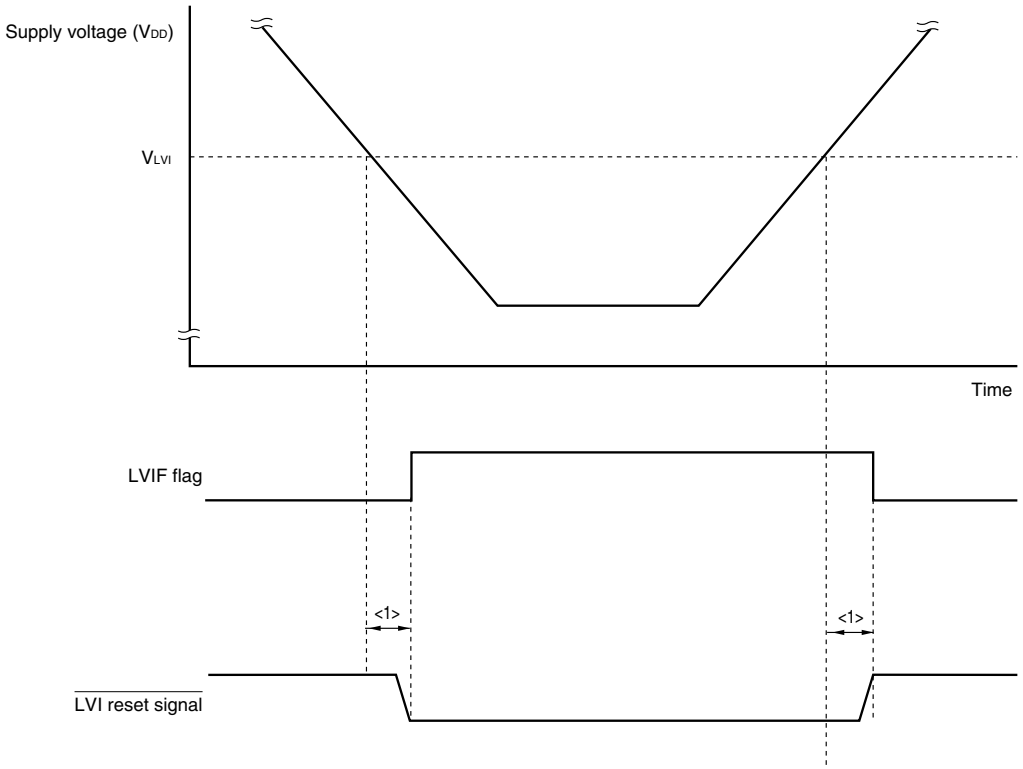
- Supply voltage (V_{DD}) → Input voltage from the external input pin (EXLVI)
- Detection voltage (V_{LVI}) → Detection voltage (V_{EXLVI} = 1.21 V)

(2) Delay from the time LVI reset source is generated until the time LVI reset has been generated or released

There is some delay from the time supply voltage (V_{DD}) < LVI detection voltage (V_{LVI}) until the time LVI reset has been generated.

In the same way, there is also some delay from the time LVI detection voltage (V_{LVI}) ≤ supply voltage (V_{DD}) until the time LVI reset has been released (see **Figure 23-12**).

Figure 23-12. Delay from the time LVI reset source is generated until the time LVI reset has been generated or released



<1>: Minimum pulse width (200 μs (MIN.))

CHAPTER 24 REGULATOR

24.1 Regulator Overview

The 78K0R/Kx3-L contains a circuit for operating the device with a constant voltage. At this time, in order to stabilize the regulator output voltage, connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

The regulator output voltage is normally 2.4 V (typ.), and in the low consumption current mode, 1.8 V (typ.).

24.2 Registers Controlling Regulator

(1) Regulator mode control register (RMC)

This register sets the output voltage of the regulator.

The RMC register is set with an 8-bit memory manipulation instruction.

Reset input sets this register to 00H.

Figure 24-1. Format of Regulator Mode Control Register (RMC)

Address: F00F4H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
RMC								

RMC[7:0]	Control of output voltage of regulator
5AH	Fixed to low consumption current mode (1.8 V)
00H	Switches normal current mode (2.4 V) and low consumption current mode (1.8 V) according to the condition (refer to **Table 24-1**)
Other than above	Setting prohibited

Cautions 1. When using the setting fixed to the low consumption current mode, the RMC register can be used in the following cases.

<When X1 clock is selected as the CPU clock> $f_X \leq 5$ MHz and $f_{CLK} \leq 1$ MHz

<When the high-speed internal oscillation clock, external input clock, or subsystem clock are selected for the CPU clock> $f_{CLK} \leq 1$ MHz

(Caution is given on the next page.)

Caution 2. A wait is required to change the operation speed mode control register (OSMC) after changing the regulator mode control register (RMC). Wait for 3.5 ms by software when setting to low consumption current mode and 10 μs when setting to normal current mode, as described in the procedure shown below.

• When setting to low consumption current mode

<1> Select a frequency of 1 MHz for f_{CLK}.
<2> Set the RMC register to 5AH (set the regulator to low consumption current mode).
<3> Wait for 3.5 ms.
<4> Set the FLPC and FSEL bits of the OSMC register to 1 and 0, respectively.

• When setting to normal current mode

<1> Set the RMC register to 00H (set the regulator to normal current mode).
<2> Wait for 10 μs.
<3> Change the FLPC and FSEL bits of the OSMC register.
<4> Change the f_{CLK} frequency.

Table 24-1. Regulator Output Voltage Conditions

Mode	Output Voltage	Condition
Low consumption current mode	1.8 V	In STOP mode (except during OCD mode)
		When both the high-speed system clock (f_{MX}), the high-speed internal oscillation clock (f_{IH}), and the 20 MHz internal high-speed oscillation clock (f_{IH20}) are stopped during CPU operation with the subsystem clock (f_{XT})[Note]
		When both the high-speed system clock (f_{MX}), the high-speed internal oscillation clock (f_{IH}), and the 20 MHz internal high-speed oscillation clock (f_{IH20}) are stopped during the HALT mode when the CPU operation with the subsystem clock (f_{XT}) has been set[Note]
Normal current mode	2.4 V	Other than above

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock. These conditions apply to products other than the 78K0R/KC3-L (40-pin).

CHAPTER 25 OPTION BYTE

25.1 Functions of Option Bytes

Addresses 000C0H to 000C3H of the flash memory of the 78K0R/Kx3-L form an option byte area.

Option bytes consist of user option byte (000C0H to 000C2H) and on-chip debug option byte (000C3H).

Upon power application or resetting and starting, an option byte is automatically referenced and a specified function is set. When using the product, be sure to set the following functions by using the option bytes.

To use the boot swap operation during self programming, 000C0H to 000C3H are replaced by 010C0H to 010C3H. Therefore, set the same values as 000C0H to 000C3H to 010C0H to 010C3H.

Caution Be sure to set FFH to 000C2H (000C2H/010C2H when the boot swap operation is used).

25.1.1 User option byte (000C0H to 000C2H/010C0H to 010C2H)

(1) 000C0H/010C0H

- ○ Operation of watchdog timer
  - Operation is stopped or enabled in the HALT or STOP mode.
- ○ Setting of interval time of watchdog timer
- ○ Operation of watchdog timer
  - Operation is stopped or enabled.
- ○ Setting of window open period of watchdog timer
- ○ Setting of interval interrupt of watchdog timer
  - Used or not used

Caution Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.

(2) 000C1H/010C1H

- ○ Setting of LVI upon reset release (upon power application)
  - LVI is ON or OFF by default upon reset release (reset by the $\overline{\text{RESET}}$ pin excluding LVI, POC, WDT, or illegal instructions).
- ○ Setting of internal high-speed oscillator frequency
  - Select from 1 MHz, 8 MHz, or 20 MHz.

Caution Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

(3) 000C2H/010C2H

- ○ Be sure to set FFH, as these addresses are reserved areas.

Caution Set FFH to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

25.1.2 On-chip debug option byte (000C3H/ 010C3H)

- Control of on-chip debug operation
  - On-chip debug operation is disabled or enabled.
- Handling of data of flash memory in case of failure in on-chip debug security ID authentication
  - Data of flash memory is erased or not erased in case of failure in on-chip debug security ID authentication.

Caution Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

25.2 Format of User Option Byte

The format of user option byte is shown below.

Figure 25-1. Format of User Option Byte (000C0H/010C0H) (1/2)

Address: 000C0H/010C0H[Note 1]

7	6	5	4	3	2	1	0
WDTINIT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON

WDTINIT	Use of interval interrupt of watchdog timer
0	Interval interrupt is not used.
1	Interval interrupt is generated when 75% of the overflow time is reached.

WINDOW1	WINDOW0	Watchdog timer window open period[Note 2]
0	0	Setting prohibited
0	1	50%
1	0	75%
1	1	100%

WDTON	Operation control of watchdog timer counter
0	Counter operation disabled (counting stopped after reset)
1	Counter operation enabled (counting started after reset)

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time (f_{IL} = 34.5 kHz (MAX.))
0	0	0	$2^7/f_{IL}$ (3.71 ms)
0	0	1	$2^8/f_{IL}$ (7.42 ms)
0	1	0	$2^9/f_{IL}$ (14.84 ms)
0	1	1	$2^{10}/f_{IL}$ (29.68 ms)
1	0	0	$2^{12}/f_{IL}$ (118.72 ms)
1	0	1	$2^{14}/f_{IL}$ (474.90 ms)
1	1	0	$2^{15}/f_{IL}$ (949.80 ms)
1	1	1	$2^{17}/f_{IL}$ (3799.19m s)

Figure 25-1. Format of User Option Byte (000C0H/010C0H) (2/2)

Address: 000C0H/010C0H[Note 1]

7	6	5	4	3	2	1	0
WDTINIT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON

WDSTBYON	Operation control of watchdog timer counter (HALT/STOP mode)
0	Counter operation stopped in HALT/STOP mode[Note 2]
1	Counter operation enabled in HALT/STOP mode

Notes 1. Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.

2. The window open period is 100% when WDSTBYON = 0, regardless the value of the WINDOW1 and WINDOW0 bits.

Caution The watchdog timer continues its operation during self-programming of the flash memory and EEPROM emulation. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

Remark f_{IL}: Internal low-speed oscillation clock frequency

Figure 25-2. Format of User Option Byte (000C1H/010C1H)

Address: 000C1H/010C1H[Note 1]

7	6	5	4	3	2	1	0
1	1	1	1	1	FRQSEL2	FRQSEL1	LVIOFF

FRQSEL2	FRQSEL1	Internal high-speed oscillator frequency
0	1	8 MHz/20 MHz [Note 2]
1	0	1 MHz [Note 3]
Other than the above		Setting prohibited

LVIOFF	Setting of LVI on power application
0	LVI is ON by default (LVI default start function enabled) upon reset release (upon power application)
1	LVI is OFF by default (LVI default start function stopped) upon reset release (upon power application)

Notes 1. Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

2. When 8 MHz or 20 MHz has been selected, the 8 MHz internal high-speed oscillator automatically starts oscillating after reset release. To use the 20 MHz internal high-speed oscillator to operate the microcontroller, oscillation is started by setting bit 0 (DSCON) of the 20 MHz internal high-speed oscillation control register (DSCCTL) to 1 with $V_{DD} \geq 2.7$ V. The circuit cannot be changed to a 1 MHz internal high-speed oscillator while the microcontroller operates.

3. When 1 MHz has been selected, the microcontroller operates on the 1 MHz internal high-speed oscillator after reset release. The circuit cannot be changed to an 8 MHz or 20 MHz internal high-speed oscillator while the microcontroller operates.

(**Cautions** are listed on the next page.)

Cautions 1. Be sure to set bits 7 to 3 to "1".

2. Even when the LVI default start function is used, if it is set to LVI operation prohibition by the software (bit 7 (LVION) of the low-voltage detection register (LVIM) is set to 0), it operates as follows:

- **Does not perform low-voltage detection during LVION = 0.**
- **If a reset is generated while LVION = 0, the LVION bit will be re-set to 1 when the CPU starts after reset release. There is a period when low-voltage detection cannot be performed normally, however, when a reset occurs due to WDT and illegal instruction execution.**
  This is due to the fact that while the pulse width detected by LVI must be 200 μs max., LVION = 1 is set upon reset occurrence, and the CPU starts operating without waiting for the LVI stabilization time.

Figure 25-3. Format of Option Byte (000C2H/010C2H)

Address: 000C2H/010C2H[Note]

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1

Note Be sure to set FFH to 000C2H, as these addresses are reserved areas. Also set FFH to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

25.3 Format of On-chip Debug Option Byte

The format of on-chip debug option byte is shown below.

Figure 25-4. Format of On-chip Debug Option Byte (000C3H/010C3H)

Address: 000C3H/010C3H[Note]

7	6	5	4	3	2	1	0
OCDENSET	0	0	0	0	1	0	OCDERSD

OCDENSET	OCDERSD	Control of on-chip debug operation
0	0	Disables on-chip debug operation.
0	1	Setting prohibited
1	0	Enables on-chip debugging. Erases data of flash memory in case of failures in authenticating on-chip debug security ID.
1	1	Enables on-chip debugging. Does not erases data of flash memory in case of failures in authenticating on-chip debug security ID.

Note Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

Caution Bits 7 and 0 (OCDENSET and OCDERSD) can only be specified a value.
Be sure to set 000010B to bits 6 to 1.

Remark The value on bits 3 to 1 will be written over when the on-chip debug function is in use and thus it will become unstable after the setting.
However, be sure to set the default values (0, 1, and 0) to bits 3 to 1 at setting.

25.4 Setting of Option Byte

The user option byte and on-chip debug option byte can be set using the RA78K0R or PM+ linker option, in addition to describing to the source. When doing so, the contents set by using the linker option take precedence, even if descriptions exist in the source, as mentioned below.

See the RA78K0R Assembler Package User's Manual for how to set the linker option.

A software description example of the option byte setting is shown below.

```
OPT   CSEG        OPT_BYTE
      DB          36H     ; Does not use interval interrupt of watchdog timer,
                          ; Enables watchdog timer operation,
                          ; Window open period of watchdog timer is 50%,
                          ; Overflow time of watchdog timer is 2^10/fIL,
                          ; Stops watchdog timer operation during HALT/STOP mode
      DB          0FBH    ; Select 8 MHz or 20 MHz for internal high-speed oscillator
                          ; Stops LVI default start function
      DB          0FFH    ; Reserved area
      DB          85H     ; Enables on-chip debug operation, does not erase flash memory
                          ; data when security ID authorization fails
```

When the boot swap function is used during self programming, 000C0H to 000C3H is switched to 010C0H to 010C3H. Describe to 010C0H to 010C3H, therefore, the same values as 000C0H to 000C3H as follows.

```
OPT2  CSEG   AT   010C0H
      DB          36H     ; Does not use interval interrupt of watchdog timer,
                          ; Enables watchdog timer operation,
                          ; Window open period of watchdog timer is 50%,
                          ; Overflow time of watchdog timer is 2^10/fIL,
                          ; Stops watchdog timer operation during HALT/STOP mode
      DB          0FBH    ; Select 8 MHz or 20 MHz for internal high-speed oscillator
                          ; Stops LVI default start function
      DB          0FFH    ; Reserved area
      DB          85H     ; Enables on-chip debug operation, does not erase flash memory
                          ; data when security ID authorization fails
```

Caution To specify the option byte by using assembly language, use OPT_BYTE as the relocation attribute name of the CSEG pseudo instruction. To specify the option byte to 010C0H to 010C3H in order to use the boot swap function, use the relocation attribute AT to specify an absolute address.

CHAPTER 26 FLASH MEMORY

The 78K0R/Kx3-L incorporates the flash memory to which a program can be written, erased, and overwritten while mounted on the board.

26.1 Writing with Flash Memory Programmer

The following dedicated flash memory programmer can be used to write data to the internal flash memory of the 78K0R/Kx3-L.

- PG-FP5, FL-PR5
- QB-MINI2

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the 78K0R/Kx3-L has been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the 78K0R/Kx3-L is mounted on the target system.

Remark FL-PR5 and FA series are products of Naito Densei Machida Mfg. Co., Ltd.

Table 26-1. Wiring Between 78K0R/Kx3-L and Dedicated Flash Memory Programmer

Pin Configuration of Dedicated Flash Memory Programmer			Pin Name	Pin No.									
				KC3-L 40-pin	KC3-L 44-pin	KC3-L 48-pin	KD3-L	KE3-L		KF3-L	KG3-L		
Signal Name	I/O	Pin Function		WQFN (6x6) Note 1	LQFP (10x10)	TQFP (7x7), WQFN (7x7) Note 1	LQFP (10x10)	LQFP (12x12), LQFP (10x10), TQFP (7x7)	FBGA (5x5), FBGA (4x4)	LQFP (12x12), LQFP (14x14)	LQFP (14x20)	LQFP (14x14)	FBGA (6x6) Note 4
SI/RxD Notes 2, 3	Input	Receive signal	TOOL0/ P40	3	2	39	4	5	D6	9	89	12	D8
SO/TxD Note 3	Output	Transmit signal											
SCK	Output	Transfer clock	–	–	–	–	–	–	–	–	–	–	–
CLK	Output	Clock output	–	–	–	–	–	–	–	–	–	–	–
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	4	3	40	5	6	E7	10	90	13	G9
FLMD0	Output	Mode signal	FLMD0	5	6	43	8	9	E8	13	93	16	F9
V_{DD}	I/O	V_{DD} voltage generation/ power monitoring	V_{DD}	10	11	48	13	15	B7	19	99	22	C9
			EV_{DD}	–	–	–	–	16	A8	–	–	–	–
			EV_{DD0}	–	–	–	–	–	–	20	100	23	C10
			EV_{DD1}	–	–	–	–	–	–	–	30	53	C1
			AV_{REF}	29	32	23	38	47	G1	59	50	73	H1
GND	–	Ground	V_{SS}	9	10	47	12	13	C7	17	97	20	F10
			EV_{SS}	–	–	–	–	14	B8	–	–	–	–
			EV_{SS0}	–	–	–	–	–	–	18	98	21	D9
			EV_{SS1}	–	–	–	–	–	–	–	20	43	A3
			AV_{SS}	30	33	24	39	48	H1	60	51	74	H2

Notes 1. Under development

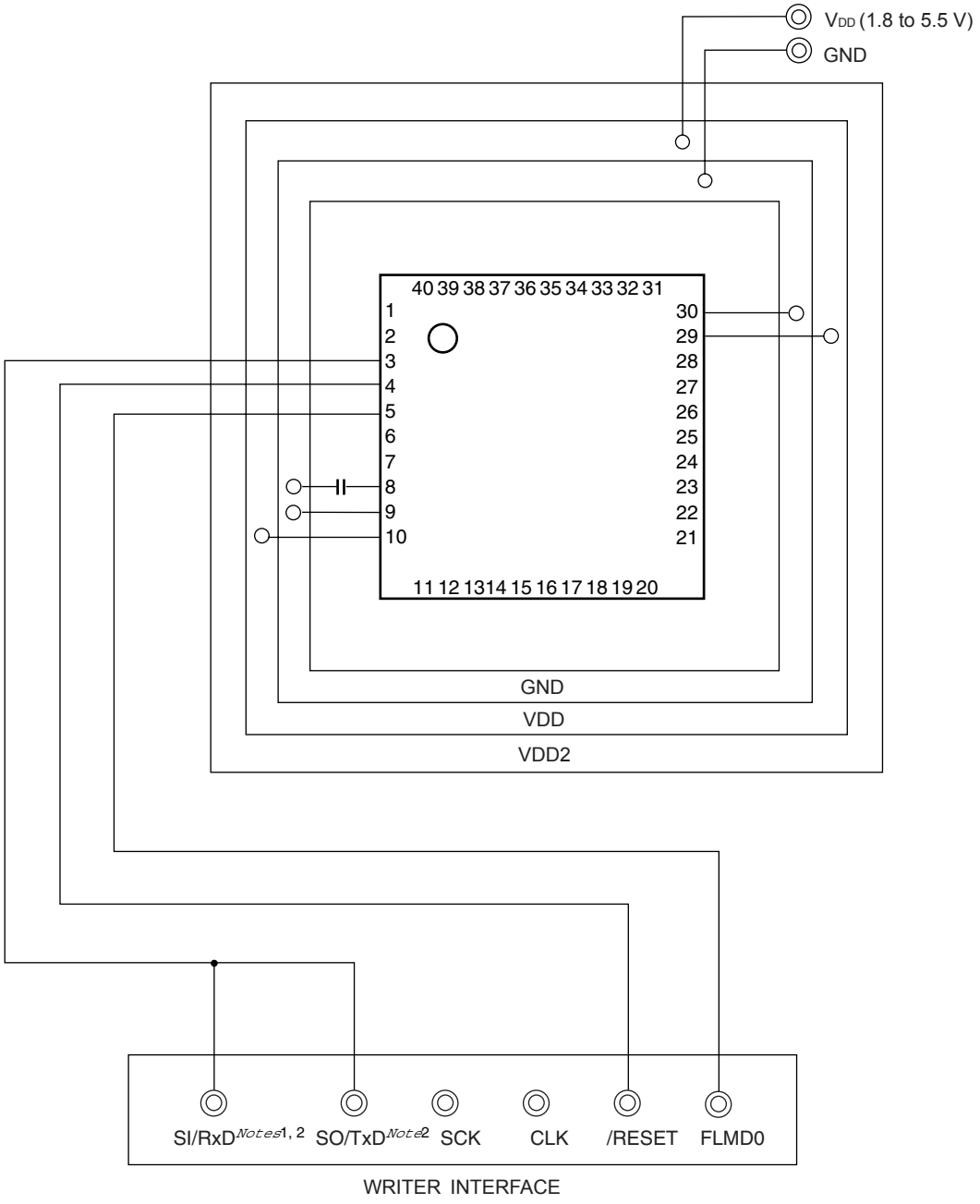
2. This pin is not required to be connected when using PG-FP5 or FL-PR5.

3. Connect SI/RxD or SO/TxD when using QB-MINI2.

4. μPD78F1013 and μPD78F1014 only

Examples of the recommended connection when using the adapter for flash memory writing are shown below.

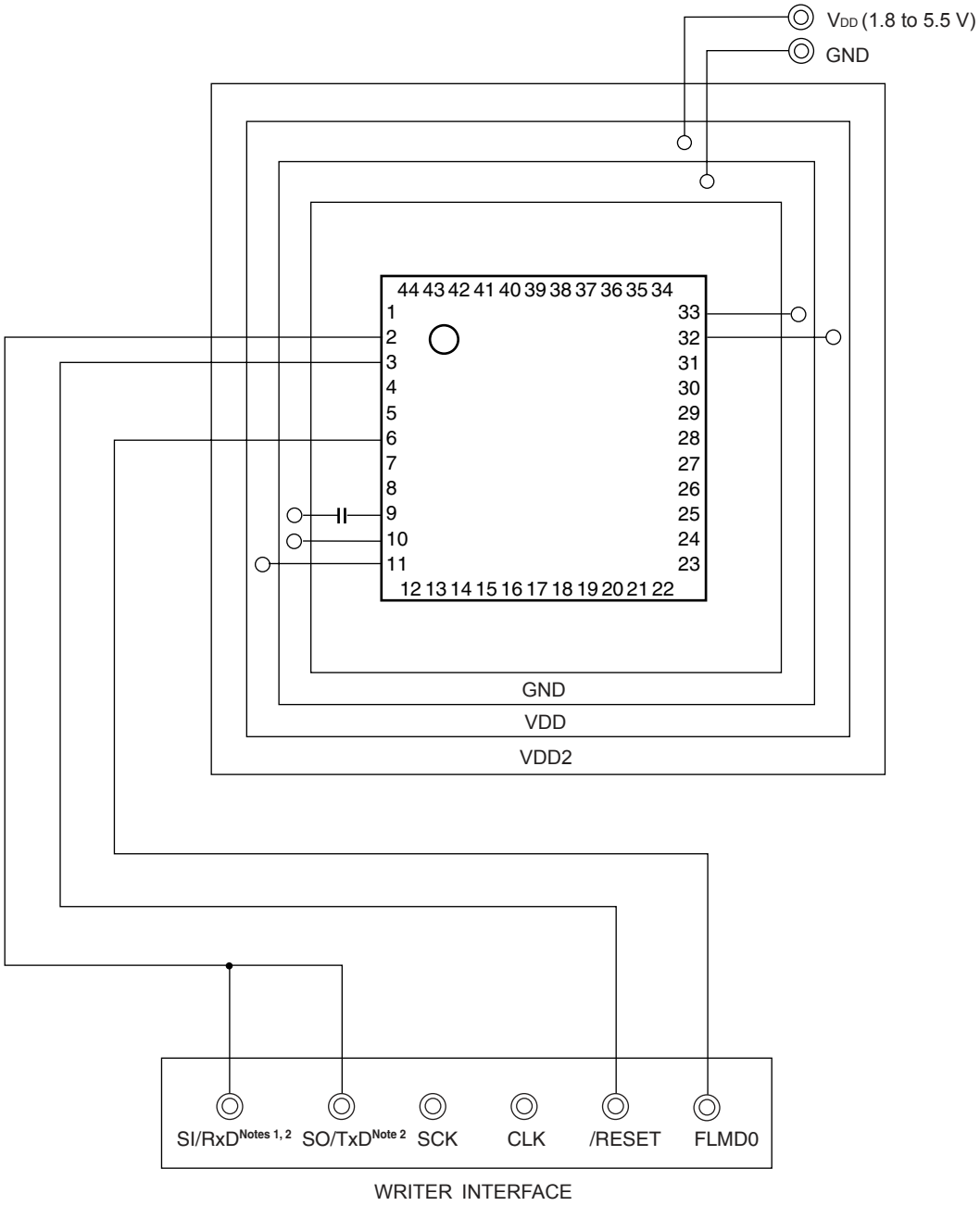
Figure 26-1. Example of Wiring Adapter for Flash Memory Writing (40-pin product of 78K0R/KC3-L)



Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

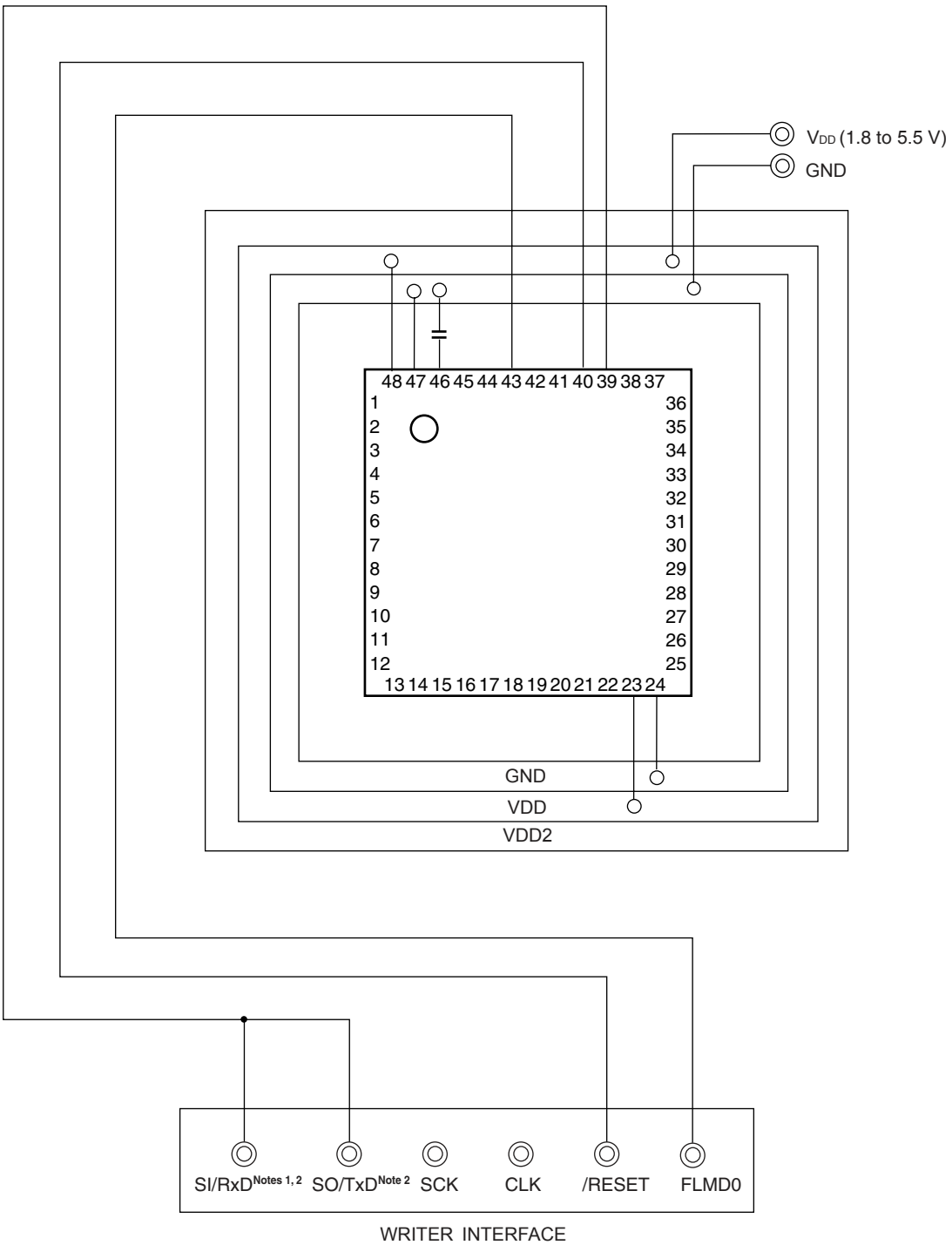
Figure 26-2. Example of Wiring Adapter for Flash Memory Writing (44-pin products of 78K0R/KC3-L)



Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

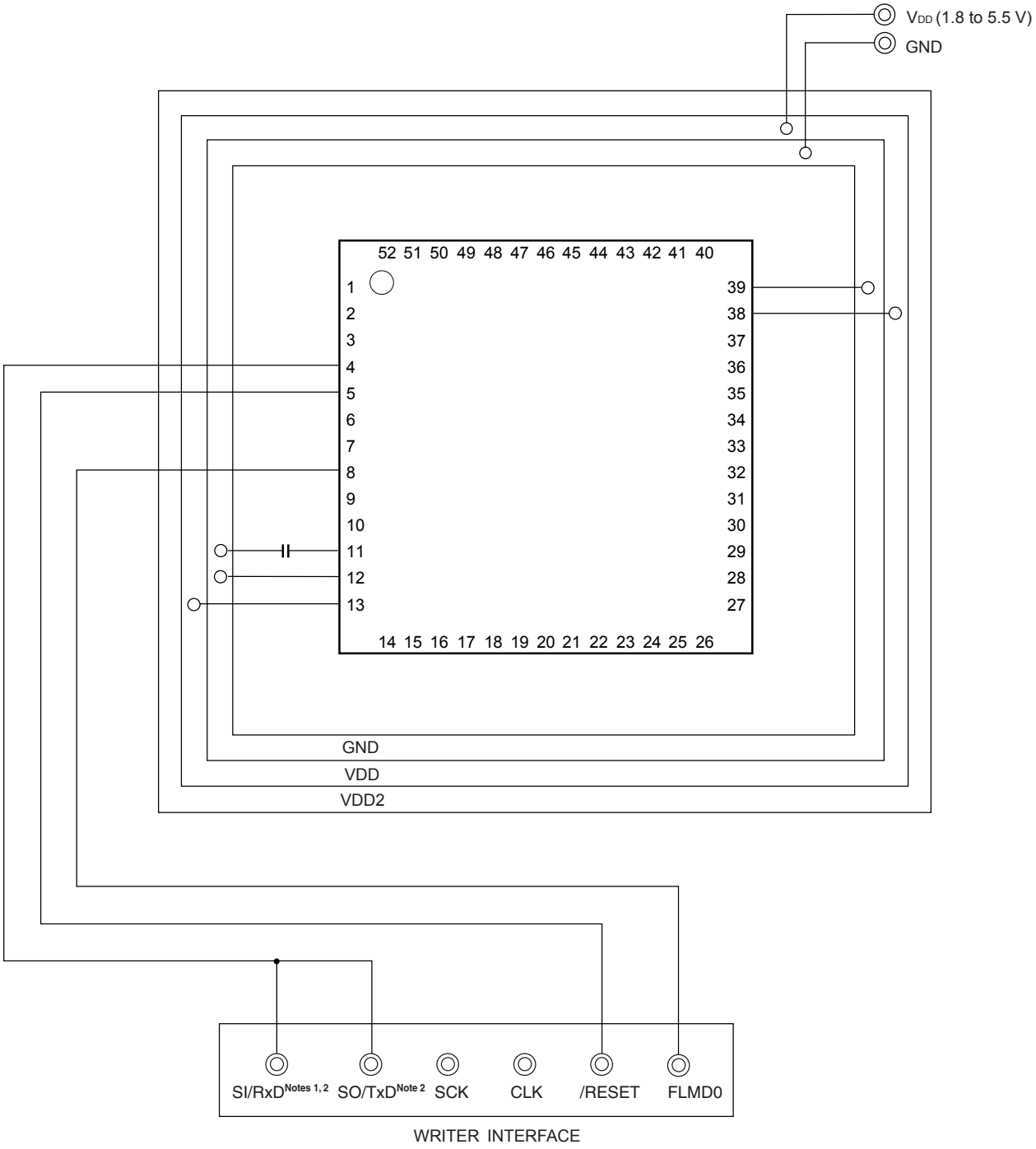
Figure 26-3. Example of Wiring Adapter for Flash Memory Writing (48-pin products of 78K0R/KC3-L)



Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

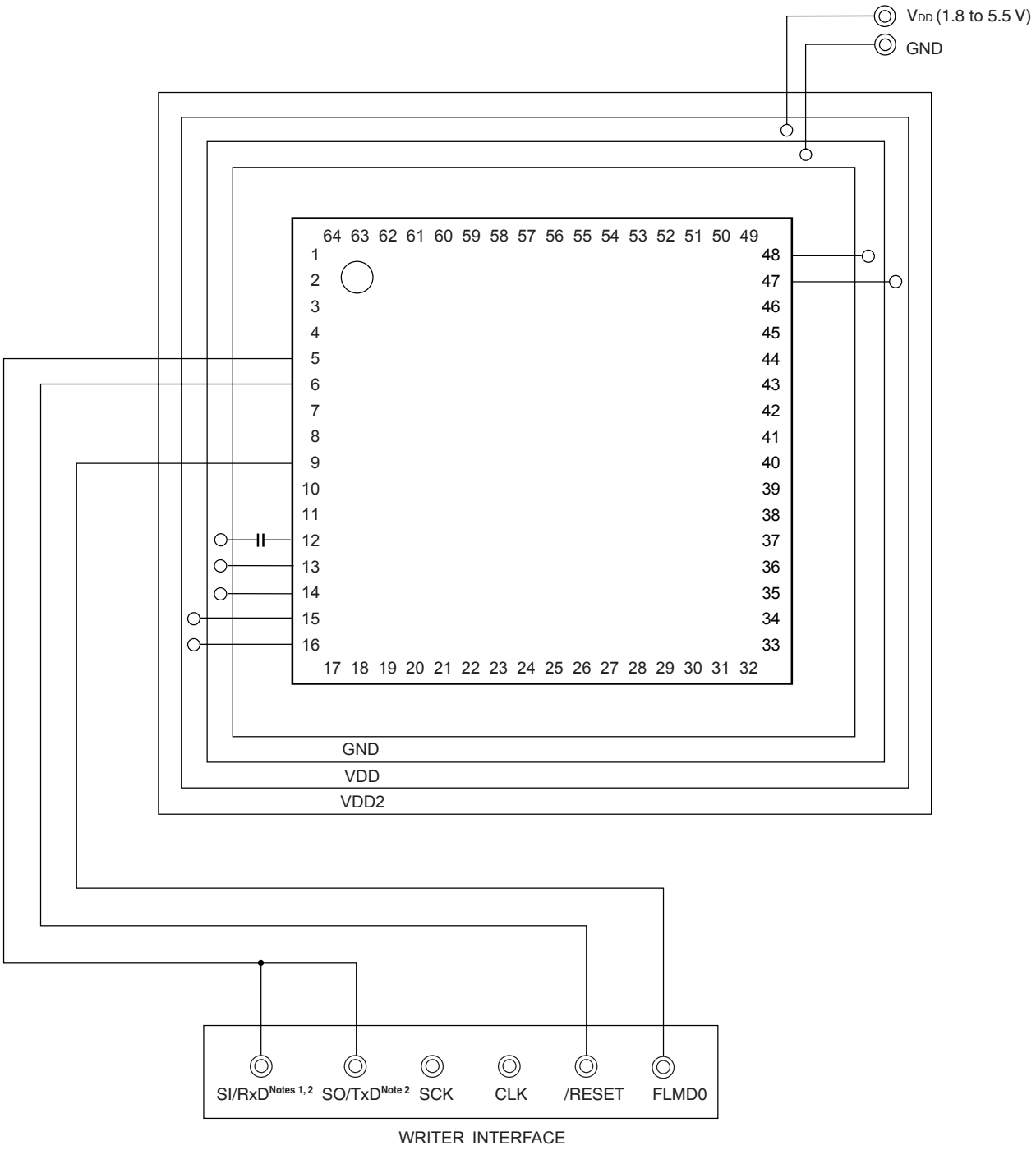
Figure 26-4. Example of Wiring Adapter for Flash Memory Writing (78K0R/KD3-L)



Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

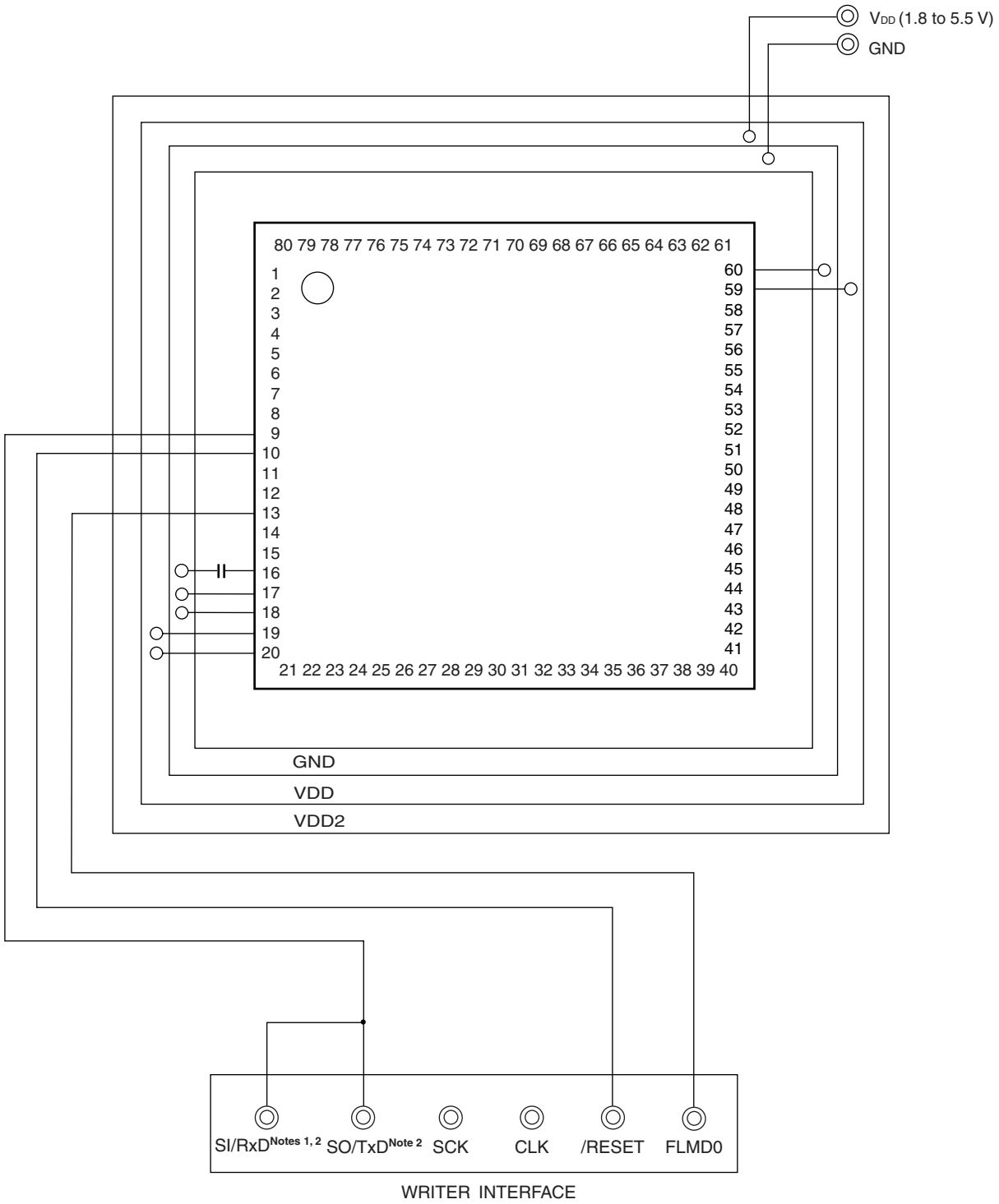
Figure 26-5. Example of Wiring Adapter for Flash Memory Writing (78K0R/KE3-L)



Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

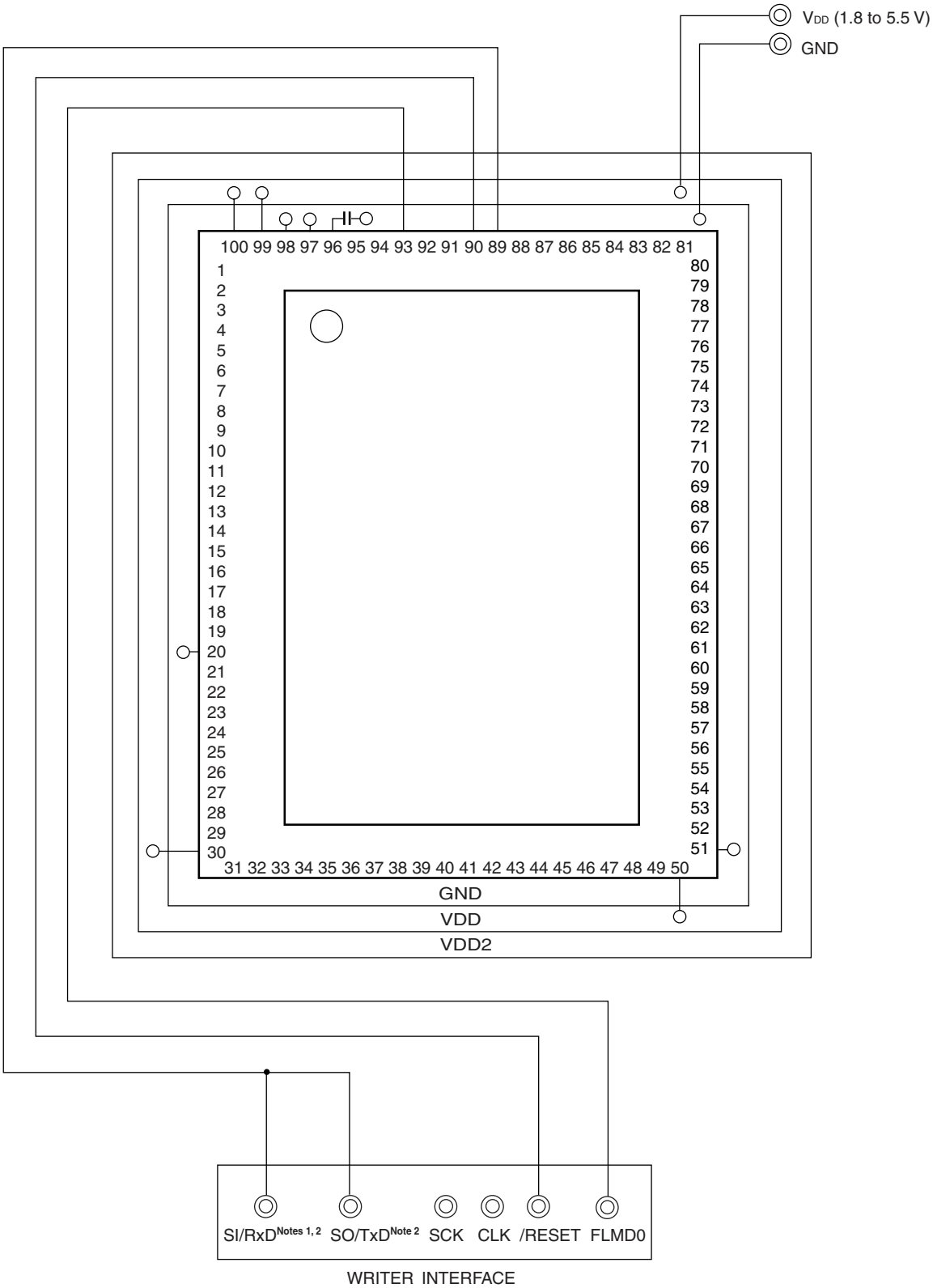
Figure 26-6. Example of Wiring Adapter for Flash Memory Writing (78K0R/KF3-L)



Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

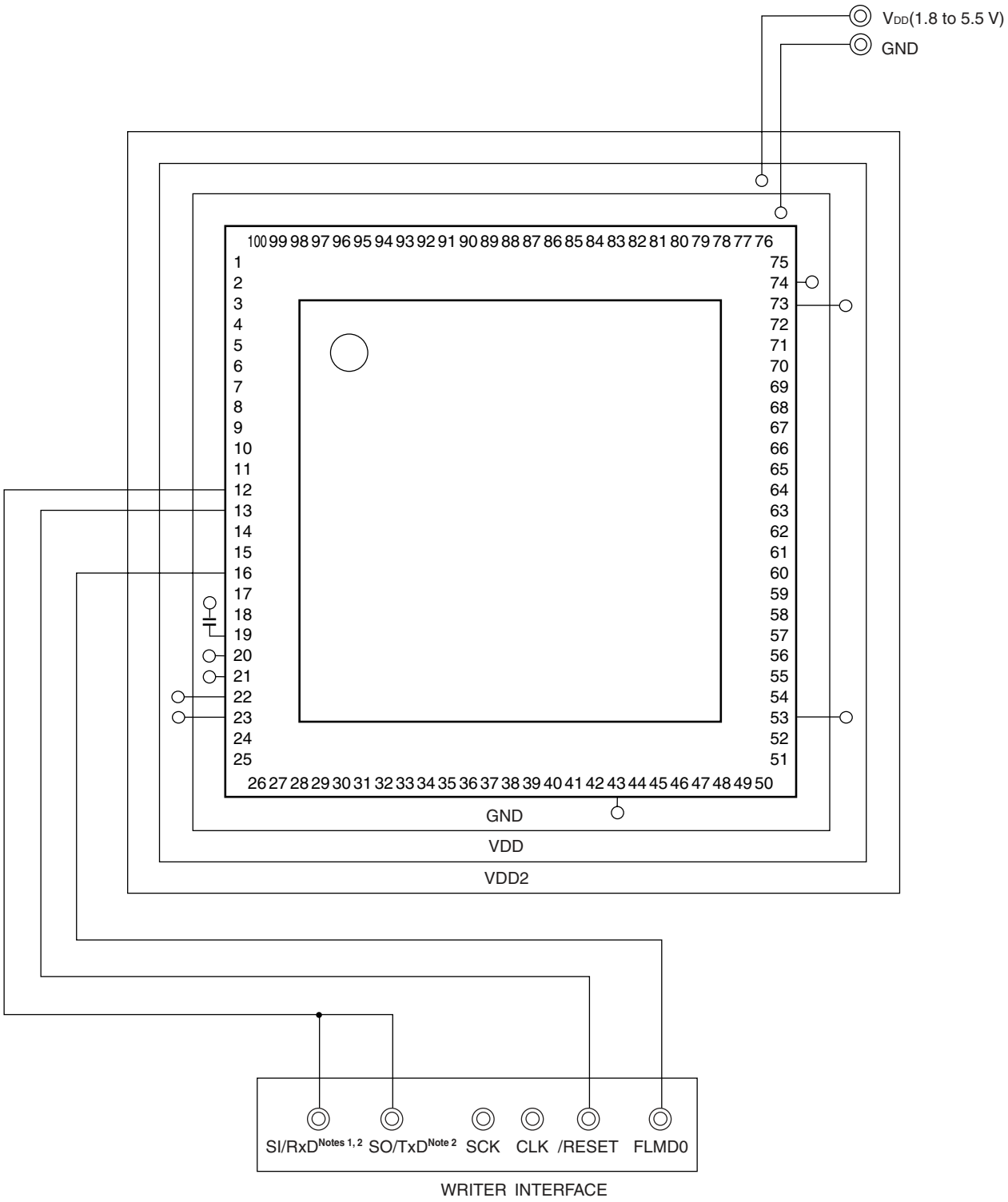
Figure 26-7. Example of Wiring Adapter for Flash Memory Writing (78K0R/KG3-L, LQFP (14x20))



Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

Figure 26-8. Example of Wiring Adapter for Flash Memory Writing (78K0R/KG3-L, LQFP (14x14))



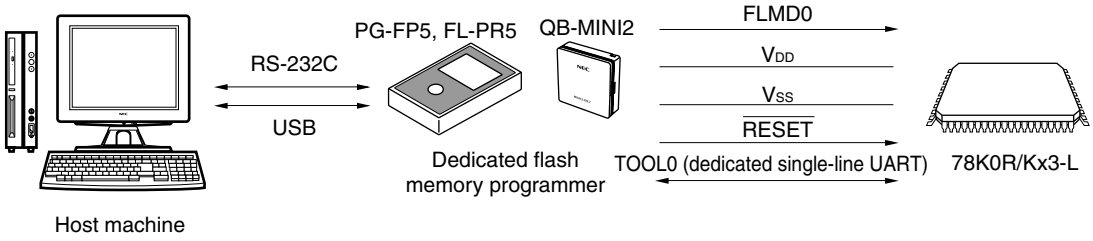
Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

26.2 Programming Environment

The environment required for writing a program to the flash memory of the 78K0R/Kx3-L is illustrated below.

Figure 26-9. Environment for Writing Program to Flash Memory



A host machine that controls the dedicated flash memory programmer is necessary.

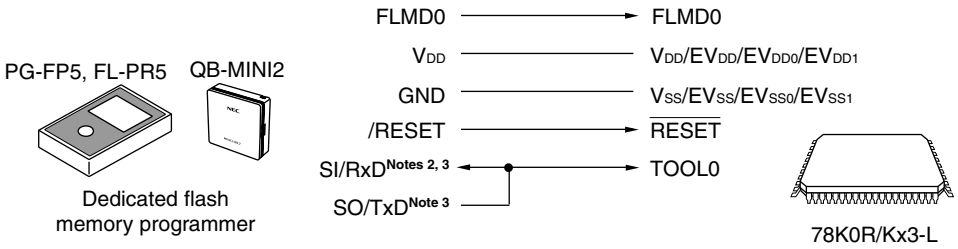
To interface between the dedicated flash memory programmer and the 78K0R/Kx3-L, the TOOL0 pin is used for manipulation such as writing and erasing via a dedicated single-line UART. To write the flash memory off-board, a dedicated program adapter (FA series) is necessary.

26.3 Communication Mode

Communication between the dedicated flash memory programmer and the 78K0R/Kx3-L is established by serial communication using the TOOL0 pin via a dedicated single-line UART of the 78K0R/Kx3-L.

Transfer rate: 115,200 bps, 250,000 bps, 500,000 bps, 1 Mbps[Note 1]

Figure 26-10. Communication with Dedicated Flash Memory Programmer



Notes 1. When using a transfer rate of 1 Mbps, do not use the wide voltage mode.

2. This pin is not required to be connected when using PG-FP5 or FL-PR5.

3. Connect SI/RxD or SO/TxD when using QB-MINI2.

The dedicated flash memory programmer generates the following signals for the 78K0R/Kx3-L. See the manual of PG-FP5, FL-PR5, or MINICUBE2 for details.

Table 26-2. Pin Connection

Dedicated Flash Memory Programmer			78K0R/Kx3-L	Connection
Signal Name	I/O	Pin Function	Pin Name	
FLMD0	Output	Mode signal	FLMD0	◎
V_{DD}	I/O	V_{DD} voltage generation/power monitoring	V_{DD}, EV_{DD}, EV_{DD0}, EV_{DD1}, AV_{REF}	◎
GND	–	Ground	V_{SS}, EV_{SS}, EV_{SS0}, EV_{SS1}, AV_{SS}	◎
CLK	Output	Clock output	–	×
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	◎
SI/RxD Notes1, 2	Input	Receive signal	TOOL0	◎
SO/TxD Note2	Output	Transmit signal		
SCK	Output	Transfer clock	–	×

Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

Remark ◎: Be sure to connect the pin.

×: The pin does not have to be connected.

26.4 Connection of Pins on Board

To write the flash memory on-board, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be handled as described below.

26.4.1 FLMD0 pin

(1) In flash memory programming mode

Directly connect this pin to a flash memory programmer when data is written by the flash memory programmer. This supplies a writing voltage of the V_{DD} level to the FLMD0 pin.

The FLMD0 pin does not have to be pulled down externally because it is internally pulled down by reset. To pull it down externally, use a resistor of 1 kΩ to 200 kΩ.

(2) In normal operation mode

It is recommended to leave this pin open during normal operation.

The FLMD0 pin must always be kept at the V_{SS} level before reset release but does not have to be pulled down externally because it is internally pulled down by reset. However, pulling it down must be kept selected (i.e., FLMDPUP = “0”, default value) by using bit 7 (FLMDPUP) of the background event control register (BECTL) (see **26.5 (1) Back ground event control register**). To pull it down externally, use a resistor of 200 kΩ or smaller.

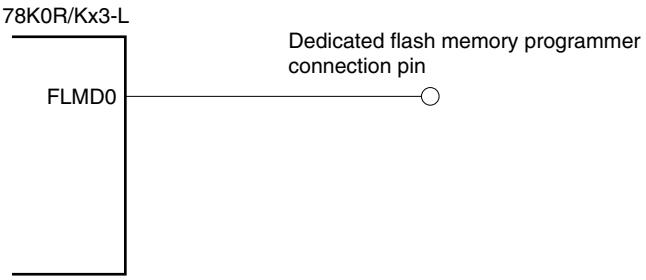
Self programming and the rewriting of flash memory with the programmer can be prohibited using hardware, by directly connecting this pin to the V_{SS} pin.

(3) In self programming mode

It is recommended to leave this pin open when using the self programming function. To pull it down externally, use a resistor of 100 kΩ to 200 kΩ.

In the self programming mode, the setting is switched to pull up in the self programming library.

Figure 26-11. FLMD0 Pin Connection Example



26.4.2 TOOL0 pin

In the flash memory programming mode, connect this pin directly to the dedicated flash memory programmer or pull it up by connecting it to EV_{DD} via an external resistor.

When on-chip debugging is enabled in the normal operation mode, pull this pin up by connecting it to EV_{DD} via an external resistor, and be sure to keep inputting the V_{DD} level to the TOOL0 pin before reset is released (pulling down this pin is prohibited).

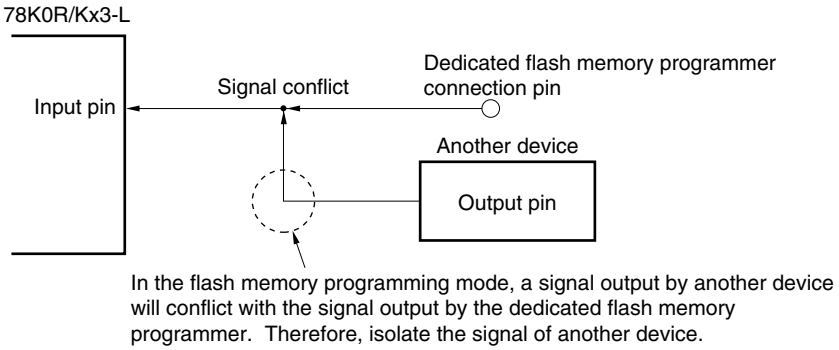
Remark The SAU and IICA pins are not used for communication between the 78K0R/Kx3-L and dedicated flash memory programmer, because single-line UART is used.

26.4.3 $\overline{\text{RESET}}$ pin

Signal conflict will occur if the reset signal of the dedicated flash memory programmer is connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board. To prevent this conflict, isolate the connection with the reset signal generator.

The flash memory will not be correctly programmed if the reset signal is input from the user system while the flash memory programming mode is set . Do not input any signal other than the reset signal of the dedicated flash memory programmer.

Figure 26-12. Signal Conflict ($\overline{\text{RESET}}$ Pin)



26.4.4 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to EV_{DD} (EV_{DD0}/EV_{DD1}) Note or EV_{SS} (EV_{SS0}/EV_{SS1}) Note via a resistor.

Note With products without an EV_{SS} (EV_{SS0}/EV_{SS1}) pin, connect them to V_{SS}. With products without an EV_{DD} (EV_{DD0}/EV_{DD1}) pin, connect them to V_{DD}.

26.4.5 REGC pin

Connect the REGC pin to GND via a capacitor (0.47 to 1 μF) in the same manner as during normal operation. Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

26.4.6 X1 and X2 pins

Connect X1 and X2 in the same status as in the normal operation mode.

Remark In the flash memory programming mode, the internal high-speed oscillation clock (f_{IH}) is used.

26.4.7 Power supply

To use the supply voltage output of the flash memory programmer, connect the V_{DD} pin to V_{DD} of the flash memory programmer, and the V_{SS} pin to GND of the flash memory programmer.

To use the on-board supply voltage, connect in compliance with the normal operation mode.

However, when using the on-board supply voltage, be sure to connect the V_{DD} and V_{SS} pins to V_{DD} and GND of the flash memory programmer to use the power monitor function with the flash memory programmer.

Supply the same other power supplies (EV_{DD}, EV_{DD0}, EV_{DD1}, EV_{SS}, EV_{SS0}, EV_{SS1}, AV_{REF}, and AV_{SS}) as those in the normal operation mode.

26.5 Registers Controlling Flash Memory

(1) Background event control register (BECTL)

Even if the FLMD0 pin is not controlled externally, it can be controlled by software with the BECTL register to set the self-programming mode.

However, depending on the processing of the FLMD0 pin, it may not be possible to set the self-programming mode by software. When using the BECTL register, leaving the FLMD0 pin open is recommended. When pulling it down externally, use a resistor with a resistance of 100 kΩ or more. In addition, in the normal operation mode, use the BECTL register with the pull down selection. In the self-programming mode, the setting is switched to pull up in the self- programming library.

The BECTL register is set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets this register to 00H.

Figure 26-13. Format of Background Event Control Register (BECTL)

Address: FFFBEH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BECTL	FLMDPUP	0	0	0	0	0	0	0

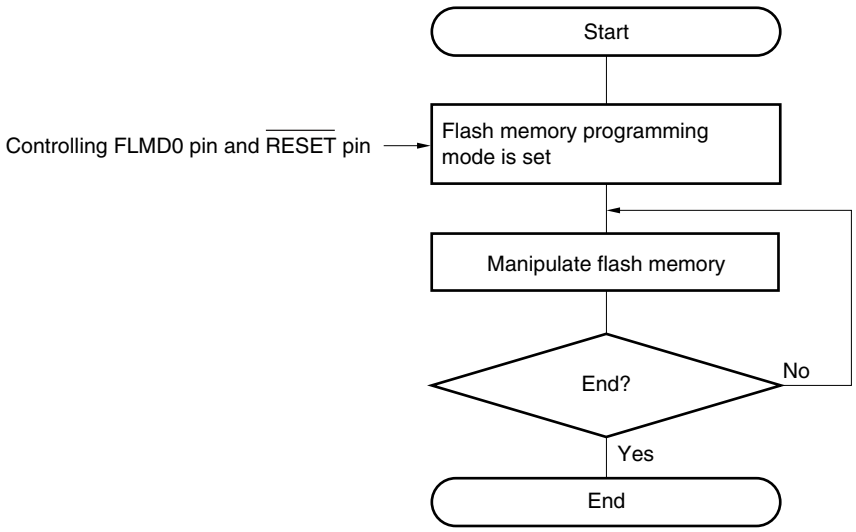
FLMDPUP	Software control of FLMD0 pin
0	Selects pull-down
1	Selects pull-up

26.6 Programming Method

26.6.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

Figure 26-14. Flash Memory Manipulation Procedure



26.6.2 Flash memory programming mode

To rewrite the contents of the flash memory by using the dedicated flash memory programmer, set the 78K0R/Kx3-L in the flash memory programming mode. To set the mode, set the FLMD0 pin and TOOL0 pin to V_{DD} and clear the reset signal.

Change the mode by using a jumper when writing the flash memory on-board.

Figure 26-15. Flash Memory Programming Mode

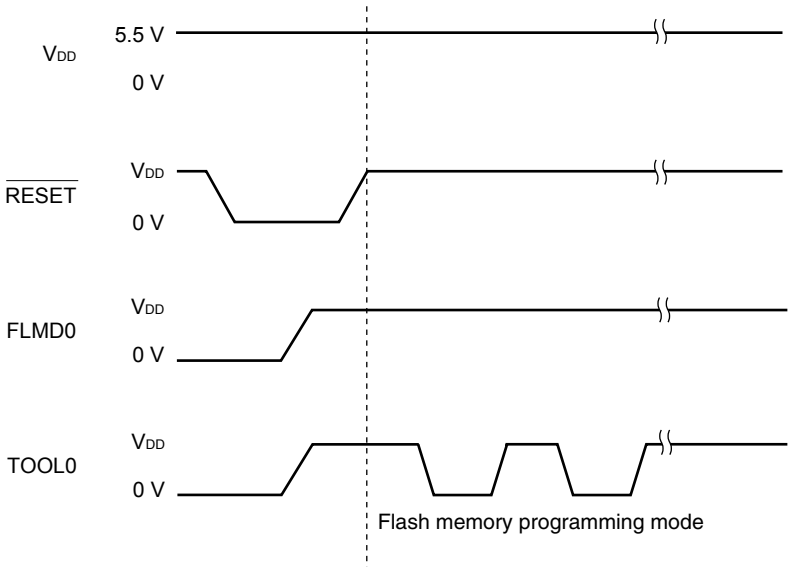


Table 26-3. Relationship Between FLMD0 Pin and Operation Mode After Reset Release

FLMD0	Operation Mode
0	Normal operation mode
V_{DD}	Flash memory programming mode

There are two flash memory programming modes for which the voltage range in which to write, erase, or verify data differs.

Table 26-4. Programming Modes and Voltages at Which Data Can Be Written, Erased, or Verified

Mode	Voltages at which data can be written, erased, or verified	Writing Clock Frequency
Wide voltage mode	1.8 V to 5.5 V	4 MHz (MAX.)
Full speed mode	2.7 V to 5.5 V	20 MHz (MAX.)

Specify the mode that corresponds to the voltage range in which to write data. Specify wide-voltage mode or full-speed mode on the GUI of the dedicated flash memory programmer.

Caution If data was erased in wide-voltage mode, data can be written or verified only in wide-voltage mode. However, such data can be written or verified in full-speed mode after re-erasing the data in full-speed mode.

Remark For details about communication commands, see **26.6.4 Communication commands**.

26.6.3 Selecting communication mode

Communication mode of the 78K0R/Kx3-L as follows.

Table 26-5. Communication Modes

Communication Mode	Standard Setting[Note 1]				Pins Used
	Port	Speed [Note 2]	Frequency	Multiply Rate	
1-line mode (dedicated single-line UART)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps [Note 3]	–	–	TOOL0

Notes 1. Selection items for Standard settings on GUI of the flash memory programmer.

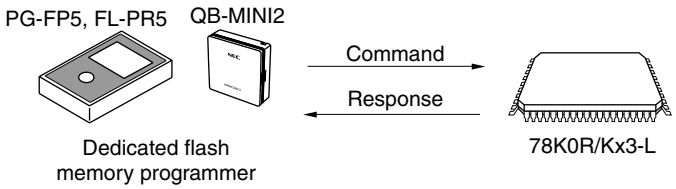
2. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

3. When using a transfer rate of 1 Mbps, do not use the wide voltage mode.

26.6.4 Communication commands

The 78K0R/Kx3-L communicates with the dedicated flash memory programmer by using commands. The signals sent from the flash memory programmer to the 78K0R/Kx3-L are called commands, and the signals sent from the 78K0R/Kx3-L to the dedicated flash memory programmer are called response.

Figure 26-16. Communication Commands



The flash memory control commands of the 78K0R/Kx3-L are listed in the table below. All these commands are issued from the programmer and the 78K0R/Kx3-L perform processing corresponding to the respective commands.

Table 26-6. Flash Memory Control Commands

Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Chip Erase	Erases the entire flash memory.
	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased.
Write	Programming	Writes data to a specified area in the flash memory.
Getting information	Silicon Signature	Gets the 78K0R/Kx3-L information (such as the part number and flash memory configuration).
	Version Get	Gets the 78K0R/Kx3-L firmware version.
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
Others	Reset	Used to detect synchronization status of communication.
	Baud Rate Set	Sets baud rate when UART communication mode is selected.

The 78K0R/Kx3-L returns a response for the command issued by the dedicated flash memory programmer. The response names sent from the 78K0R/Kx3-L are listed below.

Table 26-7. Response Names

Response Name	Function
ACK	Acknowledges command/data.
NAK	Acknowledges illegal command/data.

26.7 Security Settings

The 78K0R/Kx3-L supports a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.

The operations shown below can be performed using the Security Set command. The security setting is valid when the programming mode is set next.

- Disabling batch erase (chip erase)
  Execution of the block erase and batch erase (chip erase) commands for entire blocks in the flash memory is prohibited by this setting during on-board/off-board programming. Once execution of the batch erase (chip erase) command is prohibited, all of the prohibition settings (including prohibition of batch erase (chip erase)) can no longer be cancelled.

  Caution After the security setting for the batch erase is set, erasure cannot be performed for the device. In addition, even if a write command is executed, data different from that which has already been written to the flash memory cannot be written, because the erase command is disabled.

- Disabling block erase
  Execution of the block erase command for a specific block in the flash memory is prohibited during on-board/off-board programming. However, blocks can be erased by means of self programming.

- Disabling write
  Execution of the write and block erase commands for entire blocks in the flash memory is prohibited during on-board/off-board programming. However, blocks can be written by means of self programming.

- Disabling rewriting boot cluster 0
  Execution of the batch erase (chip erase) command, block erase command, and write command on boot cluster 0 (00000H to 00FFFH) in the flash memory is prohibited by this setting.

The batch erase (chip erase), block erase, write commands, and rewriting boot cluster 0 are enabled by the default setting when the flash memory is shipped. Security can be set by on-board/off-board programming and self programming. Each security setting can be used in combination.

All the security settings are cleared by executing the batch erase (chip erase) command.

Table 26-8 shows the relationship between the erase and write commands when the 78K0R/Kx3-L security function is enabled.

Remark To prohibit writing and erasing during self-programming, use the flash sealed window function (see **26.9.2** for detail).

Table 26-8. Relationship Between Enabling Security Function and Command

(1) During on-board/off-board programming

Valid Security	Executed Command		
	Batch Erase (Chip Erase)	Block Erase	Write
Prohibition of batch erase (chip erase)	Cannot be erased in batch	Blocks cannot be erased.	Can be performed[Note].
Prohibition of block erase	Can be erased in batch.		Can be performed.
Prohibition of writing			Cannot be performed.
Prohibition of rewriting boot cluster 0	Cannot be erased in batch	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Note Confirm that no data has been written to the write area. Because data cannot be erased after batch erase (chip erase) is prohibited, do not write data if the data has not been erased.

(2) During self programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of batch erase (chip erase)	Blocks can be erased.	Can be performed.
Prohibition of block erase		
Prohibition of writing		
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Remark To prohibit writing and erasing during self-programming, use the flash sealed window function (see **26.9.2** for detail).

Table 26-9. Setting Security in Each Programming Mode

(1) On-board/off-board programming

Security	Security Setting	How to Disable Security Setting
Prohibition of batch erase (chip erase)	Set via GUI of dedicated flash memory programmer, etc.	Cannot be disabled after set.
Prohibition of block erase		Execute batch erase (chip erase) command
Prohibition of writing		
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

(2) Self programming

Security	Security Setting	How to Disable Security Setting
Prohibition of batch erase (chip erase)	Set by using information library.	Cannot be disabled after set.
Prohibition of block erase		Execute batch erase (chip erase) command during on-board/off-board programming (cannot be disabled during self programming)
Prohibition of writing		
Prohibition of rewriting boot cluster 0		

26.8 Processing Time of Each Command When Using PG-FP5 (Reference Values)

The processing time of each command (reference values) when using PG-FP5 as the dedicated flash memory programmer is shown below.

Table 26-10. Processing Time of Each Command When Using PG-FP5 (Wide Voltage Mode) (Reference Values)

PG-FP5 Command	Port: UART								
	Speed: 500000 bps								
	16 KB	32 KB	48 KB	64 KB	64 KB	96 KB	128 KB	192 KB	256 KB
	μPD78F1000	μPD78F1001, μPD78F1004, μPD78F1007	μPD78F1002, μPD78F1005, μPD78F1008	μPD78F1003, μPD78F1006, μPD78F1009	μPD78F1010	μPD78F1011, μPD78F1013	μPD78F1012, μPD78F1014	μPD78F1027, μPD78F1029	μPD78F1028, μPD78F1030
Signature	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Blankcheck	1 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	3 s (TYP.)	4 s (TYP.)
Erase	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	3 s (TYP.)	4 s (TYP.)
Program	2.5 s (TYP.)	4 s (TYP.)	6 s (TYP.)	7 s (TYP.)	7.5 s (TYP.)	11 s (TYP.)	14 s (TYP.)	21 s (TYP.)	28 s (TYP.)
Verify	2 s (TYP.)	3 s (TYP.)	4 s (TYP.)	4.5 s (TYP.)	4.5 s (TYP.)	6.5 s (TYP.)	8.5 s (TYP.)	13 s (TYP.)	16.5 s (TYP.)
E.P.V	2.5 s (TYP.)	4.5 s (TYP.)	6.5 s (TYP.)	8 s (TYP.)	8 s (TYP.)	12 s (TYP.)	15.5 s (TYP.)	23.5 s (TYP.)	31 s (TYP.)
Checksum	1 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	3.5 s (TYP.)	4 s (TYP.)
Security	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)

Table 26-11. Processing Time of Each Command When Using PG-FP5 (Full Speed Mode) (Reference Values)

PG-FP5 Command	Port: UART								
	Speed: 1M bps								
	16 KB	32 KB	48 KB	64 KB	64 KB	96 KB	128 KB	192 KB	256 KB
	μPD78F1000	μPD78F1001, μPD78F1004, μPD78F1007	μPD78F1002, μPD78F1005, μPD78F1008	μPD78F1003, μPD78F1006, μPD78F1009	μPD78F1010	μPD78F1011, μPD78F1013	μPD78F1012, μPD78F1014	μPD78F1027, μPD78F1029	μPD78F1028, μPD78F1030
Signature	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Blankcheck	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)
Erase	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)
Program	1.5 s (TYP.)	2 s (TYP.)	3 s (TYP.)	3.5 s (TYP.)	3.5 s (TYP.)	5.5 s (TYP.)	6.5 s (TYP.)	9.5 s (TYP.)	12.5 s (TYP.)
Verify	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	3 s (TYP.)	3 s (TYP.)	4 s (TYP.)	5.5 s (TYP.)	8 s (TYP.)	10 s (TYP.)
E.P.V	1.5 s (TYP.)	2.5 s (TYP.)	3 s (TYP.)	4 s (TYP.)	4 s (TYP.)	5.5 s (TYP.)	7 s (TYP.)	10 s (TYP.)	13 s (TYP.)
Checksum	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)
Security	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)

26.9 Flash Memory Programming by Self-Programming

The 78K0R/Kx3-L supports a self-programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the 78K0R/Kx3-L self-programming library, it can be used to upgrade the program in the field.

If an interrupt occurs during self-programming, self-programming can be temporarily stopped and interrupt servicing can be executed. If an unmasked interrupt request is generated in the EI state, the request branches directly from the self-programming library to the interrupt routine. After the self-programming mode is later restored, self-programming can be resumed. However, the interrupt response time is different from that of the normal operation mode.

Cautions 1. The self-programming function cannot be used when the CPU operates with the subsystem clock.

2. In the self-programming mode, call the self-programming start library (FlashStart).

3. To prohibit an interrupt during self-programming, in the same way as in the normal operation mode, execute the self-programming library in the state where the IE flag is cleared (0) by the DI instruction. To enable an interrupt, clear (0) the interrupt mask flag to accept in the state where the IE flag is set (1) by the EI instruction, and then execute the self-programming library.

4. Disable DMA operation (DENn = 0) during the execution of self programming library functions.

Remarks 1. For details of the self-programming function and the 78K0R/Kx3-L self-programming library, refer to **78K0R Microcontroller Self Programming Library Type2 User's Manual (U19193E).**

2. For details of the time required to execute self programming, see the notes on use that accompany the flash self programming library tool.

Similar to when writing data by using the flash memory programmer, there are two flash memory programming modes for which the voltage range in which to write, erase, or verify data differs.

Table 26-12. Programming Modes and Voltages at Which Data Can Be Written, Erased, or Verified

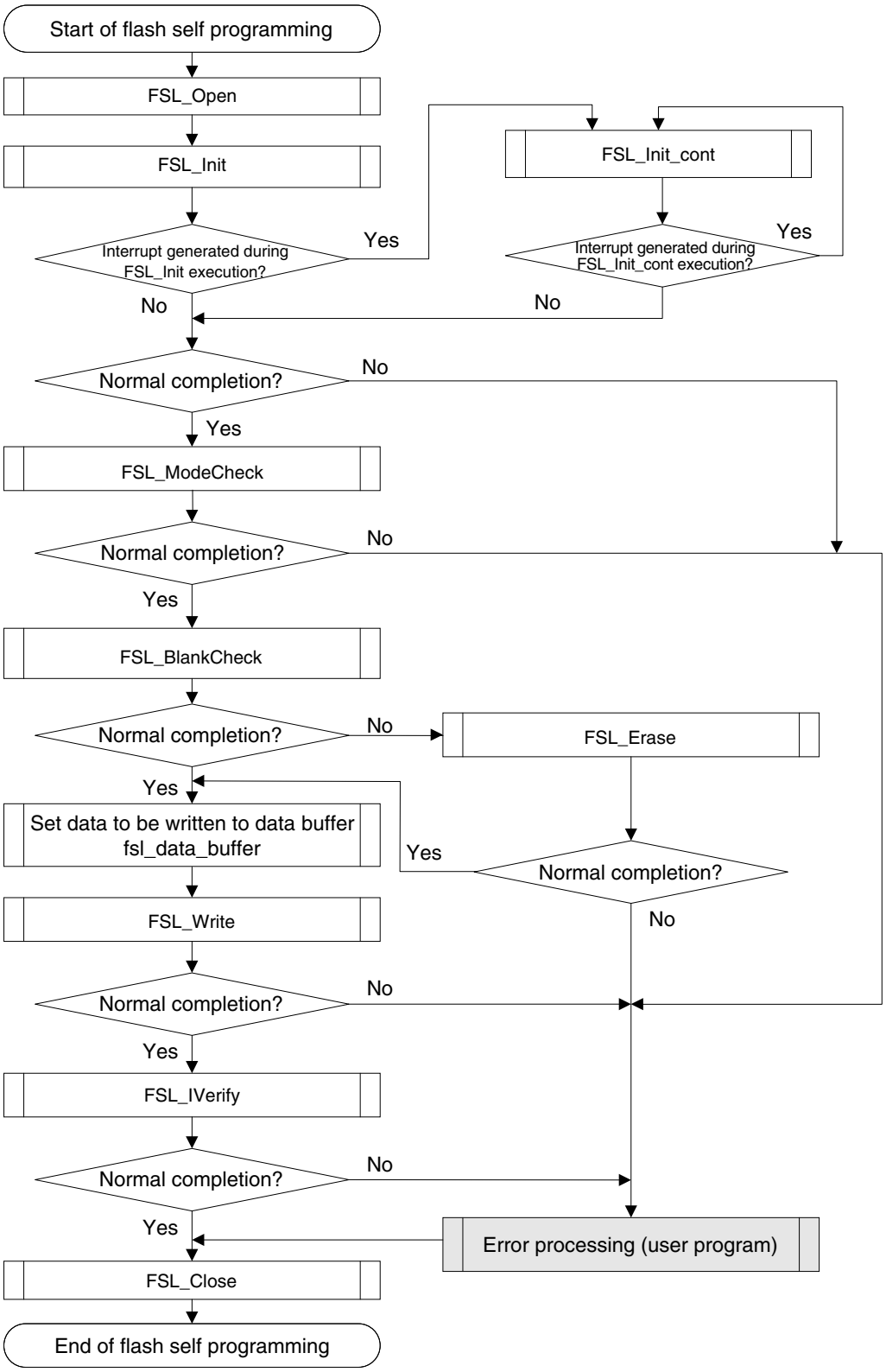
Mode	Voltages at which data can be written, erased, or verified	Writing Clock Frequency
Wide voltage mode	1.8 V to 5.5 V	4 MHz (MAX.)
Full speed mode	2.7 V to 5.5 V	20 MHz (MAX.)

Specify the mode that corresponds to the voltage range in which to write data. If the constant fsl_low_voltage_u08 is 01H when the FSL_Init function of the self programming library provided by Renesas Electronics is executed, wide-voltage mode is specified. If the constant is 00H, full-speed mode is specified.

Caution If data was erased in wide-voltage mode, data can be written or verified only in wide-voltage mode. However, such data can be written or verified in full-speed mode after re-erasing the data in full-speed mode.

The following figure illustrates a flow of rewriting the flash memory by using a self programming library.

Figure 26-17. Flow of Self Programming (Rewriting Flash Memory)



26.9.1 Boot swap function

If rewriting the boot area failed by temporary power failure or other reasons, restarting a program by resetting or overwriting is disabled due to data destruction in the boot area.

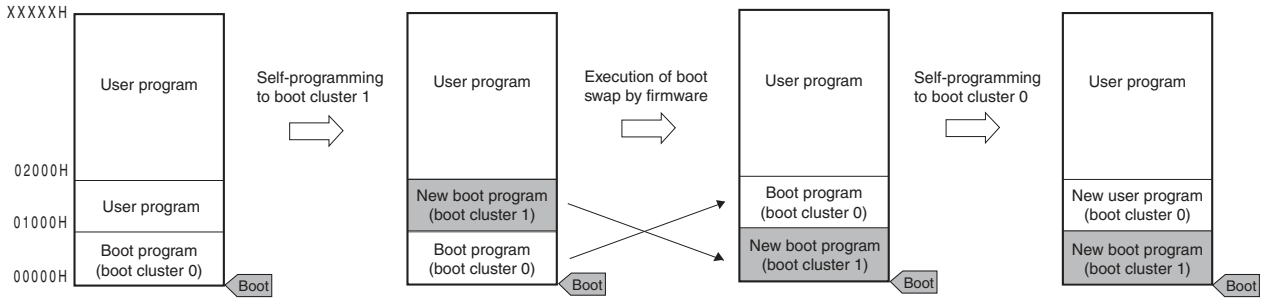
The boot swap function is used to avoid this problem.

Before erasing boot cluster 0[Note], which is a boot program area, by self-programming, write a new boot program to boot cluster 1 in advance. When the program has been correctly written to boot cluster 1, swap this boot cluster 1 and boot cluster 0 by using the set information function of the firmware of the 78K0R/Kx3-L, so that boot cluster 1 is used as a boot area. After that, erase or write the original boot program area, boot cluster 0.

As a result, even if a power failure occurs while the boot programming area is being rewritten, the program is executed correctly because it is booted from boot cluster 1 to be swapped when the program is reset and started next.

Note A boot cluster is a 4 KB area and boot clusters 0 and 1 are swapped by the boot swap function.

Figure 26-18. Boot Swap Function

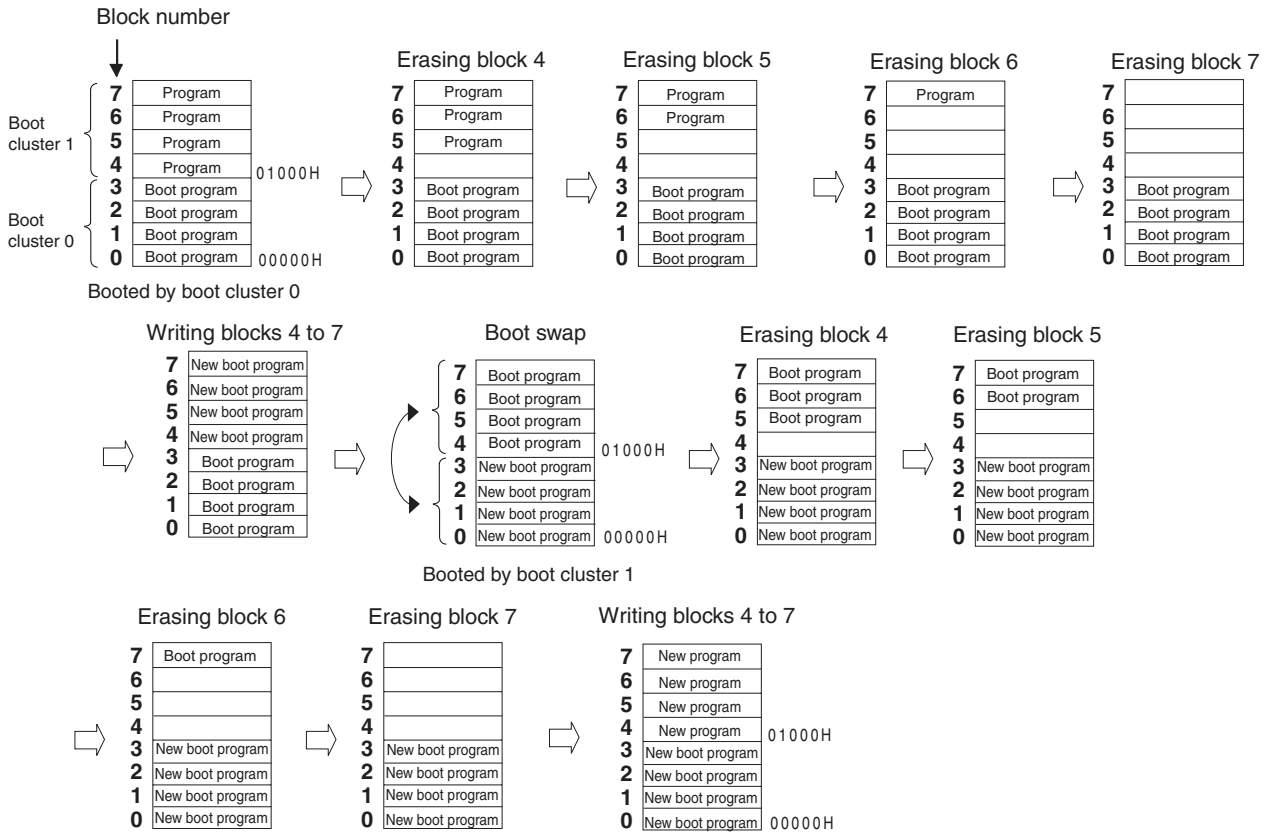


In an example of above figure, it is as follows.

Boot cluster 0: Boot program area before boot swap

Boot cluster 1: Boot program area after boot swap

Figure 26-19. Example of Executing Boot Swapping



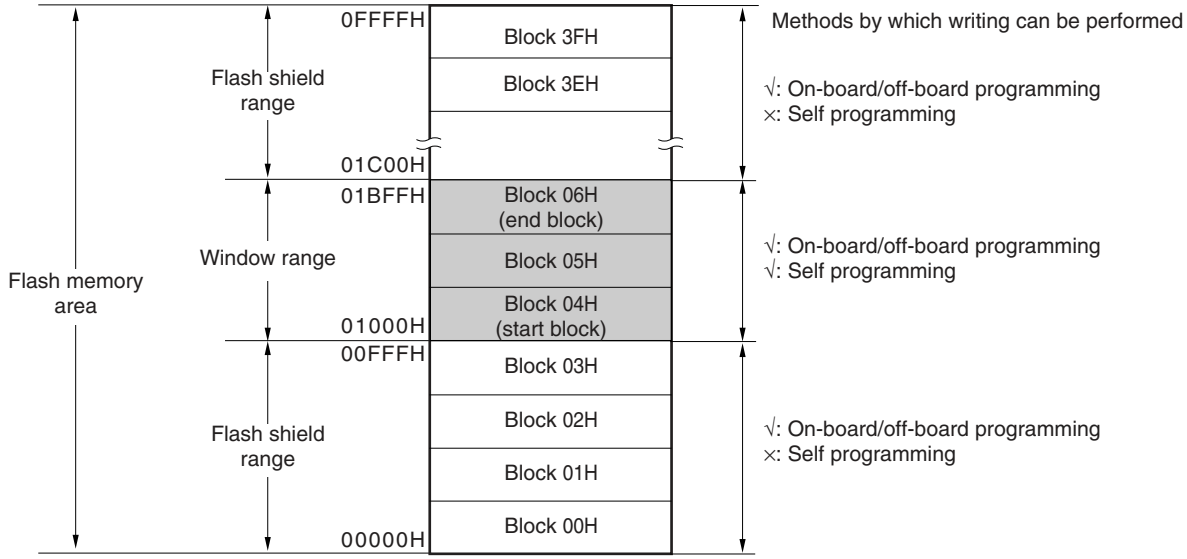
26.9.2 Flash shield window function

The flash shield window function is provided as one of the security functions for self programming. It disables writing to and erasing areas outside the range specified as a window only during self programming.

The window range can be set by specifying the start and end blocks. The window range can be set or changed during both on-board/off-board programming and self programming.

Writing to and erasing areas outside the window range are disabled during self programming. During on-board/off-board programming, however, areas outside the range specified as a window can be written and erased.

Figure 26-20. Flash Shield Window Setting Example
(Target Devices: μPD78F1003, Start Block: 04H, End Block: 06H)



Caution If the rewrite-prohibited area of the boot cluster 0 overlaps with the flash shield window range, prohibition to rewrite the boot cluster 0 takes priority.

Table 26-13. Relationship between Flash Shield Window Function Setting/Change Methods and Commands

Programming conditions	Window Range Setting/Change Methods	Execution Commands	
		Block erase	Write
Self-programming	Specify the starting and ending blocks by the set information library.	Block erasing is enabled only within the window range.	Writing is enabled only within the range of window range.
On-board/Off-board programming	Specify the starting and ending blocks on GUI of dedicated flash memory programmer, etc.	Block erasing is enabled also outside the window range.	Writing is enabled also outside the window range.

Remark See **26.7 Security Settings** to prohibit writing/erasing during on-board/off-board programming.

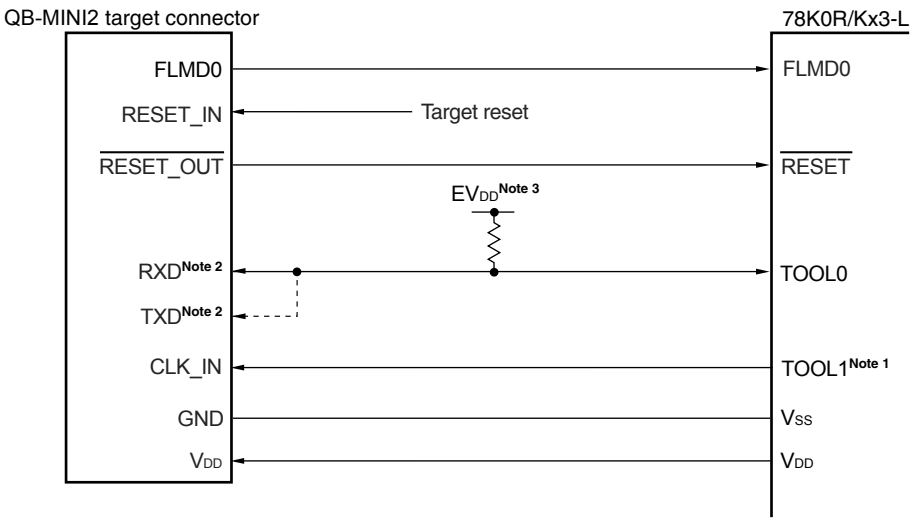
CHAPTER 27 ON-CHIP DEBUG FUNCTION

27.1 Connecting QB-MINI2 to 78K0R/Kx3-L

The 78K0R/Kx3-L uses the V_{DD}, FLMD0, $\overline{RESET}$, TOOL0, TOOL1[Note 1], and V_{SS} pins to communicate with the host machine via an on-chip debug emulator (QB-MINI2).

Caution The 78K0R/Kx3-L has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Figure 27-1. Connection Example of QB-MINI2 and 78K0R/Kx3-L



Notes 1. Connection is not required for communication in 1-line mode but required for communication in 2-line mode. At this time, perform necessary connections according to Table 2-3 Connection of Unused Pins (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or Table 3-3 Connection of Unused Pins (78K0R/KF3-L, 78K0R/KG3-L) since TOOL1 is an unused pin when QB-MINI2 is unconnected.

2. Connecting the dotted line is not necessary since RXD and TXD are shorted within QB-MIN2. When using the other flash memory programmer, RXD and TXD may not be shorted within the programmer. In this case, they must be shorted on the target system.

3. When using the 78K0R/KG3-L, read EV_{DD} as EV_{DD0} and EV_{DD1}.

Caution When communicating in 2-line mode, a clock with a frequency of half that of the CPU clock frequency is output from the TOOL1 pin. A resistor or ferrite bead can be used as a countermeasure against fluctuation of the power supply caused by that clock.

Remark The FLMD0 pin is recommended to be open for self-programming in on-chip debugging. To pull down externally, use a resistor of 100 kΩ or more.

1-line mode (single line UART) using the TOOL0 pin or 2-line mode using the TOOL0 and TOOL1 pins is used for serial communication For flash memory programming, 1-line mode is used. 1-line mode or 2-line mode is used for on-chip debugging. Table 27-1 lists the differences between 1-line mode and 2-line mode.

Table 27-1. Lists the Differences Between 1-line Mode and 2-line Mode.

Communication mode	Flash memory programming function
1-line mode	Available
2-line mode	None

Remark 2-line mode is not used for flash programming, however, even if the TOOL1 pin is connected with CLK_IN of QB-MINI2, writing is performed normally with no problem.

27.2 On-Chip Debug Security ID

The 78K0R/Kx3-L has an on-chip debug operation control bit in the flash memory at 000C3H (see **CHAPTER 25 OPTION BYTE**) and an on-chip debug security ID setting area at 000C4H to 000CDH, to prevent third parties from reading memory content.

When the boot swap function is used, also set a value that is the same as that of 010C3H and 010C4H to 010CDH in advance, because 000C3H, 000C4H to 000CDH and 010C3H, and 010C4H to 010CDH are switched.

For details on the on-chip debug security ID, refer to the **QB-MINI2 On-Chip Debug Emulator with Programming Function User's Manual (U18371E)**.

Table 27-2. On-Chip Debug Security ID

Address	On-Chip Debug Security ID
000C4H to 000CDH	Any ID code of 10 bytes
010C4H to 010CDH	

27.3 Securing of User Resources

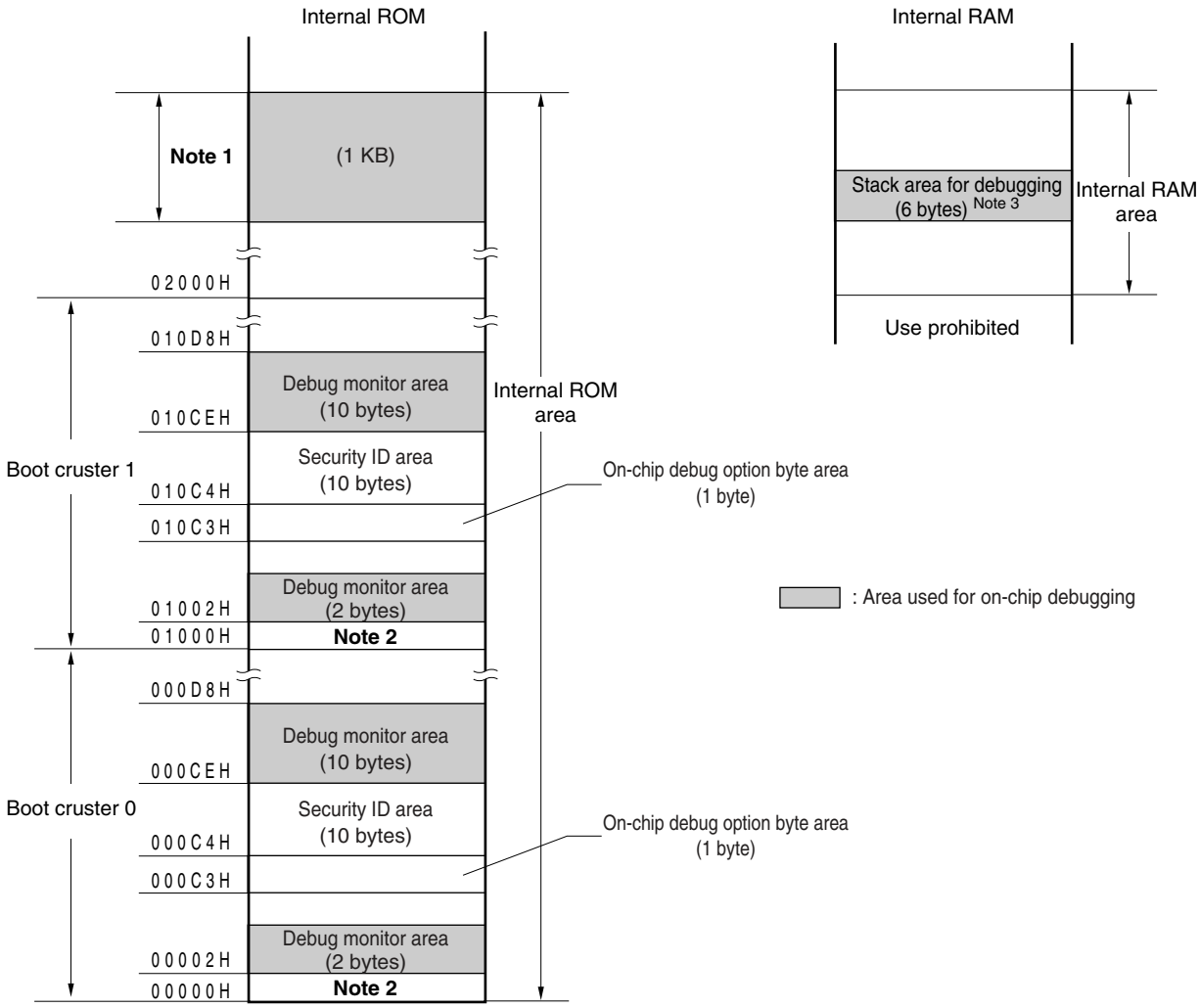
To perform communication between the 78K0R/Kx3-L and QB-MINI2, as well as each debug function, the securing of memory space must be done beforehand.

If Renesas Electronics assembler RA78K0R or compiler CC78K0R is used, the items can be set by using linker options.

(1) Securement of memory space

The shaded portions in Figure 27-2 are the areas reserved for placing the debug monitor program, so user programs or data cannot be allocated in these spaces. When using the on-chip debug function, these spaces must be secured so as not to be used by the user program. Moreover, this area must not be rewritten by the user program.

Figure 27-2. Memory Spaces Where Debug Monitor Programs Are Allocated



Notes 1. Address differs depending on products as follows.

Products ( ): Internal ROM	Address of **Note 1**
μPD78F1000 (16 KB)	03C00H to 03FFFH
μPD78F1001, 78F1004, 78F1007 (32 KB)	07C00H to 07FFFH
μPD78F1002, 78F1005, 78F1008 (48 KB)	0BC00H to 0BFFFH
μPD78F1003, 78F1006, 78F1009, 78F1010 (64 KB)	0FC00H to 0FFFFH
μPD78F1011, 78F1013 (96 KB)	17C00H to 17FFFH
μPD78F1012, 78F1014 (128 KB)	1FC00H to 1FFFFH
μPD78F1027, 78F1029 (192 KB)	2FC00H to 2FFFFH
μPD78F1028, 78F1030 (256 KB)	3FC00H to 3FFFFH

2. In debugging, reset vector is rewritten to address allocated to a monitor program.

3. Since this area is allocated immediately before the stack area, the address of this area varies depending on the stack increase and decrease. That is, 6 extra bytes are consumed for the stack area used.

For details of the way to secure of the memory space, refer to the QB-MINI2 On-Chip Debug Emulator with Programming Function User's Manual (U18371E).

CHAPTER 28 BCD CORRECTION CIRCUIT

28.1 BCD Correction Circuit Function

The result of addition/subtraction of the BCD (binary-coded decimal) code and BCD code can be obtained as BCD code with this circuit.

The decimal correction operation result is obtained by performing addition/subtraction having the A register as the operand and then adding/ subtracting the BCD correction result register (BCDADJ).

28.2 Registers Used by BCD Correction Circuit

The BCD correction circuit uses the following registers.

- BCD correction result register (BCDADJ)

(1) BCD correction result register (BCDADJ)

The BCDADJ register stores correction values for obtaining the add/subtract result as BCD code through add/subtract instructions using the A register as the operand.

The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags.

The BCDADJ register is read by an 8-bit memory manipulation instruction.

Reset input sets this register to undefined.

Figure 28-1. Format of BCD Correction Result Register (BCDADJ)

Address: F00FEH After reset: undefined R

Symbol	7	6	5	4	3	2	1	0
BCDADJ								

28.3 BCD Correction Circuit Operation

The basic operation of the BCD correction circuit is as follows.

(1) Addition: Calculating the result of adding a BCD code value and another BCD code value by using a BCD code value

<1> The BCD code value to which addition is performed is stored in the A register.

<2> By adding the value of the A register and the second operand (value of one more BCD code to be added) as are in binary, the binary operation result is stored in the A register and the correction value is stored in the BCD correction result register (BCDADJ).

<3> Decimal correction is performed by adding in binary the value of the A register (addition result in binary) and the BCDADJ register (correction value), and the correction result is stored in the A register and CY flag.

Caution The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags. Therefore, execute the instruction <3> after the instruction <2> instead of executing any other instructions. To perform BCD correction in the interrupt enabled state, saving and restoring the A register is required within the interrupt function. PSW (CY flag and AC flag) is restored by the RETI instruction.

An example is shown below.

Examples 1: 99 + 89 = 188

Instruction	A Register	CY Flag	AC Flag	BCDADJ Register
`MOV A, #99H ; <1>`	99H	–	–	–
`ADD A, #89H ; <2>`	22H	1	1	66H
`ADD A, !BCDADJ ; <3>`	88H	1	0	–

Examples 2: 85 + 15 = 100

Instruction	A Register	CY Flag	AC Flag	BCDADJ Register
`MOV A, #85H ; <1>`	85H	–	–	–
`ADD A, #15H ; <2>`	9AH	0	0	66H
`ADD A, !BCDADJ ; <3>`	00H	1	1	–

Examples 3: 80 + 80 = 160

Instruction	A Register	CY Flag	AC Flag	BCDADJ Register
`MOV A, #80H ; <1>`	80H	–	–	–
`ADD A, #80H ; <2>`	00H	1	0	60H
`ADD A, !BCDADJ ; <3>`	60H	1	0	–

(2) Subtraction: Calculating the result of subtracting a BCD code value from another BCD code value by using a BCD code value

<1> The BCD code value from which subtraction is performed is stored in the A register.

<2> By subtracting the value of the second operand (value of BCD code to be subtracted) from the A register as is in binary, the calculation result in binary is stored in the A register, and the correction value is stored in the BCD correction result register (BCDADJ).

<3> Decimal correction is performed by subtracting the value of the BCDADJ register (correction value) from the A register (subtraction result in binary) in binary, and the correction result is stored in the A register and CY flag.

Caution The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags. Therefore, execute the instruction <3> after the instruction <2> instead of executing any other instructions. To perform BCD correction in the interrupt enabled state, saving and restoring the A register is required within the interrupt function. PSW (CY flag and AC flag) is restored by the RETI instruction.

An example is shown below.

Example: 91 − 52 = 39

Instruction	A Register	CY Flag	AC Flag	BCDADJ Register
`MOV A, #91H ; <1>`	91H	–	–	–
`SUB A, #52H ; <2>`	3FH	0	1	06H
`SUB A, !BCDADJ ; <3>`	39H	0	0	–

CHAPTER 29 INSTRUCTION SET

This chapter lists the instructions in the 78K0R microcontroller instruction set. For details of each operation and operation code, refer to the separate document **78K0R Microcontrollers Instructions User's Manual (U17792E)**.

Remark The shaded parts of the tables in **Table 29-5 Operation List** indicate the operation or instruction format that is newly added for the 78K0R microcontrollers.

29.1 Conventions Used in Operation List

29.1.1 Operand identifiers and specification methods

Operands are described in the “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, !!, $, $!, [ ], and ES: are keywords and are described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: 16-bit absolute address specification
- !!: 20-bit absolute address specification
- $: 8-bit relative address specification
- $!: 16-bit relative address specification
- [ ]: Indirect address specification
- ES:: Extension address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, !!, $, $!, [ ], and ES: symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 29-1. Operand Identifiers and Specification Methods

Identifier	Description Method
r rp sfr sfrp	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special-function register symbol (SFR symbol) FFF00H to FFFFFH Special-function register symbols (16-bit manipulatable SFR symbol. Even addresses only[Note]) FFF00H to FFFFFH
saddr saddrp	FFE20H to FFF1FH Immediate data or labels FFE20H to FF1FH Immediate data or labels (even addresses only[Note])
addr20 addr16 addr5	00000H to FFFFFH Immediate data or labels 0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions[Note]) 0080H to 00BFH Immediate data or labels (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label
RBn	RB0 to RB3

Note Bit 0 = 0 when an odd address is specified.

Remark The special function registers can be described to operand sfr as symbols. See **Table 4-5 SFR List** for the symbols of the special function registers. The extended special function registers can be described to operand !addr16 as symbols. See **Table 4-6 Extended SFR (2nd SFR) List** for the symbols of the extended special function registers.

29.1.2 Description of operation column

The operation when the instruction is executed is shown in the “Operation” column using the following symbols.

Table 29-2. Symbols in “Operation” Column

Symbol	Function
A	A register; 8-bit accumulator
X	X register
B	B register
C	C register
D	D register
E	E register
H	H register
L	L register
ES	ES register
CS	CS register
AX	AX register pair; 16-bit accumulator
BC	BC register pair
DE	DE register pair
HL	HL register pair
PC	Program counter
SP	Stack pointer
PSW	Program status word
CY	Carry flag
AC	Auxiliary carry flag
Z	Zero flag
RBS	Register bank select flag
IE	Interrupt request enable flag
()	Memory contents indicated by address or register contents in parentheses
X_H, X_L X_S, X_H, X_L	16-bit registers: X_H = higher 8 bits, X_L = lower 8 bits 20-bit registers: X_S = (bits 19 to 16), X_H = (bits 15 to 8), X_L = (bits 7 to 0)
∧	Logical product (AND)
∨	Logical sum (OR)
∨	Exclusive logical sum (exclusive OR)
¯	Inverted data
addr5	16-bit immediate data (even addresses only in 0080H to 00BFH)
addr16	16-bit immediate data
addr20	20-bit immediate data
jdisp8	Signed 8-bit data (displacement value)
jdisp16	Signed 16-bit data (displacement value)

29.1.3 Description of flag operation column

The change of the flag value when the instruction is executed is shown in the “Flag” column using the following symbols.

Table 29-3. Symbols in “Flag” Column

Symbol	Change of Flag Value
(Blank)	Unchanged
0	Cleared to 0
1	Set to 1
×	Set/cleared according to the result
R	Previously saved value is restored

29.1.4 PREFIX instruction

Instructions with “ES:” have a PREFIX operation code as a prefix to extend the accessible data area to the 1 MB space (00000H to FFFFFH), by adding the ES register value to the 64 KB space from F0000H to FFFFFH. When a PREFIX operation code is attached as a prefix to the target instruction, only one instruction immediately after the PREFIX operation code is executed as the addresses with the ES register value added.

A interrupt and DMA transfer are not acknowledged between a PREFIX instruction code and the instruction immediately after.

Table 29-4. Use Example of PREFIX Operation Code

Instruction	Opcode				
	1	2	3	4	5
MOV !addr16, #byte	CFH	!addr16		#byte	–
MOV ES:!addr16, #byte	11H	CFH	!addr16		#byte
MOV A, [HL]	8BH	–	–	–	–
MOV A, ES:[HL]	11H	8BH	–	–	–

Caution Set the ES register value with MOV ES, A, etc., before executing the PREFIX instruction.

29.2 Operation List

Table 29-5. Operation List (1/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	MOV	r, #byte	2	1	–	r ← byte			
		saddr, #byte	3	1	–	(saddr) ← byte			
		sfr, #byte	3	1	–	sfr ← byte			
		!addr16, #byte	4	1	–	(addr16) ← byte			
		A, r Note 3	1	1	–	A ← r			
		r, A Note 3	1	1	–	r ← A			
		A, saddr	2	1	–	A ← (saddr)			
		saddr, A	2	1	–	(saddr) ← A			
		A, sfr	2	1	–	A ← sfr			
		sfr, A	2	1	–	sfr ← A			
		A, !addr16	3	1	4	A ← (addr16)			
		!addr16, A	3	1	–	(addr16) ← A			
		PSW, #byte	3	3	–	PSW ← byte	×	×	×
		A, PSW	2	1	–	A ← PSW			
		PSW, A	2	3	–	PSW ← A	×	×	×
		ES, #byte	2	1	–	ES ← byte			
		ES, saddr	3	1	–	ES ← (saddr)			
		A, ES	2	1	–	A ← ES			
		ES, A	2	1	–	ES ← A			
		CS, #byte	3	1	–	CS ← byte			
		A, CS	2	1	–	A ← CS			
		CS, A	2	1	–	CS ← A			
		A, [DE]	1	1	4	A ← (DE)			
		[DE], A	1	1	–	(DE) ← A			
		[DE + byte], #byte	3	1	–	(DE + byte) ← byte			
		A, [DE + byte]	2	1	4	A ← (DE + byte)			
		[DE + byte], A	2	1	–	(DE + byte) ← A			
		A, [HL]	1	1	4	A ← (HL)			
		[HL], A	1	1	–	(HL) ← A			
		[HL + byte], #byte	3	1	–	(HL + byte) ← byte			

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except r = A

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (2/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	MOV	A, [HL + byte]	2	1	4	A ← (HL + byte)	
		[HL + byte], A	2	1	–	(HL + byte) ← A	
		A, [HL + B]	2	1	4	A ← (HL + B)	
		[HL + B], A	2	1	–	(HL + B) ← A	
		A, [HL + C]	2	1	4	A ← (HL + C)	
		[HL + C], A	2	1	–	(HL + C) ← A	
		word[B], #byte	4	1	–	(B + word) ← byte	
		A, word[B]	3	1	4	A ← (B + word)	
		word[B], A	3	1	–	(B + word) ← A	
		word[C], #byte	4	1	–	(C + word) ← byte	
		A, word[C]	3	1	4	A ← (C + word)	
		word[C], A	3	1	–	(C + word) ← A	
		word[BC], #byte	4	1	–	(BC + word) ← byte	
		A, word[BC]	3	1	4	A ← (BC + word)	
		word[BC], A	3	1	–	(BC + word) ← A	
		[SP + byte], #byte	3	1	–	(SP + byte) ← byte	
		A, [SP + byte]	2	1	–	A ← (SP + byte)	
		[SP + byte], A	2	1	–	(SP + byte) ← A	
		B, saddr	2	1	–	B ← (saddr)	
		B, !addr16	3	1	4	B ← (addr16)	
		C, saddr	2	1	–	C ← (saddr)	
		C, !addr16	3	1	4	C ← (addr16)	
		X, saddr	2	1	–	X ← (saddr)	
		X, !addr16	3	1	4	X ← (addr16)	
		ES:!addr16, #byte	5	2	–	(ES, addr16) ← byte	
		A, ES:!addr16	4	2	5	A ← (ES, addr16)	
		ES:!addr16, A	4	2	–	(ES, addr16) ← A	
		A, ES:[DE]	2	2	5	A ← (ES, DE)	
		ES:[DE], A	2	2	–	(ES, DE) ← A	
		ES:[DE + byte],#byte	4	2	–	((ES, DE) + byte) ← byte	
		A, ES:[DE + byte]	3	2	5	A ← ((ES, DE) + byte)	
		ES:[DE + byte], A	3	2	–	((ES, DE) + byte) ← A	

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (3/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	MOV	A, ES:[HL]	2	2	5	A ← (ES, HL)	
		ES:[HL], A	2	2	–	(ES, HL) ← A	
		ES:[HL + byte],#byte	4	2	–	((ES, HL) + byte) ← byte	
		A, ES:[HL + byte]	3	2	5	A ← ((ES, HL) + byte)	
		ES:[HL + byte], A	3	2	–	((ES, HL) + byte) ← A	
		A, ES:[HL + B]	3	2	5	A ← ((ES, HL) + B)	
		ES:[HL + B], A	3	2	–	((ES, HL) + B) ← A	
		A, ES:[HL + C]	3	2	5	A ← ((ES, HL) + C)	
		ES:[HL + C], A	3	2	–	((ES, HL) + C) ← A	
		ES:word[B], #byte	5	2	–	((ES, B) + word) ← byte	
		A, ES:word[B]	4	2	5	A ← ((ES, B) + word)	
		ES:word[B], A	4	2	–	((ES, B) + word) ← A	
		ES:word[C], #byte	5	2	–	((ES, C) + word) ← byte	
		A, ES:word[C]	4	2	5	A ← ((ES, C) + word)	
		ES:word[C], A	4	2	–	((ES, C) + word) ← A	
		ES:word[BC], #byte	5	2	–	((ES, BC) + word) ← byte	
		A, ES:word[BC]	4	2	5	A ← ((ES, BC) + word)	
		ES:word[BC], A	4	2	–	((ES, BC) + word) ← A	
		B, ES:!addr16	4	2	5	B ← (ES, addr16)	
		C, ES:!addr16	4	2	5	C ← (ES, addr16)	
		X, ES:!addr16	4	2	5	X ← (ES, addr16)	
	XCH	A, r Note 3	1 (r = X) 2 (other than r = X)	1	–	A ←→ r	
		A, saddr	3	2	–	A ←→ (saddr)	
		A, sfr	3	2	–	A ←→ sfr	
		A, !addr16	4	2	–	A ←→ (addr16)	
		A, [DE]	2	2	–	A ←→ (DE)	
		A, [DE + byte]	3	2	–	A ←→ (DE + byte)	
		A, [HL]	2	2	–	A ←→ (HL)	
		A, [HL + byte]	3	2	–	A ←→ (HL + byte)	
		A, [HL + B]	2	2	–	A ←→ (HL + B)	
		A, [HL + C]	2	2	–	A ←→ (HL + C)	

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except r = A

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (4/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	XCH	A, ES:!addr16	5	3	–	A ←→ (ES, addr16)			
		A, ES:[DE]	3	3	–	A ←→ (ES, DE)			
		A, ES:[DE + byte]	4	3	–	A ←→ ((ES, DE) + byte)			
		A, ES:[HL]	3	3	–	A ←→ (ES, HL)			
		A, ES:[HL + byte]	4	3	–	A ←→ ((ES, HL) + byte)			
		A, ES:[HL + B]	3	3	–	A ←→ ((ES, HL) + B)			
		A, ES:[HL + C]	3	3	–	A ←→ ((ES, HL) + C)			
	ONEB	A	1	1	–	A ← 01H			
		X	1	1	–	X ← 01H			
		B	1	1	–	B ← 01H			
		C	1	1	–	C ← 01H			
		saddr	2	1	–	(saddr) ← 01H			
		!addr16	3	1	–	(addr16) ← 01H			
		ES:!addr16	4	2	–	(ES, addr16) ← 01H			
	CLRB	A	1	1	–	A ← 00H			
		X	1	1	–	X ← 00H			
		B	1	1	–	B ← 00H			
		C	1	1	–	C ← 00H			
		saddr	2	1	–	(saddr) ← 00H			
		!addr16	3	1	–	(addr16) ← 00H			
		ES:!addr16	4	2	–	(ES,addr16) ← 00H			
	MOVS	[HL + byte], X	3	1	–	(HL + byte) ← X	×		×
		ES:[HL + byte], X	4	2	–	(ES, HL + byte) ← X	×		×
16-bit data transfer	MOVW	rp, #word	3	1	–	rp ← word			
		saddrp, #word	4	1	–	(saddrp) ← word			
		sfrp, #word	4	1	–	sfrp ← word			
		AX, saddrp	2	1	–	AX ← (saddrp)			
		saddrp, AX	2	1	–	(saddrp) ← AX			
		AX, sfrp	2	1	–	AX ← sfrp			
		sfrp, AX	2	1	–	sfrp ← AX			
		AX, rp Note 3	1	1	–	AX ← rp			
		rp, AX Note 3	1	1	–	rp ← AX			

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except rp = AX

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (5/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit data transfer	MOVW	AX, !addr16	3	1	4	AX ← (addr16)			
		!addr16, AX	3	1	–	(addr16) ← AX			
		AX, [DE]	1	1	4	AX ← (DE)			
		[DE], AX	1	1	–	(DE) ← AX			
		AX, [DE + byte]	2	1	4	AX ← (DE + byte)			
		[DE + byte], AX	2	1	–	(DE + byte) ← AX			
		AX, [HL]	1	1	4	AX ← (HL)			
		[HL], AX	1	1	–	(HL) ← AX			
		AX, [HL + byte]	2	1	4	AX ← (HL + byte)			
		[HL + byte], AX	2	1	–	(HL + byte) ← AX			
		AX, word[B]	3	1	4	AX ← (B + word)			
		word[B], AX	3	1	–	(B + word) ← AX			
		AX, word[C]	3	1	4	AX ← (C + word)			
		word[C], AX	3	1	–	(C + word) ← AX			
		AX, word[BC]	3	1	4	AX ← (BC + word)			
		word[BC], AX	3	1	–	(BC + word) ← AX			
		AX, [SP + byte]	2	1	–	AX ← (SP + byte)			
		[SP + byte], AX	2	1	–	(SP + byte) ← AX			
		BC, saddrp	2	1	–	BC ← (saddrp)			
		BC, !addr16	3	1	4	BC ← (addr16)			
		DE, saddrp	2	1	–	DE ← (saddrp)			
		DE, !addr16	3	1	4	DE ← (addr16)			
		HL, saddrp	2	1	–	HL ← (saddrp)			
		HL, !addr16	3	1	4	HL ← (addr16)			
		AX, ES:!addr16	4	2	5	AX ← (ES, addr16)			
		ES:!addr16, AX	4	2	–	(ES, addr16) ← AX			
		AX, ES:[DE]	2	2	5	AX ← (ES, DE)			
		ES:[DE], AX	2	2	–	(ES, DE) ← AX			
		AX, ES:[DE + byte]	3	2	5	AX ← ((ES, DE) + byte)			
		ES:[DE + byte], AX	3	2	–	((ES, DE) + byte) ← AX			
		AX, ES:[HL]	2	2	5	AX ← (ES, HL)			
		ES:[HL], AX	2	2	–	(ES, HL) ← AX			

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (6/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit data transfer	MOVW	AX, ES:[HL + byte]	3	2	5	AX ← ((ES, HL) + byte)			
		ES:[HL + byte], AX	3	2	–	((ES, HL) + byte) ← AX			
		AX, ES:word[B]	4	2	5	AX ← ((ES, B) + word)			
		ES:word[B], AX	4	2	–	((ES, B) + word) ← AX			
		AX, ES:word[C]	4	2	5	AX ← ((ES, C) + word)			
		ES:word[C], AX	4	2	–	((ES, C) + word) ← AX			
		AX, ES:word[BC]	4	2	5	AX ← ((ES, BC) + word)			
		ES:word[BC], AX	4	2	–	((ES, BC) + word) ← AX			
		BC, ES:!addr16	4	2	5	BC ← (ES, addr16)			
		DE, ES:!addr16	4	2	5	DE ← (ES, addr16)			
		HL, ES:!addr16	4	2	5	HL ← (ES, addr16)			
	XCHW	AX, rp Note 3	1	1	–	AX ←→ rp			
	ONEW	AX	1	1	–	AX ← 0001H			
		BC	1	1	–	BC ← 0001H			
	CLRW	AX	1	1	–	AX ← 0000H			
		BC	1	1	–	BC ← 0000H			
8-bit operation	ADD	A, #byte	2	1	–	A, CY ← A + byte	×	×	×
		saddr, #byte	3	2	–	(saddr), CY ← (saddr) + byte	×	×	×
		A, r Note 4	2	1	–	A, CY ← A + r	×	×	×
		r, A	2	1	–	r, CY ← r + A	×	×	×
		A, saddr	2	1	–	A, CY ← A + (saddr)	×	×	×
		A, !addr16	3	1	4	A, CY ← A + (addr16)	×	×	×
		A, [HL]	1	1	4	A, CY ← A + (HL)	×	×	×
		A, [HL + byte]	2	1	4	A, CY ← A + (HL + byte)	×	×	×
		A, [HL + B]	2	1	4	A, CY ← A + (HL + B)	×	×	×
		A, [HL + C]	2	1	4	A, CY ← A + (HL + C)	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A + (ES, addr16)	×	×	×
		A, ES:[HL]	2	2	5	A,CY ← A + (ES, HL)	×	×	×
		A, ES:[HL + byte]	3	2	5	A,CY ← A + ((ES, HL) + byte)	×	×	×
		A, ES:[HL + B]	3	2	5	A,CY ← A + ((ES, HL) + B)	×	×	×
		A, ES:[HL + C]	3	2	5	A,CY ← A + ((ES, HL) + C)	×	×	×

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except rp = AX

4. Except r = A

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (7/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	ADDC	A, #byte	2	1	–	A, CY ← A + byte + CY	×	×	×
		saddr, #byte	3	2	–	(saddr), CY ← (saddr) + byte + CY	×	×	×
		A, r Note 3	2	1	–	A, CY ← A + r + CY	×	×	×
		r, A	2	1	–	r, CY ← r + A + CY	×	×	×
		A, saddr	2	1	–	A, CY ← A + (saddr) + CY	×	×	×
		A, !addr16	3	1	4	A, CY ← A + (addr16) + CY	×	×	×
		A, [HL]	1	1	4	A, CY ← A + (HL) + CY	×	×	×
		A, [HL + byte]	2	1	4	A, CY ← A + (HL + byte) + CY	×	×	×
		A, [HL + B]	2	1	4	A, CY ← A + (HL + B) + CY	×	×	×
		A, [HL + C]	2	1	4	A, CY ← A + (HL + C) + CY	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A + (ES, addr16) + CY	×	×	×
		A, ES:[HL]	2	2	5	A, CY ← A + (ES, HL) + CY	×	×	×
		A, ES:[HL + byte]	3	2	5	A, CY ← A + ((ES, HL) + byte) + CY	×	×	×
		A, ES:[HL + B]	3	2	5	A, CY ← A + ((ES, HL) + B) + CY	×	×	×
		A, ES:[HL + C]	3	2	5	A, CY ← A + ((ES, HL) + C) + CY	×	×	×
	SUB	A, #byte	2	1	–	A, CY ← A – byte	×	×	×
		saddr, #byte	3	2	–	(saddr), CY ← (saddr) – byte	×	×	×
		A, r Note 3	2	1	–	A, CY ← A – r	×	×	×
		r, A	2	1	–	r, CY ← r – A	×	×	×
		A, saddr	2	1	–	A, CY ← A – (saddr)	×	×	×
		A, !addr16	3	1	4	A, CY ← A – (addr16)	×	×	×
		A, [HL]	1	1	4	A, CY ← A – (HL)	×	×	×
		A, [HL + byte]	2	1	4	A, CY ← A – (HL + byte)	×	×	×
		A, [HL + B]	2	1	4	A, CY ← A – (HL + B)	×	×	×
		A, [HL + C]	2	1	4	A, CY ← A – (HL + C)	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A – (ES:addr16)	×	×	×
		A, ES:[HL]	2	2	5	A, CY ← A – (ES:HL)	×	×	×
		A, ES:[HL + byte]	3	2	5	A, CY ← A – ((ES:HL) + byte)	×	×	×
		A, ES:[HL + B]	3	2	5	A, CY ← A – ((ES:HL) + B)	×	×	×
		A, ES:[HL + C]	3	2	5	A, CY ← A – ((ES:HL) + C)	×	×	×

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except r = A

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (8/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	SUBC	A, #byte	2	1	–	A, CY ← A – byte – CY	×	×	×
		saddr, #byte	3	2	–	(saddr), CY ← (saddr) – byte – CY	×	×	×
		A, r Note 3	2	1	–	A, CY ← A – r – CY	×	×	×
		r, A	2	1	–	r, CY ← r – A – CY	×	×	×
		A, saddr	2	1	–	A, CY ← A – (saddr) – CY	×	×	×
		A, !addr16	3	1	4	A, CY ← A – (addr16) – CY	×	×	×
		A, [HL]	1	1	4	A, CY ← A – (HL) – CY	×	×	×
		A, [HL + byte]	2	1	4	A, CY ← A – (HL + byte) – CY	×	×	×
		A, [HL + B]	2	1	4	A, CY ← A – (HL + B) – CY	×	×	×
		A, [HL + C]	2	1	4	A, CY ← A – (HL + C) – CY	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A – (ES:addr16) – CY	×	×	×
		A, ES:[HL]	2	2	5	A, CY ← A – (ES:HL) – CY	×	×	×
		A, ES:[HL + byte]	3	2	5	A, CY ← A – ((ES:HL) + byte) – CY	×	×	×
		A, ES:[HL + B]	3	2	5	A, CY ← A – ((ES:HL) + B) – CY	×	×	×
		A, ES:[HL + C]	3	2	5	A, CY ← A – ((ES:HL) + C) – CY	×	×	×
	AND	A, #byte	2	1	–	A ← A ∧ byte	×		
		saddr, #byte	3	2	–	(saddr) ← (saddr) ∧ byte	×		
		A, r Note 3	2	1	–	A ← A ∧ r	×		
		r, A	2	1	–	r ← r ∧ A	×		
		A, saddr	2	1	–	A ← A ∧ (saddr)	×		
		A, !addr16	3	1	4	A ← A ∧ (addr16)	×		
		A, [HL]	1	1	4	A ← A ∧ (HL)	×		
		A, [HL + byte]	2	1	4	A ← A ∧ (HL + byte)	×		
		A, [HL + B]	2	1	4	A ← A ∧ (HL + B)	×		
		A, [HL + C]	2	1	4	A ← A ∧ (HL + C)	×		
		A, ES:!addr16	4	2	5	A ← A ∧ (ES:addr16)	×		
		A, ES:[HL]	2	2	5	A ← A ∧ (ES:HL)	×		
		A, ES:[HL + byte]	3	2	5	A ← A ∧ ((ES:HL) + byte)	×		
		A, ES:[HL + B]	3	2	5	A ← A ∧ ((ES:HL) + B)	×		
		A, ES:[HL + C]	3	2	5	A ← A ∧ ((ES:HL) + C)	×		

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except r = A

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (9/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	OR	A, #byte	2	1	–	A ← A ∨ byte	×		
		saddr, #byte	3	2	–	(saddr) ← (saddr) ∨ byte	×		
		A, r Note 3	2	1	–	A ← A ∨ r	×		
		r, A	2	1	–	r ← r ∨ A	×		
		A, saddr	2	1	–	A ← A ∨ (saddr)	×		
		A, !addr16	3	1	4	A ← A ∨ (addr16)	×		
		A, [HL]	1	1	4	A ← A ∨ (HL)	×		
		A, [HL + byte]	2	1	4	A ← A ∨ (HL + byte)	×		
		A, [HL + B]	2	1	4	A ← A ∨ (HL + B)	×		
		A, [HL + C]	2	1	4	A ← A ∨ (HL + C)	×		
		A, ES:!addr16	4	2	5	A ← A ∨ (ES:addr16)	×		
		A, ES:[HL]	2	2	5	A ← A ∨ (ES:HL)	×		
		A, ES:[HL + byte]	3	2	5	A ← A ∨ ((ES:HL) + byte)	×		
		A, ES:[HL + B]	3	2	5	A ← A ∨ ((ES:HL) + B)	×		
		A, ES:[HL + C]	3	2	5	A ← A ∨ ((ES:HL) + C)	×		
	XOR	A, #byte	2	1	–	A ← A ⊻ byte	×		
		saddr, #byte	3	2	–	(saddr) ← (saddr) ⊻ byte	×		
		A, r Note 3	2	1	–	A ← A ⊻ r	×		
		r, A	2	1	–	r ← r ⊻ A	×		
		A, saddr	2	1	–	A ← A ⊻ (saddr)	×		
		A, !addr16	3	1	4	A ← A ⊻ (addr16)	×		
		A, [HL]	1	1	4	A ← A ⊻ (HL)	×		
		A, [HL + byte]	2	1	4	A ← A ⊻ (HL + byte)	×		
		A, [HL + B]	2	1	4	A ← A ⊻ (HL + B)	×		
		A, [HL + C]	2	1	4	A ← A ⊻ (HL + C)	×		
		A, ES:!addr16	4	2	5	A ← A ⊻ (ES:addr16)	×		
		A, ES:[HL]	2	2	5	A ← A ⊻ (ES:HL)	×		
		A, ES:[HL + byte]	3	2	5	A ← A ⊻ ((ES:HL) + byte)	×		
		A, ES:[HL + B]	3	2	5	A ← A ⊻ ((ES:HL) + B)	×		
		A, ES:[HL + C]	3	2	5	A ← A ⊻ ((ES:HL) + C)	×		

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except r = A

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (10/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	CMP	A, #byte	2	1	–	A – byte	×	×	×
		saddr, #byte	3	1	–	(saddr) – byte	×	×	×
		A, r Note 3	2	1	–	A – r	×	×	×
		r, A	2	1	–	r – A	×	×	×
		A, saddr	2	1	–	A – (saddr)	×	×	×
		A, !addr16	3	1	4	A – (addr16)	×	×	×
		A, [HL]	1	1	4	A – (HL)	×	×	×
		A, [HL + byte]	2	1	4	A – (HL + byte)	×	×	×
		A, [HL + B]	2	1	4	A – (HL + B)	×	×	×
		A, [HL + C]	2	1	4	A – (HL + C)	×	×	×
		!addr16, #byte	4	1	4	(addr16) – byte	×	×	×
		A, ES:!addr16	4	2	5	A – (ES:addr16)	×	×	×
		A, ES:[HL]	2	2	5	A – (ES:HL)	×	×	×
		A, ES:[HL + byte]	3	2	5	A – ((ES:HL) + byte)	×	×	×
		A, ES:[HL + B]	3	2	5	A – ((ES:HL) + B)	×	×	×
		A, ES:[HL + C]	3	2	5	A – ((ES:HL) + C)	×	×	×
		ES:!addr16, #byte	5	2	5	(ES:addr16) – byte	×	×	×
	CMP0	A	1	1	–	A – 00H	×	×	×
		X	1	1	–	X – 00H	×	×	×
		B	1	1	–	B – 00H	×	×	×
		C	1	1	–	C – 00H	×	×	×
		saddr	2	1	–	(saddr) – 00H	×	×	×
		!addr16	3	1	4	(addr16) – 00H	×	×	×
		ES:!addr16	4	2	5	(ES:addr16) – 00H	×	×	×
	CMPS	X, [HL + byte]	3	1	4	X – (HL + byte)	×	×	×
		X, ES:[HL + byte]	4	2	5	X – ((ES:HL) + byte)	×	×	×

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except r = A

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (11/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit operation	ADDW	AX, #word	3	1	–	AX, CY ← AX + word	×	×	×
		AX, AX	1	1	–	AX, CY ← AX + AX	×	×	×
		AX, BC	1	1	–	AX, CY ← AX + BC	×	×	×
		AX, DE	1	1	–	AX, CY ← AX + DE	×	×	×
		AX, HL	1	1	–	AX, CY ← AX + HL	×	×	×
		AX, saddrp	2	1	–	AX, CY ← AX + (saddrp)	×	×	×
		AX, !addr16	3	1	4	AX, CY ← AX + (addr16)	×	×	×
		AX, [HL+byte]	3	1	4	AX, CY ← AX + (HL + byte)	×	×	×
		AX, ES:!addr16	4	2	5	AX, CY ← AX + (ES:addr16)	×	×	×
		AX, ES: [HL+byte]	4	2	5	AX, CY ← AX + ((ES:HL) + byte)	×	×	×
	SUBW	AX, #word	3	1	–	AX, CY ← AX – word	×	×	×
		AX, BC	1	1	–	AX, CY ← AX – BC	×	×	×
		AX, DE	1	1	–	AX, CY ← AX – DE	×	×	×
		AX, HL	1	1	–	AX, CY ← AX – HL	×	×	×
		AX, saddrp	2	1	–	AX, CY ← AX – (saddrp)	×	×	×
		AX, !addr16	3	1	4	AX, CY ← AX – (addr16)	×	×	×
		AX, [HL+byte]	3	1	4	AX, CY ← AX – (HL + byte)	×	×	×
		AX, ES:!addr16	4	2	5	AX, CY ← AX – (ES:addr16)	×	×	×
		AX, ES: [HL+byte]	4	2	5	AX, CY ← AX – ((ES:HL) + byte)	×	×	×
	CMPW	AX, #word	3	1	–	AX – word	×	×	×
		AX, BC	1	1	–	AX – BC	×	×	×
		AX, DE	1	1	–	AX – DE	×	×	×
		AX, HL	1	1	–	AX – HL	×	×	×
		AX, saddrp	2	1	–	AX – (saddrp)	×	×	×
		AX, !addr16	3	1	4	AX – (addr16)	×	×	×
		AX, [HL+byte]	3	1	4	AX – (HL + byte)	×	×	×
		AX, ES:!addr16	4	2	5	AX – (ES:addr16)	×	×	×
		AX, ES: [HL+byte]	4	2	5	AX – ((ES:HL) + byte)	×	×	×
Multiply	MULU	X	1	1	–	AX ← A × X			

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (12/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Increment/ decrement	INC	r	1	1	–	r ← r + 1	×	×	
		saddr	2	2	–	(saddr) ← (saddr) + 1	×	×	
		!addr16	3	2	–	(addr16) ← (addr16) + 1	×	×	
		[HL+byte]	3	2	–	(HL+byte) ← (HL+byte) + 1	×	×	
		ES:!addr16	4	3	–	(ES, addr16) ← (ES, addr16) + 1	×	×	
		ES: [HL+byte]	4	3	–	((ES:HL) + byte) ← ((ES:HL) + byte) + 1	×	×	
	DEC	r	1	1	–	r ← r – 1	×	×	
		saddr	2	2	–	(saddr) ← (saddr) – 1	×	×	
		!addr16	3	2	–	(addr16) ← (addr16) – 1	×	×	
		[HL+byte]	3	2	–	(HL+byte) ← (HL+byte) – 1	×	×	
		ES:!addr16	4	3	–	(ES, addr16) ← (ES, addr16) – 1	×	×	
		ES: [HL+byte]	4	3	–	((ES:HL) + byte) ← ((ES:HL) + byte) – 1	×	×	
	INCW	rp	1	1	–	rp ← rp + 1			
		saddrp	2	2	–	(saddrp) ← (saddrp) + 1			
		!addr16	3	2	–	(addr16) ← (addr16) + 1			
		[HL+byte]	3	2	–	(HL+byte) ← (HL+byte) + 1			
		ES:!addr16	4	3	–	(ES, addr16) ← (ES, addr16) + 1			
		ES: [HL+byte]	4	3	–	((ES:HL) + byte) ← ((ES:HL) + byte) + 1			
	DECW	rp	1	1	–	rp ← rp – 1			
		saddrp	2	2	–	(saddrp) ← (saddrp) – 1			
		!addr16	3	2	–	(addr16) ← (addr16) – 1			
		[HL+byte]	3	2	–	(HL+byte) ← (HL+byte) – 1			
		ES:!addr16	4	3	–	(ES, addr16) ← (ES, addr16) – 1			
		ES: [HL+byte]	4	3	–	((ES:HL) + byte) ← ((ES:HL) + byte) – 1			
Shift	SHR	A, cnt	2	1	–	(CY ← A_0, A_{m-1} ← A_m, A_7 ← 0) × cnt			×
	SHRW	AX, cnt	2	1	–	(CY ← AX_0, AX_{m-1} ← AX_m, AX_{15} ← 0) × cnt			×
	SHL	A, cnt	2	1	–	(CY ← A_7, A_m ← A_{m-1}, A_0 ← 0) × cnt			×
		B, cnt	2	1	–	(CY ← B_7, B_m ← B_{m-1}, B_0 ← 0) × cnt			×
		C, cnt	2	1	–	(CY ← C_7, C_m ← C_{m-1}, C_0 ← 0) × cnt			×
	SHLW	AX, cnt	2	1	–	(CY ← AX_{15}, AX_m ← AX_{m-1}, AX_0 ← 0) × cnt			×
		BC, cnt	2	1	–	(CY ← BC_{15}, BC_m ← BC_{m-1}, BC_0 ← 0) × cnt			×
	SAR	A, cnt	2	1	–	(CY ← A_0, A_{m-1} ← A_m, A_7 ← A_7) × cnt			×
	SARW	AX, cnt	2	1	–	(CY ← AX_0, AX_{m-1} ← AX_m, AX_{15} ← AX_{15}) × cnt			×

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

3. cnt indicates the bit shift count.

Table 29-5. Operation List (13/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Rotate	ROR	A, 1	2	1	–	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1			×
	ROL	A, 1	2	1	–	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1			×
	RORC	A, 1	2	1	–	(CY $\leftarrow A_0$, $A_7 \leftarrow$ CY, $A_{m-1} \leftarrow A_m$) × 1			×
	ROLC	A, 1	2	1	–	(CY $\leftarrow A_7$, $A_0 \leftarrow$ CY, $A_{m+1} \leftarrow A_m$) × 1			×
	ROLWC	AX,1	2	1	–	(CY $\leftarrow AX_{15}$, $AX_0 \leftarrow$ CY, $AX_{m+1} \leftarrow AX_m$) × 1			×
		BC,1	2	1	–	(CY $\leftarrow BC_{15}$, $BC_0 \leftarrow$ CY, $BC_{m+1} \leftarrow BC_m$) × 1			×
Bit manipulate	MOV1	CY, saddr.bit	3	1	–	CY ← (saddr).bit			×
		CY, sfr.bit	3	1	–	CY ← sfr.bit			×
		CY, A.bit	2	1	–	CY ← A.bit			×
		CY, PSW.bit	3	1	–	CY ← PSW.bit			×
		CY,[HL].bit	2	1	4	CY ← (HL).bit			×
		saddr.bit, CY	3	2	–	(saddr).bit ← CY			
		sfr.bit, CY	3	2	–	sfr.bit ← CY			
		A.bit, CY	2	1	–	A.bit ← CY			
		PSW.bit, CY	3	4	–	PSW.bit ← CY	×	×	
		[HL].bit, CY	2	2	–	(HL).bit ← CY			
		CY, ES:[HL].bit	3	2	5	CY ← (ES, HL).bit			×
		ES:[HL].bit, CY	3	3	–	(ES, HL).bit ← CY			
	AND1	CY, saddr.bit	3	1	–	CY ← CY ∧ (saddr).bit			×
		CY, sfr.bit	3	1	–	CY ← CY ∧ sfr.bit			×
		CY, A.bit	2	1	–	CY ← CY ∧ A.bit			×
		CY, PSW.bit	3	1	–	CY ← CY ∧ PSW.bit			×
		CY,[HL].bit	2	1	4	CY ← CY ∧ (HL).bit			×
		CY, ES:[HL].bit	3	2	5	CY ← CY ∧ (ES, HL).bit			×
	OR1	CY, saddr.bit	3	1	–	CY ← CY ∨ (saddr).bit			×
		CY, sfr.bit	3	1	–	CY ← CY ∨ sfr.bit			×
		CY, A.bit	2	1	–	CY ← CY ∨ A.bit			×
		CY, PSW.bit	3	1	–	CY ← CY ∨ PSW.bit			×
		CY, [HL].bit	2	1	4	CY ← CY ∨ (HL).bit			×
		CY, ES:[HL].bit	3	2	5	CY ← CY ∨ (ES, HL).bit			×

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (14/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Bit manipulate	XOR1	CY, saddr.bit	3	1	–	CY ← CY ⊻ (saddr).bit			×
		CY, sfr.bit	3	1	–	CY ← CY ⊻ sfr.bit			×
		CY, A.bit	2	1	–	CY ← CY ⊻ A.bit			×
		CY, PSW.bit	3	1	–	CY ← CY ⊻ PSW.bit			×
		CY, [HL].bit	2	1	4	CY ← CY ⊻ (HL).bit			×
		CY, ES:[HL].bit	3	2	5	CY ← CY ⊻ (ES, HL).bit			×
	SET1	saddr.bit	3	2	–	(saddr).bit ← 1			
		sfr.bit	3	2	–	sfr.bit ← 1			
		A.bit	2	1	–	A.bit ← 1			
		!addr16.bit	4	2	–	(addr16).bit ← 1			
		PSW.bit	3	4	–	PSW.bit ← 1	×	×	×
		[HL].bit	2	2	–	(HL).bit ← 1			
		ES:!addr16.bit	5	3	–	(ES, addr16).bit ← 1			
		ES:[HL].bit	3	3	–	(ES, HL).bit ← 1			
	CLR1	saddr.bit	3	2	–	(saddr.bit) ← 0			
		sfr.bit	3	2	–	sfr.bit ← 0			
		A.bit	2	1	–	A.bit ← 0			
		!addr16.bit	4	2	–	(addr16).bit ← 0			
		PSW.bit	3	4	–	PSW.bit ← 0	×	×	×
		[HL].bit	2	2	–	(HL).bit ← 0			
		ES:!addr16.bit	5	3	–	(ES, addr16).bit ← 0			
		ES:[HL].bit	3	3	–	(ES, HL).bit ← 0			
	SET1	CY	2	1	–	CY ← 1			1
	CLR1	CY	2	1	–	CY ← 0			0
	NOT1	CY	2	1	–	CY ← $\overline{CY}$			×

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (15/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Call/ return	CALL	rp	2	3	–	(SP – 2) ← (PC + 2)S, (SP – 3) ← (PC + 2)H, (SP – 4) ← (PC + 2)L, PC ← CS, rp, SP ← SP – 4			
		$!addr20	3	3	–	(SP – 2) ← (PC + 3)S, (SP – 3) ← (PC + 3)H, (SP – 4) ← (PC + 3)L, PC ← PC + 3 + jdisp16, SP ← SP – 4			
		!addr16	3	3	–	(SP – 2) ← (PC + 3)S, (SP – 3) ← (PC + 3)H, (SP – 4) ← (PC + 3)L, PC ← 0000, addr16, SP ← SP – 4			
		!!addr20	4	3	–	(SP – 2) ← (PC + 4)S, (SP – 3) ← (PC + 4)H, (SP – 4) ← (PC + 4)L, PC ← addr20, SP ← SP – 4			
	CALLT	[addr5]	2	5	–	(SP – 2) ← (PC + 2)S, (SP – 3) ← (PC + 2)H, (SP – 4) ← (PC + 2)L , PCS ← 0000, PCH ← (0000, addr5 + 1), PCL ← (0000, addr5), SP ← SP – 4			
	BRK	–	2	5	–	(SP – 1) ← PSW, (SP – 2) ← (PC + 2)S, (SP – 3) ← (PC + 2)H, (SP – 4) ← (PC + 2)L, PCS ← 0000, PCH ← (0007FH), PCL ← (0007EH), SP ← SP – 4, IE ← 0			
	RET	–	1	6	–	PCL ← (SP), PCH ← (SP + 1), PCS ← (SP + 2), SP ← SP + 4			
	RETI	–	2	6	–	PCL ← (SP), PCH ← (SP + 1), PCS ← (SP + 2), PSW ← (SP + 3), SP ← SP + 4	R	R	R
	RETB	–	2	6	–	PCL ← (SP), PCH ← (SP + 1), PCS ← (SP + 2), PSW ← (SP + 3), SP ← SP + 4	R	R	R

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (16/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Stack manipulate	PUSH	PSW	2	1	–	(SP – 1) ← PSW, (SP – 2) ← 00H, SP ← SP – 2			
		rp	1	1	–	(SP – 1) ← rp_H, (SP – 2)← rp_L, SP ← SP – 2			
	POP	PSW	2	3	–	PSW ← (SP + 1), SP ← SP + 2	R	R	R
		rp	1	1	–	rp_L ← (SP), rp_H ← (SP + 1), SP ← SP + 2			
	MOVW	SP, #word	4	1	–	SP ← word			
		SP, AX	2	1	–	SP ← AX			
		AX, SP	2	1	–	AX ← SP			
		HL, SP	3	1	–	HL ← SP			
		BC, SP	3	1	–	BC ← SP			
		DE, SP	3	1	–	DE ← SP			
	ADDW	SP, #byte	2	1	–	SP ← SP + byte			
	SUBW	SP, #byte	2	1	–	SP ← SP – byte			
Unconditional branch	BR	AX	2	3	–	PC ← CS, AX			
		$addr20	2	3	–	PC ← PC + 2 + jdisp8			
		$!addr20	3	3	–	PC ← PC + 3 + jdisp16			
		!addr16	3	3	–	PC ← 0000, addr16			
		!!addr20	4	3	–	PC ← addr20			
Conditional branch	BC	$addr20	2	2/4[Note 3]	–	PC ← PC + 2 + jdisp8 if CY = 1			
	BNC	$addr20	2	2/4[Note 3]	–	PC ← PC + 2 + jdisp8 if CY = 0			
	BZ	$addr20	2	2/4[Note 3]	–	PC ← PC + 2 + jdisp8 if Z = 1			
	BNZ	$addr20	2	2/4[Note 3]	–	PC ← PC + 2 + jdisp8 if Z = 0			
	BH	$addr20	3	2/4[Note 3]	–	PC ← PC+3+jdisp8 if (Z ∨ CY)=0			
	BNH	$addr20	3	2/4[Note 3]	–	PC ← PC+3+jdisp8 if (Z ∨ CY)=1			
	BT	saddr.bit, $addr20	4	3/5[Note 3]	–	PC ← PC + 4 + jdisp8 if (saddr).bit = 1			
		sfr.bit, $addr20	4	3/5[Note 3]	–	PC ← PC + 4 + jdisp8 if sfr.bit = 1			
		A.bit, $addr20	3	3/5[Note 3]	–	PC ← PC + 3 + jdisp8 if A.bit = 1			
		PSW.bit, $addr20	4	3/5[Note 3]	–	PC ← PC + 4 + jdisp8 if PSW.bit = 1			
		[HL].bit, $addr20	3	3/5[Note 3]	6/7	PC ← PC + 3 + jdisp8 if (HL).bit = 1			
		ES:[HL].bit, $addr20	4	4/6[Note 3]	7/8	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 1			

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. This indicates the number of clocks “when condition is not met/when condition is met”.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Table 29-5. Operation List (17/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Conditional branch	BF	saddr.bit, $addr20	4	3/5[Note 3]	–	PC ← PC + 4 + jdisp8 if (saddr).bit = 0			
		sfr.bit, $addr20	4	3/5[Note 3]	–	PC ← PC + 4 + jdisp8 if sfr.bit = 0			
		A.bit, $addr20	3	3/5[Note 3]	–	PC ← PC + 3 + jdisp8 if A.bit = 0			
		PSW.bit, $addr20	4	3/5[Note 3]	–	PC ← PC + 4 + jdisp8 if PSW.bit = 0			
		[HL].bit, $addr20	3	3/5[Note 3]	6/7	PC ← PC + 3 + jdisp8 if (HL).bit = 0			
		ES:[HL].bit, $addr20	4	4/6[Note 3]	7/8	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 0			
	BTCLR	saddr.bit, $addr20	4	3/5[Note 3]	–	PC ← PC + 4 + jdisp8 if (saddr).bit = 1 then reset (saddr).bit			
		sfr.bit, $addr20	4	3/5[Note 3]	–	PC ← PC + 4 + jdisp8 if sfr.bit = 1 then reset sfr.bit			
		A.bit, $addr20	3	3/5[Note 3]	–	PC ← PC + 3 + jdisp8 if A.bit = 1 then reset A.bit			
		PSW.bit, $addr20	4	3/5[Note 3]	–	PC ← PC + 4 + jdisp8 if PSW.bit = 1 then reset PSW.bit	×	×	×
		[HL].bit, $addr20	3	3/5[Note 3]	–	PC ← PC + 3 + jdisp8 if (HL).bit = 1 then reset (HL).bit			
		ES:[HL].bit, $addr20	4	4/6[Note 3]	–	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 1 then reset (ES, HL).bit			
Conditional skip	SKC	–	2	1	–	Next instruction skip if CY = 1			
	SKNC	–	2	1	–	Next instruction skip if CY = 0			
	SKZ	–	2	1	–	Next instruction skip if Z = 1			
	SKNZ	–	2	1	–	Next instruction skip if Z = 0			
	SKH	–	2	1	–	Next instruction skip if (Z ∨ CY) = 0			
	SKNH	–	2	1	–	Next instruction skip if (Z ∨ CY) = 1			
CPU control	SEL	RBn	2	1	–	RBS[1:0] ← n			
	NOP	–	1	1	–	No Operation			
	EI	–	3	4	–	IE ← 1(Enable Interrupt)			
	DI	–	3	4	–	IE ← 0(Disable Interrupt)			
	HALT	–	2	3	–	Set HALT Mode			
	STOP	–	2	3	–	Set STOP Mode			

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. This indicates the number of clocks “when condition is not met/when condition is met”.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

3. n indicates the number of register banks (n = 0 to 3)

CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

Cautions 1. The 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted are as follows according to product.

30.1 Pins Mounted According to Product

30.1.1 Port functions

Port	78K0R/KC3-L			78K0R/KD3-L	78K0R/KE3-L
	40-pin	44-pin	48-pin	52-pin	64-pin
Port 0	–	–	–	P00, P01	
Port 1	P10 to P13				P10 to P17
Port 2	P20 to P27				
Port 3	P30 to P32				P30 to P33
Port 4	P40, P41				P40 to P43
Port 5	P50, P51	P50 to P52			P50 to P53
Port 6	–		P60, P61		
Port 7	P70 to P75			P70 to P77	
Port 8	P80, P81, P83	P80 to P83			
Port 12	P120 to P122	P120 to P124			
Port 14	–		P140		P140, P141
Port 15	P150, P151		P150 to P152		P150 to P153

30.1.2 Non-port functions

Function Name		78K0R/KC3-L			78K0R/KD3-L	78K0R/KE3-L
		40-pin	44-pin	48-pin	52-pin	64-pin
Power supply, ground		V_{DD}, AV_{REF}, V_{SS}, AV_{SS}				V_{DD}, EV_{DD}, AV_{REF}, V_{SS}, EV_{SS}, AV_{SS}
Regulator		REGC				
Reset		$\overline{\text{RESET}}$				
Clock oscillation		X1, X2, EXCLK	X1, X2, XT1, XT2, EXCLK			
Writing to flash memory		FLMD0				
Interrupt		INTP0 to INTP6	INTP0 to INTP7			
Timer		TI02 to TI07, TO02-TO07	SLTI, SLTO, TI02 to TI07, TO02 to TO07		SLTI, SLTO, TI00, TI02 to TI07, TO00, TO02 to TO07	
Real time counter		–	RTCDIV, RTCCL, RTC1HZ			
Comparator		CMP0M, CMP0P, CMP1M	CMP0M, CMP0P, CMP1M, CMP1P			
Programmable gain amplifier		PGAI				
Serial interface	UART0	RxD0, TxD0				
	UART1	RxD1, TxD1				
	CSI00	SCK00, SI00, SO00				
	CSI01	SCK01, SI01, SO01				
	CSI10	SCK10, SI10, SO10				
	IIC10	SCL10, SDA10				
	IICA	–		SCL0, SDA0		
A/D converter		ANI0 to ANI9		ANI0 to ANI10		ANI0 to ANI11
Clock Output/Buzzer Output		–		PCLBUZ0		PCLBUZ0, PCLBUZ1
Key Interrupt		KR0 to KR5			KR0 to KR7	
Low-voltage detector (LVI)		EXLVI				
On-chip debug function		TOOL0, TOOL1				

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.2 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	EV_{DD}		−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	EV_{SS}		−0.5 to +0.3	V
	AV_{REF}		−0.5 to V_{DD} + 0.3 Note 1	V
	AV_{SS}		−0.5 to + 0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to + 3.6 and −0.3 to V_{DD} + 0.3 Note 2	V
Input voltage	V_{I1}	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P70 to P77, P120 to P124, P141, EXCLK, $\overline{\text{RESET}}$, FLMD0	−0.3 to EV_{DD} + 0.3 and −0.3 to V_{DD} + 0.3 Note 1	V
	V_{I2}	P60, P61 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	P20 to P27, P80 to P83, P150 to P153	−0.3 to AV_{REF} + 0.3 and −0.3 to V_{DD} + 0.3 Note 1	V
Output voltage	V_{O1}	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P60, P61, P70 to P77, P120, P140, P141	−0.3 to EV_{DD} + 0.3 Note 1	V
	V_{O2}	P20 to P27, P80 to P83, P150 to P153	−0.3 to AV_{REF} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI11, PGAI, CMP0M, CMP0P, CMP1M, CMP1P	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V

Notes 1. Must be 6.5 V or lower.

2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P70 to P77, P120, P140, P141	−10	mA
		Total of all pins −80 mA	P00, P01, P40 to P43, P120, P140, P141	−25	mA
			P10 to P17, P30 to P33, P50 to P53, P70 to P77	−55	mA
	I_{OH2}	Per pin	P20 to P27, P80 to P83, P150 to P153	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P60, P61, P70 to P77, P120, P140, P141	30	mA
		Total of all pins 200 mA	P00, P01, P40 to P43, P120, P140, P141	60	mA
			P10 to P17, P30 to P33, P50 to P53, P60, P61, P70 to P77	140	mA
	I_{OL2}	Per pin	P20 to P27, P80 to P83, P150 to P153	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

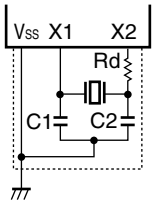
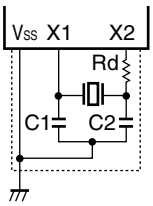
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.3 Oscillator Characteristics

30.3.1 Main system clock oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	2.0		5.0	
Crystal resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	2.0		5.0	

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.3.2 Internal oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

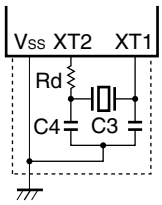
Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
Internal high-speed oscillation clock frequency Note	f_{IH1M}	Low consumption current mode		0.87	1	1.13	MHz
	f_{IH8M}	2.7 V ≤ V_{DD} ≤ 5.5 V, T_A = –40 to +85°C		7.856	8	8.144	MHz
		1.8 V ≤ V_{DD} < 2.7 V, T_A = –20 to +70°C		7.848	8	8.152	MHz
		1.8 V ≤ V_{DD} < 2.7 V, T_A = –40 to +85°C		7.84	8	8.16	MHz
	f_{IH20M}	2.7 V ≤ V_{DD} ≤ 5.5 V		19.52	20	20.48	MHz
Internal low-speed oscillation clock frequency	f_{IL}	Normal current mode	2.7 V ≤ V_{DD} ≤ 5.5 V	27	30	33	kHz
			1.8 V ≤ V_{DD} < 2.7 V	25.5	30	34.5	kHz
		Low consumption current mode		25.5	30	34.5	kHz

Note This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Remark For details on the normal current mode and low consumption current mode according to the regulator output voltage, refer to **CHAPTER 24 REGULATOR**.

30.3.3 Sub system clock oscillator characteristics Note 1

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Items	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT}) Note 2		32	32.768	35	kHz

Notes 1. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

2. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

30.3.4 Recommended oscillator circuit constants

(1) X1 oscillation: Ceramic resonator (AMPH = 0, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
Murata Manufacturing Co., Ltd..	CSTCC2M00G56-R0	SMD	2.0	Internal (47)	Internal (47)	0	1.8	5.5
	CSTCR4M00G55-R0	SMD	4.0	Internal (39)	Internal (39)	0		
	CSTLS4M00G56-B0	Lead		Internal (47)	Internal (47)	0		
	CSTLS4M19G56-B0	Lead	4.194	Internal (47)	Internal (47)	0		
	CSTCR4M19G55-R0	SMD		Internal (39)	Internal (39)	0		
	CSTCR4M91G55-R0	SMD	4.915	Internal (39)	Internal (39)	0		
	CSTLS4M91G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCR5M00G55-R0	SMD	5.0	Internal (39)	Internal (39)	0		
	CSTLS5M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCR6M00G53-R0	SMD	6.0	Internal (15)	Internal (15)	0		
	CSTLS6M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE8M00G52-R0	SMD	8.0	Internal (10)	Internal (10)	0		
	CSTLS8M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE8M38G52-R0	SMD	8.388	Internal (10)	Internal (10)	0		
	CSTLS8M38G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE10M0G52-R0	SMD	10.0	Internal (10)	Internal (10)	0		
	CSTLS10M0G53-B0	Lead		Internal (15)	Internal (15)	0		
TDK Corporation	CCR4.0MUC8	SMD	4.0	Internal (27)	Internal (27)	0	1.8	5.5
	CCR4.19MUC8	SMD	4.19	Internal (27)	Internal (27)	0		
	CCR4.91MUC8	SMD	4.91	Internal (27)	Internal (27)	0		
	CCR5.0MUC8	SMD	5.0	Internal (27)	Internal (27)	0		
	CCR6.0MUC8	SMD	6.0	Internal (27)	Internal (27)	0		
	CCR8.0MXC8	SMD	8.0	Internal (18)	Internal (18)	0		
	CCR8.38MXC8	SMD	8.38	Internal (18)	Internal (18)	0		
	CCR10.0MXC8	SMD	10.0	Internal (18)	Internal (18)	0		

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(2) X1 oscillation: Crystal resonator (AMPH = 0, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
KYOCERA KINSEKI Corporation	HC49SFNB	Lead	4.0	8	8	3.3	1.8	5.5
	HC49SFNB	Lead	4.9152	18	18	0		
	HC49SFNB	Lead	6.0	18	18	0		
	HC49SFNB	Lead	8.0	10	10	0		
	HC49SFNB	Lead	8.38	10	10	0		

(3) X1 oscillation: Ceramic resonator (AMPH = 1, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
Murata Manufacturing Co., Ltd..	CSTCE12M0G52-R0	SMD	12.0	Internal (10)	Internal (10)	0	1.8	5.5
	CSTCE16M0V51-R0	SMD	16.0	Internal (5)	Internal (5)	0		
	CSTCE20M0V51-R0	SMD	20.0	Internal (5)	Internal (5)	0	2.0	

(4) X1 oscillation: Crystal resonator (AMPH = 1, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
KYOCERA KINSEKI Corporation	HC49SFNB	Lead	12.0	10	10	0	1.8	5.5
	HS49SFNB	Lead	16.0	8	8	0		
	HS49SFNB	Lead	20.0	5	5	0		

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(5) XT1 oscillation: Crystal resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Load Capacitance CL (pF)	XT1 osclllator oscillation mode [Note 1]	Recommended Circuit Constants			Oscillation Voltage Range	
						C3 (pF)	C4 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
Seiko Instruments Inc. [Note 2]	SSP-T7-F	SMD	32.768	9.0	Normal oscillation	15	15	0	1.8	5.5
				7.0		10	10	0		
	SSP-T7-FL			6.0	Low power consumption oscillation	9	8	0		
				6.0	Ultra-low power consumption oscillation	9	8	0		
				4.4		5	5	0		
				3.7		4	3	0		
	VT-200-F	Lead		12.5	Normal oscillation	20	20	0		
				8.7		15	13	0		
	VT-200-FL			6.0	Low power consumption oscillation	9	8	0		
				6.0	Ultra-low power consumption oscillation	9	8	0		
				4.4		5	5	0		
				3.7		4	3	0		
EPSON TOYOCOM CORPORATION [Note 3]	MC-146	SMD	32.768	7.0	Normal oscillation	12	10	0	1.8	5.5
				–	Low power consumption oscillation	12	10	0		

Notes 1. Set the XT1 oscillation mode by using bits AMPHS1 and AMPHS0 of the clock operation mode control register (CMC).

2. Contact Seiko Instruments Inc. (http://www.sii-crystal.com) when using this resonator.

3. Contact EPSON TOYOCOM CORPORATION. (http://www.epsontoyocom.co.jp/english/index.html) when using this resonator.

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L so that the internal operation conditions are within the specifications of the DC and AC characteristics.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.4 DC Characteristics

30.4.1 Pin characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P70 to P77, P120, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V			–3.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–1.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–1.0	mA
		Total of P00, P01, P40 to P43, P120, P140, P141 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			–20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total of P10 to P17, P30 to P33, P50 to P53, P70 to P77 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			–30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–19.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–10.0	mA
		Total of all pins (When duty = 60%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			–50.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–29.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–15.0	mA
	I_{OH2}	Per pin for P20 to P27, P80 to P83, P150 to P153	AV_{REF} = V_{DD}			–0.1	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD} pin to an output pin.

2. Specification under conditions where the duty factor is 60% or 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
• Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 50% and I_{OH} = –20.0 mA
Total output current of pins = (–20.0 × 0.7)/(50 × 0.01) = –28.0 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P30 to P32, P70, P72, P73, and P75 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00, P01, P10 to P17, P30, P33, P40 to P43, P50 to P53, P70 to P77, P120, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.5	mA
		Per pin for P31, P32	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.6	mA
		Per pin for P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			3.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Total of P00, P01, P40 to P43, P120, P140, P141 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P10 to P17, P30 to P33, P50 to P53, P60, P61, P70 to P77 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			45.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty = 60%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			65.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			40.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			29.0	mA
	I_{OL2}	Per pin for P20 to P27, P80 to P83, P150 to P153	AV_{REF} = V_{DD}			0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS}, V_{SS}, and AV_{SS} pins.

2. Specification under conditions where the duty factor is 60% or 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
• Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)
<Example> Where n = 50% and I_{OL} = 20.0 mA
Total output current of pins = (20.0 × 0.7)/(50 × 0.01) = 28.0 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P01, P30, P33, P42, P43, P53, P123, P124, P141		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P10 to P17, P31, P32, P40, P41, P50 to P52, P70 to P77, P120 to P122, EXCLK, $\overline{\text{RESET}}$	Normal input buffer	0.8V_{DD}		V_{DD}	V
	V_{IH3}	P31, P32, P71, P72, P74, P75	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 2.7 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 1.8 V ≤ V_{DD} < 2.7 V	1.6		V_{DD}	V
	V_{IH4}	P20 to P27, P81, P83, P150 to P153	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH5}	P80, P82	AV_{REF} = V_{DD}	0.8AV_{REF}		AV_{REF}	V
	V_{IH6}	P60, P61		0.7V_{DD}		6.0	V
	V_{IH7}	FLMD0		0.9V_{DD} Note		V_{DD}	V

Note Must be 0.9V_{DD} or higher when used in the flash memory programming mode.

Caution The maximum value of V_{IH} of pins P30 to P32, P70, P72, P73, and P75 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	P01, P30, P33, P42, P43, P53, P123, P124, P141		0		0.3V_{DD}	V
	V_{IL2}	P00, P10 to P17, P31, P32, P40, P41, P50 to P52, P70 to P77, P120 to P122, EXCLK, $\overline{\text{RESET}}$	Normal input buffer	0		0.2V_{DD}	V
	V_{IL3}	P31, P32, P71, P72, P74, P75	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 2.7 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.8 V ≤ V_{DD} < 2.7 V	0		0.2	V
	V_{IL4}	P20 to P27, P81, P83, P150 to P153	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
	V_{IL5}	P80, P82	AV_{REF} = V_{DD}	0		0.2AV_{REF}	V
	V_{IL6}	P60, P61		0		0.3V_{DD}	V
	V_{IL7}	FLMD0 Note		0		0.1V_{DD}	V

Note When disabling writing of the flash memory, connect the FLMD0 pin processing directly to V_{SS}, and maintain a voltage less than 0.1V_{DD}.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P70 to P77, P120, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.0 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27, P80 to P83, P150 to P153	AV_{REF} = V_{DD}, I_{OH2} = –0.1 mA	AV_{REF} – 0.5			V
Output voltage, low	V_{OL1}	P00, P01, P10 to P17, P30, P33, P40 to P43, P50 to P53, P70 to P77, P120, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.0 mA			0.5	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.5 mA			0.4	V
		P31, P32	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.5	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P27, P80 to P83, P150 to P153	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 2.0 mA			0.4	V

Caution P30 to P32, P70, P72, P73, and P75 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P60, P61, P70 to P77, P120, P141, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P20 to P27, P80 to P83, P150 to P153	$V_I = AV_{REF}$, $AV_{REF} = V_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{DD}$	In input port			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P60, P61, P70 to P77, P120, P141, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL2}	P20 to P27, P80 to P83, P150 to P153	$V_I = V_{SS}$, $AV_{REF} = V_{DD}$				–1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{SS}$	In input port			–1	μA
				In resonator connection			–10	μA

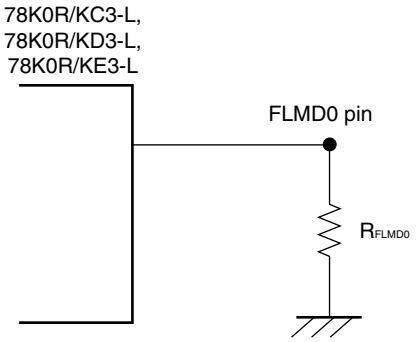
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
On-chip pull-up resistance	R_U	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P70 to P77, P120, P141	V_I = V_{SS}, In input port	10	20	100	kΩ
FLMD0 pin external pull-down resistance[Note]	R_{FLMD0}	When enabling the self-programming mode setting with software		100			kΩ

Note It is recommended to leave the FLMD0 pin open. If the pin is required to be pulled down externally, set R_{FLMD0} to 100 kΩ or more.



Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.4.2 Supply current characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Square wave input		5.0	7.1	mA
				Resonator connection		5.3	7.4	mA
			f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Square wave input		5.0	7.1	mA
				Resonator connection		5.3	7.4	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 5.0 V	Square wave input		2.9	4.2	mA
				Resonator connection		3.0	4.3	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		2.9	4.2	mA
				Resonator connection		3.0	4.3	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		1.6	2.5	mA
				Resonator connection		1.7	2.6	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 2.0 V	Square wave input		1.2	2.1	mA
				Resonator connection		1.2	2.1	mA
			f_{IH20} = 20 MHz Note 4	V_{DD} = 5.0 V		5.3	7.4	mA
				V_{DD} = 3.0 V		5.3	7.4	mA
			f_{IH} = 8 MHz Note 4	V_{DD} = 5.0 V		2.4	3.5	mA
				V_{DD} = 3.0 V		2.4	3.5	mA
<R>			f_{IH} = 1 MHz Note 4, 5	V_{DD} = 3.0 V		180	346	μA
			f_{SUB} = 32.768 kHz Note 6, T_A = –40 to +50°C	V_{DD} = 5.0 V		3.7	7.5	μA
				V_{DD} = 3.0 V		3.7	7.5	μA
				V_{DD} = 2.0 V		3.7	7.5	μA
			f_{SUB} = 32.768 kHz Note 6, T_A = –40 to +70°C	V_{DD} = 5.0 V		3.7	9.4	μA
				V_{DD} = 3.0 V		3.7	9.4	μA
				V_{DD} = 2.0 V		3.7	9.4	μA
			f_{SUB} = 32.768 kHz Note 6, T_A = –40 to +85°C	V_{DD} = 5.0 V		3.7	11.7	μA
				V_{DD} = 3.0 V		3.7	11.7	μA
				V_{DD} = 2.0 V		3.7	11.7	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, programmable gain amplifier, comparator, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. When internal high-speed oscillation, 20 MHz internal high-speed oscillation, and subsystem clock are stopped.

3. When AMPH (bit 0 of clock operation mode control register (CMC)) = 0, FLPC and FSEL (bits 1 and 0 of operation speed mode control register (OSMC)) = 0 and 0.

4. When high-speed system clock and subsystem clock are stopped.

5. When low consumption current mode is set (RMC = 5AH, OSMC = 02H).

6. When operating real-time counter (RTC) and setting ultra-low current consumption (AMPHS1 (bit2 of CMC register) = 1, OSMC = 82H). When internal high-speed oscillation, 20 MHz internal high-speed oscillation, and high-speed system clock are stopped. When watchdog timer is stopped.

(**Remarks** are given on the next page.)

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH20}: 20 MHz internal high-speed oscillation clock frequency

3. f_{IH}: Internal high-speed oscillation clock frequency

4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

5. RMC: Regulator mode control register (RMC)

6. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
<R> Supply current	I_{DD2} Note 1	HALT mode	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Square wave input		0.9	3.2	mA
				Resonator connection		1.2	3.5	mA
			f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Square wave input		0.9	3.2	mA
				Resonator connection		1.2	3.5	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 5.0 V	Square wave input		0.5	2.0	mA
				Resonator connection		0.6	2.1	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		0.5	2.0	mA
				Resonator connection		0.6	2.1	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		0.35	1.7	mA
				Resonator connection		0.40	1.7	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 2.0 V	Square wave input		0.21	1.2	mA
				Resonator connection		0.26	1.3	mA
			f_{IH20} = 20 MHz Note 4	V_{DD} = 5.0 V		1.2	3.5	mA
				V_{DD} = 3.0 V		1.2	3.5	mA
			f_{IH} = 8 MHz Note 4	V_{DD} = 5.0 V		0.41	1.6	mA
				V_{DD} = 3.0 V		0.41	1.6	mA
			f_{IH} = 1 MHz Note 4, 5	V_{DD} = 3.0 V		45	148	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value includes the peripheral operation current. However, not including the current flowing into the A/D converter, programmable gain amplifier, comparator, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. During HALT instruction execution by flash memory.

2. When internal high-speed oscillation, 20 MHz internal high-speed oscillation, and subsystem clock are stopped.

3. When AMPH (bit 0 of clock operation mode control register (CMC)) = 0, FLPC and FSEL (bits 1 and 0 of operation speed mode control register (OSMC)) = 0 and 0.

4. When high-speed system clock and subsystem clock are stopped.

5. When low consumption current mode is set (RMC = 5AH, OSMC = 02H).

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH20}: 20 MHz internal high-speed oscillation clock frequency

3. f_{IH}: Internal high-speed oscillation clock frequency

4. RMC: Regulator mode control register (RMC)

5. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD2} Note 1	HALT mode	f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +50°C	V_{DD} = 5.0 V		0.9	2.9	μA
				V_{DD} = 3.0 V		0.9	2.9	μA
				V_{DD} = 2.0 V		0.9	2.9	μA
			f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +70°C	V_{DD} = 5.0 V		0.9	4.8	μA
				V_{DD} = 3.0 V		0.9	4.8	μA
				V_{DD} = 2.0 V		0.9	4.8	μA
			f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +85°C	V_{DD} = 5.0 V		0.9	7.1	μA
				V_{DD} = 3.0 V		0.9	7.1	μA
				V_{DD} = 2.0 V		0.9	7.1	μA
	I_{DD3} Note 3	STOP mode	T_A = –40 to +50°C			0.33	2.1	μA
			T_A = –40 to +70°C			0.33	4	μA
			T_A = –40 to +85°C			0.33	6.2	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value includes the peripheral operation current. However, not including the current flowing into the A/D converter, programmable gain amplifier, comparator, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. During HALT instruction execution in flash memory.

2. When operating real-time counter (RTC) and setting ultra-low current consumption (AMPHS1 (bit2 of CMC register) = 1, OSMC = 82H).When internal high-speed oscillation, 20 MHz internal high-speed oscillation, and high-speed system clock are stopped. When watchdog timer is stopped. When RTCLPC = 1 (stops supply of subsystem clock to peripheral functions other than real-time counter). When output function of RTC is stopped.

3. Total current flowing into V_{DD}, EV_{DD}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value includes the peripheral operation current. However, not including the current flowing into the A/D converter, programmable gain amplifier, comparator, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. When subsystem clock is stopped. When watchdog timer is stopped.

Remarks 1. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

2. RTCLPC: bit 7 of the operation speed mode control register (OSMC)

3. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Real-time counter operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz		V_{DD} = 3.0 V		0.2	1.0	μA
				V_{DD} = 2.0 V		0.2	1.0	μA
Watchdog timer operating current	I_{WDT} Notes 2, 3	f_{IL} = 30 kHz				0.31	0.35	μA
A/D converter operating current	I_{ADC} Note 4	During conversion at maximum speed	High speed mode 1	AV_{REF} = V_{DD} = 5.0 V		1.72	3.2	mA
			High speed mode 2	AV_{REF} = V_{DD} = 3.0 V		0.72	1.6	mA
			Normal mode	AV_{REF} = V_{DD} = 5.0 V		0.86	1.9	mA
			Low voltage mode	AV_{REF} = V_{DD} = 3.0 V		0.37	0.8	mA
Programmable gain amplifier operating current	I_{AMP} Note 5					0.56	1.2	mA
Comparator operating current	I_{CMP} Note 6	Per channel when the internal reference voltage is not used		AV_{REF} = V_{DD} = 5.0 V		120	240	μA
				AV_{REF} = V_{DD} = 3.0 V			120	μA
		Per channel when the internal reference voltage is used		AV_{REF} = V_{DD} = 5.0 V		160	300	μA
				AV_{REF} = V_{DD} = 3.0 V			150	μA
LVI operating current	I_{LVI} Note 7					9	18	μA

Notes 1. Current flowing only to the real-time counter (excluding the operating current of the XT1 oscillator). The TYP. value of the current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of the TYP. values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time counter operates in operation mode or HALT mode. The I_{DD1} and I_{DD2} MAX. values also include the real-time counter operating current. When the real-time counter operates during f_{CLK} = f_{SUB}/2, the TYP. value of I_{DD2} includes the real-time counter operating current.

2. When internal high-speed oscillation, 20 MHz internal high-speed oscillation, and high-speed system clock are stopped.

3. Current flowing only to the watchdog timer (including the operating current of the 30 kHz internal oscillator). The current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when f_{CLK} = f_{SUB}/2 when the watchdog timer operates in STOP mode.

4. Current flowing only to the A/D converter (AV_{REF} pin). The current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing only to the programmable gain amplifier (AV_{REF} pin). The current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of I_{DD1} or I_{DD2} and I_{AMP} when the programmable gain amplifier operates in an operation mode or the HALT mode.

6. Current flowing only to the comparator (AV_{REF} pin). The current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of I_{DD1} or I_{DD2} and I_{CMP} when the comparator operates in an operation mode or the HALT mode.

7. Current flowing only to the LVI circuit. The current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates in the Operating, HALT or STOP mode.

Remarks 1. f_{IL}: Internal low-speed oscillation clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.5 AC Characteristics

30.5.1 Basic operation

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	Normal current mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		8	μs
				1.8 V ≤ V_{DD} < 2.7 V	0.2		8	μs
			Low consumption current mode		1		8	μs
		Subsystem clock (f_{SUB}) operation[Note]			57.2	61	62.5	μs
		In the self programming mode	Normal current mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		1	μs
				1.8 V ≤ V_{DD} < 2.7 V	0.2		1	μs
			Low consumption current mode			1		μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			2.0		20.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V			2.0		5.0	MHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		1.8 V ≤ V_{DD} < 2.7 V			96			ns
TI00, TI02 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns
TO00, TO02 to TO07 output frequency	f_{TO}	2.7 V ≤ V_{DD} ≤ 5.5 V					10	MHz
		1.8 V ≤ V_{DD} < 2.7 V					5	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	2.7 V ≤ V_{DD} ≤ 5.5 V					10	MHz
		1.8 V ≤ V_{DD} < 2.7 V					5	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}				1			μs
Key interrupt input low-level width	t_{KR}				250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

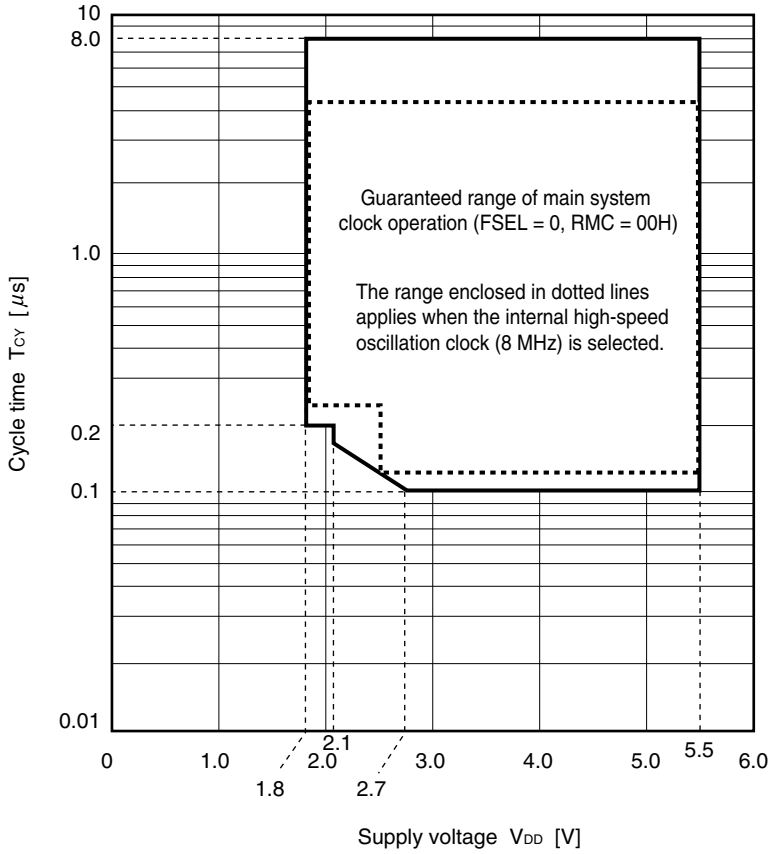
Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Remarks 1. f_{MCK}: Operation clock frequency of timer array unit
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

2. For details on the normal current mode and low consumption current mode according to the regulator output voltage, refer to **CHAPTER 24 REGULATOR**.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

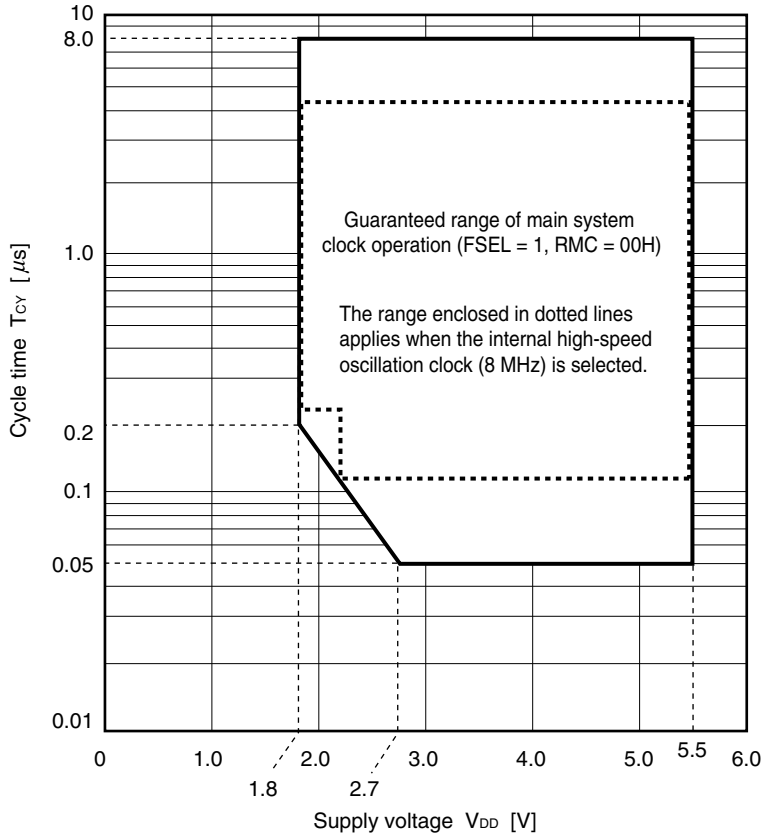
Minimum instruction execution time during main system clock operation (FSEL = 0, RMC = 00H)



Remark FSEL: Bit 0 of the operation speed mode control register (OSMC)
RMC: Regulator mode control register (RMC)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Minimum instruction execution time during main system clock operation (FSEL = 1, RMC = 00H)

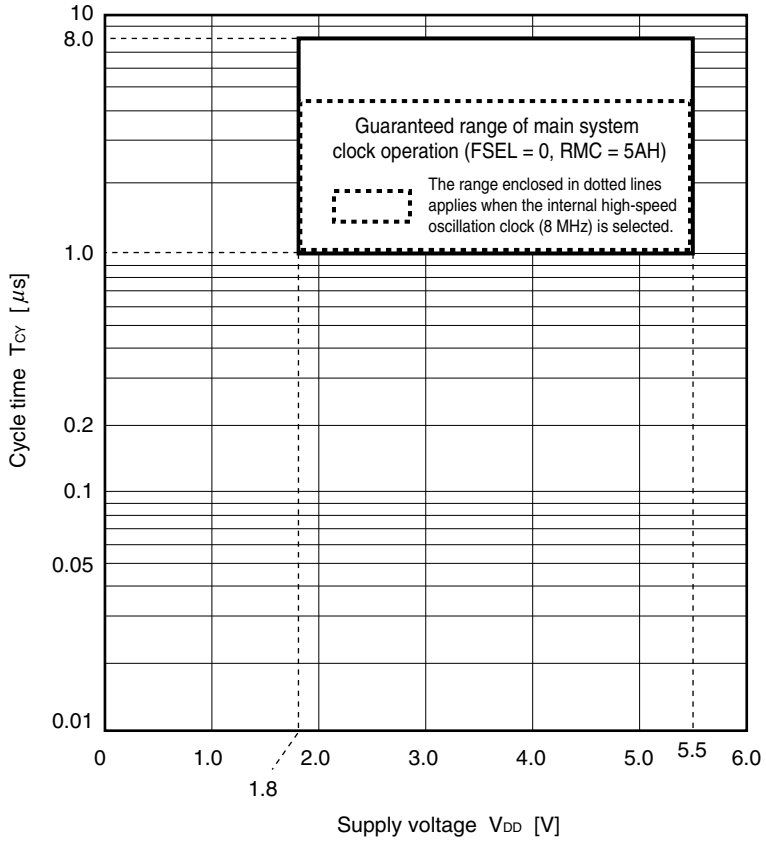


Caution When V_{DD} < 2.25 V and FSEL = 1, It is prohibited to release STOP mode during f_{EX} operation or f_{IH} operation (This must not be performed even if the frequency is divided. The STOP mode may be released during fx operation.).

Remark FSEL: Bit 0 of the operation speed mode control register (OSMC)
RMC: Regulator mode control register (RMC)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Minimum instruction execution time during main system clock operation (FSEL = 0, RMC = 5AH)

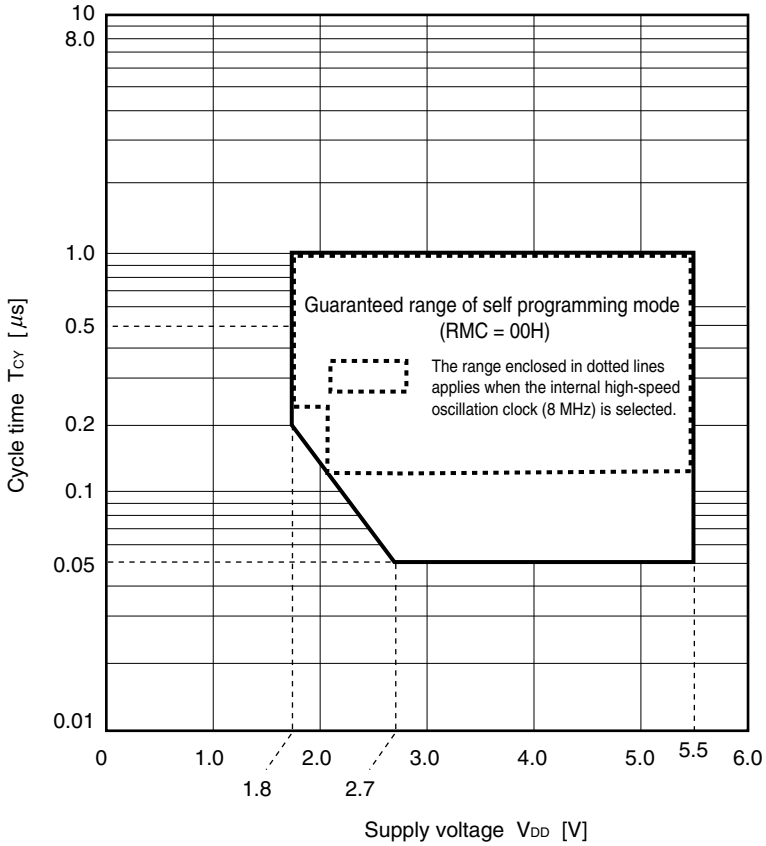


Remarks 1. FSEL: Bit 0 of the operation speed mode control register (OSMC)
RMC: Regulator mode control register

2. The entire voltage range is 1 MHz (MAX.) when RMC is set to 5AH.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Minimum instruction execution time during self programming mode (RMC = 00H)



Remarks 1. RMC: Regulator mode control register (RMC)

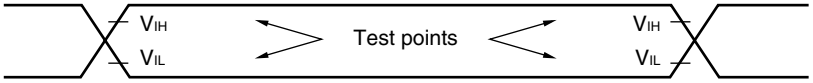
2. The self programming function cannot be used when the CPU operates with the subsystem clock.

3. The entire voltage range is 1 MHz when RMC is set to 5AH.

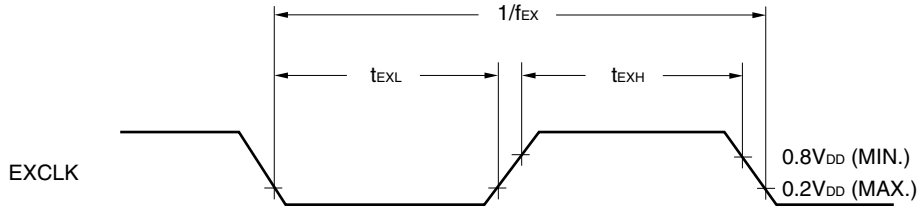
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.5.2 Measurement conditions

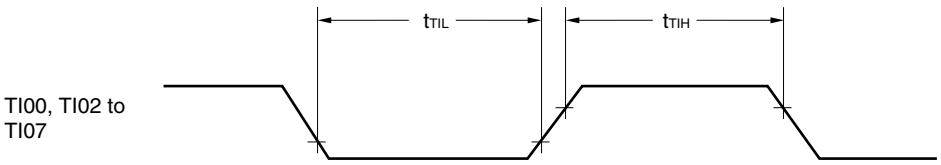
AC Timing Test Points



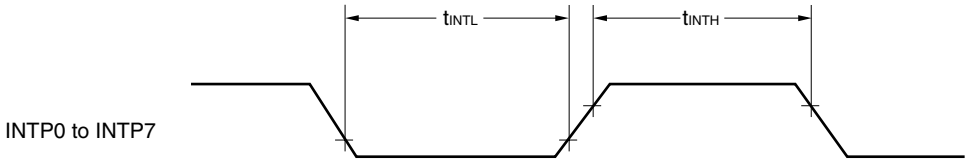
External Main System Clock Timing



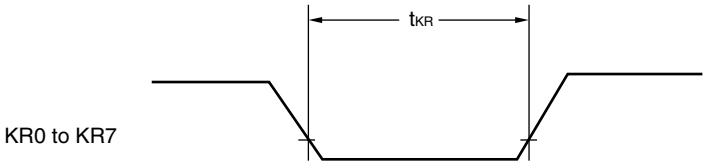
TI Timing



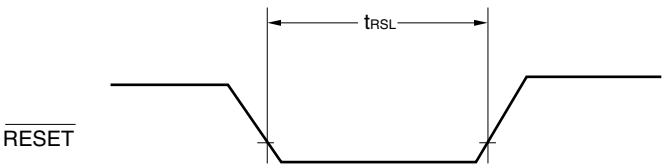
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.6 Peripheral Functions Characteristics

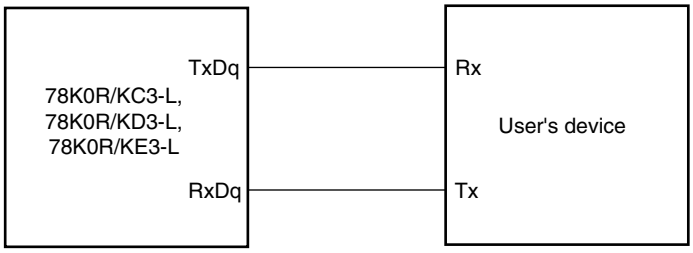
30.6.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

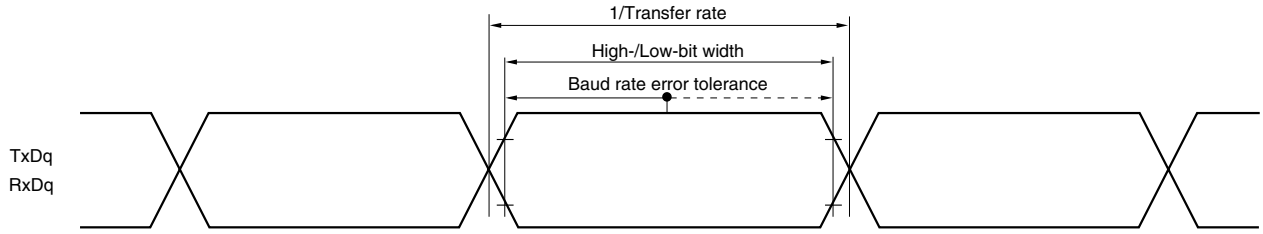
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		1.8 V ≤ V_{DD} ≤ 5.5 V			f_{MCK}/6	bps
		f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}, 2.7 V ≤ V_{DD} ≤ 5.5 V			3.3	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0, 1) , g: PIM and POM number (g = 3, 7)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of serial mode register 0n (SMR0n). n: Channel number (n = 0 to 3))

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(2) During communication at same potential (CSI mode) (master mode, $\overline{SCKp}$... internal clock output)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	200 Note 1			ns
		2.7 V ≤ V_{DD} < 4.0 V	300 Note 1			ns
		1.8 V ≤ V_{DD} < 2.7 V	600 Note 1			ns
$\overline{SCKp}$ high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 20			ns
		2.7 V ≤ V_{DD} < 4.0 V	t_{KCY1}/2 – 35			ns
		1.8 V ≤ V_{DD} < 2.7 V	t_{KCY1}/2 – 80			ns
SIp setup time (to $\overline{SCKp}$↑) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	70			ns
		2.7 V ≤ V_{DD} < 4.0 V	100			ns
		1.8 V ≤ V_{DD} < 2.7 V	190			ns
SIp hold time (from $\overline{SCKp}$↑) Note 3	t_{KSI1}		30			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 4	t_{KSO1}	C = 30 pF Note 5			40	ns

Notes 1. The value must also be 4/f_{CLK} or more.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

4. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

5. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and the $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01, 10), n: Channel number (n = 0 to 2), g: PIM and POM number (g = 3, 7)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(3) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK}			ns
		1.8 V ≤ V_{DD} < 4.0 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑)[Note 1]	t_{SIK2}			80			ns
SIp hold time (from $\overline{SCKp}$↑)[Note 2]	t_{KSI2}			1/f_{MCK}+50			ns
Delay time from $\overline{SCKp}$↓ to SOp output[Note 3]	t_{KSO2}	C = 30 pF[Note 4]	4.0 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK}+45	ns
			2.7 V ≤ V_{DD} < 4.0 V			2/f_{MCK}+57	ns
			1.8 V ≤ V_{DD} < 2.7 V			2/f_{MCK}+125	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

4. C is the load capacitance of the SOp output lines.

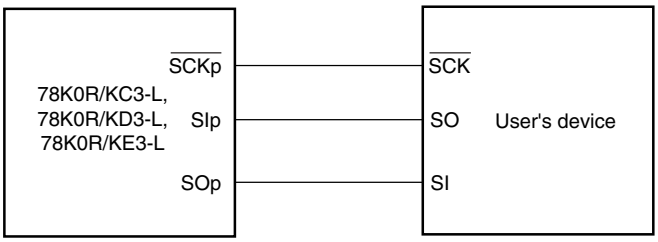
Caution Select the normal input buffer for the SIp pin and $\overline{SCKp}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10), g: PIM and POM number (g = 3, 7)

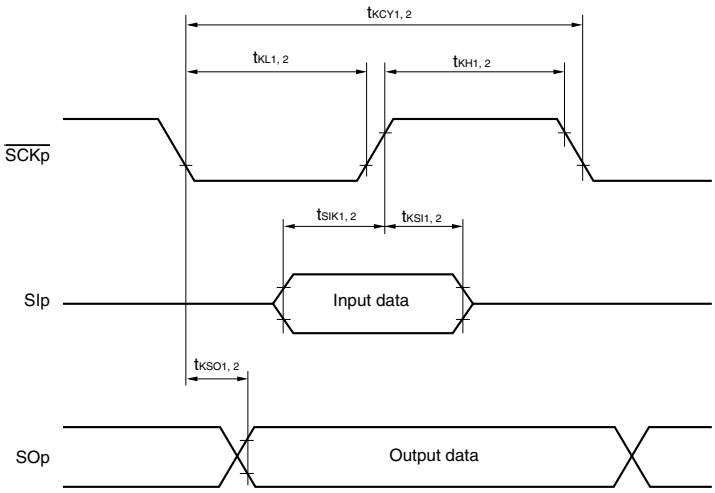
2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of the SMR0n register. n: Channel number (n = 0 to 2))

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

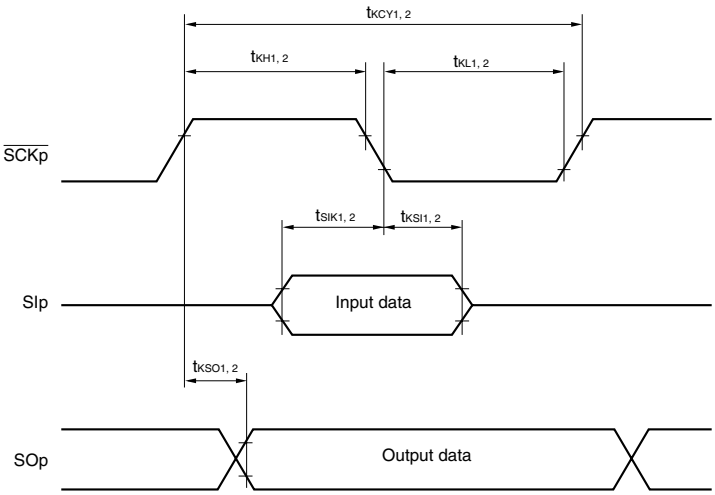
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10)

2. n: Channel number (n = 0 to 2)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

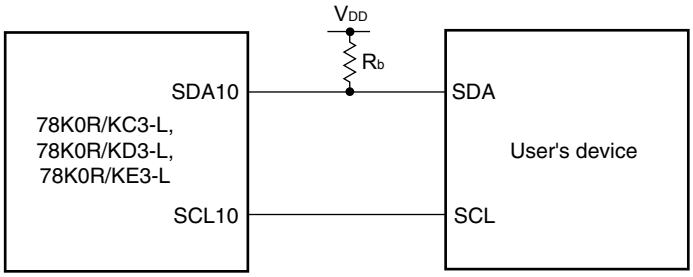
(4) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCL10 clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note	kHz
Hold time when SCL10 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1200		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1500		ns
Hold time when SCL10 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1200		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1500		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK}+120		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK}+230		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	660	ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	710	ns

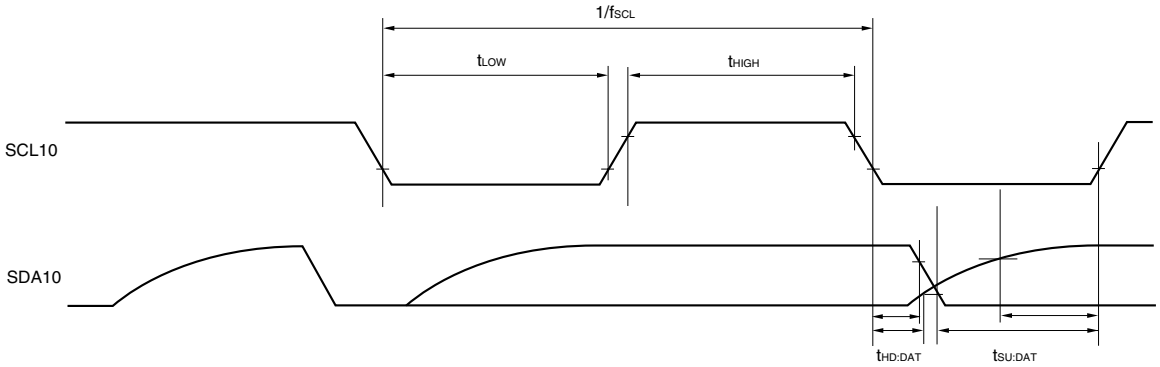
Note The value must also be f_{MCK}/4 or more.

Simplified I^2C mode connection diagram (during communication at same potential)



Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDA10 pin and the normal output mode for the SCL10 pin by using port input mode register 3 (PIM3) and port output mode register 3 (POM3).

Remarks 1. R_b[Ω]:Communication line (SDA10) pull-up resistance,
C_b[F]: Communication line (SCL10, SDA10) load capacitance

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS02 bit of serial mode register 02 (SMR02))

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(5) Communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (1/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V				f_{MCK}/6	bps
				f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps
			2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V				f_{MCK}/6	bps
				f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0, 1) , g: PIM and POM number (g = 3, 7)

2. V_b[V]: Communication line voltage

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of the SMR0n register. n: Channel number (n = 0 to 3))

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(5) Communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (2/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V				**Note 1**	
				f_{CLK} = 16.8 MHz, f_{MCK} = f_{CLK}, C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V			2.8[Note 2]	Mbps
			2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V				**Note 3**	
				f_{CLK} = 19.2 MHz, f_{MCK} = f_{CLK}, C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V			1.2[Note 4]	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1-\frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1-\frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} = EV_{DD} ≤ 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1-\frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1-\frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(Remarks are given on the next page.)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

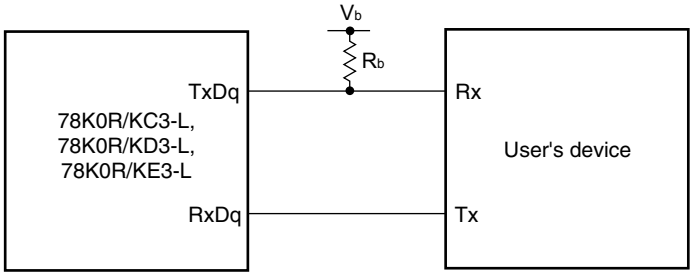
2. q: UART number (q = 0, 1) , g: PIM and POM number (g = 3, 7)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of serial mode register 0n (SMR0n). n: Channel number (n = 0 to 3))

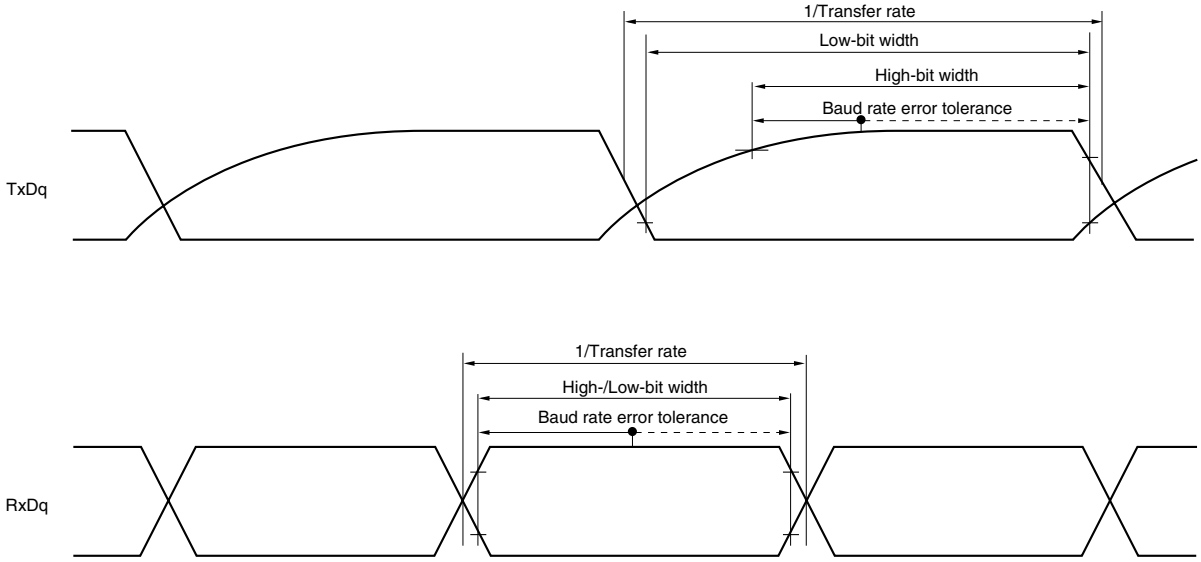
4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

UART mode connection diagram (communication at different potential)



UART mode bit width (communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage

2. q: UART number (q = 0, 1) , g: PIM and POM number (g = 3, 7)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock (1/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	400 Note 1			ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	800 Note 1			ns
$\overline{SCKp}$ high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 75			ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 170			ns
$\overline{SCKp}$ low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 20			ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 35			ns
SIp setup time (to $\overline{SCKp}$↑) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	150			ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	275			ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	30			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			120	ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			215	ns

Notes 1. The value must also be 4/f_{CLK} or more.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance,
C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 01, 10), n: Channel number (n = 0 to 2), g: PIM and POM number (g = 3, 7)

3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

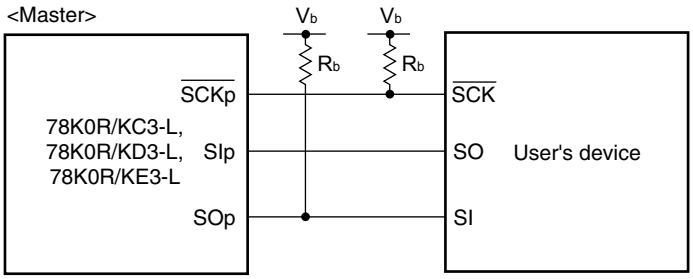
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (2/2)
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIp setup time (to $\overline{SCKp}$↓)[Note]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	70			ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	100			ns
SIp hold time (from $\overline{SCKp}$↓)[Note]	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	30			ns
Delay time from $\overline{SCKp}$↑ to SOp output[Note]	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			40	ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			40	ns

Note When DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

CSI mode connection diagram (communication at different potential)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

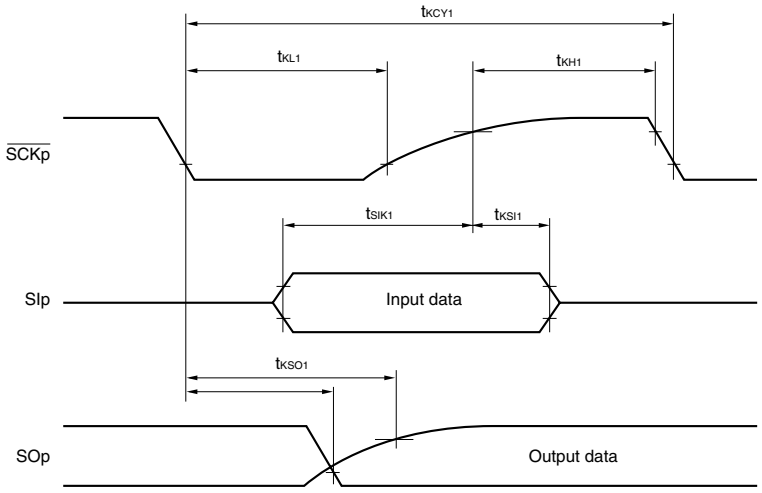
Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance,
C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 01, 10), n: Channel number (n = 0 to 2), g: PIM and POM number (g = 3, 7)

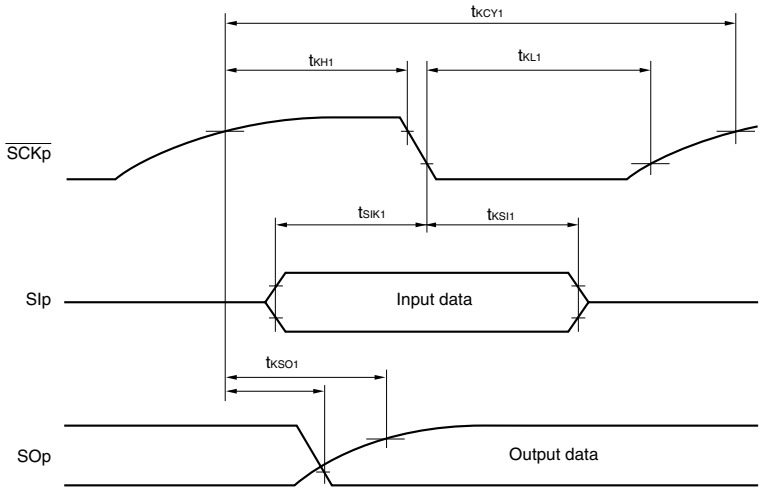
3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

CSI mode serial transfer timing: master mode (communication at different potential)
(When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1)



CSI mode serial transfer timing: master mode (communication at different potential)
(When DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01, 10), n: Channel number (n = 0 to 2), g: PIM and POM number (g = 3, 7)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	13.6 MHz < f_{MCK}	10/f_{MCK}			ns
			6.8 MHz < f_{MCK} ≤ 13.6 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 6.8 MHz	6/f_{MCK}			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	18.5 MHz < f_{MCK}	16/f_{MCK}			ns
			14.8 MHz < f_{MCK} ≤ 18.5 MHz	14/f_{MCK}			ns
			11.1 MHz < f_{MCK} ≤ 14.8 MHz	12/f_{MCK}			ns
			7.4 MHz < f_{MCK} ≤ 11.1 MHz	10/f_{MCK}			ns
			3.7 MHz < f_{MCK} ≤ 7.4 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 3.7 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{KCY2}/2 – 20			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{KCY2}/2 – 35			ns
SIp setup time (to $\overline{SCKp}$↑)[Note 1]	t_{SIK2}			90			ns
SIp hold time (from $\overline{SCKp}$↑)[Note 2]	t_{KSI2}			1/f_{MCK} + 50			ns
Delay time from $\overline{SCKp}$↓ to SOp output[Note 3]	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 230	ns

(Notes, Caution and Remarks are given on the next page.)

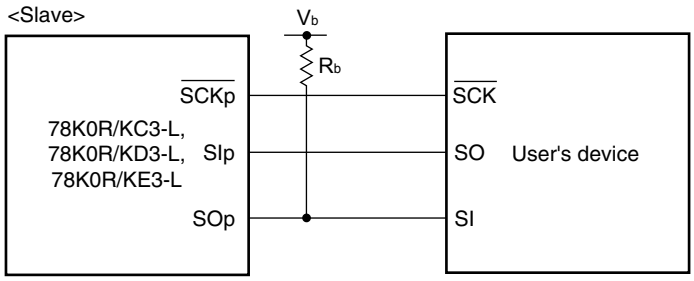
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

CSI mode connection diagram (communication at different potential)



Caution Select the TTL input buffer for the SIp pin and $\overline{SCKp}$ pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (SOp) pull-up resistance,
C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

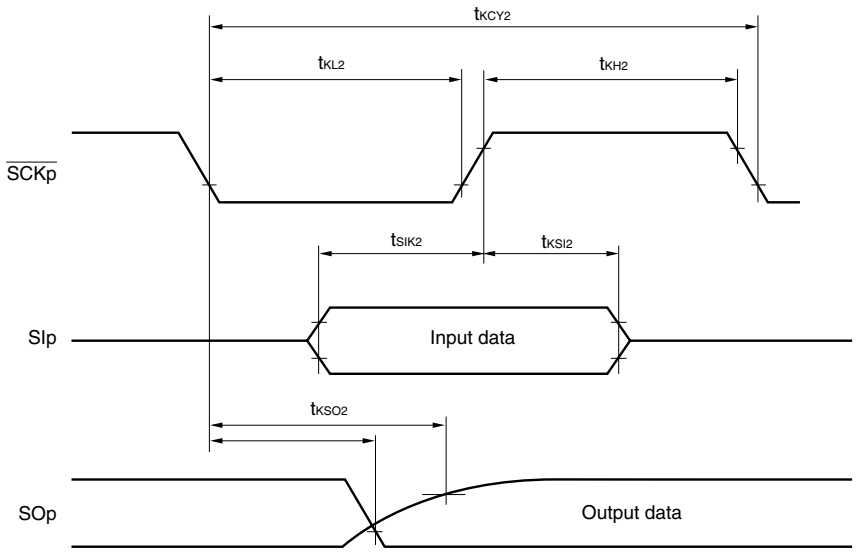
2. p: CSI number (p = 00, 01, 10), g: PIM and POM number (g = 3, 7)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of serial mode register 0n (SMR0n). n: Channel number (n = 0 to 2))

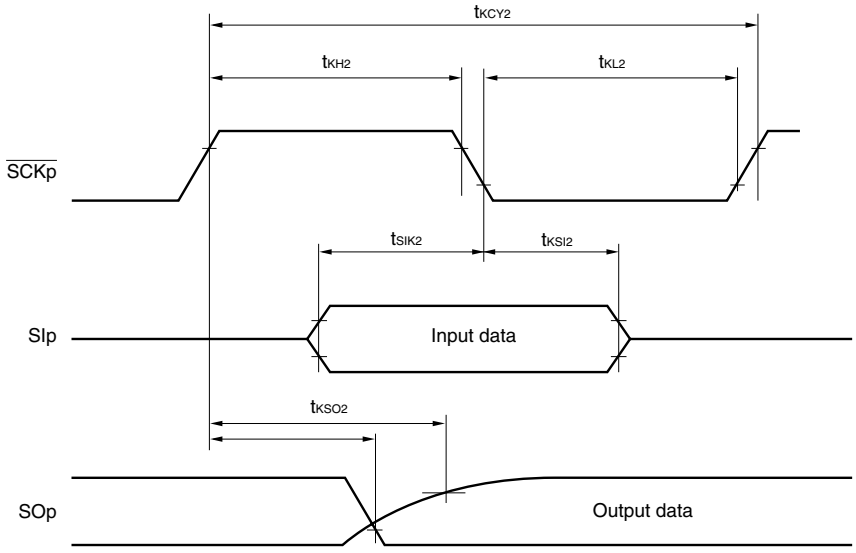
4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

CSI mode serial transfer timing: slave mode (communication at different potential)
(When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1)



CSI mode serial transfer timing: slave mode (communication at different potential)
(When DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0)



Caution Select the TTL input buffer for the SIp pin and $\overline{\text{SCKp}}$ pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01, 10), n: Channel number (n = 0 to 2), g: PIM and POM number (g = 3, 7)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(8) Communication at different potential (2.5 V, 3 V) (simplified I^2C mode)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCL10 clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ		400 Note	kHz
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note	kHz
Hold time when SCL10 = “L”	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	1275		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1275		ns
Hold time when SCL10 = “H”	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	655		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	655		ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	1/f_{MCK} + 190		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	0	640	ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	660	ns

Note The value must also be f_{MCK}/4 or more.

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDA10 pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCL10 pin by using port input mode register 3 (PIM3) and port output mode register 3 (POM3).

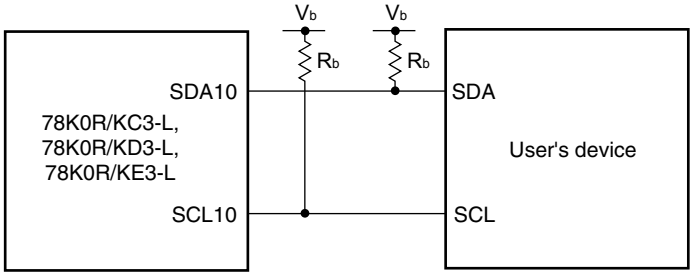
Remarks 1. R_b[Ω]:Communication line (SDA10, SCL10) pull-up resistance,
C_b[F]: Communication line (SDA10, SCL10) load capacitance, V_b[V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS02 bit of serial mode register 02 (SMR02).)

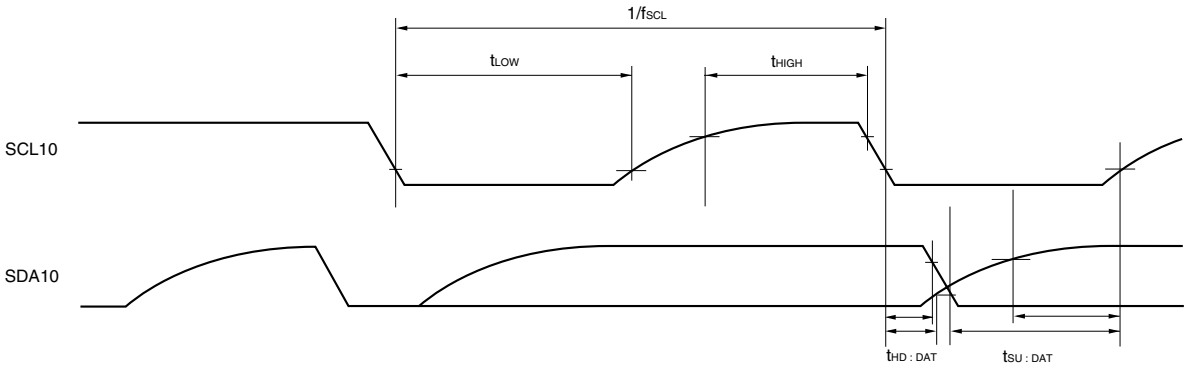
3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified I^2C mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Simplified I²C mode connection diagram (communication at different potential)



Simplified I²C mode serial transfer timing (communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDA10 pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCL10 pin by using port input mode register 3 (PIM3) and port output mode register 3 (POM3).

Remark R_b[Ω]:Communication line (SDA10, SCL10) pull-up resistance, V_b[V]: Communication line voltage

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.6.2 Serial interface IICA

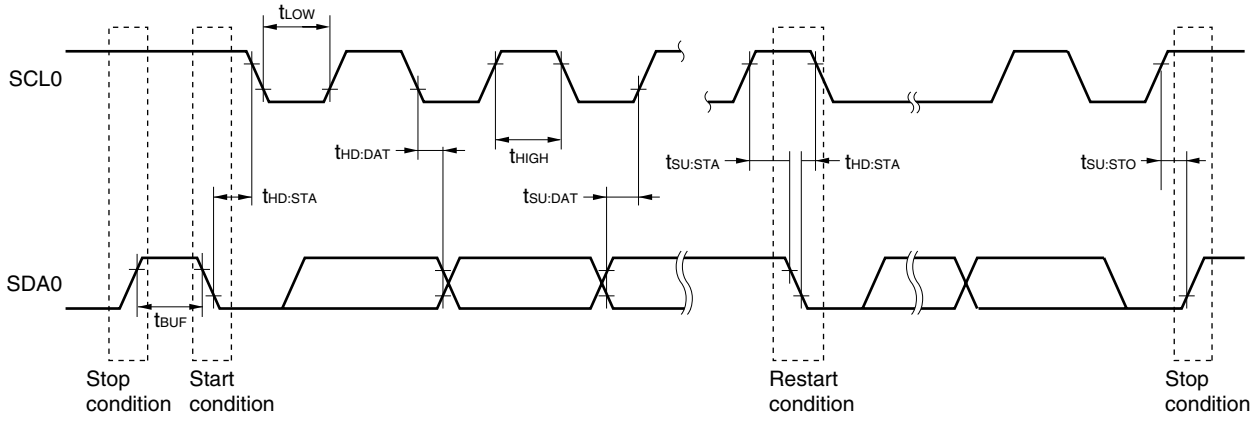
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{SCL}	High speed mode: f_{CLK} ≥ 3.5 MHz Normal mode: f_{CLK} ≥ 1 MHz	0	100	0	400	kHz
Setup time of restart condition Note 1	$t_{SU:STA}$		4.7		0.6		μs
Hold time	$t_{HD:STA}$		4.0		0.6		μs
Hold time when SCL0 = "L"	t_{LOW}		4.7		1.3		μs
Hold time when SCL0 = "H"	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		μs
Bus-free time	t_{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

IICA serial transfer timing



30.6.3 On-chip debug (UART)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			$f_{CLK}/2^{12}$		$f_{CLK}/6$	bps
		Flash memory programming mode			3.33	Mbps
TOOL1 output frequency	f_{TOOL1}	2.7 V ≤ V_{DD} ≤ 5.5 V			10	MHz
		1.8 V ≤ V_{DD} < 2.7 V			2.5	MHz

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.6.4 A/D converter characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					10	bit
Overall error[Notes 1, 2]	AINL					±0.35	%FSR
Conversion time	tCONV	4.0 V ≤ AV_{REF} ≤ 5.5 V	High speed mode 1	2.5		66.6	μs
			Normal mode	5.2		66.6	μs
		2.7 V ≤ AV_{REF} ≤ 5.5 V	High speed mode 2	3.5		66.6	μs
			Normal mode	8.6		66.6	μs
		1.8 V ≤ AV_{REF} ≤ 4.0 V	Low voltage mode	24.1		66.6	μs
Zero-scale error[Notes 1, 2]	EZS					±0.25	%FSR
Full-scale error[Notes 1, 2]	EFS					±0.25	%FSR
Integral non-linearity error[Note 1]	ILE					±2.5	LSB
Differential non-linearity error[Note 1]	DLE					±1.5	LSB
Analog input voltage	VAIN	1.8 V ≤ AV_{REF} ≤ 5.5 V		AV_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

30.6.5 Programmable gain amplifier characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input offset voltage	VIO_{AMP}				±5	±10	mV
Input voltage range	VI_{AMP}			0.1AV_{REF} /gain		0.9AV_{REF} /gain	V
Maximum output voltage	VO_{AMP}			0.1AV_{REF}		0.9AV_{REF}	V
Slew rate	SR_F	Rising edge	4.0 V ≤ AV_{REF} ≤ 5.5 V	3.5			V/μs
			2.7 V ≤ AV_{REF} < 4.0 V	2			V/μs
	SR_R	Falling edge	4.0 V ≤ AV_{REF} ≤ 5.5 V	4			V/μs
			2.7 V ≤ AV_{REF} < 4.0 V	2.5			V/μs
Gain	RG			4 to 12			times
Operation stabilization wait time	t_{AMP}					3	μs

Remark Slew rate: The change with respect to the rise or fall of the output voltage

V/μs: The change in voltage per 1 μs

Operation stabilization wait time: Time required until a state is entered where the DC and AC specifications of the programmable gain amplifier are satisfied after the operation of the programmable gain amplifier has been enabled (OAEN of programmable gain amplifier control register (OAM) = 1)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

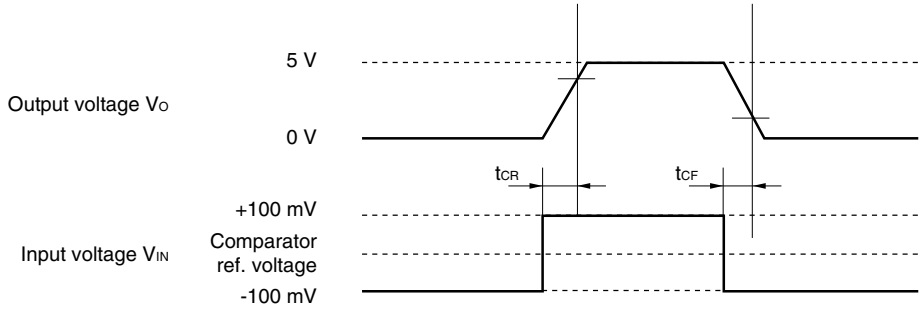
30.6.6 Comparator characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	VIO_{CMP}			±5	±40	mV
Input voltage range	VI_{CMP}		0.1AV_{REF}		0.9AV_{REF}	V
Internal reference voltage deviation	ΔV_{IREF}			2.5	10	%
Response time	t_{CR}	Input amplitude = ±100 mV, at rising edge Note 1		150	300	ns
	t_{CF}	Input amplitude = ±100 mV, at falling edge Note 2		150	300	ns
Operation stabilization wait time	t_{CMP}				1	μs
Reference voltage stabilization wait time	t_{VR}				1	μs

Notes 1. Characteristics of pulse response when CMP0P input or programmable gain amplifier output changes from the comparator reference voltage –100 mV to the comparator reference voltage +100 mV.

2. Characteristics of pulse response when CMP0P input or programmable gain amplifier output changes from the comparator reference voltage +100 mV to the comparator reference voltage –100 mV.



Remark Operation stabilization wait time: Time required until a state is entered where the DC and AC specifications of the comparator are satisfied after the operation of the comparator has been enabled (CnEN bit of comparator n control register (CnCTL) = 1) (n = 0, 1)

Reference voltage stabilization wait time: Time required until the voltage level of the internal reference voltage circuit reaches 99% of the ideal value after the internal reference voltage has been enabled (CnVRE bit of comparator n internal reference voltage setting register (CnRVM) = 1) (n = 0, 1)

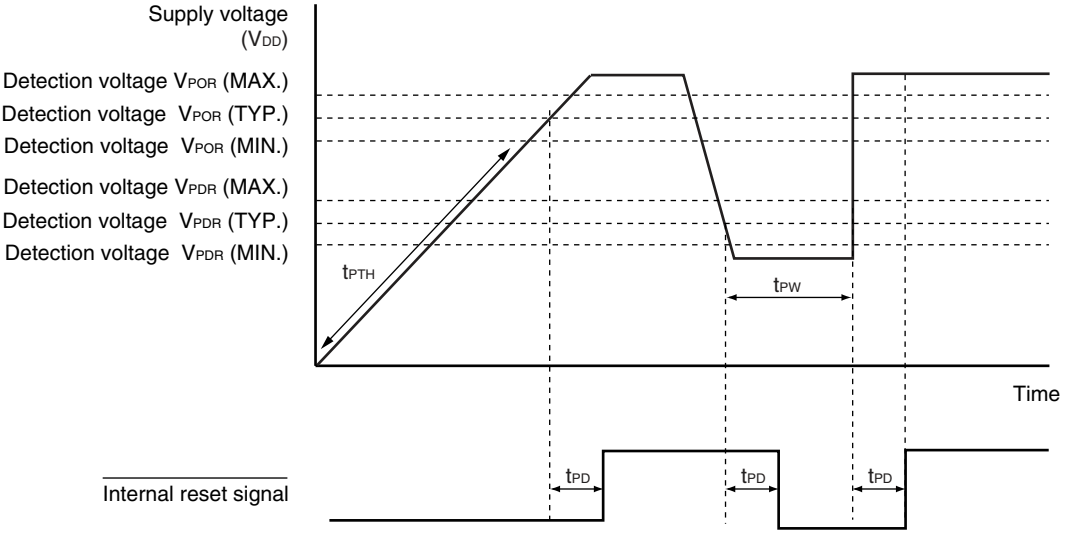
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.6.7 POC circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.52	1.61	1.70	V
	V_{PDR}	Power supply fall time	1.5	1.59	1.68	V
Power supply voltage rise inclination	t_{PTH}	Change inclination of V_{DD}: 0 V → V_{POR}	0.5			V/ms
Minimum pulse width	t_{PW}	When the voltage drops	200			μs
Detection delay time	t_{PD}				200	μs

POC Circuit Timing



Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.6.8 Supply voltage rise time

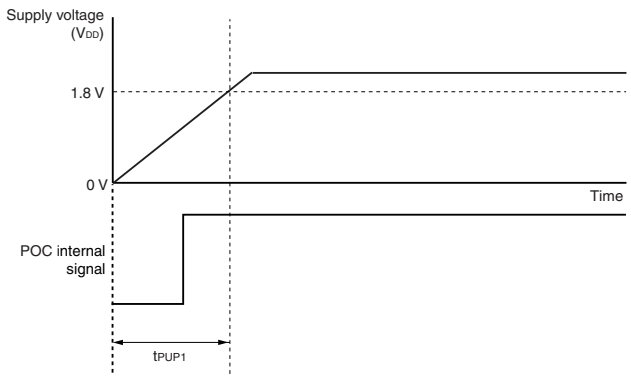
(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.8 V (V_{DD} (MIN.))[Note] (V_{DD}: 0 V → 1.8 V)	t_{PUP1}	LVI default start function stopped is set (LVIOFF (option byte) = 1), when $\overline{\text{RESET}}$ input is not used			3.6	ms
Maximum time to rise to 1.8 V (V_{DD} (MIN.))[Note] (releasing $\overline{\text{RESET}}$ input → V_{DD}: 1.8 V)	t_{PUP2}	LVI default start function stopped is set (LVIOFF (option byte) = 1), when $\overline{\text{RESET}}$ input is used			1.88	ms

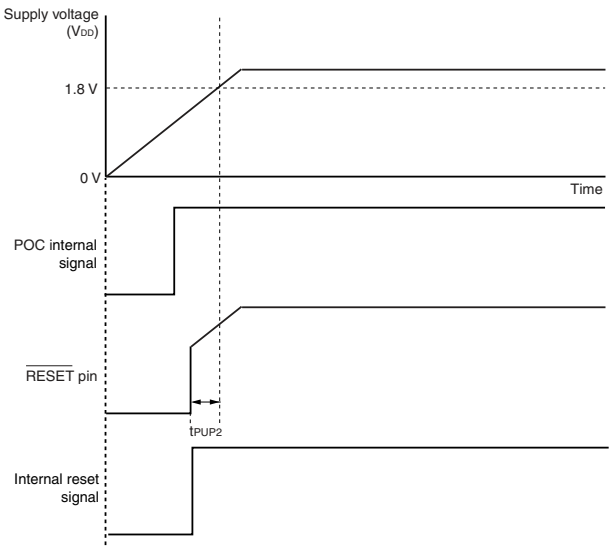
Note Make sure to raise the power supply in a shorter time than this.

Supply Voltage Rise Time Timing

- When the $\overline{\text{RESET}}$ pin input is not used



- When the $\overline{\text{RESET}}$ pin input is used (when external reset is released by the $\overline{\text{RESET}}$ pin, after POC has been released)



Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.6.9 LVI circuit characteristics

(T_A = –40 to +85°C, $V_{PDR} \le V_{DD} = EV_{DD} \le 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)

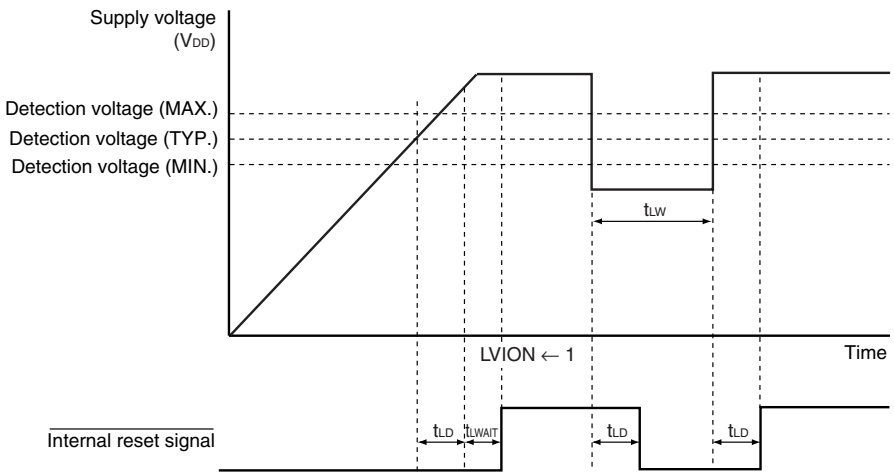
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.12	4.22	4.32	V
		V_{LVI1}		3.97	4.07	4.17	V
		V_{LVI2}		3.82	3.92	4.02	V
		V_{LVI3}		3.66	3.76	3.86	V
		V_{LVI4}		3.51	3.61	3.71	V
		V_{LVI5}		3.35	3.45	3.55	V
		V_{LVI6}		3.20	3.30	3.40	V
		V_{LVI7}		3.05	3.15	3.25	V
		V_{LVI8}		2.89	2.99	3.09	V
		V_{LVI9}		2.74	2.84	2.94	V
		V_{LVI10}		2.58	2.68	2.78	V
		V_{LVI11}		2.43	2.53	2.63	V
		V_{LVI12}		2.28	2.38	2.48	V
		V_{LVI13}		2.12	2.22	2.32	V
		V_{LVI14}		1.97	2.07	2.17	V
		V_{LVI15}		1.81	1.91	2.01	V
	External input pin[Note 1]	V_{EXLVI}	EXLVI < V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
	Power supply voltage on power application	V_{PUPLVI}	When LVI default start function enabled is set	1.87	2.07	2.27	V
Minimum pulse width		t_{LW}		200			μs
Detection delay time		t_{LD}				200	μs
Operation stabilization wait time[Note 2]		t_{LWAIT}				10	μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 15

LVI Circuit Timing



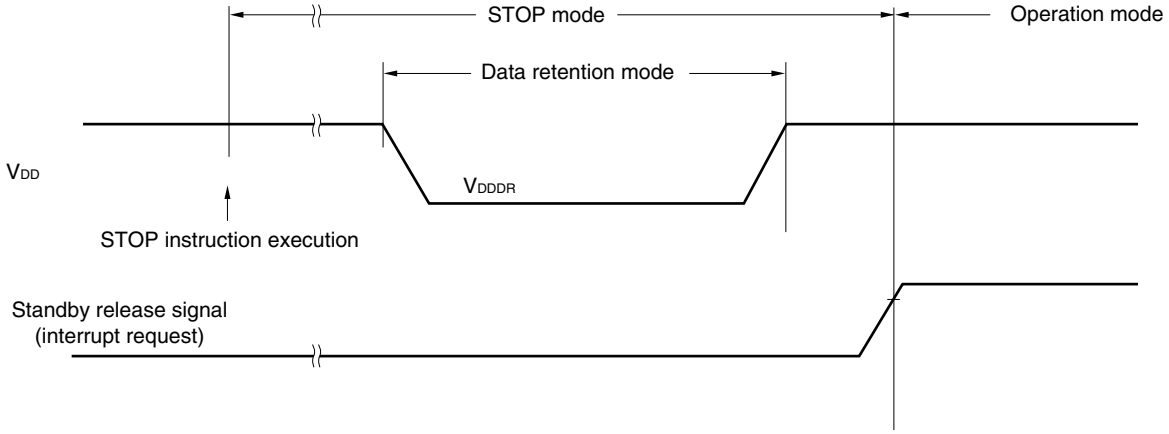
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.5[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



30.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
V_{DD} supply current	I_{DD}	Typ. = 10 MHz, Max. = 20 MHz			6	20	mA
Number of rewrites (number of deletes per block)	C_{erwr}	Used for updating programs When using flash memory programmer and Renesas Electronics self programming library	Retained for 15 years	1,000			Times
		Used for updating data When using Renesas Electronics EEPROM emulation library (available ROM area: 3 to 8 KB of 3 to 8 continuous blocks)	Retained for 5 years	10,000			Times

Remark When updating data multiple times, use the flash memory as one for updating data.

CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)

Cautions 1. The 78K0R/KF3-L, 78K0R/KG3-L have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted are as follows according to product.

31.1 Pins Mounted According to Product

31.1.1 Port functions

Port	78K0R/KF3-L		78K0R/KG3-L	
	μPD78F10xx : xx = 10, 11, 12	μPD78F10xx : xx = 27, 28	μPD78F10xx : xx = 13, 14	μPD78F10xx : xx = 29, 30
Port 0	P02 to P06		P00 to P06	
Port 1	P10 to P17			
Port 2	P20 to P27			
Port 3	P30, P31			
Port 4	P40 to P47			
Port 5	P50 to P55		P50 to P57	
Port 6	P60 to P67			
Port 7	P70 to P77			
Port 8	–		P80 to P87	
Port 9	P90, P91		P91	
Port 11	P110, P111			
Port 12	P120 to P124			
Port 13	P130		P130, P131	
Port 14	P140, P142 to P144		P140 to P145	
Port 15	P150 to P153		P150 to P157	

31.1.2 Non-port functions

Function Name		78K0R/KF3-L		78K0R/KG3-L	
		μPD78F10xx : xx = 10, 11, 12	μPD78F10xx : xx = 27, 28	μPD78F10xx : xx = 13, 14	μPD78F10xx : xx = 29, 30
Power supply, ground		V_{DD}, EV_{DD0}, AV_{REF}, V_{SS}, EV_{SS0}, AV_{SS}		V_{DD}, EV_{DD0}, EV_{DD1}, AV_{REF}, V_{SS}, EV_{SS0}, EV_{SS1}, AV_{SS}	
Regulator		REGC			
Reset		$\overline{\text{RESET}}$			
Clock oscillation		X1, X2, XT1, XT2, EXCLK			
Writing to flash memory		FLMD0			
Interrupt		INTP0-INTP11			
Timer		TI00 to TI07, TI10 to TI13, TO00-TO07, TO10-TO13			
Real time counter		RTCDIV, RTCCL, RTC1HZ			
Serial interface	UART0	RxD0, TxD0			
	UART1	RxD1, TxD1			
	UART2	RxD2, TxD2			
	UART3	RxD3, TxD3			
	UART4	–	RxD4, TxD4	–	RxD4, TxD4
	CSI00	$\overline{\text{SCK00}}$, SI00, SO00			
	CSI01	$\overline{\text{SCK01}}$, SI01, SO01			
	CSI10	$\overline{\text{SCK10}}$, SI10, SO10			
	CSI20	$\overline{\text{SCK20}}$, SI20, SO20			
	CSI40	–	$\overline{\text{SCK40}}$, SI40, SO40	–	$\overline{\text{SCK40}}$, SI40, SO40
	CSI41	–	$\overline{\text{SCK41}}$, SI40, SO40	–	$\overline{\text{SCK41}}$, SI40, SO40
	IIC10	SCL10, SDA10			
	IIC20	SCL20, SDA20			
	IICA	SCL0, SDA0			
A/D converter		ANI0 to ANI11		ANI0 to ANI15	
Clock Output/Buzzer Output		PCLBUZ0, PCLBUZ1			
Key Interrupt		KR0 to KR7			
Low-voltage detector (LVI)		EXLVI			
On-chip debug function		TOOL0, TOOL1			

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.2 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	EV_{DD0} = EV_{DD1}	−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	EV_{SS0}, EV_{SS1}	EV_{SS0} = EV_{SS1}	−0.5 to +0.3	V
	AV_{REF}		−0.5 to V_{DD} +0.3 Note 1	V
	AV_{SS}		−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to 3.6 and −0.3 to V_{DD} +0.3 Note 2	V
Input voltage	V_{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120 to P124, P131, P140 to P145, EXCLK, $\overline{\text{RESET}}$, FLMD0	−0.3 to EV_{DD0}, EV_{DD1} +0.3 and −0.3 to V_{DD} +0.3 Note 1	V
	V_{I2}	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	P20 to P27, P150 to P157	−0.3 to AV_{REF} +0.3 and −0.3 to V_{DD} +0.3 Note 1	V
Output voltage	V_{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P130, P131, P140 to P145	−0.3 to EV_{DD0}, EV_{DD1} +0.3 Note 1	V
	V_{O2}	P20 to P27, P150 to P157	−0.3 to AV_{REF} +0.3	V

Notes 1. Must be 6.5 V or lower.

2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF: target). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Analog input voltage	V_{AN}	ANI0 to ANI15		−0.3 to AV_{REF} +0.3[Note] and −0.3 to V_{DD} +0.3[Note]	V
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P130, P131, P140 to P145	−10	mA
		Total of all pins −80 mA	P00 to P04, P40 to P47, P120, P130, P131, P140 to P145	−25	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111	−55	mA
	I_{OH2}	Per pin	P20 to P27, P150 to P157	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P130, P131, P140 to P145	30	mA
		Total of all pins 200 mA	P00 to P04, P40 to P47, P120, P130, P131, P140 to P145	60	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111	140	mA
	I_{OL2}	Per pin	P20 to P27, P150 to P157	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

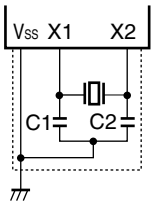
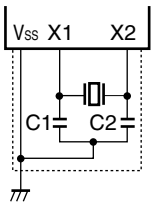
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.3 Oscillator Characteristics

31.3.1 Main system clock oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} ≤ 2.7 V	2.0		5.0	MHz
Crystal resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} ≤ 2.7 V	2.0		5.0	MHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.3.2 Internal oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

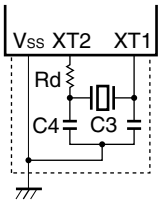
Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
Internal high-speed oscillation clock frequency Note	f_{IH1M}	Low consumption current mode		0.87	1	1.13	MHz
	f_{IH8M}	2.7 V ≤ V_{DD} ≤ 5.5 V, T_A = –40 to +85°C		7.856	8	8.144	MHz
		1.8 V ≤ V_{DD} < 2.7 V, T_A = –20 to +70°C		7.848	8	8.152	MHz
		1.8 V ≤ V_{DD} < 2.7 V, T_A = –40 to +85°C		7.84	8	8.16	MHz
	f_{IH20M}	2.7 V ≤ V_{DD} ≤ 5.5 V		19.52	20	20.48	MHz
Internal low-speed oscillation clock frequency	f_{IL}	Normal current mode	2.7 V ≤ V_{DD} ≤ 5.5 V	27	30	33	kHz
			1.8 V ≤ V_{DD} < 2.7 V	25.5	30	34.5	kHz
		Low consumption current mode		25.5	30	34.5	kHz

Note This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Remark For details on the normal current mode and low consumption current mode according to the regulator output voltage, refer to **CHAPTER 24 REGULATOR**.

31.3.3 Sub system clock oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Items	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT}) Note		32	32.768	35	kHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

31.3.4 Recommended oscillator circuit constants

(1) X1 oscillation: Ceramic resonator (AMPH = 0, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
Murata Manufacturing Co., Ltd.	CSTCC2M00G56-R0	SMD	2.0	Internal (47)	Internal (47)	0	1.8	5.5
	CSTCR4M00G55-R0	SMD	4.0	Internal (39)	Internal (39)	0		
	CSTLS4M00G56-B0	Lead		Internal (47)	Internal (47)	0		
	CSTCR4M19G55-R0	SMD	4.194	Internal (39)	Internal (39)	0		
	CSTLS4M19G56-B0	Lead		Internal (47)	Internal (47)	0		
	CSTCR4M91G55-R0	SMD	4.915	Internal (39)	Internal (39)	0		
	CSTLS4M91G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCR5M00G55-R0	SMD	5.0	Internal (39)	Internal (39)	0		
	CSTLS5M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCR6M00G53-R0	SMD	6.0	Internal (15)	Internal (15)	0		
	CSTLS6M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE8M00G55-R0	SMD	8.0	Internal (33)	Internal (33)	0		
	CSTLS8M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE8M38G55-R0	SMD	8.388	Internal (33)	Internal (33)	0		
	CSTLS8M38G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE10M0G52-R0	SMD	10.0	Internal (10)	Internal (10)	0		
	CSTLS10M0G53-B0	Lead		Internal (15)	Internal (15)	0		

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KF3-L, 78K0R/KG3-L so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(2) X1 oscillation: Crystal resonator (AMPH = 0, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
KYOCERA KINSEKI Corporation	HC49SFNB	Lead	4.0	10	10	0	1.8	5.5
	HC49SFNB	Lead	4.9152	10	10	0		
	HC49SFNB	Lead	5.0	10	10	0		
	HC49SFNB	Lead	6.0	10	10	0		
	HC49SFNB	Lead	8.0	10	10	0		
	HC49SFNB	Lead	8.38	10	10	0		
	HC49SFNB	Lead	10.0	10	10	0		

(3) X1 oscillation: Ceramic resonator (AMPH = 1, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
Murata Manufacturing Co., Ltd.	CSTCE12M0G55-R0	SMD	12.0	Internal (33)	Internal (33)	0	1.8	5.5
	CSTCE16M0V53-R0	SMD	16.0	Internal (15)	Internal (15)	0		
	CSTCE20M0V53-R0	SMD	20.0	Internal (15)	Internal (15)	0		

(4) X1 oscillation: Crystal resonator (AMPH = 1, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
KYOCERA KINSEKI Corporation	HC49SFNB	Lead	12.0	10	10	0	1.8	5.5
	HC49SFNB	Lead	16.0	10	10	0		
	HC49SFNB	Lead	20.0	10	10	0		

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KF3-L, 78K0R/KG3-L so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(5) XT1 oscillation: Crystal resonator (T_A = –40 to +85°C) (1/2)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Load Capacitance CL (pF)	XT1 osclllator oscillation mode Note	Recommended Circuit Constants			Oscillation Voltage Range	
						C3 (pF)	C4 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
CITIZEN FINETECH MIYOTA CO., LTD.	CFS-206	Lead	32.768	8	Normal oscillation	8	8	0	1.8	5.5
				8	Low power consumption oscillation	8	8	0		
				8	Ultra-low power consumption oscillation	8	8	0		
	CM200S	SMD		8	Normal oscillation	7	8	0		
				8	Low power consumption oscillation	7	8	0		
				8	Ultra-low power consumption oscillation	7	8	0		
	CM315	SMD		7	Normal oscillation	7	7	0		
				7	Low power consumption oscillation	7	7	0		
				7	Ultra-low power consumption oscillation	7	7	0		

Note Set the XT1 oscillation mode by using bits AMPHS1 and AMPHS0 of the clock operation mode control register (CMC).

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KF3-L, 78K0R/KG3-L so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(5) XT1 oscillation: Crystal resonator (T_A = –40 to +85°C) (2/2)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Load Capacitance CL (pF)	XT1 osclllator oscillation mode Note 1	Recommended Circuit Constants			Oscillation Voltage Range	
						C3 (pF)	C4 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
SEIKO INSTRUMENTS INC Note 2	SSP-T7-F	SMD	32.768	9.0	Normal oscillation	15	15	0	1.8	5.5
				7.0		10	10	0		
	SSP-T7-FL			6.0	Low power consumption oscillation	9	8	0		
				6.0	Ultra-low power consumption oscillation	9	8	0		
				4.4		5	5	0		
				3.7		4	3	0		
	VT-200-F	Lead		12.5	Normal oscillation	20	20	0		
				8.7		15	13	0		
	VT200-FL			6.0	Low power consumption oscillation	9	8	0		
				6.0	Ultra-low power consumption oscillation	9	8	0		
				4.4		5	5	0		
				3.7		4	3	0		

Notes 1. Set the XT1 oscillation mode by using bits AMPHS1 and AMPHS0 of the clock operation mode control register (CMC).

2. Contact SEIKO INSTRUMENTS INC. (http://www.sii-crystal.com) when using this resonator.

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KF3-L, 78K0R/KG3-L so that the internal operation conditions are within the specifications of the DC and AC characteristics.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.4 DC Characteristics

31.4.1 Pin characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P130, P131, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V			–3.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–1.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–1.0	mA
		Total of P00 to P04, P40 to P47, P120, P130, P131, P140 to P145 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			–20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			–30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–19.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–10.0	mA
		Total of all pins (When duty = 60%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			–50.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–29.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–15.0	mA
	I_{OH2}	Per pin for P20 to P27, P150 to P157	AV_{REF} = V_{DD}			–0.1	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0} or EV_{DD1} pin to an output pin.

2. Specification under conditions where the duty factor is 60% or 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OH} = –20.0 mA

Total output current of pins = (–20.0 × 0.7)/(50 × 0.01) = –28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P02 to P04, P10, P12, P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P130, P131, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.5	mA
		Per pin for P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			3.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Total of P00 to P04, P40 to P47, P120, P130, P131, P140 to P145 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			45.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty = 60%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			65.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			50.0	mA
			1.8 V ≤ V_{DD} ≤ 2.7 V			29.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P157	AV_{REF} = V_{DD}			0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1}, V_{SS}, and AV_{SS} pin.

2. Specification under conditions where the duty factor is 60% or 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OL} = 20.0 mA

Total output current of pins = (20.0 × 0.7)/(50 × 0.01) = 28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P01, P02, P12, P13, P15, P41, P45, P52, P56, P57, P80 to P87, P90, P91, P111, P123, P124, P144		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P03 to P06, P10, P11, P14, P16, P17, P30, P31, P40, P42 to P44, P46, P47, P50, P51, P53 to P55, P64 to P67, P70 to P77, P110, P120 to P122, P131, P140 to P143, P145, EXCLK, $\overline{\text{RESET}}$	Normal input buffer	0.8V_{DD}		V_{DD}	V
	V_{IH3}	P03, P04, P10, P11, P142, P143	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 2.7 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 1.8 V ≤ V_{DD} < 2.7 V	1.6		V_{DD}	V
	V_{IH4}	P20 to P27, P150 to P157	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH5}	P60 to P63		0.7V_{DD}		6.0	V
	V_{IH6}	FLMD0		0.9V_{DD} Note		V_{DD}	V

Note Must be 0.9V_{DD} or higher when used in the flash memory programming mode.

Cautions The maximum value of V_{IH} of pins P02 to P04, P10, P12, and P142 to P144 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	P01, P02, P12, P13, P15, P41, P45, P52, P56, P57, P80 to P87, P90, P91, P111, P123, P124, P144		0		0.3V_{DD}	V
	V_{IL2}	P00, P03 to P06, P10, P11, P14, P16, P17, P30, P31, P40, P42 to P44, P46, P47, P50, P51, P53 to P55, P64 to P67, P70 to P77, P110, P120 to P122, P131, P140 to P143, P145, EXCLK, $\overline{\text{RESET}}$	Normal input buffer	0		0.2V_{DD}	V
	V_{IL3}	P03, P04, P10, P11, P142, P143	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 2.7 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.8 V ≤ V_{DD} < 2.7 V	0		0.2	V
	V_{IL4}	P20 to P27, P150 to P157	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
	V_{IL5}	P60 to P63		0		0.3V_{DD}	V
	V_{IL6}	FLMD0 Note		0		0.1V_{DD}	V

Note When disabling writing of the flash memory, connect the FLMD0 pin processing directly to V_{SS}, and maintain a voltage less than 0.1V_{DD}.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P130, P131, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = – 3.0 mA	V_{DD} – 0.7			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.0 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27, P150 to P157	AV_{REF} = V_{DD}, I_{OH2} = –0.1 mA	AV_{REF} – 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P130, P131, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.0 mA			0.5	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = 0.5 mA			0.4	V
	V_{OL2}	P20 to P27, P150 to P157	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA			0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 2.0 mA			0.4	V

Caution The maximum value of V_{IH} of pins P02 to P04, P10, P12, and P142 to P144 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P131, P140 to P145, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P20 to P27, P150 to P157	$V_I = AV_{REF}$ $AV_{REF} = V_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{DD}$	In input port			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P131, P140 to P145, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL2}	P20 to P27, P150 to P157	$V_I = V_{SS}$ $AV_{REF} = V_{DD}$				–1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{SS}$	In input port			–1	μA
				In resonator connection			–10	μA

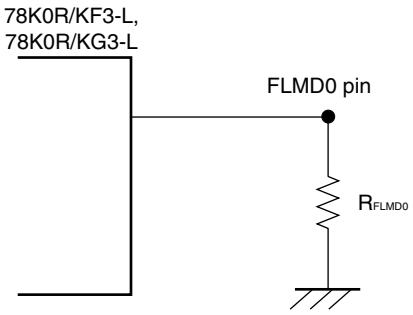
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
On-chip pll-up resistance	R_U	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P131, P140 to P145	V_I = V_{SS}, In input port	10	20	100	kΩ
FLMD0 pin external pull-down resistance[Note]	R_{FLMD0}	When enabling the self-programming mode setting with software		100			kΩ

Note It is recommended to leave the FLMD0 pin open. If the pin is required to be pulled down externally, set R_{FLMD0} to 100 kΩ or more.



Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.4.2 Supply current characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Square wave input		5.9	8.3	mA
				Resonator connection		6.2	8.6	mA
			f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Square wave input		5.9	8.3	mA
				Resonator connection		6.2	8.6	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 5.0 V	Square wave input		3.3	4.8	mA
				Resonator connection		3.4	4.9	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		3.3	4.8	mA
				Resonator connection		3.4	4.9	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		1.8	2.7	mA
				Resonator connection		1.9	2.8	mA
<R>			f_{MX} = 5 MHz Notes 2, 3,	Square wave input		1.4	2.2	mA
<R>			V_{DD} = 2.0 V	Resonator connection		1.4	2.2	mA
			f_{IH20} = 20 MHz Note 4	V_{DD} = 5.0 V		6.1	8.6	mA
				V_{DD} = 3.0 V		6.1	8.6	mA
<R>			f_{IH} = 8 MHz Note 4	V_{DD} = 5.0 V		2.7	3.8	mA
<R>				V_{DD} = 3.0 V		2.7	3.8	mA
<R>			f_{IH} = 1 MHz Notes 4, 5	V_{DD} = 3.0 V		210	389	μA
			f_{SUB} = 32.768 kHz Note 6, T_A = –40 to +50 °C	V_{DD} = 5.0 V		4.3	9.3	μA
				V_{DD} = 3.0 V		4.3	9.3	μA
				V_{DD} = 2.0 V		4.3	9.3	μA
			f_{SUB} = 32.768 kHz Note 6, T_A = –40 to +70 °C	V_{DD} = 5.0 V		4.3	12.3	μA
				V_{DD} = 3.0 V		4.3	12.3	μA
				V_{DD} = 2.0 V		4.3	12.3	μA
			f_{SUB} = 32.768 kHz Note 6, T_A = –40 to +85 °C	V_{DD} = 5.0 V		4.3	15.5	μA
				V_{DD} = 3.0 V		4.3	15.5	μA
				V_{DD} = 2.0 V		4.3	15.5	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. When internal high-speed oscillator, 20 MHz internal high-speed oscillator, and subsystem clock are stopped.

3. When AMPH (bit 0 of clock operation mode control register (CMC)) = 0, FLPC and FSEL (bits 1 and 0 of operation speed mode control register (OSMC)) = 0 and 0.

4. When high-speed system clock and subsystem clock are stopped.

5. When low consumption current mode is set (RMC = 5AH, OSMC = 02H).

6. When operating real-time counter (RTC) and setting ultra-low current consumption (AMPHS1 (bit2 of CMC register) = 1, OSMC = 82H). When internal high-speed oscillation, 20 MHz internal high-speed oscillation, and high-speed system clock are stopped. When watchdog timer is stopped.

(Remarks are given on the next page.)

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH20}: 20 MHz internal high-speed oscillation clock frequency

3. f_{IH}: Internal high-speed oscillation clock frequency

4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

5. RMC: Regulator mode control register (RMC)

6. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD2} Note 1	HALT mode	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Square wave input		1.2	3.6	mA
				Resonator connection		1.5	3.9	mA
			f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Square wave input		1.2	3.6	mA
				Resonator connection		1.5	3.9	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 5.0 V	Square wave input		0.55	2.1	mA
				Resonator connection		0.65	2.2	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		0.55	2.1	mA
				Resonator connection		0.65	2.2	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		0.40	1.8	mA
				Resonator connection		0.45	1.8	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 2.0 V	Square wave input		0.28	1.3	mA
				Resonator connection		0.33	1.4	mA
			f_{IH20} = 20 MHz Note 4	V_{DD} = 5.0 V		1.4	3.9	mA
				V_{DD} = 3.0 V		1.4	3.9	mA
			f_{IH} = 8 MHz Note 4	V_{DD} = 5.0 V		0.48	1.8	mA
				V_{DD} = 3.0 V		0.48	1.8	mA
			f_{IH} = 1 MHz Note 4, 5	V_{DD} = 3.0 V		50	168	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value include the peripheral operation current. However, not including the current flowing into the A/D converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. During HALT instruction execution by flash memory.

2. When internal high-speed oscillator, 20 MHz internal high-speed oscillator, and subsystem clock are stopped.

3. When AMPH (bit 0 of clock operation mode control register (CMC)) = 0, FLPC and FSEL (bits 1 and 0 of operation speed mode control register (OSMC)) = 0 and 0.

4. When high-speed system clock and subsystem clock are stopped.

5. When low consumption current mode is set (RMC = 5AH, OSMC = 02H).

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH20}: 20 MHz internal high-speed oscillation clock frequency

3. f_{IH}: Internal high-speed oscillation clock frequency

4. RMC: Regulator mode control register (RMC)

5. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD2} Note 1	HALT mode	f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +50 °C	V_{DD} = 5.0 V		1.0	3.7	μA
				V_{DD} = 3.0 V		1.0	3.7	μA
				V_{DD} = 2.0 V		1.0	3.7	μA
			f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +70 °C	V_{DD} = 5.0 V		1.0	6.1	μA
				V_{DD} = 3.0 V		1.0	6.1	μA
				V_{DD} = 2.0 V		1.0	6.1	μA
			f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +85 °C	V_{DD} = 5.0 V		1.0	8.9	μA
				V_{DD} = 3.0 V		1.0	8.9	μA
				V_{DD} = 2.0 V		1.0	8.9	μA
	I_{DD3} Note 3	STOP mode	T_A = –40 to +50 °C			0.37	2.8	μA
			T_A = –40 to +70 °C			0.37	5.2	μA
			T_A = –40 to +85 °C			0.37	7.9	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value include the peripheral operation current. However, not including the current flowing into the A/D converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. During HALT instruction execution by flash memory.

2. When operating real-time counter (RTC) and setting ultra-low current consumption (AMPHS1 (bit2 of CMC register) = 1, OSMC = 82H). When internal high-speed oscillation, 20 MHz internal high-speed oscillation, and high-speed system clock are stopped. When watchdog timer is stopped. When RTCLPC = 1 (stops supply of subsystem clock to peripheral functions other than real-time counter). When output function of RTC is stopped.

3. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value includes the peripheral operation current and STOP leakage current. However, not including the current flowing into the A/D converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. When subsystem clock is stopped. When watchdog timer is stopped.

Remarks 1. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

2. RTCLPC: bit 7 of the operation speed mode control register (OSMC)

3. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Real-time counter operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz		V_{DD} = 3.0 V		0.2	1.0	μA
				V_{DD} = 2.0 V		0.2	1.0	
Watchdog timer operating current	I_{WDT} Notes 2, 3	f_{IL} = 30 kHz				0.31	0.35	μA
A/D converter operating current	I_{ADC} Note 4	During conversion at maximum speed	High speed mode 1	AV_{REF} = V_{DD} = 5.0 V		1.72	3.2	mA
			High speed mode 2	AV_{REF} = V_{DD} = 3.0 V		0.72	1.6	mA
			Normal mode	AV_{REF} = V_{DD} = 5.0 V		0.86	1.9	mA
			Low voltage mode	AV_{REF} = V_{DD} = 3.0 V		0.37	0.8	mA
LVI operating current	I_{LVI} Note 5					9	18	μA

Notes 1. Current flowing only to the real-time counter (excluding the operating current of the XT1 oscillator). The TYP. value of the current value of the 78K0R/KF3-L, 78K0R/KG3-L is the sum of the TYP. values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time counter operates in operation mode or HALT mode. The I_{DD1} and I_{DD2} MAX. values also include the real-time counter operating current. When the real-time counter operates during f_{CLK} = f_{SUB}/2, the TYP. value of I_{DD2} includes the real-time counter operating current.

2. When internal high-speed oscillator and high-speed system clock are stopped.

3. Current flowing only to the watchdog timer (including the operating current of the 30 kHz internal oscillator). The current value of the 78K0R/KF3-L, 78K0R/KG3-L is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates during f_{CLK} = f_{SUB}/2 or STOP mode.

4. Current flowing only to the A/D converter (AV_{REF} pin). The current value of the 78K0R/KF3-L, 78K0R/KG3-L is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing only to the LVI circuit. The current value of the 78K0R/KF3-L, 78K0R/KG3-L is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates in the Operating, HALT or STOP mode.

Remarks 1. f_{IL}: Internal low-speed oscillation clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.5 AC Characteristics

31.5.1 Basic operation

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

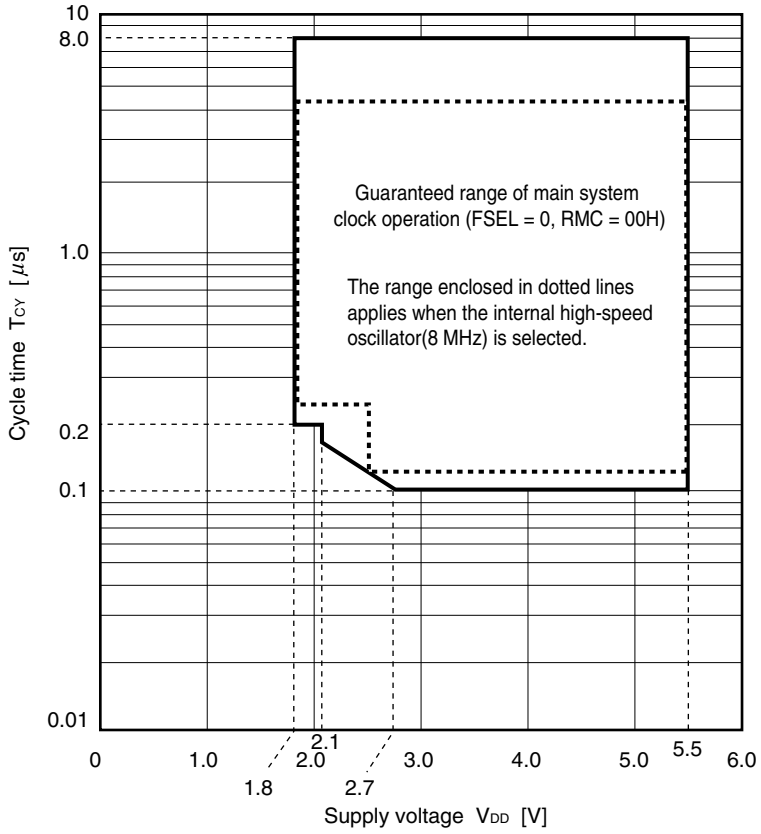
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	Normal current mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		8	μs
				1.8 V ≤ V_{DD} < 2.7 V	0.2		8	μs
			Low consumption current mode		1		8	μs
		Subsystem clock (f_{SUB}) operation			57.2	61	62.5	μs
		In the self programming mode	Normal current mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		1	μs
				1.8 V ≤ V_{DD} < 2.7 V	0.2		1	μs
			Low consumption current mode			1		μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			2.0		20.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V			2.0		5.0	MHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		1.8 V ≤ V_{DD} < 2.7 V			96			ns
TI00 to TI07, TI10 to TI13 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns
TO00 to TO07, TO10 to TO13 output frequency	f_{TO}	2.7 V ≤ V_{DD} ≤ 5.5 V					10	MHz
		1.8 V ≤ V_{DD} < 2.7 V					5	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	2.7 V ≤ V_{DD} ≤ 5.5 V					10	MHz
		1.8 V ≤ V_{DD} < 2.7 V					5	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}				1			μs
Key interrupt input low-level width	t_{KR}				250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Remarks 1. f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

2. For details on the normal current mode and low consumption current mode according to the regulator output voltage, refer to **CHAPTER 24 REGULATOR**.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

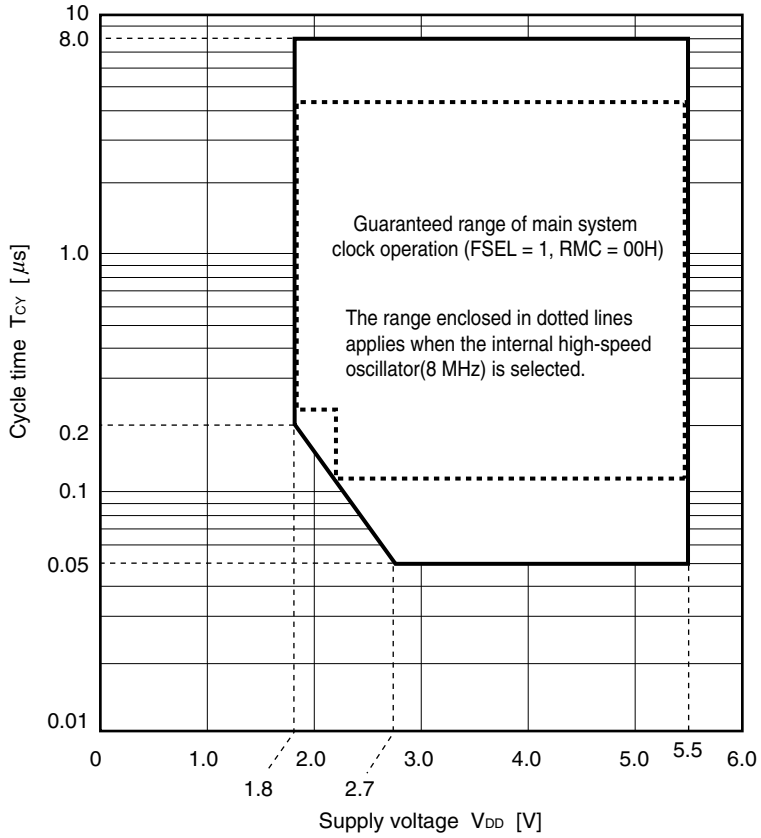
Minimum instruction execution time during main system clock operation (FSEL = 0, RMC = 00H)



Remark FSEL: Bit 0 of the operation speed mode control register (OSMC)
RMC: Regulator mode control register

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Minimum instruction execution time during main system clock operation (FSEL = 1, RMC = 00H)

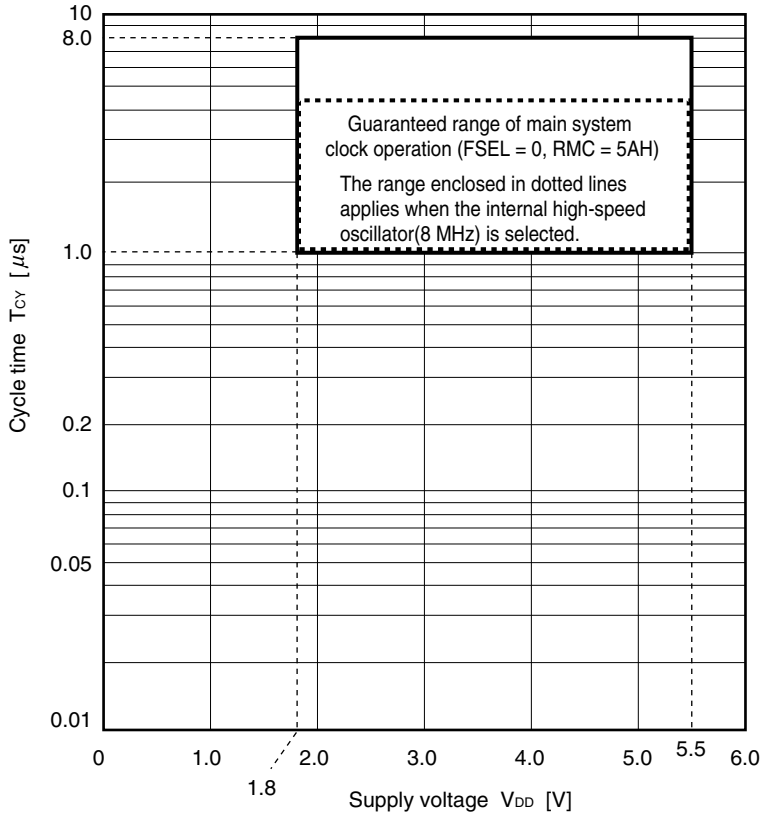


Caution When V_{DD} < 2.25 V and FSEL = 1, It is prohibited to release STOP mode during f_{EX} operation or f_{IH} operation (This must not be performed even if the frequency is divided. The STOP mode may be released during f_X operation.).

Remark FSEL: Bit 0 of the operation speed mode control register (OSMC)
RMC: Regulator mode control register

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Minimum instruction execution time during main system clock operation (FSEL = 0, RMC = 5AH)

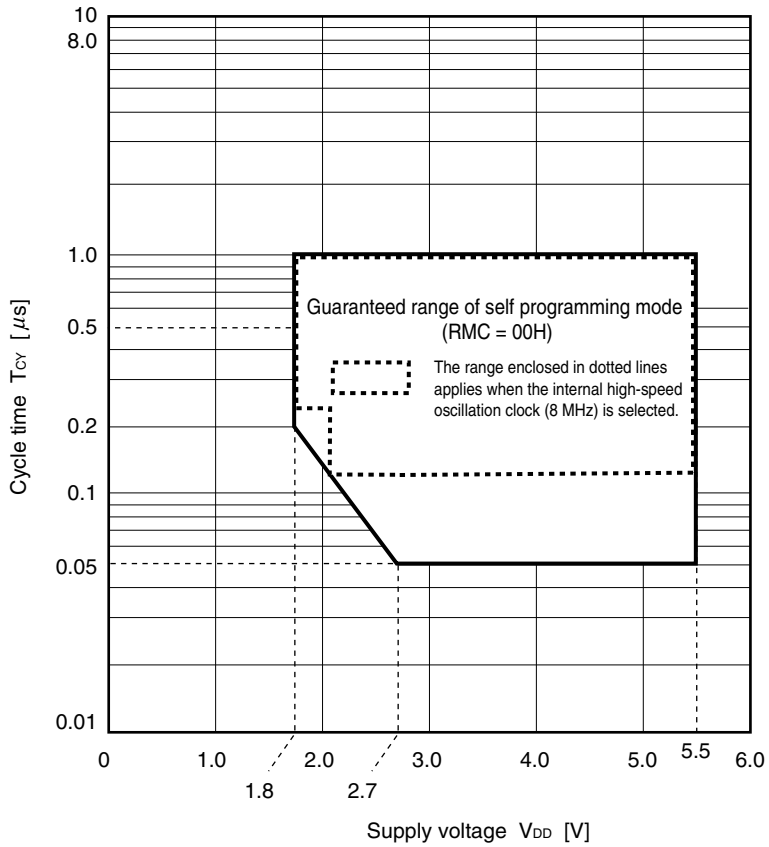


Remarks 1. FSEL: Bit 0 of the operation speed mode control register (OSMC)
RMC: Regulator mode control register

2. The entire voltage range is 1 MHz (MAX.) when RMC is set to 5AH.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Minimum instruction execution time during self programming mode (RMC = 00H)



Remarks 1. RMC: Regulator mode control register (RMC)

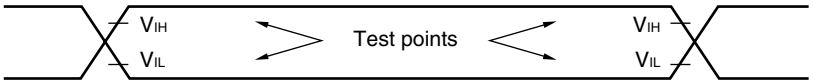
2. The self programming function cannot be used when the CPU operates with the subsystem clock.

3. The entire voltage range is 1 MHz when RMC is set to 5AH.

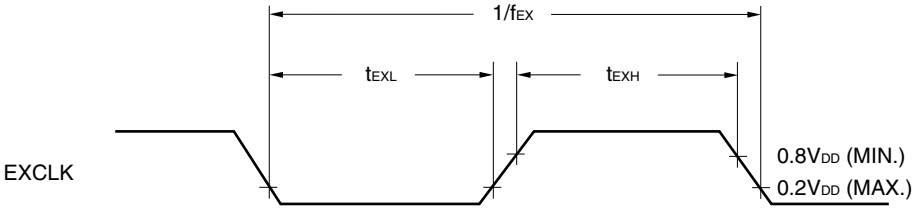
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.5.2 Measurement conditions

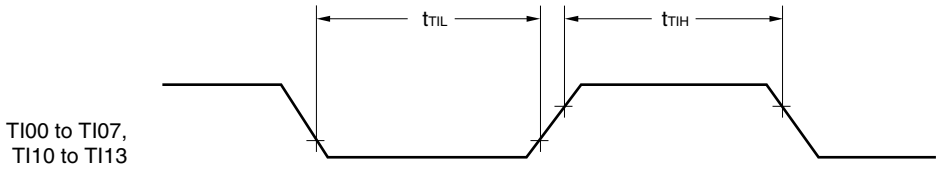
AC Timing Test Points (Excluding external bus interface)



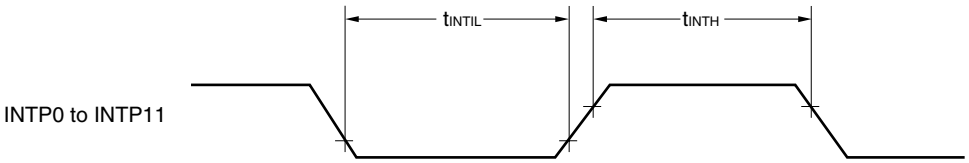
External Main System Clock Timing



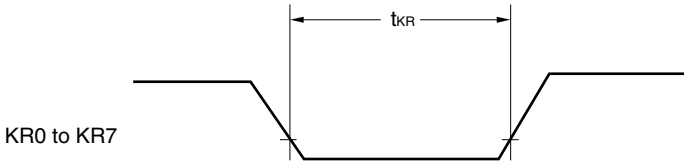
TI Timing



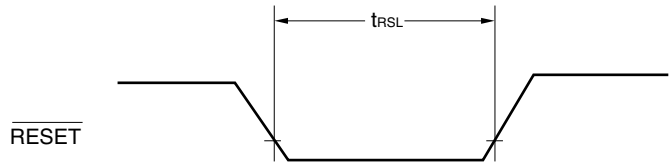
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.6 Peripheral Functions Characteristics

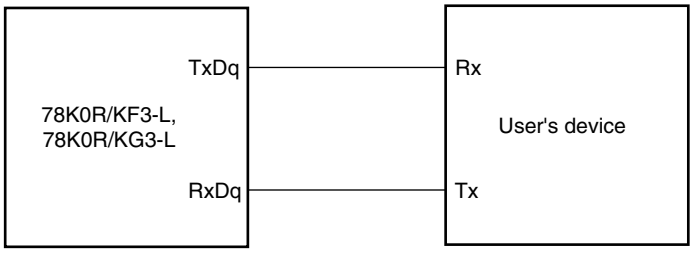
31.6.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

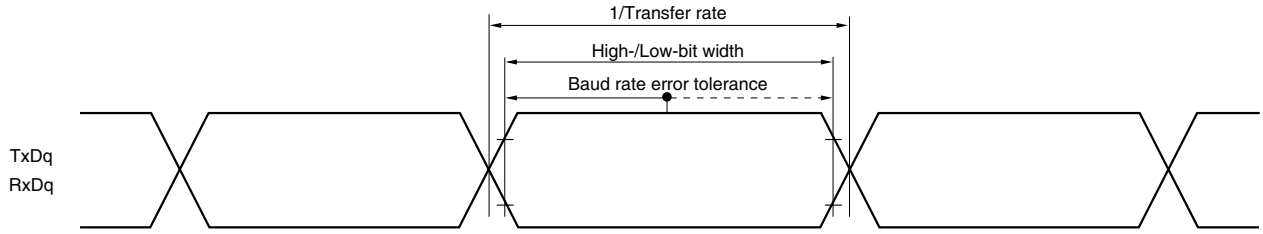
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		1.8 V ≤ V_{DD} ≤ 5.5 V			f_{MCK}/6	bps
		f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}, 2.7 V ≤ V_{DD} ≤ 5.5 V			3.3	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0 to 4), g: PIM and POM number (g = 0, 1, 14)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3))

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(2) During communication at same potential (CSI mode) (master mode, $\overline{SCKp}$... internal clock output)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	200 Note 1			ns
		2.7 V ≤ V_{DD} < 4.0 V	300 Note 1			ns
		1.8 V ≤ V_{DD} < 2.7 V	600 Note 1			ns
$\overline{SCKp}$ high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 20			ns
		2.7 V ≤ V_{DD} < 4.0 V	t_{KCY1}/2 – 35			ns
		1.8 V ≤ V_{DD} < 2.7 V	t_{KCY1}/2 – 80			ns
SIp setup time (to $\overline{SCKp}$↑) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	70			ns
		2.7 V ≤ V_{DD} < 4.0 V	100			ns
		1.8 V ≤ V_{DD} < 2.7 V	190			ns
SIp hold time (from $\overline{SCKp}$↑) Note 3	t_{KSI1}		30			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 4	t_{KSO1}	C = 30 pF Note 5			40	ns

Notes 1. The value must also be 4/f_{CLK} or more.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 20, 40, 41), g: PIM and POM number (g = 0, 1, 14)

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2))

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(3) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK}			ns
		1.8 V ≤ V_{DD} < 4.0 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑) Note 1	t_{SIK2}			80			ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI2}			1/f_{MCK}+50			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	4.0 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK}+45	ns
			2.7 V ≤ V_{DD} < 4.0 V			2/f_{MCK}+57	ns
			1.8 V ≤ V_{DD} < 2.7 V			2/f_{MCK}+125	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

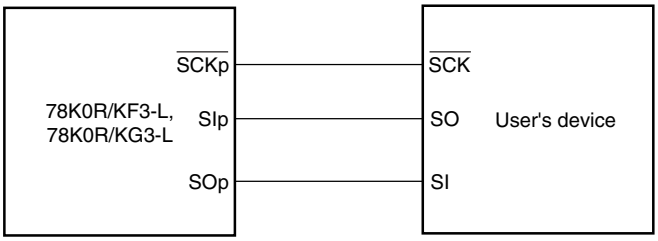
Caution Select the normal input buffer for the SIp pin and $\overline{SCKp}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 20, 40, 41), g: PIM and POM number (g = 0, 1, 14)

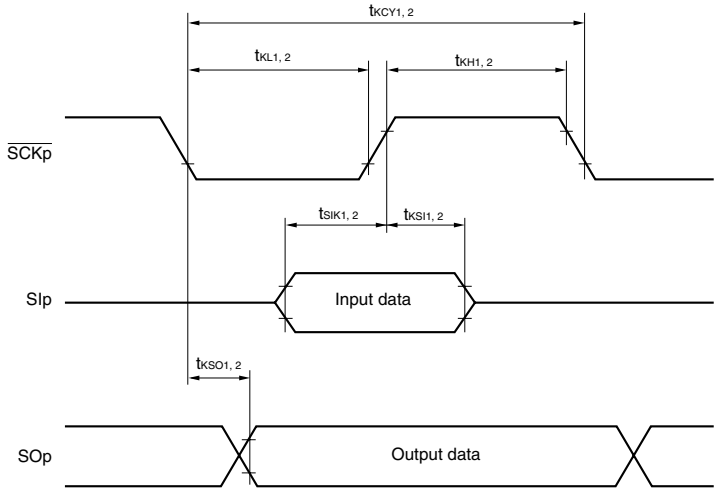
2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of the SMRmn register. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2))

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

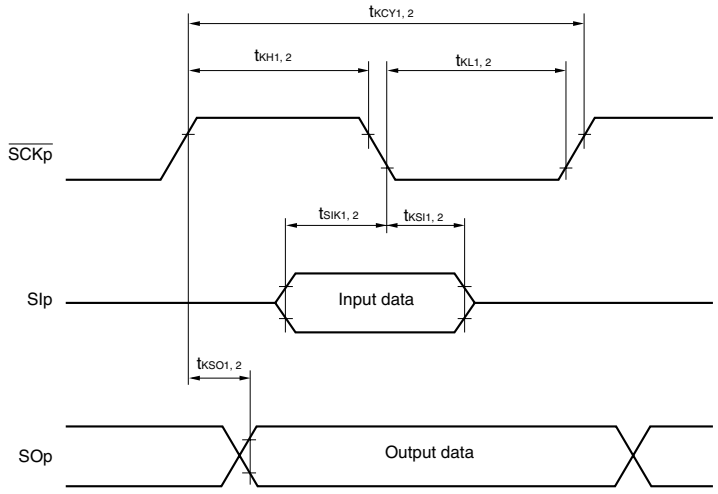
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 20, 40, 41)

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

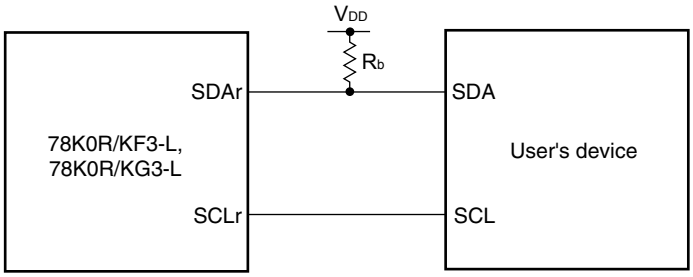
(4) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1200		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1500		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1200		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1500		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK}+120		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK}+230		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	660	ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	710	ns

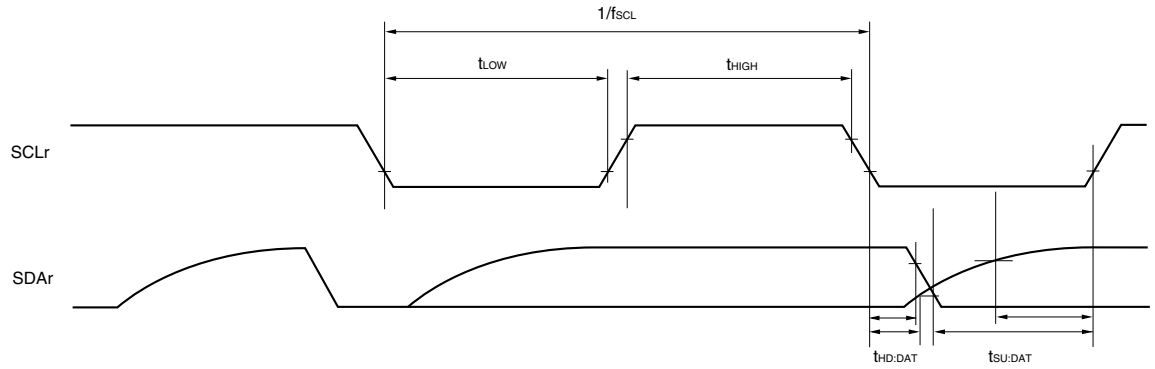
Note The value must also be f_{MCK}/4 or more.

Simplified I^2C mode mode connection diagram (during communication at same potential)



Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Simplified I^2C mode serial transfer timing (during communication at same potential)



Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (SDAr) pull-up resistance,
C_b[F]: Communication line (SCLr, SDAr) load capacitance

2. r: IIC number (r = 10, 20), g: PIM and POM number (g = 0, 14)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 02, 10)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(5) Communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V				f_{MCK}/6	bps
				f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V				f_{MCK}/6	bps
				f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2, 4), g: PIM and POM number (g = 0, 1, 14)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3))

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(5) Communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V				**Note 1**	
				f_{CLK} = 16.8 MHz, f_{MCK} = f_{CLK}, C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V			2.8 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V				**Note 3**	
				f_{CLK} = 19.2 MHz, f_{MCK} = f_{CLK}, C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V			1.2 Note 4	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(**Remark** are given on the next page.)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

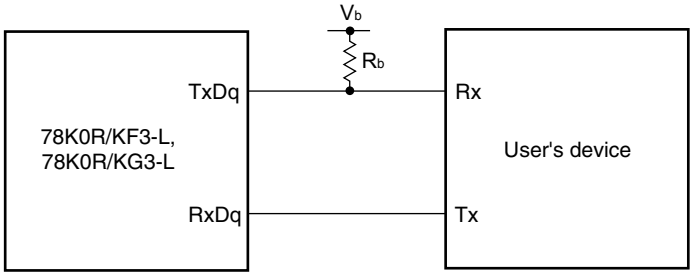
2. q: UART number (q = 0 to 2, 4), g: PIM and POM number (g = 0, 1, 14)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3))

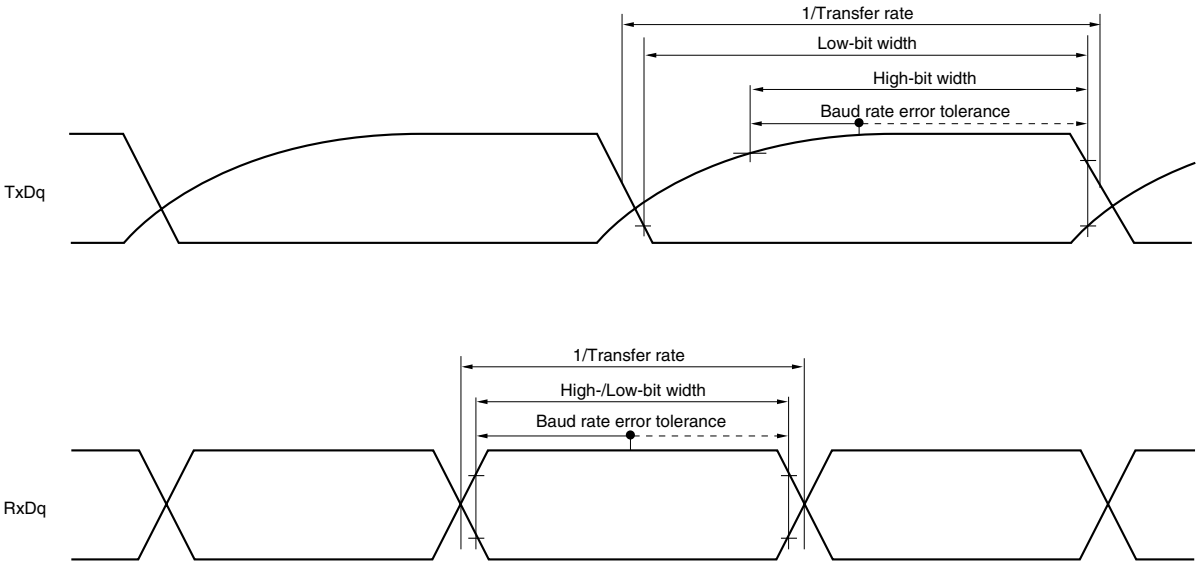
4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2, 4), g: PIM and POM number (g = 0, 1, 14)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock (1/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	400 Note 1			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	800 Note 1			ns
$\overline{SCKp}$ high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 75			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 170			ns
$\overline{SCKp}$ low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 20			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 35			ns
SIp setup time (to $\overline{SCKp}$↑) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	150			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	275			ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	30			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			215	ns

Notes 1. The value must also be 4/f_{CLK} or more.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 01, 10, 20, 40, 41), g: PIM and POM number (g = 0, 1, 14)

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

3. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance,
C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

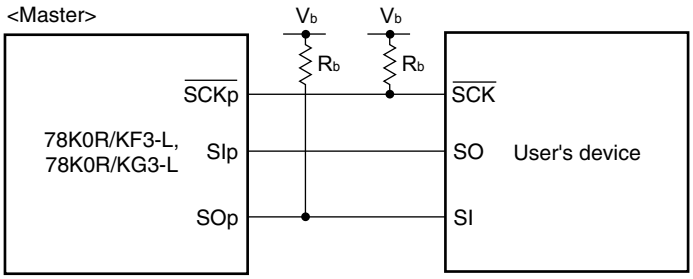
(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (2/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIp setup time (to $\overline{SCKp}$↓) Note	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	70			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	100			ns
SIp hold time (from $\overline{SCKp}$↓) Note	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	30			ns
Delay time from $\overline{SCKp}$↑ to SOp output Note	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			40	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			40	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 01, 10, 20, 40, 41), g: PIM and POM number (g = 0, 1, 14)

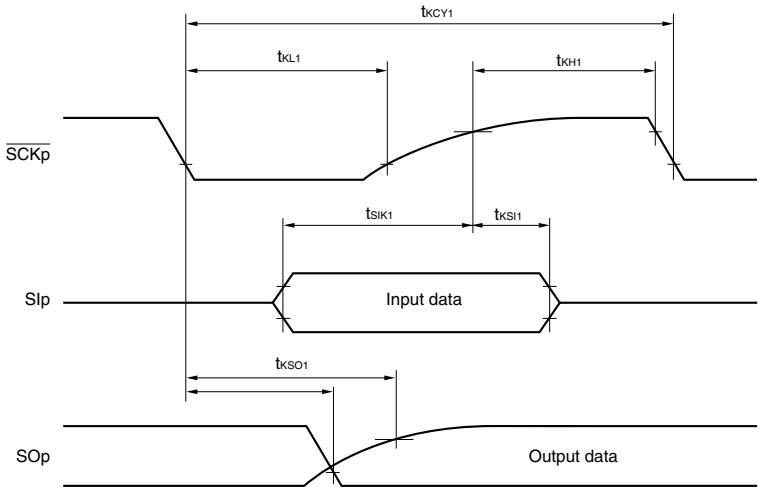
2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

3. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance,
C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

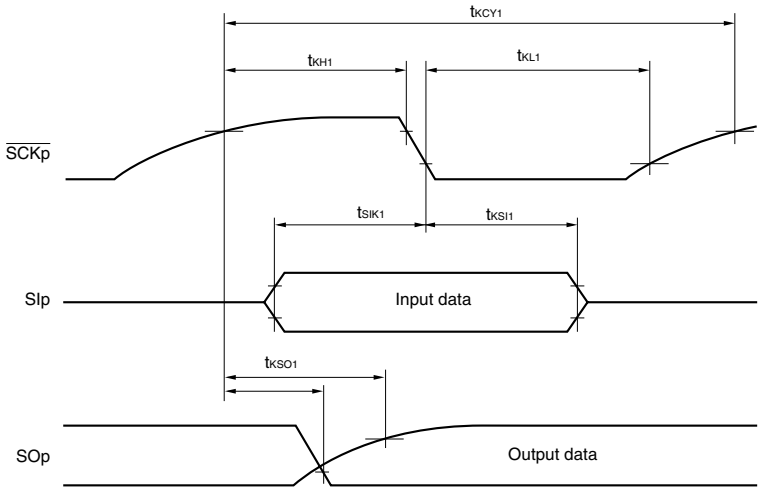
4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 01, 10, 20, 40, 41), g: PIM and POM number (g = 0, 1, 14)

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

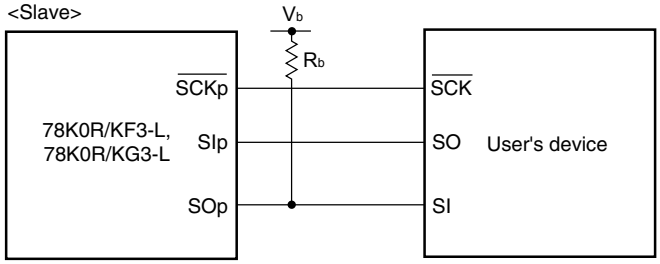
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	13.6 MHz < f_{MCK}	10/f_{MCK}			ns
			6.8 MHz < f_{MCK} ≤ 13.6 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 6.8 MHz	6/f_{MCK}			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	18.5 MHz < f_{MCK}	16/f_{MCK}			ns
			14.8 MHz < f_{MCK} ≤ 18.5 MHz	14/f_{MCK}			ns
			11.1 MHz < f_{MCK} ≤ 14.8 MHz	12/f_{MCK}			ns
			7.4 MHz < f_{MCK} ≤ 11.1 MHz	10/f_{MCK}			ns
			3.7 MHz < f_{MCK} ≤ 7.4 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 3.7 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 – 20			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 35			ns
SIp setup time (to $\overline{SCKp}$↑) Note 1	t_{SIK2}			90			ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI2}			1/f_{MCK} + 50			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 3	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 230	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

CSI mode connection diagram (during communication at different potential)



(**Caution** and **Remark** are given on the next page.)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Caution Select the TTL input buffer for the SIp pin and $\overline{SCKp}$ pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 01, 10, 20, 40, 41), g: PIM and POM number (g = 0, 1, 14)

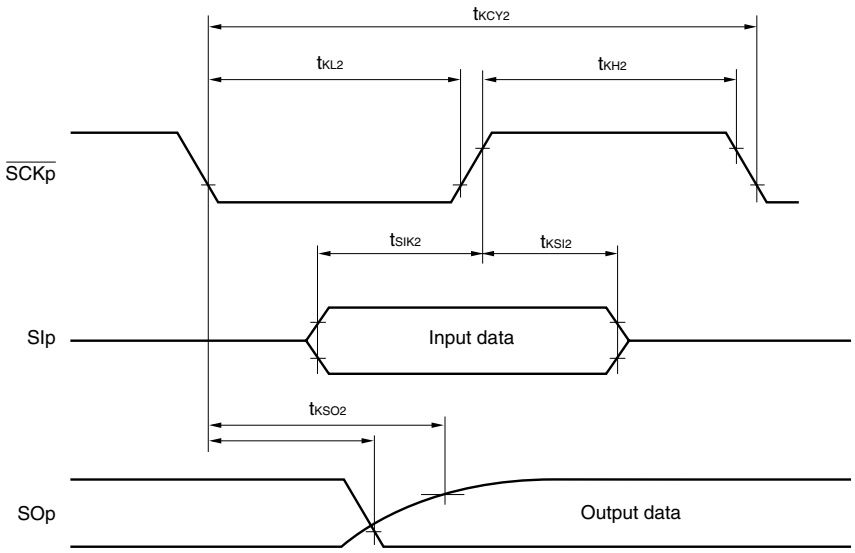
2. R_b[Ω]:Communication line (SOp) pull-up resistance,
C_b[F]: Communication line (SOp, $\overline{SCKp}$) load capacitance, V_b[V]: Communication line voltage

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2))

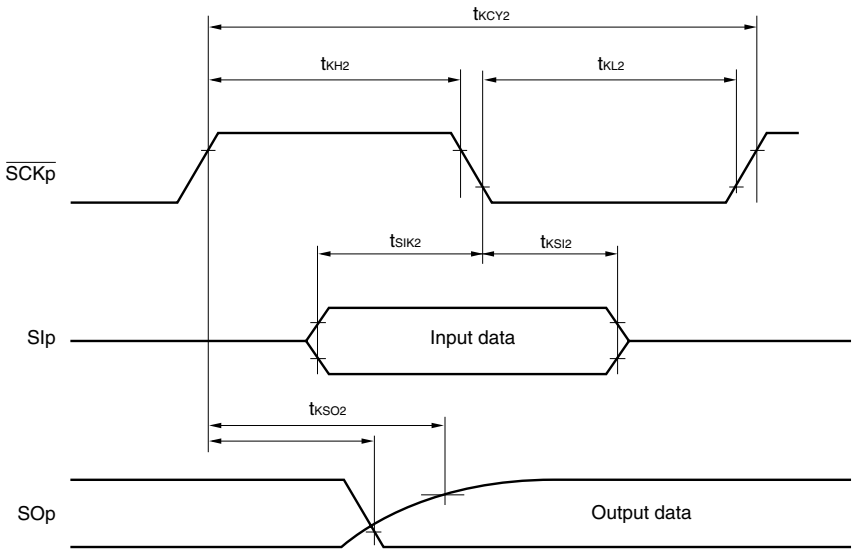
4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.
$4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$: $V_{IH} = 2.2\ V$, $V_{IL} = 0.8\ V$
$2.7\ V \le V_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$: $V_{IH} = 2.0\ V$, $V_{IL} = 0.5\ V$

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and $\overline{\text{SCKp}}$ pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 01, 10, 20, 40, 41), g: PIM and POM number (g = 0, 1, 14)

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(8) Communication at different potential (2.5 V, 3 V) (simplified I^2C mode)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ		400 Note	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note	kHz
Hold time when SCLr = “L”	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	1275		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1275		ns
Hold time when SCLr = “H”	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	655		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	655		ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	1/f_{MCK} + 190		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	0	640	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	660	ns

Note The value must also be f_{MCK}/4 or more.

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance,
C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

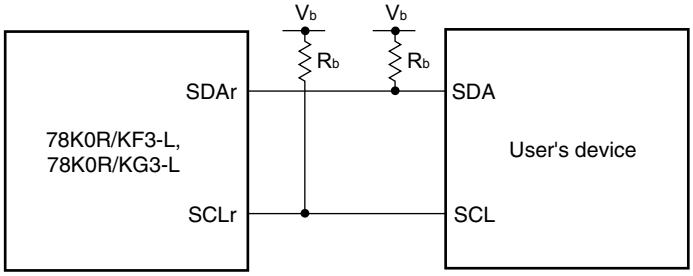
2. r: IIC number (r = 10, 20), g: PIM, POM number (g = 0, 14)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 02, 10)

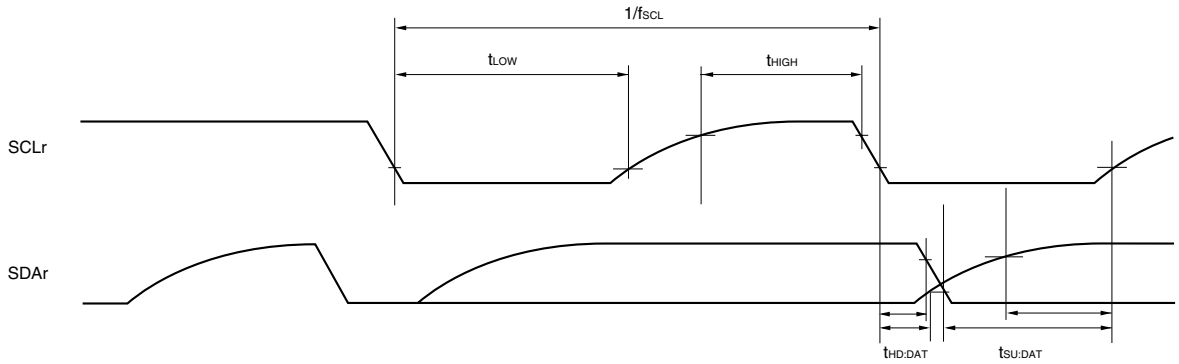
4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified I^2C mode mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, V_b[V]: Communication line voltage

2. r: IIC number (r = 10, 20), g: PIM and POM number (g = 0, 14)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.6.2 Serial interface IICA

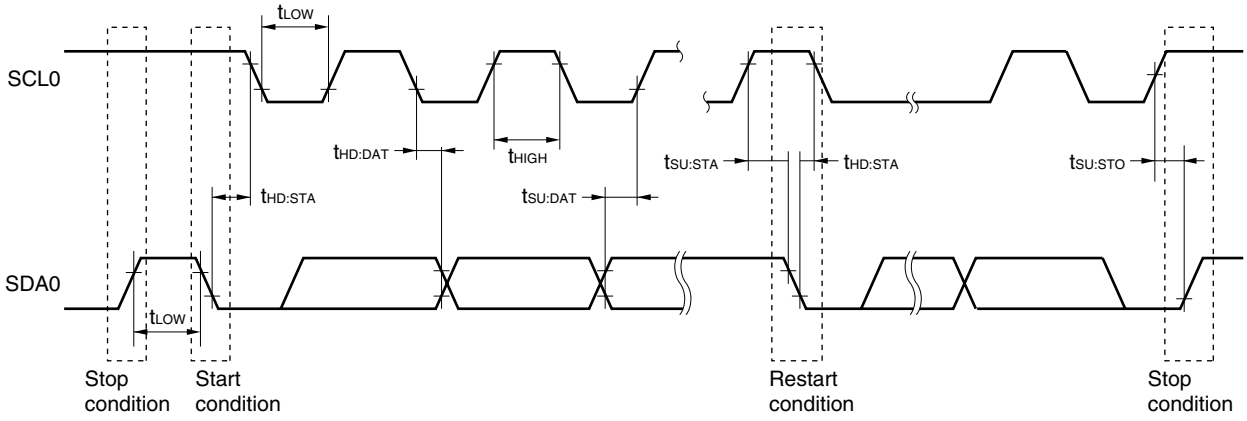
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{SCL}	High speed mode: f_{CLK} ≥ 3.5 MHz Normal mode: f_{CLK} ≥ 1 MHz	0	100	0	400	kHz
Setup time of restart condition[Note 1]	$t_{SU:STA}$		4.7		0.6		μs
Hold time	$t_{HD:STA}$		4.0		0.6		μs
Hold time when SCL0 = "L"	t_{LOW}		4.7		1.3		μs
Hold time when SCL0 = "H"	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		μs
Bus-free time	t_{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

IICA serial transfer timing



31.6.3 On-chip debug (UART)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			$f_{CLK}/2^{12}$		$f_{CLK}/6$	bps
		Flash memory programming mode			3.33	Mbps
TOOL1 output frequency	f_{TOOL1}	2.7 V ≤ V_{DD} ≤ 5.5 V			10	MHz
		1.8 V ≤ V_{DD} < 2.7 V			2.5	MHz

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.6.4 A/D converter characteristics

A/D Converter Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}					10	bit
Overall error[Notes 1, 2]	AINL					±0.35	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	High speed mode 1	2.5		66.6	μs
			Normal mode	5.2		66.6	μs
		2.7 V ≤ AV_{REF} ≤ 5.5 V	High speed mode 2	3.5		66.6	μs
			Normal mode	8.6		66.6	μs
		1.8 V ≤ AV_{REF} ≤ 4.0 V	Low voltage mode	24.1		66.6	μs
Zero-scale error[Notes 1, 2]	EZS					±0.25	%FSR
Full-scale error[Notes 1, 2]	EFS					±0.25	%FSR
Integral linearity error[Note 1]	ILE					±2.5	LSB
Differential linearity error[Note 1]	DLE					±1.5	LSB
Analog input voltage	V_{AIN}	1.8 V ≤ AV_{REF} ≤ 5.5 V		AV_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

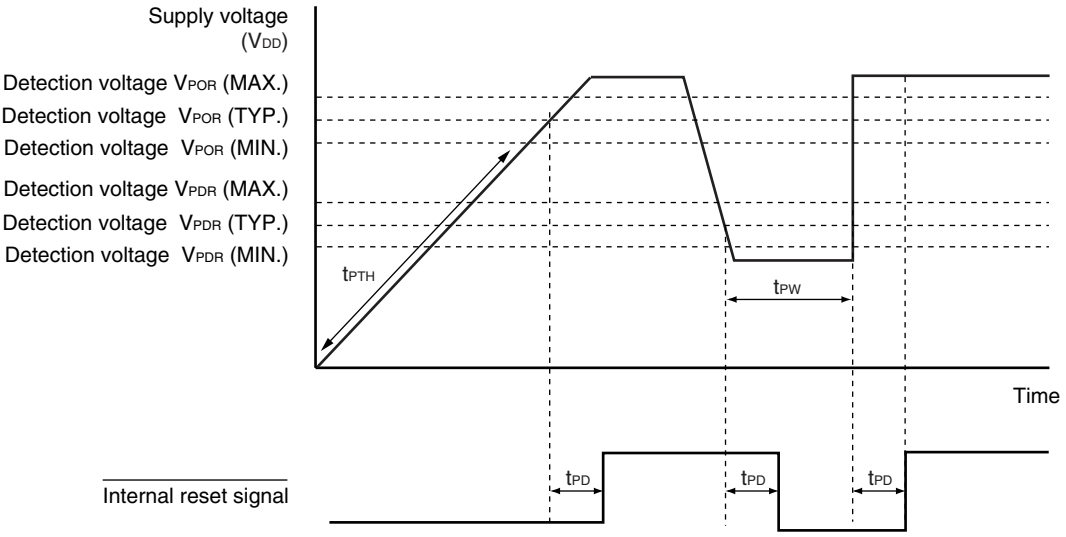
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.6.5 POC circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.52	1.61	1.70	V
	V_{PDR}	Power supply fall time	1.50	1.59	1.68	V
Power supply voltage rise inclination	t_{PTH}	Change inclination of V_{DD}: 0 V → V_{POR}	0.5			V/ms
Minimum pulse width	t_{PW}	When the voltage drops	200			μs
Detection delay time	t_{PD}				200	μs

POC Circuit Timing



Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.6.6 Supply voltage rise time

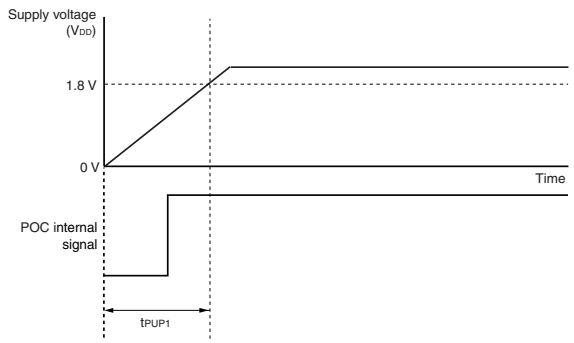
(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.8 V (V_{DD} (MIN.))[Note] (V_{DD}: 0 V → 1.8 V)	t_{PUP1}	LVI default start function stopped is set (LVIOFF (Option Byte) = 1), when $\overline{\text{RESET}}$ input is not used			3.6	ms
Maximum time to rise to 1.8 V (V_{DD} (MIN.))[Note] (releasing $\overline{\text{RESET}}$ input → V_{DD}: 1.8 V)	t_{PUP2}	LVI default start function stopped is set (LVIOFF (Option Byte) = 1), when $\overline{\text{RESET}}$ input is used			1.88	ms

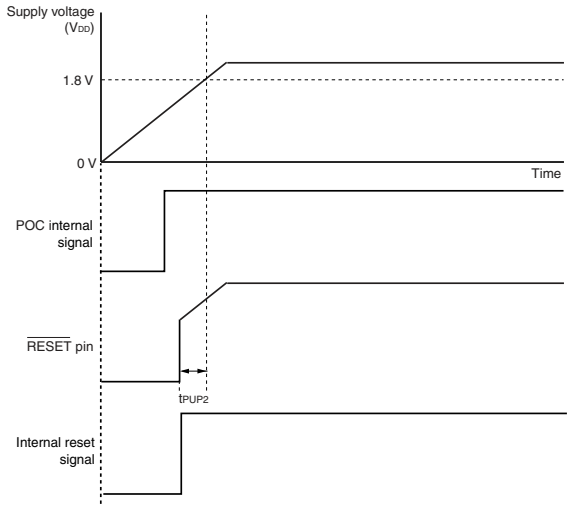
Note Make sure to raise the power supply in a shorter time than this.

Supply Voltage Rise Time Timing

• When the $\overline{\text{RESET}}$ pin input is not used



• When the $\overline{\text{RESET}}$ pin input is used (when external reset is released by the $\overline{\text{RESET}}$ pin, after POC has been released)



Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.6.7 LVI circuit characteristics

(T_A = –40 to +85°C, $V_{PDR} \le V_{DD} = EV_{DD0} = EV_{DD1} \le 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

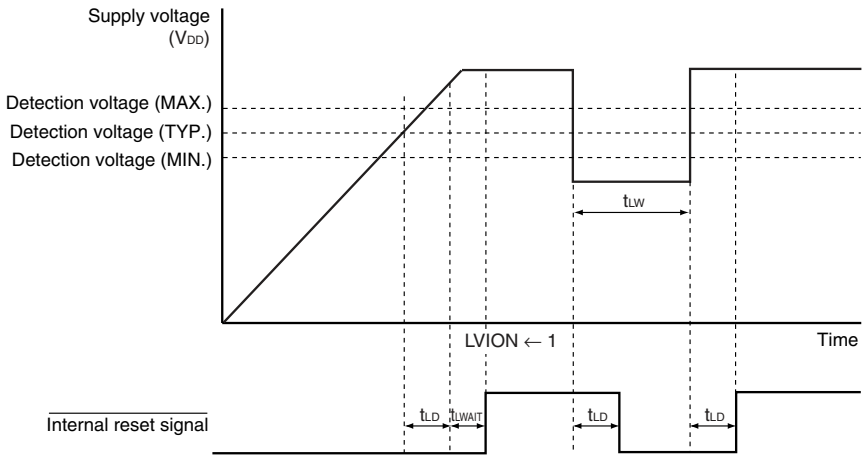
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.12	4.22	4.32	V
		V_{LVI1}		3.97	4.07	4.17	V
		V_{LVI2}		3.82	3.92	4.02	V
		V_{LVI3}		3.66	3.76	3.86	V
		V_{LVI4}		3.51	3.61	3.71	V
		V_{LVI5}		3.35	3.45	3.55	V
		V_{LVI6}		3.20	3.30	3.40	V
		V_{LVI7}		3.05	3.15	3.25	V
		V_{LVI8}		2.89	2.99	3.09	V
		V_{LVI9}		2.74	2.84	2.94	V
		V_{LVI10}		2.58	2.68	2.78	V
		V_{LVI11}		2.43	2.53	2.63	V
		V_{LVI12}		2.28	2.38	2.48	V
		V_{LVI13}		2.12	2.22	2.32	V
		V_{LVI14}		1.97	2.07	2.17	V
		V_{LVI15}		1.81	1.91	2.01	V
	External input pin[Note 1]	V_{EXLVI}	EXLVI < V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
	Power supply voltage on power application	V_{PUPLVI}	When LVI default start function enabled is set	1.87	2.07	2.27	V
Minimum pulse width		t_{LW}		200			μs
Detection delay time		t_{LD}				200	μs
Operation stabilization wait time[Note 2]		t_{LWAIT}				10	μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 15

LVI Circuit Timing



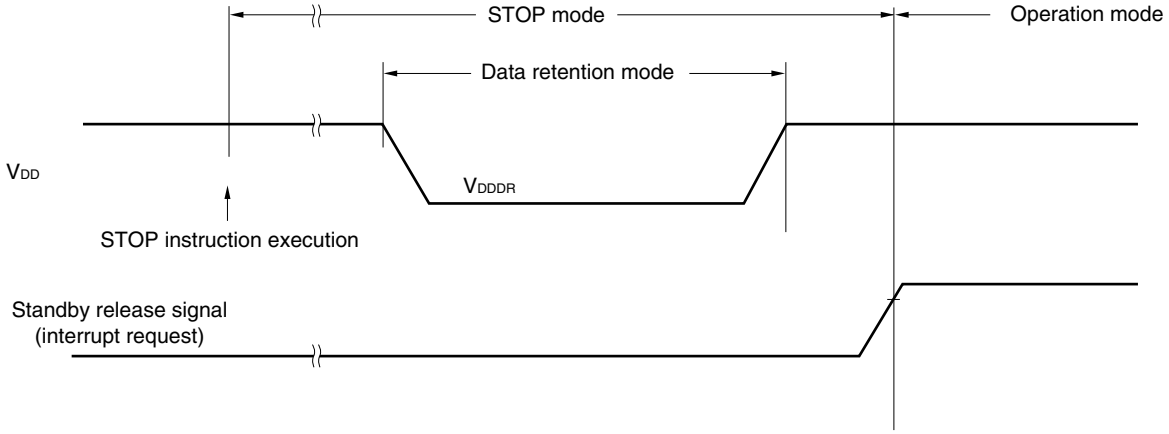
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.5[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained before a POC reset is effected, but data is not retained when a POC reset is effected.



31.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} supply current	I_{DD}	Typ. = 10 MHz, Max. = 20 MHz		6	20	mA
Number of rewrites (number of deletes per block)	C_{erwr}	Used for updating programs When using flash memory programmer and Renesas Electronics self programming library	Retained for 15 years	1,000		Times
		Used for updating data When using Renesas Electronics EEPROM emulation library (available ROM area: 3 to 8 KB of 3 to 8 continuous blocks)	Retained for 5 years	10,000		Times

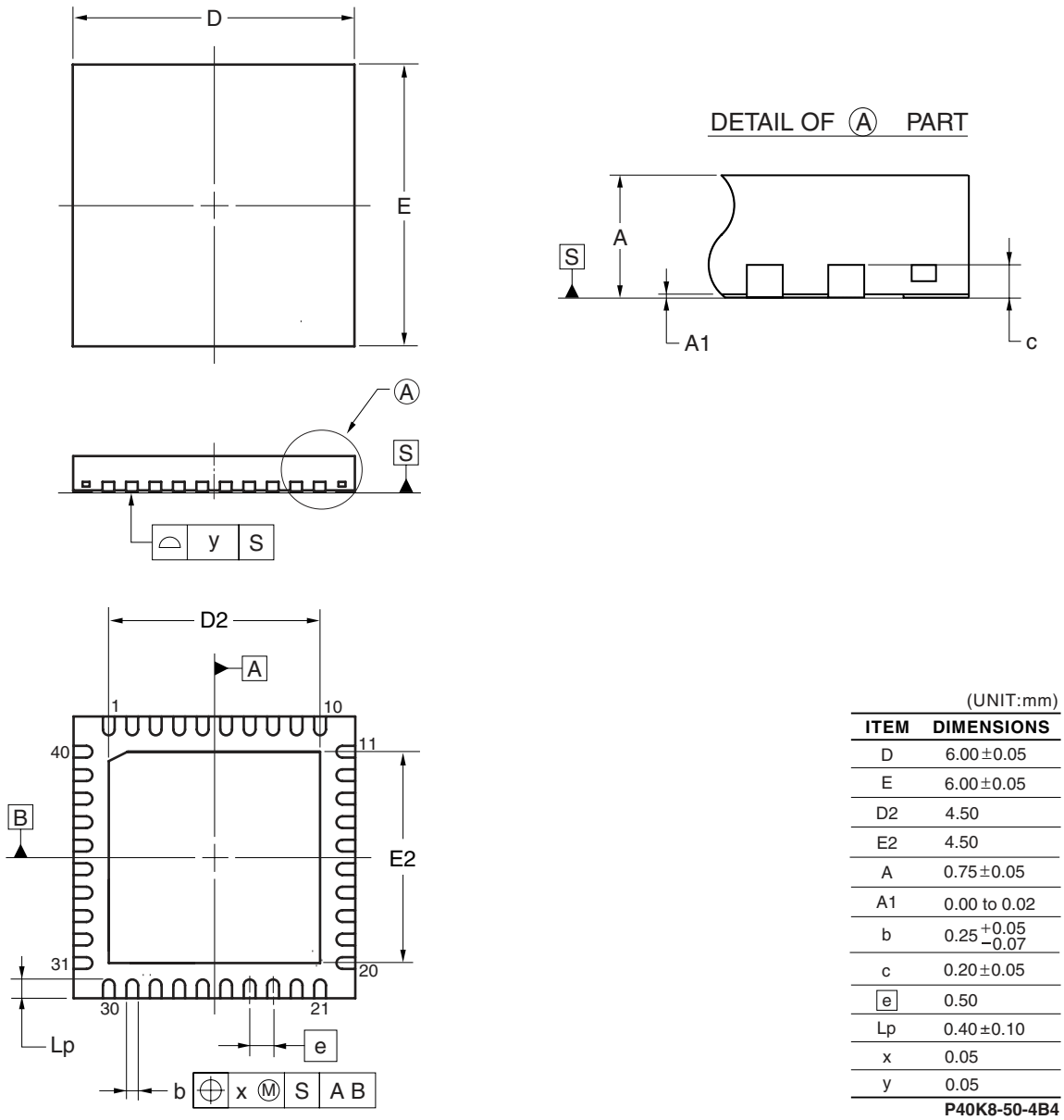
Remark When updating data multiple times, use the flash memory as one for updating data.

CHAPTER 32 PACKAGE DRAWINGS

32.1 78K0R/KC3-L (40-pin products)

μPD78F1000K8-4B4-AX, 78F1001K8-4B4-AX, 78F1002K8-4B4-AX, 78F1003K8-4B4-AX (Under development)

40-PIN PLASTIC WQFN(6x6)



(UNIT:mm)

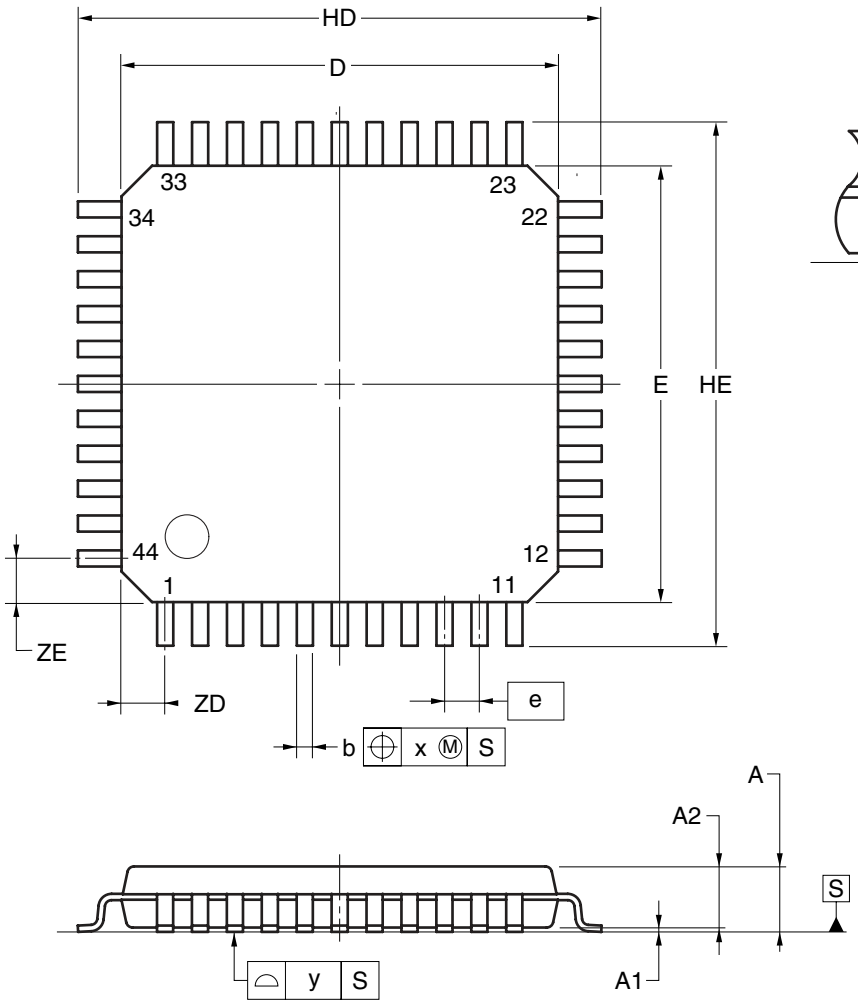
ITEM	DIMENSIONS
D	6.00±0.05
E	6.00±0.05
D2	4.50
E2	4.50
A	0.75±0.05
A1	0.00 to 0.02
b	$0.25^{+0.05}_{-0.07}$
c	0.20±0.05
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

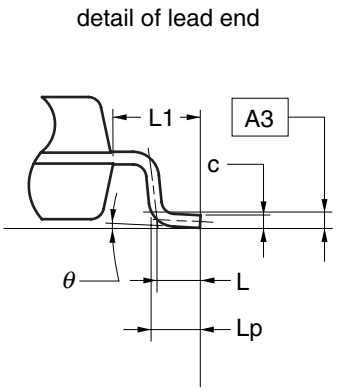
P40K8-50-4B4

32.2 78K0R/KC3-L (44-pin products)

μPD78F1000GB-GAF-AX, 78F1001GB-GAF-AX, 78F1002GB-GAF-AX, 78F1003GB-GAF-AX

44-PIN PLASTIC LQFP (10x10)





(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.35^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.80
x	0.20
y	0.10
ZD	1.00
ZE	1.00

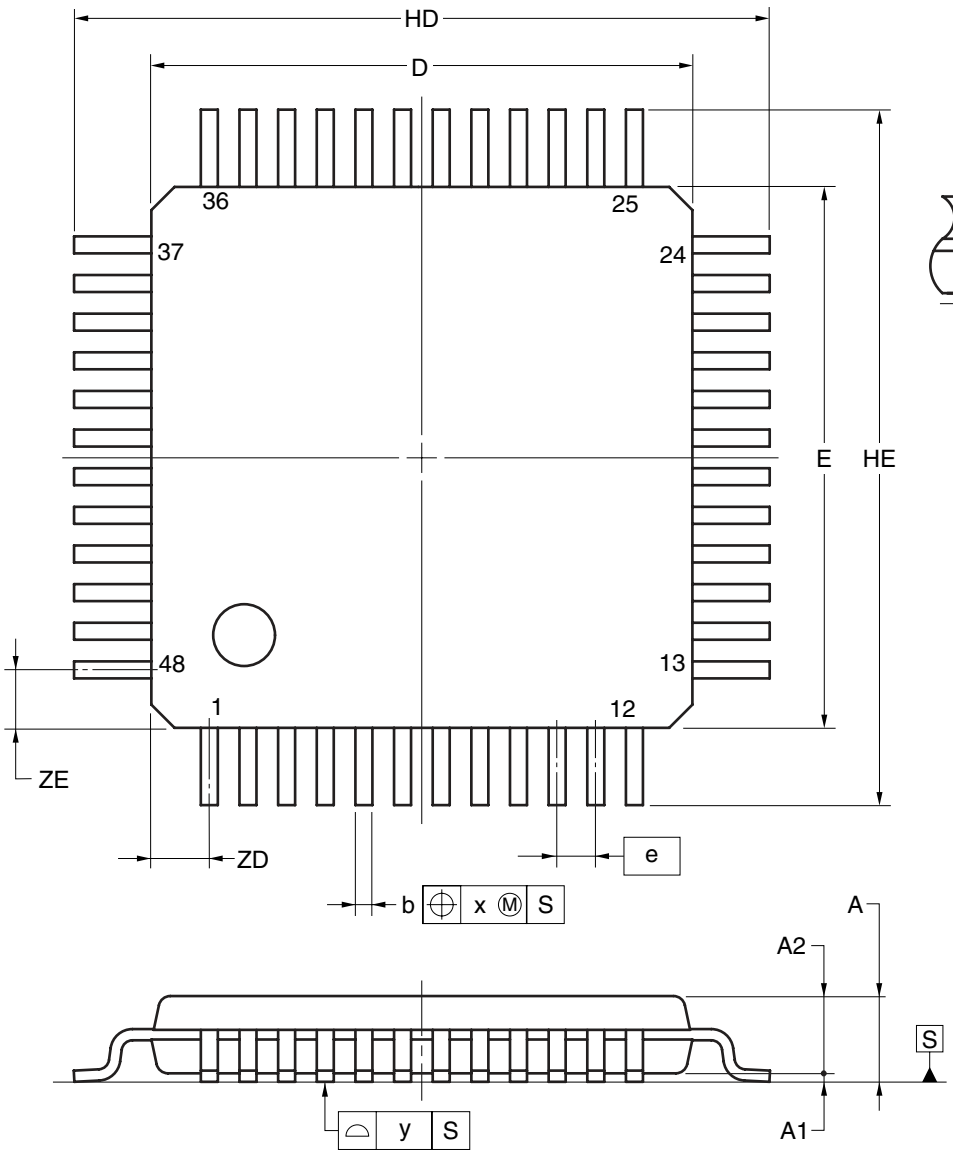
P44GB-80-GAF

NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

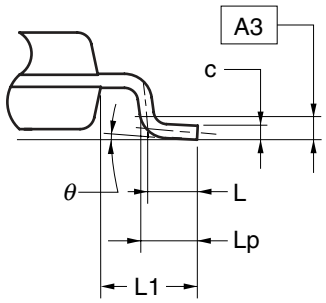
32.3 78K0R/KC3-L (48-pin products)

μPD78F1001GA-HAA-AX, 78F1002GA-HAA-AX, 78F1003GA-HAA-AX

48-PIN PLASTIC TQFP (FINE PITCH) (7x7)



detail of lead end



(UNIT:mm)

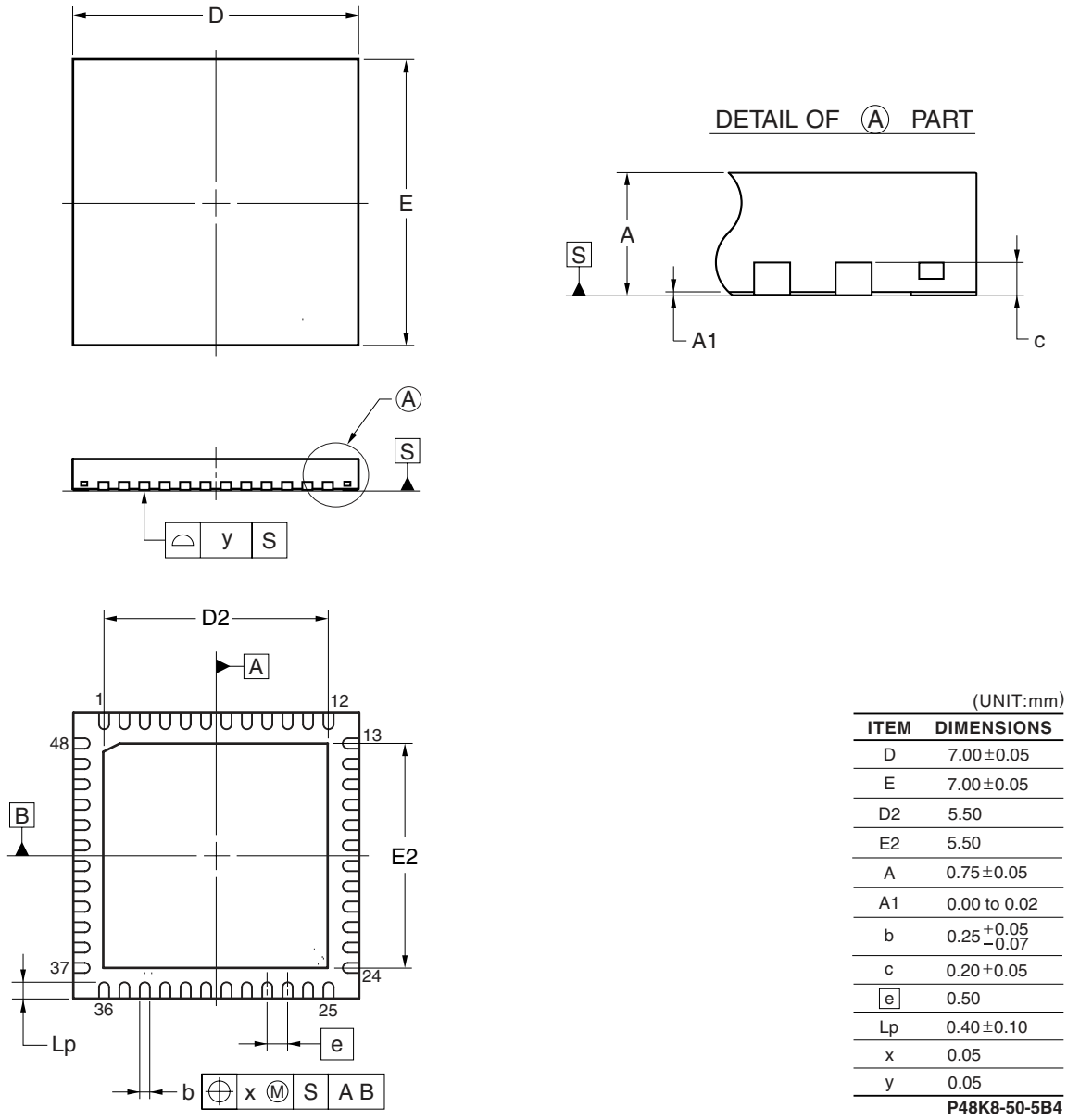
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.20 MAX.
A1	0.10±0.05
A2	1.00±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

P48GA-50-HAA

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

μPD78F1001K8-5B4-AX, 78F1002K8-5B4-AX, 78F1003K8-5B4-AX (Under development)

48-PIN PLASTIC WQFN(7x7)



(UNIT:mm)

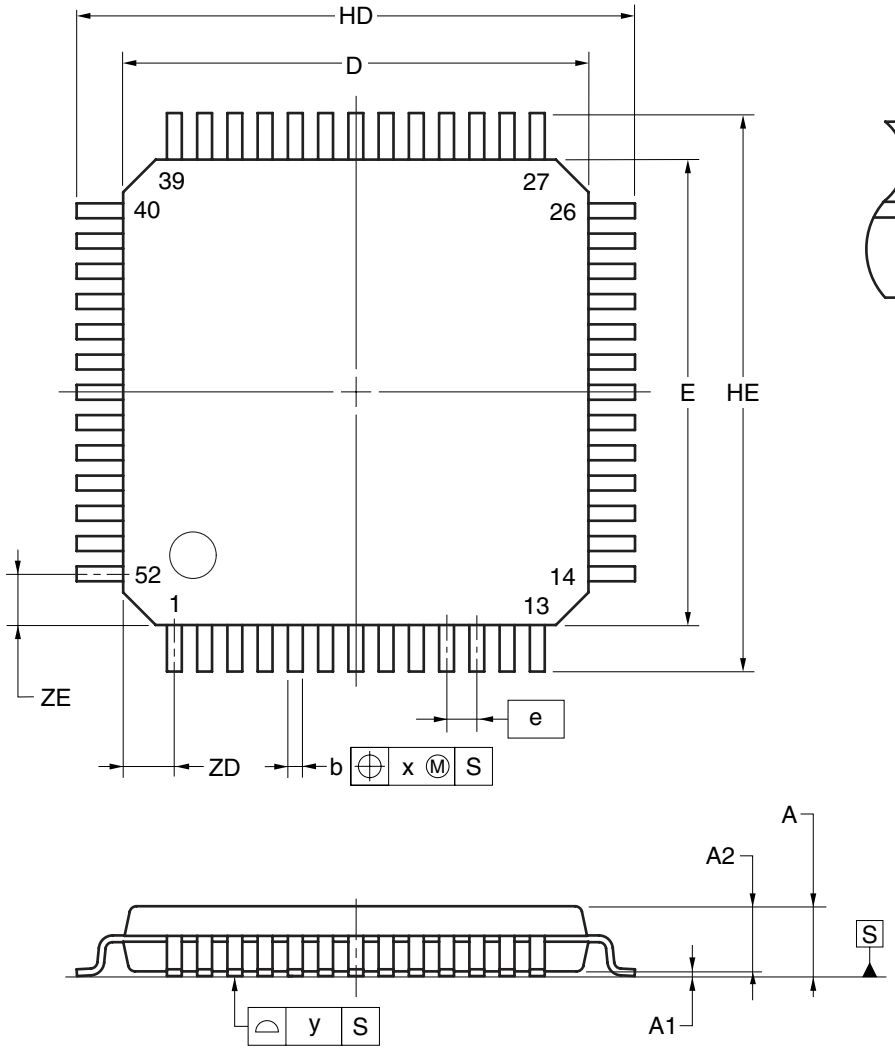
ITEM	DIMENSIONS
D	7.00±0.05
E	7.00±0.05
D2	5.50
E2	5.50
A	0.75±0.05
A1	0.00 to 0.02
b	$0.25^{+0.05}_{-0.07}$
c	0.20±0.05
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

P48K8-50-5B4

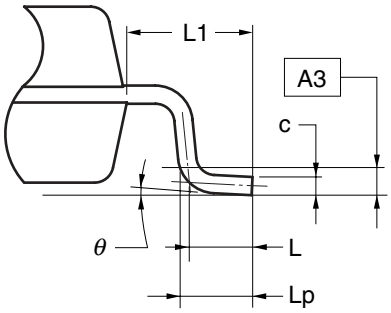
32.4 78K0R/KD3-L

μPD78F1004GB-GAG-AX, 78F1005GB-GAG-AX, 78F1006GB-GAG-AX

52-PIN PLASTIC LQFP (10x10)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.30^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.10
ZE	1.10

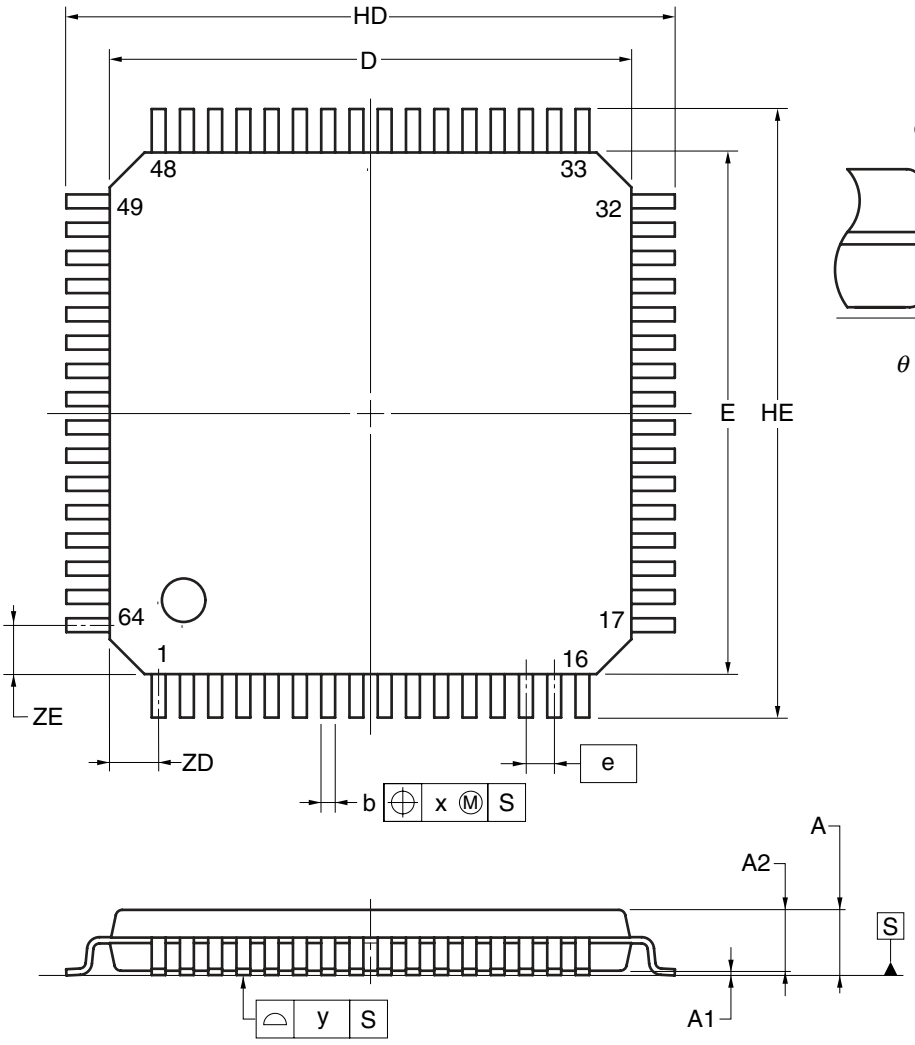
P52GB-65-GAG

NOTE
Each lead centerline is located within 0.13mm of its true position at maximum material condition.

32.5 78K0R/KE3-L

μPD78F1007GK-GAJ-AX, 78F1008GK-GAJ-AX, 78F1009GK-GAJ-AX

64-PIN PLASTIC LQFP (12x12)



(UNIT:mm)

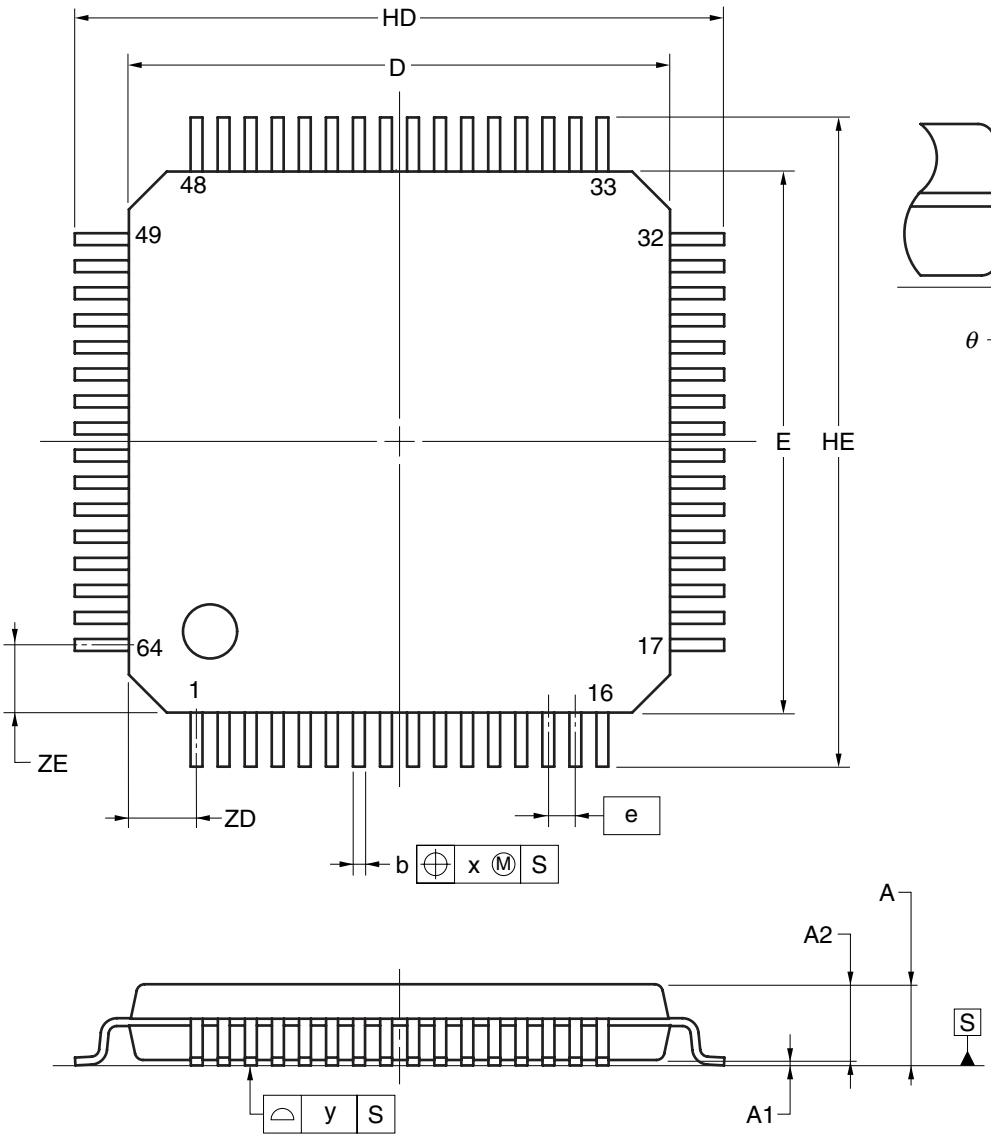
ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.30^{+0.08}_{-0.04}$
c	$0.125^{+0.75}_{-0.25}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125

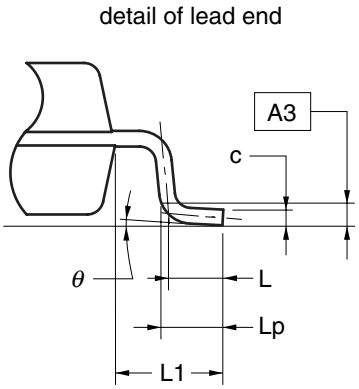
P64GK-65-GAJ

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

μPD78F1007GB-GAH-AX, 78F1008GB-GAH-AX, 78F1009GB-GAH-AX

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)





(UNIT:mm)

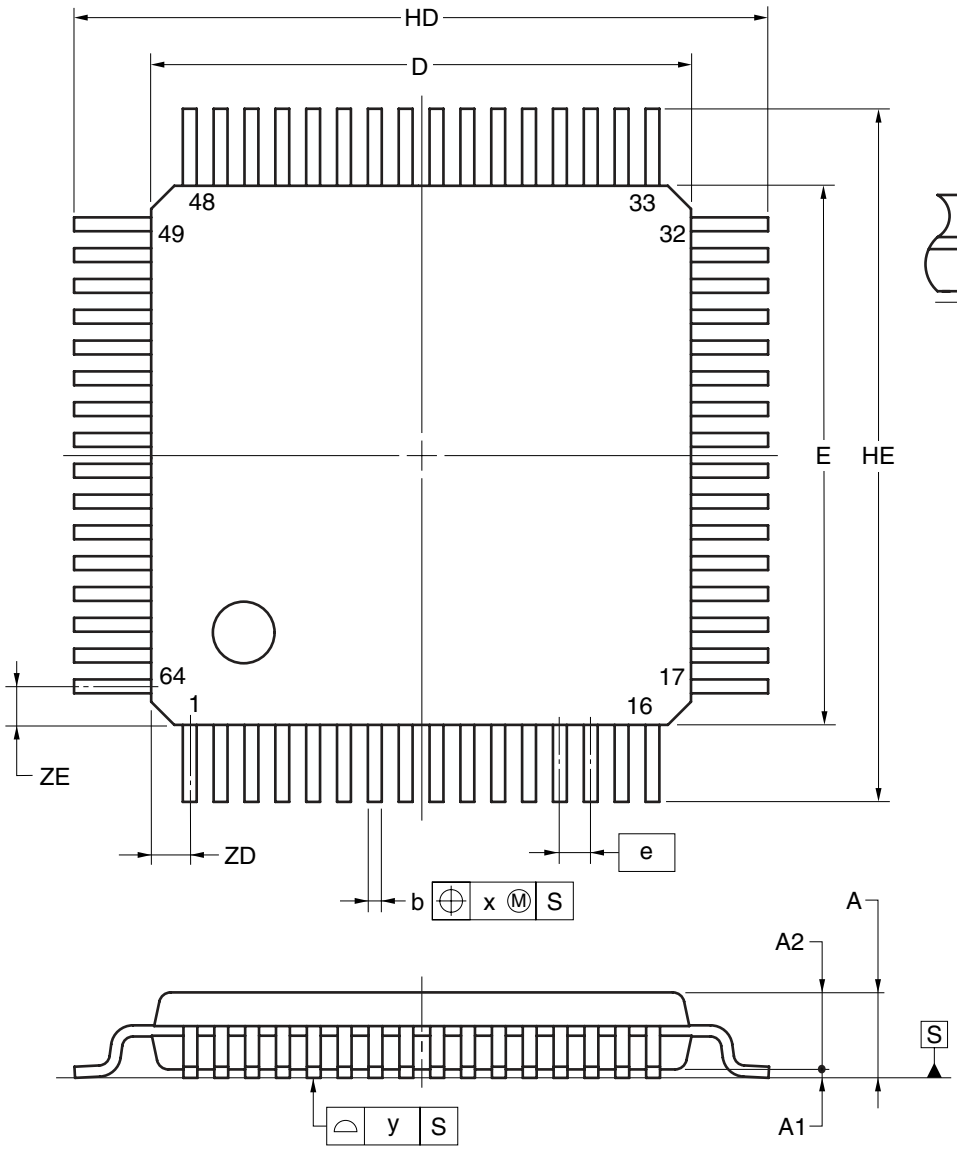
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P64GB-50-GAH

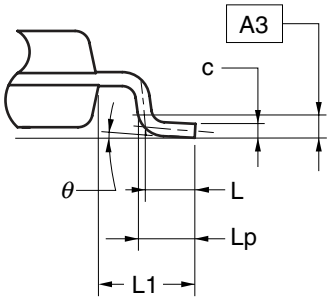
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

μPD78F1007GA-HAB-AX, 78F1008GA-HAB-AX, 78F1009GA-HAB-AX

64-PIN PLASTIC TQFP (FINE PITCH) (7x7)



detail of lead end



(UNIT:mm)

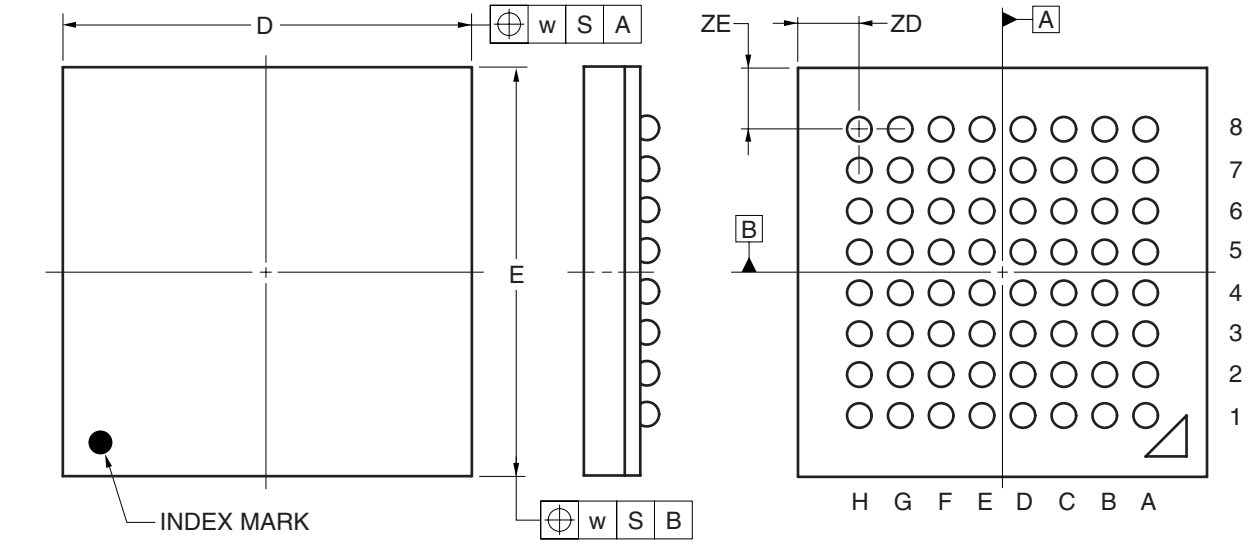
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.20 MAX.
A1	0.10±0.05
A2	1.00±0.05
A3	0.25
b	$0.16^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.40
x	0.07
y	0.08
ZD	0.50
ZE	0.50

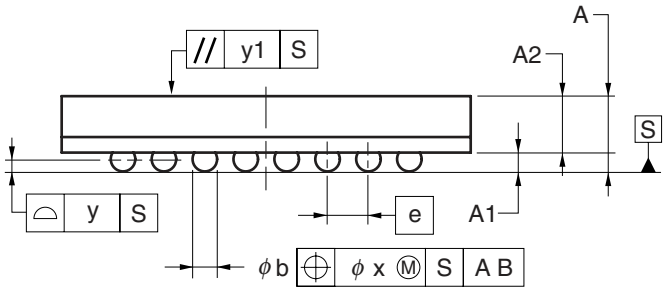
P64GA-40-HAB

NOTE
Each lead centerline is located within 0.07mm of its true position at maximum material condition.

μPD78F1007F1-AN1-A, 78F1008F1-AN1-A, 78F1009F1-AN1-A

64-PIN PLASTIC FBGA (5x5)





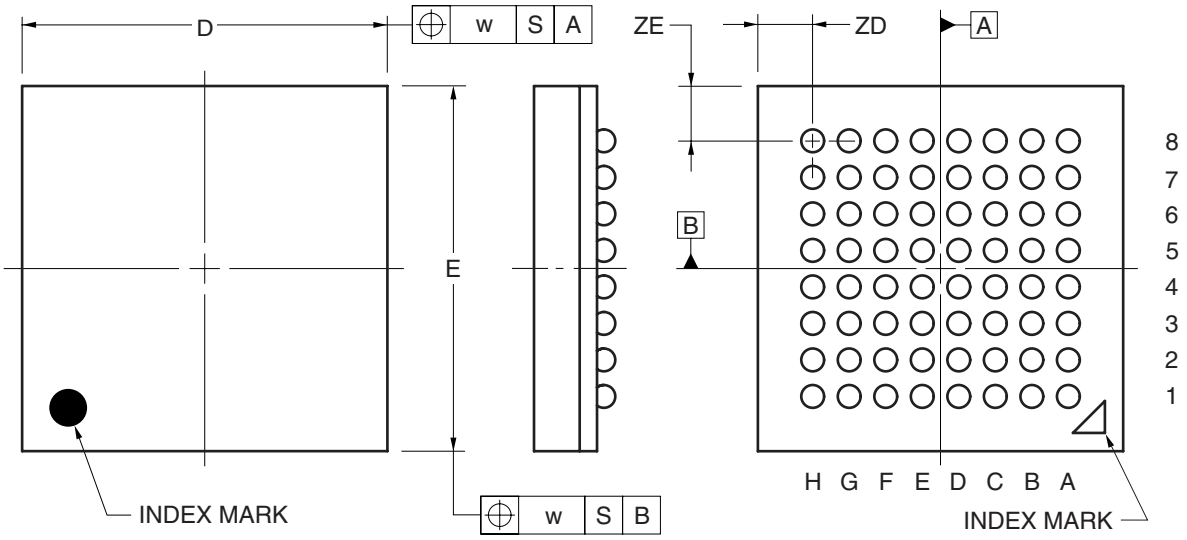
(UNIT:mm)

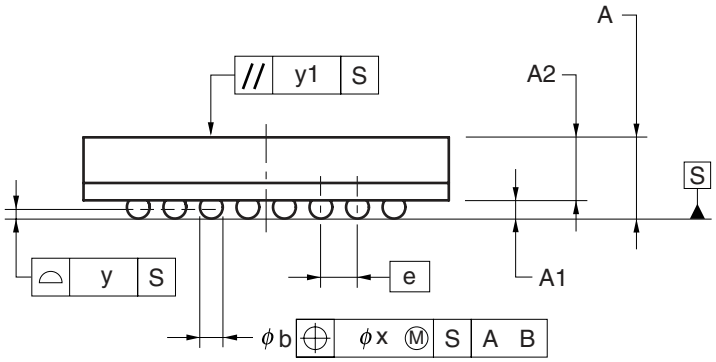
ITEM	DIMENSIONS
D	5.00±0.10
E	5.00±0.10
w	0.20
A	0.90±0.10
A1	0.21±0.05
A2	0.69
e	0.50
b	0.32±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P64F1-50-AN1

μPD78F1007F1-AA2-A, 78F1008F1-AA2-A, 78F1009F1-AA2-A

64-PIN PLASTIC FBGA (4x4)





(UNIT:mm)

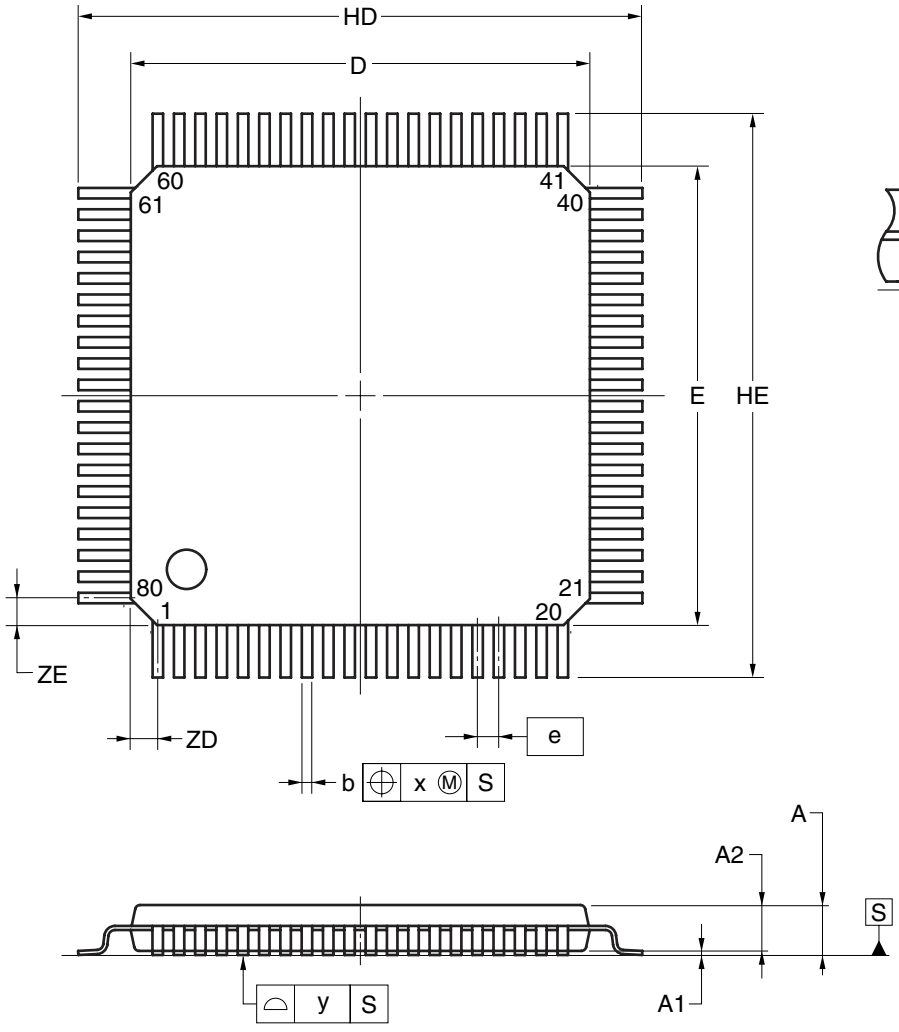
ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.15
A	0.89±0.10
A1	0.20±0.05
A2	0.69
e	0.40
b	0.25±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60

P64F1-40-AA2

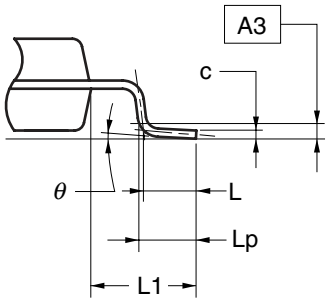
32.6 78K0R/KF3-L

μPD78F1010GC-GAD-AX, 78F1011GC-GAD-AX, 78F1012GC-GAD-AX, 78F1027GC-GAD-AX, 78F1028GC-GAD-AX

80-PIN PLASTIC LQFP (14x14)



detail of lead end



(UNIT:mm)

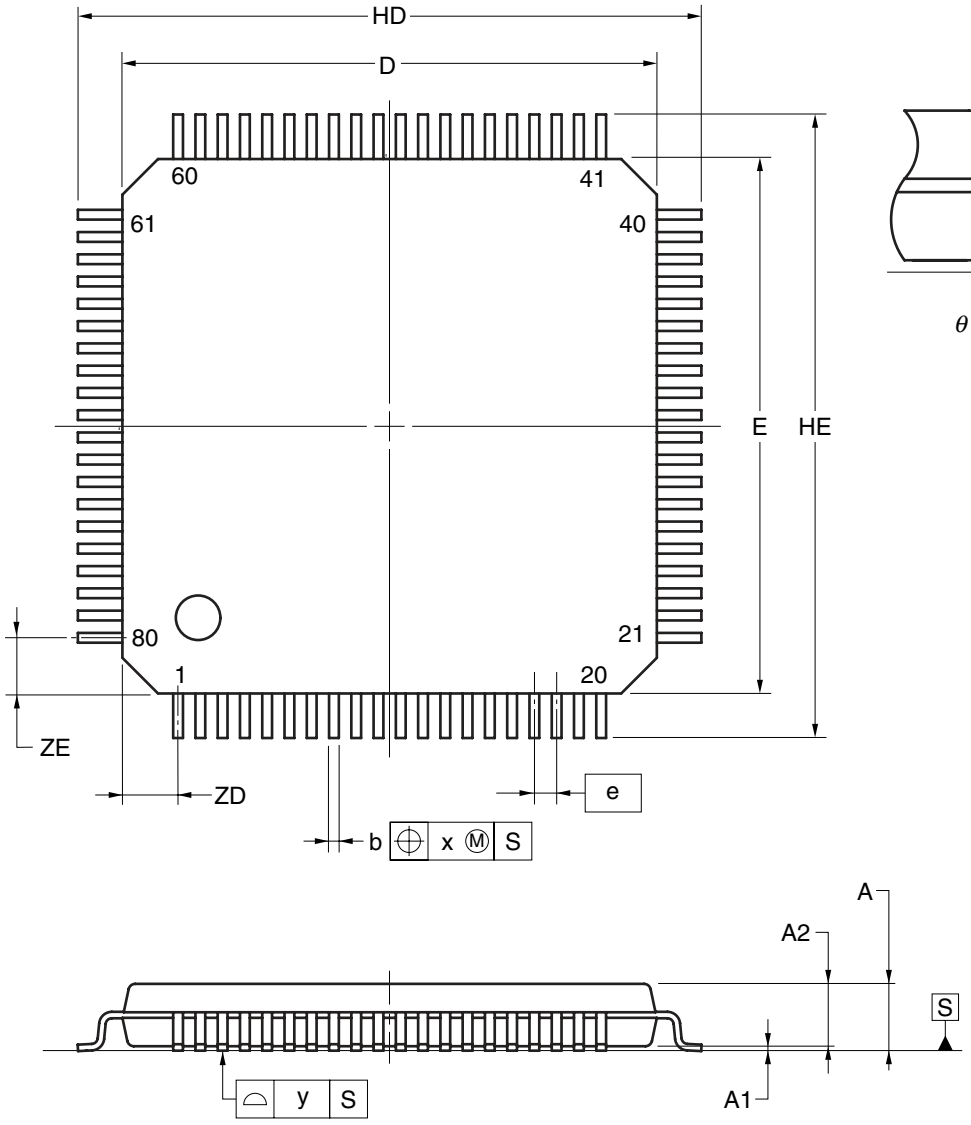
ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	17.20±0.20
HE	17.20±0.20
A	1.70 MAX.
A1	0.125±0.075
A2	1.40±0.05
A3	0.25
b	$0.30^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.80
Lp	0.886±0.15
L1	1.60±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	0.825
ZE	0.825

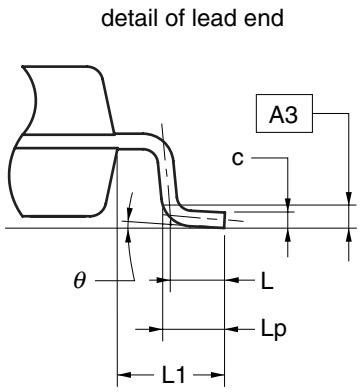
P80GC-65-GAD

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

μPD78F1010GK-GAK-AX, 78F1011GK-GAK-AX, 78F1012GK-GAK-AX, 78F1027GK-GAK-AX, 78F1028GK-GAK-AX

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)





(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

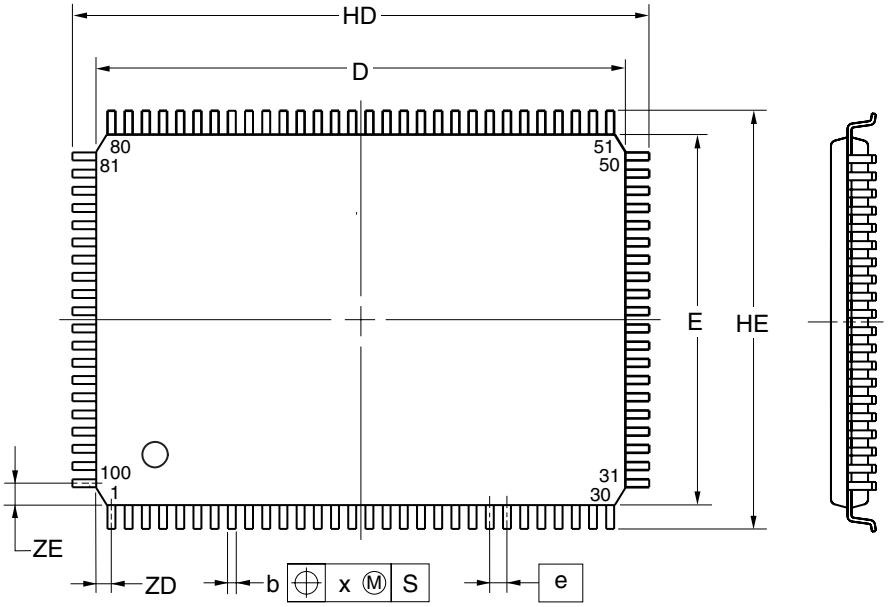
P80GK-50-GAK

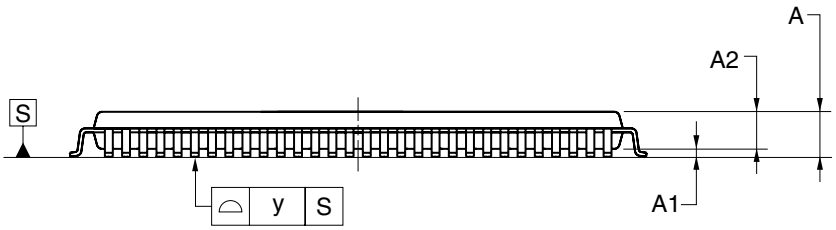
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

32.7 78K0R/KG3-L

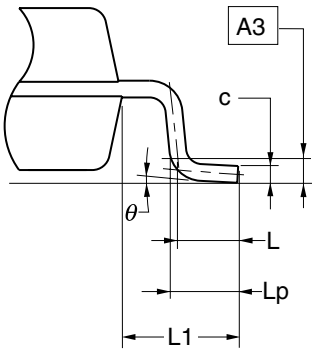
μPD78F1013GF-GAS-AX, 78F1014GF-GAS-AX, 78F1029GF-GAS-AX, 78F1030GF-GAS-AX

100-PIN PLASTIC LQFP (14x20)





detail of lead end



(UNIT:mm)

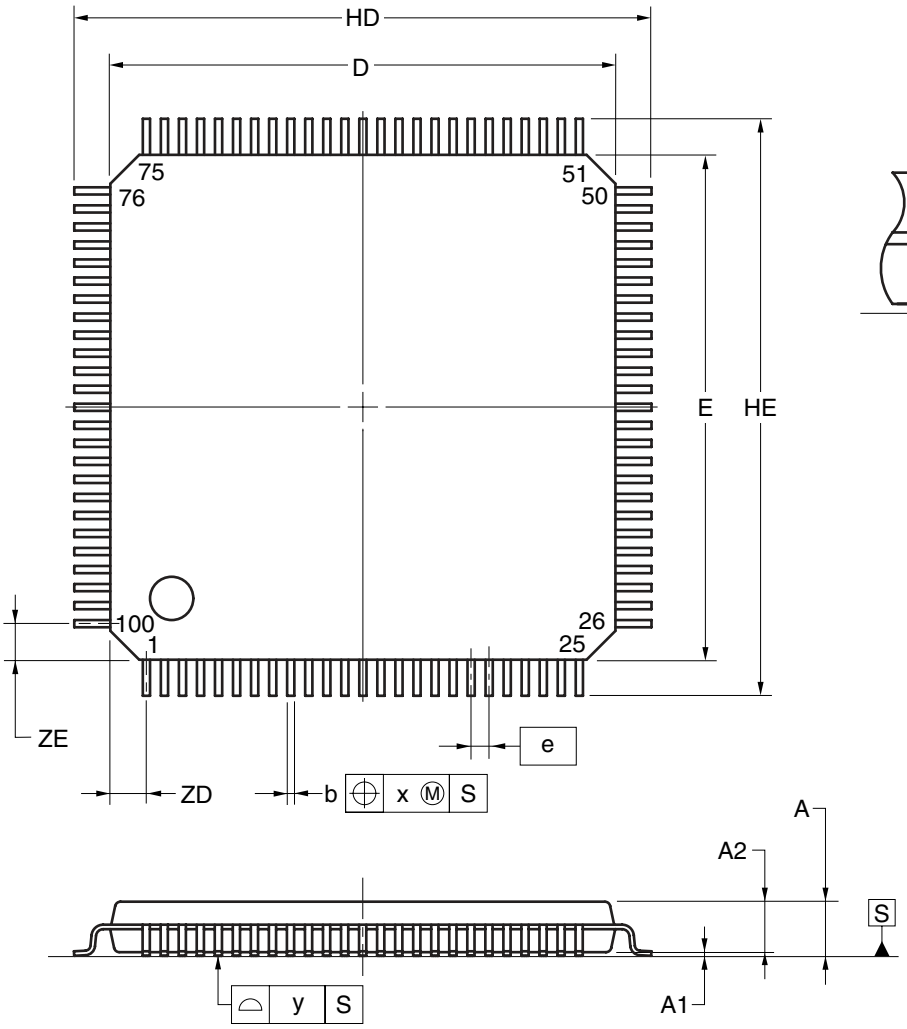
ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.30^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	0.575
ZE	0.825

P100GF-65-GAS

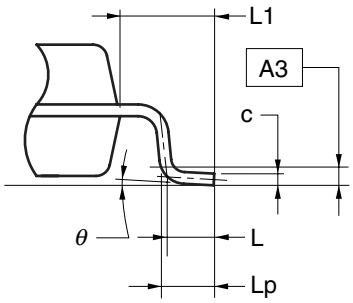
NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

μPD78F1013GC-UEU-AX, 78F1014GC-UEU-AX, 78F1029GC-UEU-AX, 78F1030GC-UEU-AX

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end



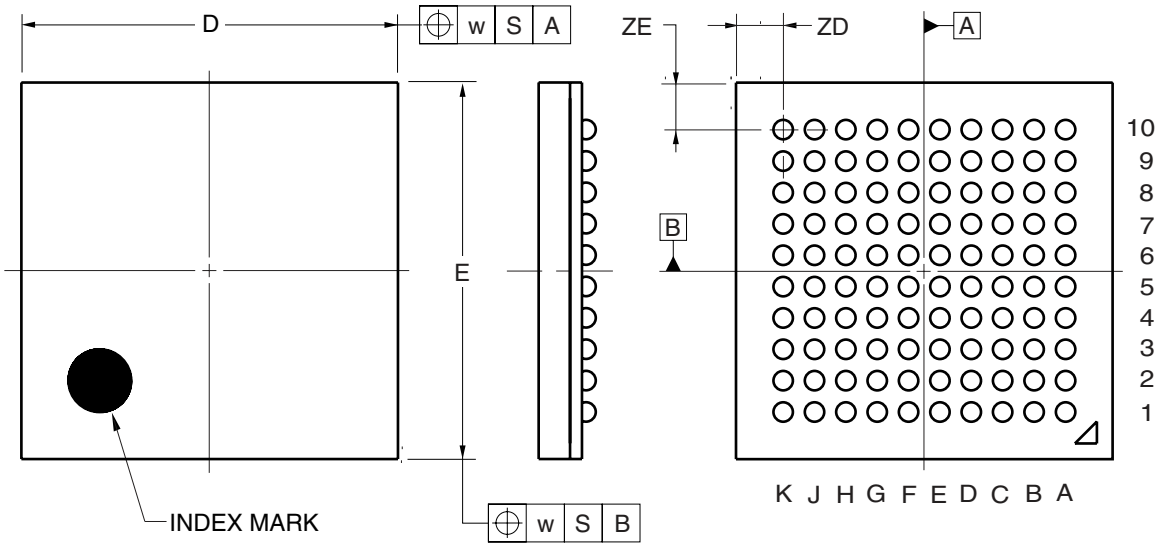
(UNIT:mm)

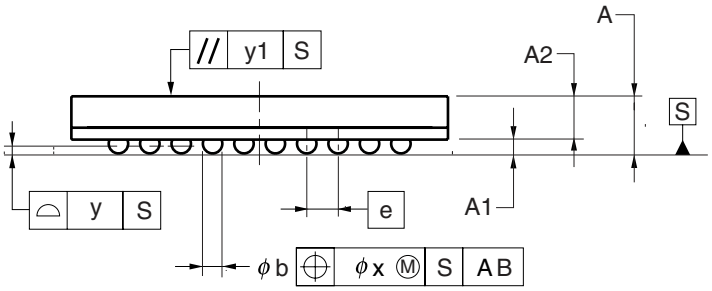
ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

P100GC-50-UEU-1

μPD78F1013F1-BAK-A, 78F1014F1-BAK-A

100-PIN PLASTIC FBGA (6x6)





(UNIT:mm)

ITEM	DIMENSIONS
D	6.00±0.10
E	6.00±0.10
w	0.20
A	0.91±0.10
A1	0.22±0.05
A2	0.69
e	0.50
b	0.31±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P100F1-50-BAK

CHAPTER 33 RECOMMENDED SOLDERING CONDITIONS

Cautions 1. Recommended soldering conditions about WQFN package of the 78K0R/KC3-L and 78K0R/KE3-L are under development.

2. For soldering methods and conditions other than those recommended below, contact an Renesas Electronics sales representative.

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an Renesas Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.renesas.com/prod/package/index.html) (under production)

Table 33-1. Surface Mounting Type Soldering Conditions (1/2)

- **44-pin plastic LQFP (10 × 10)**
  μPD78F1000GB-GAF-AX, μPD78F1001GB-GAF-AX, μPD78F1002GB-GAF-AX, μPD78F1003GB-GAF-AX
- **52-pin plastic LQFP (10 × 10)**
  μPD78F1004GB-GAG-AX, μPD78F1005GB-GAG-AX, μPD78F1006GB-GAG-AX
- **64-pin plastic LQFP (12 × 12)**
  μPD78F1007GK-GAJ-AX, μPD78F1008GK-GAJ-AX, μPD78F1009GK-GAJ-AXX
- **80-pin plastic LQFP (14 × 14)**
  μPD78F1010GC-GAD-AX, μPD78F1011GC-GAD-AX, μPD78F1012GC-GAD-AX,
  μPD78F1027GC-GAD-AX, μPD78F1028GC-GAD-AX
- **100-pin plastic LQFP (14 × 20)**
  μPD78F1013GF-GAS-AX, μPD78F1014GF-GAS-AX, μPD78F1029GF-GAS-AX, μPD78F1030GF-GAS-AX

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR60-107-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	WS60-107-1
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Table 33-1. Surface Mounting Type Soldering Conditions (2/2)

- **48-pin plastic TQFP (fine pitch) (7 × 7)**
  μPD78F1001GA-HAA-AX, μPD78F1002GA-HAA-AX, μPD78F1003GA-HAA-AX
- **64-pin plastic LQFP (fine pitch) (10 × 10)**
  μPD78F1007GB-GAH-AX, μPD78F1008GB-GAH-AX, μPD78F1009GB-GAH-AX
- **64-pin plastic TQFP (fine pitch) (7 × 7)**
  μPD78F1007GA-HAB-AX, μPD78F1008GA-HAB-AX, μPD78F1009GA-HAB-AX
- **80-pin plastic LQFP (fine pitch) (12 × 12)**
  μPD78F1010GK-GAK-AX, μPD78F1011GK-GAK-AX, μPD78F1012GK-GAK-AX,
  μPD78F1027GK-GAK-AX, μPD78F1028GK-GAK-AX
- **100-pin plastic LQFP (fine pitch) (14 × 14)**
  μPD78F1013GC-UEU-AX, μPD78F1014GC-UEU-AX, μPD78F1029GC-UEU-AX, μPD78F1030GC-UEU-AX

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR60-107-3
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

- **64-pin plastic FBGA (5 × 5)**
  μPD78F1007F1-AN1-A, μPD78F1008F1-AN1-A, μPD78F1009F1-AN1-A
- **64-pin plastic FBGA (4 × 4)**
  μPD78F1007F1-AA2-A, μPD78F1008F1-AA2-A, μPD78F1009F1-AA2-A
- **100-pin plastic FBGA (6 × 6)** [Note 1]
  μPD78F1013F1-BAK-A, μPD78F1041F1-BAK-A

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 7 days[Note 2] (after that, prebake at 125°C for 10 to 72 hours)	IR60-107-3

Notes 1. The μPD78F1029 and μPD78F1030 don't have the FBGA package.

2. After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

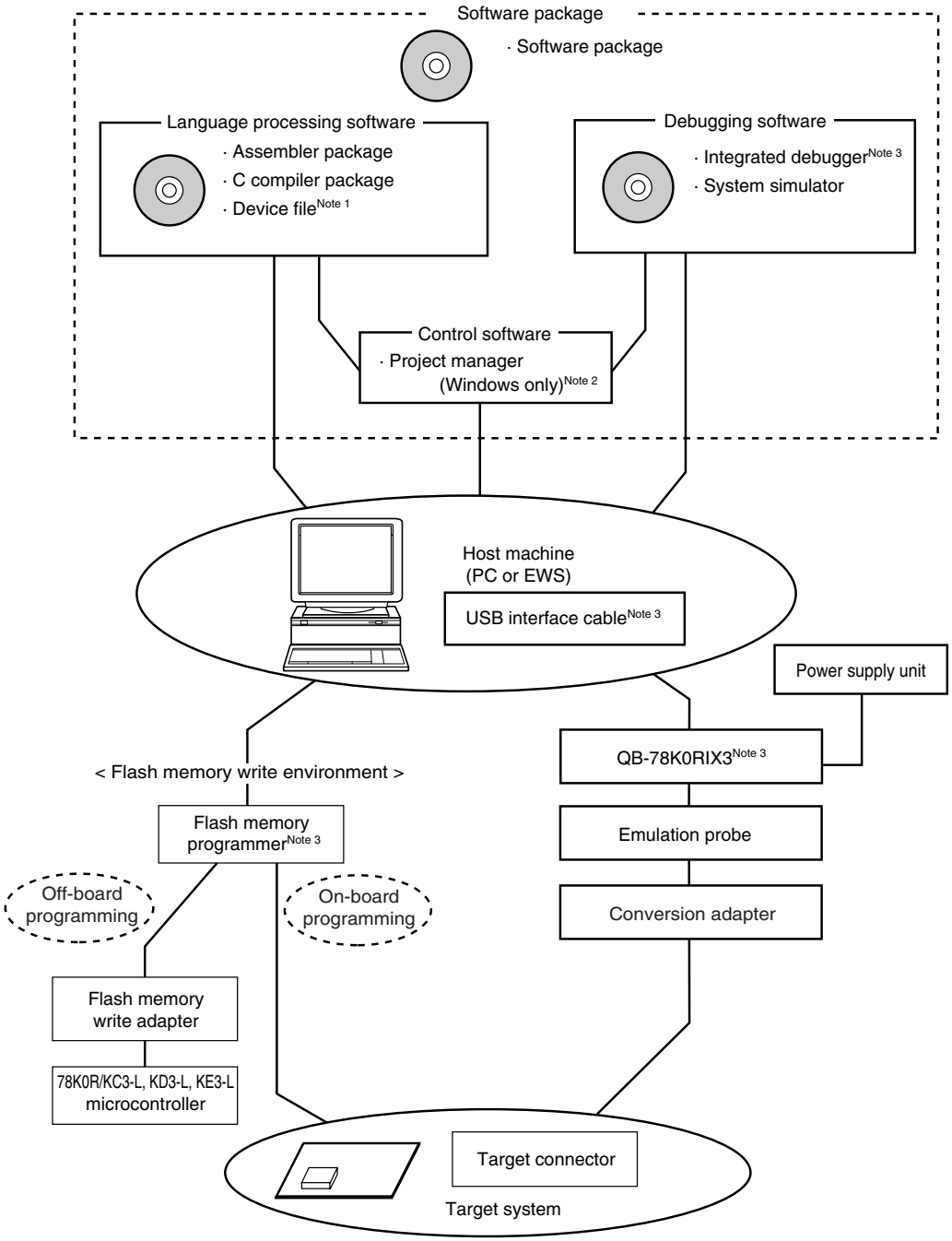
Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for the development of systems that employ the 78K0R/Kx3-L.
Figure A-1 shows the development tool configuration.

Figure A-1. Development Tool Configuration (1/3)

(1) When using the in-circuit emulator QB-78K0RIX3 (compatible with 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)



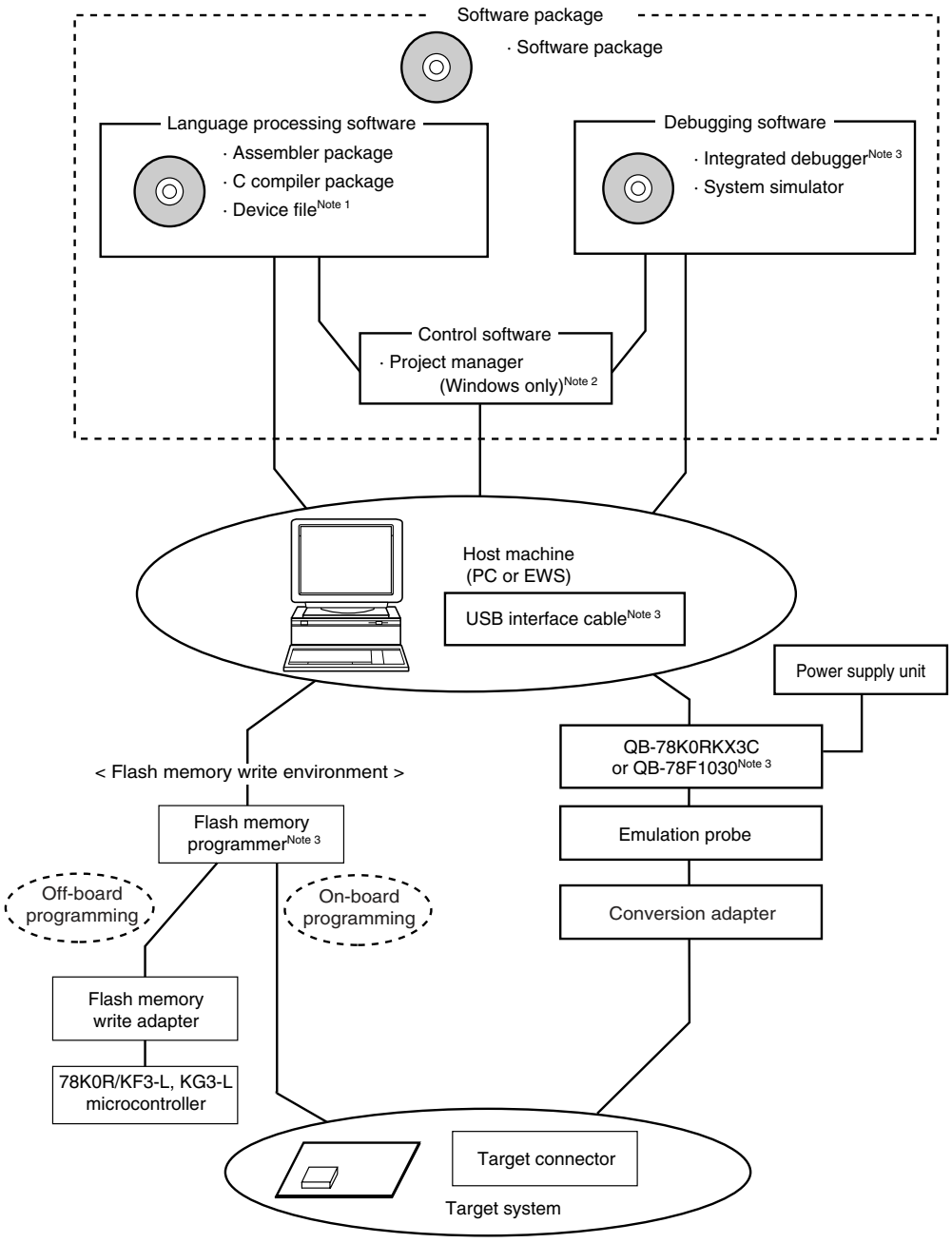
Notes 1. Download the device file for the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L (DF781014) from the download site for development tools (http://www2.renesas.com/micro/en/ods/).

2. The project manager PM+ is included in the assembler package.
The PM+ is only used for Windows.

3. In-circuit emulator QB-78K0RIX3 is supplied with integrated debugger ID78K0R-QB, on-chip debug emulator with programming function QB-MINI2 and USB interface cable. Any other products are sold separately.

Figure A-1. Development Tool Configuration (2/3)

(2) When using the in-circuit emulator QB-78K0RKX3C or QB-78F1030 (compatible with 78K0R/KF3-L, 78K0R/KG3-L)



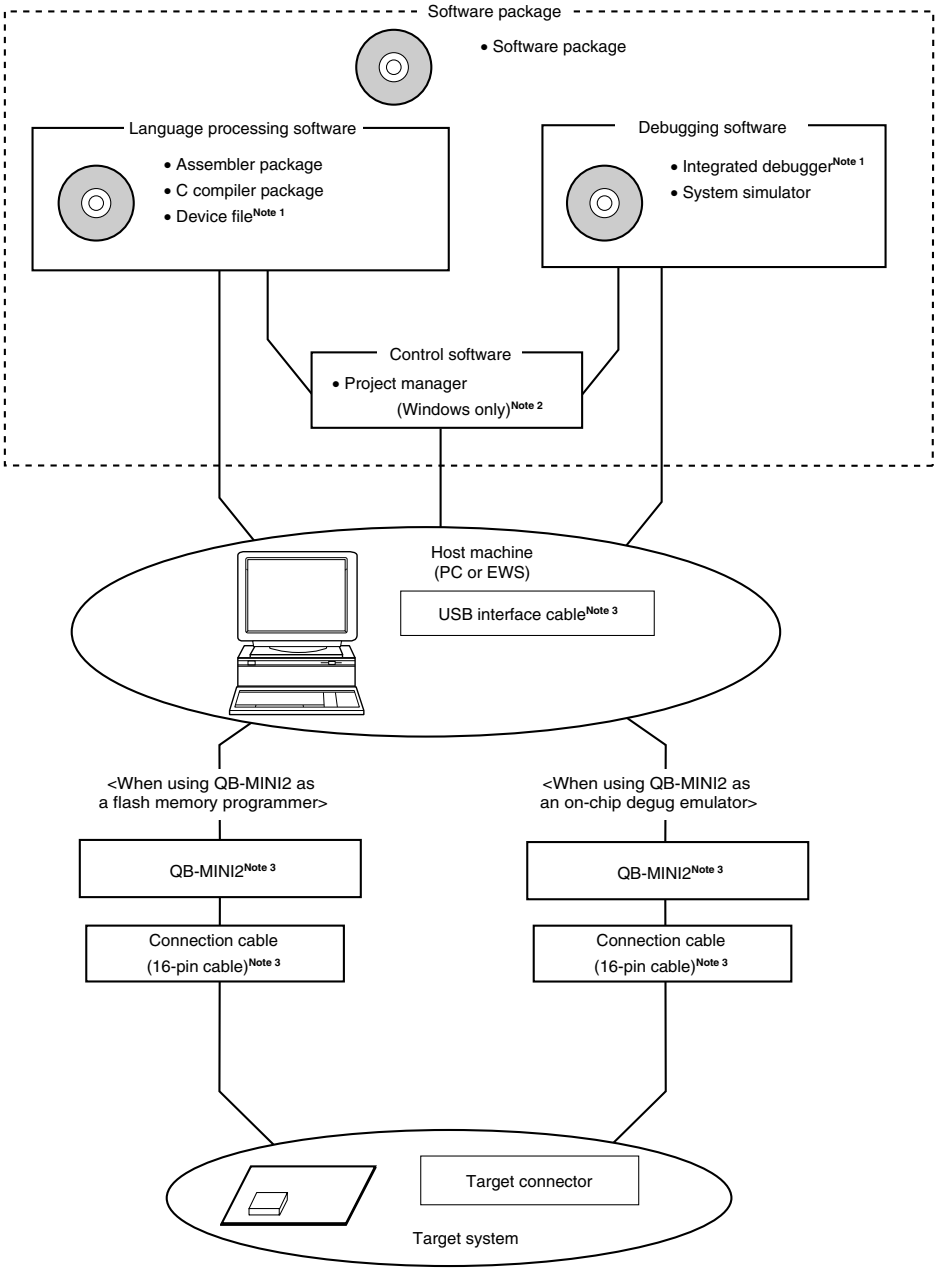
Notes 1. Download the device file for the 78K0R/KF3-L, 78K0R/KG3-L (DF781014/DF78F1030) from the download site for development tools (http://www2.renesas.com/micro/en/ods/).

2. The project manager PM+ is included in the assembler package.
The PM+ is only used for Windows.

3. In-circuit emulator QB-78K0RKX3C and QB-78F1030 are supplied with integrated debugger ID78K0R-QB, on-chip debug emulator with programming function QB-MINI2 and USB interface cable. Any other products are sold separately.

Figure A-1. Development Tool Configuration (3/3)

(3) When using the on-chip debug emulator with programming function QB-MINI2



Notes 1. Download the device file for the 78K0R/Kx3-L (DF781014/DF78F1030) and the integrated debugger (ID78K0R-QB) from the download site for development tools (http://www2.renesas.com/micro/en/ods/).

2. The project manager PM+ is included in the assembler package.
The PM+ is only used for Windows.

3. QB-MINI2 is supplied with USB interface cable, connection cables (10-pin cable and 16-pin cable), and 78K0-OCD board. Any other products are sold separately. In addition, download the software for operating the QB-MINI2 from the download site for MINICUBE2 (http://www2.renesas.com/micro/en/development/asia/minicube2/minicube2.html).

A.1 Software Package

SP78K0R 78K0R Series software package	Development tools (software) common to the 78K0R microcontrollers are combined in this package.
	Part number: μS××××SP78K0R

Remark ×××× in the part number differs depending on the host machine and OS used.

μS××××SP78K0R

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	

A.2 Language Processing Software

RA78K0R Assembler package	This assembler converts programs written in mnemonics into object codes executable with a microcontroller. This assembler is also provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with a device file (DF781014/DF781030[Note1]). **<Precaution when using RA78K0R in PC environment>** This assembler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (included in assembler package) on Windows.
	Part number: μS××××RA78K0R
CC78K0R C compiler package	This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an assembler package and device file (both sold separately). **<Precaution when using CC78K0R in PC environment>** This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (included in assembler package) on Windows.
	Part number: μS××××CC78K0R
DF781014/DF781030[Notes 1, 2] Device file	This file contains information peculiar to the device. This device file should be used in combination with a tool (RA78K0R, CC78K0R, SM+ for 78K0R, and ID78K0R-QB) (all sold separately). The corresponding OS and host machine differ depending on the tool to be used.
	Part number: μS××××DF781014, μS××××DF781030

Notes 1. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L, 78K0R/KF3-L (μ PD78F1010, 78F1011, 78F1012), 78K0R/KG3-L (μ PD78F1013, 78F1014) : DF781014
78K0R/KF3-L (μ PD78F1027, 78F1028), 78K0R/KG3-L (μ PD78F1029, 78F1030) : DF781030

2. The DF781014 and DF781030 can be used in common with the RA78K0R, CC78K0R, SM+ for 78K0R, and ID78K0R-QB. Download the DF781009 and DF781014 from the download site for development tools (http://www2.renesas.com/micro/en/ods/).

Remark ××××in the part number differs depending on the host machine and OS used.

μS××××RA78K0R
μS××××CC78K0R

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	

μS××××DF781014
μS××××DF781030

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	3.5-inch 2HD FD
BB13		Windows (English version)	

A.3 Control Software

PM+ Project manager	This is control software designed to enable efficient user program development in the Windows environment. All operations used in development of a user program, such as starting the editor, building, and starting the debugger, can be performed from the project manager. **<Caution>** The project manager is included in the assembler package (RA78K0R). It can only be used in Windows.

A.4 Flash Memory Programming Tools

A.4.1 When using flash memory programmer PG-FP5 and FL-PR5

PG-FP5 and FL-PR5 Flash memory programmer	Flash memory programmer dedicated to microcontrollers with on-chip flash memory.
FA-xxxx[Note] Flash memory programming adapter	Flash memory programming adapter used connected to the flash memory programmer for use.

Note The part numbers of the flash memory programming adapter and the packages of the target device are described below.

Package		Flash Memory Programming Adapter
78K0R/KC3-L	44-pin plastic LQFP (GB-GAF type)	FA-78F1003GB-GAF-RX
	48-pin plastic TQFP (GA-HAA type)	FA-78F1003GA-HAA-RX
78K0R/KD3-L	52-pin plastic LQFP (GB-GAG type)	FA-78F1006GB-GAG-RX
78K0R/KE3-L	64-pin plastic LQFP (GK-GAJ type)	FA-78F1009GK-GAJ-RX
	64-pin plastic LQFP (GB-GAH type)	FA-78F1009GB-GAH-RX
	64-pin plastic TQFP (GA-HAB type)	FA-78F1009GA-HAB-RX
	64-pin plastic FBGA (F1-AN1 type)	FA-78F1009F1-AN1-RX
	64-pin plastic FBGA (F1-AA2 type)	FA-78F1009F1-AA2-RX
78K0R/KF3-L	80-pin plastic LQFP (GC-GAD type)	FA-78F1012GC-GAD-RX
	80-pin plastic LQFP (GK-GAK type)	FA-78F1012GK-GAK-RX
78K0R/KG3-L	100-pin plastic LQFP (GC-UEU type)	FA-78F1014GC-UEU-RX
	100-pin plastic LQFP (GF-GAS type)	FA-78F1014GF-GAS-RX
	100-pin plastic FBGA (F1-BAK type)	FA-78F1014F1-BAK-RX

Remarks 1. The FL-PR5 and FA-xxxx are products of Naito Densei Machida Mfg. Co., Ltd.

2. Use the latest version of the flash memory programming adapter.

A.4.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This is a flash memory programmer dedicated to microcontrollers with on-chip flash memory. It is available also as on-chip debug emulator which serves to debug hardware and software when developing application systems using the 78K0R/Kx3-L microcontrollers. The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. To use the 78K0R/Kx3-L, use USB interface cable and 16-pin connection cable.

Remark Download the software for operating the QB-MINI2 from the download site for MINICUBE2 (http://www2.renesas.com/micro/en/development/asia/minicube2/minicube2.html).

A.5 Debugging Tools (Hardware)

A.5.1 When using in-circuit emulator

(1) QB-78K0RIX3 (compatible with 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

QB-78K0RIX3 In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L microcontrollers. It supports to the integrated debugger (ID78K0R-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-COMMON-PW-××Note 1	This power supply unit can be used in common with the all products of in-circuit emulator IECUBE and the flash memory programmer PG-FP5.
QB-144-CA-01 Check pin adapter	This check pin adapter is used in waveform monitoring using the oscilloscope, etc.
QB-80-EP-01T Emulation probe	This emulation probe is flexible type and used to connect the in-circuit emulator and target system.
QB-xxxx-EA-xxxNote 2 Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector.
QB-xxxx-YS-xxxxNote 2 Space adapter	This space adapter is used to adjust the height between the target system and in-circuit emulator.
QB-xxxx-YQ-xxxNote 2 YQ connector	This YQ connector is used to connect the target connector and exchange adapter.
QB-xxxx-HQ-XxxNote 2 Mount adapter	This mount adapter is used to mount the target device with socket.
QB-xxxx-NQ-xxxNote 2 Target connector	This target connector is used to mount on the target system.

Notes 1. ×× differs depending on the target area of each product.

2. The part numbers of the exchange adapter, space adapter, YQ connector, mount adapter, and target connector and the packages of the target device are described below.

	Package		Exchange Adapter	Space Adapter	YQ Connector	Mount Adapter	Target Connector
<R>	78K0R/KC3-L	40-pin plastic WQFN (K8-4B4 type)	QB-40K8-EA-02T	None	None	None	QB-40K8-NQ-01T
		44-pin plastic LQFP (GB-GAF type)	QB-44GB-EA-04T	QB-44GB-YS-01T	QB-44GB-YQ-01T	QB-44GB-HQ-01T	QB-44GB-NQ-01T
		48-pin plastic LQFP (GA-HAA type)	QB-48GA-EA-04T	QB-48GA-YS-01T	QB-48GA-YQ-01T	QB-48GA-HQ-01T	QB-48GA-NQ-01T
<R>		48-pin plastic WQFN (K8-5B4 type)	QB-48K8-EA-02T	None	None	None	QB-48K8-NQ-01T
	78K0R/KD3-L	52-pin plastic LQFP (GB-GAG type)	QB-52GB-EA-04T	QB-52GB-YS-01T	QB-52GB-YQ-01T	QB-52GB-HQ-01T	QB-52GB-NQ-01T
	78K0R/KE3-L	64-pin plastic LQFP (GB-GAH type)	QB-64GB-EA-04T	QB-64GB-YS-01T	QB-64GB-YQ-01T	QB-64GB-HQ-01T	QB-64GB-NQ-01T
		64-pin plastic LQFP (GK-GAJ type)	QB-64GK-EA-04T	QB-64GK-YS-01T	QB-64GK-YQ-01T	QB-64GK-HQ-01T	QB-64GK-NQ-01T
		64-pin plastic TQFP (GA-HAB type)	QB-64GA-EA-01T	QB-64GA-YS-01T	QB-64GA-YQ-01T	QB-64GA-HQ-01T	QB-64GA-NQ-01T
		64-pin plastic FBGA (F1-AN1 type)	QB-64FC-EA-01T	None	None	None	QB-64FC-NQ-01T
		64-pin plastic FBGA (F1-AA2 type)	QB-64F1-EA-03T	None	None	None	QB-64F1-NQ-01T

(Remarks are listed on the next page or later.)

Remarks 1. The QB-78K0RIX3 is supplied with a USB interface cable, integrated debugger ID78K0R-QB and on-chip debug emulator with programming function QB-MINI2.

2. The packed contents differ depending on the part number, as follows.

Part Number \ Packed Contents	In-Circuit Emulator	Emulation Probe	Exchange Adapter	YQ Connector	Target Connector
QB-78K0RIX3-ZZZ	QB-78K0RIX3	None			
<R> QB-78K0RIX3-T40K8		QB-80-EP-01T	QB-40K8-EA-02T	None	QB-40K8-NQ-01T
QB-78K0RIX3-T44GB			QB-44GB-EA-04T	QB-44GB-YQ-01T	QB-44GB-NQ-01T
QB-78K0RIX3-T48GA			QB-48GA-EA-04T	QB-48GA-YQ-01T	QB-48GA-NQ-01T
<R> QB-78K0RIX3-T48K8			QB-48K8-EA-02T	None	QB-48K8-NQ-01T
QB-78K0RIX3-T52GB			QB-52GB-EA-04T	QB-52GB-YQ-01T	QB-52GB-NQ-01T
QB-78K0RIX3-T64GB			QB-64GB-EA-04T	QB-64GB-YQ-01T	QB-64GB-NQ-01T
QB-78K0RIX3-T64GK			QB-64GK-EA-04T	QB-64GK-YQ-01T	QB-64GK-NQ-01T
QB-78K0RIX3-T64GA			QB-64GA-EA-01T	QB-64GA-YQ-01T	QB-64GA-NQ-01T
QB-78K0RIX3-T64F1			QB-64FC-EA-01T	None	QB-64FC-NQ-01T

(2) QB-78K0RKX3C, QB-78F1030 (compatible with 78K0R/KF3-L, 78K0R/KG3-L)

QB-78K0RKX3C In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0R/KF3-L, 78K0R/KG3-L microcontrollers (μPD78F1010, 78F1011, 78F1012, 78F1013, and 78F1014). It supports to the integrated debugger (ID78K0R-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-78F1030 In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0R/KF3-L, 78K0R/KG3-L microcontrollers (μPD78F1027, 78F1028, 78F1029, and 78F1030). It supports to the integrated debugger (ID78K0R-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-COMMON-PW-××Note 1	This power supply unit can be used in common with the all products of in-circuit emulator IECUBE and the flash memory programmer PG-FP5.
QB-144-CA-01 Check pin adapter	This check pin adapter is used in waveform monitoring using the oscilloscope, etc.
QB-144-EP-02S Emulation probe	This emulation probe is flexible type and used to connect the in-circuit emulator and target system.
QB-xxxx-EA-xxxNote 2 Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector.
QB-xxxx-YS-xxxxNote 2 Space adapter	This space adapter is used to adjust the height between the target system and in-circuit emulator.
QB-xxxx-YQ-xxxNote 2 YQ connector	This YQ connector is used to connect the target connector and exchange adapter.
QB-xxxx-HQ-XxxNote 2 Mount adapter	This mount adapter is used to mount the target device with socket.
QB-xxxx-NQ-xxxNote 2 Target connector	This target connector is used to mount on the target system.

Notes 1. ×× differs depending on the target area of each product.

2. The part numbers of the exchange adapter, space adapter, YQ connector, mount adapter, and target connector and the packages of the target device are described below.

Package		Exchange Adapter	Space Adapter	YQ Connector	Mount Adapter	Target Connector
78K0R/KF3-L	80-pin plastic LQFP (GC-GAD type)	QB-80GC-EA-10T	QB-80GC-YS-01T	QB-80GC-YQ-01T	QB-80GC-HQ-01T	QB-80GC-NQ-01T
	80-pin plastic LQFP (GK-GAK type)	QB-80GK-EA-09T	QB-80GK-YS-01T	QB-80GK-YQ-01T	QB-80GK-HQ-01T	QB-80GK-NQ-01T
78K0R/KG3-L	100-pin plastic LQFP (GC-UEU type)	QB-100GC-EA-07T	QB-100GC-YS-01T	QB-100GC-YQ-01T	QB-100GC-HQ-01T	QB-100GC-NQ-01T
	100-pin plastic LQFP (GF-GAS type)	QB-100GF-EA-05T	QB-100GF-YS-01T	QB-100GF-YQ-01T	QB-100GF-HQ-03T	QB-100GF-NQ-01T
	100-pin plastic FBGA (F1-BAK type)	QB-100F1-EA-01T	None	None	None	QB-100F1-NQ-1T

(Remarks are listed on the next page.)

Remarks 1. The QB-78K0RKX3C and QB-78F1030 are supplied with a USB interface cable, integrated debugger ID78K0R-QB and on-chip debug emulator with programming function QB-MINI2.

2. The packed contents differ depending on the part number, as follows.

Packed Contents / Part Number	In-Circuit Emulator	Emulation Probe	Exchange Adapter	YQ Connector	Target Connector
QB-78K0RKX3C-ZZZ	QB-78K0RKX3C	None			
QB-78F1030-ZZZ	QB-78F1030				
QB-78K0RKX3C-T80GC	QB-78K0RKX3C	QB-80-EP-01T	QB-80GC-EA-10T	QB-80GC-YQ-01T	QB-80GC-NQ-01T
QB-78K0RKX3C-T80GK			QB-80GK-EA-09T	QB-80GK-YQ-01T	QB-80GK-NQ-01T
QB-78K0RKX3C-T80GC	QB-78F1030		QB-80GC-EA-10T	QB-80GC-YQ-01T	QB-80GC-NQ-01T
QB-78K0RKX3C-T80GK			QB-80GK-EA-09T	QB-80GK-YQ-01T	QB-80GK-NQ-01T
QB-78K0RKX3C-T100GC	QB-78K0RKX3C		QB-100GC-EA-07T	QB-100GC-YQ-01T	QB-100GC-NQ-01T
QB-78K0RKX3C-T100GF			QB-100GF-EA-05T	QB-100GF-YQ-01T	QB-100GF-NQ-01T
QB-78K0RKX3C-T100F1			QB-100F1-EA-01T	None	QB-100F1-NQ-01T
QB-78K0RKX3C-T100GC	QB-78F1030		QB-100GC-EA-07T	QB-100GC-YQ-01T	QB-100GC-NQ-01T
QB-78K0RKX3C-T100GF			QB-100GF-EA-05T	QB-100GF-YQ-01T	QB-100GF-NQ-01T

A.5.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This on-chip debug emulator serves to debug hardware and software when developing application systems using the 78K0R/Kx3-L microcontrollers. It is available also as flash memory programmer dedicated to microcontrollers with on-chip flash memory. The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. To use the 78K0R/Kx3-L, use USB interface cable and 16-pin connection cable.

Remark Download the software for operating the QB-MINI2 from the download site for MINICUBE2 (http://www2.renesas.com/micro/en/development/asia/minicube2/minicube2.html).

A.6 Debugging Tools (Software)

SM+ for 78K0R System simulator	SM+ for 78K0R is Windows-based software. It is used to perform debugging at the C source level or assembler level while simulating the operation of the target system on a host machine. Use of SM+ for 78K0R allows the execution of application logical testing and performance testing on an independent basis from hardware development, thereby providing higher development efficiency and software quality. SM+ for 78K0R should be used in combination with the device file (DF781014/DF781030 Note).
	Part number: μS××××SM781000
ID78K0R-QB Integrated debugger	This debugger supports the in-circuit emulators for the 78K0R microcontrollers. The ID78K0R-QB is Windows-based software. It has improved C-compatible debugging functions and can display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. It should be used in combination with the device file (DF781014/DF781030 Note).
	Part number: μS××××ID78K0R-QB

Notes 1. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L, 78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012),
78K0R/KG3-L (μPD78F1013, 78F1014) : DF781014
78K0R/KF3-L (μPD78F1027, 78F1028),
78K0R/KG3-L (μPD78F1029, 78F1030) : DF781030

Remark ×××× in the part number differs depending on the host machine and OS used.

μS××××SM781000
μS××××ID78K0R-QB

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	

APPENDIX B REVISION HISTORY

B.1 Major Revisions in This Edition

Page	Description	Classification
CHAPTER 13 A/D CONVERTER		
pp. 557 to 559	Change of **Table 13-2. A/D Conversion Time Selection**	(c)
p. 569	Change of **Figure 13-12. Basic Operation of A/D Converter**	(c)
CHAPTER 14 SERIAL ARRAY UNIT		
p. 631	Change of **Notes** in **Figure 14-28. Example of Contents of Registers for Master Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41)**	(c)
p. 641	Change of **Notes** in **Figure 14-36. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41)**	(c)
p. 650	Change of **Notes** in **Figure 14-44. Example of Contents of Registers for Master Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41)**	(c)
pp. 659, 660	Change of **Notes** in **Figure 14-52. Example of Contents of Registers for Slave Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41)**	(c)
pp. 669, 670	Change of **Notes** in **Figure 14-60. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41)**	(c)
pp. 676, 677	Change of **Notes** in **Figure 14-66. Example of Contents of Registers for Slave Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSK40, CSK41)**	(c)
p. 692	Change of **Notes** in **Figure 14-75. Example of Contents of Registers for UART Transmission of UART (UART0 to UART4)**	(c)
pp. 724, 725	Change of **Notes** in **Figure 14-98. Example of Contents of Registers for Address Field Transmission of Simplified I2C (IIC10, IIC20)**	(c)
pp. 730, 731	Change of **Notes** in **Figure 14-102. Example of Contents of Registers for Data Transmission of Simplified I2C (IIC10, IIC20)**	(c)
pp. 734, 735	Change of **Notes** in **Figure 14-105. Example of Contents of Registers for Data Reception of Simplified I2C (IIC10, IIC20)**	(c)
CHAPTER 15 SERIAL INTERFACE IICA		
pp. 827 to 833	Change of figure and description in **Figure 15-32. Example of Master to Slave Communication (9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave)**	(c)
pp. 835 to 839	Change of figure and description in **Figure 15-33. Example of Slave to Master Communication (8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave)**	(c)
CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L 78K0R/KE3-L)		
pp. 1038, 1040	Change of **30.4.2 Supply current characteristics**	(b)
CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)		
p. 1091	Change of **31.4.2 Supply current characteristics**	(b)
APPENDIX A DEVELOPMENT TOOLS		
pp. 1150, 1151	Change of status in target connector of 78K0R/KC3-L from under development to mass production	(b)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

B.2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

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Edition	Description	Chapter
Previous version (U19291E) 2nd edition	Change of 64-pin plastic FBGA (5 × 5) **in 1.4.3 78K0R/KE3-L**	CHAPTER 1 OUTLINE
	Change of description in **2.2.14 $\overline{\text{RESET}}$**	CHAPTER 2 PIN FUNCTIONS
	Deletion of description in **2.2.15 REGC**	
	Addition of description to **3.1.2 Mirror area**	CHAPTER 3 CPU ARCHITECTURE
	Change of **Table 3-6. Extended SFR (2nd SFR) List (3/4), (4/4)**	
	Change of **Figure 4-19. Block Diagram of P80**	CHAPTER 4 PORT FUNCTIONS
	Change of **Figure 4-20. Block Diagram of P81 and P83**	
	Change of **Figure 4-21. Block Diagram of P82**	
	Addition of **Cautions 1** and **3** in **Figure 5-7. Format of 20 MHz Internal High-Speed Oscillation Control Register (DSCCTL)**	CHAPTER 5 CLOCK GENERATOR
	Change of **Cautions 4** and **5** in **Figure 5-9. Format of Operation Speed Mode Control Register (OSMC)**	
	Change of **(3) CPU operating with subsystem clock (D) after reset release (A)** in **Table 5-4**	
	Change of **(9) CPU clock changing from high-speed system clock (C) to subsystem clock (D)** in **Table 5-4**	
	Change of **(11) CPU clock changing from subsystem clock (D) to high-speed system clock (C)** in **Table 5-4**	
	Change of **(12) CPU clock changing from 20 MHz internal high-speed oscillation clock (J) to internal high-speed oscillation clock (B)** in **Table 5-4**	
	Change of **(14) • STOP mode (H) set while CPU is operating with internal high-speed oscillation clock (B), •STOP mode (I) set while CPU is operating with high-speed system clock (C)** in **Table 5-4**	
	Change of **Table 5-5. Changing CPU Clock**	
	Change of description of the CCS0n bit in **Figure 6-6 Format of Timer Mode Register 0n (TMR0n)**	CHAPTER 6 TIMER ARRAY UNIT
	Change of description in **6.4.3 (1) Changing values set in registers TO0, TOE0, TOL0, and TOM0 during timer operation**	
	Addition of description to **6.7.1 (1) Interval timer**	
	Change of **Figure 6-35 Block Diagram of Operation as Interval Timer/Square Wave Output**	
	Addition of **(2) When f_{SUB}/4 is selected as count clock** to **Figure 6-37. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output**	
	Change of **Figure 6-38 Operation Procedure of Interval Timer/Square Wave Output Function**	
	Change of description during operation in **Figure 6-42 Operation Procedure When External Event Counter Function Is Used**	
	Change of description during operation in **Figure 6-46 Operation Procedure When Frequency Divider Function Is Used**	
	Change of description during operation in **Figure 6-50 Operation Procedure When Input Pulse Interval Measurement Function Is Used**	

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Edition	Description	Chapter
Previous version (U19291E) 2nd edition	Change of description during operation in **Figure 6-54 Operation Procedure When Input Signal High-/Low-Level Width Measurement Function Is Used**	CHAPTER 6 TIMER ARRAY UNIT
	Change of description during operation in **Figure 6-59 Operation Procedure When PWM Function Is Used**	
	Change of description during operation in **Figure 6-64 Operation Procedure of One-Shot Pulse Output Function**	
	Change of description during operation in **Figure 6-69 Operation Procedure When Multiple PWM Output Function Is Used**	
	Change of description of the CT2 to CT1 bits in **Figure 7-3 Format of Real-Time Counter Control Register 0 (RTCC0)**	CHAPTER 7 REAL-TIME COUNTER
	Change of description of the WALE bit in **Figure 7-4 Format of Real-Time Counter Control Register 1 (RTCC1)**	
	Addition of **Caution 3** to **Figure 7-5 Format of Real-Time Counter Control Register 2 (RTCC2)**	
	Change of description in **7.3 (7) Minute count register (MIN)**, **(8) Hour count register (HOUR)**, **(9) Day count register (DAY)**, **(11) Month count register (MONTH)**, and **(12) Year count register (YEAR)**	
	Addition of description to **7.3 (13) Watch error correction register (SUBCUD)**	
	Addition of **Caution 3** to **Figure 8-3. Format of Programmable Gain Amplifier Control Register (OAM)**	CHAPTER 8 COMPARATORS/PROGRAMMABLE GAIN AMPLIFIERS
	Addition of **Caution 5** to **Figure 8-4. Format of Comparator n Control Register (CnCTL)**	
	Addition of **Caution 4** to **Figure 8-5. Format of Comparator n Internal Reference Voltage Selection Register (CnRVM)**	
	Change of **Caution 2** in **Figure 9-2. Format of Clock Output Select Register n (CKSn)**	CHAPTER 9 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER
	Change of **Remark 1** in **9.4.1 Operation as output pin**	
	Change of **Figure 9-4. Remote Control Output Application Example**	
	Change of description in **11.6 (1) Operating current in STOP mode**	CHAPTER 11 A/D CONVERTER
	Change of **(b) When receiving last data** in **Figure 12-95. Timing Chart of Data Reception**	CHAPTER 12 SERIAL ARRAY UNIT
	Addition of **Caution 3** to **Figure 13-3. Format of IICA Shift Register (IICA)**	CHAPTER 13 SERIAL INTERFACE IICA
	Change of **Figure 13-6. Format of IICA Control Register 0 (IICCTL0)**	
	Addition of description to the WUP bit in **Figure 13-9. Format of IICA Control Register 1 (IICCTL1)**	
	Addition of **13.4.2 Setting transfer clock by using IICWL and IICWH registers**	
	Deletion of description in **Figure 13-23. Flow When Setting WUP = 0 upon Address Match (Including Extension Code Reception)**	
	Deletion of descriptions in **13.5.13 Wakeup function**	
	Change of **Figure 13-24. When Operating as Master Device after Releasing STOP Mode other than by INTIICA**	
	Deletion of **Figure 13-25. When Operating as Slave Device after Releasing STOP Mode other than by INTIICA (When Not Required to Operate as Master Device)**	

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Edition	Description	Chapter
Previous version (U19291E) 2nd edition	Change of **Table 15-2 Response Time of DMA Transfer**	CHAPTER 15 DMA CONTROLLER
	Change of **Table 16-1 Interrupt Source List (2/2)**	CHAPTER 16 INTERRUPT FUNCTIONS
	Addition of **(C) External maskable interrupt (INTKR)** to **Figure 16-1. Basic Configuration of Interrupt Function (2/2)**	
	Change of **Caution 2** in **17.3 (1) Key return mode register (KRM)**	CHAPTER 17 KEY INTERRUPT FUNCTION
	Addition of **Note** to **Figure 18-3 HALT Mode Release by Interrupt Request Generation**	CHAPTER 18 STANDBY FUNCTION
	Change of **Note 4** and **Caution 1** in **Figure 21-2. Format of Low-Voltage Detection Register (LVIM)**	CHAPTER 21 LOW-VOLTAGE DETECTOR
	Change of description in **21.4.1 (1) When detecting level of supply voltage (V_{DD})**	
	Change of description in **21.4.1 (2) When detecting level of input voltage from external input pin (EXLVI)**	
	Change of description in **21.4.2 (1) When detecting level of supply voltage (V_{DD})**	
	Change of description in **21.4.2 (2) When detecting level of input voltage from external input pin (EXLVI)**	
	Change of **Figure 21-12. Delay from the time LVI reset source is generated until the time LVI reset has been generated or released**	
	Addition of **Caution 5** to **24.8 Flash Memory Programming by Self-Programming**	CHAPTER 24 FLASH MEMORY
	Change of description in **24.8.2 Flash shield window function**	
	Addition of chapter	APPENDIX B REVISION HISTORY
Previous version (U19291E) 3rd edition	Change of **On-chip internal high-speed oscillation clocks** in **1.1 Features**	CHAPTER 1 OUTLINE
	Change of **1.3 Ordering Information**	
	Addition of **64-pin plastic FBGA (4 × 4)** to **1.4.3 78K0R/KE3-L**	
	Change of **1.7 Outline of Functions**	
	Addition of **Note** to **Figures 3-1** to **3-4 Memory Map**	CHAPTER 3 CPU ARCHITECTURE
	Addition of description to **3.1.1 (1) Vector table area**	
	Change of **Table 3-5. SFR List (3/4)**	
	Addition of **Caution 3** to **Figure 4-39. Format of A/D Port Configuration Register (ADPC)**	CHAPTER 4 PORT FUNCTIONS
	Change of **Figure 5-3. Format of System Clock Control Register (CKC)**	CHAPTER 5 CLOCK GENERATOR
	Addition of **Note** and **Cautions 3, 6** to **Figure 5-4. Format of Clock Operation Status Control Register (CSC)**	
	Change of **Caution 3** in **Figure 5-6. Format of Oscillation Stabilization Time Select Register (OSTS)**	
	Addition of **Caution 4** to **Figure 5-7. Format of 20 MHz Internal High-Speed Oscillation Control Register (DSCCTL)**	
	Addition of description to **5.3 (7) Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2)**	
	Change of **Cautions 2** and **3** in **Figure 5-9. Format of Operation Speed Mode Control Register (OSMC)**	
	Change of **Caution 7** in **Figure 5-9. Format of Operation Speed Mode Control Register (OSMC)**	
	Change of **5.4.3 Internal high-speed oscillator**	

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Edition	Description	Chapter
Previous version (U19291E) 3rd edition	Change of **Figure 5-13. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Stopped Is Set (Option Byte: LVIOFF = 1))**	CHAPTER 5 CLOCK GENERATOR
	Change of **Figure 5-14. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Enabled Is Set (Option Byte: LVIOFF = 0))**	
	Change of **5.6 Controlling Clock**	
	Addition of **Notes 3** and **4** to **5.6.6 CPU clock status transition diagram**	
	Change of **6.1.1 Independent channel operation function**	CHAPTER 6 TIMER ARRAY UNIT
	Change of **6.1.2 Simultaneous channel operation function**	
	Change of **Figure 6-1. Entire Configuration of Timer Array Unit TAUS**	
	Addition of **Figure 6-2. Internal Block Diagram of Channel of Timer Array Unit TAUS**	
	Change of **Figure 6-21. Format of Timer Output Mode Register 0 (TOM0)**	
	Change of **Figure 6-22. Format of Input Switch Control Register (ISC)**	
	Change of description of operation start in **Figure 6-39. Operation Procedure of Interval Timer/Square Wave Output Function**	
	Change of description in **6.7.2 Operation as external event counter**	
	Addition of **Caution** to **6.7.5 Operation as input signal high-/low-level width measurement**	
	Change of description in **6.8.2 Operation as PWM function**	
	Change of **Note** in **Figure 7-2. Format of Peripheral Enable Register 0 (PER0)**	CHAPTER 7 REAL-TIME COUNTER
	Addition of **Note** to **Figure 7-18. Procedure for Starting Operation of Real-Time Counter**	
	Change of **10.4.3 Setting window open period of watchdog timer** (deletion of window open period 25% setting)	CHAPTER 10 WATCHDOG TIMER
	Change of **Figure 11-5. A/D Converter Sampling and A/D Conversion Timing**	CHAPTER 11 A/D CONVERTER
	Change of description in **11.6 (9) Conversion results just after A/D conversion start**	
	Change of **Table 11-4. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)**	
	Change of **Note 2** in **Figure 12-4. Format of Serial Clock Select Register 0 (SPS0)**	CHAPTER 12 SERIAL ARRAY UNIT
	Change of description of the MD0n0 bit in **Figure 12-5. Format of Serial Mode Register 0n (SMR0n) (2/2)**	
	Addition of **Note** to **Figure 12-6. Format of Serial Communication Operation Setting Register 0n (SCR0n) (2/3)**	
	Change of description in **12.3 (5) Higher 7 bits of the serial data register 0n (SDR0n)**	
	Change of **Figure 12-8. Format of Serial Flag Clear Trigger Register 0n (SIR0n)**	
	Change of **Figure 12-9. Format of Serial Status Register 0n (SSR0n)**	
	Change of **Figure 12-25. Procedure for Stopping Master Transmission**	
	Change of **Figure 12-27. Timing Chart of Master Transmission (in Single-Transmission Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of **Figure 12-29. Timing Chart of Master Transmission (in Continuous Transmission Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	

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Edition	Description	Chapter
Previous version (U19291E) 3rd edition	Change of **Figure 12-31. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10) (2/2)**	CHAPTER 12 SERIAL ARRAY UNIT
	Change of **Figure 12-34. Procedure for Resuming Master Reception**	
	Change of **Figure 12-35. Timing Chart of Master Reception (in Single-Reception Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of **Figure 12-36. Flowchart of Master Reception (in Single-Reception Mode)**	
	Change of **Figure 12-39. Procedure for Stopping Master Transmission/Reception**	
	Change of **Figure 12-41. Timing Chart of Master Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of **Figure 12-43. Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of transfer rate in **12.5.4 Slave transmission**	
	Change of **Figure 12-47. Procedure for Stopping Slave Transmission**	
	Change of **Figure 12-49. Timing Chart of Slave Transmission (in Single-Transmission Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of **Figure 12-51. Timing Chart of Slave Transmission (in Continuous Transmission Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of transfer rate in **12.5.5 Slave reception**	
	Change of **Figure 12-53. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10) (2/2)**	
	Change of **Figure 12-56. Procedure for Resuming Slave Reception**	
	Change of **Figure 12-57. Timing Chart of Slave Reception (in Single-Reception Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of **Figure 12-58. Flowchart of Slave Reception (in Single-Reception Mode)**	
	Change of transfer rate in **12.5.6 Slave transmission/reception**	
	Change of **Figure 12-61. Procedure for Stopping Slave Transmission/Reception**	
	Change of **Figure 12-63. Timing Chart of Slave Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of **Figure 12-65. Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of **Note** in **12.5.7 Calculating transfer clock frequency**	
	Change of **Note 2** in **Table 12-2. Selection of Operation Clock**	
	Addition of **Caution** to **12.6 Operation of UART (UART0, UART1) Communication**	
	Change of **Figure 12-70. Procedure for Stopping UART Transmission**	
	Change of **Figure 12-72. Timing Chart of UART Transmission (in Single-Transmission Mode)**	
	Change of **Figure 12-74. Timing Chart of UART Transmission (in Continuous Transmission Mode)**	
	Change of description in **12.6.2 UART reception**	
	Change of **Figure 12-76. Example of Contents of Registers for UART Reception of UART (UART0, UART1) (2/2)**	
	Change of **Figure 12-79. Procedure for Resuming UART Reception**	
	Change of **Figure 12-80. Timing Chart of UART Reception**	

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Edition	Description	Chapter
Previous version (U19291E) 3rd edition	Change of **Figure 12-81. Flowchart of UART Reception**	CHAPTER 12 SERIAL ARRAY UNIT
	Change of **Note 2** in **Table 12-3. Selection of Operation Clock**	
	Addition of **Note** to **12.7.1 Address field transmission**	
	Change of **Figure 12-92. Timing Chart of Address Field Transmission**	
	Addition of **Note** to **12.7.2 Data transmission**	
	Change of **Figure 12-95. Timing Chart of Data Transmission**	
	Addition of **Note** to **12.7.3 Data reception**	
	Change of **Note 2** in **Table 12-4. Selection of Operation Clock**	
	Change of description of the STT bit in **Figure 13-6. Format of IICA Control Register 0 (IICCTL0) (3/4)**	CHAPTER 13 SERIAL INTERFACE IICA
	Change of **Caution** and description of the SPT bit in **Figure 13-6. Format of IICA Control Register 0 (IICCTL0) (4/4)**	
	Change of **Note** in **Figure 13-7. Format of IICA Status Register (IICS) (2/3)**	
	Change of **13.4.2 Setting transfer clock by using IICWL and IICWH registers**	
	Addition of **Caution** to **15.5.4 Holding DMA transfer pending by DWAITn bit**	CHAPTER 15 DMA CONTROLLER
	Addition of description to **15.5.5 Forced termination by software**	
	Addition of **Example 3** to **Figure 15-11. Forced Termination of DMA Transfer (2/2)**	
	Change of **15.6 (2) DMA response time**	
	Change of **16.2 Interrupt Sources and Configuration**	CHAPTER 16 INTERRUPT FUNCTIONS
	Change of **Figure 18-5. STOP Mode Release by Interrupt Request Generation (2/2)**	CHAPTER 18 STANDBY FUNCTION
	Addition of **(6) Internal reset by a reset processing check error**	CHAPTER 19 RESET FUNCTION
	Change of **Figure 19-1. Block Diagram of Reset Function**	
	Change of **Figure 19-3. Timing of Reset Due to Execution of Illegal Instruction or Watchdog Timer Overflow**	
	Change of **Note 2** in **Table 19-2. Hardware Statuses After Reset Acknowledgment (3/4)**	
	Change of **Figure 19-5. Format of Reset Control Flag Register (RESF)**	
	Change of **Table 19-3. RESF Register Status When Reset Request Is Generated**	
	Change of **Figure 20-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector**	CHAPTER 20 POWER-ON-CLEAR CIRCUIT
	Change of **Figure 20-3. Example of Software Processing After Reset Release (2/2)**	
	Addition of **Caution 4** to **Figure 21-2. Format of Low-Voltage Detection Register (LVIM)**	CHAPTER 21 LOW-VOLTAGE DETECTOR
	Addition of **Caution 4** to **Figure 21-3. Format of Low-Voltage Detection Level Select Register (LVIS)**	
	Change of **Figure 21-11. Example of Software Processing After Reset Release (2/2)**	
	Change of **Caution 2** in **Figure 22-1. Format of Regulator Mode Control Register (RMC)**	CHAPTER 22 REGULATOR
	Change of **Figure 23-1. Format of User Option Byte (000C0H/010C0H) (1/2)**	CHAPTER 23 OPTION BYTE
	Change of **23.4 Setting of Option Byte**	

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Edition	Description	Chapter
Previous version (U19291E) 3rd edition	Addition of PG-FP5, FL-PR5, and QB-MINI2 as dedicated flash memory programmers, and deletion of PG-FP4, FL-PR4	CHAPTER 24 FLASH MEMORY
	Addition of description to **24.6.2 Flash memory programming mode**	
	Change of **Table 24-5. Communication Modes**	
	Addition of description to **24.8 Flash Memory Programming by Self-Programming**	
	Change of **Caution** in **25.1 Connecting QB-MINI2 to 78K0R/Kx3-L**	CHAPTER 25 ON-CHIP DEBUG FUNCTION
	Change of **Table 25-1. Lists the Differences Between 1-line Mode and 2-line Mode.**	
	Change of **Remark** in **Table 27-1. Operand Identifiers and Specification Methods**	CHAPTER 27 INSTRUCTION SET
	Addition of description to **27.1.4 PREFIX instruction**	
	Change of **Remark 2** in **Table 27-5. Operation List**	
	Change of **Internal Oscillator Characteristics**	CHAPTER 28 ELECTRICAL SPECIFICATIONS
	Addition of manufacturer names and part numbers to **Recommended Oscillator Circuit Constants**	
	Change of output current, low in **DC Characteristics**	
	Change of output voltage, low in **DC Characteristics**	
	Change of supply current in **DC Characteristics**	
	Change of operating current in **DC Characteristics**	
	Addition of value of in the self programming mode to Instruction cycle in **AC Characteristics**	
	Change of **Caution** in **Minimum instruction execution time during main system clock operation (FSEL = 1, RMC = 00H)** in **AC Characteristics**	
	Change of **Minimum instruction execution time during self programming mode (RMC = 00H)** in **AC Characteristics**	
	Change of **(a) During communication at same potential (UART mode) (dedicated baud rate generator output)** in **(2) Serial interface: Serial array unit**	
	Change of **(d) During communication at same potential (simplified I^2C mode) (dedicated baud rate generator output)** in **(2) Serial interface: Serial array unit**	
	Change of **A/D Converter Characteristics**	
	Change of **Programmable gain amplifier characteristics**	
	Change of **Comparator characteristics**	
	Change of **Flash Memory Programming Characteristics**	
	Addition of **64-pin plastic FBGA (4 × 4) to 29.4 78K0R/KE3-L**	CHAPTER 29 PACKAGE DRAWINGS
	Change of **Figure A-1. Development Tool Configuration (2/2)**	APPENDIX A DEVELOPMENT TOOLS
	Change of **A.5.1 When using in-circuit emulator QB-78K0RIX3**	

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Edition	Description	Chapter
Current Version (U20024E) 1st edition	Addition of the 78K0R/KF3-L and 78K0R/KG3-L products.	Throughout
	Change of **Documents Related to Devices** and **Documents Related to Development Tools (Hardware) (User's Manuals)**	Related Documents
	Addition of **Caution 3** to **1.4.1 78K0R/KC3-L**	CHAPTER 1 OUTLINE
	Addition of **Caution 3** to **1.4.2 78K0R/KD3-L**	
	Addition of **Caution 4** and **Remark** to **1.4.3 78K0R/KE3-L**	
	Change of **Table 2-3. Connection of Unused Pins**	CHAPTER 2 PIN FUNCTIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)
	Change of description of the AMPH bit in **Figure 7-3. Format of Clock Operation Mode Control Register (CMC)**	CHAPTER 7 CLOCK GENERATOR
	Addition of **Note** to **Figure 7-4. Format of System Clock Control Register (CKC)**	
	Change of **Figure 7-15. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Stopped Is Set (Option Byte: LVIOFF = 1))**	
	Change of **Caution 1** in **Figure 7-16. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Enabled Is Set (Option Byte: LVIOFF = 0))**	
	Change of **Table 7-4. CPU Clock Transition and SFR Register Setting Examples (1/6) (2)**	
	Change of **Table 7-4. CPU Clock Transition and SFR Register Setting Examples (2/6) (5)**	
	Change of **Table 7-8. Maximum Number of Clocks Required for $f_{IH} \leftrightarrow f_{MX}$**	
	Change of **Table 7-9. Maximum Number of Clocks Required for $f_{MAIN} \leftrightarrow f_{SUB}$**	
	Change of **8.3 (14) Noise filter enable registers 1, 2 (NFEN1, NFEN2)**	CHAPTER 8 TIMER ARRAY UNIT
	Change of description of the AMPM bit in **Figure 9-3. Format of Real-Time Counter Control Register 0 (RTCC0)**	CHAPTER 9 REAL-TIME COUNTER
	Change of description of the RWAIT bit in **Figure 9-4. Format of Real-Time Counter Control Register 1 (RTCC1)**	
	Change of description in **9.3 (8) Hour count register (HOUR)**	
	Change of **Figure 9-18. Procedure for Starting Operation of Real-Time Counter**, and addition of Note 2	
	Change of **9.4.5 1 Hz output of real-time counter**	
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	Change of **Figure 22-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (1/2)**	CHAPTER 22 POWER-ON-CLEAR CIRCUIT
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	Addition of the 78K0R/KC3-L (40-pin), 78K0R/KF3-L (μ PD78F1027, 78F1028), and 78K0R/KG3-L (μ PD78F1029, 78F1030) products. Addition of WQFN package to 78K0R/KC3-L (48-pin) and 78K0R/KE3-L (64-pin).	CHAPTER 1 OUTLINE
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	Addition of the 78K0R/KC3-L (40-pin), 78K0R/KF3-L (μ PD78F1027, 78F1028), and 78K0R/KG3-L (μ PD78F1029, 78F1030) products. Addition of the serial allay unit 2.	CHAPTER 14 SERIAL ARRAY UNIT
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	Change of status of 100-pin plastic FBGA from under development to mass production	
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