KAF-09001

3024 (H) x 3024 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAF−09001 image sensor provides advanced imaging performance for demanding applications such as next−generation low cost digital still/motion radiography and scientific imaging systems. Building on the success of the KAF−09000 image sensor, the KAF−09001 combines high resolution and outstanding sensitivity with an updated output design that provides a 10x increase in full−resolution frame rate, along with support for binned output that provides even faster throughput. The high sensitivity and improved frame rate of the KAF−09001 directly enable lower patient exposure in medical applications and improved productivity in scientific imaging.

A high sensitivity 12 micron full frame CCD pixel design combines with a low noise output architecture to allow system designers to improve overall image quality or relax system tolerances to reduce cost. Excellent uniformity preserves overall image integrity by simplifying image corrections, while integrated anti−blooming protection prevents image bleed from overexposure in bright areas of the image.

Table 1. GENERAL SPECIFICATION

Parameter	Typical Value (1)
Architecture	Full Frame CCD [Square Pixels]
Total Number of Pixels (Note 2)	3092 (H) x 3072 (V) = 9.5 Mp
Number of Effective Pixels	3072 (H) x 3072 (V) = 9.4 Mp
Number of Active Pixels	3024 (H) x 3024 (V) = 9.1 Mp
Pixel Size	12.0 μm (H) x 12.0 μm (V)
Active Image Size	36.3 mm (H) x 36.3 mm (V)
Photographic Diagonal	51.3 mm diagonal
Optical Format	645 1.3x optical format
Aspect Ratio	Square 1:1
Horizontal Outputs	4
Charge Capacity	110 ke$^-$
Output Sensitivity	24 μV/e$^-$
Read Noise (e$^-$ rms)	7 @ 3 MHz; 18 @ 20 MHz
Dark Current (T = 25°C)	~5 electrons/s
Dynamic Range (Linear)	84 dB @ 3 MHz; 75 dB @ 20 MHz linear
Quantum Efficiency (Peak) Mono (540 nm)	64%
Maximum HCLOCK	20 MHz
Blooming Suppression	>1000x at t_{int} = 4 ms

1. Unless noted, all parameters are specified at 25°C.
2. Total including all photoactive, buffer, dark reference, and dummy pixels.

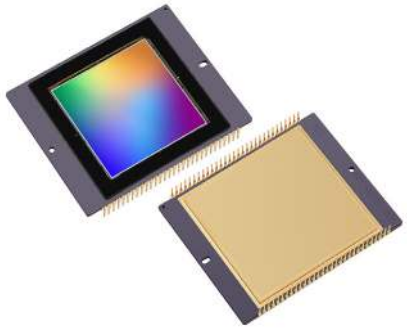


Figure 1. KAF09001 CCD Image Sensor

Features

- Large Pixel Size
- Large Image Area
- High Quantum Efficiency
- Low Noise Architecture
- 10 fps 3x3 Binned Video with 20 ms Exposure

Applications

- Medical
- Scientific

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAF− 09001 IMAGE SENSOR

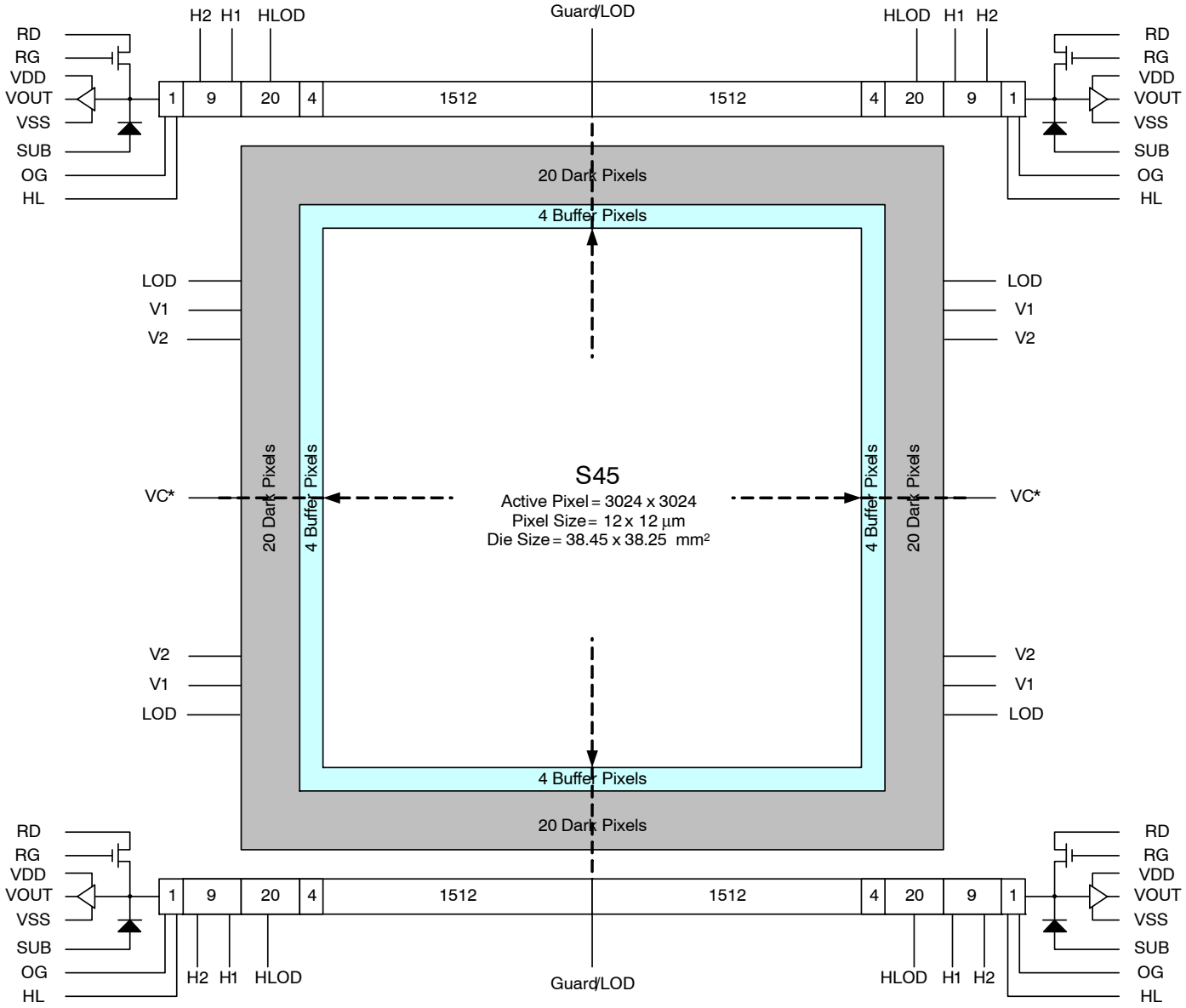
Part Number	Description	Marking Code
KAF−09001−ABA−DD−BA	Monochrome, Microlens, CERDIP Package, Sealed Clear Cover Glass with AR coating (both sides), Production Grade	KAF−09001−ABA Serial Number
KAF−09001−ABA−DD−AE	Monochrome, Microlens, CERDIP Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	
KAF−09001−ABA−DP−BA	Monochrome, Microlens, CERDIP Package, Taped Clear Cover Glass, no coatings, Production Grade	
KAF−09001−ABA−DP−AE	Monochrome, Microlens, CERDIP Package, Taped Clear Cover Glass, no coatings, Engineering Grade	

1. Part numbers are listed for informational purposes only, and are not available for orders at this time. Please contact ON Semiconductor for availability dates.

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

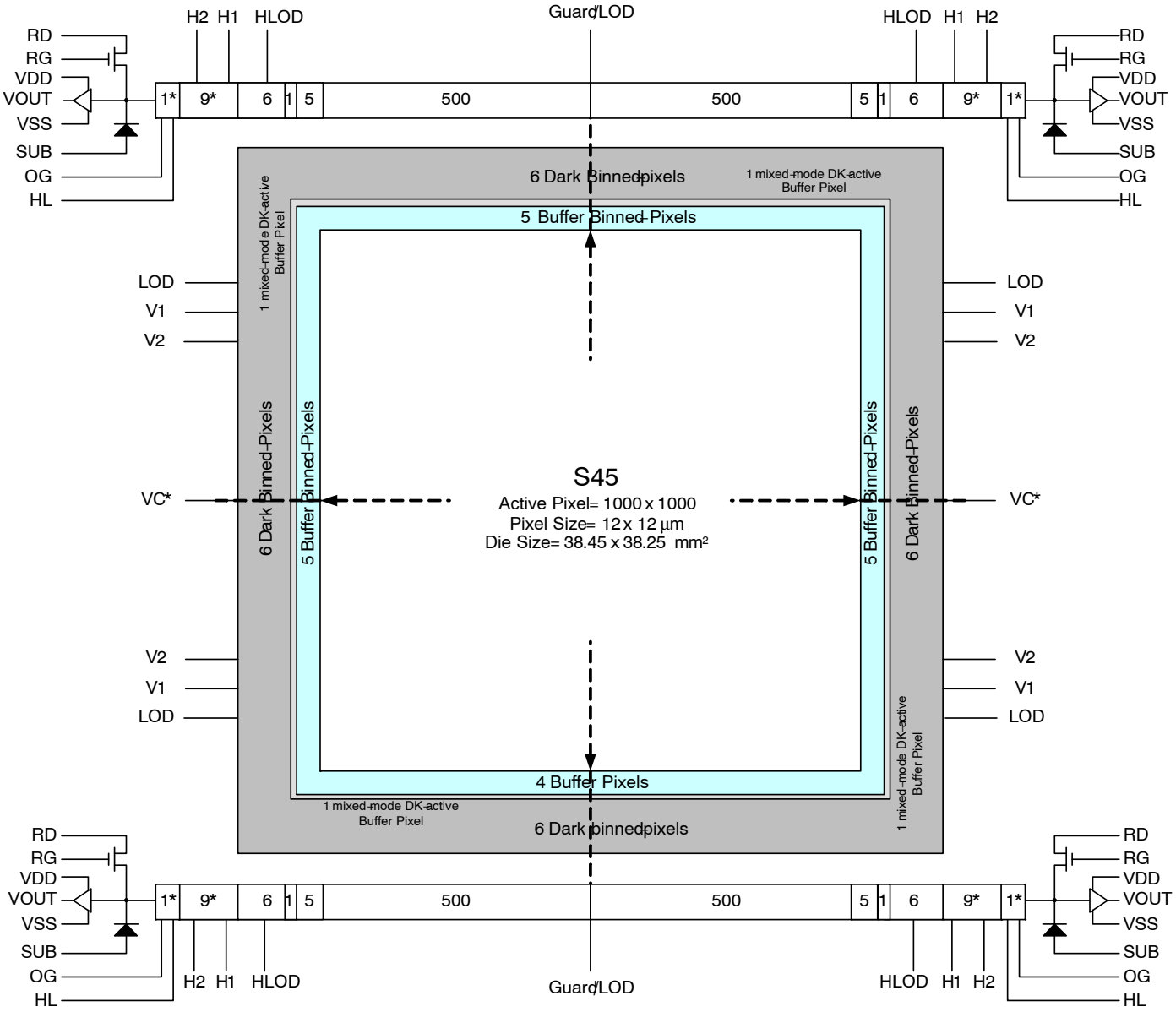
DEVICE DESCRIPTION

Architecture



- 3024 x 3024 active pixels with 12 µm pixel size.
- 3072 x 3072 total pixels including active, buffer, and dark pixels
- 10 leading dummy pixels in horizontal in each quadrant
- VC* = Voltage control pad, to minimize center−seam artifacting
- Guard/LOD = Can be connected to LOD
- All V2 gates are internally connected

Figure 2. Block Diagram (Standard Resolution Mode)



- 1000 x 1000 active (3x3) binned-pixels with 12 µm pixel size
- 1524 x 1524 total (3x3) binned-pixels including active, buffer, and dark pixels
- 10 standard resolution leading dummy pixels in horizontal in each quadrant Clock accoridngly to standard resolution method
- VC* = Voltage control pad, to minimize center−seam artifacts
- Guard/LOD = Can be connected to LOD
- All V2 gates are internally connected

Figure 3. Block Diagram (3x3 Binning Mode) − One Possible Approach

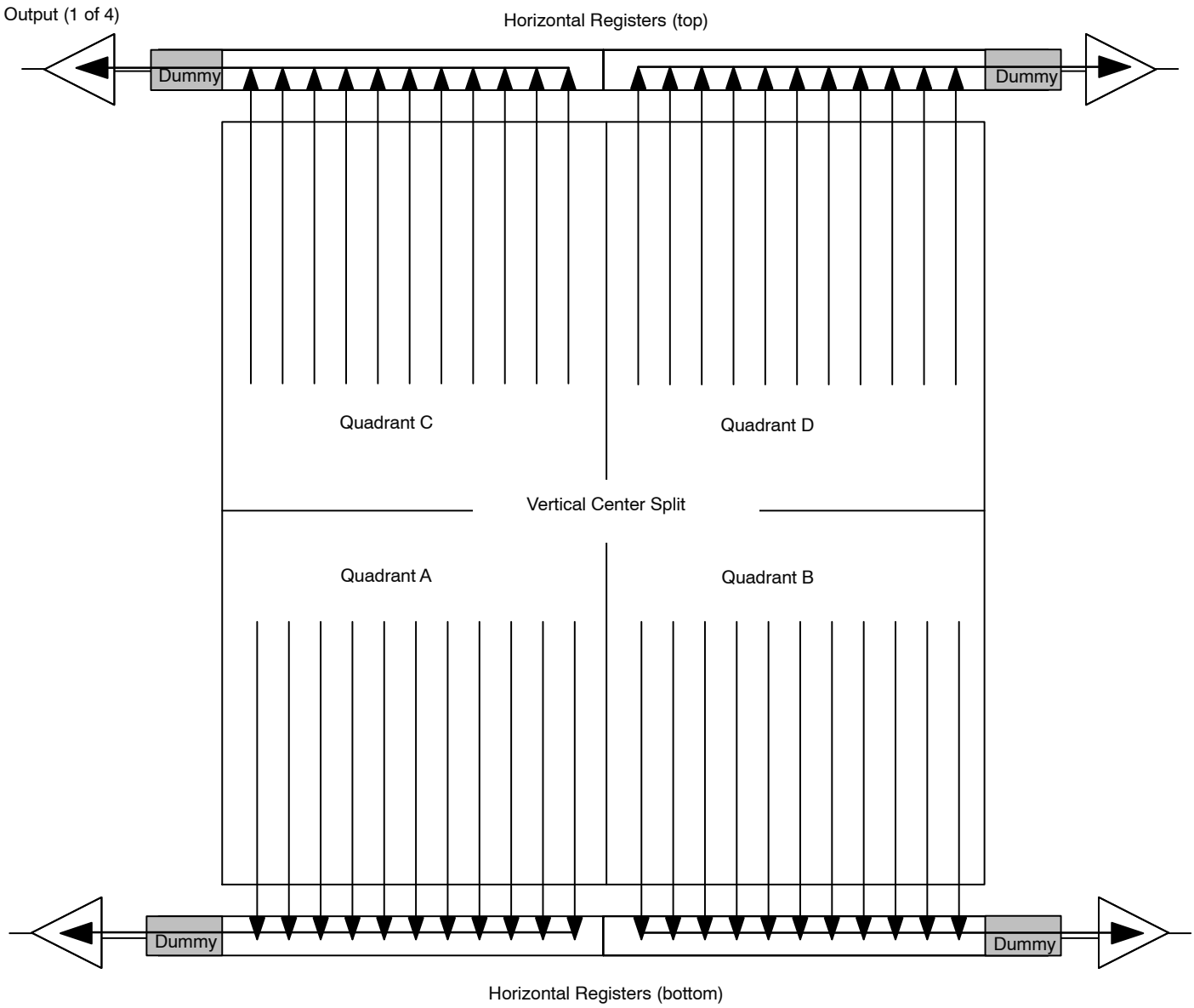


Figure 4. General Sensor Architecture

Imaging Area

The imaging area is composed of active photogates (pixels). The imaging area is arranged in 4 quadrants to facilitate increased frame rate. Some of the pixels in each quadrant are specially purposed to assist in acquiring an accurate and robust image. The specially purposed sections of the imaging area are described below.

The leading 10 pixels of each line are considered Dummy Pixels. The Dummy Pixels are not described in the Imaging Area section of this description. In actuality, the Dummy Pixels are not associated with any light sensitive structures, or pixels and are only extra cells required to transport the signal to the output structure. The Dummy Pixels are described in the Horizontal Register section below.

Dark Reference Pixels

The imaging area of this sensor is partitioned into quadrants. The periphery of the imaging area has its pixels specially shielded from light. The light shielded pixels are arranged in a border of light creating a dark region. The dark region includes 20 leading dark pixels at the start of every line in a quadrant. In addition, there are also 20 full dark lines at the start of every quadrant of the imager.

Under typical circumstances, some of these pixels do not respond to light and may be used as a dark reference. In some applications it may be important to establish a robust dark reference. It is good practice to exclude several of the leading and trailing dark reference pixels in line to avoid any effects of stray signal from influencing this dark reference level. It should also be noted that some low−level defects may be present in the dark reference region that may influence line level clamping.

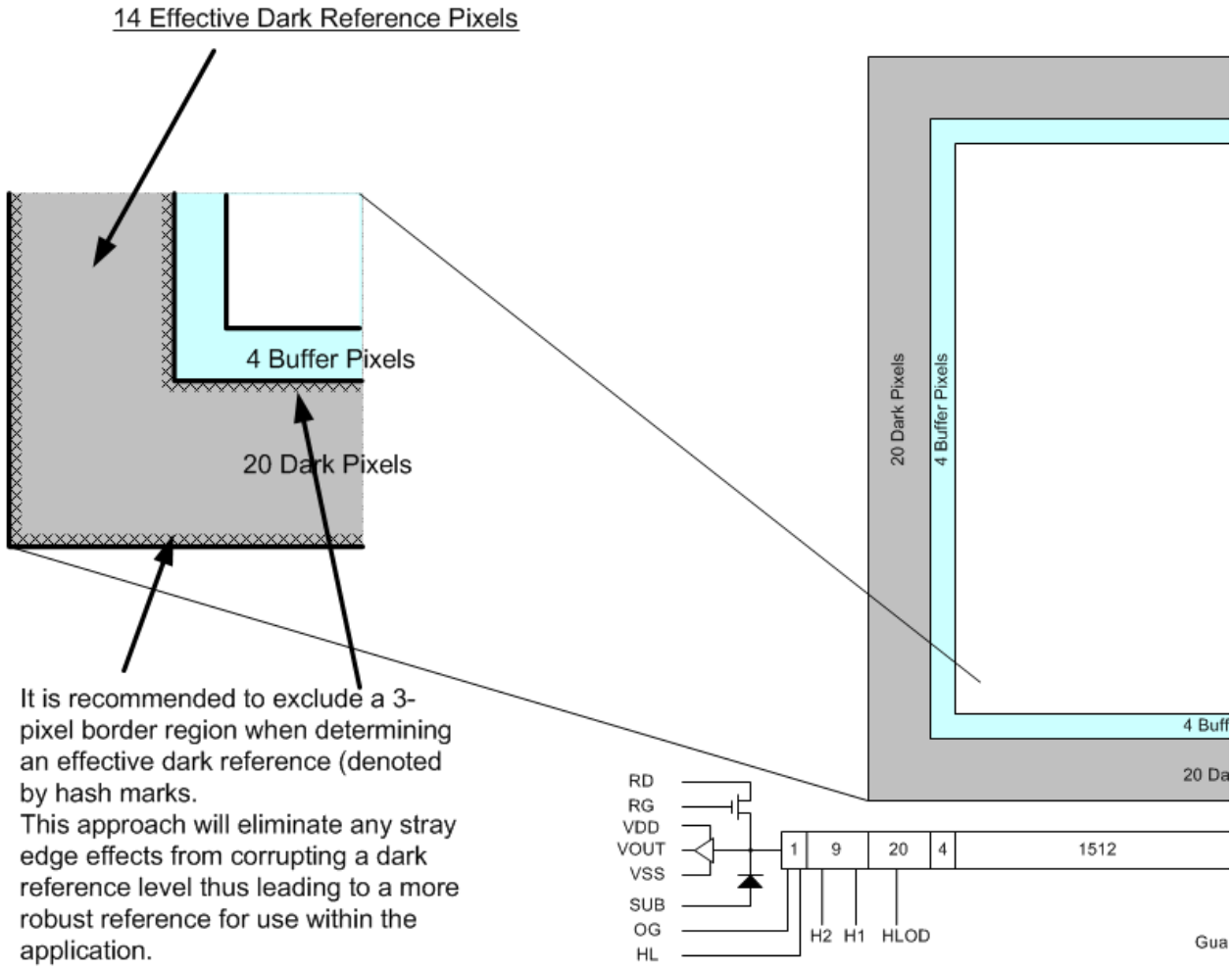


Figure 5. Effective Dark Reference Pixels (Standard Resolution Mode)

Active Buffer Pixels

Forming the outer boundary of the effective active pixel region, there are 4 unshielded active buffer pixels between the photoactive area and the dark reference. These pixels are light sensitive but they are not tested for defects and non−uniformities.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron−hole pairs within the device. These photon−induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non−linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Vertical Center Bias (VC)

The vertical center bias is applied through a gate and is wired out separately to the VC pin. A bias level can be applied to remove any extra electrons that might be caused by stray light leaking through the microlens gap at the center of the active imager array without impacting the overall image integrity. Therefore, any extra electrons can be drained away to the LOD so that the pixels of rows 1536 and 1537 will have the same amount of the signal as rows 1535 and 1538. In practical use cases, the vertical center seam difference can be narrowed within 1% in bright field image.

By design there is no detectable difference of the center seam in the dark field image.

Horizontal Register

Dummy Pixels

Within each quadrant there is a horizontal shift register that is used to clock out the image of that quadrant. As each quadrant data is clocked to the output, each image line begins with 10 leading additional shift phases 1+9 (see Figure 2). These pixels are designated as dummy pixels and are not associated with a packet of charge from a pixel element. Although the Dummy pixels will appear to clock out immediately leading the dark reference pixels of the imaging area, the Dummy pixels should not be used to determine a dark reference level for that quadrant.

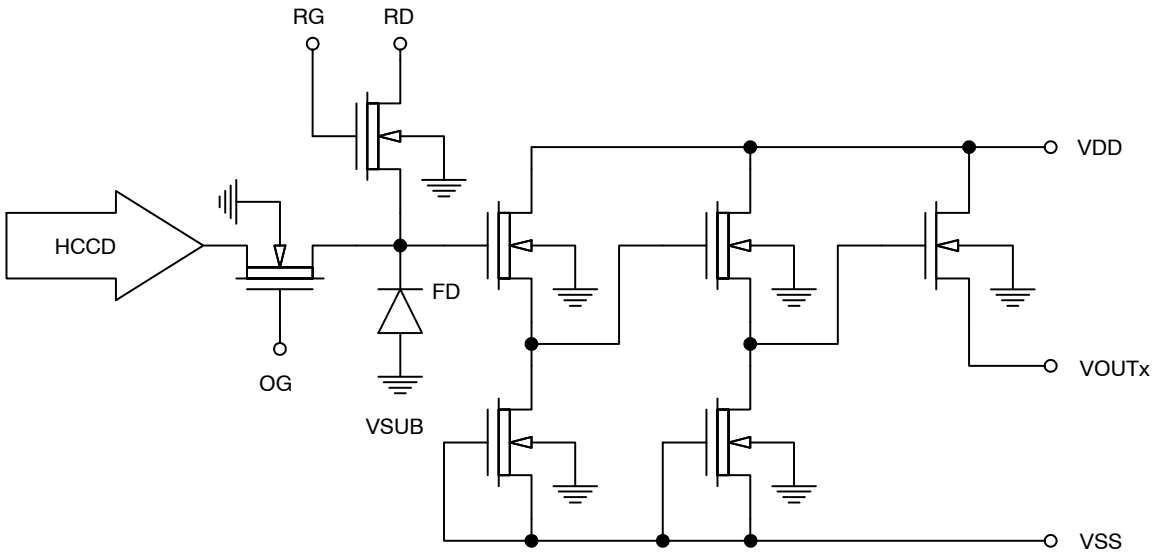
Charge Transport

The integrated charge from each photogate (pixel) is transported to the output using a two−step process. Each line (row) of charge is first transported from the vertical CCD's to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented with a new line on the falling edge of V2 while H1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion output amplifier. On each falling edge of H1L a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

HLOD

This feature is important for applications that may have large signal exposures. For instance, when operating the image sensor in binned−mode, binning multiple lines into the horizontal registers, excess charge may collect that extends beyond the HCCD charge capacity limit. The horizontal register is designed to allow this excess charge to drain off and be discarded, preventing back−blooming charge into the vertical photosites.

Output Structure

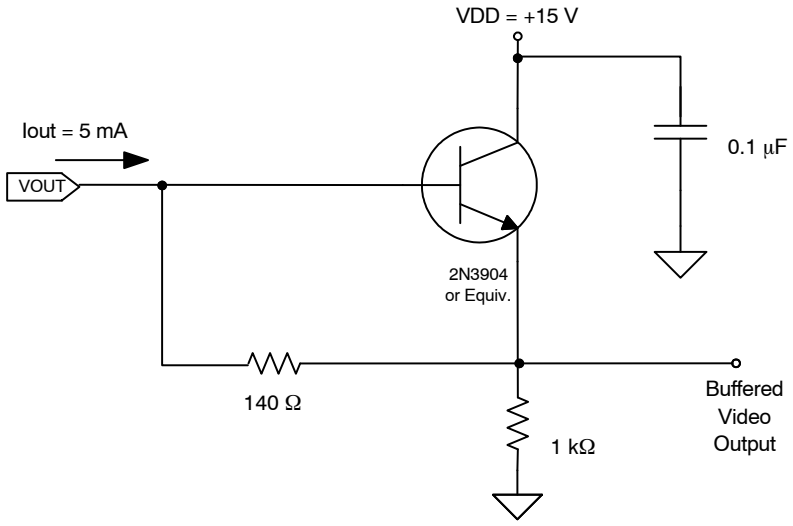


Note: Represents one of the four outputs. The designation is omitted in the figure.

Figure 6. Output Architecture (1 of 4)

The output consists of a floating diffusion capacitance connected to a three−stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off−chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structures, an off−chip current source must be added to the VOUT pins of the device. See Figure 7.

Output Load



Note: Component values may be revised based on operating conditions and other design considerations.

Figure 7. Recommended Output Structure Load Diagram

Physical Description

Pin Description and Device Orientation

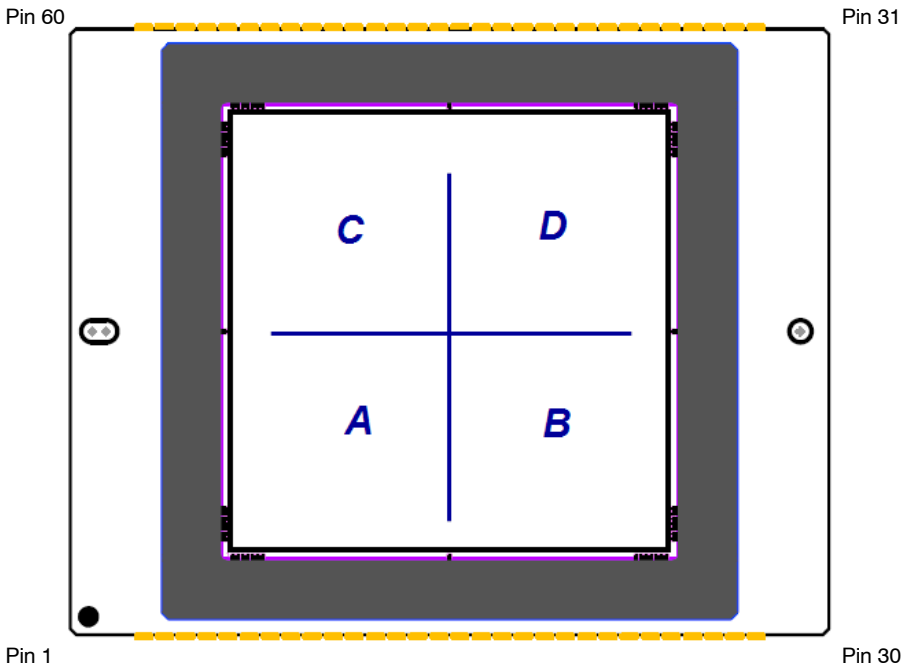


Figure 8. Pinout Diagram, showing Optical Quadrants

Device Pinout Table

Table 3. PIN DESCRIPTION

Pin	Function	Description
1	VSUB	Substrate
2	VC	Vertical gate, center
3	V2	Vertical phase 2
4	V1_bot	Vertical phase 1, bottom of die
5	LOD_bot	Lateral overflow drain, bottom of die
6	VDD_a	Amplifier supply, Output A
7	VOUT_a	Video output A
8	VSS_a	Amplifier return, Output A
9	RD_a	Reset drain, Output A
10	RG_a	Reset gate, Output A
11	OG_a	Output gate, Output A
12	HL_a	Last horizontal phase, Output A
13	HLOD_bot	Horizontal lateral overflow drain, bottom of die
14	H2_a	Horizontal phase 2, A quadrant
15	H1_a	Horizontal phase 1, A quadrant
16	Guard / LOD_bot	ESD guard / Lateral overflow drain, bottom of die
17	H1_b	Horizontal phase 1, B quadrant
18	H2_b	Horizontal phase 2, B quadrant
19	HLOD_bot	Horizontal lateral overflow drain, bottom of die
20	HL_b	Last horizontal phase, Output B
21	OG_b	Output gate, Output B
22	RG_b	Reset gate, Output B
23	RD_b	Reset drain, Output B
24	VSS_b	Amplifier return, Output B
25	VOUT_b	Video output B
26	VDD_b	Amplifier supply, Output B
27	LOD_bot	Lateral overflow drain, bottom of die
28	V1_bot	Vertical phase 1, bottom of die
29	V2	Vertical phase 2
30	VSUB	Substrate

Pin	Function	Description
31	VSUB	Substrate
32	VC	Vertical gate, center
33	V2	Vertical phase 2
34	V1_top	Vertical phase 1, top of die
35	LOD_top	Lateral overflow drain, top of die
36	VDD_d	Amplifier supply, Output D
37	VOUT_d	Video output D
38	VSS_d	Amplifier return, Output D
39	RD_d	Reset drain, Output D
40	RG_d	Reset gate, Output D
41	OG_d	Output gate, Output D
42	HL_d	Last horizontal phase, Output D
43	HLOD_top	Horizontal lateral overflow drain, top of die
44	H2_d	Horizontal phase 2, D quadrant
45	H1_d	Horizontal phase 1, D quadrant
46	Guard / LOD_top	ESD guard / Lateral overflow drain, top of die
47	H1_c	Horizontal phase 1, C quadrant
48	H2_c	Horizontal phase 2, C quadrant
49	HLOD_top	Horizontal lateral overflow drain, top of die
50	HL_c	Last horizontal phase, Output C
51	OG_c	Output gate, Output C
52	RG_c	Reset gate, Output C
53	RD_c	Reset drain, Output C
54	VSS_c	Amplifier return, Output C
55	VOUT_c	Video output C
56	VDD_c	Amplifier supply, Output C
57	LOD_top	Lateral overflow drain, top of die
58	V1_top	Vertical phase 1, top of die
59	V2	Vertical phase 2
60	VSUB	Substrate

IMAGING PERFORMANCE

Typical Operational Conditions

Unless otherwise noted, the Specifications are measured using the following conditions.

Table 4. TYPICAL OPERATIONAL CONDITIONS

Description	Condition	Notes
Readout Time ($t_{readout}$)	191 ms Standard Resolution 85.5 ms Binned Mode	Includes Overclock Pixels
Integration Time (t_{int})	Varies per test: Bright Field 250 ms, Dark Field 1 s, Saturation 250 ms, Low light 33 ms	
Horizontal Clock Frequency	20 MHz	
Temperature	Approximately 25°C	As tested at room temperature, although the device may operate at temperatures approaching 50°C without external cooling or air flow. See Figure 10 for the typical factory test temperature
Mode	Integrate − Readout Cycle	

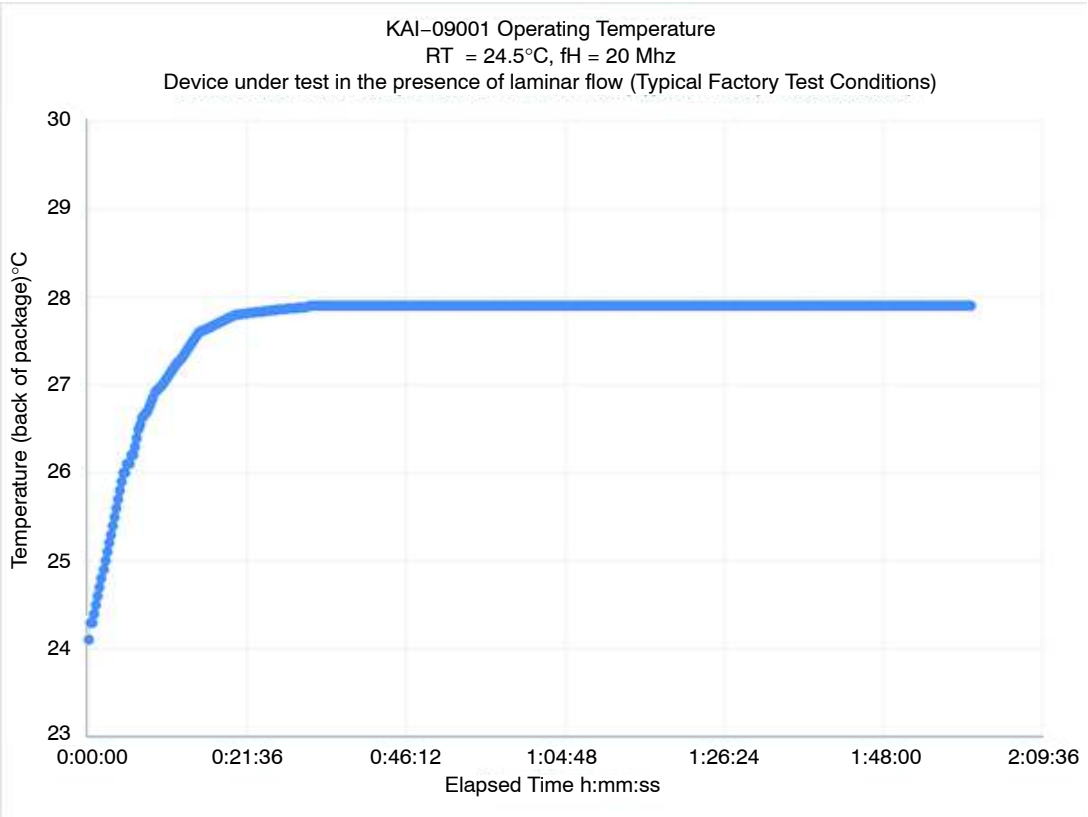


Figure 9. Typical Factory Test Temperature (measured at back of package)

Specifications

Table 5. SPECIFICATIONS, FULL RESOLUTION MODE

	Symbol	Min	Nom	Max	Units	Verification Plan
Saturation Signal	N_{e-sat}	90	110		ke⁻	Die (Note 11)
Quantum Efficiency (550 nm) (Note 1)	QE		64		%	Design (Note 12)
Photo Response Non−Linearity (Note 2)	PRNL		1		%	Design (Note 12)
Photo Response Non−Uniformity (Note 3)	PRNU	−10	0.6	10	%	Die (Note 11)
Integration Dark Signal (Note 4)	Vdark, int		7	20	e/pix/sec	Design (Note 12)
			0.84	2.8	pA/cm^2	
			0.8	4.8	mV/s	Die (Note 11)
Readout Dark Signal (Note 5)	Vdark, read		80	320	e⁻	Design (Note 12)
			2	20	mV/s	Die (Note 11)
Dark Signal Non−Uniformity (Note 6)	DSNU			20	e/pix/sec	Design (Note 12)
			0.3	6.64	mV	Die (Note 11)
Dark Signal Doubling Temperature	DT		5		°C	Design (Note 12)
Read Noise (Note 7)	NR		7		e⁻rms	Design (Note 12)
Linear Dynamic Range (Note 8)	DR		84		dB	Design (Note 12)
Blooming Protection (Note 9)	Xab		>1000		X Vsat	Design (Note 12)
Output Amplifier Sensitivity	V_{out}/N_{e-Xab}		24		μV/e	Design (Note 12)
DC Offset, output amplifier (Note 10)	V_{odc}	8	9	10	V	Die (Note 11)
Output Amplifier Bandwidth	f_{-3dB}		88		MHz	Design (Note 12)
Output Impedance, Amplifier	R_{OUT}		116	250	Ω	Die (Note 11)
Center Seam Correction Variation	ΔCS_Corr		0.1	2	%	Die (Note 11)

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst case deviation from straight line fit, between 0% and 65% of Vsat.
3. One Sigma deviation of a 128 x 128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25°C.
5. Read out dark current depends on the read out time, primarily when the vertical CCD clocks are at their high levels. This value, calculated by design, is approximately 0.125 sec/image for nominal timing conditions, tVw = 20 μs. The read out dark current will increase as tVw is increased. The readout dark current and noise performance is also dependent on the operating temperature. The specification applies to 25°C.
6. Average integration dark signal of any of 32 x 32 blocks within the sensor (Each block is 128 x 128 pixels).
7. Output amplifier noise only. Operating at pixel frequency up to 4 MHz, bandwidth < 20 MHz, t_{int} = 0, and no dark current shot noise.
8. 20log (V_{sat}/V_N)
9. Xab is the number of times above the V_{sat} illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. Xab is measured at 4 ms.
10. Video level offset with respect to ground.
11. A parameter that is measured on every sensor during production testing.
12. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

Figure 10. Typical Quantum Efficiency

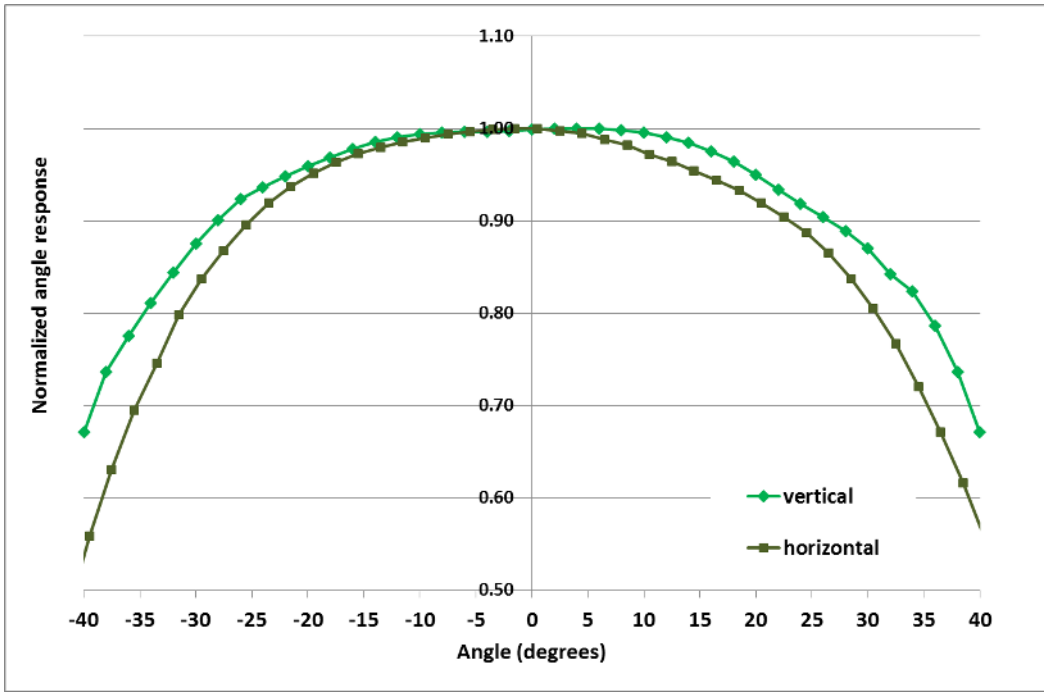


Figure 11. Typical Vertical and Horizontal Angular Dependence of Quantum Efficiency

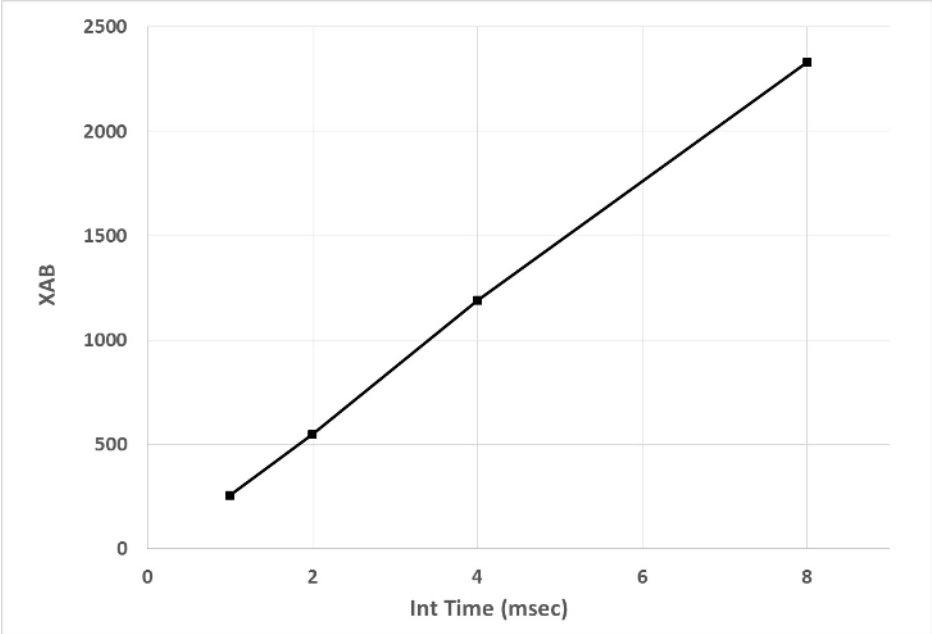


Figure 12. Typical Anti−blooming Performance: Signal vs. Exposure

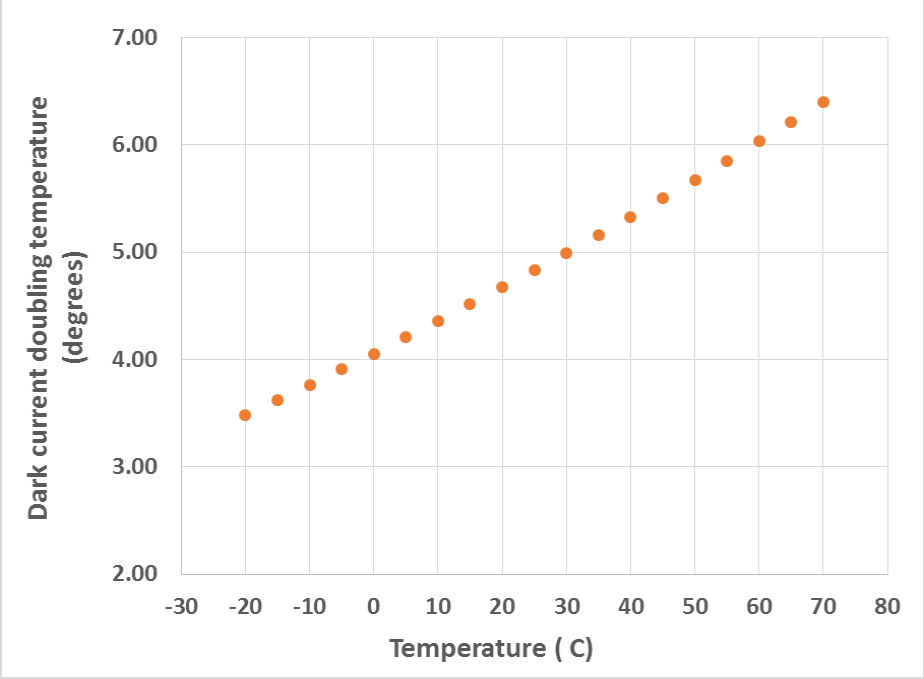


Figure 13. Dark Current Doubling Temperature

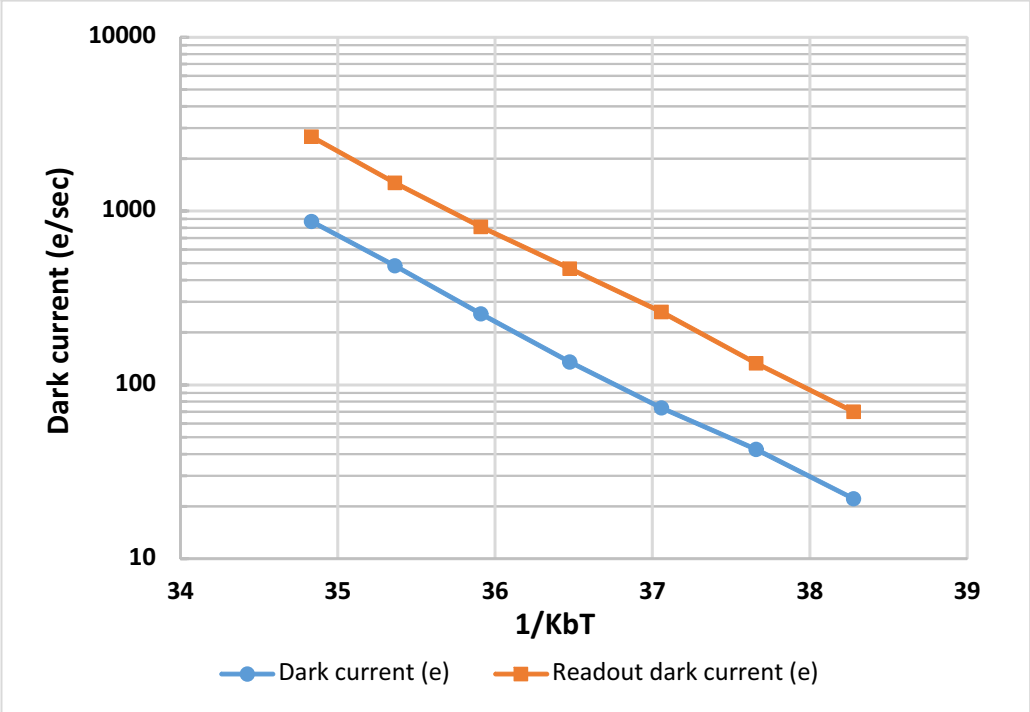


Figure 14. Typical Dark Current Performance vs. Temperature

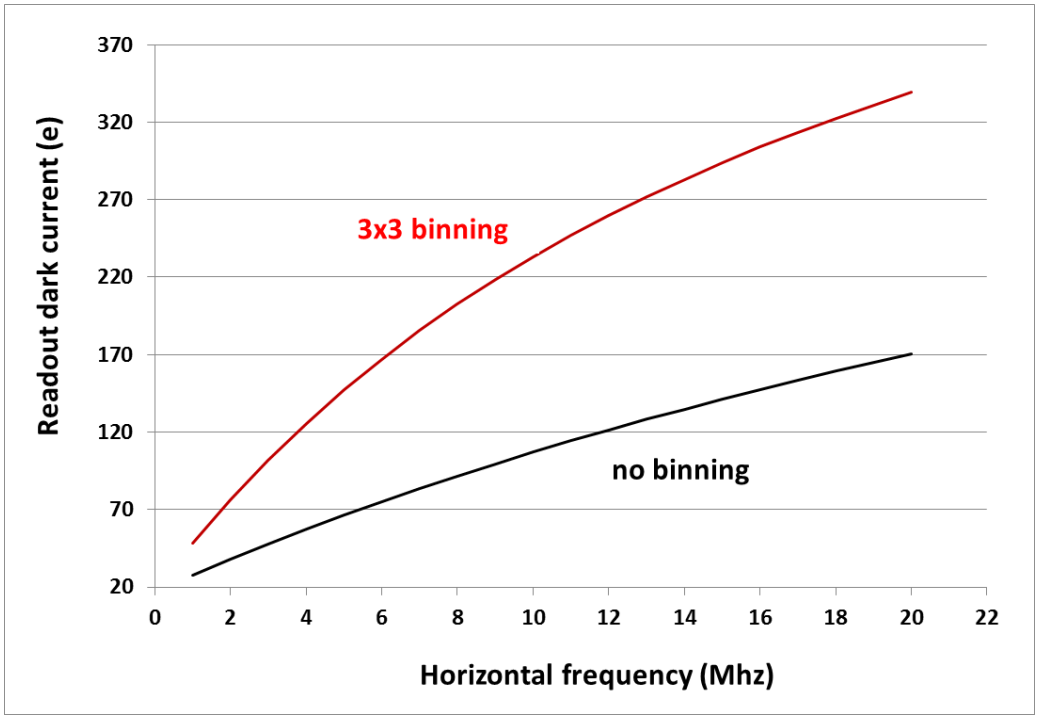


Figure 15. Readout Dark Current vs. Horizontal Clock Frequency

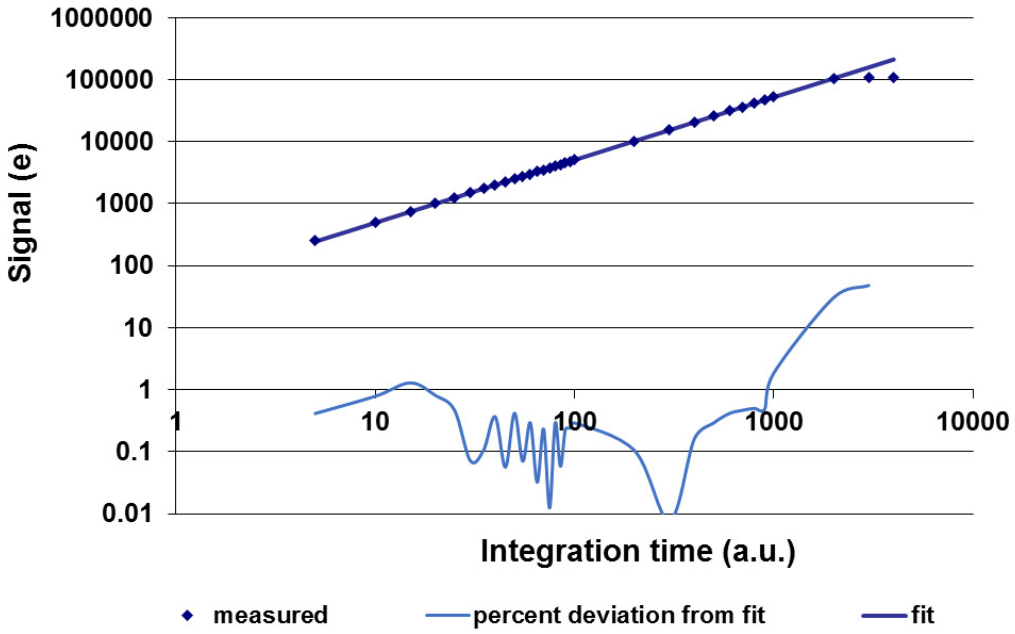


Figure 16. Typical Linearity Performance: Standard Resolution (20 MHz)

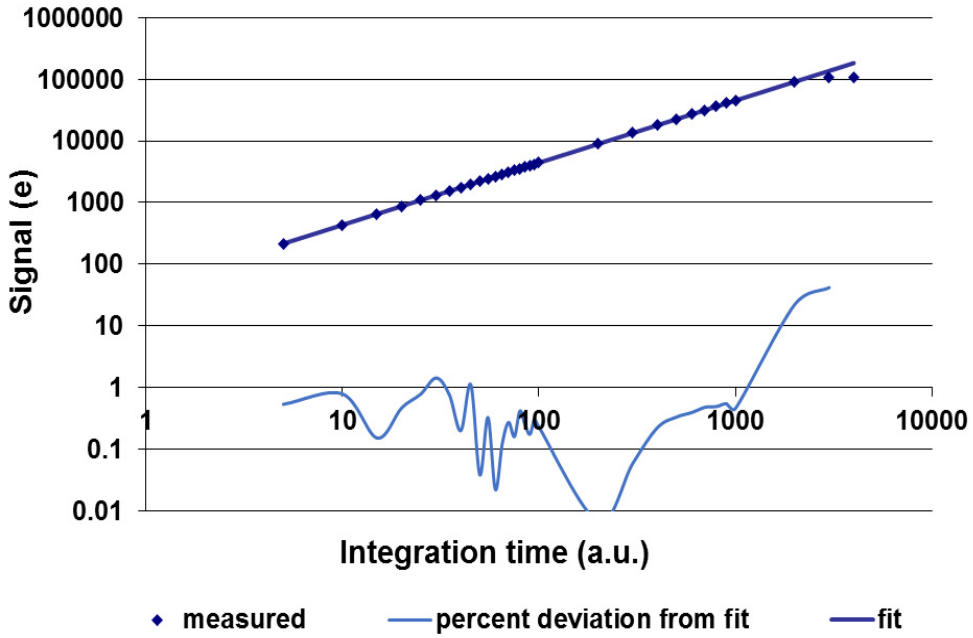


Figure 17. Typical linearity Performance: 3x3 Binned Resolution (20 MHz)

DEFECT DEFINITIONS

Operating Conditions and Standard Resolution

Bright defect tests performed at T = 25°C, t_{int} = 250 ms

Dark defect tests performed at T = 25°C, t_{int} = 1000 ms

Table 6. SPECIFICATIONS

Classification	Points	Clusters	Columns
Standard Grade	≤ 200	≤ 20	< 10

Defect Definition:

Point Defects

A pixel that deviates by more than 72 mV above neighboring pixels under non−illuminated conditions

−or−

A pixel that deviates by more than 6% above or below neighboring pixels under illuminated conditions

Cluster Defect

A grouping of adjacent point defects that can number in size from 2 to 10 pixels.

Cluster Separation

Cluster defects are separated by no less than 4 good pixels in any direction.

Column Defect

A grouping of more than 10 point defects along a single column.

−or−

A column that deviates by more than 1.5mV above neighboring columns under non−illuminated conditions [dk fld br col]

−or−

A column that deviates by more than 6% above or below neighboring columns under illuminated conditions

Column Separation

Column defects are separated by no less than 4 good pixels in any direction. No multiple column defects (double or more) will be permitted.

Dead Column

A column that deviates by more than 50% below neighboring columns under illuminated conditions.

Saturated Columns

A column that deviates by more than 100 mV above neighboring columns under non−illuminated conditions. No saturated columns are allowed.

Trap Defects

A group of pixels, which loses more than 6 mV under 13 mV illumination.

OPERATION

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If the level or condition is exceeded damage may occur. The device will then be degraded and device functionality should not be assumed or reliability may be affected.

Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units
Diode Pin Voltages (Note 1, 2)	V_{diode}	−0.5	20	V
Adjacent Gate Pin Voltages (Note 1, 3)	V_{gate1}	−18	18	V
Isolated Gate Pin Voltages (Note 4)	V_{1-2}	−0.5	20	V
Output Bias Current (Note 5)	I_{out}		−30	mA
LOD Diode Voltage (Note 6)	V_{LOD}	−0.5	13.0	V
Operating Temperature (Note 7, 8)	T_{OP}	−50	60	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin SUB
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H2, VOG, VC
4. Includes pins: RG.
5. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
6. V1, H1, V2, H2, H1L, VOG, VC and RD are tied to 0 V.
7. Noise performance will degrade at higher temperatures due to the temperature dependence of the dark current.
8. Image performance will degrade at lower temperatures due to increasing transfer inefficiency. Below −40°C the device should be operated at frequencies below 10 MHz.

Power−up Sequence

The sequence chosen to perform an initial power−up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (VSUB).
2. Supply the appropriate biases and clocks to the remaining pins.

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Effective Capacitance
Reset Drain	RD	12.8	13.0	13.2	V	
Output Amplifier Return	VSS	1.8	2.0	2.2	V	
Output Amplifier Supply	VDD	14.8	15.0	17.0	V	
Substrate	SUB		0		V	−
Output Gate	OG	−0.2	0	0.2	V	C_{OG} 10 pF
Vertical Lateral Overflow Drain	VLOD	8.2	9.0	9.2	V	
Horizontal Lateral Overflow Drain	HLOD	11.8	12.0	12.2	V	
Video Output Load Current (Note 1)	I_{OUT}	−3.0	−5.0	−7.0	mA	
Vertical Gate, Center	VC	−2.5	−2.25	−2.0	V	

1. An output load sink must be applied to the VOUT pin to activate output amplifier − see Figure 6 and 7.

AC Operating Conditions

Table 9. CLOCK LEVELS

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance
Vertical CCD Clock − Phase 1	V1	Low	−9.2	−9.0	−8.8	V	C_{V1} 90 nF
		High	2.3	2.5	2.7	V	
Vertical CCD Clock − Phase 2	V2	Low	−9.2	−9.0	−8.8	V	C_{V2} 135 nF
		High	2.3	2.5	2.7	V	
Horizontal CCD Clock − Phase 1*	H1	Low	−3.2	−3.0	−2.8	V	C_{H1} 290 pF
		High	2.8	3.0	3.2	V	
Horizontal CCD Clock − Phase 2*	H2	Low	−3.2	−3.0	−2.8	V	C_{H2} 210 pF
		High	2.8	3.0	3.2	V	
Horizontal CCD Clock − Phase 1 (Last)	H1L	Low	−5.2	−5.0	−4.8	V	C_{H1L} 10 pF
		High	2.8	3.0	3.2	V	
Reset Gate	RG	Low	4.8	5.0	5.2	V	C_{OG} 10 pF
		High	10.8	11.0	11.2	V	

1. All capacitance values in the table are estimated values and they are for single quadrant. If one clock driver drives all similar pins, then the capacitance value for that pin needs to be multiplied by 4.

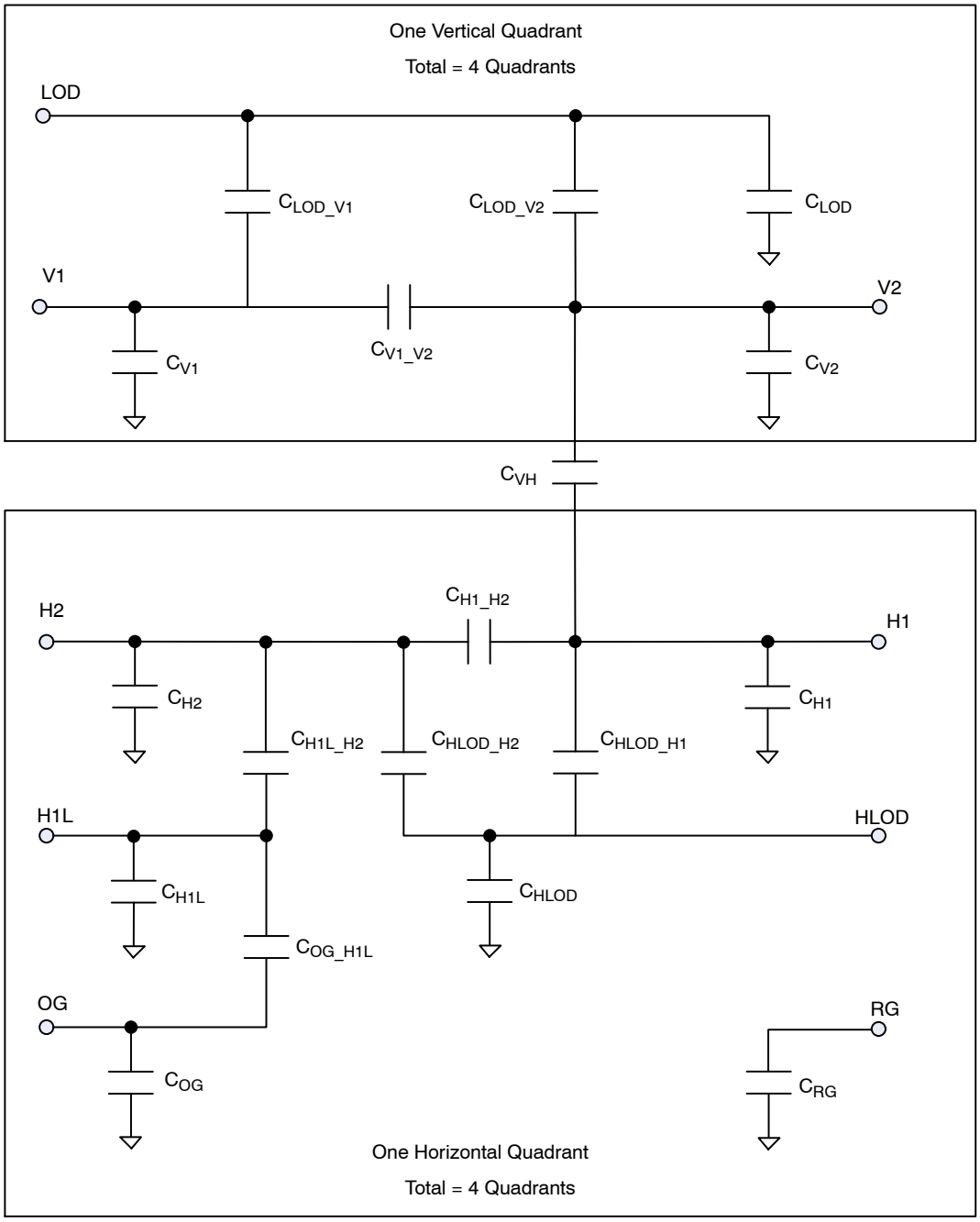


Figure 18. Capacitance Model

Requirements and Characteristics

Table 10. FULL RESOLUTION MODE

Description	Symbol	Minimum	Nominal	Maximum	Units
H1, H2 Clock Frequency (Notes 1, 2)	f_H		20	20	MHz
V1, V2 Rise, Fall Times	t_{V1r}, t_{V1f}	3	3		μs
V1 − V2 Cross−over	V_{VCR}	−1	0	1	V
H1 − H2 Cross−over	V_{HCR}		0		V
H1L Rise − H2 Fall Crossover	V_{H1LCR}		−0.5		V
V_{CCD} to H_{CCD} Transfer	T_{vh}		5		μs
H1, H2 Setup Time	t_{HS}	5			μs
RG Clock Pulse Width (Note 6)	t_{RGw}	3.2	5		ns
V1, V2 Clock Pulse High	t_v	10	10		μs
Pixel Period (1 Count) (Note 2)	t_e		50		ns

Table 11. FULL RESOLUTION TIMING DESCRIPTION (USING ABOVE NOMINAL CONDITIONS)

Description	Symbol	No Overclocking	As tested, with Overclocking	Units
Line Time	t_{line}	110.13	117.8	μs
Readout Time (Note 3)	$t_{readout}$	169.15	191.05	ms
Frame Time (Note 5)	t_{frame}	−	1916	ms
Frame Rate (Note 5)	F_{rate}	−	0.84	fps
Integration Time (Note 4)	t_{int}	−	varies	
Integration Time, testing bright field (Note 4)		−	250	ms
Integration Time, testing dark field (Note 4)		−	1000	ms
Integration Time, testing at saturation (Note 4)		−	250	ms
Integration Time, testing low light (Note 4)		−	33	ms

Table 12. BINNED (3x3) RESOLUTION TIMING DESCRIPTION (USING ABOVE NOMINAL CONDITIONS)

Description	Symbol	No overclocking	As tested, with overclocking	Units
Line Time	t_{line}	157.43	166.55	μs
Readout Time (Note 3)	$t_{readout}$	80.6	85.3	ms
Frame Time (Note 5)	t_{frame}	−	118.2	ms
Frame Rate (Note 5)	F_{rate}	10	8.5	fps
Integration Time (Note 4)	t_{int}	20	33.3	ms
Integration Time, testing bright field (Note 4)		−	250	ms
Integration Time, testing dark field (Note 4)		−	1000	ms
Integration Time, testing at saturation (Note 4)		−	250	ms
Integration Time, testing low light (Note 4)		−	33	ms

1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. $t_{readout} = t_{line}$ * 1536 lines (+ any overlocked lines)
4. Integration time is user specified.
5. Frame rate depends on the value of integration time which is user specified.
6. The Reset Gate Clock High (minimum value), as stated in Table 9, must be maintained, or exceeded, for this duration in order to be effective.

Edge Alignment

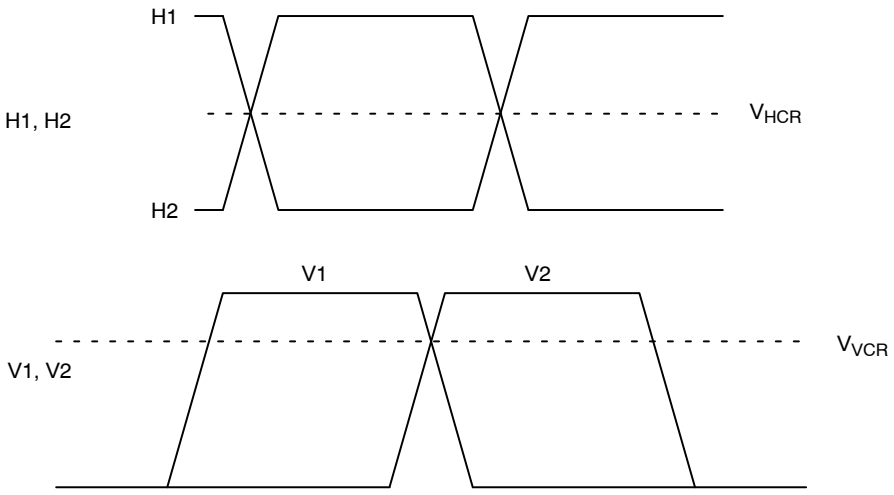


Figure 19. Timing Edge Alignment

Frame Timing

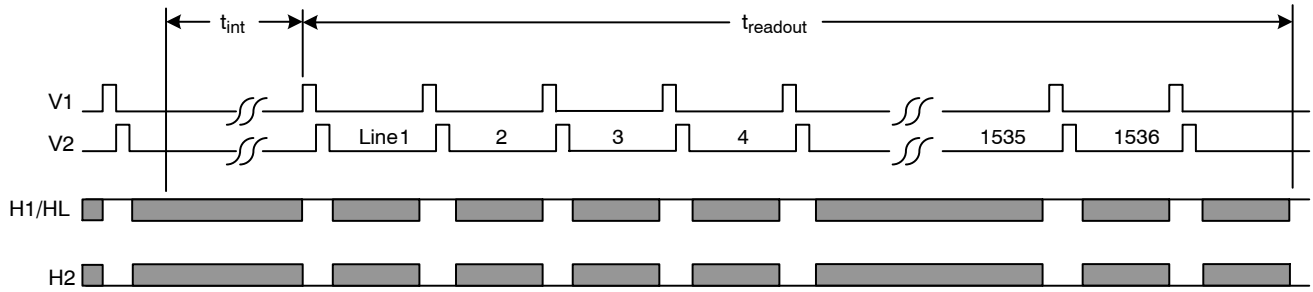


Figure 20. Frame Timing

Frame Timing Detail

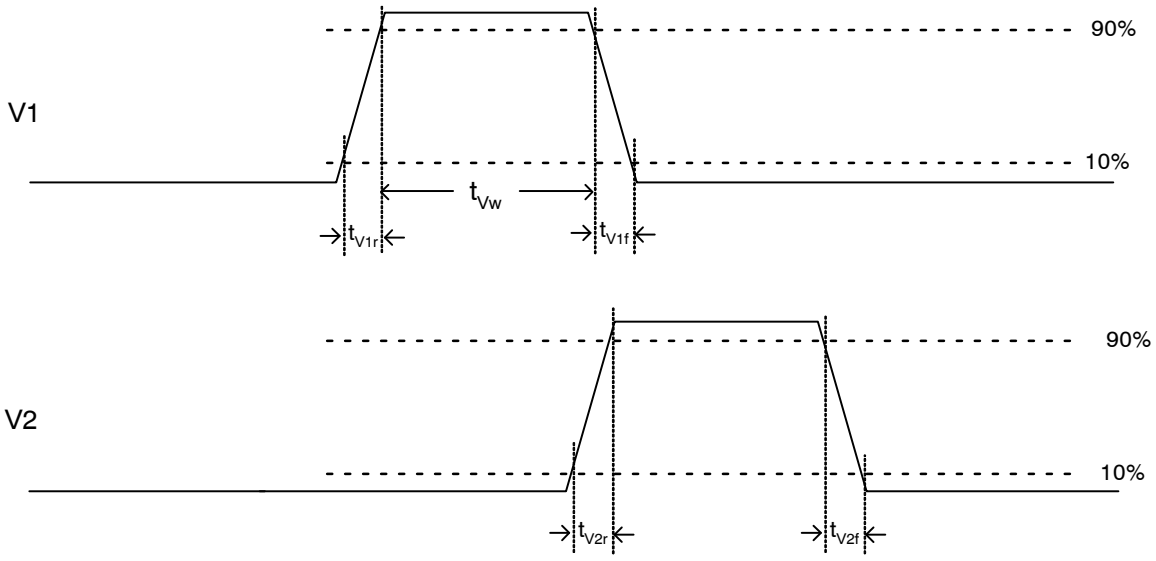


Figure 21. Frame Timing Detail

Standard Resolution Readout

Standard Resolution Readout (per quadrant output, each output contains half of the lines and half of the columns).

Line Timing

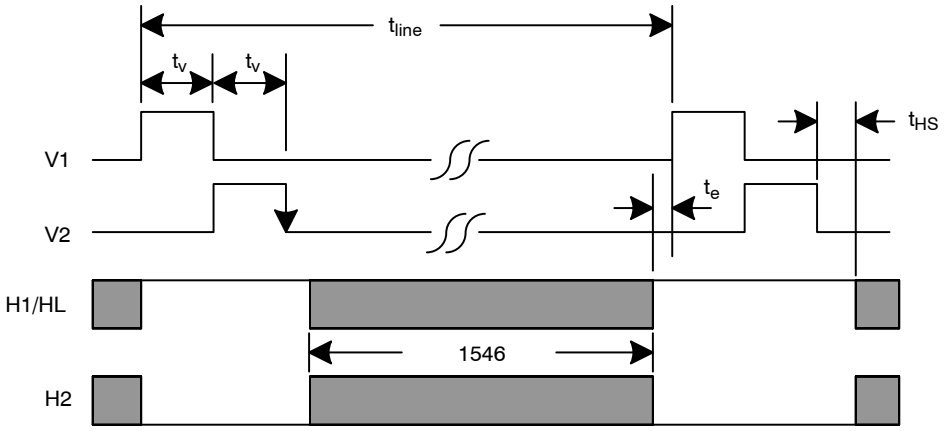


Figure 22. Line Timing

Pixel Timing

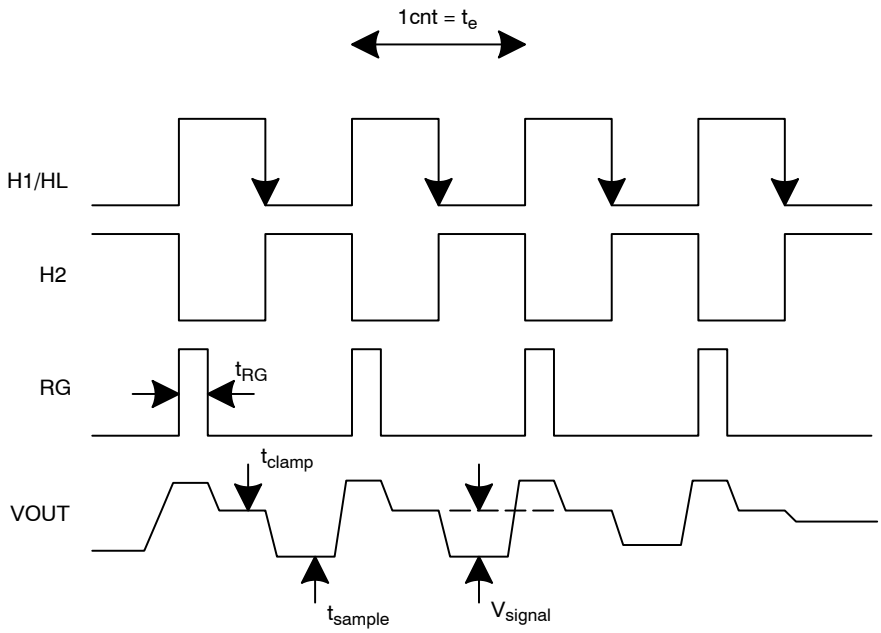


Figure 23. Pixel Timing

3 x 3 Binning − Readout

Line Timing − Binning Three Lines into the Horizontal CCD

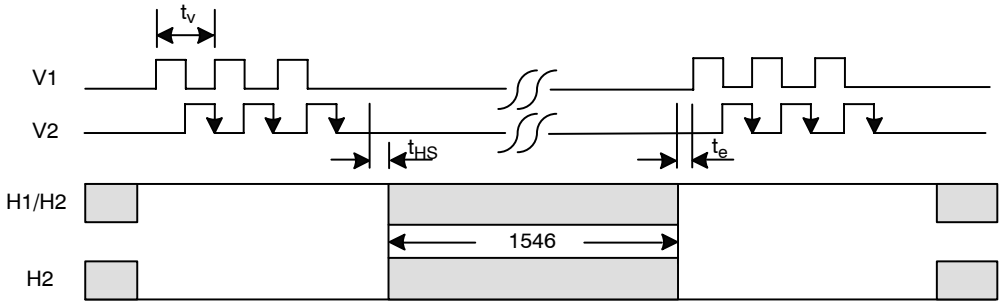


Figure 24. Line Timing (3x3 Binning)

Pixel Timing − Binning Three Pixels at the Output

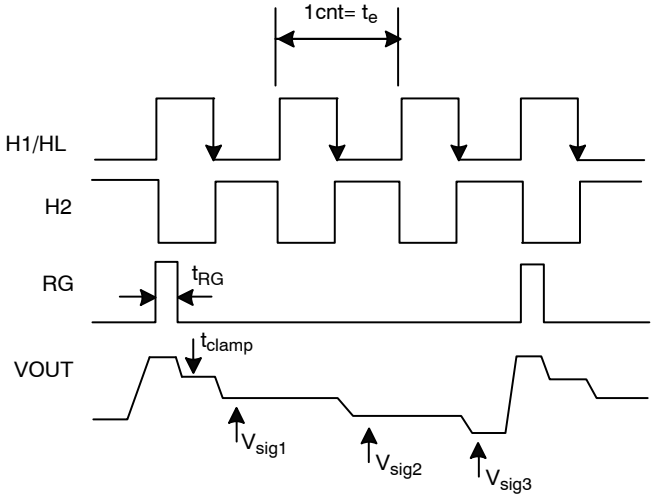


Figure 25. Pixel Timing (3x3 Binning)

Flush Timing

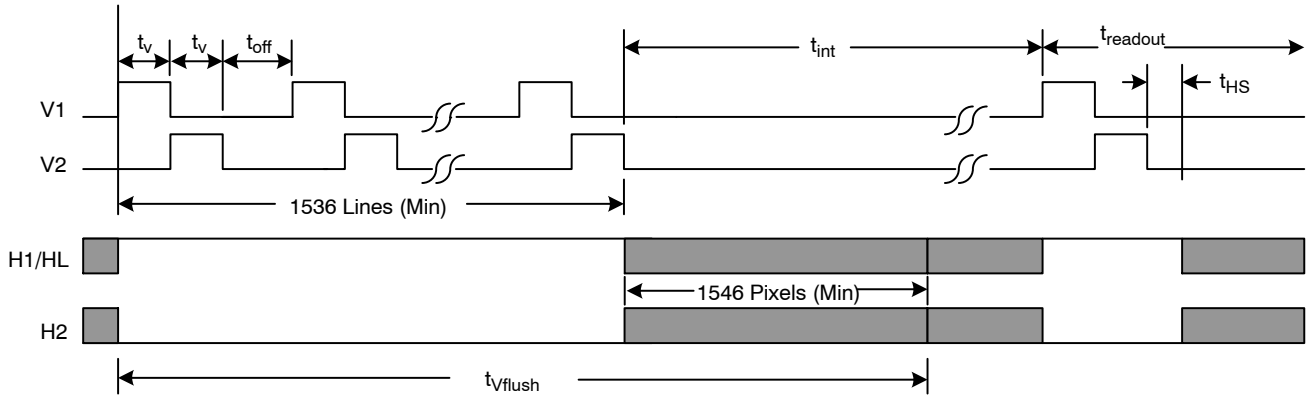


Figure 26. Flush Timing

STORAGE AND HANDLING

Table 13. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units
Storage Temperature (Note 1)	T_{ST}	−20	70	°C
Humidity (Note 2)	RH	5	70	%

1. Long term storage toward the maximum temperature will degrade spectral response.
2. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D).

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D).

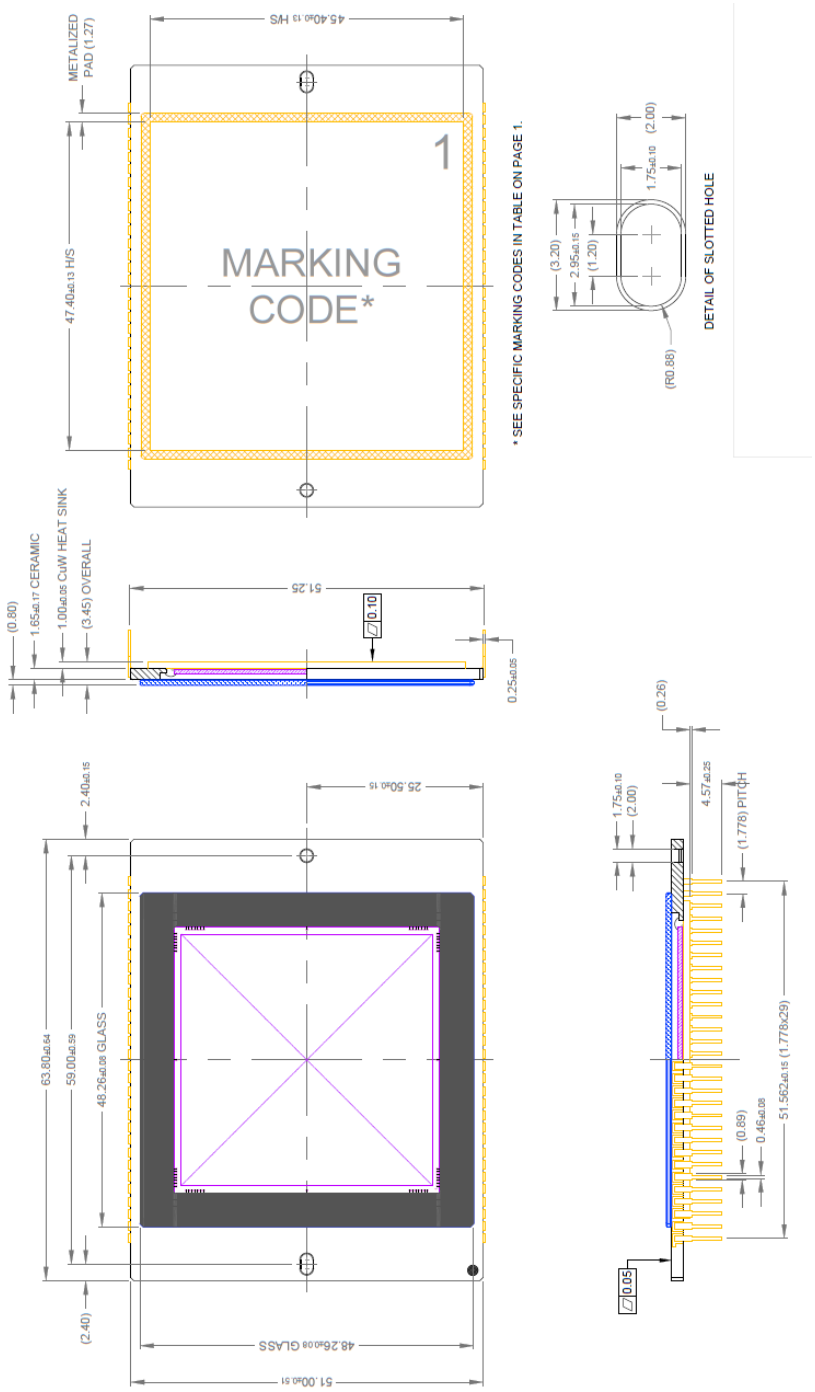
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D).

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D).

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly



NOTES:

1. Applications and assemblies that use the KAF−09001 image sensor that are subject to high impact mechanical shock are advised to provide mechanical and stabilized support for the ends of the ceramic package. The portion of the package that extends beyond the cover glass and device pins should be supported securely so as it is not to fracture when subjected to situations of high levels of shock, such as defined that exceed the standard enforced at the time of production release, MIL−STD−883K, Method 2002.5, Condition A, (500G).
2. The thru−holes provided are for alignment.

Figure 27. Completed Assembly Drawing

Cover Glass Specification

1. Scratch and dig: 20 micron max
2. Substrate material: Schott D263T eco @ 0.76 mm thickness
3. Multilayer anti−reflective coating or Clear (See Ordering Information)

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