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LMH6657/LMH6658

270MHz Single Supply, Single & Dual Amplifiers

General Description

The LMH6657/6658 are low-cost operational amplifiers that operate from a single supply with input voltage range extending below the V^- . Based on easy to use voltage feedback topology and boasting fast slew rate (700V/ μ s) and high speed (140MHz GBWP), the LMH6657 (Single) and LMH6658 (dual) can be used in high speed large signal applications. These applications include instrumentation, communication devices, set-top boxes, etc.

With a -3dB BW of 100MHz ($A_v = +2$) and DG & DP of 0.03% & 0.10° respectively, the LMH6657/6658 are well suited for video applications. The output stage can typically supply 80mA into the load with a swing of about 1V from either rail.

For Industrial applications, the LMH6657/6658 are excellent cost-saving choices. Input referred voltage noise is low and the input voltage can extend below V^- to ease amplification of low level signals that could be at or near the system ground. With low distortion and fast settling, LMH6657/6658 can provide buffering for A/D and D/A applications.

The LMH6657/6658 versatility and ease of use is extended even further by offering these high slew rate, high speed Op Amps in miniature packages such as SOT23-5, SC70, SOIC-8, and MSOP-8. Refer to the Ordering Information section for packaging options available for each device.

Features

$V_S = 5V$, $T_A = 25^\circ C$, $R_L = 100\Omega$ (Typical values unless specified)

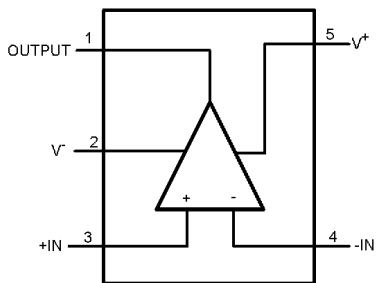
- -3dB BW ($A_v = +1$) 270MHz
- Supply voltage range 3V to 12V
- Slew rate, ($V_S = \pm 5V$) 700V/ μ s
- Supply current 6.2mA/amp
- Output current +80/-90mA
- Input common mode volt. 0.5V beyond V^- , 1.7V from V^+
- Output voltage swing ($R_L = 2k\Omega$) 0.8V from rails
- Input voltage noise 11nV/ \sqrt{Hz}
- Input current noise 2.1pA/ \sqrt{Hz}
- DG error 0.03%
- DP error 0.10°
- THD (5MHz) -55dBc
- Settling time (0.1%) 37ns
- Fully characterized for 5V, and $\pm 5V$
- Output overdrive recovery 18ns
- Output short circuit protected (Note 10)
- No output phase reversal with CMVR exceeded

Applications

- CD/DVD ROM
- ADC buffer amp
- Portable video
- Current sense buffer
- Portable communications

Connection Diagrams

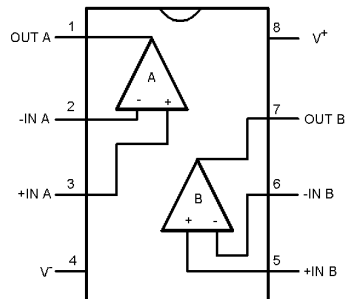
SOT23-5/SC70-5 (LMH6657)



Top View

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SOIC-8/MSOP-8 (LMH6658)



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance	
Human Body Model	2KV (Note 2)
Machine Model	200V (Note 9)
V_{IN} Differential	$\pm 2.5V$
Output Short Circuit Duration	(Note 3), (Note 11)
Input Current	$\pm 10mA$
Supply Voltage ($V^+ - V^-$)	12.6V
Voltage at Input/Output pins	$V^+ + 0.8V, V^- - 0.8V$
Soldering Information	
Infrared or Convection (20 sec.)	235°C

Wave Soldering (10 sec.)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature (Note 4)	+150°C

Operating Ratings (Note 1)

Supply Voltage ($V^+ - V^-$)	3V to 12V
Operating Temperature Range (Note 4)	-40°C to +85°C
Package Thermal Resistance (θ_{JA}) (Note 4)	
SC70	478°C/W
SOT23-5	265°C/W
MSOP-8	235°C/W
SOIC-8	190°C/W

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, and $R_L = 100\Omega$ (or as specified) tied to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
GB	Gain Bandwidth Product	$V_{OUT} < 200mV_{PP}$		140		MHz
SSBW	-3dB BW	$A_V = +1, V_{OUT} = 200mV_{PP}$	220	270		MHz
		$A_V = +2$ or $-1, V_{OUT} = 200mV_{PP}$		100		
GFP	Frequency Response Peaking	$A_V = +2, V_{OUT} = 200mV_{PP}$, DC to 100MHz		1.5		dB
GFR	Frequency Response Rolloff	$A_V = +2, V_{OUT} = 200mV_{PP}$, DC to 100MHz		0.5		dB
LPD _{1°}	1° Linear Phase Deviation	$A_V = +2, V_{OUT} = 200mV_{PP}, \pm 1^\circ$		30		MHz
GF _{0.1dB}	0.1dB Gain Flatness	$A_V = +2, \pm 0.1dB, V_{OUT} = 200mV_{PP}$		13		MHz
PBW	Full Power Bandwidth	-1dB, $V_{OUT} = 3V_{PP}, A_V = -1$		55		MHz
DG	Differential Gain	NTSC, $V_{CM} = 2V, R_L = 150\Omega$ to $V^+/2$, Pos. Video Only		0.03		%
DP	Differential Phase	NTSC, $V_{CM} = 2V, R_L = 150\Omega$ to $V^+/2$ Pos. Video Only		0.1		deg

Time Domain Response

t_r	Rise and Fall Time	$A_V = +2, V_{OUT} = 500mV_{PP}$		3.3		ns
		$A_V = -1, V_{OUT} = 500mV_{PP}$		3.4		
OS	Overshoot, Undershoot	$A_V = +2, V_{OUT} = 500mV_{PP}$		18		%
t_s	Settling Time	$V_O = 2V_{PP}, \pm 0.1\%, R_L = 500\Omega$ to $V^+/2, A_V = -1$		37		ns
SR	Slew Rate (Note 8)	$A_V = -1, V_O = 3V_{PP}$ (Note 13)		470		V/ μs
		$A_V = +2, V_O = 3V_{PP}$ (Note 13)		420		

Distortion and Noise Response

HD2	2 nd Harmonic Distortion	$f = 5MHz, V_O = 2V_{PP}, A_V = -1$		-70		dBc
HD3	3 rd Harmonic Distortion	$f = 5MHz, V_O = 2V_{PP}, A_V = -1$		-57		dBc
THD	Total Harmonic Distortion	$f = 5MHz, V_O = 2V_{PP}, A_V = -1$		-55.5		dBc
V_n	Input-Referred Voltage Noise	$f = 100KHz$		11		nV/ \sqrt{Hz}
		$f = 1KHz$		19		
I_n	Input-Referred Current Noise	$f = 100KHz$		2.1		pA/ \sqrt{Hz}
		$f = 1KHz$		7.5		
XTLKA	Cross-Talk Rejection (LMH6658)	$f = 5MHz, R_L (SND) = 100\Omega$ RCV: $R_F = R_G = 1k$		69		dB

Static, DC Performance

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$, and $R_L = 100\Omega$ (or as specified) tied to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
A_{VOL}	Large Signal Voltage Gain	$V_O = 1.25\text{V to } 3.75\text{V}$, $R_L = 2\text{k to } V^+/2$	85	95		dB
		$V_O = 1.5\text{V to } 3.5\text{V}$, $R_L = 150\Omega \text{ to } V^+/2$	75	85		
		$V_O = 2\text{V to } 3\text{V}$, $R_L = 50\Omega \text{ to } V^+/2$	70	80		
CMVR	Input Common-Mode Voltage Range	CMRR $\geq 50\text{dB}$	-0.2 -0.1	-0.5		V
			3.0 2.8	3.3		
V_{OS}	Input Offset Voltage			± 1.1	± 5 ± 7	mV
TC V_{OS}	Input Offset Voltage Average Drift	(Note 12)		± 2		$\mu\text{V}/\text{C}$
I_{B}	Input Bias Current	(Note 7)		-5	-20 -30	μA
TC I_{B}	Input Bias Current Average Drift	(Note 12)		0.01		nA/C
I_{OS}	Input Offset Current			50	300 500	nA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.0V	72	82		dB
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 4.5\text{V to } 5.5\text{V}$, $V_{\text{CM}} = 1\text{V}$	72	82		dB
I_{S}	Supply Current (per channel)	No load		6.2	8.5 10	mA
Miscellaneous Performance						
V_{OH}	Output Swing High	$R_L = 2\text{k to } V^+/2$	4.10 3.8	4.25		V
		$R_L = 150\Omega \text{ to } V^+/2$	4.00 3.70	4.19		
		$R_L = 75\Omega \text{ to } V^+/2$	3.85 3.50	4.15		
V_{OL}	Output Swing Low	$R_L = 2\text{k to } V^+/2$	900 1100	800		mV
		$R_L = 150\Omega \text{ to } V^+/2$	970 1200	870		
		$R_L = 75\Omega \text{ to } V^+/2$	990 1250	885		
I_{OUT}	Output Current	$V_{\text{OUT}} = 1\text{V}$ from either rail	± 40	+85, -105		mA
I_{SC}	Output Short Circuit Current (Note 10)	Sourcing to $V^+/2$	100 80	155		mA
		Sinking to $V^+/2$	100 80	220		
R_{IN}	Common Mode Input Resistance			3		$\text{M}\Omega$
C_{IN}	Common Mode Input Capacitance			1.8		pF
R_{OUT}	Output Impedance	$f = 1\text{MHz}$, $A_v = +1$		0.06		Ω

±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = -5\text{V}$, $V_{\text{CM}} = V_O$, and $R_L = 100\Omega$ (or as specified) tied to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
GB	Gain Bandwidth Product	$V_{\text{OUT}} < 200\text{mV}_{\text{PP}}$		140		MHz
SSBW	-3dB BW	$A_V = +1$, $V_{\text{OUT}} = 200\text{mV}_{\text{PP}}$	220	270		MHz
		$A_V = +2$ or -1 , $V_{\text{OUT}} = 200\text{mV}_{\text{PP}}$		100		
GFP	Frequency Response Peaking	$A_V = +2$, $V_{\text{OUT}} = 200\text{mV}_{\text{PP}}$, DC to 100MHz		1.0		dB
GFR	Frequency Response Rolloff	$A_V = +2$, $V_{\text{OUT}} = 200\text{mV}_{\text{PP}}$, DC to 100MHz		0.9		dB
LPD _{1°}	1° Linear Phase Deviation	$A_V = +2$, $V_{\text{OUT}} = 200\text{mV}_{\text{PP}}$, $\pm 1^\circ$		30		MHz
GF _{0.1dB}	0.1dB Gain Flatness	$A_V = +2$, $\pm 0.1\text{dB}$, $V_{\text{OUT}} = 200\text{mV}_{\text{PP}}$		20		MHz
PBW	Full Power Bandwidth	-1dB, $V_{\text{OUT}} = 8V_{\text{PP}}$, $A_V = -1$		30		MHz
DG	Differential Gain	NTSC, $R_L = 150\Omega$, Pos. or Neg. Video		0.03		%
DP	Differential Phase	NTSC, $R_L = 150\Omega$, Pos. or Neg. Video		0.1		deg
Time Domain Response						
t_r	Rise and Fall Time	$A_V = +2$, $V_{\text{OUT}} = 500\text{mV}_{\text{PP}}$		3.3		ns
		$A_V = -1$, $V_{\text{OUT}} = 500\text{mV}_{\text{PP}}$		3.3		
OS	Overshoot, Undershoot	$A_V = +2$, $V_{\text{OUT}} = 500\text{mV}_{\text{PP}}$		16		%
t_s	Settling Time	$V_O = 5V_{\text{PP}}$, $\pm 0.1\%$, $R_L = 500\Omega$, $A_V = -1$		35		ns
SR	Slew Rate (Note 8)	$A_V = -1$, $V_O = 8V_{\text{PP}}$		700		V/ μs
		$A_V = +2$, $V_O = 8V_{\text{PP}}$		500		
Distortion and Noise Response						
HD2	2 nd Harmonic Distortion	$f = 5\text{MHz}$, $V_O = 2V_{\text{PP}}$, $A_V = -1$		-70		dBc
HD3	3 rd Harmonic Distortion	$f = 5\text{MHz}$, $V_O = 2V_{\text{PP}}$, $A_V = -1$		-57		dBc
THD	Total Harmonic Distortion	$f = 5\text{MHz}$, $V_O = 2V_{\text{PP}}$, $A_V = -1$		-55.5		dBc
V_n	Input-Referred Voltage Noise	$f = 100\text{KHz}$		11		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{KHz}$		19		
I_n	Input-Referred Current Noise	$f = 100\text{KHz}$		2.1		pA/ $\sqrt{\text{Hz}}$
		$f = 1\text{KHz}$		7.5		
XTLKA	Cross-Talk Rejection (LMH6658)	$f = 5\text{MHz}$, R_L (SND) = 100 Ω RCV: $R_F = R_G = 1\text{k}$		69		dB
Static, DC Performance						
A_{VOL}	Large Signal Voltage Gain	$V_O = -3.75\text{V}$ to 3.75V , $R_L = 2\text{k}$	87	100		dB
		$V_O = -3.5\text{V}$ to 3.5V , $R_L = 150\Omega$	80	90		
		$V_O = -3\text{V}$ to 3V , $R_L = 50\Omega$	75	85		
CMVR	Input Common-Mode Voltage Range	CMRR $\geq 50\text{dB}$	-5.2	-5.5		V
			-5.1			
			3.0	3.3		
				2.8		
V_{OS}	Input Offset Voltage			± 1.0	± 5 ± 7	mV
TC V_{OS}	Input Offset Voltage Average Drift	(Note 12)		± 2		$\mu\text{V}/\text{C}$
I_B	Input Bias Current	(Note 7)		-5	-20 -30	μA
TC I_B	Input Bias Current Average Drift	(Note 12)		0.01		nA/ $^\circ\text{C}$

±5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = -5\text{V}$, $V_{CM} = V_O$, and $R_L = 100\Omega$ (or as specified) tied to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_{OS}	Input Offset Current			50	300 500	nA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from -5V to 3.0V	75	84		dB
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 4.5\text{V}$ to 5.5V , $V_{CM} = -4\text{V}$	75	82		dB
-PSRR	Negative Power Supply Rejection Ratio	$V^- = -4.5\text{V}$ to -5.5V	78	85		dB
I_S	Supply Current (per channel)	No load		6.5	9.0 11	mA
Miscellaneous Performance						
V_{OH}	Output Swing High	$R_L = 2\text{k}$	4.10 3.80	4.25		V
		$R_L = 150\Omega$	4.00 3.70	4.20		
		$R_L = 75\Omega$	3.85 3.50	4.18		
V_{OL}	Output Swing Low	$R_L = 2\text{k}$	-4.05 -3.80	-4.19		V
		$R_L = 150\Omega$	-3.90 -3.65	-4.05		
		$R_L = 75\Omega$	-3.80 -3.50	-4.00		
I_{OUT}	Output Current	$V_{OUT} = 1\text{V}$ from either rail	± 45	+100, -110		mA
I_{SC}	Output Short Circuit Current (Note 10)	Sourcing to Ground	120 100	180		mA
		Sinking to Ground	120 100	230		
R_{IN}	Common Mode Input Resistance			4		$M\Omega$
C_{IN}	Common Mode Input Capacitance			1.8		pF
R_{OUT}	Output Impedance	$f = 1\text{MHz}$, $A_V = +1$		0.06		Ω

Note 1: Note 1: Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5k Ω in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Positive current corresponds to current flowing into the device.

Note 8: Slew rate is the "worst case" of the rising and falling slew rates.

Note 9: Machine Model, 0 Ω in series with 200pF.

Note 10: Short circuit test is a momentary test. See Note 11.

Note 11: Output short circuit duration is infinite for $V_S < 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

Note 12: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

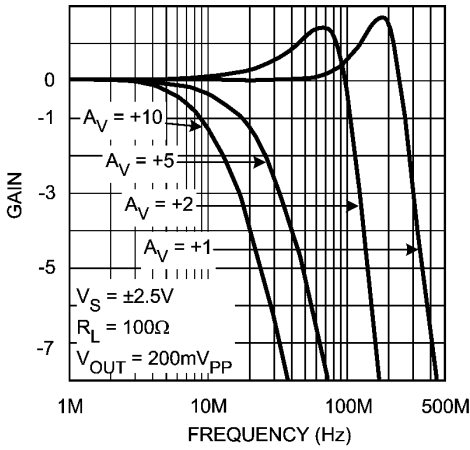
Note 13: Output Swing not limited by Slew Rate limit.

Ordering Information

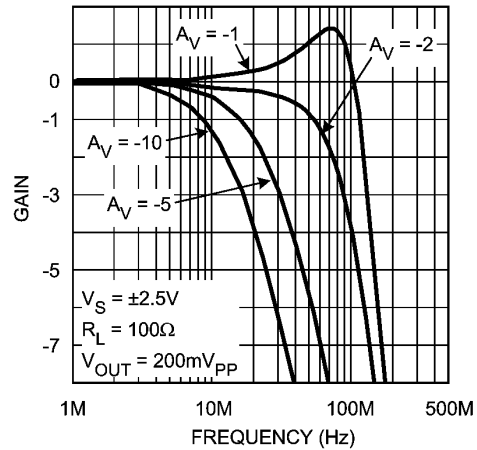
Package	Part Number	Package Marking	Transport Media	NSC Drawing
SOT23-5	LMH6657MF	A85A	1k Units Tape and Reel	MF05A
	LMH6657MFX		3k Units Tape and Reel	
SC70-5	LMH6657MG	A76	1k Units Tape and Reel	MAA05A
	LMH6657MGX		3k Units Tape and Reel	
SOIC-8	LMH6658MA	LMH6658MA	Rails	M08A
	LMH6658MAX		2.5k Units Tape and Reel	
MSOP-8	LMH6658MM	A88A	1k Units Tape and Reel	MUA08A
	LMH6658MMX		3.5k Units Tape and Reel	

Typical Performance Characteristics

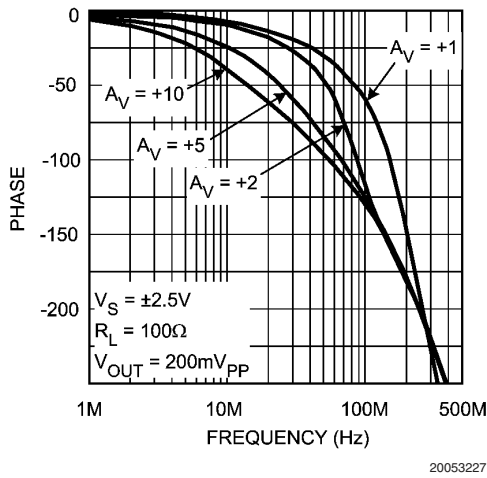
Non-Inverting Frequency Response, Gain



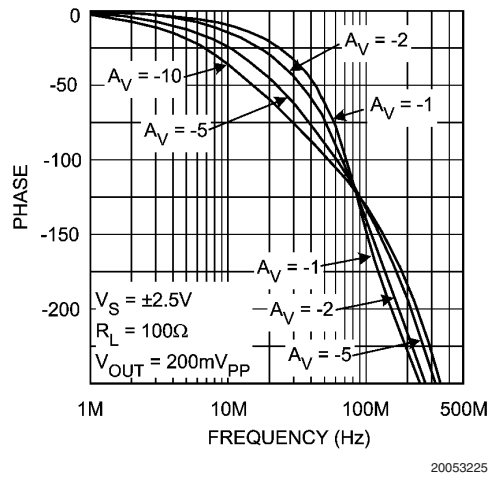
Inverting Frequency Response, Gain



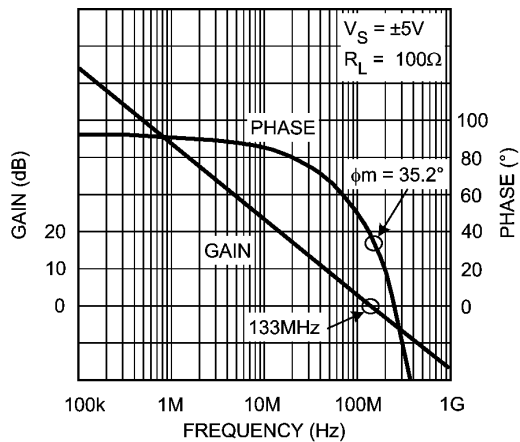
Non-Inverting Frequency Response, Phase



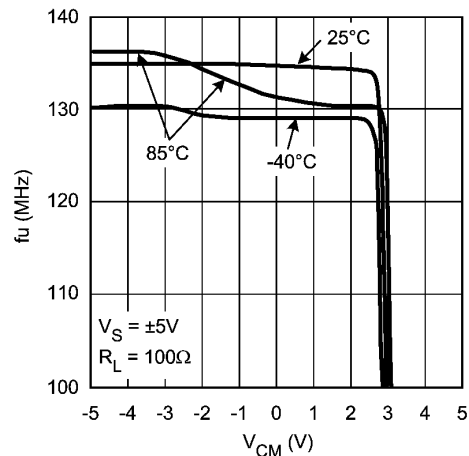
Inverting Frequency Response, Phase



Open Loop Gain/Phase vs. Frequency

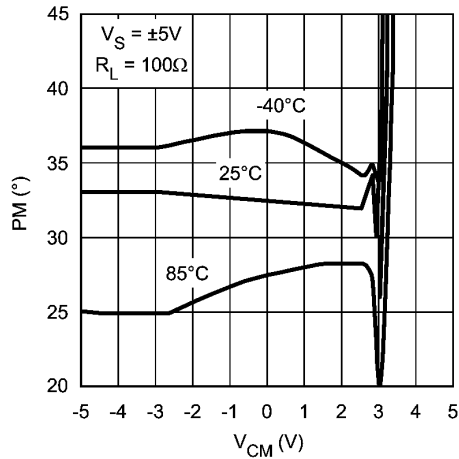


Unity Gain Frequency vs. V_{CM}



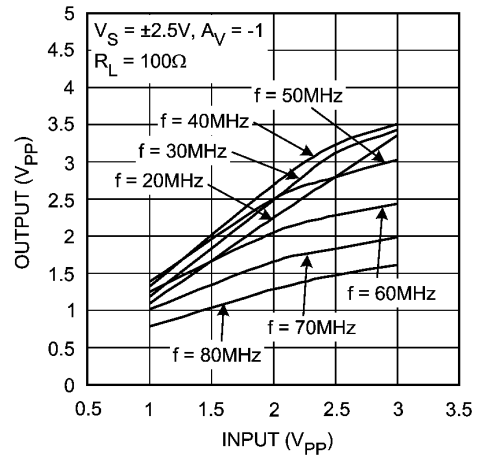
Typical Performance Characteristics (Continued)

Phase Margin vs. V_{CM}



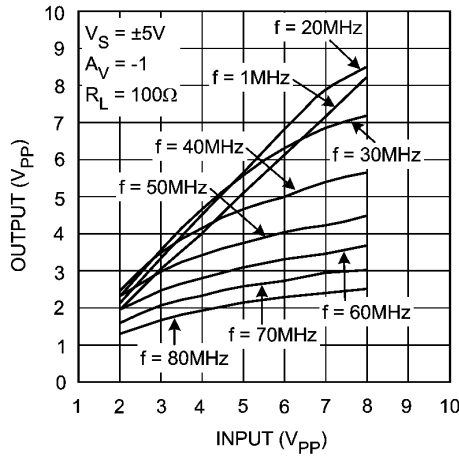
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Output vs. Input



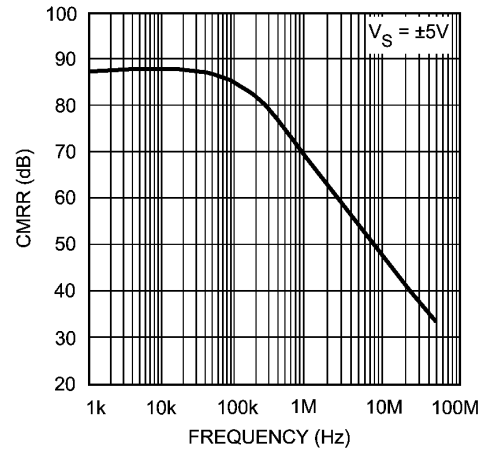
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Output vs. Input



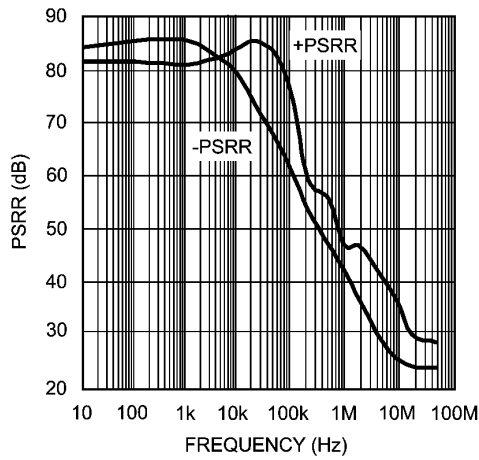
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CMRR vs. Frequency



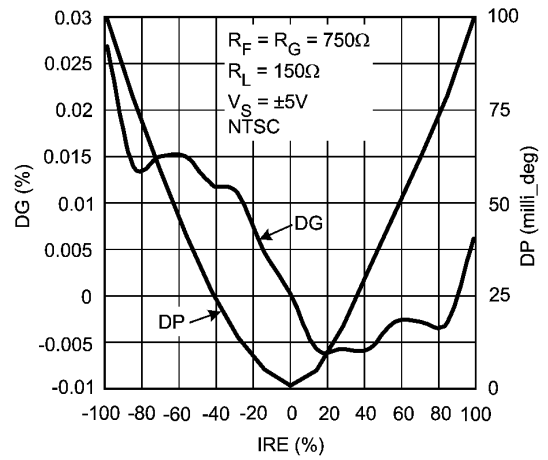
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PSRR vs. Frequency



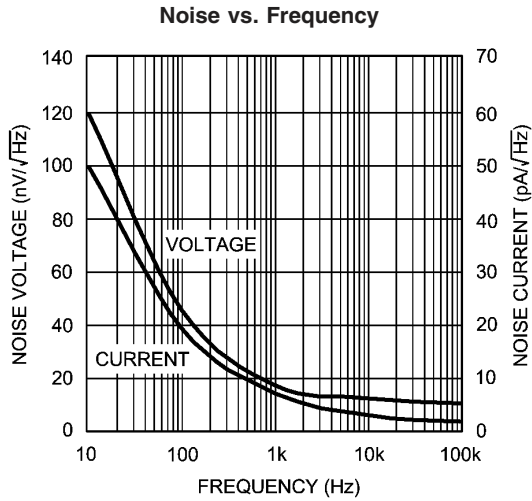
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DG/DP vs. IRE

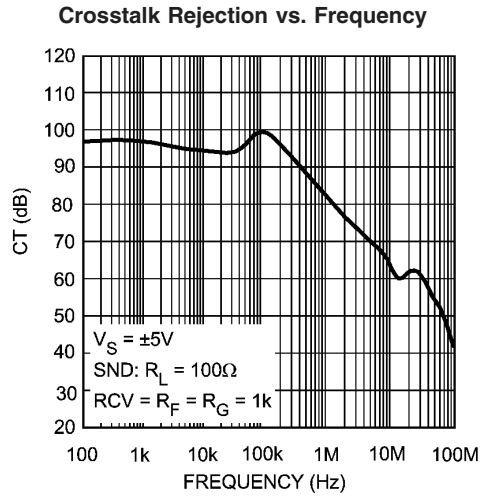


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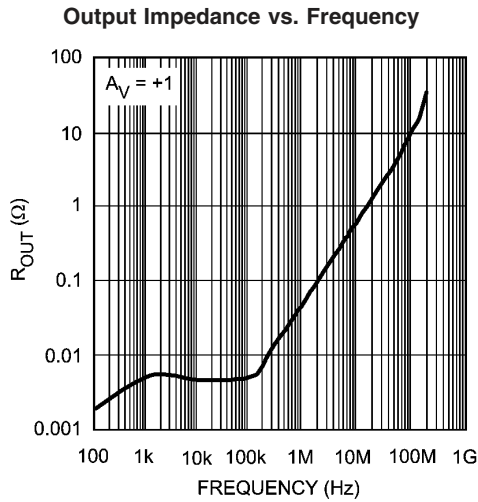
Typical Performance Characteristics (Continued)



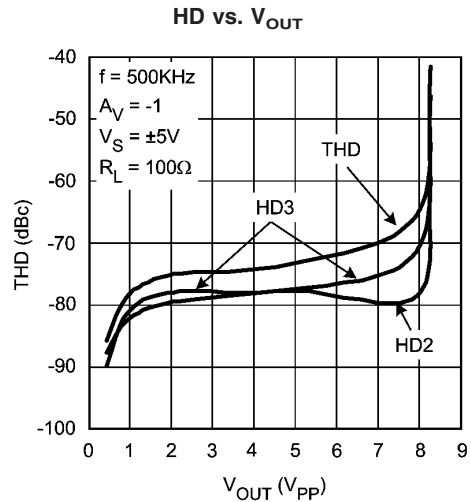
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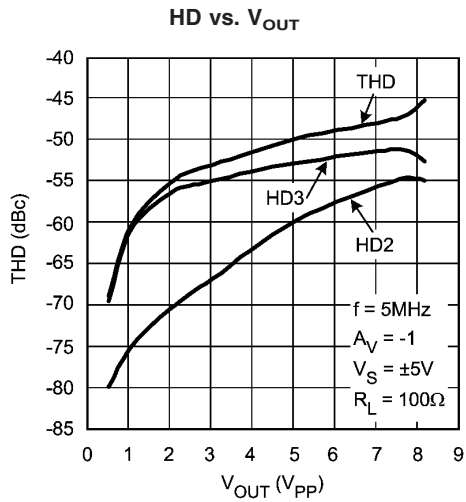
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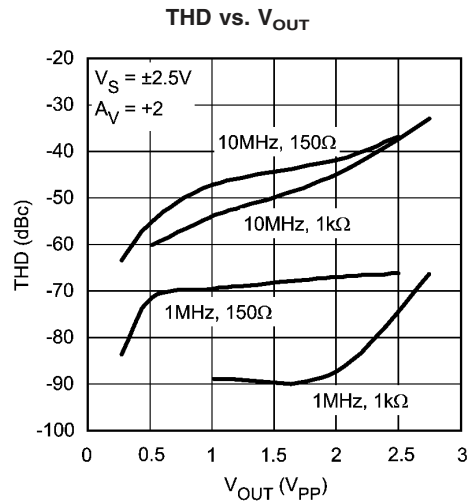
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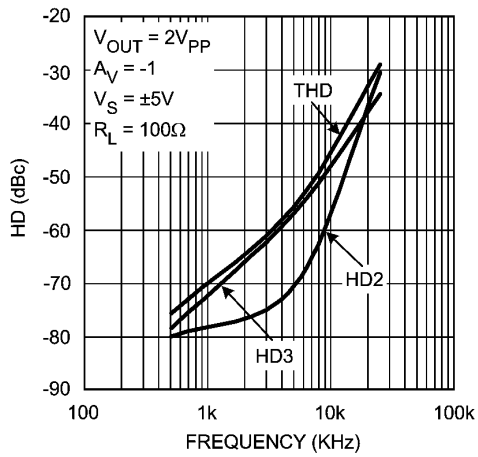
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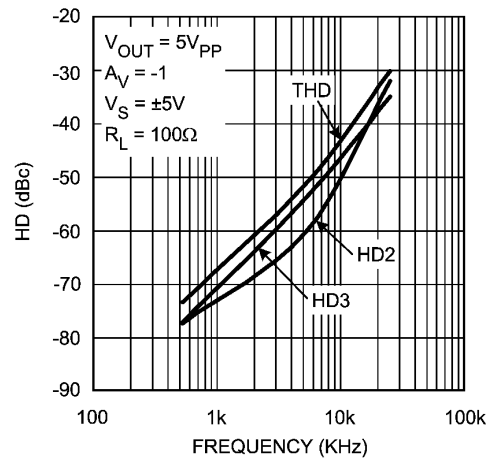
Typical Performance Characteristics (Continued)

HD vs. Frequency



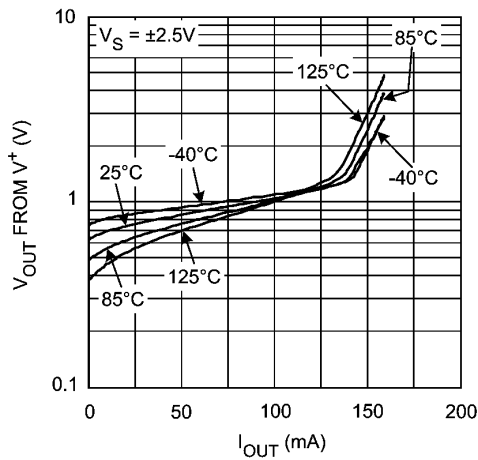
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HD vs. Frequency



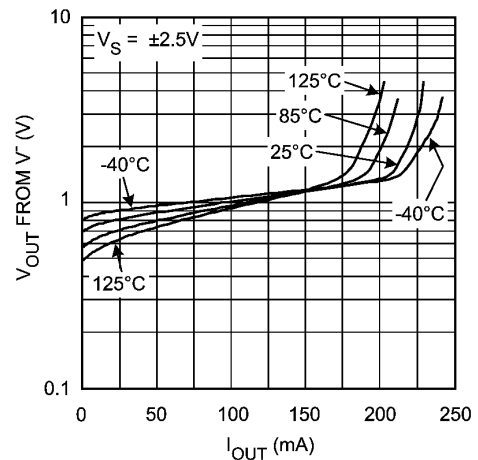
20053215

V_{OUT} vs. I_{SOURCE}



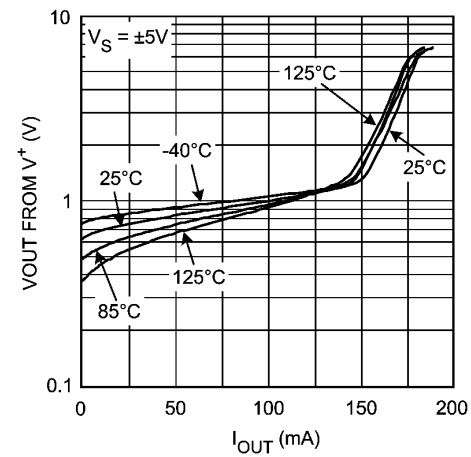
20053243

V_{OUT} vs. I_{SINK}



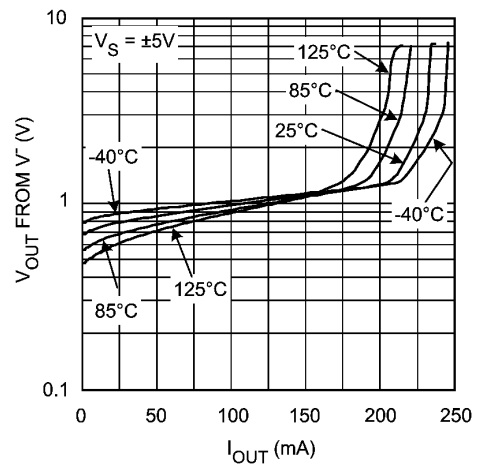
20053244

V_{OUT} vs. I_{SOURCE}



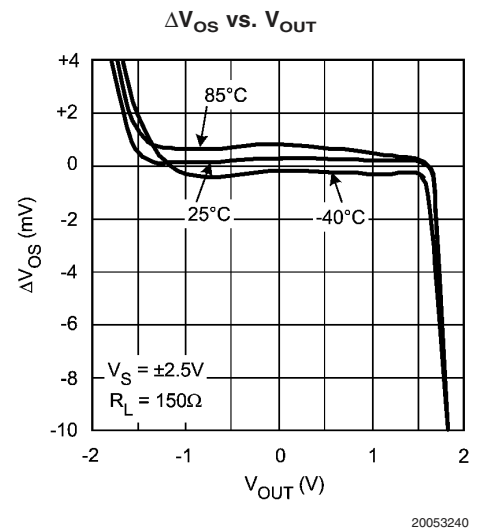
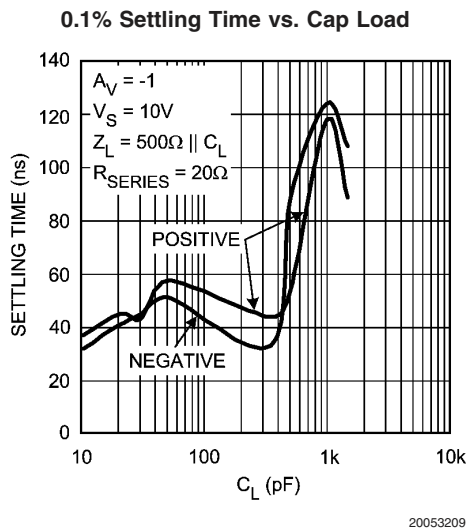
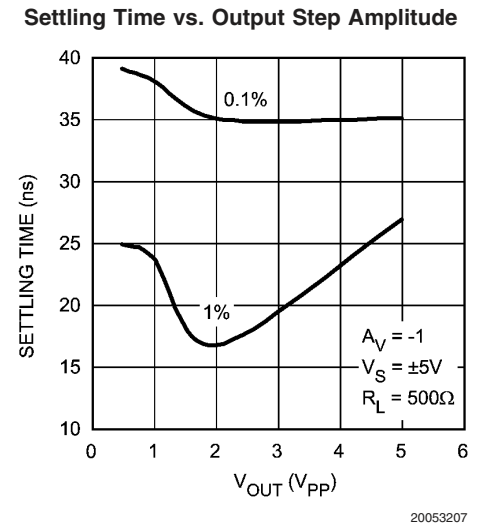
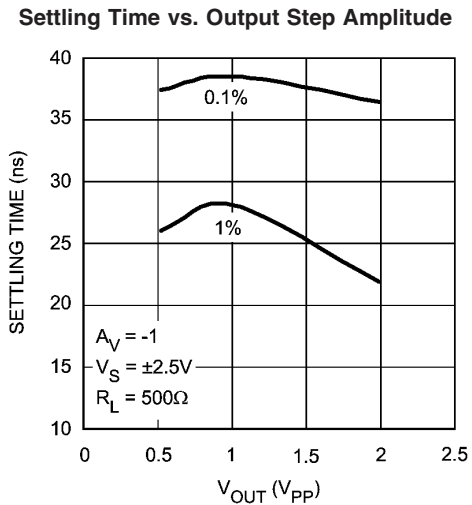
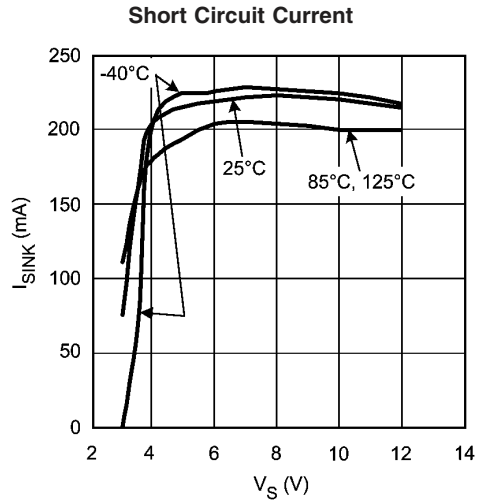
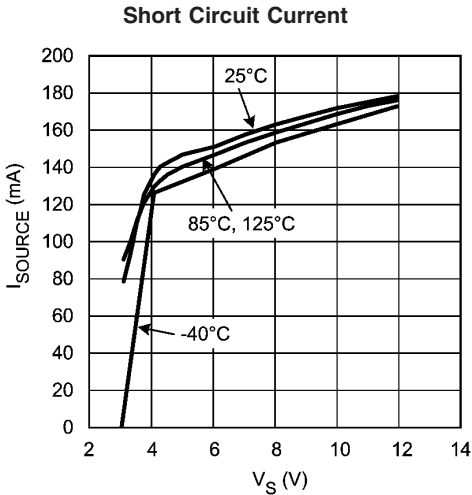
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V_{OUT} vs. I_{SINK}

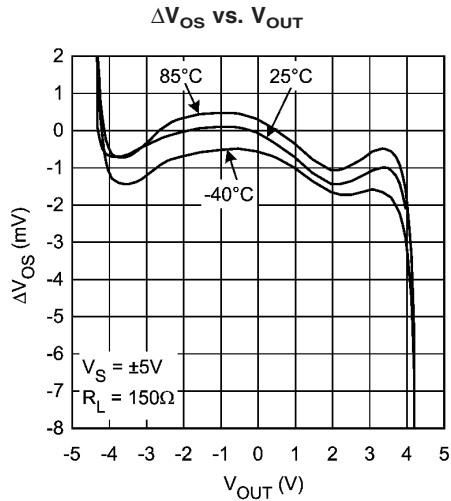


20053246

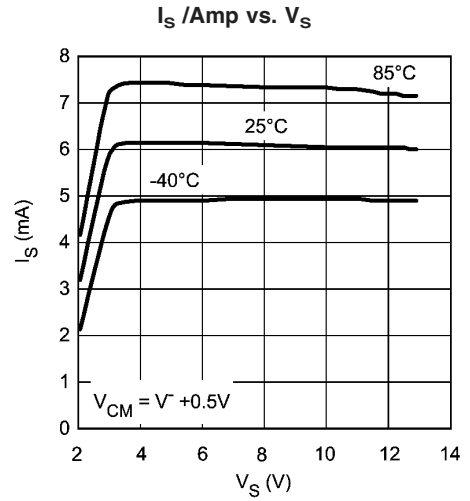
Typical Performance Characteristics (Continued)



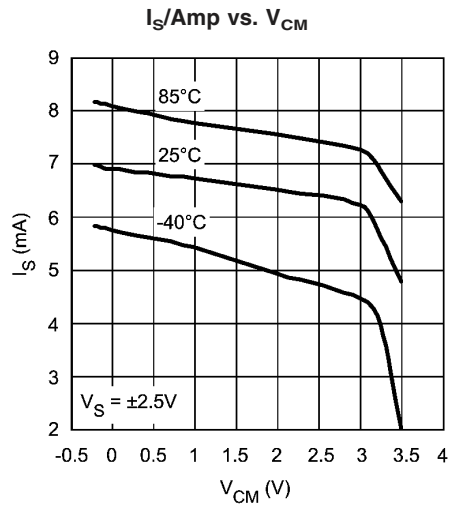
Typical Performance Characteristics (Continued)



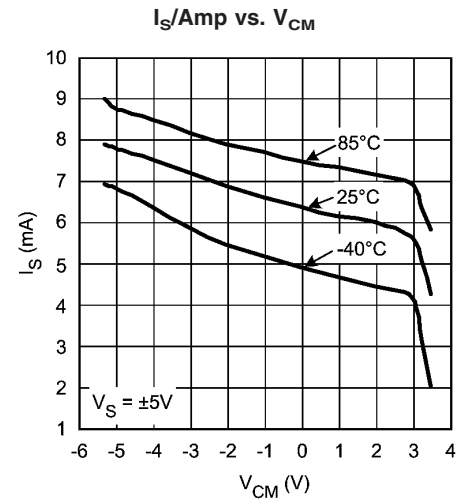
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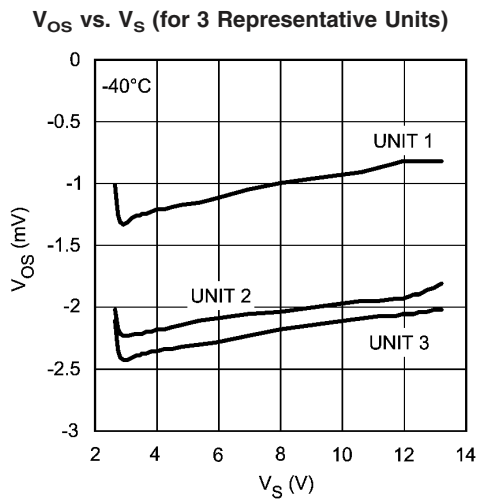
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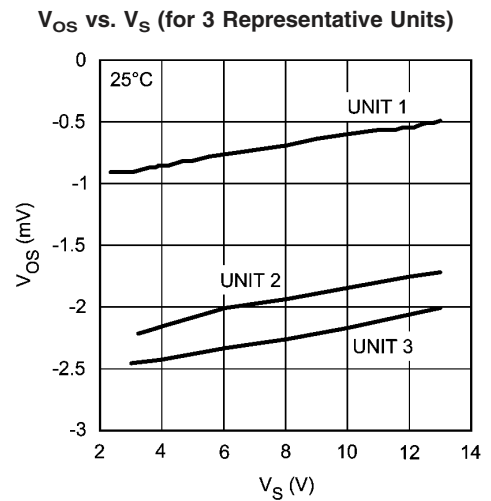
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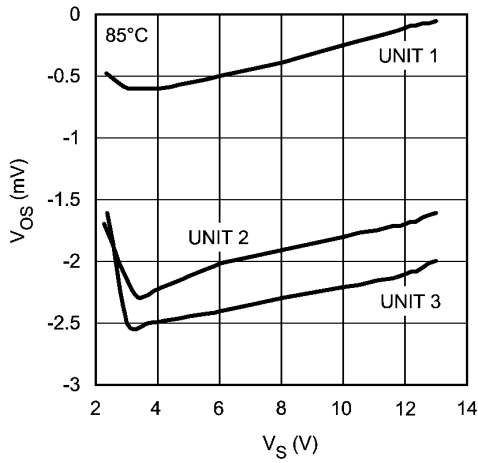
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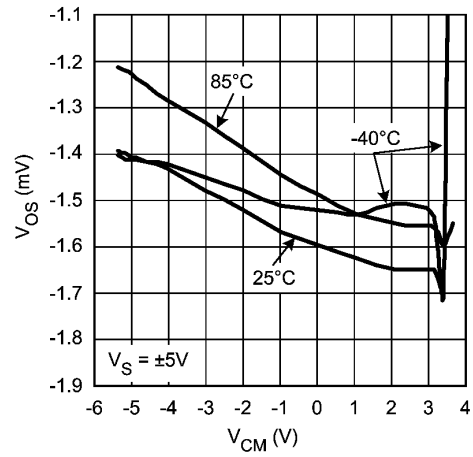
Typical Performance Characteristics (Continued)

V_{OS} vs. V_S (for 3 Representative Units)



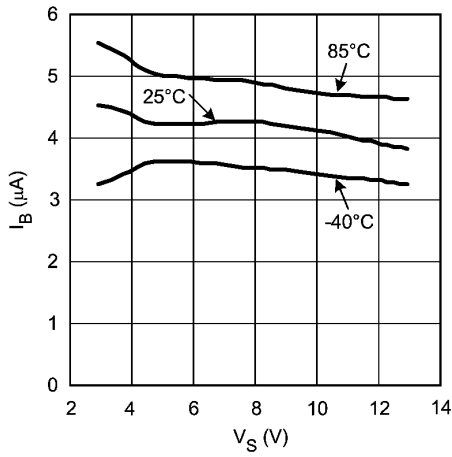
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V_{OS} vs. V_{CM} (A Typical Unit)



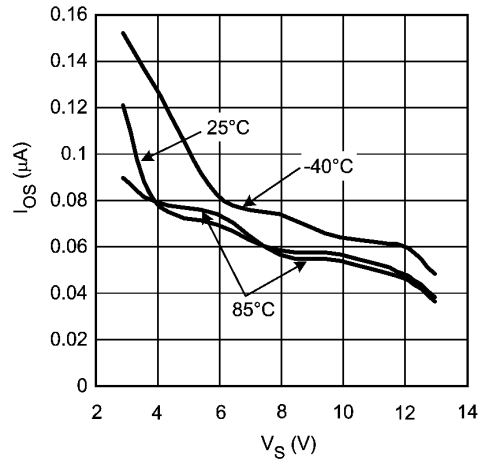
20053236

$|I_B|$ vs. V_S



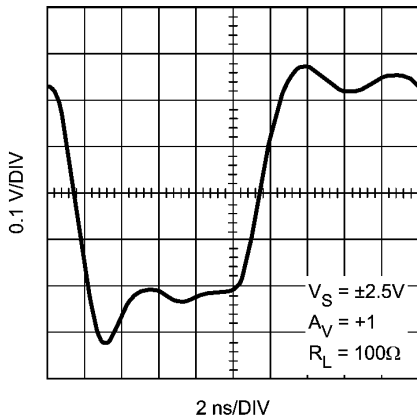
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I_{OS} vs. V_S



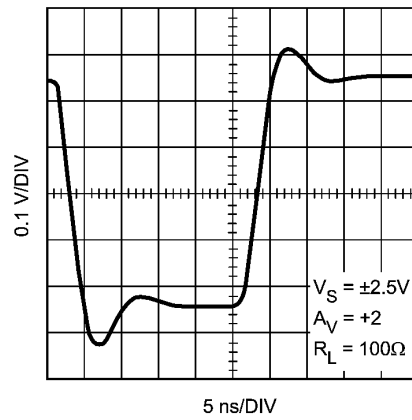
20053229

Small Signal Step Response



20053222

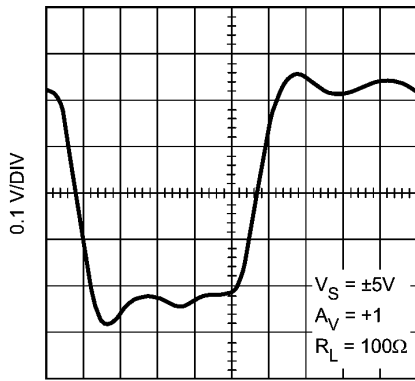
Small Signal Step Response



20053220

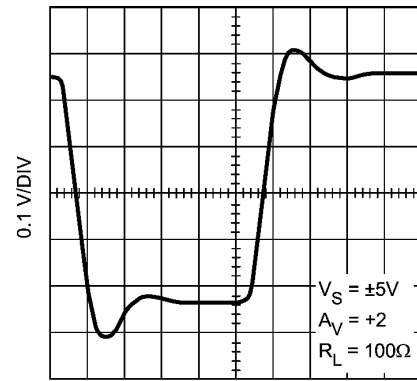
Typical Performance Characteristics (Continued)

Small Signal Step Response



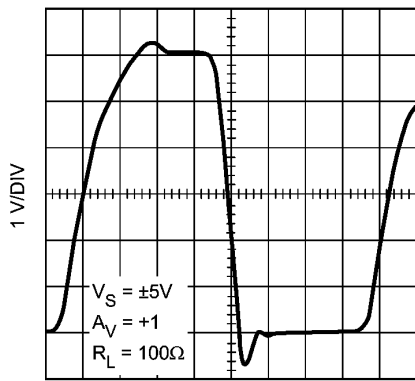
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Small Signal Step Response



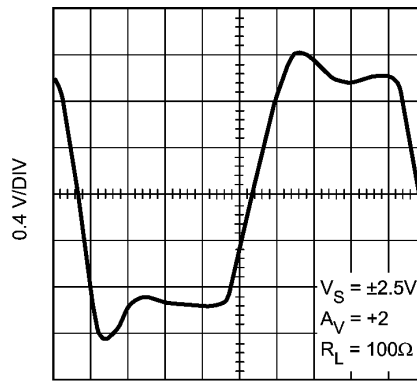
20053221

Large Signal Step Response



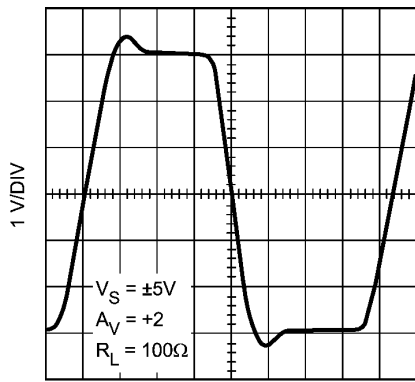
20053217

Large Signal Step Response



20053219

Large Signal Step Response



20053218

Application Section

LARGE SIGNAL BEHAVIOR

The LMH6657/6658 is specially designed to handle large output swings, such as those encountered in video waveforms, without being slew rate limited. With 5V supply, the LMH6657/6658 slew rate limit is larger than that might be necessary to make full allowable output swing excursions. Therefore, the large signal frequency response is dominated by the small signal characteristics, rather than the conventional limitation imposed by slew rate limit.

The LMH6657/6658 input stage is designed to provide excess overdrive when needed. This occurs when fast input signal excursions cannot be followed by the output stage. In these situations, the device encounters larger input signals than would be encountered under normal closed loop conditions. The LMH6657/6658 input stage is designed to take advantage of this "input overdrive" condition. The larger the amount of this overdrive, the greater is the speed with which the output voltage can change. Here is a plot of how the output slew rate limitation varies with respect to the amount of overdrive imposed on the input:

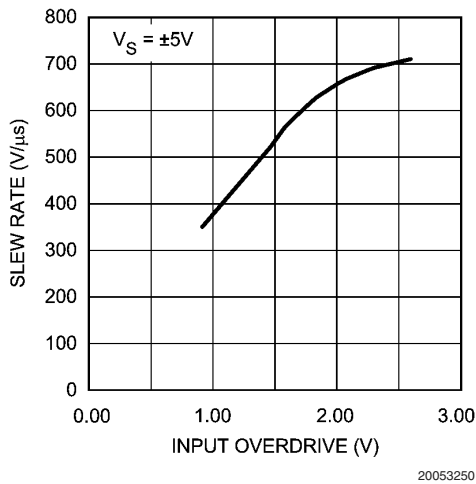


FIGURE 1. Plot Showing the Relationship Between Slew Rate and Input Overdrive

To relate the explanation above to a practical example, consider the following application example. Consider the case of a closed loop amplifier with a gain of -1 amplifying a sinusoidal waveform. From the plot of Output vs. Input (Typical Performance Characteristics section), with a 30MHz signal and $7V_{PP}$ input signal, it can be seen that the output will be limited to a swing of $6.9V_{PP}$. From the frequency Response plot it can be seen that the inverting gain of -1 has a -32° output phase shift at this frequency. It can be shown that this setup will result in about $1.9V_{PP}$ differential input voltage corresponding to $650V/\mu s$ of slew rate from Figure 1, above ($SR = V_O(pp) \cdot \pi \cdot f = 650V/\mu s$). Note that the amount of overdrive appearing on the input for a given sinusoidal test waveform is affected by the following:

- Output swing
- Gain setting
- Input/output phase relationship for the given test frequency
- Amplifier configuration (inverting or non-inverting)

Due to the higher frequency phase shift between input and output, there is no closed form solution to input overdrive for a given input. Therefore, Figure 1 is not very useful by itself in determining the output swing.

The following plots aid in predicting the output transition time based on the amount of swing required for a given gain setting.

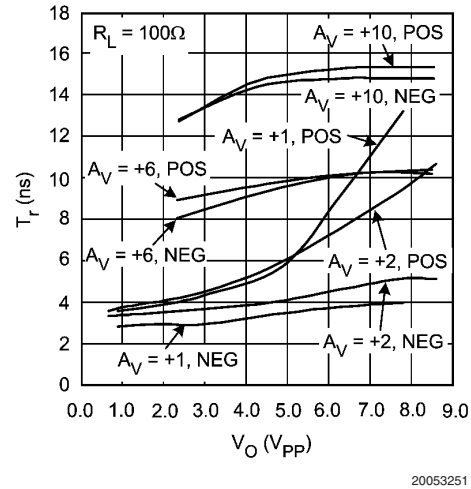


FIGURE 2. Output 20%-80% Transition vs. Output Voltage Swing (Non-Inverting Gain)

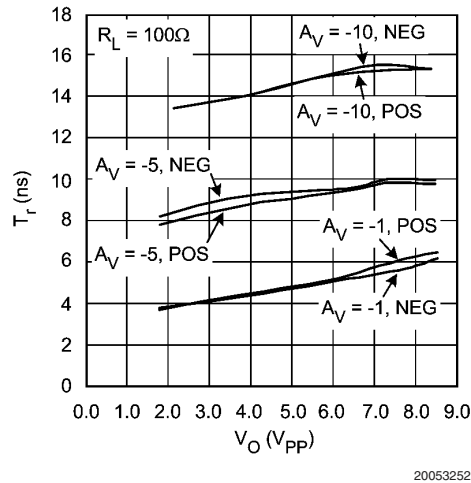


FIGURE 3. Output 20%-80% Transition vs. Output Voltage Swing (Inverting Gain)

Beyond a gain of 5 or so, the LMH6657/6658 output transition would be limited by bandwidth. For example, with a gain of 5, the $-3dB$ BW would be around 30MHz corresponding to a rise time of about 12ns (10% - 90%). Assuming a near linear transition, the 20%-80% transition time would be around 9ns which matches the measured results as shown in Figure 2.

When the output is heavily loaded, output swing may be limited by current capability of the device. Refer to "Output Current Capability" section, below, for more details.

Output Characteristics

OUTPUT CURRENT CAPABILITY

The LMH6657/6658 output swing for a given load can be determined by referring to the Output Voltage vs. Output Current plots (Typical Performance Characteristics section). Characteristic Tables show the output current when the output is 1V from either rail. The plots and table values can be used to predict closed loop continuous value of current for a given load. If left unchecked, the output current capability of the LMH6657/6658 could easily result in junction temperature exceeding the maximum allowed value specified under Absolute Maximum Ratings. Proper heat sinking or other precautions are required if conditions as such, exist.

Under transient conditions, such as when the input voltage makes a large transition and the output has not had time to reach its final value, the device can deliver output currents in excess of the typical plots mentioned above. Plots shown in *Figure 5* and below, depict how the output current capability improves under higher input overdrive voltages:

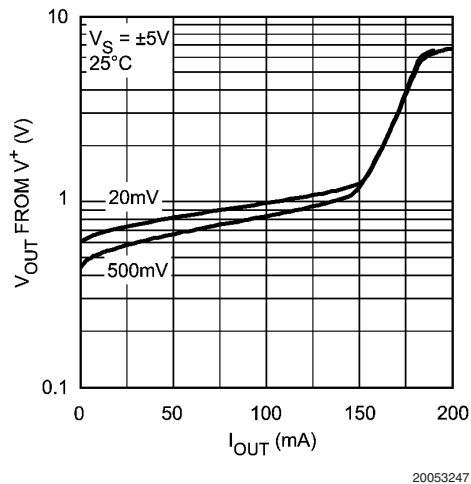


FIGURE 4. V_{OUT} vs. I_{SOURCE} (for Various Overdrive)

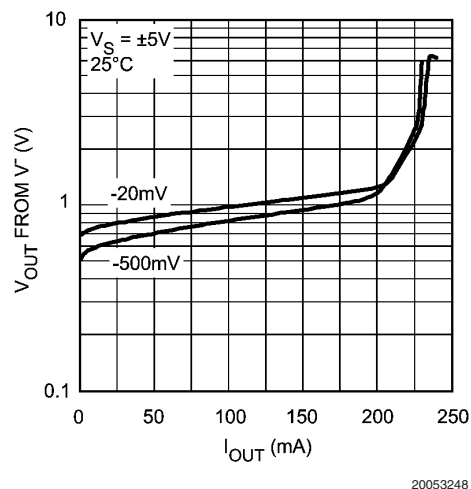


FIGURE 5. V_{OUT} vs. I_{SINK} (for Various Overdrive)

The LMH6657/6658 output stage is designed to swing within approximately one diode drop of each supply voltage by

utilizing specially designed high speed output clamps. This allows adequate output voltage swing even with 5V supplies and yet avoids some of the issues associated with rail-to-rail output operational amplifiers. Some of these issues are:

- Supply current increases when output reaches saturation at or near the supply rails
- Prolonged recovery when output approaches the rails

The LMH6657/6658 output is exceedingly well-behaved when it comes to recovering from an overload condition. As can be seen from *Figure 6* below, the LMH6657/6658 will typically recover from an output overload condition in about 18ns, regardless of the duration of the overload.

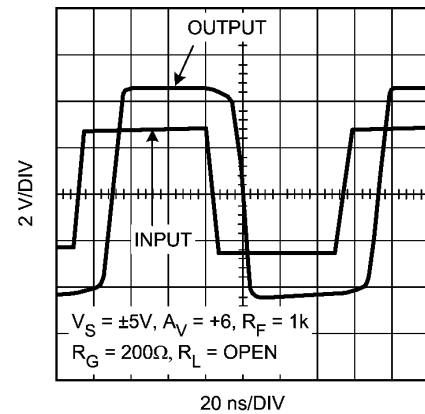


FIGURE 6. Output Overload Recovery

OUTPUT PHASE REVERSAL

This is a problem with some operational amplifiers. This effect is caused by phase reversal in the input stage due to saturation of one or more of the transistors when the inputs exceed the normal expected range of voltages. Some applications, such as servo control loops among others, are sensitive to this kind of behavior and would need special safeguards to ensure proper functioning. The LMH6657/6658 is immune to output phase reversal with input overload. With inputs exceeded, the LMH6657/6658 output will stay at the clamped voltage from the supply rail. Exceeding the input supply voltages beyond the Absolute Maximum Ratings of the device could however damage or otherwise adversely effect the reliability or life of the device.

DRIVING CAPACITIVE LOADS

The LMH6657/6658 can drive moderate values of capacitance by utilizing a series isolation resistor between the output and the capacitive load. Typical Performance Characteristics section shows the settling time behavior for various capacitive loads and 20Ω of isolation resistance. Capacitive load tolerance will improve with higher closed loop gain values. Applications such as ADC buffers, among others, present complex and varying capacitive loads to the Op Amp; best value for this isolation resistance is often found by experimentation and actual trial and error for each application.

DISTORTION

Applications with demanding distortion performance requirements are best served with the device operating in the inverting mode. The reason for this is that in the inverting configuration, the input common mode voltage does not vary

Output Characteristics (Continued)

with the signal and there is no subsequent ill effects due to this shift in operating point and the possibility of additional non-linearity. Moreover, under low closed loop gain settings (most suited to low distortion), the non-inverting configuration is at a further disadvantage of having to contend with the input common voltage range. There is also a strong relationship between output loading and distortion performance (i.e. $1k\Omega$ vs. 100Ω distortion improves by about 20dB @100KHz) especially at the lower frequency end where the distortion tends to be lower. At higher frequency, this dependence diminishes greatly such that this difference is only about 4dB at 10MHz. But, in general, lighter output load leads to reduced HD3 term and thus improves THD.

PRINTED CIRCUIT BOARD LAYOUT AND COMPONENT VALUES SECTIONS

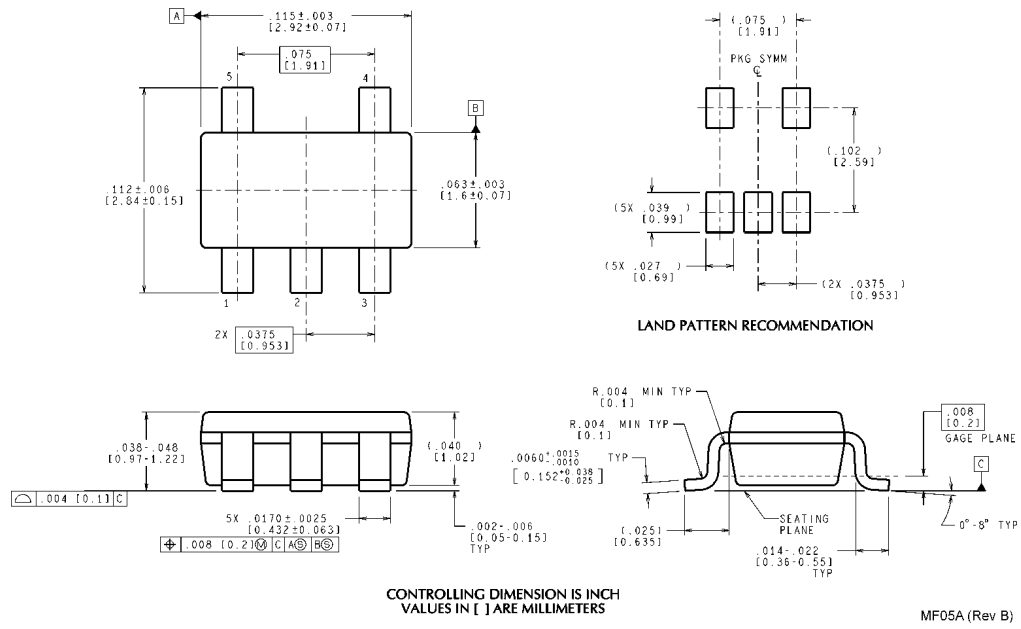
Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). National Semiconductor suggests the following

evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

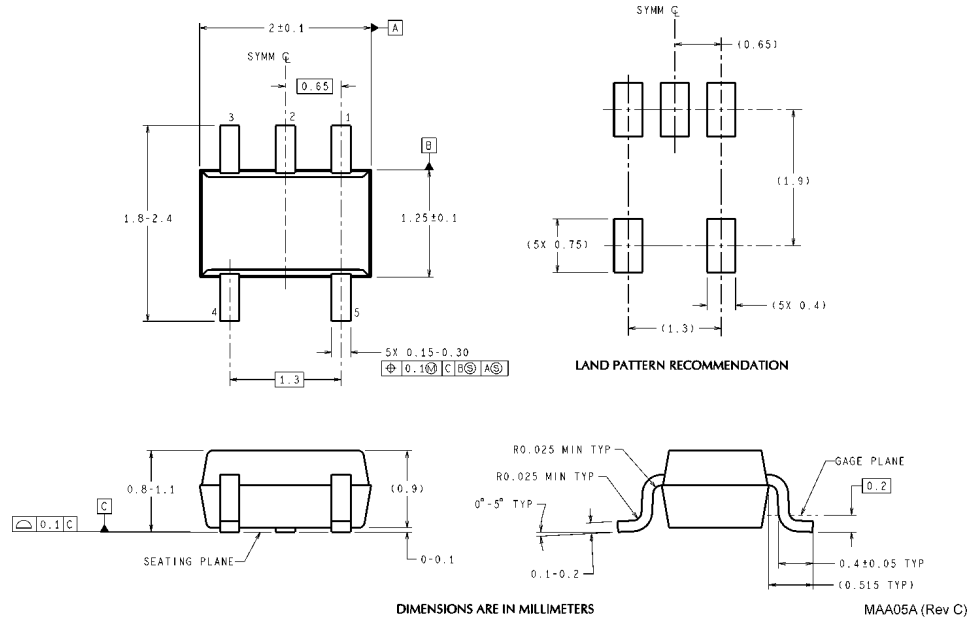
Device	Package	Evaluation Board PN
LMH6657MF	SOT23-5	CLC730068
LMH6657MG	SC-70	NA
LMH6658MA	8-Pin SOIC	CLC730036
LMH6658MM	8-Pin MSOP	CLC730123

These free evaluation boards are shipped when a device sample request is placed with National Semiconductor. Another important parameter in working with high speed/high performance amplifiers, is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors will load down nodes and will contribute to higher overall power dissipation.

Physical Dimensions inches (millimeters) unless otherwise noted

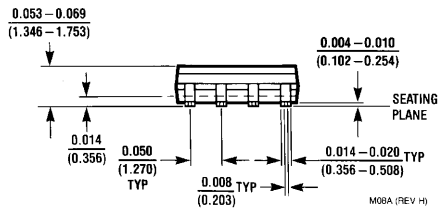
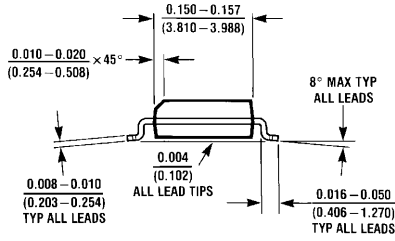
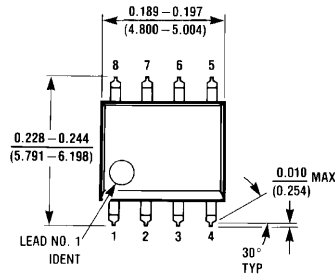


**5-Pin SOT23
NS Package Number MF05A**

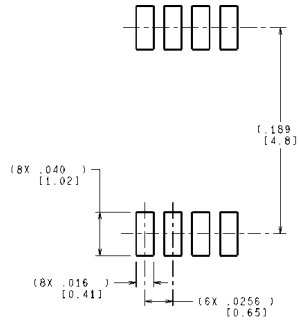
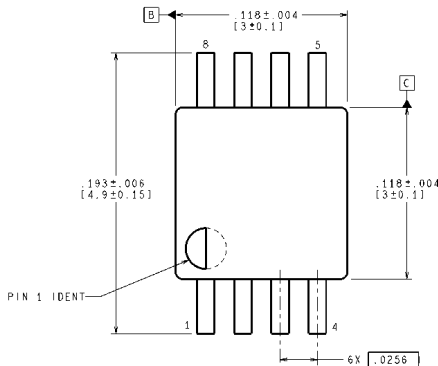


**SC70-5
NS Package Number MAA05A**

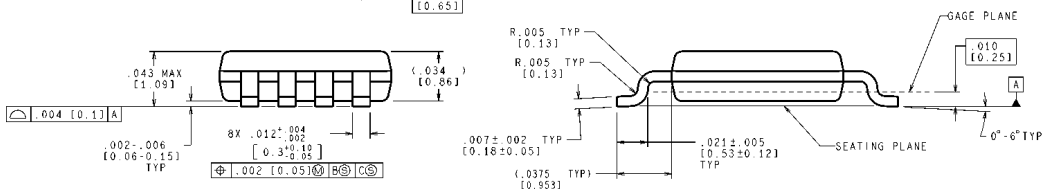
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Pin SOIC
NS Package Number M08A



LAND PATTERN RECOMMENDATION



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MUA08A (Rev E)

8-Pin MSOP
NS Package Number MUA08A

Notes

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