

## ADC342x Quad-Channel, 12-Bit, 25-MSPS to 125-MSPS, Analog-to-Digital Converter

### 1 Features

- Quad Channel
- 12-Bit Resolution
- Single Supply: 1.8 V
- Serial LVDS Interface
- Flexible Input Clock Buffer with Divide-by-1, -2, -4
- SNR = 70.2 dBFS, SFDR = 87 dBc at  $f_{IN} = 70$  MHz
- Ultra-Low Power Consumption:
  - 98 mW/Ch at 125 MSPS
- Channel Isolation: 105 dB
- Internal Dither and Chopper
- Support for Multi-Chip Synchronization
- Pin-to-Pin Compatible with 14-Bit Version
- Package: VQFN-56 (8 mm × 8 mm)

### 2 Applications

- Multi-Carrier, Multi-Mode Cellular Base Stations
- Radar and Smart Antenna Arrays
- Munitions Guidance
- Motor Control Feedback
- Network and Vector Analyzers
- Communications Test Equipment
- Nondestructive Testing
- Microwave Receivers
- Software-Defined Radios (SDRs)
- Quadrature and Diversity Radio Receivers

### 3 Description

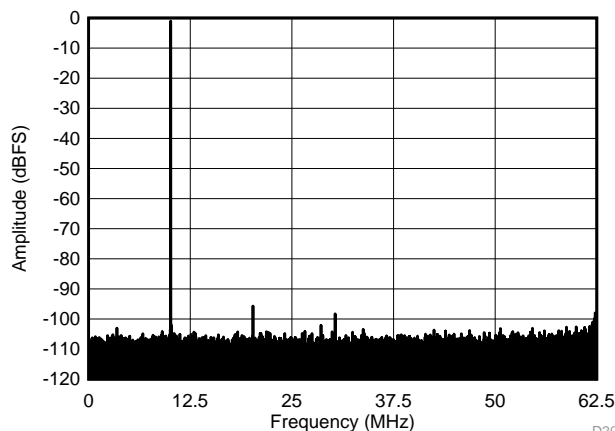
The ADC342x are a high-linearity, ultra-low power, quad-channel, 12-bit, 25-MSPS to 125-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design and the SYSREF input enables complete system synchronization. The ADC342x family supports serial low-voltage differential signaling (LVDS) in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 12-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC342x	VQFN (56)	8.00 mm × 8.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Spectrum at 10-MHz IF**  
(SFDR = 97 dBc, SNR = 70.4 dBFS, SINAD = 70.4 dBFS, THD = 98 dBc, HD2 = 95 dBc, HD3 = 97 dBc)



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## 4 Revision History

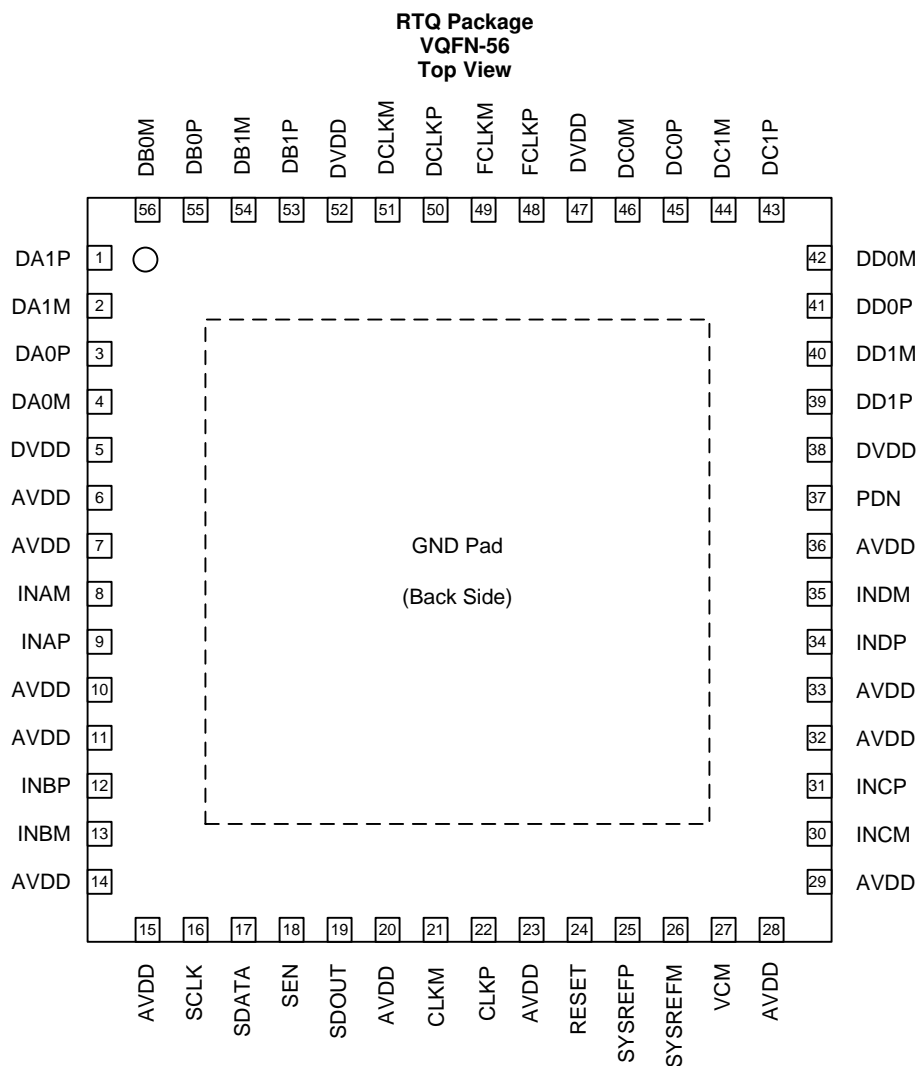
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Original (July 2014) to Revision A</b>	<b>Page</b>
• Released to production.....	<b>1</b>

## 5 Device Comparison Table

INTERFACE	RESOLUTION (Bits)	25 MSPS	50 MSPS	80 MSPS	125 MSPS	160 MSPS
Serial LVDS	12	<a href="#">ADC3421</a>	<a href="#">ADC3422</a>	<a href="#">ADC3423</a>	<a href="#">ADC3424</a>	—
	14	<a href="#">ADC3441</a>	<a href="#">ADC3442</a>	<a href="#">ADC3443</a>	<a href="#">ADC3444</a>	—
JESD204B	12	—	<a href="#">ADC34J22</a>	<a href="#">ADC34J23</a>	<a href="#">ADC34J24</a>	<a href="#">ADC34J25</a>
	14	—	<a href="#">ADC34J42</a>	<a href="#">ADC34J43</a>	<a href="#">ADC34J44</a>	<a href="#">ADC34J45</a>

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	6, 7, 10, 11, 14, 15, 20, 23, 28, 29, 32, 33, 36	I	Analog 1.8-V power supply
CLKM	21	I	Negative differential clock input for the ADC
CLKP	22	I	Positive differential clock input for the ADC
DA0M	4	O	Negative serial LVDS output for wire-0 of channel A
DA0P	3	O	Positive serial LVDS output for wire-0 of channel A
DA1M	2	O	Negative serial LVDS output for wire-1 of channel A
DA1P	1	O	Positive serial LVDS output for wire-1 of channel A
DB0M	56	O	Negative serial LVDS output for wire-0 of channel B
DB0P	55	O	Positive serial LVDS output for wire-0 of channel B
DB1M	54	O	Negative serial LVDS output for wire-1 of channel B
DB1P	53	O	Positive serial LVDS output for wire-1 of channel B
DC0M	46	O	Negative serial LVDS output for wire-0 of channel C
DC0P	45	O	Positive serial LVDS output for wire-0 of channel C
DC1M	44	O	Negative serial LVDS output for wire-1 of channel C
DC1P	43	O	Positive serial LVDS output for wire-1 of channel C
DD0M	42	O	Negative serial LVDS output for wire-0 of channel D
DD0P	41	O	Positive serial LVDS output for wire-0 of channel D
DD1M	40	O	Negative serial LVDS output for wire-1 of channel D
DD1P	39	O	Positive serial LVDS output for wire-1 of channel D
DCLKM	51	O	Negative bit clock output
DCLKP	50	O	Positive bit clock output
DVDD	5, 38, 47, 52	I	Digital 1.8-V power supply
FCLKM	49	O	Negative frame clock output
FCLKP	48	O	Positive frame clock output
GND	PowerPAD™	I	Ground, 0 V
INAM	8	I	Negative differential analog input for channel A
INAP	9	I	Positive differential analog input for channel A
INBM	13	I	Negative differential analog input for channel B
INBP	12	I	Positive differential analog input for channel B
INCM	30	I	Negative differential analog input for channel C
INCP	31	I	Positive differential analog input for channel C
INDM	35	I	Negative differential analog input for channel D
INDP	34	I	Positive differential analog input for channel D
PDN	37	I	Power-down control. This pin can be configured via the SPI. This pin has an internal 150-kΩ pulldown resistor.
RESET	24	I	Hardware reset; active high. This pin has an internal 150-kΩ pulldown resistor.
SCLK	16	I	Serial interface clock input. This pin has an internal 150-kΩ pulldown resistor.
SDATA	17	I	Serial interface data input. This pin has an internal 150-kΩ pulldown resistor.
SDOUT	19	O	Serial interface data output
SEN	18	I	Serial interface enable; active low. This pin has an internal 150-kΩ pullup resistor to AVDD.
SYSREFM	26	I	Negative external SYSREF input
SYSREFP	25	I	Positive external SYSREF input
VCM	27	O	Common-mode voltage for analog inputs

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Analog supply voltage range, AVDD		-0.3	2.1	V
Digital supply voltage range, DVDD		-0.3	2.1	V
Voltage applied to input pins	INAP, INBP, INCP, INDP, INAM, INBM, INCM, INDM	-0.3	min (1.9, AVDD + 0.3)	V
	CLKP, CLKM	-0.3	AVDD + 0.3	
	SYSREFP, SYSREFM	-0.3	AVDD + 0.3	
	SCLK, SEN, SDATA, RESET, PDN	-0.3	3.9	
Temperature	Operating free-air, T <sub>A</sub>	-40	85	°C
	Operating junction, T <sub>J</sub>		125	
	Storage, T <sub>stg</sub>	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
<b>SUPPLIES</b>					
AVDD	Analog supply voltage range	1.7	1.8	1.9	V
DVDD	Digital supply voltage range	1.7	1.8	1.9	V
<b>ANALOG INPUT</b>					
V <sub>ID</sub>	Differential input voltage	For input frequencies < 450 MHz		2	V <sub>PP</sub>
		For input frequencies < 600 MHz		1	
V <sub>IC</sub>	Input common-mode voltage	VCM ± 0.025			V
<b>CLOCK INPUT</b>					
	Input clock frequency	Sampling clock frequency	15 <sup>(2)</sup>	125 <sup>(3)</sup>	MSPS
	Input clock amplitude (differential)	Sine wave, ac-coupled	0.2	1.5	V <sub>PP</sub>
		LPECL, ac-coupled		1.6	
		LVDS, ac-coupled		0.7	
	Input clock duty cycle		35%	50%	65%
	Input clock common-mode voltage			0.95	V
<b>DIGITAL OUTPUTS</b>					
C <sub>LOAD</sub>	Maximum external load capacitance from each output pin to GND			3.3	pF
R <sub>LOAD</sub>	Single-ended load resistance			100	Ω

- (1) After power-up, use only the RESET pin to reset the device for the first time; see the [Register Initialization](#) section for details.  
(2) See [Table 3](#) for details.  
(3) With the clock divider enabled by default for divide-by-1. Maximum sampling clock frequency for the divide-by-4 option is 500 MSPS.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ADC342x	UNIT
		RTQ (VQFN)	
		56 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	25.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	9.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	3.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	3.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics: General

Typical values are over the operating free-air temperature range, at T<sub>A</sub> = 25°C, full temperature range is T<sub>MIN</sub> = –40°C to T<sub>MAX</sub> = 85°C, maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>					
	Differential input full-scale		2.0		V <sub>PP</sub>
r <sub>i</sub>	Input resistance	Differential at dc	6.6		kΩ
c <sub>i</sub>	Input capacitance	Differential at dc	3.7		pF
V <sub>OC(VCM)</sub>	VCM common-mode voltage output		0.95		V
	VCM output current capability		10		mA
	Input common-mode current	Per analog input pin	1.5		μA/MSPS
	Analog input bandwidth (3 dB)	50-Ω differential source driving 50-Ω termination across INP and INM	540		MHz
<b>DC ACCURACY</b>					
E <sub>O</sub>	Offset error		–25	25	mV
α <sub>EO</sub>	Temperature coefficient of offset error		± 0.024		mV/°C
E <sub>G(REF)</sub>	Gain error as a result of internal reference inaccuracy alone		–2	2	%FS
E <sub>G(CHAN)</sub>	Gain error of channel alone		–2		%FS
α <sub>(EGCHAN)</sub>	Temperature coefficient of E <sub>G(CHAN)</sub>		±0.008		Δ%FS/Ch
<b>CHANNEL-TO-CHANNEL ISOLATION</b>					
Crosstalk <sup>(1)</sup>	f <sub>IN</sub> = 10 MHz	Near channel		105	dB
		Far channel		105	
	f <sub>IN</sub> = 100 MHz	Near channel		95	
		Far channel		105	
	f <sub>IN</sub> = 200 MHz	Near channel		94	
		Far channel		105	
	f <sub>IN</sub> = 230 MHz	Near channel		92	
		Far channel		105	
	f <sub>IN</sub> = 300 MHz	Near channel		85	
		Far channel		105	

(1) Crosstalk is measured with a –1-dBFS input signal on the aggressor channel and no input on the victim channel.

## 7.6 Electrical Characteristics: ADC3421, ADC3422

Typical values are over the operating free-air temperature range, at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , maximum sampling rate, 50% clock duty cycle,  $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$ , and  $-1\text{-dBFS}$  differential input, unless otherwise noted.

PARAMETER	ADC3421			ADC3422			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
ADC clock frequency			25			50	MSPS
Resolution	12			12			Bits
1.8-V analog supply current		54	71		71	90	mA
1.8-V digital supply current		45	71		56	90	mA
Total power dissipation		177	240		228	305	mW
Global power-down dissipation		5	17		5	17	mW
Standby power-down dissipation		34	75		35	75	mW

## 7.7 Electrical Characteristics: ADC3423, ADC3424

Typical values are over the operating free-air temperature range, at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , maximum sampling rate, 50% clock duty cycle,  $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$ , and  $-1\text{-dBFS}$  differential input, unless otherwise noted.

PARAMETER	ADC3423			ADC3424			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
ADC clock frequency			80			125	MSPS
Resolution	12			12			Bits
1.8-V analog supply current		92	107		119	145	mA
1.8-V digital supply current		68	100		98	145	mA
Total power dissipation		288	365		391	475	mW
Global power-down dissipation		5	17		5	17	mW
Standby power-down dissipation		40	88		43	103	mW

## 7.8 AC Performance: ADC3421

Typical values are over the operating free-air temperature range, at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3421 ( $f_s = 25$ MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio (from 1-MHz offset)	$f_{\text{IN}} = 10$ MHz	70.9			71.1			dBFS
		$f_{\text{IN}} = 20$ MHz	68.9	70.7		70.9			
		$f_{\text{IN}} = 70$ MHz	70.4			70.6			
		$f_{\text{IN}} = 100$ MHz	70.3			70.5			
		$f_{\text{IN}} = 170$ MHz	69.7			69.9			
		$f_{\text{IN}} = 230$ MHz	68.9			69.1			
	Signal-to-noise ratio (full Nyquist band)	$f_{\text{IN}} = 10$ MHz	70.2			70.5			dBFS
		$f_{\text{IN}} = 20$ MHz	70.1			70.3			
		$f_{\text{IN}} = 70$ MHz	69.8			70.0			
		$f_{\text{IN}} = 100$ MHz	69.6			69.8			
		$f_{\text{IN}} = 170$ MHz	69.2			69.3			
		$f_{\text{IN}} = 230$ MHz	68.3			68.5			
NSD <sup>(1)</sup>	Noise spectral density (averaged across Nyquist zone)	$f_{\text{IN}} = 10$ MHz	–141.5			–141.7			dBFS/Hz
		$f_{\text{IN}} = 20$ MHz	–141.3	–139.5		–141.5			
		$f_{\text{IN}} = 70$ MHz	–141.0			–141.2			
		$f_{\text{IN}} = 100$ MHz	–140.9			–141.1			
		$f_{\text{IN}} = 170$ MHz	–140.3			–140.5			
		$f_{\text{IN}} = 230$ MHz	–139.5			–139.7			
SINAD <sup>(1)</sup>	Signal-to-noise and distortion ratio	$f_{\text{IN}} = 10$ MHz	71			71.1			dBFS
		$f_{\text{IN}} = 20$ MHz	67.9	70.8		70.9			
		$f_{\text{IN}} = 70$ MHz	69.5			70			
		$f_{\text{IN}} = 100$ MHz	70.5			70.7			
		$f_{\text{IN}} = 170$ MHz	69.6			69.8			
		$f_{\text{IN}} = 230$ MHz	68.7			68.7			
ENOB <sup>(1)</sup>	Effective number of bits	$f_{\text{IN}} = 10$ MHz	11.5			11.5			Bits
		$f_{\text{IN}} = 20$ MHz	11	11.4		11.4			
		$f_{\text{IN}} = 70$ MHz	11.4			11.4			
		$f_{\text{IN}} = 100$ MHz	11.4			11.4			
		$f_{\text{IN}} = 170$ MHz	11.3			11.3			
		$f_{\text{IN}} = 230$ MHz	11.1			11.1			
SFDR	Spurious-free dynamic range	$f_{\text{IN}} = 10$ MHz	93			90			dBc
		$f_{\text{IN}} = 20$ MHz	84	91		85			
		$f_{\text{IN}} = 70$ MHz	93			88			
		$f_{\text{IN}} = 100$ MHz	85			82			
		$f_{\text{IN}} = 170$ MHz	86			85			
		$f_{\text{IN}} = 230$ MHz	82			82			

(1) Reported from a 1-MHz offset.



**AC Performance: ADC3421 (continued)**

Typical values are over the operating free-air temperature range, at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle,  $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$ , and  $-1\text{-dBFS}$  differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC3421 ( $f_S = 25\text{ MSPS}$ )						UNIT
		DITHER ON			DITHER OFF			
		MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second-order harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		93			92	dBc
		$f_{\text{IN}} = 20\text{ MHz}$	84	100			94	
		$f_{\text{IN}} = 70\text{ MHz}$		93			92	
		$f_{\text{IN}} = 100\text{ MHz}$		94			93	
		$f_{\text{IN}} = 170\text{ MHz}$		86			85	
		$f_{\text{IN}} = 230\text{ MHz}$		86			82	
HD3	Third-order harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		96			90	dBc
		$f_{\text{IN}} = 20\text{ MHz}$	84	91			85	
		$f_{\text{IN}} = 70\text{ MHz}$		93			88	
		$f_{\text{IN}} = 100\text{ MHz}$		85			82	
		$f_{\text{IN}} = 170\text{ MHz}$		89			89	
		$f_{\text{IN}} = 230\text{ MHz}$		82			82	
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	$f_{\text{IN}} = 10\text{ MHz}$		99			92	dBc
		$f_{\text{IN}} = 20\text{ MHz}$	87	98			91	
		$f_{\text{IN}} = 70\text{ MHz}$		96			92	
		$f_{\text{IN}} = 100\text{ MHz}$		95			93	
		$f_{\text{IN}} = 170\text{ MHz}$		92			90	
		$f_{\text{IN}} = 230\text{ MHz}$		97			91	
THD	Total harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		90			86	dBc
		$f_{\text{IN}} = 20\text{ MHz}$	81	90			83	
		$f_{\text{IN}} = 70\text{ MHz}$		89			85	
		$f_{\text{IN}} = 100\text{ MHz}$		84			80	
		$f_{\text{IN}} = 170\text{ MHz}$		84			83	
		$f_{\text{IN}} = 230\text{ MHz}$		80			79	
IMD3	Two-tone, third-order intermodulation distortion	$f_{\text{IN1}} = 45\text{ MHz}$ , $f_{\text{IN2}} = 50\text{ MHz}$		-98			-98	dBFS
		$f_{\text{IN1}} = 185\text{ MHz}$ , $f_{\text{IN2}} = 190\text{ MHz}$		-91			-91	

## 7.9 AC Performance: ADC3422

Typical values are over the operating free-air temperature range, at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle,  $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$ , and  $-1\text{-dBFS}$  differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3422 ( $f_s = 50\text{ MSPS}$ )						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio (from 1-MHz offset)	$f_{\text{IN}} = 10\text{ MHz}$	70.8			71			dBFS
		$f_{\text{IN}} = 20\text{ MHz}$	68.9	70.6		70.8			
		$f_{\text{IN}} = 70\text{ MHz}$	70.5			70.7			
		$f_{\text{IN}} = 100\text{ MHz}$	70.4			70.6			
		$f_{\text{IN}} = 170\text{ MHz}$	69.8			70.1			
		$f_{\text{IN}} = 230\text{ MHz}$	68.8			69			
	Signal-to-noise ratio (full Nyquist band)	$f_{\text{IN}} = 10\text{ MHz}$	70.2			70.4			
		$f_{\text{IN}} = 20\text{ MHz}$	69.8			70.0			
		$f_{\text{IN}} = 70\text{ MHz}$	69.7			69.9			
		$f_{\text{IN}} = 100\text{ MHz}$	69.8			70.1			
		$f_{\text{IN}} = 170\text{ MHz}$	69.3			69.5			
		$f_{\text{IN}} = 230\text{ MHz}$	68.2			68.4			
NSD <sup>(1)</sup>	Noise spectral density (averaged across Nyquist zone)	$f_{\text{IN}} = 10\text{ MHz}$	-144.6			-144.8			dBFS/Hz
		$f_{\text{IN}} = 20\text{ MHz}$	-144.4	-142.7		-144.6			
		$f_{\text{IN}} = 70\text{ MHz}$	-144.3			-144.5			
		$f_{\text{IN}} = 100\text{ MHz}$	-144.2			-144.4			
		$f_{\text{IN}} = 170\text{ MHz}$	-143.6			-143.9			
		$f_{\text{IN}} = 230\text{ MHz}$	-142.6			-142.8			
SINAD <sup>(1)</sup>	Signal-to-noise and distortion ratio	$f_{\text{IN}} = 10\text{ MHz}$	70.8			71			dBFS
		$f_{\text{IN}} = 20\text{ MHz}$	67.9	70.7		70.9			
		$f_{\text{IN}} = 70\text{ MHz}$	70.3			70.6			
		$f_{\text{IN}} = 100\text{ MHz}$	70.6			70.8			
		$f_{\text{IN}} = 170\text{ MHz}$	69.7			69.9			
		$f_{\text{IN}} = 230\text{ MHz}$	68.6			68.8			
ENOB <sup>(1)</sup>	Effective number of bits	$f_{\text{IN}} = 10\text{ MHz}$	11.5			11.5			Bits
		$f_{\text{IN}} = 20\text{ MHz}$	11	11.4		11.5			
		$f_{\text{IN}} = 70\text{ MHz}$	11.4			11.5			
		$f_{\text{IN}} = 100\text{ MHz}$	11.4			11.5			
		$f_{\text{IN}} = 170\text{ MHz}$	11.3			11.3			
		$f_{\text{IN}} = 230\text{ MHz}$	11.1			11.1			
SFDR	Spurious-free dynamic range	$f_{\text{IN}} = 10\text{ MHz}$	90			92			dBc
		$f_{\text{IN}} = 20\text{ MHz}$	82	95		90			
		$f_{\text{IN}} = 70\text{ MHz}$	93			92			
		$f_{\text{IN}} = 100\text{ MHz}$	87			87			
		$f_{\text{IN}} = 170\text{ MHz}$	87			86			
		$f_{\text{IN}} = 230\text{ MHz}$	83			83			

(1) Reported from a 1-MHz offset.

**AC Performance: ADC3422 (continued)**

Typical values are over the operating free-air temperature range, at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle,  $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$ , and  $-1\text{-dBFS}$  differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC3422 ( $f_S = 50\text{ MSPS}$ )						UNIT
		DITHER ON			DITHER OFF			
		MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second-order harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		95			92	dBc
		$f_{\text{IN}} = 20\text{ MHz}$	83	98			95	
		$f_{\text{IN}} = 70\text{ MHz}$		93			92	
		$f_{\text{IN}} = 100\text{ MHz}$		94			92	
		$f_{\text{IN}} = 170\text{ MHz}$		87			86	
		$f_{\text{IN}} = 230\text{ MHz}$		85			83	
HD3	Third-order harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		90			92	dBc
		$f_{\text{IN}} = 20\text{ MHz}$	82	94			92	
		$f_{\text{IN}} = 70\text{ MHz}$		94			92	
		$f_{\text{IN}} = 100\text{ MHz}$		87			87	
		$f_{\text{IN}} = 170\text{ MHz}$		88			89	
		$f_{\text{IN}} = 230\text{ MHz}$		83			88	
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	$f_{\text{IN}} = 10\text{ MHz}$		99			93	dBc
		$f_{\text{IN}} = 20\text{ MHz}$	87	99			93	
		$f_{\text{IN}} = 70\text{ MHz}$		98			92	
		$f_{\text{IN}} = 100\text{ MHz}$		95			94	
		$f_{\text{IN}} = 170\text{ MHz}$		96			89	
		$f_{\text{IN}} = 230\text{ MHz}$		96			90	
THD	Total harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		88			87	dBc
		$f_{\text{IN}} = 20\text{ MHz}$	79	89			89	
		$f_{\text{IN}} = 70\text{ MHz}$		90			87	
		$f_{\text{IN}} = 100\text{ MHz}$		86			85	
		$f_{\text{IN}} = 170\text{ MHz}$		84			83	
		$f_{\text{IN}} = 230\text{ MHz}$		81			81	
IMD3	Two-tone, third-order intermodulation distortion	$f_{\text{IN1}} = 45\text{ MHz}$ , $f_{\text{IN2}} = 50\text{ MHz}$		-95			-95	dBFS
		$f_{\text{IN1}} = 185\text{ MHz}$ , $f_{\text{IN2}} = 190\text{ MHz}$		-88			-88	

## 7.10 AC Performance: ADC3423

Typical values are over the operating free-air temperature range, at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3423 ( $f_s = 80$ MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio (from 1-MHz offset)	$f_{\text{IN}} = 10$ MHz	70.7			70.9			dBFS
		$f_{\text{IN}} = 70$ MHz	68.7	70.5		70.7			
		$f_{\text{IN}} = 100$ MHz	70.3			70.5			
		$f_{\text{IN}} = 170$ MHz	70.1			70.3			
		$f_{\text{IN}} = 230$ MHz	69.6			69.9			
	Signal-to-noise ratio (full Nyquist band)	$f_{\text{IN}} = 10$ MHz	70.3			70.5			
		$f_{\text{IN}} = 70$ MHz	70.1			70.4			
		$f_{\text{IN}} = 100$ MHz	69.9			70.2			
		$f_{\text{IN}} = 170$ MHz	69.7			69.9			
		$f_{\text{IN}} = 230$ MHz	69.3			69.6			
NSD <sup>(1)</sup>	Noise spectral density (averaged across Nyquist zone)	$f_{\text{IN}} = 10$ MHz	–146.6			–146.8			dBFS/Hz
		$f_{\text{IN}} = 70$ MHz	–146.4	–144.6		–146.6			
		$f_{\text{IN}} = 100$ MHz	–146.2			–146.4			
		$f_{\text{IN}} = 170$ MHz	–146.0			–146.2			
		$f_{\text{IN}} = 230$ MHz	–145.5			–145.8			
SINAD <sup>(1)</sup>	Signal-to-noise and distortion ratio	$f_{\text{IN}} = 10$ MHz	70.7			70.8			dBFS
		$f_{\text{IN}} = 70$ MHz	67.7	70.3		70.4			
		$f_{\text{IN}} = 100$ MHz	70.4			70.7			
		$f_{\text{IN}} = 170$ MHz	70			70.2			
		$f_{\text{IN}} = 230$ MHz	69.5			69.7			
ENOB <sup>(1)</sup>	Effective number of bits	$f_{\text{IN}} = 10$ MHz	11.5			11.5			Bits
		$f_{\text{IN}} = 70$ MHz	11	11.4		11.4			
		$f_{\text{IN}} = 100$ MHz	11.4			11.5			
		$f_{\text{IN}} = 170$ MHz	11.3			11.4			
		$f_{\text{IN}} = 230$ MHz	11.3			11.3			
SFDR	Spurious-free dynamic range	$f_{\text{IN}} = 10$ MHz	90			90			dBc
		$f_{\text{IN}} = 70$ MHz	81	91		90			
		$f_{\text{IN}} = 100$ MHz	93			93			
		$f_{\text{IN}} = 170$ MHz	88			86			
		$f_{\text{IN}} = 230$ MHz	87			85			

(1) Reported from a 1-MHz offset.

**AC Performance: ADC3423 (continued)**

Typical values are over the operating free-air temperature range, at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle,  $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$ , and  $-1\text{-dBFS}$  differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC3423 ( $f_S = 80\text{ MSPS}$ )						UNIT
		DITHER ON			DITHER OFF			
		MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second-order harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		94		91		dBc
		$f_{\text{IN}} = 70\text{ MHz}$	81	96		92		
		$f_{\text{IN}} = 100\text{ MHz}$		97		93		
		$f_{\text{IN}} = 170\text{ MHz}$		88		86		
		$f_{\text{IN}} = 230\text{ MHz}$		87		85		
HD3	Third-order harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		90		90		dBc
		$f_{\text{IN}} = 70\text{ MHz}$	81	91		90		
		$f_{\text{IN}} = 100\text{ MHz}$		93		99		
		$f_{\text{IN}} = 170\text{ MHz}$		96		93		
		$f_{\text{IN}} = 230\text{ MHz}$		87		87		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	$f_{\text{IN}} = 10\text{ MHz}$		99		94		dBc
		$f_{\text{IN}} = 70\text{ MHz}$	86	98		93		
		$f_{\text{IN}} = 100\text{ MHz}$		94		94		
		$f_{\text{IN}} = 170\text{ MHz}$		95		92		
		$f_{\text{IN}} = 230\text{ MHz}$		94		91		
THD	Total harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		88		86		dBc
		$f_{\text{IN}} = 70\text{ MHz}$	78	89		86		
		$f_{\text{IN}} = 100\text{ MHz}$		91		90		
		$f_{\text{IN}} = 170\text{ MHz}$		87		84		
		$f_{\text{IN}} = 230\text{ MHz}$		84		82		
IMD3	Two-tone, third-order intermodulation distortion	$f_{\text{IN1}} = 45\text{ MHz}$ , $f_{\text{IN2}} = 50\text{ MHz}$		-97		-97		dBFS
		$f_{\text{IN1}} = 185\text{ MHz}$ , $f_{\text{IN2}} = 190\text{ MHz}$		-92		-92		

## 7.11 AC Performance: ADC3424

Typical values are over the operating free-air temperature range, at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$ , and  $-1\text{-dBFS}$  differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3424 ( $f_s = 125\text{ MSPS}$ )						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio (from 1-MHz offset)	$f_{\text{IN}} = 10\text{ MHz}$	70.5			70.7			dBFS
		$f_{\text{IN}} = 70\text{ MHz}$	68	70.3		70.6			
		$f_{\text{IN}} = 100\text{ MHz}$	70.1			70.4			
		$f_{\text{IN}} = 170\text{ MHz}$	69.8			70.3			
		$f_{\text{IN}} = 230\text{ MHz}$	69.2			69.9			
	Signal-to-noise ratio (full Nyquist band)	$f_{\text{IN}} = 10\text{ MHz}$	70.3			70.5			
		$f_{\text{IN}} = 70\text{ MHz}$	70.1			70.4			
		$f_{\text{IN}} = 100\text{ MHz}$	70.0			70.2			
		$f_{\text{IN}} = 170\text{ MHz}$	69.6			70.1			
		$f_{\text{IN}} = 230\text{ MHz}$	69.0			69.7			
NSD <sup>(1)</sup>	Noise spectral density (averaged across Nyquist zone)	$f_{\text{IN}} = 10\text{ MHz}$	-148.4			-148.6			dBFS/Hz
		$f_{\text{IN}} = 70\text{ MHz}$	-148.2	-145.9		-148.5			
		$f_{\text{IN}} = 100\text{ MHz}$	-148.0			-148.3			
		$f_{\text{IN}} = 170\text{ MHz}$	-147.7			-148.2			
		$f_{\text{IN}} = 230\text{ MHz}$	-147.1			-147.8			
SINAD <sup>(1)</sup>	Signal-to-noise and distortion ratio	$f_{\text{IN}} = 10\text{ MHz}$	70.5			70.6			dBFS
		$f_{\text{IN}} = 70\text{ MHz}$	67	70.3		70.5			
		$f_{\text{IN}} = 100\text{ MHz}$	70.1			70.5			
		$f_{\text{IN}} = 170\text{ MHz}$	69.7			70.1			
		$f_{\text{IN}} = 230\text{ MHz}$	68.6			69.1			
ENOB <sup>(1)</sup>	Effective number of bits	$f_{\text{IN}} = 10\text{ MHz}$	11.4			11.4			Bits
		$f_{\text{IN}} = 70\text{ MHz}$	10.8	11.4		11.4			
		$f_{\text{IN}} = 100\text{ MHz}$	11.4			11.4			
		$f_{\text{IN}} = 170\text{ MHz}$	11.3			11.4			
		$f_{\text{IN}} = 230\text{ MHz}$	11.2			11.3			
SFDR	Spurious-free dynamic range	$f_{\text{IN}} = 10\text{ MHz}$	93			89			dBc
		$f_{\text{IN}} = 70\text{ MHz}$	80	94		90			
		$f_{\text{IN}} = 100\text{ MHz}$	90			87			
		$f_{\text{IN}} = 170\text{ MHz}$	86			85			
		$f_{\text{IN}} = 230\text{ MHz}$	81			80			

(1) Reported from a 1-MHz offset.

**AC Performance: ADC3424 (continued)**

Typical values are over the operating free-air temperature range, at  $T_A = 25^\circ\text{C}$ , full temperature range is  $T_{\text{MIN}} = -40^\circ\text{C}$  to  $T_{\text{MAX}} = 85^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{\text{DD}} = DV_{\text{DD}} = 1.8\text{ V}$ , and  $-1\text{-dBFS}$  differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC3424 ( $f_s = 125\text{ MSPS}$ )						UNIT
		DITHER ON			DITHER OFF			
		MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second-order harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		93			92	dBc
		$f_{\text{IN}} = 70\text{ MHz}$	80	94			91	
		$f_{\text{IN}} = 100\text{ MHz}$		90			91	
		$f_{\text{IN}} = 170\text{ MHz}$		86			85	
		$f_{\text{IN}} = 230\text{ MHz}$		81			80	
HD3	Third-order harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		96			88	dBc
		$f_{\text{IN}} = 70\text{ MHz}$	81	95			89	
		$f_{\text{IN}} = 100\text{ MHz}$		97			90	
		$f_{\text{IN}} = 170\text{ MHz}$		93			87	
		$f_{\text{IN}} = 230\text{ MHz}$		87			86	
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	$f_{\text{IN}} = 10\text{ MHz}$		100			93	dBc
		$f_{\text{IN}} = 70\text{ MHz}$	86	99			94	
		$f_{\text{IN}} = 100\text{ MHz}$		94			93	
		$f_{\text{IN}} = 170\text{ MHz}$		95			92	
		$f_{\text{IN}} = 230\text{ MHz}$		94			90	
THD	Total harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		90			85	dBc
		$f_{\text{IN}} = 70\text{ MHz}$	77	90			85	
		$f_{\text{IN}} = 100\text{ MHz}$		88			86	
		$f_{\text{IN}} = 170\text{ MHz}$		85			82	
		$f_{\text{IN}} = 230\text{ MHz}$		80			78	
IMD3	Two-tone, third-order intermodulation distortion	$f_{\text{IN1}} = 45\text{ MHz}$ , $f_{\text{IN2}} = 50\text{ MHz}$		95			95	dBFS
		$f_{\text{IN1}} = 185\text{ MHz}$ , $f_{\text{IN2}} = 190\text{ MHz}$		89			89	

## 7.12 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, PDN)</b>						
V <sub>IH</sub>	High-level input voltage	All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V <sub>IL</sub>	Low-level input voltage	All digital inputs support 1.8-V and 3.3-V CMOS logic levels			0.4	V
I <sub>IH</sub>	High-level input current	RESET, SDATA, SCLK, PDN	V <sub>HIGH</sub> = 1.8 V	10		μA
		SEN <sup>(1)</sup>	V <sub>HIGH</sub> = 1.8 V	0		μA
I <sub>IL</sub>	Low-level input current	RESET, SDATA, SCLK, PDN	V <sub>LOW</sub> = 0 V	0		μA
		SEN	V <sub>LOW</sub> = 0 V	10		μA
<b>DIGITAL INPUTS (SYSREFF, SYSREFM)</b>						
V <sub>IH</sub>	High-level input voltage			1.3		V
V <sub>IL</sub>	Low-level input voltage			0.5		V
	Common-mode voltage for SYSREF			0.9		V
<b>DIGITAL OUTPUTS (CMOS Interface, SDOOUT)</b>						
V <sub>OH</sub>	High-level output voltage		DVDD – 0.1	DVDD		V
V <sub>OL</sub>	Low-level output voltage			0	0.1	V
<b>DIGITAL OUTPUTS (LVDS Interface)</b>						
V <sub>ODH</sub>	High-level output differential voltage	With an external 100-Ω termination	280	350	460	mV
V <sub>ODL</sub>	Low-level output differential voltage	With an external 100-Ω termination	–460	–350	–280	mV
V <sub>OCM</sub>	Output common-mode voltage			1.05		V

(1) SEN has an internal 150-kΩ pullup resistor to AVDD. SPI pins (SEN, SCLK, SDATA) can be driven by 1.8 V or 3.3 V CMOS buffers.

## 7.13 Timing Requirements: General

Typical values are at T<sub>A</sub> = 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T<sub>MIN</sub> = –40°C to T<sub>MAX</sub> = 85°C.

		MIN	TYP	MAX	UNIT
t <sub>A</sub>	Aperture delay	1.24	1.44	1.64	ns
	Aperture delay matching between two channels of the same device		±70		ps
	Aperture delay variation between two devices at same temperature and supply voltage		±150		ps
t <sub>J</sub>	Aperture jitter		130		f <sub>S</sub> rms
	Wake-up time:	Time to valid data after exiting standby power-down mode		35	200
Time to valid data after exiting global power-down mode (in this mode, both channels power down)			85	450	μs
ADC latency <sup>(1)</sup> :	2-wire mode (default)		9		Clock cycles
	1-wire mode		8		Clock cycles
t <sub>SU_SYSREF</sub>	SYSREF reference time:	Setup time for SYSREF referenced to input clock rising edge	1000		ps
t <sub>H_SYSREF</sub>		Hold time for SYSREF referenced to input clock rising edge	100		ps

(1) Overall latency = ADC latency + t<sub>PDJ</sub>.



## 7.14 Timing Requirements: LVDS Output<sup>(1)(2)</sup>

Typical values are at  $T_A = 25^\circ\text{C}$ ,  $AVDD = DVDD = 1.8\text{ V}$ , and  $-1\text{-dBFS}$  differential input, 6x Serialization (2-Wire Mode),  $C_{LOAD} = 3.3\text{ pF}^{(3)}$ , and  $R_{LOAD} = 100\ \Omega^{(4)}$ , unless otherwise noted.. Minimum and maximum values are across the full temperature range:  $T_{MIN} = -40^\circ\text{C}$  to  $T_{MAX} = 85^\circ\text{C}$ .

		MIN	TYP	MAX	UNIT
$t_{SU}$	Data setup time: data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM) <sup>(5)</sup>	0.43	0.5		ns
$t_{HO}$	Data hold time: zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid <sup>(5)</sup>	0.48	0.58		ns
$t_{PDI}$	Clock propagation delay: input clock falling edge cross-over to frame clock rising edge cross-over (15 MSPS < sampling frequency < 125 MSPS)	1-wire mode	4.5	6.5	ns
		2-wire mode	$0.44 \times t_S + t_{DELAY}$		ns
$t_{DELAY}$	Delay time	3	4.5	5.9	ns
	LVDS bit clock duty cycle: duty cycle of differential clock (CLKOUTP – CLKOUTM)		49%		
$t_{FALL}$ , $t_{RISE}$	Data fall time, data rise time: rise time measured from $-100\text{ mV}$ to $100\text{ mV}$ , $15\text{ MSPS} \leq \text{Sampling frequency} \leq 125\text{ MSPS}$		0.11		ns
$t_{CLKRISE}$ , $t_{CLKFALL}$	Output clock rise time, output clock fall time: rise time measured from $-100\text{ mV}$ to $100\text{ mV}$ , $15\text{ MSPS} \leq \text{Sampling frequency} \leq 125\text{ MSPS}$		0.11		ns

- (1) Measurements are done with a transmission line of a  $100\text{-}\Omega$  characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
- (2) Timing parameters are ensured by design and characterization and are not tested in production.
- (3)  $C_{LOAD}$  is the effective external single-ended load capacitance between each output pin and ground.
- (4)  $R_{LOAD}$  is the differential load resistance between the LVDS output pair.
- (5) Data valid refers to a logic high of  $100\text{ mV}$  and a logic low of  $-100\text{ mV}$ .

**Table 1. LVDS Timing at Lower Sampling Frequencies: 6X Serialization (2-Wire Mode)**

SAMPLING FREQUENCY (MSPS)	SETUP TIME ( $t_{SU}$ , ns)			HOLD TIME ( $t_{HO}$ , ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
25	2.61	3.06		2.75	3.12	
40	1.69	1.9		1.8	1.98	
60	1.11	1.23		1.18	1.31	
80	0.81	0.89		0.88	0.97	
100	0.6	0.68		0.68	0.77	

**Table 2. LVDS Timings at Lower Sampling Frequencies: 12X Serialization (1-Wire Mode)**

SAMPLING FREQUENCY (MSPS)	SETUP TIME ( $t_{SU}$ , ns)			HOLD TIME ( $t_{HO}$ , ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
25	1.3	1.48		1.32	1.57	
40	0.76	0.88		0.79	0.97	
50	0.57	0.68		0.61	0.77	
60	0.42	0.55		0.45	0.62	
70	0.35	0.44		0.4	0.51	
80	0.26	0.35		0.35	0.43	

### 7.15 Typical Characteristics: ADC3421

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle,  $AVDD = 1.8\text{ V}$ ,  $DVDD = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled, unless otherwise noted.

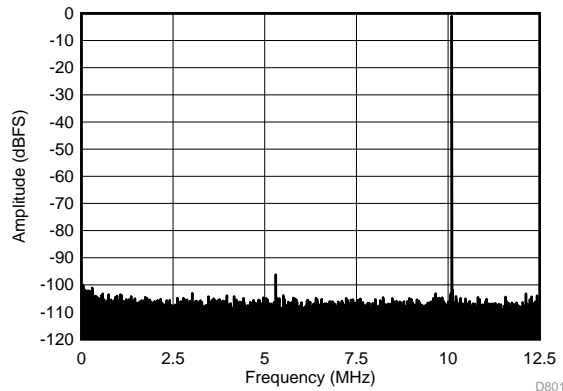


Figure 1. FFT for 10-MHz Input Signal (Dither On)

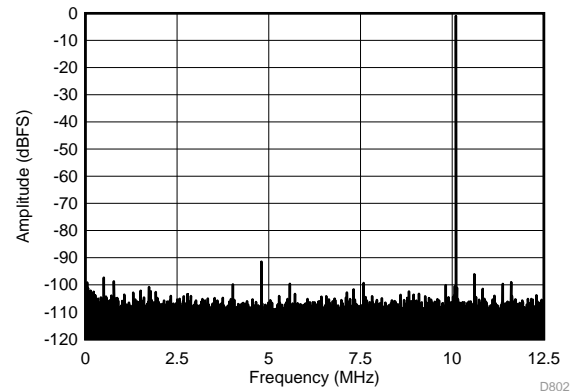


Figure 2. FFT for 10-MHz Input Signal (Dither Off)

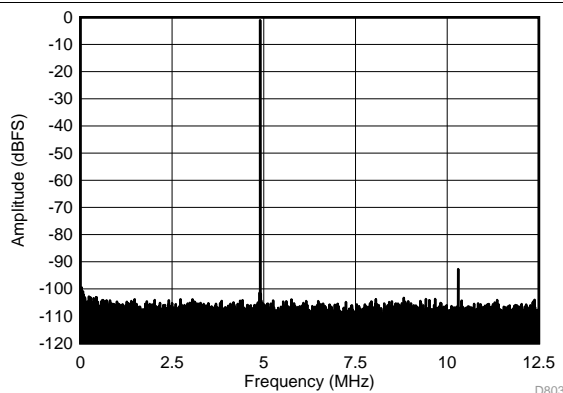


Figure 3. FFT for 70-MHz Input Signal (Dither On)

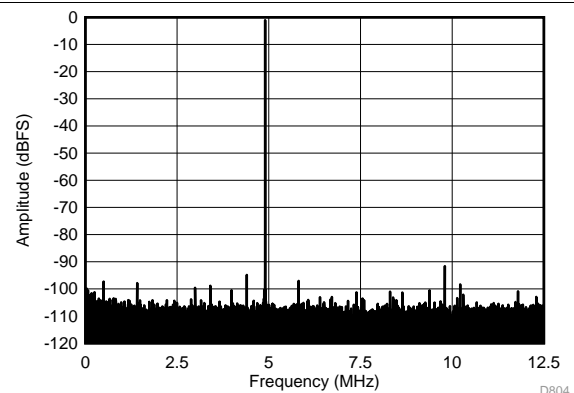


Figure 4. FFT for 70-MHz Input Signal (Dither Off)

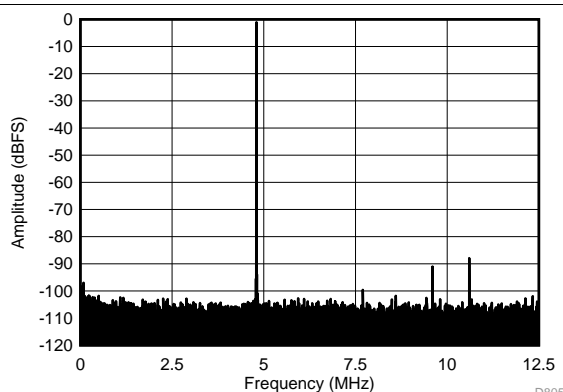


Figure 5. FFT for 170-MHz Input Signal (Dither On)

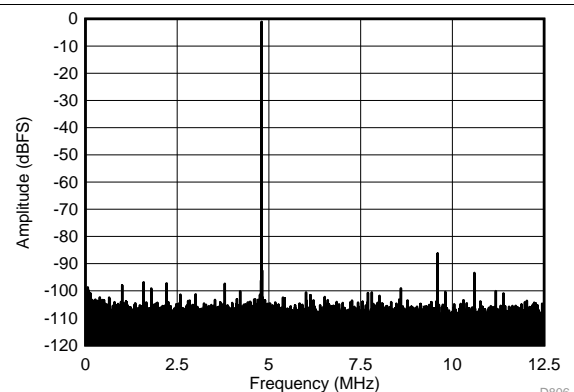
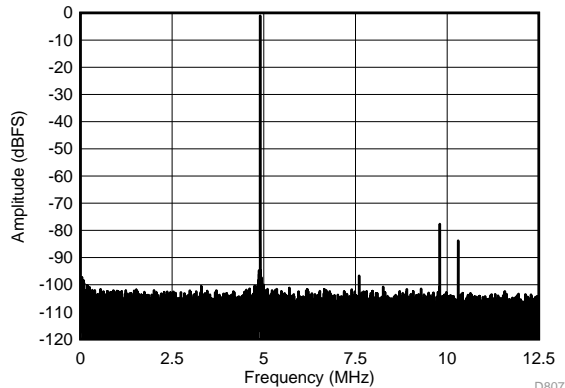


Figure 6. FFT for 170-MHz Input Signal (Dither Off)

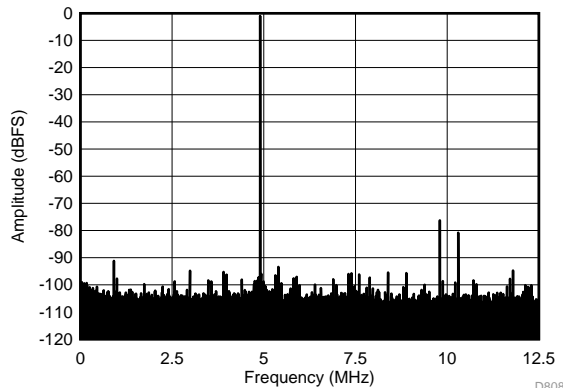
**Typical Characteristics: ADC3421 (continued)**

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, 2- $V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.



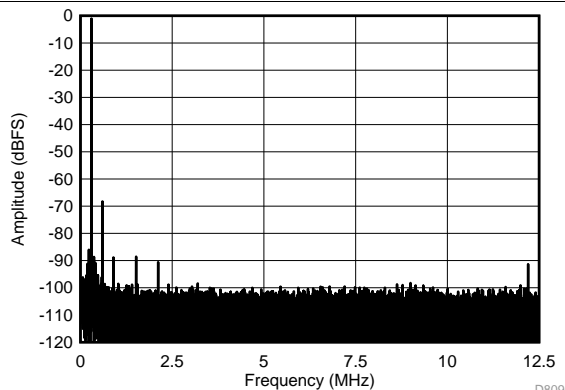
SFDR = 77 dBc, SNR = 68.2 dBFS, SINAD = 67.7 dBFS, THD = 75 dBc, HD2 = 77 dBc, HD3 = 83 dBc

**Figure 7. FFT for 270-MHz Input Signal (Dither On)**



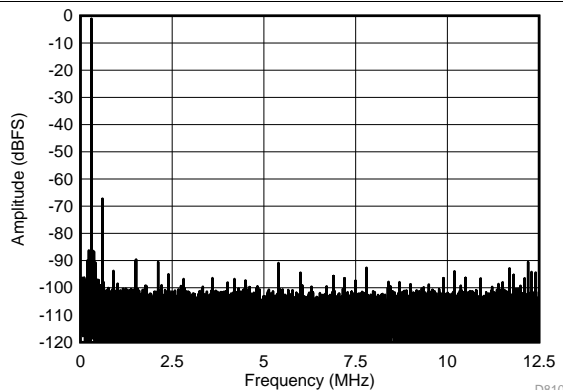
SFDR = 75 dBc, SNR = 68.4 dBFS, SINAD = 67.5 dBFS, THD = 74 dBc, HD2 = 75 dBc, HD3 = 80 dBc

**Figure 8. FFT for 270-MHz Input Signal (Dither Off)**



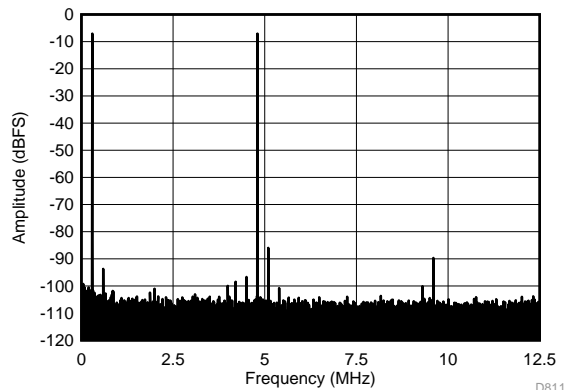
SFDR = 67 dBc, SNR = 66.4 dBFS, SINAD = 66.4 dBFS, THD = 93 dBc, HD2 = 67 dBc, HD3 = 88 dBc

**Figure 9. FFT for 450-MHz Input Signal (Dither On)**



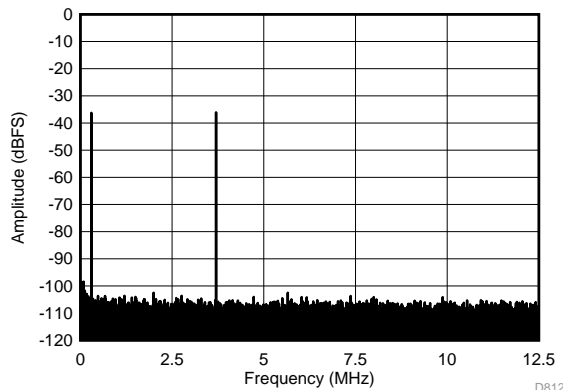
SFDR = 66 dBc, SNR = 66.5 dBFS, SINAD = 66.5 dBFS, THD = 87 dBc, HD2 = 66 dBc, HD3 = 93 dBc

**Figure 10. FFT for 450-MHz Input Signal (Dither Off)**



$f_{IN1} = 46 \text{ MHz}$ ,  $f_{IN2} = 50 \text{ MHz}$ , IMD3 = 90, each tone at = -7 dBFS

**Figure 11. FFT for Two-Tone Input Signal (-7 dBFS at 46 MHz and 50 MHz)**

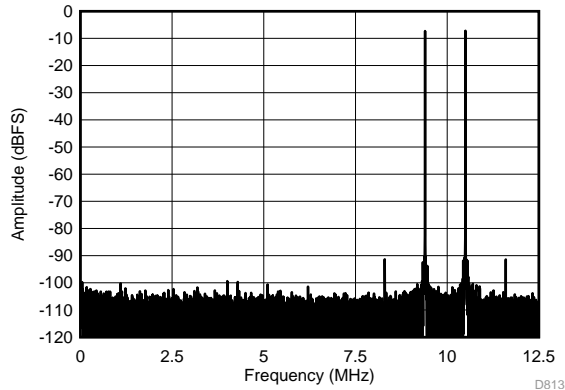


$f_{IN1} = 46 \text{ MHz}$ ,  $f_{IN2} = 50 \text{ MHz}$ , IMD3 = 105, each tone at = -36 dBFS

**Figure 12. FFT for Two-Tone Input Signal (-36 dBFS at 46 MHz and 50 MHz)**

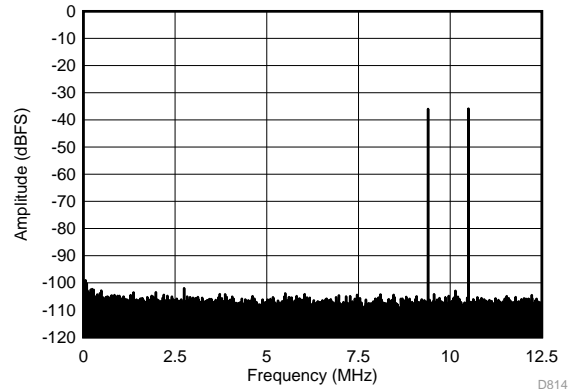
**Typical Characteristics: ADC3421 (continued)**

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.



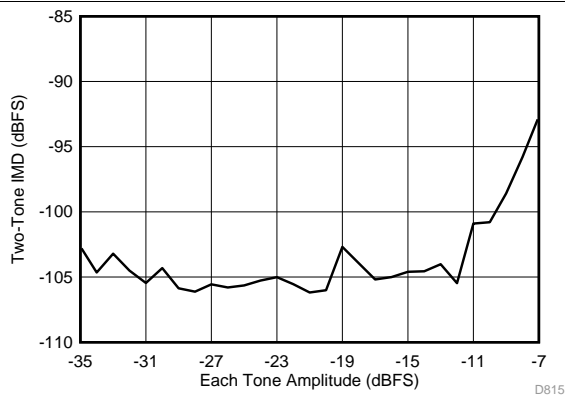
$f_{IN1} = 184.5 \text{ MHz}$ ,  $f_{IN2} = 189.5 \text{ MHz}$ ,  $\text{IMD3} = 91$ , each tone at  $-7 \text{ dBFS}$

**Figure 13. FFT for Two-Tone Input Signal (-7 dBFS at 185 MHz and 190 MHz)**

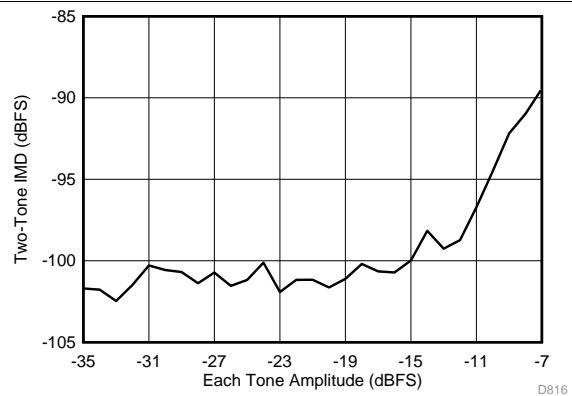


$f_{IN1} = 184.5 \text{ MHz}$ ,  $f_{IN2} = 189.5 \text{ MHz}$ ,  $\text{IMD3} = 98 \text{ dBFS}$ , each tone at  $-36 \text{ dBFS}$

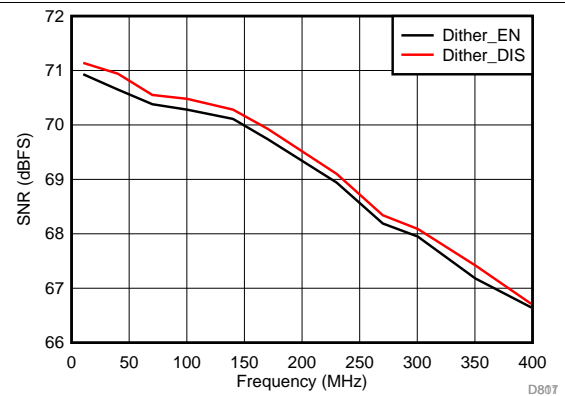
**Figure 14. FFT for Two-Tone Input Signal (-36 dBFS at 185 MHz and 190 MHz)**



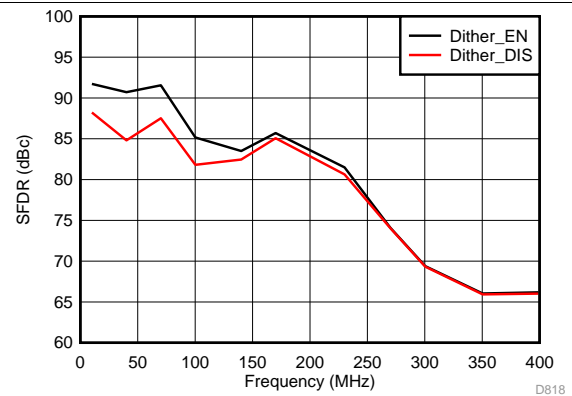
**Figure 15. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)**



**Figure 16. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)**



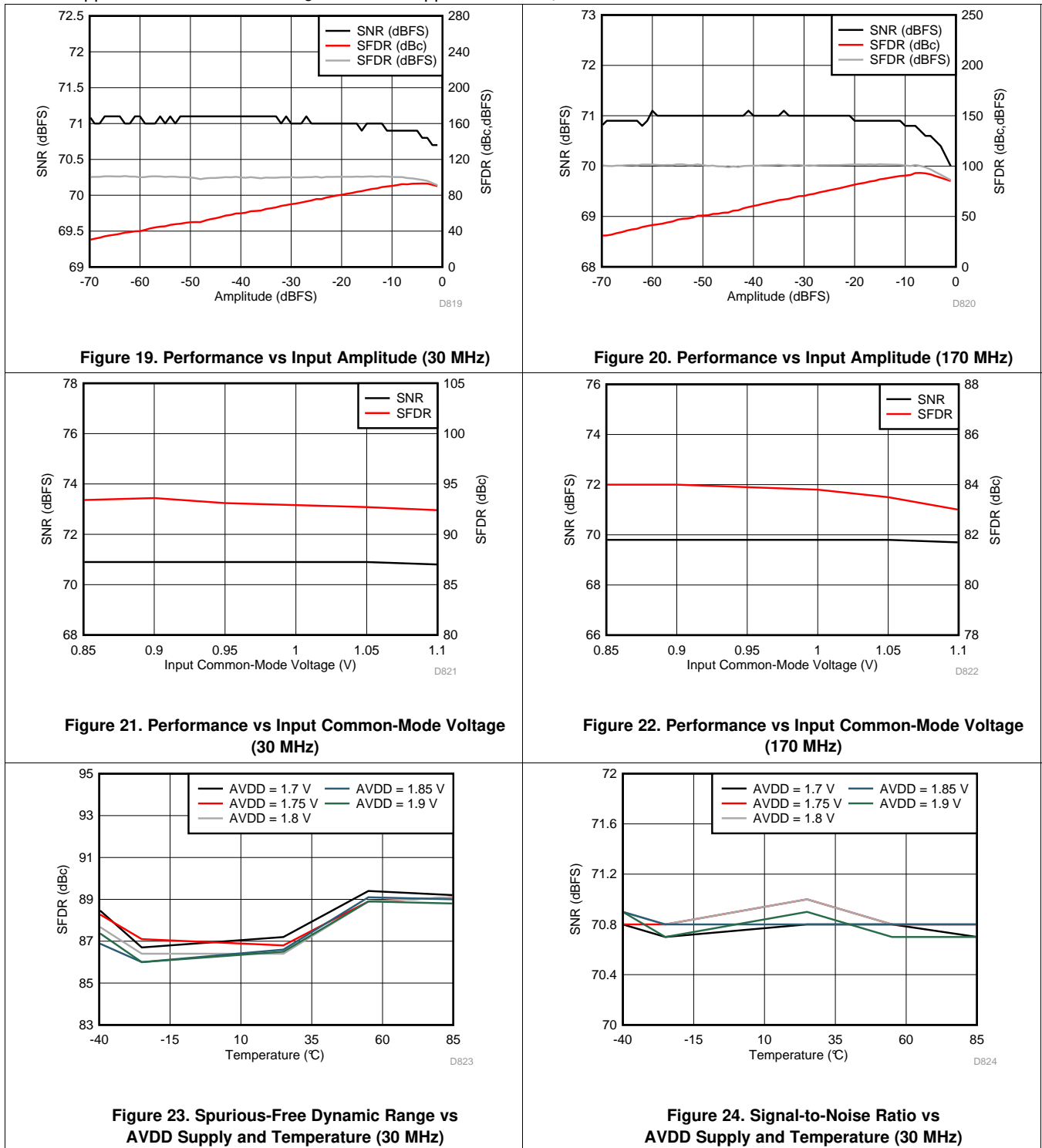
**Figure 17. Signal-to-Noise Ratio vs Input Frequency**



**Figure 18. Spurious-Free Dynamic Range vs Input Frequency**

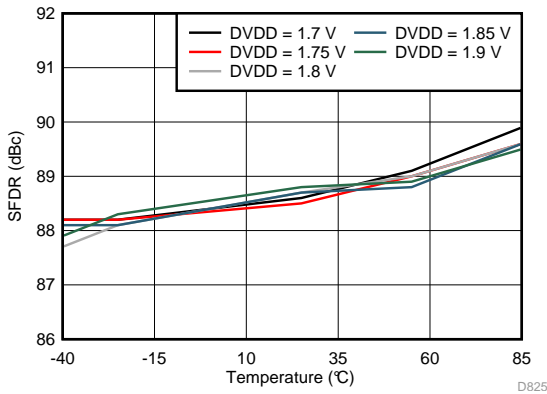
**Typical Characteristics: ADC3421 (continued)**

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.

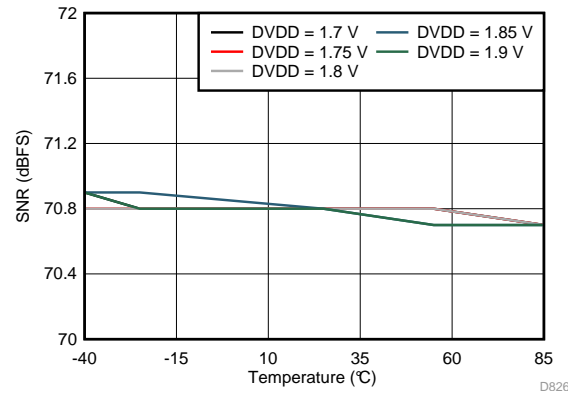


**Typical Characteristics: ADC3421 (continued)**

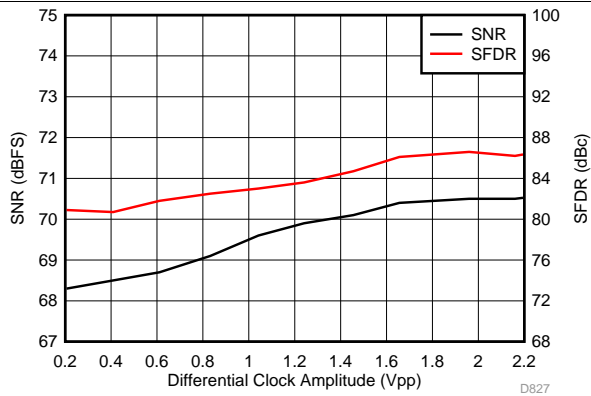
Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input,  $2\cdot V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.



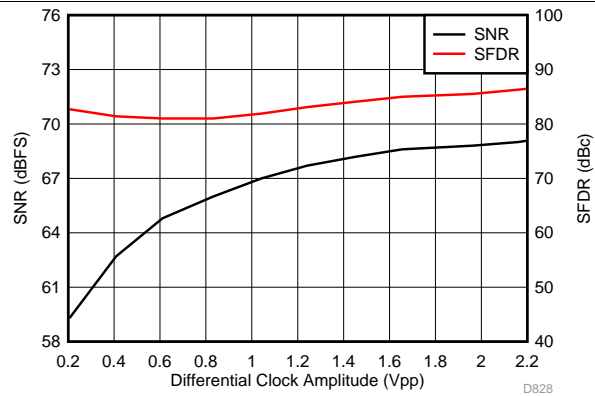
**Figure 25. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (30 MHz)**



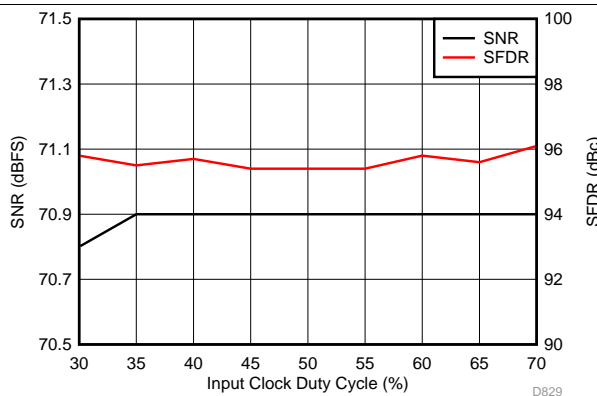
**Figure 26. Signal-to-Noise Ratio vs DVDD Supply and Temperature (30 MHz)**



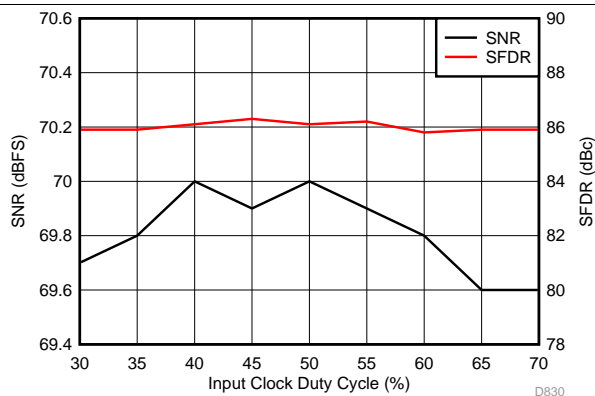
**Figure 27. Performance vs Clock Amplitude (40 MHz)**



**Figure 28. Performance vs Clock Amplitude (150 MHz)**



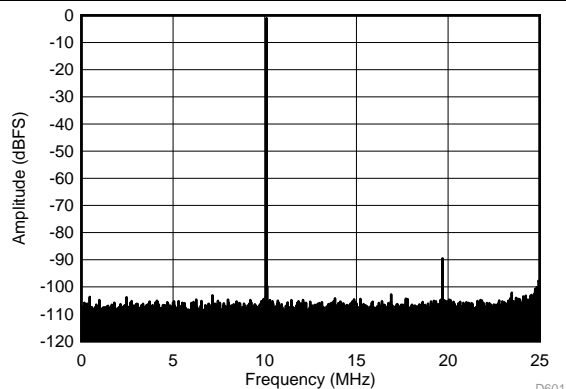
**Figure 29. Performance vs Clock Duty Cycle (30 MHz)**



**Figure 30. Performance vs Clock Duty Cycle (150 MHz)**

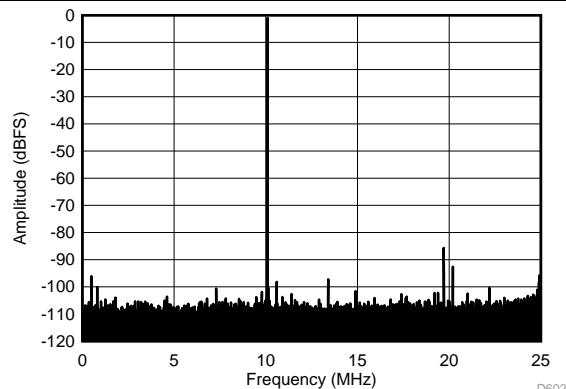
## 7.16 Typical Characteristics: ADC3422

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled, unless otherwise noted.



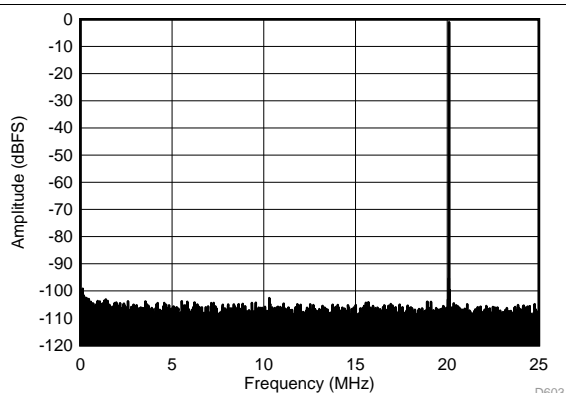
SFDR = 89 dBc, SNR = 70.9 dBFS, SINAD = 70.8 dBFS,  
THD = 88 dBc, HD2 = 110 dBc, HD3 = 89 dBc

**Figure 31. FFT for 10-MHz Input Signal (Dither On)**



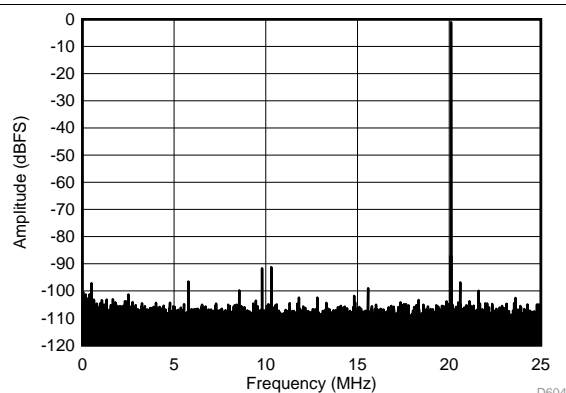
SFDR = 85 dBc, SNR = 71.2 dBFS, SINAD = 70.9 dBFS,  
THD = 83 dBc, HD2 = 92 dBc, HD3 = 85 dBc

**Figure 32. FFT for 10-MHz Input Signal (Dither Off)**



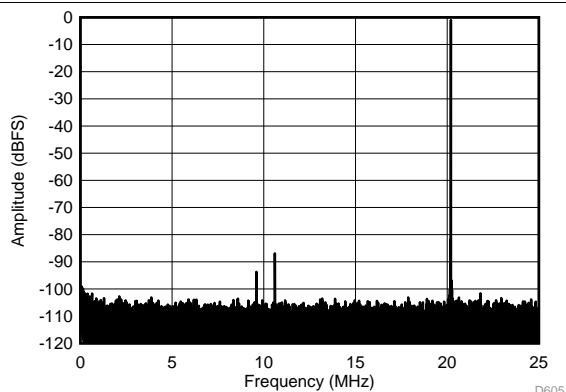
SFDR = 101 dBc, SNR = 70.6 dBFS, SINAD = 70.5 dBFS,  
THD = 98 dBc, HD2 = 106 dBc, HD3 = 101 dBc

**Figure 33. FFT for 70-MHz Input Signal (Dither On)**



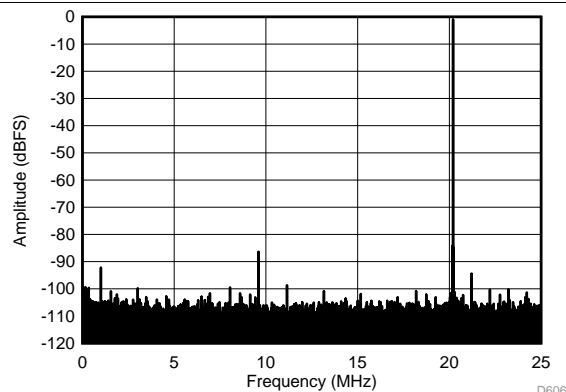
SFDR = 90 dBc, SNR = 70.8 dBFS, SINAD = 70.6 dBFS,  
THD = 87 dBc, HD2 = 91 dBc, HD3 = 90 dBc

**Figure 34. FFT for 70-MHz Input Signal (Dither Off)**



SFDR = 86 dBc, SNR = 69.9 dBFS, SINAD = 69.8 dBFS,  
THD = 85 dBc, HD2 = 93 dBc, HD3 = 86 dBc

**Figure 35. FFT for 170-MHz Input Signal (Dither On)**

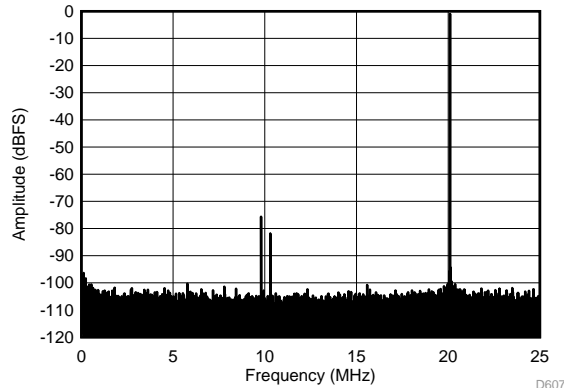


SFDR = 85 dBc, SNR = 70.1 dBFS, SINAD = 70 dBFS,  
THD = 86 dBc, HD2 = 85 dBc, HD3 = 112 dBc

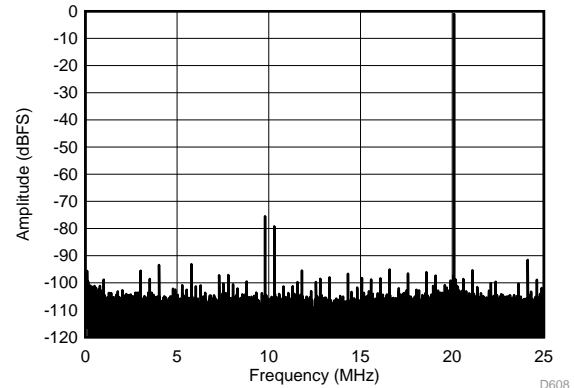
**Figure 36. FFT for 170-MHz Input Signal (Dither Off)**

**Typical Characteristics: ADC3422 (continued)**

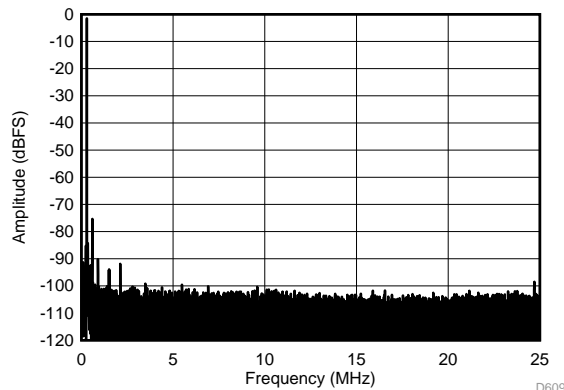
Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{ dBFS}$  differential input,  $2 \cdot V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.



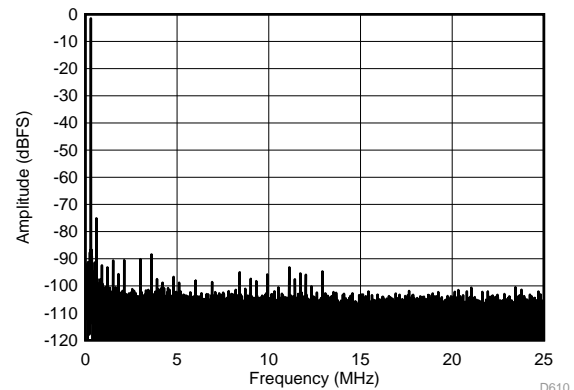
SFDR = 75 dBc, SNR = 69 dBFS, SINAD = 67.9 dBFS,  
THD = 74 dBc, HD2 = 75 dBc, HD3 = 81 dBc

**Figure 37. FFT for 270-MHz Input Signal (Dither On)**


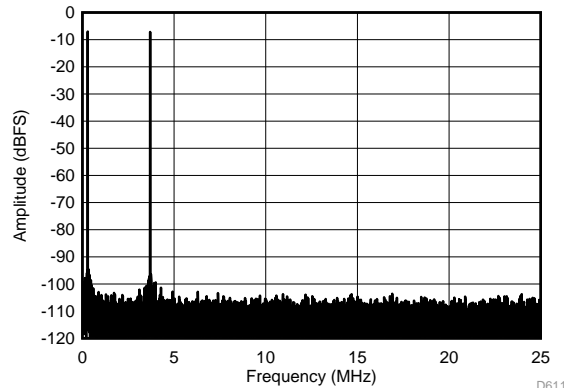
SFDR = 75 dBc, SNR = 69.2 dBFS, SINAD = 67.9 dBFS,  
THD = 73 dBc, HD2 = 75 dBc, HD3 = 81 dBc

**Figure 38. FFT for 270-MHz Input Signal (Dither Off)**


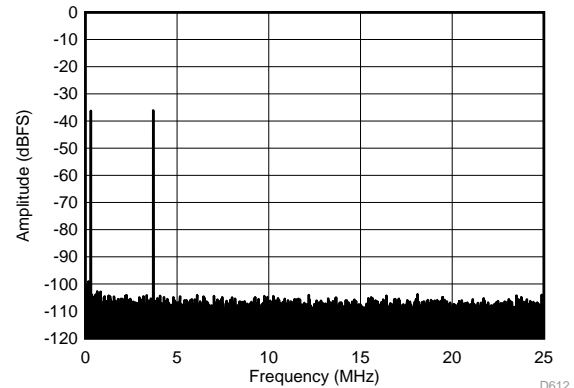
SFDR = 68 dBc, SNR = 67.2 dBFS, SINAD = 67.1 dBFS,  
THD =  $-86\text{ dBc}$ , HD2 = 75 dBc, HD3 = 73 dBc

**Figure 39. FFT for 450-MHz Input Signal (Dither On)**


SFDR = 68 dBc, SNR = 67.5 dBFS, SINAD = 67.4 dBFS,  
THD =  $-87\text{ dBc}$ , HD2 =  $-68\text{ dBc}$ , HD3 =  $-87\text{ dBc}$

**Figure 40. FFT for 450-MHz Input Signal (Dither Off)**


$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 102 dBFS,  
each tone at  $-7\text{ dBFS}$

**Figure 41. FFT for Two-Tone Input Signal  
( $-7\text{ dBFS}$  at 46 MHz and 50 MHz)**


$f_{IN1} = 46.3\text{ MHz}$ ,  $f_{IN2} = 50.3\text{ MHz}$ , IMD3 = 110 dBFS,  
each tone at  $-36\text{ dBFS}$

**Figure 42. FFT for Two-Tone Input Signal  
( $-36\text{ dBFS}$  at 46 MHz and 50 MHz)**



Typical Characteristics: ADC3422 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.

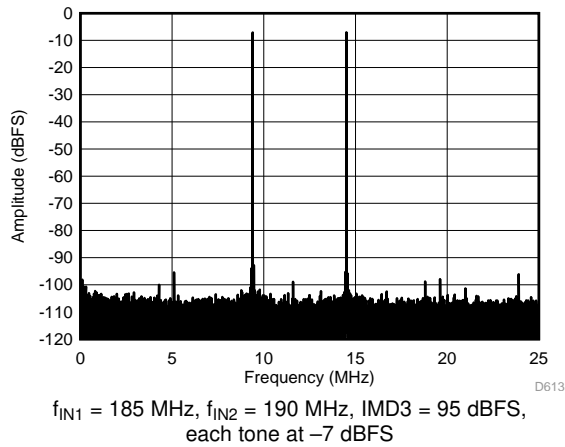


Figure 43. FFT for Two-Tone Input Signal (-7 dBFS at 185 MHz and 190 MHz)

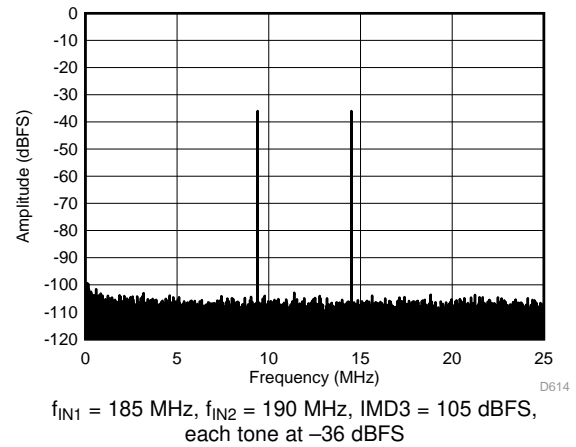


Figure 44. FFT for Two-Tone Input Signal (-36 dBFS at 185 MHz and 190 MHz)

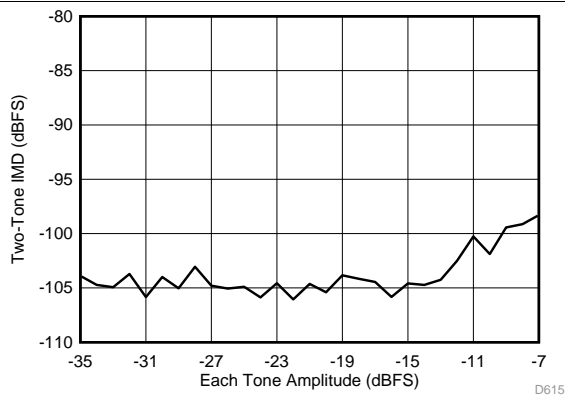


Figure 45. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

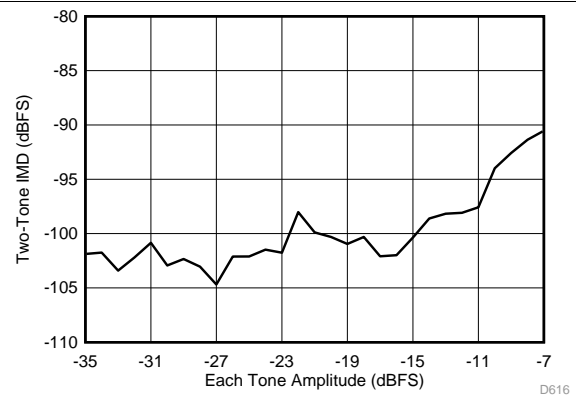


Figure 46. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

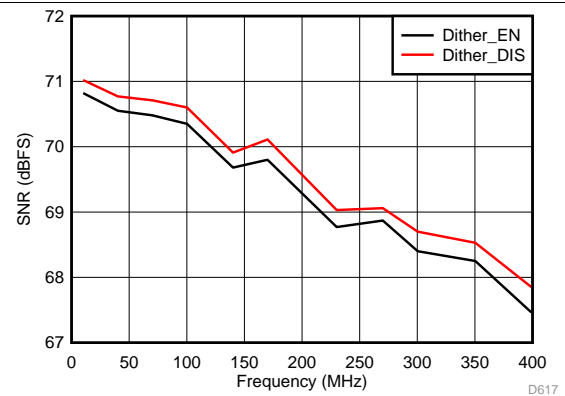


Figure 47. Signal-to-Noise Ratio vs Input Frequency

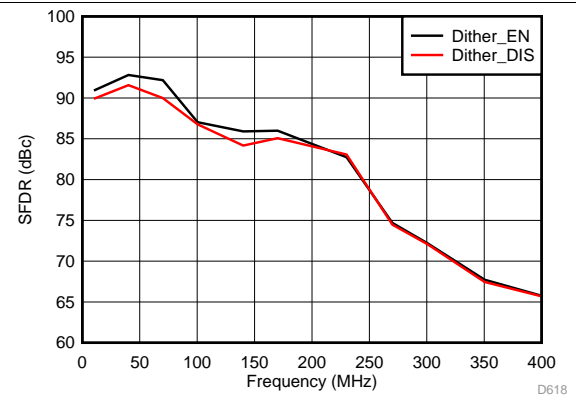


Figure 48. Spurious-Free Dynamic Range vs Input Frequency

### Typical Characteristics: ADC3422 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.

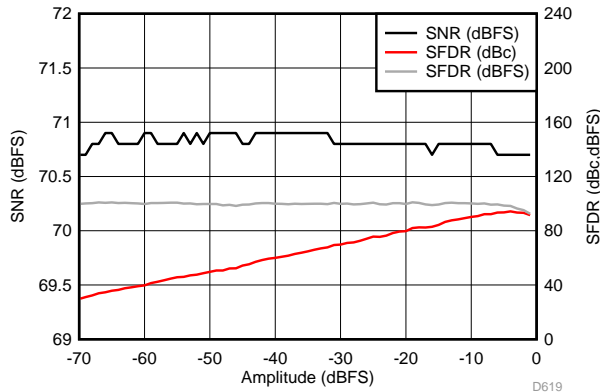


Figure 49. Performance vs Input Amplitude (30 MHz)

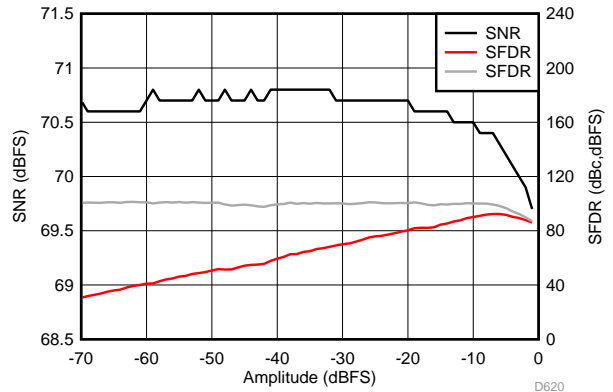


Figure 50. Performance vs Input Amplitude (170 MHz)

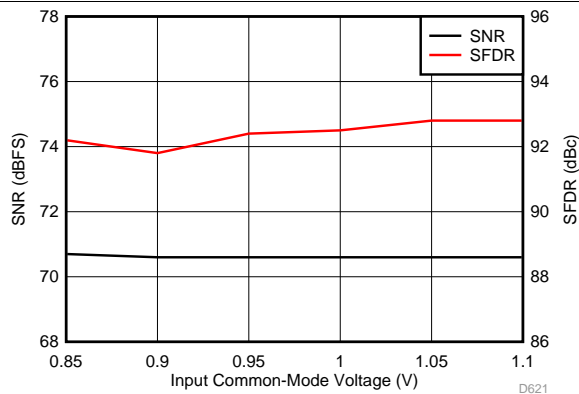


Figure 51. Performance vs Input Common-Mode Voltage (30 MHz)

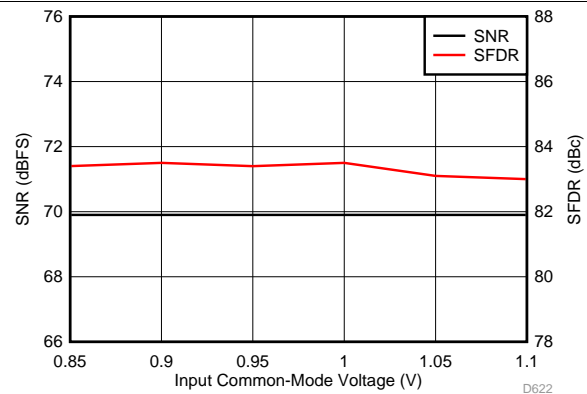


Figure 52. Performance vs Input Common-Mode Voltage (170 MHz)

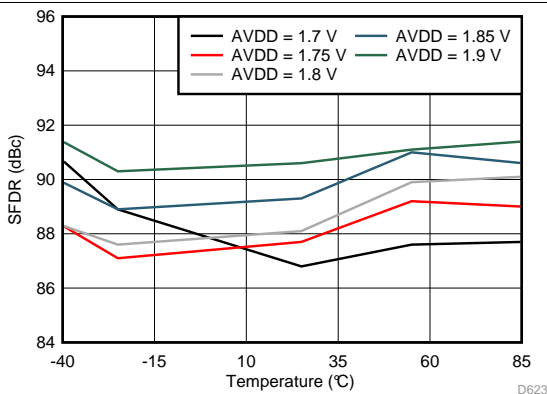


Figure 53. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (30 MHz)

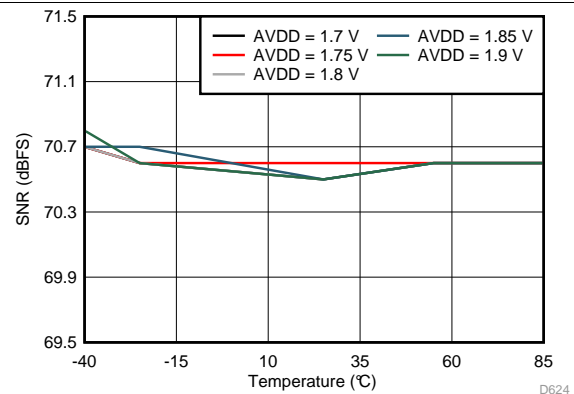


Figure 54. Signal-to-Noise Ratio vs AVDD Supply and Temperature (30 MHz)

Typical Characteristics: ADC3422 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled, unless otherwise noted.

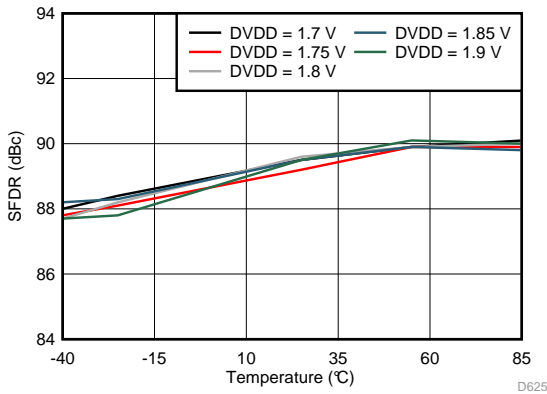


Figure 55. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (30 MHz)

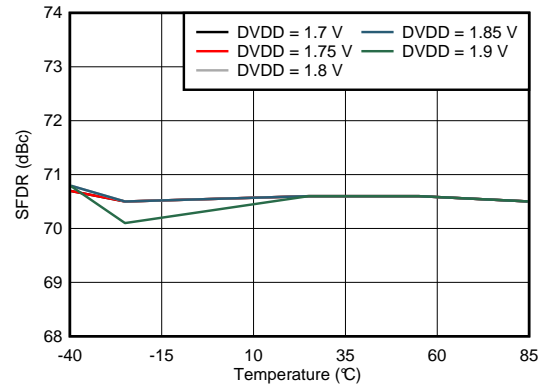


Figure 56. Signal-to-Noise Ratio vs DVDD Supply and Temperature (30 MHz)

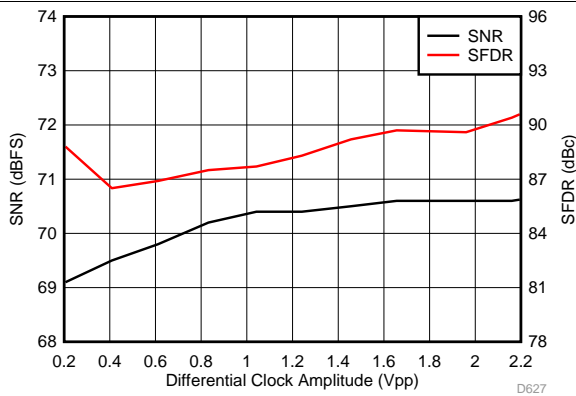


Figure 57. Performance vs Clock Amplitude (40 MHz)

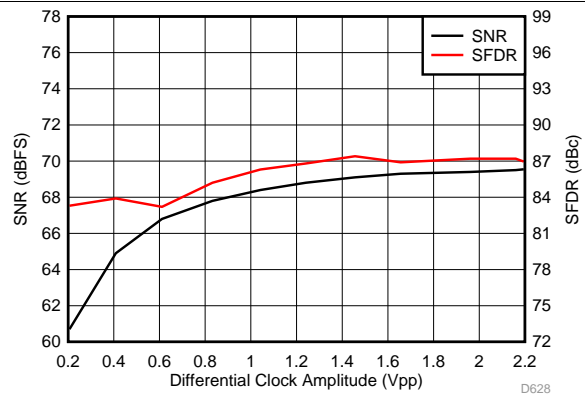


Figure 58. Performance vs Clock Amplitude (150 MHz)

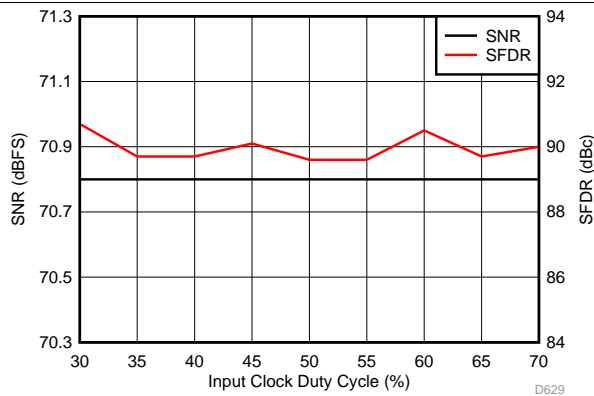


Figure 59. Performance vs Clock Duty Cycle (30 MHz)

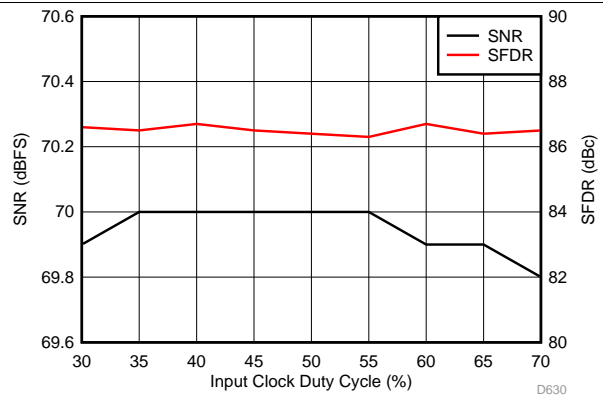
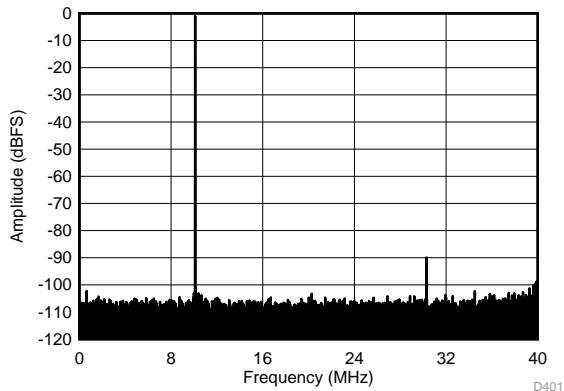


Figure 60. Performance vs Clock Duty Cycle (150 MHz)

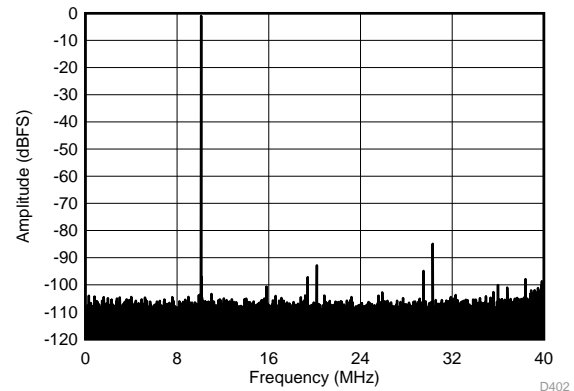
### 7.17 Typical Characteristics: ADC3423

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled, unless otherwise noted.



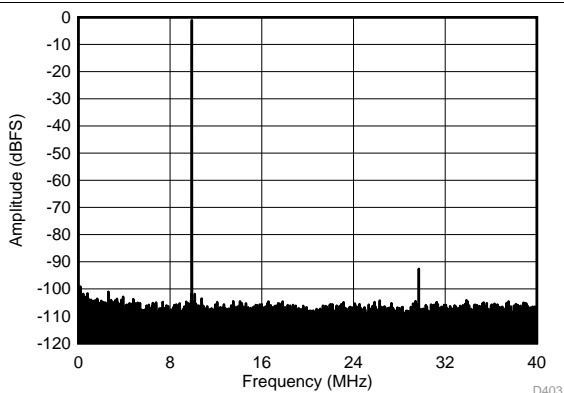
SFDR = 89 dBc, SNR = 70.7 dBFS, SINAD = 70.6 dBFS, THD = 89 dBc, HD2 = 108 dBc, HD3 = 89 dBc

Figure 61. FFT for 10-MHz Input Signal (Dither On)



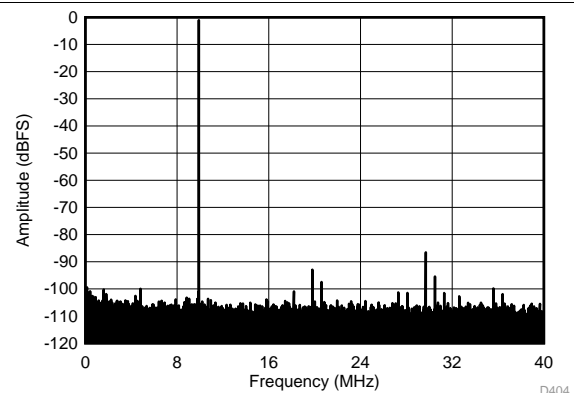
SFDR = 84 dBc, SNR = 70.9 dBFS, SINAD = 70.7 dBFS, THD = 83 dBc, HD2 = 92 dBc, HD3 = 84 dBc

Figure 62. FFT for 10-MHz Input Signal (Dither Off)



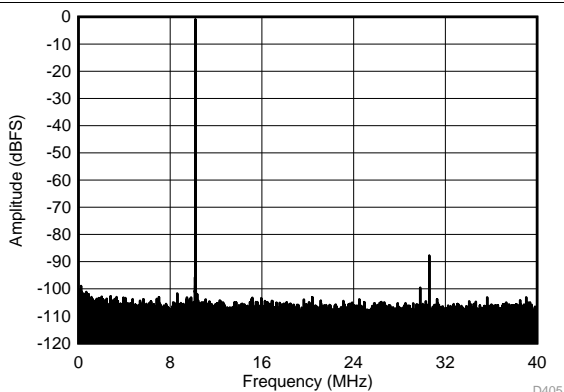
SFDR = 92 dBc, SNR = 70.5 dBFS, SINAD = 70.4 dBFS, THD = 91 dBc, HD2 = 112 dBc, HD3 = 92 dBc

Figure 63. FFT for 70-MHz Input Signal (Dither On)



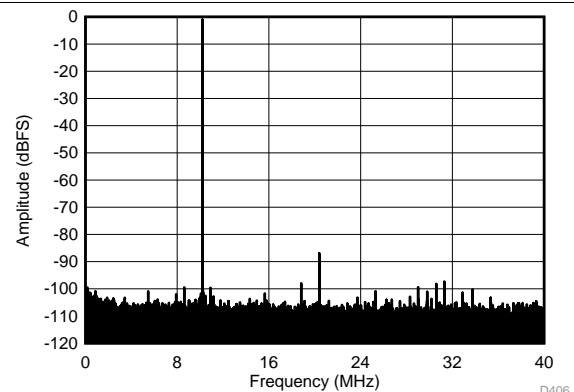
SFDR = 86 dBc, SNR = 70.7 dBFS, SINAD = 70.5 dBFS, THD = 84 dBc, HD2 = 92 dBc, HD3 = 86 dBc

Figure 64. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 87 dBc, SNR = 70.2 dBFS, SINAD = 70.1 dBFS, THD = 93 dBc, HD2 = 102 dBc, HD3 = 87 dBc

Figure 65. FFT for 170-MHz Input Signal (Dither On)

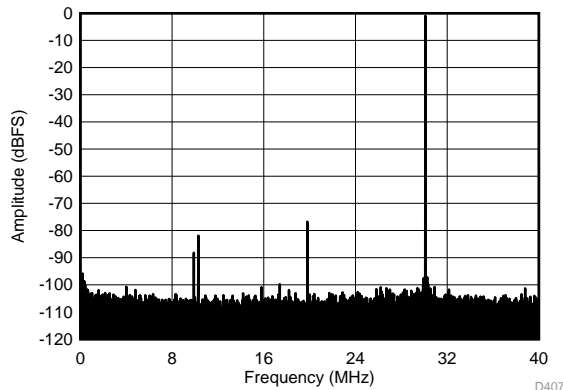


SFDR = 86 dBc, SNR = 70.5 dBFS, SINAD = 70.4 dBFS, THD = 88 dBc, HD2 = 86 dBc, HD3 = 97 dBc

Figure 66. FFT for 170-MHz Input Signal (Dither Off)

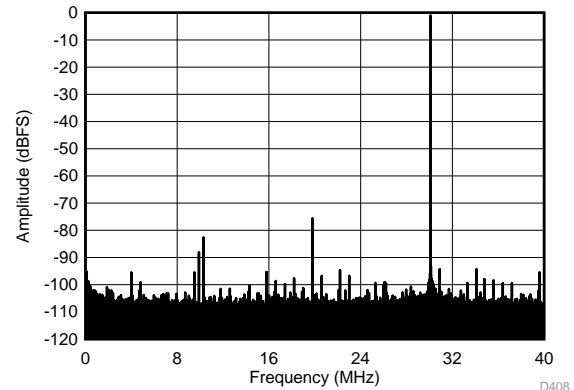
**Typical Characteristics: ADC3423 (continued)**

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.



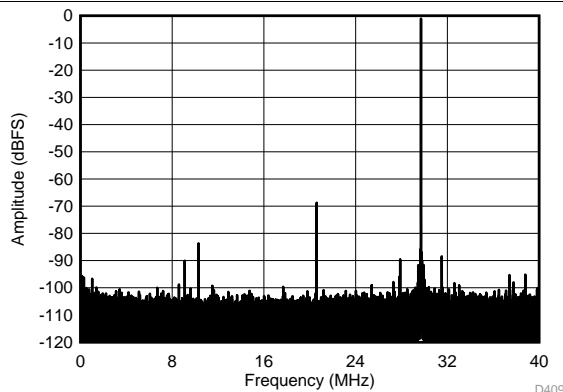
SFDR = 76 dBc, SNR = 69.2 dBFS, SINAD = 68.3 dBFS, THD = 75 dBc, HD2 = 76 dBc, HD3 = 81 dBc

**Figure 67. FFT for 270-MHz Input Signal (Dither On)**



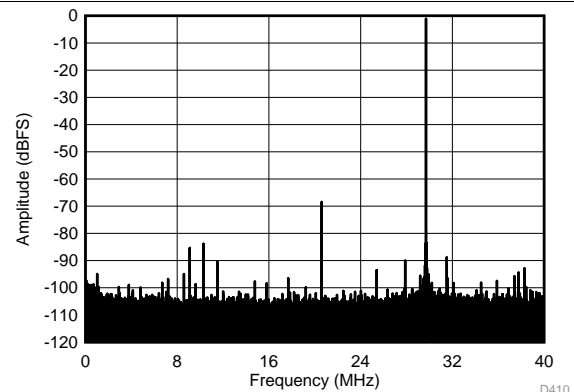
SFDR = 75 dBc, SNR = 69.5 dBFS, SINAD = 68.4 dBFS, THD = 75 dBc, HD2 = 75 dBc, HD3 = 82 dBc

**Figure 68. FFT for 270-MHz Input Signal (Dither Off)**



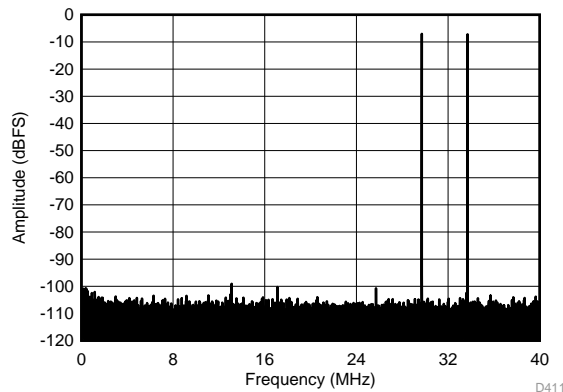
SFDR = 68 dBc, SNR = 67.5 dBFS, SINAD = 67.1 dBFS, THD = 77 dBc, HD2 = 68 dBc, HD3 = 89 dBc

**Figure 69. FFT for 450-MHz Input Signal (Dither On)**



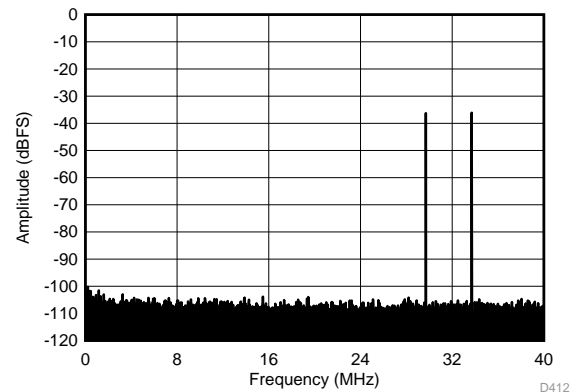
SFDR = 67 dBc, SNR = 67.7 dBFS, SINAD = 67.3 dBFS, THD = 77 dBc, HD2 = 67 dBc, HD3 = 84 dBc

**Figure 70. FFT for 450-MHz Input Signal (Dither Off)**



$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 98 dBFS, each tone at -7 dBFS

**Figure 71. FFT for Two-Tone Input Signal (-7 dBFS at 46 MHz and 50 MHz)**

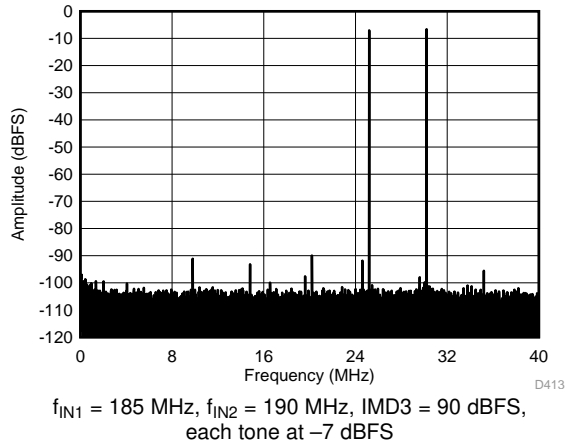


$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 105 dBFS, each tone at -36 dBFS

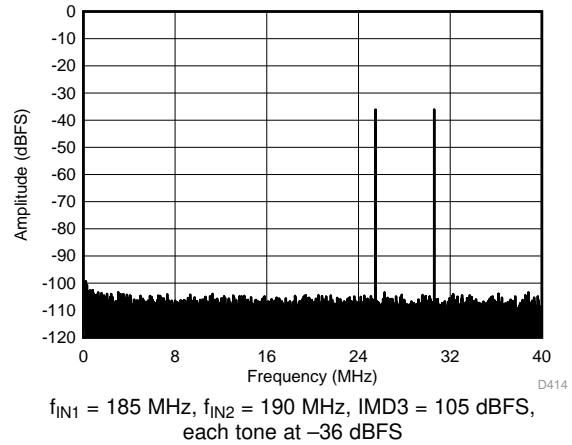
**Figure 72. FFT for Two-Tone Input Signal (-36 dBFS at 46 MHz and 50 MHz)**

### Typical Characteristics: ADC3423 (continued)

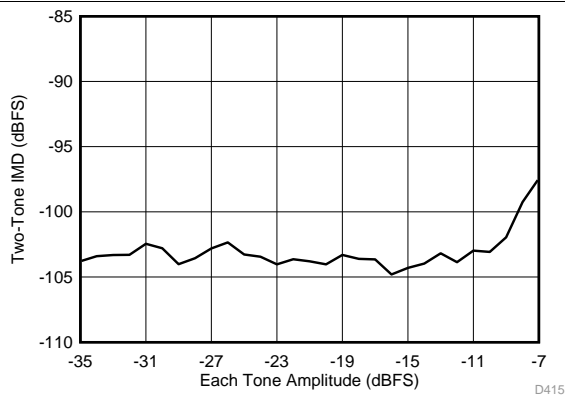
Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{ dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.



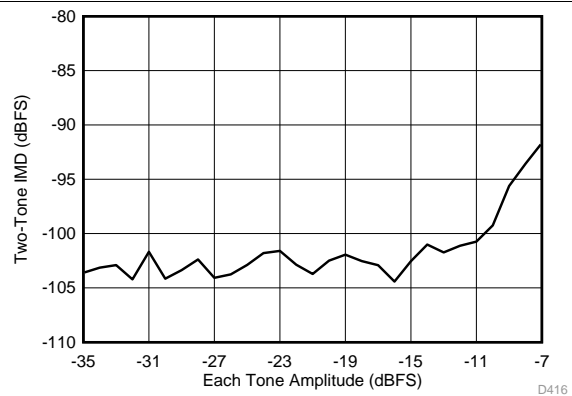
**Figure 73. FFT FOR Two-Tone Input Signal (-7 dBFS at 185 MHz and 190 MHz)**



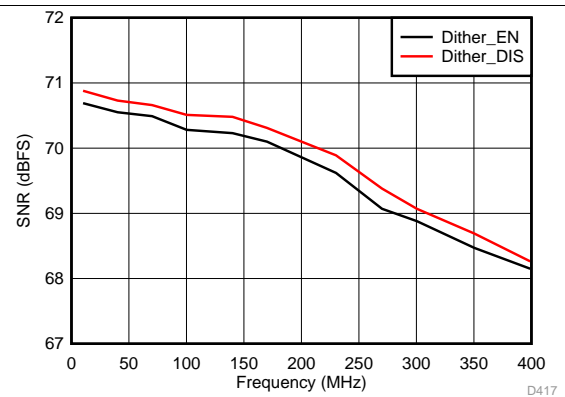
**Figure 74. FFT FOR Two-Tone Input Signal (-36 dBFS at 185 MHz and 190 MHz)**



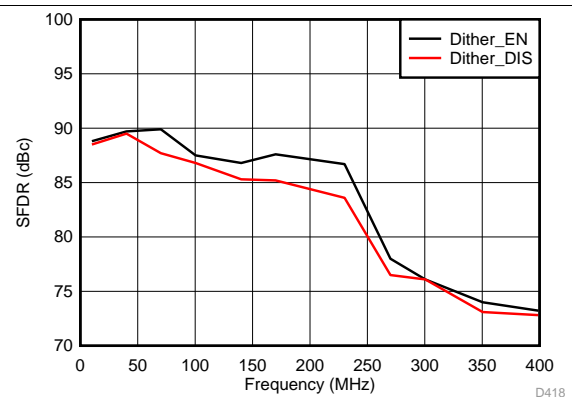
**Figure 75. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)**



**Figure 76. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)**



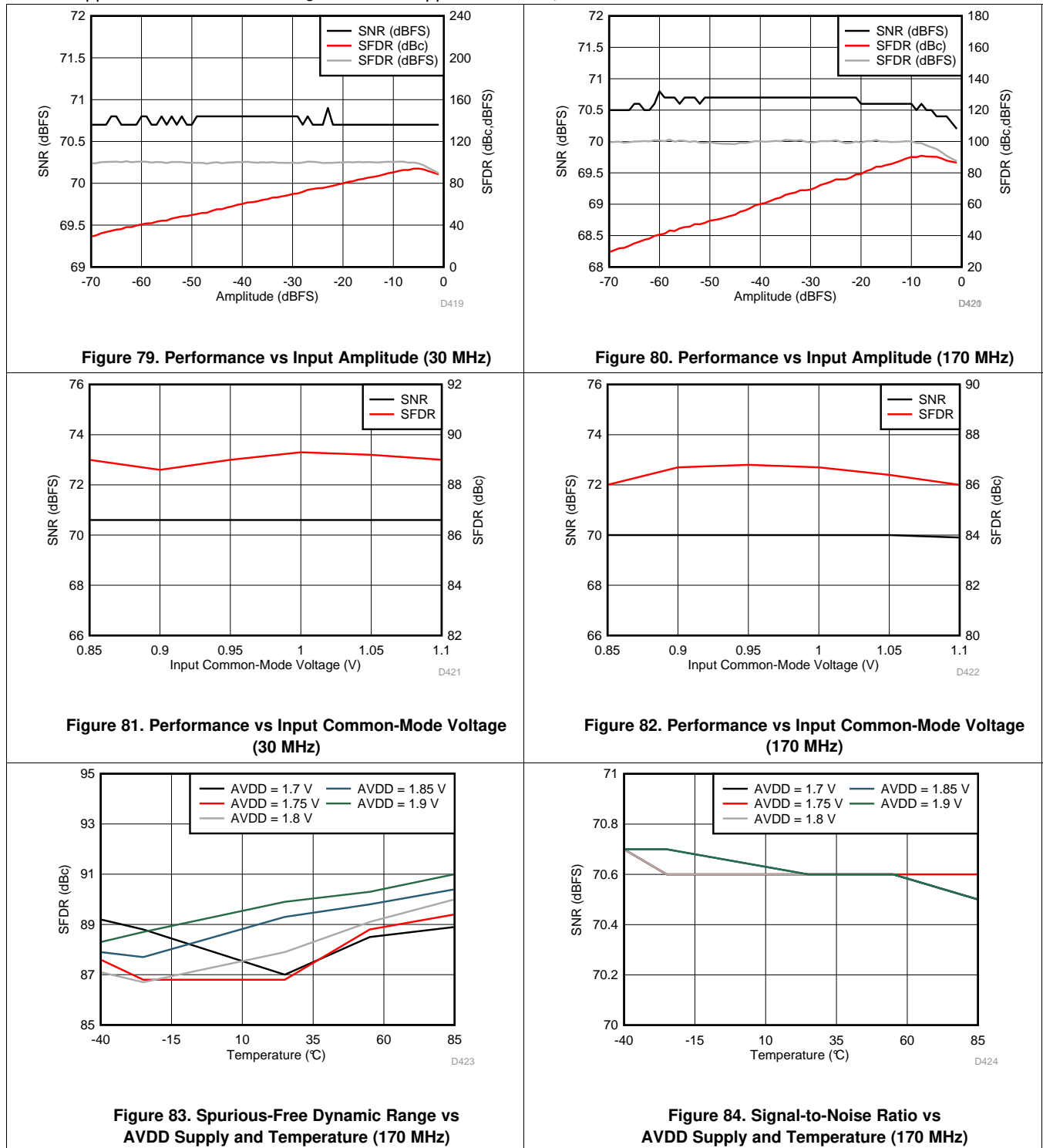
**Figure 77. Signal-to-Noise Ratio vs Input Frequency**



**Figure 78. Spurious-Free Dynamic Range vs Input Frequency**

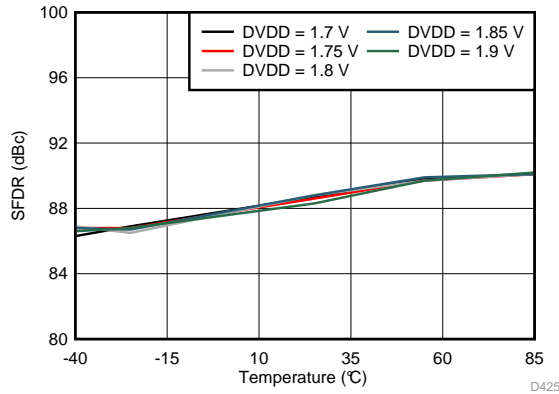
Typical Characteristics: ADC3423 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.

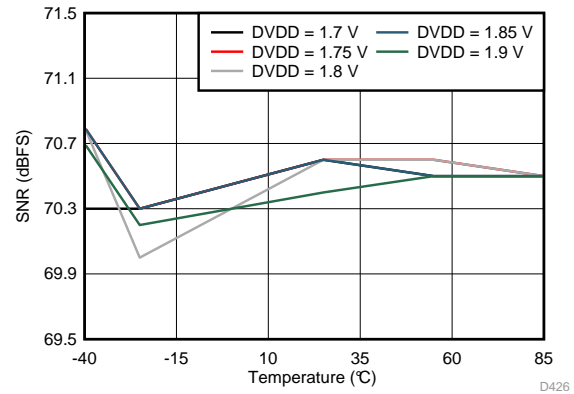


**Typical Characteristics: ADC3423 (continued)**

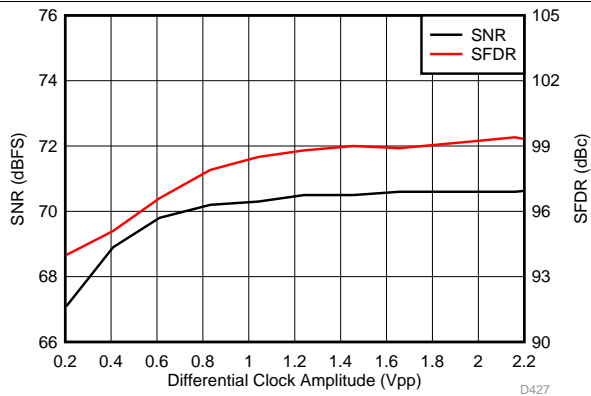
Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, 2- $V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.



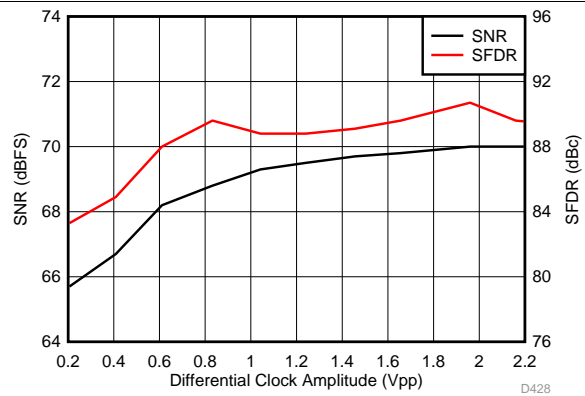
**Figure 85. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (170 MHz)**



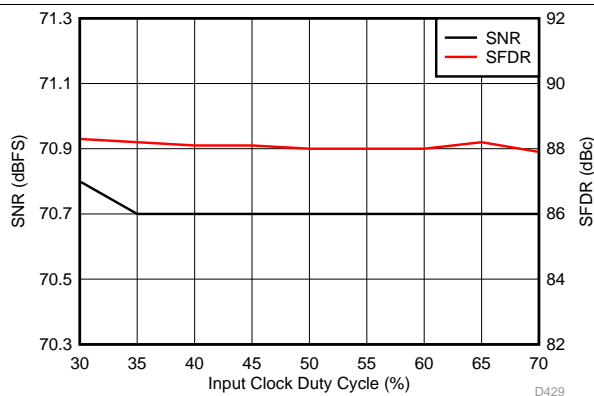
**Figure 86. Signal-to-Noise Ratio vs DVDD Supply and Temperature (170 MHz)**



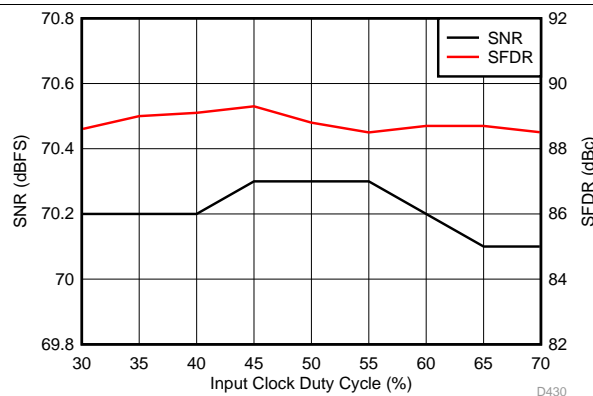
**Figure 87. Performance vs Clock Amplitude (40 MHz)**



**Figure 88. Performance vs Clock Amplitude (150 MHz)**



**Figure 89. Performance vs Clock Duty Cycle (30 MHz)**

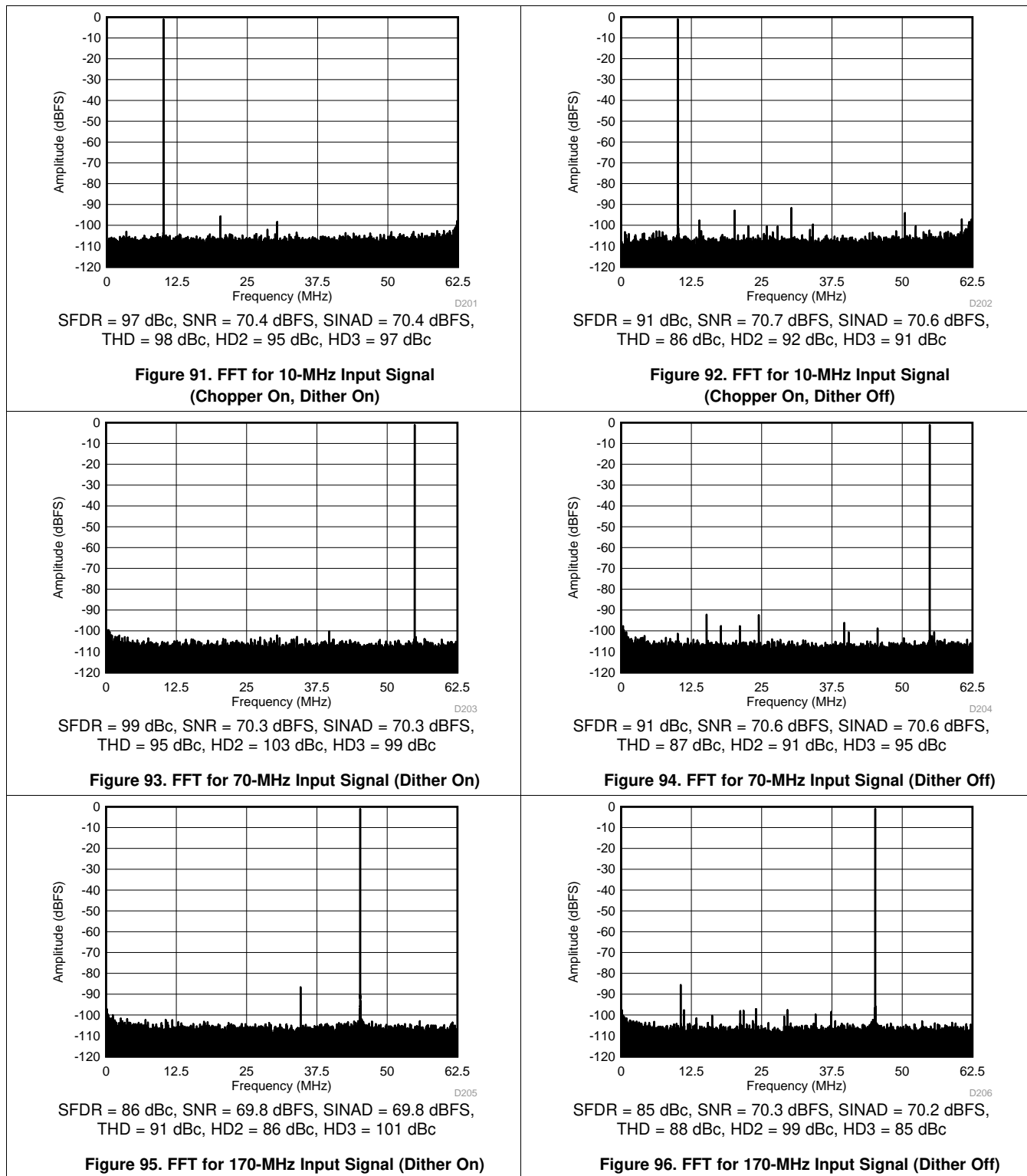


**Figure 90. Performance vs Clock Duty Cycle (150 MHz)**



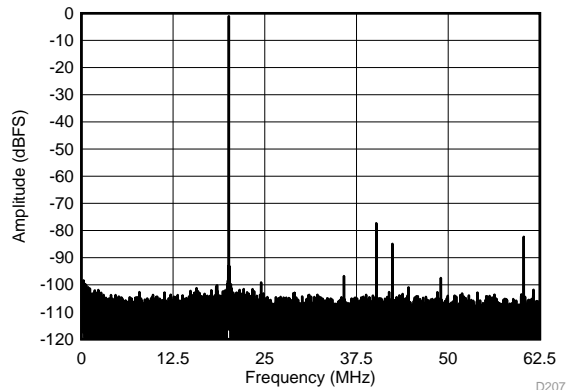
### 7.18 Typical Characteristics: ADC3424

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AVDD = 1.8\text{ V}$ ,  $DVDD = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled, unless otherwise noted.



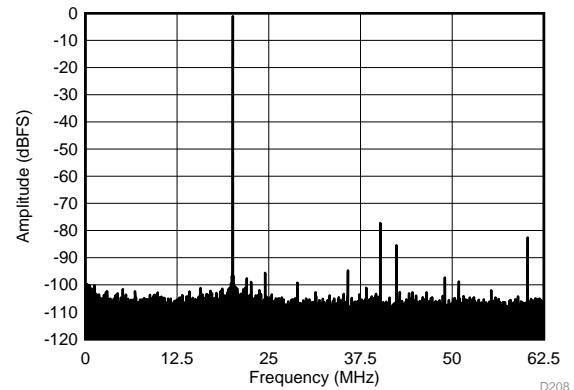
### Typical Characteristics: ADC3424 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{ dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.



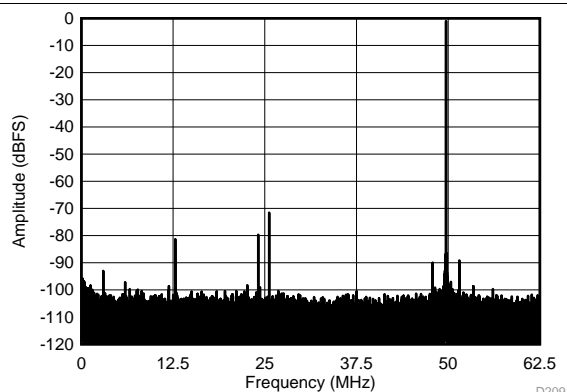
SFDR = 76 dBc, SNR = 68.94 dBFS, SINAD = 68.4 dBFS, THD = 75 dBc, HD2 = 76 dBc, HD3 = 81 dBc

Figure 97. FFT for 270-MHz Input Signal (Dither On)



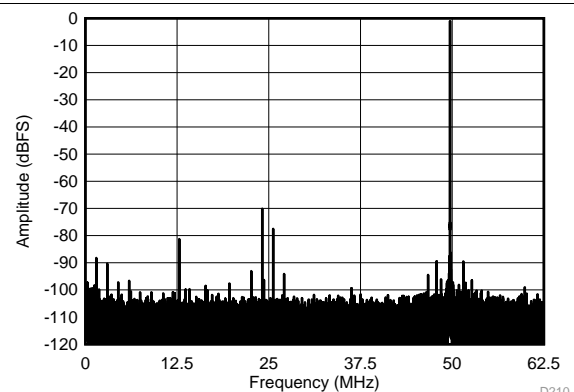
SFDR = 76 dBc, SNR = 69.3 dBFS, SINAD = 68.6 dBFS, THD = 75 dBc, HD2 = 76 dBc, HD3 = 82 dBc

Figure 98. FFT for 270-MHz Input Signal (Dither Off)



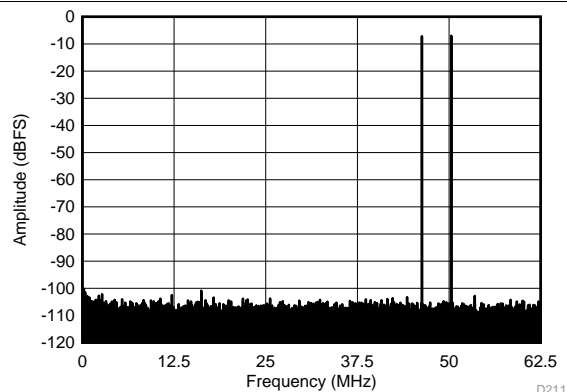
SFDR = 71 dBc, SNR = 67.2 dBFS, SINAD = 66.5 dBFS, THD = 74 dBc, HD2 = 71 dBc, HD3 = 79 dBc

Figure 99. FFT for 450-MHz Input Signal (Dither On)



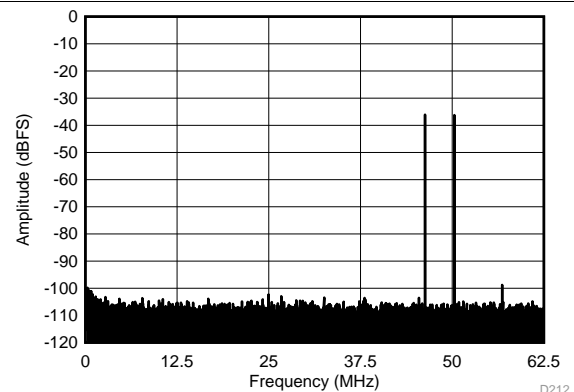
SFDR = 69 dBc, SNR = 67.8 dBFS, SINAD = 66.8 dBFS, THD = 73 dBc, HD2 = 77 dBc, HD3 = 69 dBc

Figure 100. FFT for 450-MHz Input Signal (Dither Off)



$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 100 dBFS, each tone at  $-7\text{ dBFS}$

Figure 101. FFT for Two-Tone Input Signal ( $-7\text{ dBFS}$  at 46 MHz and 50 MHz)

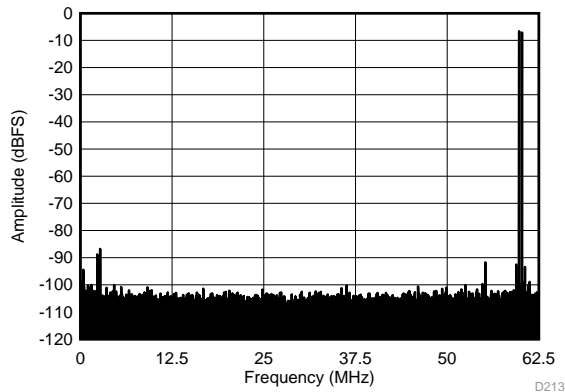


$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 99 dBFS, each tone at  $-36\text{ dBFS}$

Figure 102. FFT for Two-Tone Input Signal ( $-36\text{ dBFS}$  at 46 MHz and 50 MHz)

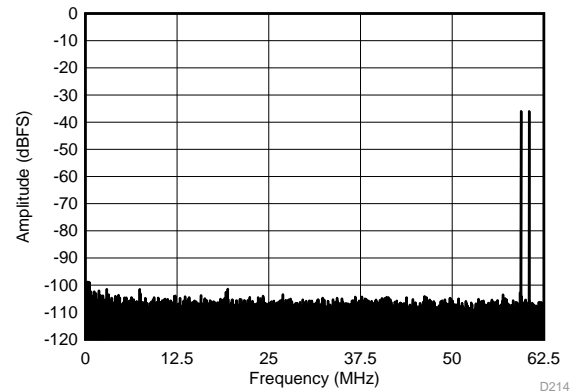
**Typical Characteristics: ADC3424 (continued)**

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{ dBFS}$  differential input,  $2 \cdot V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled, unless otherwise noted.



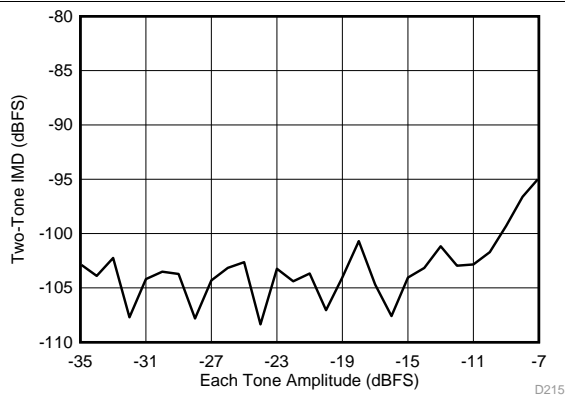
$f_{IN1} = 185\text{ MHz}$ ,  $f_{IN2} = 190\text{ MHz}$ ,  $IMD3 = 86\text{ dBFS}$ , each tone at  $-7\text{ dBFS}$

**Figure 103. FFT for Two-Tone Input Signal (-7 dBFS at 185 MHz and 190 MHz)**

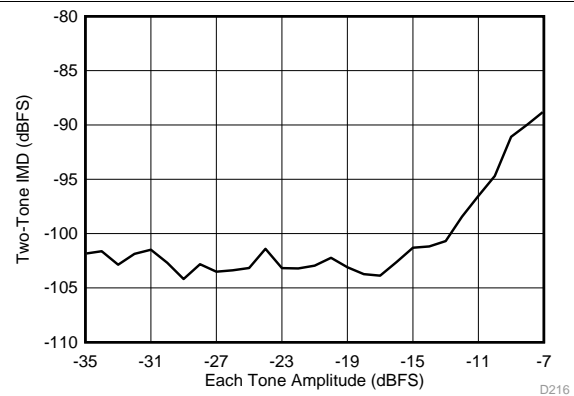


$f_{IN1} = 185\text{ MHz}$ ,  $f_{IN2} = 190\text{ MHz}$ ,  $IMD3 = 102\text{ dBFS}$ , each tone at  $-36\text{ dBFS}$

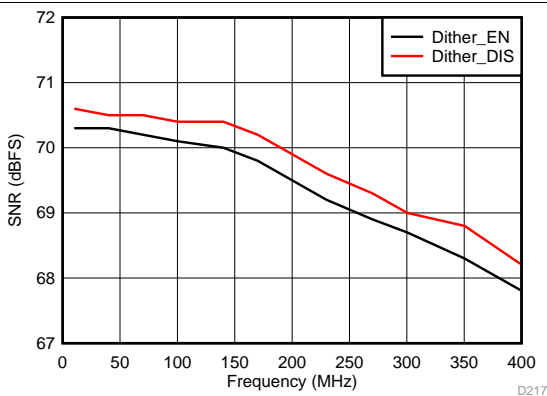
**Figure 104. FFT for Two-Tone Input Signal (-36 dBFS at 185 MHz and 190 MHz)**



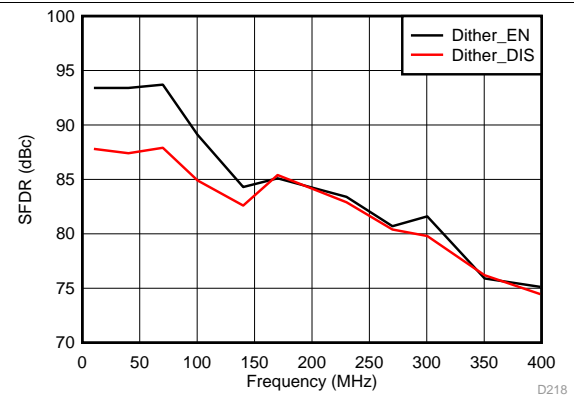
**Figure 105. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)**



**Figure 106. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)**



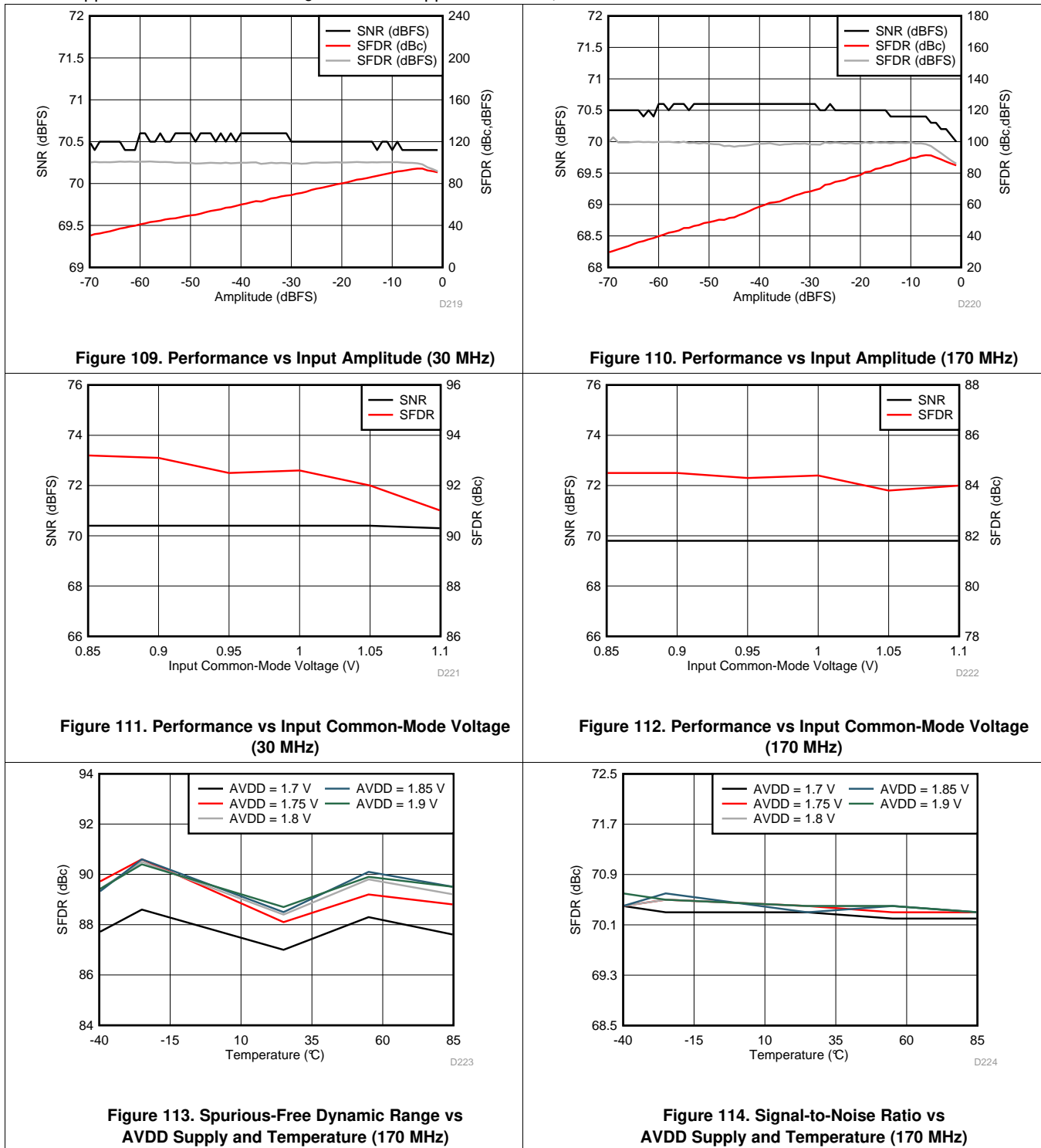
**Figure 107. Signal-to-Noise Ratio vs Input Frequency**



**Figure 108. Spurious-Free Dynamic Range vs Input Frequency**

**Typical Characteristics: ADC3424 (continued)**

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AVDD = 1.8\text{ V}$ ,  $DVDD = 1.8\text{ V}$ ,  $-1\text{ dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.



Typical Characteristics: ADC3424 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{ dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.

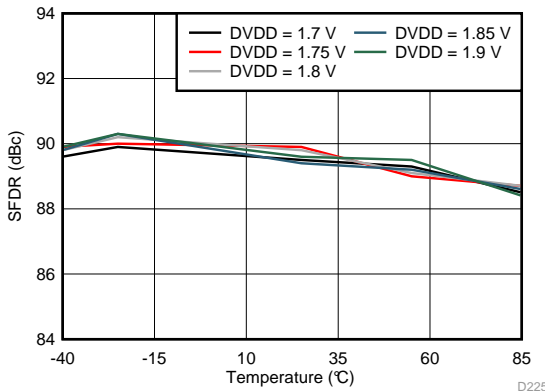


Figure 115. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (170 MHz)

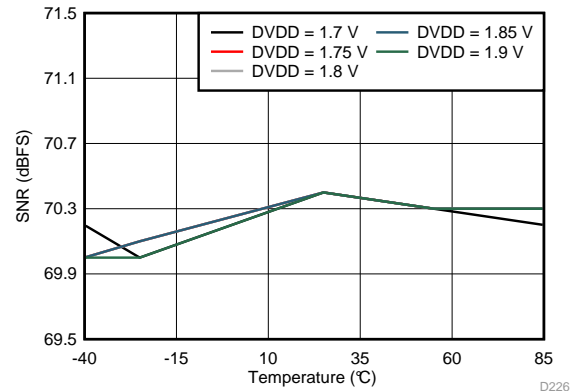


Figure 116. Signal-to-Noise Ratio vs DVDD Supply and Temperature (170 MHz)

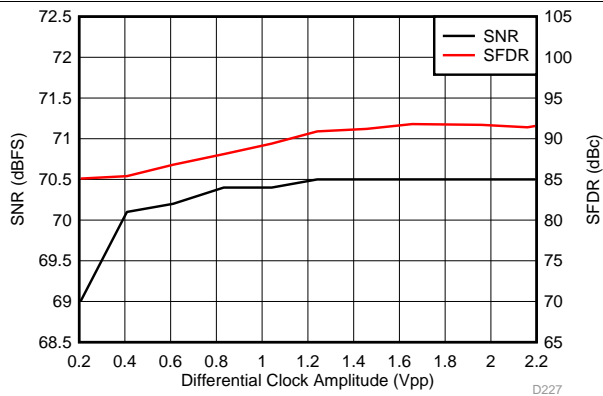


Figure 117. Performance vs Clock Amplitude (40 MHz)

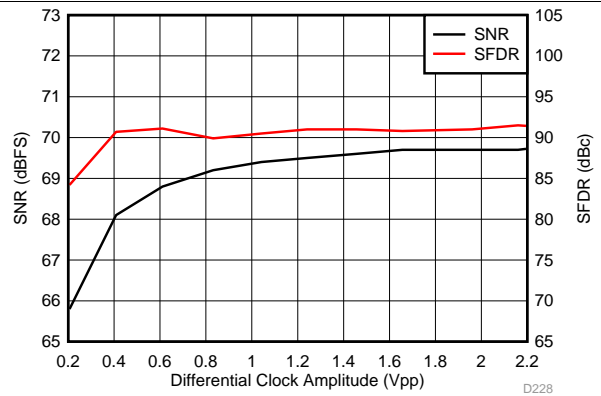


Figure 118. Performance vs Clock Amplitude (150 MHz)

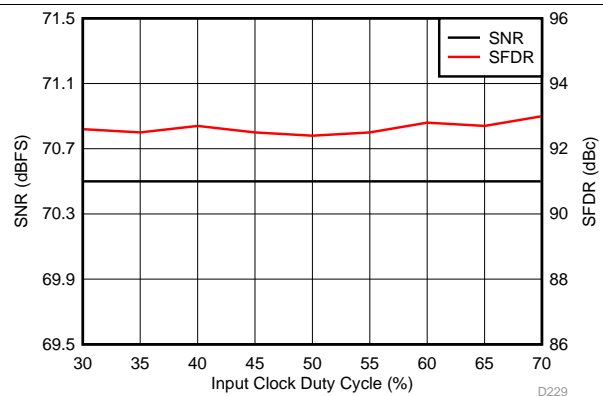


Figure 119. Performance vs Clock Duty Cycle (30 MHz)

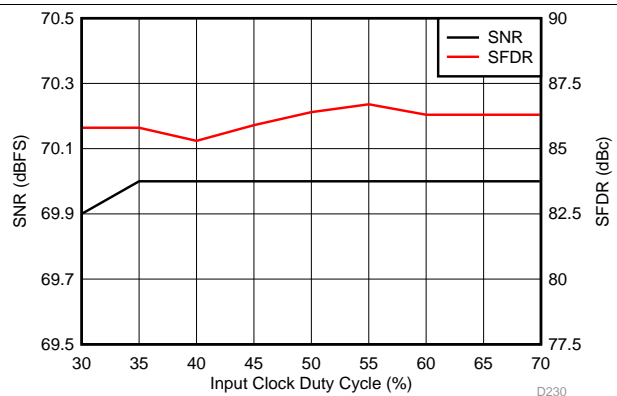


Figure 120. Performance vs Clock Duty Cycle (150 MHz)

### 7.19 Typical Characteristics: Common

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_s / 2$  when chopper is enabled, unless otherwise noted.

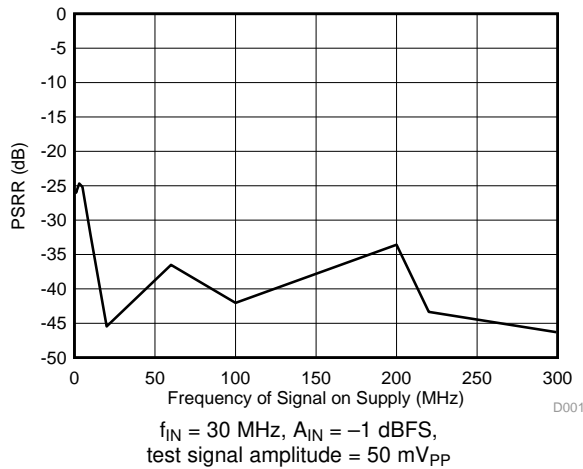


Figure 121. Power-Supply Rejection Ratio vs Test Signal Frequency

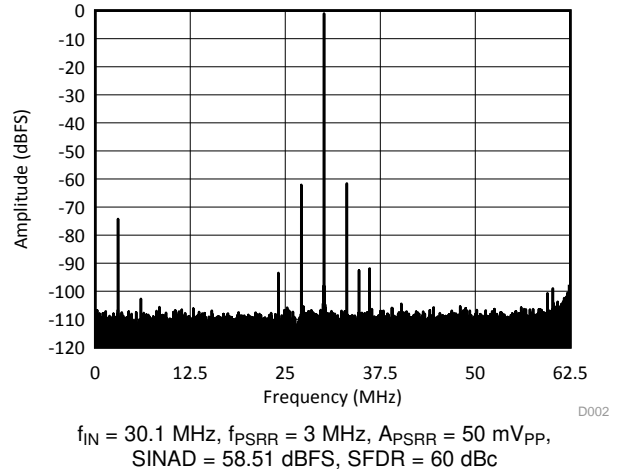


Figure 122. Power-Supply Rejection Ratio Spectrum

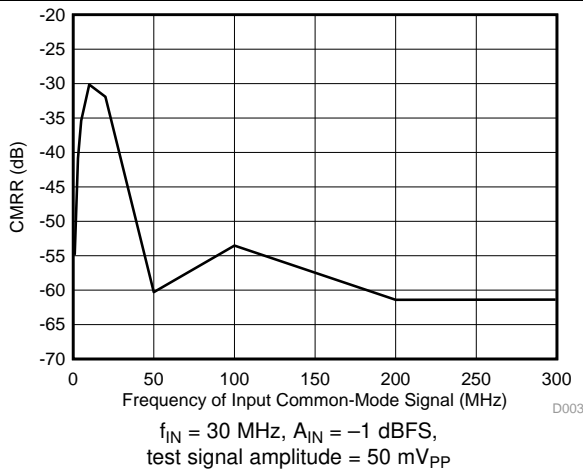


Figure 123. Common-Mode Rejection Ratio vs Test Signal Frequency

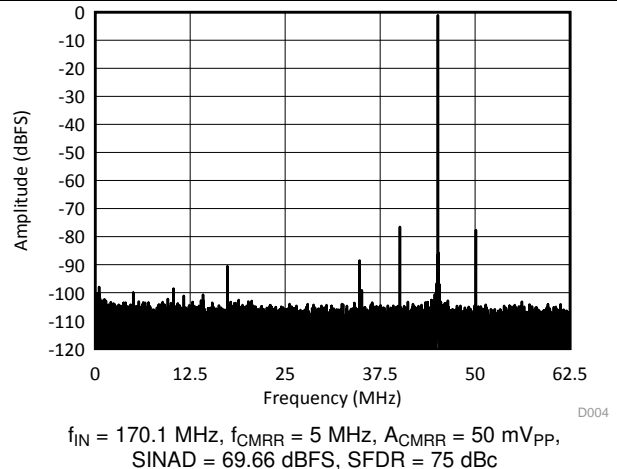


Figure 124. Common-Mode Rejection Ratio Spectrum

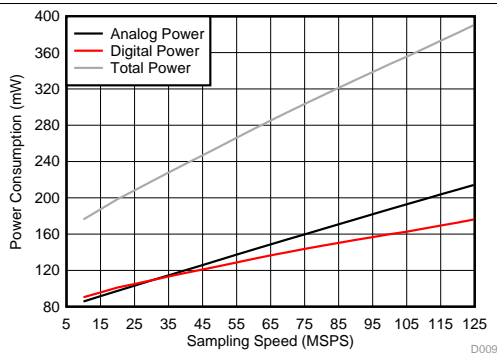


Figure 125. Power vs Sampling Frequency (Two-Wire Mode)

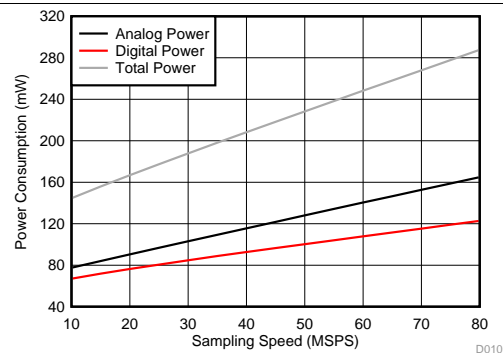
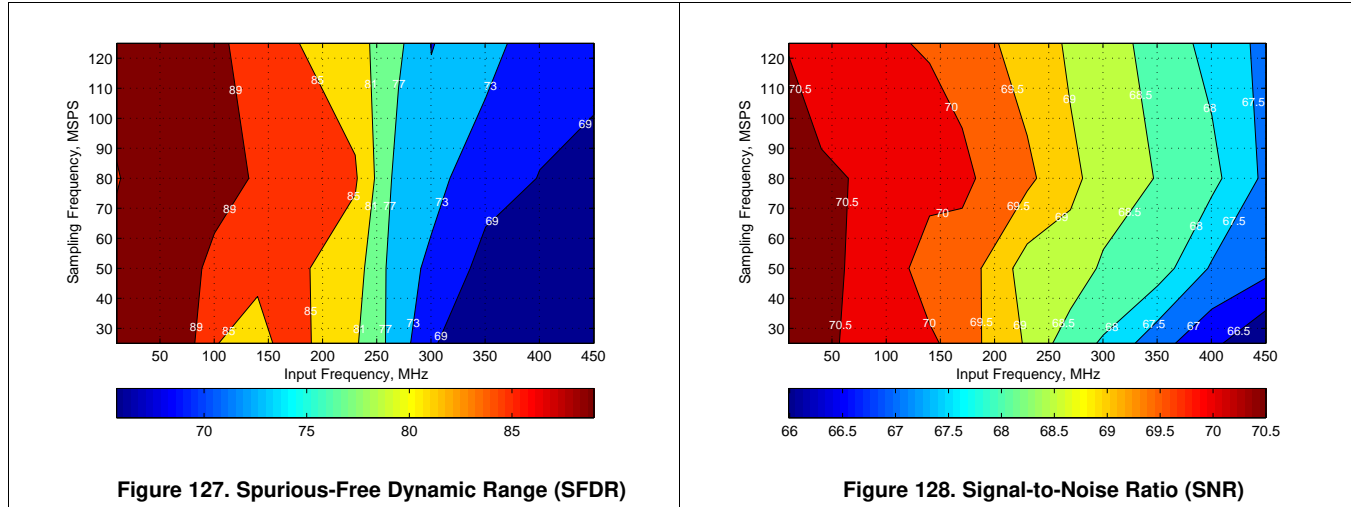


Figure 126. Power vs Sampling Frequency (One-Wire Mode)

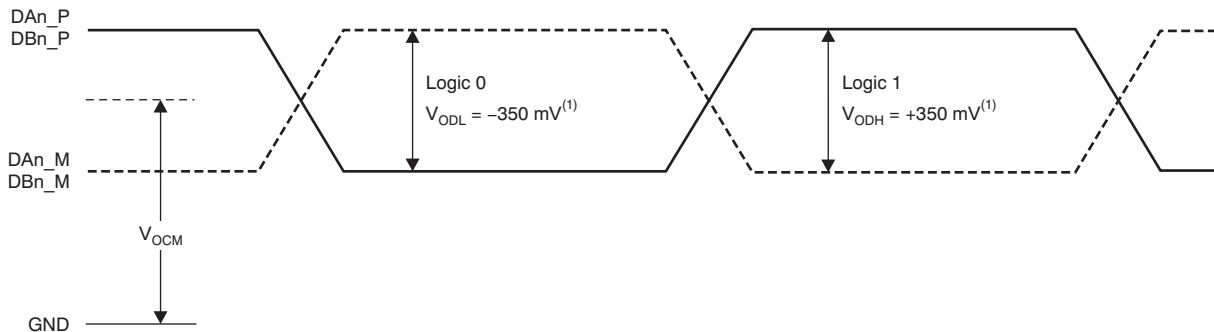
## 7.20 Typical Characteristics: Contour

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when is chopper enabled, unless otherwise noted.



## 8 Parameter Measurement Information

### 8.1 Timing Diagrams



(1) With an external 100- $\Omega$  termination.

**Figure 129. Serial LVDS Output Voltage Levels**

Timing Diagrams (continued)

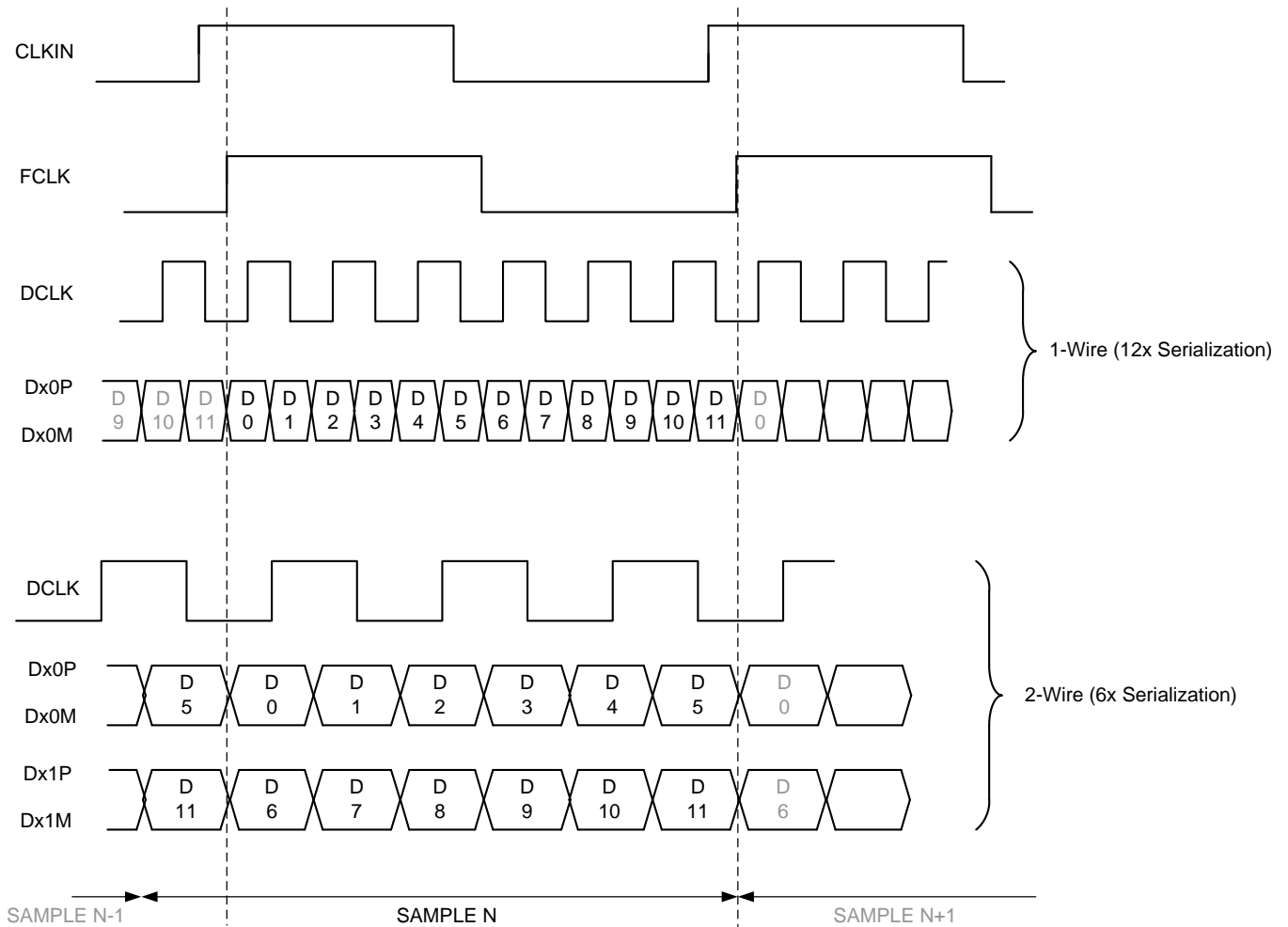


Figure 130. Output Timing Diagram

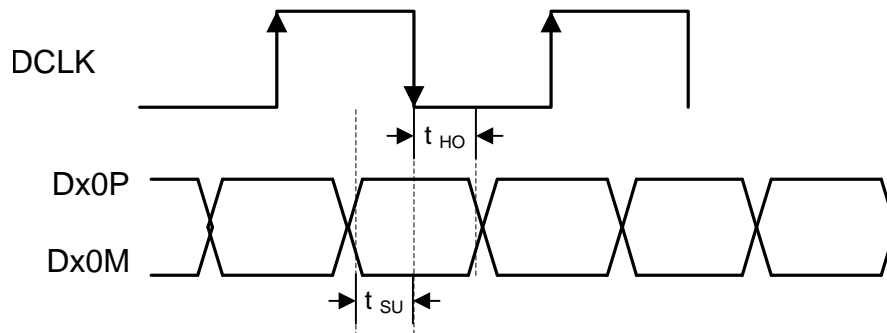


Figure 131. Setup and Hold Time

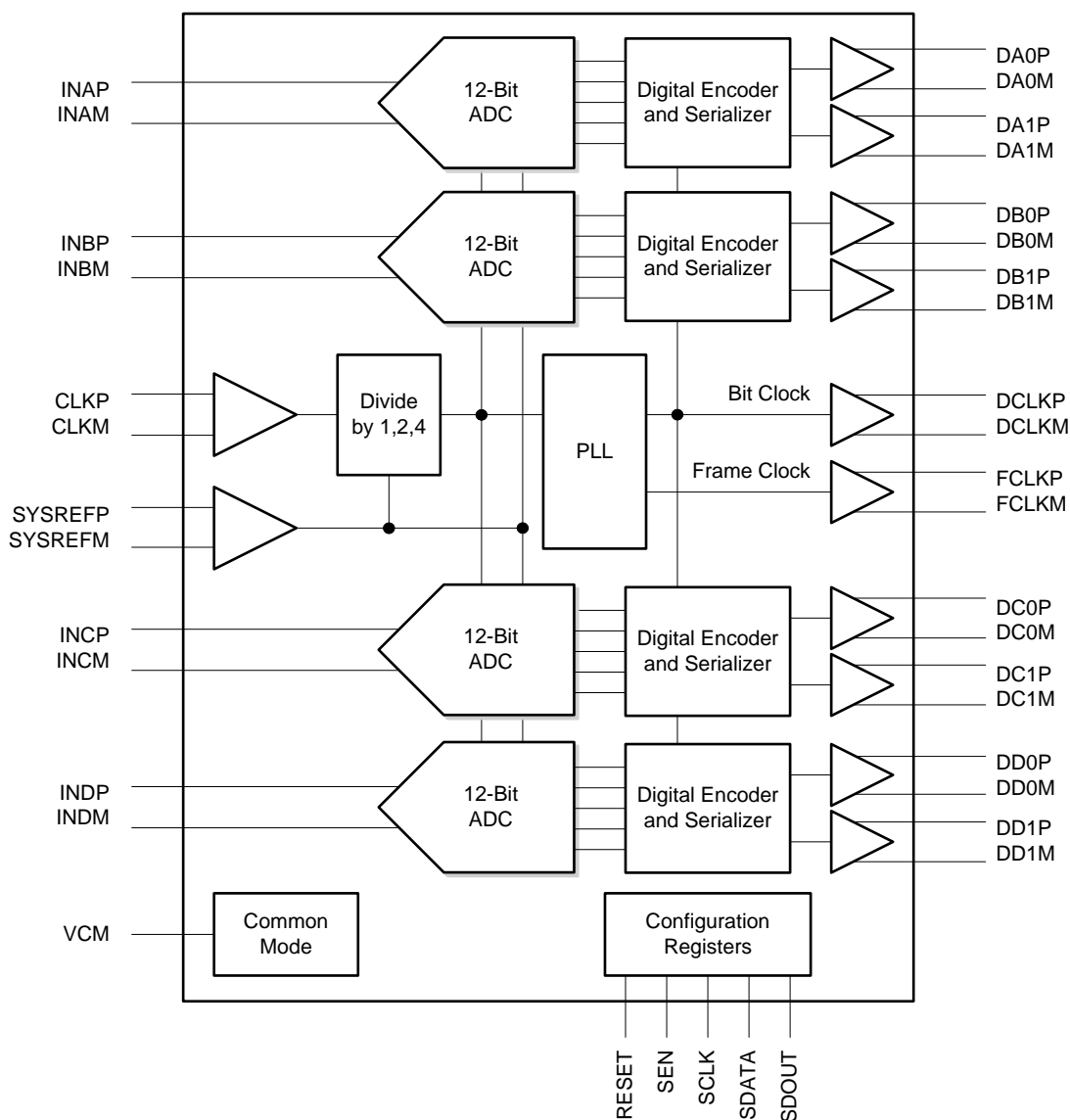


## 9 Detailed Description

### 9.1 Overview

The ADC342x are a high-linearity, ultra-low power, quad-channel, 12-bit, 25-MSPS to 125-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design and the SYSREF input enables complete system synchronization. The ADC342x family supports a serial low-voltage differential signaling (LVDS) interface in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 12-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

### 9.2 Functional Block Diagram



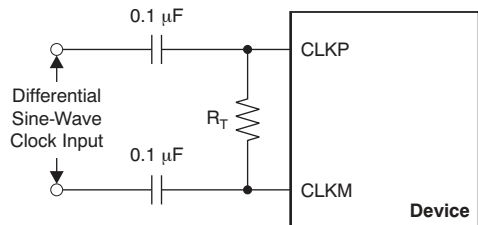
## 9.3 Feature Description

### 9.3.1 Analog Inputs

The ADC342x analog signal inputs are designed to be driven differentially. Each input pin (INP, INM) must swing symmetrically between  $(V_{CM} + 0.5\text{ V})$  and  $(V_{CM} - 0.5\text{ V})$ , resulting in a  $2\text{-}V_{PP}$  (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 540 MHz (50- $\Omega$  source driving 50- $\Omega$  termination between INP and INM).

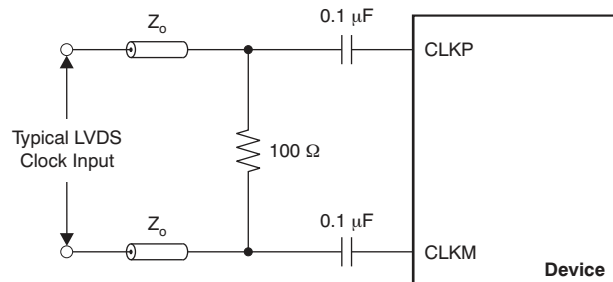
### 9.3.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95 V using internal 5-k $\Omega$  resistors. The self-bias clock inputs of the ADC342x can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 132, Figure 133, and Figure 134. See Figure 135 for details regarding the internal clock buffer.

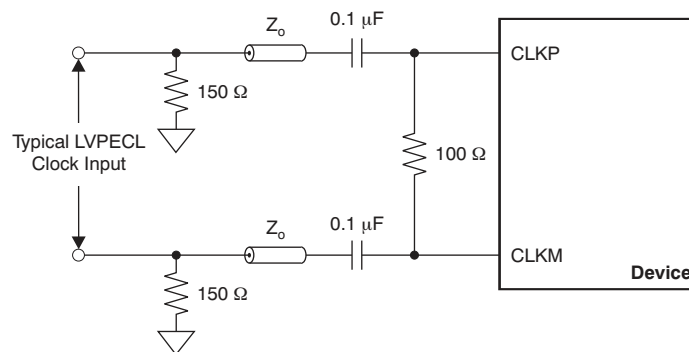


NOTE:  $R_T$  = termination resistor, if necessary.

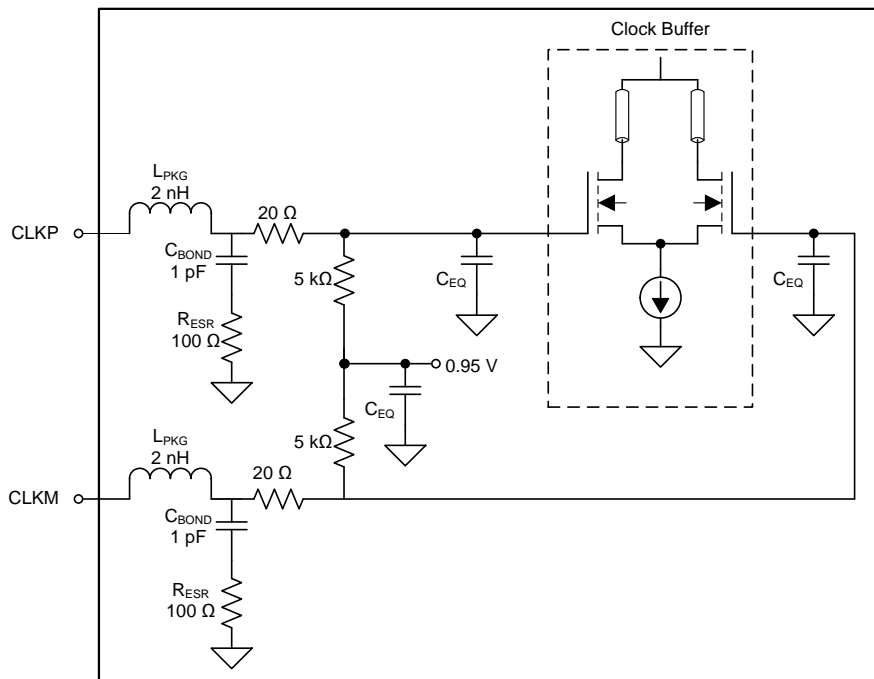
**Figure 132. Differential Sine-Wave Clock Driving Circuit**



**Figure 133. LVDS Clock Driving Circuit**



**Figure 134. LVPECL Clock Driving Circuit**



NOTE: C<sub>EQ</sub> is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 135. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-μF capacitor, as shown in Figure 136. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

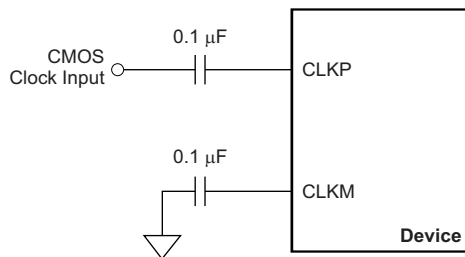


Figure 136. Single-Ended Clock Driving Circuit

### 9.3.2.1 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors, as shown in Equation 1. Quantization noise (typically 74 dB for a 12-bit ADC) and thermal noise limit SNR at low input frequencies, and the clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

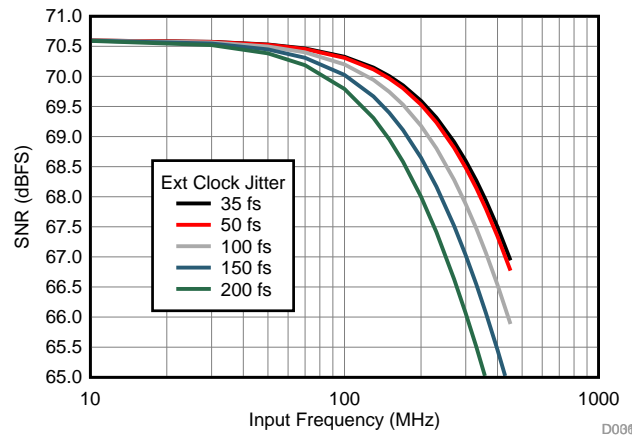
The SNR limitation resulting from sample clock jitter can be calculated with Equation 2.

$$SNR_{Jitter}[dBc] = -20 \cdot \log(2\pi \cdot f_{in} \cdot T_{Jitter}) \quad (2)$$

The total clock jitter ( $T_{Jitter}$ ) has two components: the internal aperture jitter (130 fs for the device) which is set by the noise of the clock input buffer and the external clock.  $T_{Jitter}$  can be calculated with [Equation 3](#).

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (3)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input; a faster clock slew rate improves the ADC aperture jitter. The devices have a typical thermal noise of 72.7 dBFS and internal aperture jitter of 130 fs. The SNR, depending on the amount of external jitter for different input frequencies, is shown in [Figure 137](#).



**Figure 137. SNR vs Frequency for Different Clock Jitter**

### 9.3.3 Digital Output Interface

The devices offer two different output format options, thus making interfacing to a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC) easy. Each option can be easily programmed using the serial interface, as shown in [Table 3](#). The output interface options are:

- One-wire, 1x frame clock, 12x serialization with the DDR bit clock and
- Two-wire, 1x frame clock, 6x serialization with the DDR bit clock.

**Table 3. Interface Rates**

INTERFACE OPTIONS	SERIALIZATION	RECOMMENDED SAMPLING FREQUENCY (MSPS)		BIT CLOCK FREQUENCY (MHz)	FRAME CLOCK FREQUENCY (MHz)	SERIAL DATA RATE PER WIRE (Mbps)
		MINIMUM	MAXIMUM			
One-wire	12x	15		90	15	180
			80	480	80	960
Two-wire (Default after Reset)	6x	20 <sup>(1)</sup>		60	20	120
			125	375	125	750

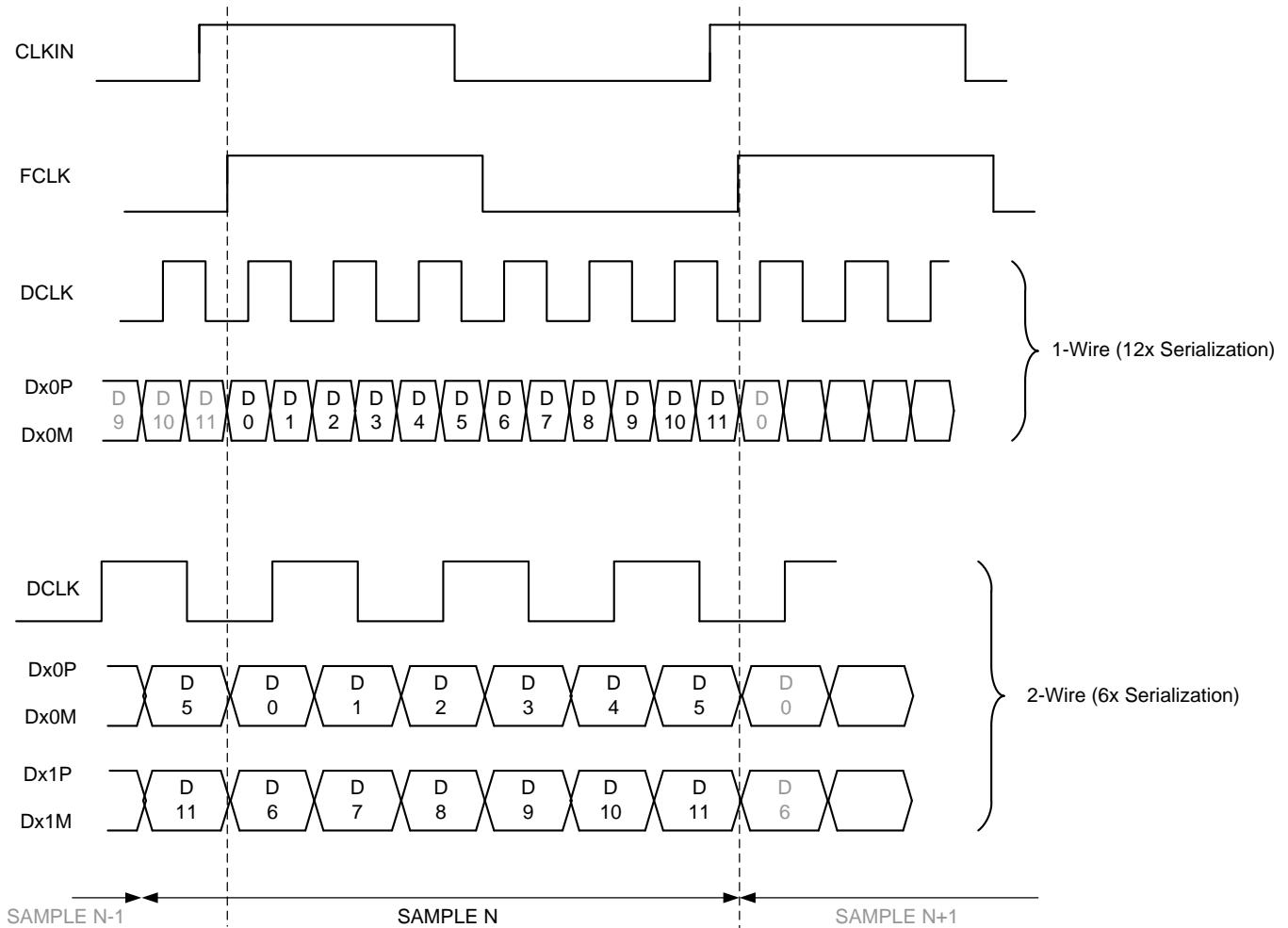
(1) Use the LOW SPEED ENABLE register bits for low speed operation; see [Table 21](#).

#### 9.3.3.1 One-Wire Interface: 12x Serialization

In this interface option, the device outputs the data of each ADC serially on a single LVDS pair (one-wire). The data are available at the rising and falling edges of the bit clock (DDR bit clock). The ADC outputs a new word at the rising edge of every frame clock, starting with the LSB. The data rate is 12x sample frequency (12x serialization).

**9.3.3.2 Two-Wire Interface: 6x Serialization**

The two-wire interface is recommended for sampling frequencies above 65 MSPS. The output data rate is 6x sample frequency because six data bits are output every clock cycle on each differential pair. Each ADC sample is sent over the two wires with the six MSBs on Dx1P, Dx1M and the six LSBs on Dx0P, Dx0M, as shown in Figure 138.



**Figure 138. Output Timing Diagram**

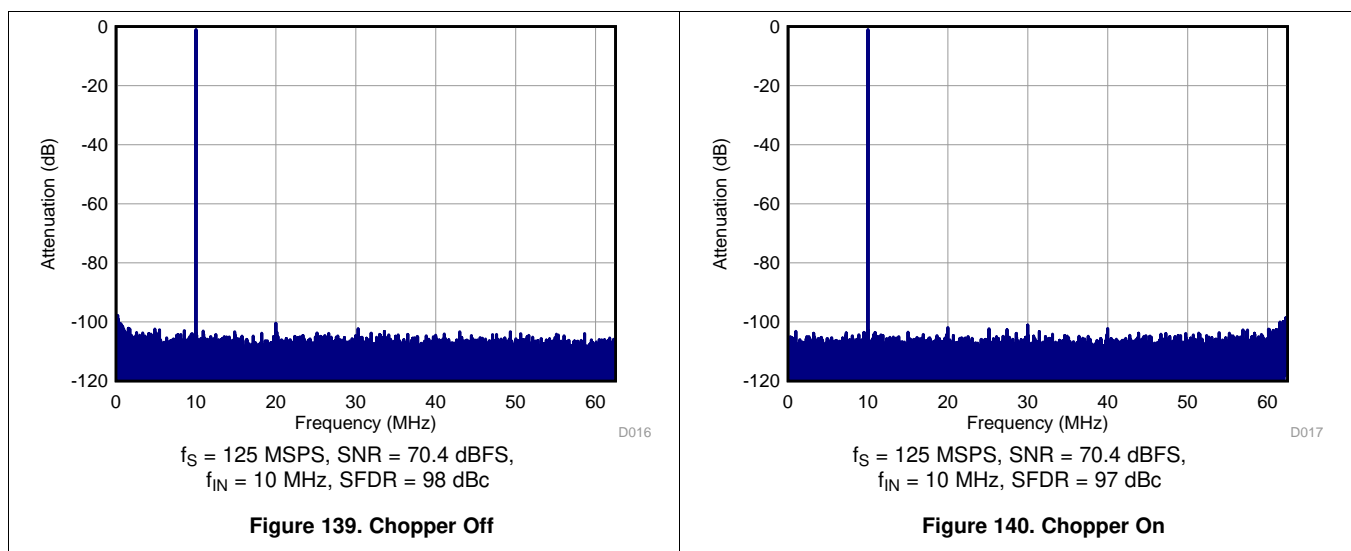
## 9.4 Device Functional Modes

### 9.4.1 Input Clock Divider

The devices are equipped with an internal divider on the clock input. The clock divider allows operation with a faster input clock, thus simplifying the system clock distribution design. The clock divider can be bypassed for operation with a 125-MHz clock and the divide-by-2 option supports a maximum input clock of 250 MHz and the divide-by-4 option provides a maximum input clock frequency of 500 MHz.

### 9.4.2 Chopper Functionality

The devices are equipped with an internal chopper front-end. Enabling the chopper function swaps the ADC noise spectrum by shifting the  $1/f$  noise from dc to  $f_S / 2$ . [Figure 139](#) shows the noise spectrum with the chopper off and [Figure 140](#) shows the noise spectrum with the chopper on. This function is especially useful in applications requiring good ac performance at low input frequencies or in dc-coupled applications. The chopper can be enabled via SPI register writes and is recommended for input frequencies below 30 MHz. The chopper function creates a spur at  $f_S / 2$  that must be filtered out digitally.



### 9.4.3 Power-Down Control

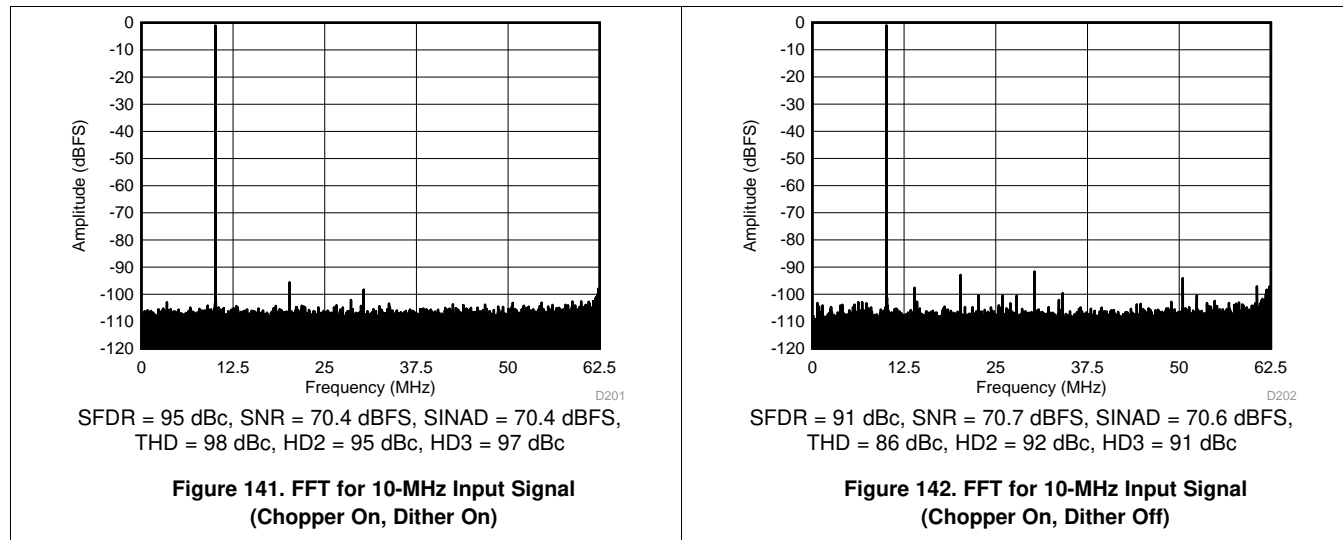
The power-down functions of the ADC342x can be controlled either through the parallel control pin (PDN) or through an SPI register setting (see [register 15h](#)). The PDN pin can also be configured via SPI to a global power-down or standby functionality, as shown in [Table 4](#).

**Table 4. Power-Down Modes**

FUNCTION	POWER CONSUMPTION (mW)	WAKE-UP TIME ( $\mu$ s)
Global power-down	5	85
Standby	45	35

### 9.4.4 Internal Dither Algorithm

The ADC342x use an internal dither algorithm to achieve high SFDR and a clean spectrum. However, the dither algorithm marginally degrades SNR, creating a trade-off between SNR and SFDR. If desired, the dither algorithm can be turned off by using the DIS DITH CHx registers bits. Figure 141 and Figure 142 show the effect of using dither algorithms.



### 9.4.5 Summary of Performance Mode Registers

Table 5 lists the location, value, and functions of performance mode registers in the device.

Table 5. Performance Modes

MODE	REGISTER SETTINGS	DESCRIPTION
Special modes	Registers 139 (bit 3), 239 (bit 3), 439 (bit 3), and 539 (bit 3)	Always write 1 for best performance
Disable dither	Registers 1 (bits 7:0), 134 (bits 5 and 3), 234 (bits 5 and 3), 434 (bits 5 and 3), and 534 (bits 5 and 3)	Disable dither to improve SNR
Disable chopper	Registers 122 (bit 1), 222 (bit 1), 422 (bit 1), and 522 (bit 1)	Disable chopper (shifts 1/f noise floor at dc)
High IF modes	Registers 11Dh (bit 1), 21Dh (bit 1), 41Dh (bit 1), 51Dh (bit 1), 308h (bits 7-6) and 608h (bits 7-6)	Improves HD3 by a couple of dB for IF > 100 MHz

## 9.5 Programming

The ADC342x can be configured using a serial programming interface, as described in this section.

### 9.5.1 Serial Interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

## Programming (continued)

### 9.5.1.1 Register Initialization

After power-up, the internal registers **must** be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin (of durations greater than 10 ns), as shown in [Figure 143](#). If required, the serial interface registers can be cleared during operation either:

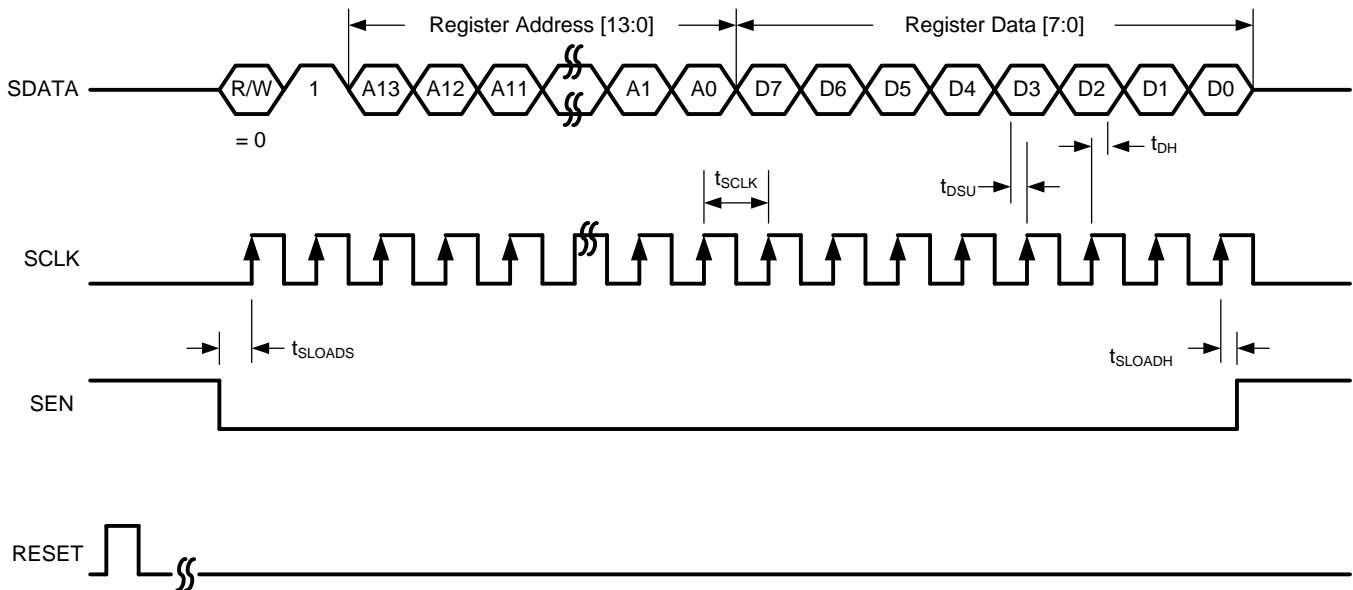
1. Through a hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

#### 9.5.1.1.1 Serial Register Write

The device internal register can be programmed with these steps:

1. Drive the SEN pin low,
2. Set the R/W bit to 0 (bit A15 of the 16-bit address),
3. Set bit A14 in the address field to 1,
4. Initiate a serial interface cycle by specifying the address of the register (A13 to A0) whose content must be written, and
5. Write the 8-bit data that are latched in on the SCLK rising edge.

[Figure 143](#) and [Table 6](#) show the timing requirements for the serial register write operation.



**Figure 143. Serial Register Write Timing Diagram**

**Table 6. Serial Interface Timing<sup>(1)</sup>**

		MIN	TYP	MAX	UNIT
$f_{SCLK}$	SCLK frequency (equal to $1 / t_{SCLK}$ )	> dc		20	MHz
$t_{SLOADS}$	SEN to SCLK setup time	25			ns
$t_{SLOADH}$	SCLK to SEN hold time	25			ns
$t_{DSU}$	SDIO setup time	25			ns
$t_{DH}$	SDIO hold time	25			ns

(1) Typical values are at 25°C, full temperature range is from  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ , and  $AVDD = DVDD = 1.8\text{ V}$ , unless otherwise noted.



### 9.5.1.1.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low.
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Set bit A14 in the address field to 1.
4. Initiate a serial interface cycle specifying the address of the register (A13 to A0) whose content must be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK rising edge.
7. To enable register writes, reset the R/W register bit to 0.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 144 shows a timing diagram of the serial register read operation. Data appear on the SDOUT pin at the SCLK falling edge with an approximate delay ( $t_{SD\_DELAY}$ ) of 20 ns, as shown in Figure 145.

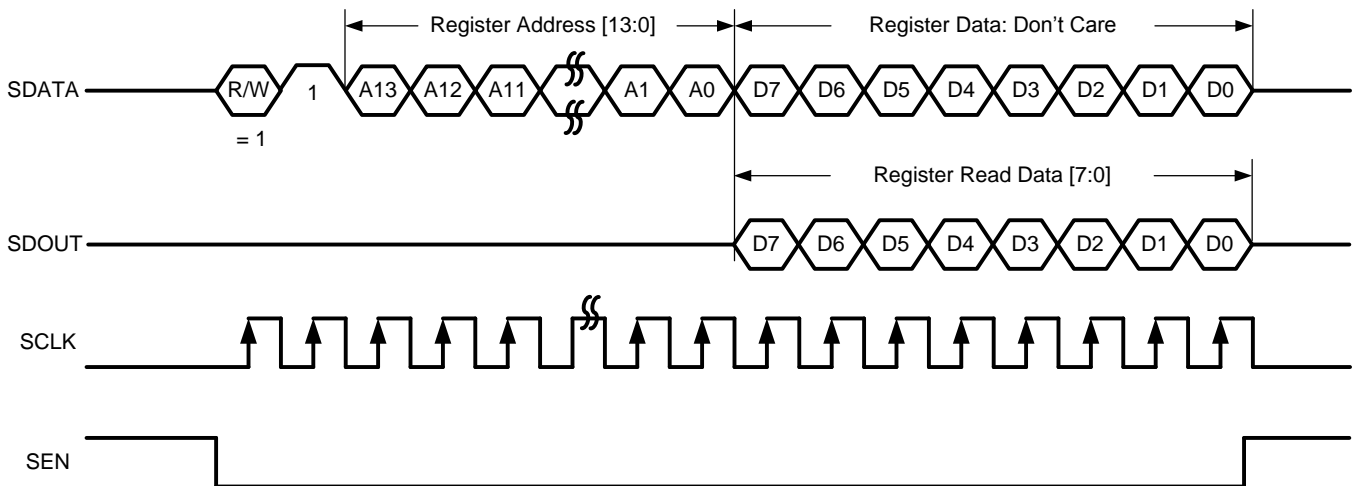


Figure 144. Serial Register Read Timing Diagram

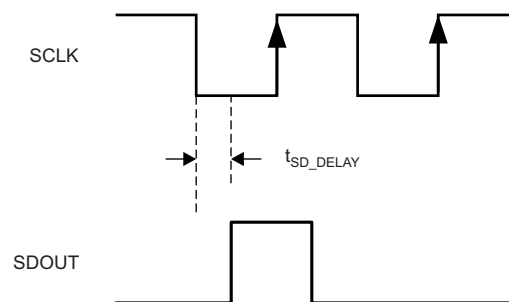
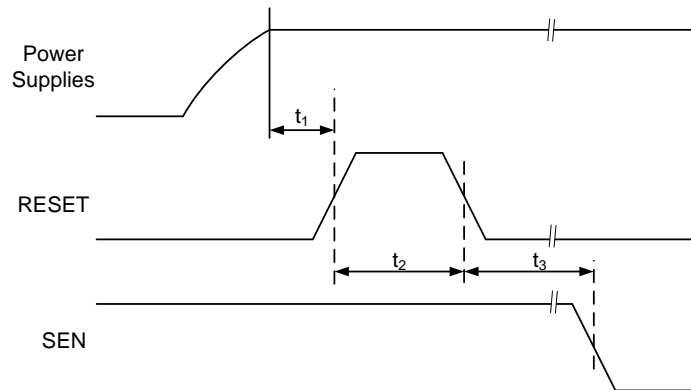


Figure 145. SDOUT Timing Diagram

### 9.5.2 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in [Figure 146](#) and [Table 7](#).



**Figure 146. Initialization of Serial Registers after Power-Up**

**Table 7. Power-Up Timing**

		MIN	TYP	MAX	UNIT
$t_1$	Power-on delay from power-up to active high RESET pulse	1			ms
$t_2$	Reset pulse duration: active high RESET pulse duration	10			ns
$t_3$	Register write delay from RESET disable to SEN active	100			ns

If required, the serial interface registers can be cleared during operation either:

1. Through hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

## 9.6 Register Maps

**Table 8. Register Map Summary**

REGISTER ADDRESS, A[13:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
Register 01h	DIS DITH CHA		DIS DITH CHB		DIS DITH CHC		DIS DITH CHD	
Register 03h	0	0	0	0	0	0	0	ODD EVEN
Register 04h	0	0	0	0	0	0	0	FLIP WIRE
Register 05h	0	0	0	0	0	0	0	1W-2W
Register 06h	0	0	0	0	0	0	TEST PATTERN EN	RESET
Register 07h	0	0	0	0	0	0	0	OVR ON LSB
Register 09h	0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
Register 0Ah	CHA TEST PATTERN				CHB TEST PATTERN			
Register 0Bh	CHC TEST PATTERN 0				CHD TEST PATTERN			
Register 0Eh	CUSTOM PATTERN[11:4]							
Register 0Fh	CUSTOM PATTERN[3:0]				0	0	0	0
Register 13h	0	0	0	0	0	0	LOW SPEED ENABLE	
Register 15h	CHA PDN	CHB PDN	CHC PDN	CHD PDN	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN
Register 25h	LVDS SWING							
Register 27h	CLK DIV		0	0	0	0	0	0
Register 11Dh	0	0	0	0	0	0	HIGH IF MODE0	0
Register 122h	0	0	0	0	0	0	DIS CHOP CHA	0
Register 134h	0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
Register 139h	0	0	0	0	SP1 CHA	0	0	0
Register 21Dh	0	0	0	0	0	0	HIGH IF MODE1	0
Register 222h	0	0	0	0	0	0	DIS CHOP CHD	0
Register 234h	0	0	DIS DITH CHD	0	DIS DITH CHD	0	0	0
Register 239h	0	0	0	0	SP1 CHD	0	0	0
Register 308	HIGH IF MODE <5:4>		0	0	0	0	0	0
Register 41Dh	0	0	0	0	0	0	HIGH IF MODE2	0
Register 422h	0	0	0	0	0	0	DIS CHOP CHB	0
Register 434h	0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0
Register 439h	0	0	0	0	SP1 CHB	0	0	0
Register 51Dh	0	0	0	0	0	0	HIGH IF MODE3	0
Register 522h	0	0	0	0	0	0	DIS CHOP CHC	0
Register 534h	0	0	DIS DITH CHC	0	DIS DITH CHC	0	0	0
Register 539h	0	0	0	0	SP1 CHC	0	0	0
Register 608h	HIGH IF MODE <7:6>		0	0	0	0	0	0
Register 70Ah	0	0	0	0	0	0	0	PDN SYSREF

## 9.6.1 Serial Register Description

### 9.6.1.1 Register 01h (address = 01h)

**Figure 147. Register 01h**

7	6	5	4	3	2	1	0
DIS DITH CHA		DIS DITH CHB		DIS DITH CHC		DIS DITH CHD	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

**Table 9. Register 01h Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	DIS DITH CHA	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 134h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
5-4	DIS DITH CHB	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 434h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
3-2	DIS DITH CHC	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 534h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
1-0	DIS DITH CHD	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 234h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz.

### 9.6.1.2 Register 03h (address = 03h)

**Figure 148. Register 03h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ODD EVEN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 10. Register 03h Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
0	ODD EVEN	R/W	0h	This bit selects the bit sequence on the output wires (in 2-wire mode only). 0 = Bits 0, 1, 2, and so forth appear on wire-0; bits 7, 8, 9, and so forth appear on wire-1. 1 = Bits 0, 2, 4, and so forth appear on wire-0; bits 1, 3, 5, and so forth appear on wire-1.

### 9.6.1.3 Register 04h (address = 04h)

**Figure 149. Register 04h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FLIP WIRE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 11. Register 04h Field Descriptions**

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	FLIP WIRE	R/W	0h	This bit flips the data on the output wires. Valid only in two wire configuration. 0 = Default 1 = Data on output wires is flipped. Pin D0x becomes D1x, and vice versa.

### 9.6.1.4 Register 05h (address = 05h)

**Figure 150. Register 05h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1W-2W
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 12. Register 05h Field Descriptions**

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	1W-2W	R/W	0h	This bit transmits output data on either one or two wires. 0 = Output data are transmitted on two wires (Dx0P, Dx0M and Dx1P, Dx1M) 1 = Output data are transmitted on one wire (Dx0P, Dx0M). In this mode, the recommended $f_S$ is less than 80 MSPS.

### 9.6.1.5 Register 06h (address = 06h)

**Figure 151. Register 06h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TEST PATTERN EN	RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 13. Register 06h Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	TEST PATTERN EN	R/W	0h	This bit enables test pattern selection for the digital outputs. 0 = Normal output 1 = Test pattern output enabled
0	RESET	R/W	0h	This bit applies a software reset. This bit resets all internal registers to the default values and self-clears to 0.

**9.6.1.6 Register 07h (address = 07h)**
**Figure 152. Register 07h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	OVR ON LSB
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 14. Register 07h Field Descriptions**

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	OVR ON LSB	R/W	0h	This bit provides OVR information on the LSB bits. 0 = Output data bit 0 functions as the LSB of the 12-bit data 1 = Output data bit 0 carries the overrange (OVR) information

**9.6.1.7 Register 09h (address = 09h)**
**Figure 153. Register 09h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 15. Register 09h Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	ALIGN TEST PATTERN	R/W	0h	This bit aligns the test patterns across the outputs of both channels. 0 = Test patterns of both channels are free running 1 = Test patterns of both channels are aligned
0	DATA FORMAT	R/W	0h	This bit selects the digital output data format. 0 = Twos complement 1 = Offset binary

**9.6.1.8 Register 0Ah (address = 0Ah)**
**Figure 154. Register 0Ah**

7	6	5	4	3	2	1	0
CHA TEST PATTERN				CHB TEST PATTERN			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

**Table 16. Register 0Ah Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	CHA TEST PATTERN	R/W	0h	<p>These bits control the test pattern for channel A after the TEST PATTERN EN bit is set.</p> <p>0000 = Normal operation  0001 = All 0's  0010 = All 1's  0011 = Toggle pattern: data alternate between 1010101010 and 0101010101  0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095  0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits  0110 = Deskew pattern: data are AAAh  1000 = PRBS pattern: data are a sequence of pseudo random numbers  1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, and 599  Others = Do not use</p>
3-0	CHB TEST PATTERN	R/W	0h	<p>These bits control the test pattern for channel B after the TEST PATTERN EN bit is set.</p> <p>0000 = Normal operation  0001 = All 0's  0010 = All 1's  0011 = Toggle pattern: data alternate between 1010101010 and 0101010101  0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095  0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits  0110 = Deskew pattern: data are AAAh  1000 = PRBS pattern: data are a sequence of pseudo random numbers  1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, and 599  Others = Do not use</p>

**9.6.1.9 Register 0Bh (address = 0Bh)**
**Figure 155. Register 0Bh**

7	6	5	4	3	2	1	0
CHC TEST PATTERN				CHD TEST PATTERN			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

**Table 17. Register 0Bh Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	CHC TEST PATTERN	R/W	0h	These bits control the test pattern for channel C after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095. 0110 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 1000 = Deskew pattern: data are AAAh. 1010 = PRBS pattern: data are a sequence of pseudo random numbers. 1011 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, 599. Others = Do not use
3-0	CHD TEST PATTERN	R/W	0h	These bits control the test pattern for channel D after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095. 0110 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 1000 = Deskew pattern: data are AAAh. 1010 = PRBS pattern: data are a sequence of pseudo random numbers. 1011 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, 599. Others = Do not use

**9.6.1.10 Register 0Eh (address = 0Eh)**
**Figure 156. Register 0Eh**

7	6	5	4	3	2	1	0
CUSTOM PATTERN[11:4]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

**Table 18. Register 0Eh Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	CUSTOM PATTERN[11:4]	R/W	0h	These bits set the 12-bit custom pattern (bits 11-4) for all channels.



**9.6.1.11 Register 0Fh (address = 0Fh)**
**Figure 157. Register 0Fh**

7	6	5	4	3	2	1	0
CUSTOM PATTERN[3:0]				0	0	0	0
R/W-0h				W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 19. Register 0Fh Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	CUSTOM PATTERN[3:0]	R/W	0h	These bits set the 12-bit custom pattern (bits 3-0) for all channels.
3-0	0	W	0h	Must write 0.

**9.6.1.12 Register 13h (address = 13h)**
**Figure 158. Register 13h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LOW SPEED ENABLE	
W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 20. Register 13h Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1-0	LOW SPEED ENABLE	R/W	0h	Enables low speed operation in 1-wire and 2-wire mode. Depending upon sampling frequency, write this bit as per <a href="#">Table 21</a> .

**Table 21. LOW SPEED ENABLE Register Settings Across  $f_s$** 

$f_s$ , MSPS		REGISTER BIT LOW SPEED ENABLE	
MIN	MAX	1-WIRE MODE	2-WIRE MODE
25	125	00	00
20	25	10	11
15	20	10	Not supported

**9.6.1.13 Register 15h (address = 15h)**
**Figure 159. Register 15h**

7	6	5	4	3	2	1	0
CHA PDN	CHB PDN	CHC PDN	CHD PDN	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN
W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 22. Register 15h Field Descriptions**

Bit	Field	Type	Reset	Description
7	CHA PDN	W	0h	0 = Normal operation 1 = Power-down channel A
6	CHB PDN	R/W	0h	0 = Normal operation 1 = Power-down channel B
5	CHC PDN	R/W	0h	0 = Normal operation 1 = Power-down channel C
4	CHD PDN	W	0h	0 = Normal operation 1 = Power-down channel D
3	STANDBY	R/W	0h	The ADCs of both channels enter standby. 0 = Normal operation 1 = Standby
2	GLOBAL PDN	R/W	0h	0 = Normal operation 1 = Global power-down
1	0	W	0h	Must write 0.
0	CONFIG PDN PIN	R/W	0h	This bit configures the PDN pin as either a global power-down or standby pin. 0 = Logic high voltage on the PDN pin sends the device into global power-down 1 = Logic high voltage on the PDN pin sends the device into standby

**9.6.1.14 Register 25h (address = 25h)**
**Figure 160. Register 25h**

7	6	5	4	3	2	1	0
LVDS SWING							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

**Table 23. Register 25h Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LVDS SWING	R/W	0h	These bits control the swing of the LVDS outputs (including the data output, bit clock, and frame clock).

**9.6.1.15 Register 27h (address = 27h)**
**Figure 161. Register 27h**

7	6	5	4	3	2	1	0
CLK DIV		0	0	0	0	0	0
R/W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 24. Register 27h Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	CLK DIV	R/W	0h	These bits select the internal clock divider for the input sampling clock. 00 = Divide-by-1 01 = Divide-by-1 10 = Divide-by-2 11 = Divide-by-4
5-0	0	W	0h	Must write 0.

**9.6.1.16 Register 11Dh (address = 11Dh)**
**Figure 162. Register 11Dh**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 25. Register 11Dh Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE0			Set the HIGH IF MODE[7:0] bits together to 1111. Improves HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

**9.6.1.17 Register 122h (address = 122h)**
**Figure 163. Register 122h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHA	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 26. Register 122h Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHA	R/W	0h	This bit disables the chopper. Set this bit to shift the 1/f noise floor at dc. 0 = 1/f noise floor is centered at $f_S / 2$ (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

**9.6.1.18 Register 134h (address = 134h)**
**Figure 164. Register 134h**

7	6	5	4	3	2	1	0
0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 27. Register 134h Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHA	R/W	0h	Set this bit along with bits 7 and 6 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHA	R/W	0h	Set this bit along with bits 7 and 6 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

**9.6.1.19 Register 139h (address = 139h)**
**Figure 165. Register 139h**

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHA	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 28. Register 139h Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHA	R/W	0h	This bit sets the special mode for best performance on channel A. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

**9.6.1.20 Register 21Dh (address = 21Dh)**
**Figure 166. Register 21Dh**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE1	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 29. Register 21Dh Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE1	R/W	0h	Set the HIGH IF MODE[7:0] bits together to 1111. Improves HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

**9.6.1.21 Register 222h (address = 222h)**
**Figure 167. Register 222h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHD	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 30. Register 222h Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHD	R/W	0h	This bit disables the chopper. Set this bit to shift the 1/f noise floor at dc. 0 = 1/f noise floor is centered at $f_s / 2$ (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

**9.6.1.22 Register 234h (address = 234h)**
**Figure 168. Register 234h**

7	6	5	4	3	2	1	0
0	0	DIS DITH CHD	0	DIS DITH CHD	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 31. Register 234h Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHD	R/W	0h	Set this bit with bits 1 and 0 of register 01h. 00 = Default 11 = Dither is disabled for channel D. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHD	R/W	0h	Set this bit with bits 1 and 0 of register 01h. 00 = Default 11 = Dither is disabled for channel D. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

**9.6.1.23 Register 239h (address = 239h)**
**Figure 169. Register 239h**

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHD	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 32. Register 239h Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHD	R/W	0h	This bit sets the special mode for best performance on channel D. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

**9.6.1.24 Register 308h (address = 308h)**
**Figure 170. Register 308h**

7	6	5	4	3	2	1	0
HIGH IF MODE<5:4>	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 33. Register 308h Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	HIGH IF MODE<5:4>	R/W	0h	Set the HIGH IF MODE[7:0] bits together to FFh. Improves HD3 by a couple of dB for IF > 100 MHz.
5-0	0	W	0h	Must write 0.

**9.6.1.25 Register 41Dh (address = 41Dh)**
**Figure 171. Register 41Dh**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE2	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 34. Register 41Dh Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE2	R/W	0h	Set the HIGH IF MODE[7:0] bits together to FFh. Improves HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

**9.6.1.26 Register 422h (address = 422h)**
**Figure 172. Register 422h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHB	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 35. Register 422h Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHB	R/W	0h	This bit disables the chopper. Set this bit to shift the 1/f noise floor at dc. 0 = 1/f noise floor is centered at $f_s / 2$ (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

**9.6.1.27 Register 434h (address = 434h)**
**Figure 173. Register 434h**

7	6	5	4	3	2	1	0
0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 36. Register 434h Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHB	R/W	0h	Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHB	R/W	0h	Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

**9.6.1.28 Register 439h (address = 439h)**
**Figure 174. Register 439h**

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHB	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 37. Register 439h Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHB	R/W	0h	This bit sets the special mode for best performance on channel B. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

**9.6.1.29 Register 51Dh (address = 51Dh)**
**Figure 175. Register 51Dh**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE3	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 38. Register 51Dh Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE3	R/W	0h	Set the HIGH IF MODE[7:0] bits together to FFh. Improves HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

**9.6.1.30 Register 522h (address = 522h)**
**Figure 176. Register 522h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHC	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 39. Register 522h Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHC	R/W	0h	This bit disables the chopper. Set this bit to shift the 1/f noise floor at dc. 0 = 1/f noise floor is centered at $f_s / 2$ (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.



**9.6.1.31 Register 534h (address = 534h)**
**Figure 177. Register 534h**

7	6	5	4	3	2	1	0
0	0	DIS DITH CHC	0	DIS DITH CHC	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 40. Register 534h Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHC	R/W	0h	Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel C. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHC	R/W	0h	Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel C. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

**9.6.1.32 Register 539h (address = 539h)**
**Figure 178. Register 539h**

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHC	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 41. Register 539h Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHC	R/W	0h	This bit sets the special mode for best performance on channel C. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

**9.6.1.33 Register 608h (address = 608h)**
**Figure 179. Register 608h**

7	6	5	4	3	2	1	0
HIGH IF MODE<7:6>	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

**Table 42. Register 608h Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	HIGH IF MODE<7:6>	R/W	0h	Set the HIGH IF MODE[7:0] bits together to FFh. Improves HD3 by a couple of dB for IF > 100 MHz.
5-0	0	W	0h	Must write 0.

9.6.1.34 Register 70Ah (address = 70Ah)

Figure 180. Register 70Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PDN SYSREF
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 43. Register 70Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	PDN SYSREF	R/W	0h	If the SYSREF pins are not used in the system, the SYSREF buffer must be powered down by setting this bit. 0 = Normal operation 1 = Powers down the SYSREF buffer

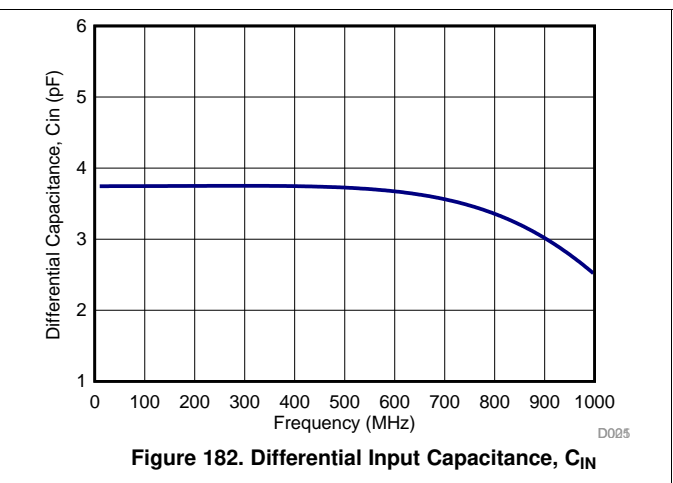
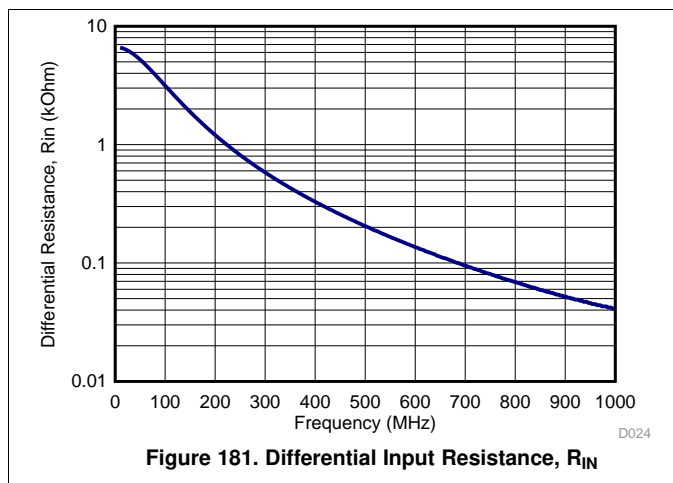
10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 250 MHz to achieve good phase and amplitude balances at ADC inputs. When designing the dc driving circuits, the ADC input impedance must be considered. Figure 181 and Figure 182 show the impedance ( $Z_{in} = R_{in} || C_{in}$ ) across the ADC input pins.



## 10.2 Typical Applications

### 10.2.1 Driving Circuit Design: Low Input Frequencies

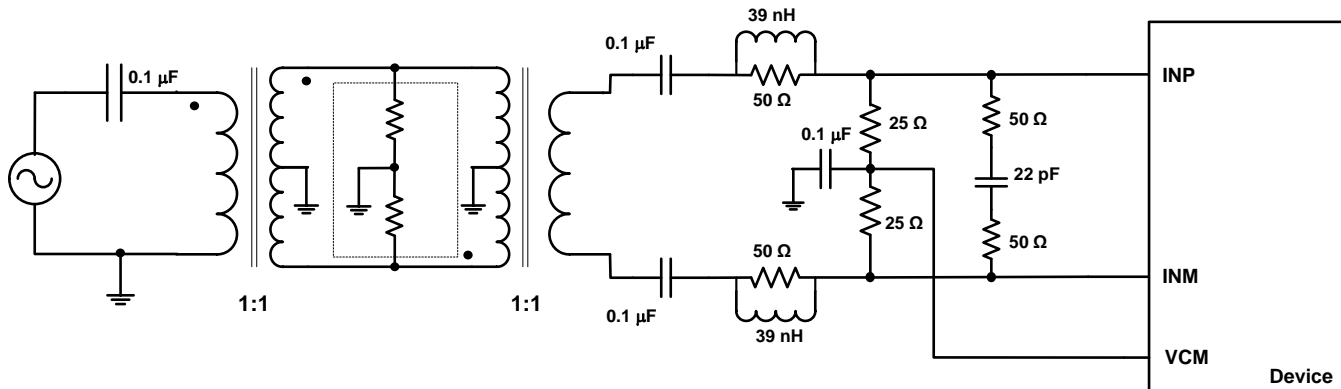


Figure 183. Driving Circuit for Low Input Frequencies

#### 10.2.1.1 Design Requirements

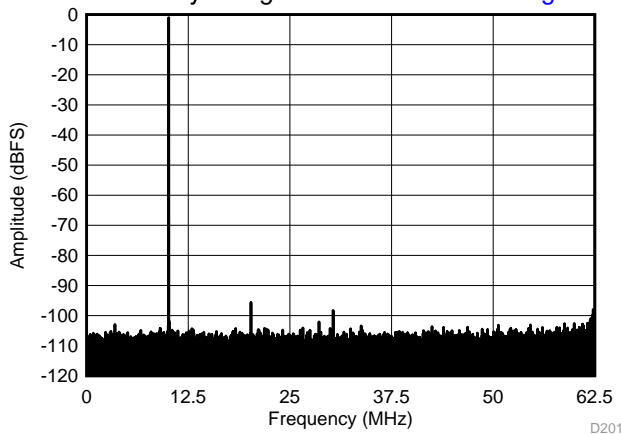
For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitic. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

#### 10.2.1.2 Detailed Design Procedure

A typical application involving using two back-to-back coupled transformers is illustrated in Figure 183. The circuit is optimized for low input frequencies. An external R-C-R filter using 50-Ω resistors and a 22-pF capacitor is used with the series inductor (39 nH), this combination helps absorb the sampling glitches.

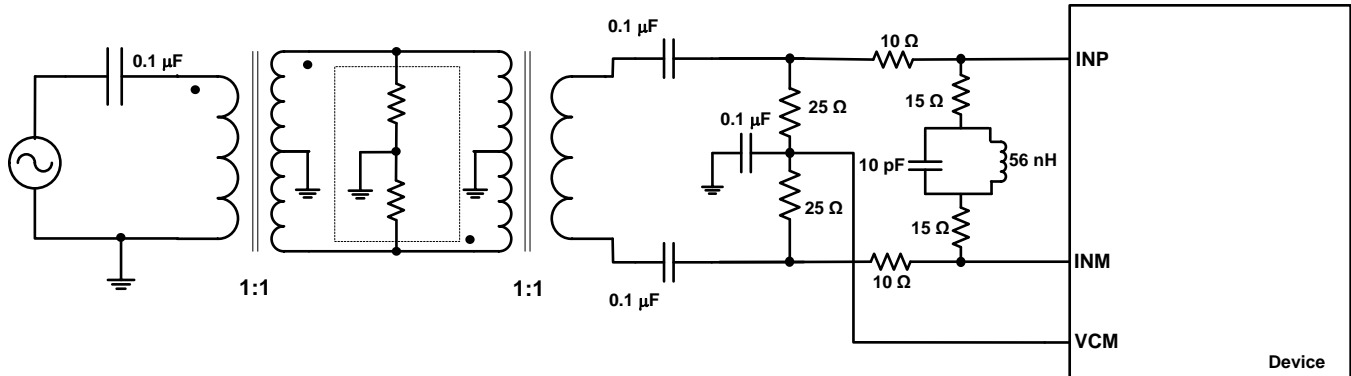
#### 10.2.1.3 Application Curve

Figure 184 shows the performance obtained by using the circuit shown in Figure 183.



SFDR = 97 dBc, SNR = 70.4 dBFS, SINAD = 70.4 dBFS,  
THD = 98 dBc, HD2 = 95 dBc, HD3 = 97 dBc

Figure 184. Performance FFT at 10 MHz (Low Input Frequency)

**Typical Applications (continued)**
**10.2.2 Driving Circuit Design: Input Frequencies Between 100 MHz to 230 MHz**


**Figure 185. Driving Circuit for Mid-Range Input Frequencies ( $100 \text{ MHz} < f_{\text{IN}} < 230 \text{ MHz}$ )**

**10.2.2.1 Design Requirements**

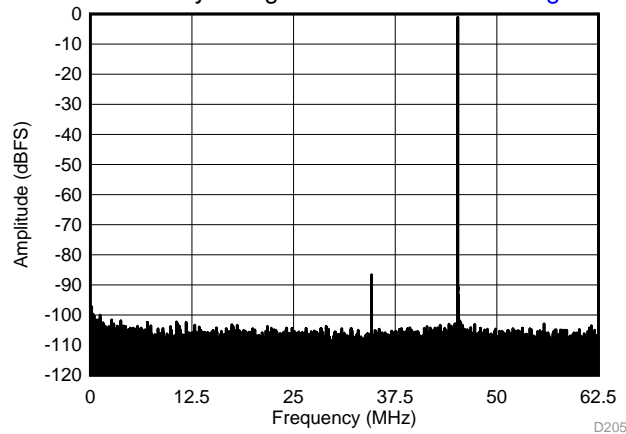
See the [Design Requirements](#) section for further details.

**10.2.2.2 Detailed Design Procedure**

When input frequencies are between 100 MHz to 230 MHz, an R-LC-R circuit can be used to optimize performance, as shown in [Figure 185](#).

**10.2.2.3 Application Curve**

[Figure 186](#) shows the performance obtained by using the circuit shown in [Figure 185](#).



SFDR = 86 dBc, SNR = 69.8 dBFS, SINAD = 69.8 dBFS,  
THD = 91 dBc, HD2 = 86 dBc, HD3 = 101 dBc

**Figure 186. Performance FFT at 170 MHz (Mid Input Frequency)**

## Typical Applications (continued)

### 10.2.3 Driving Circuit Design: Input Frequencies Greater than 230 MHz

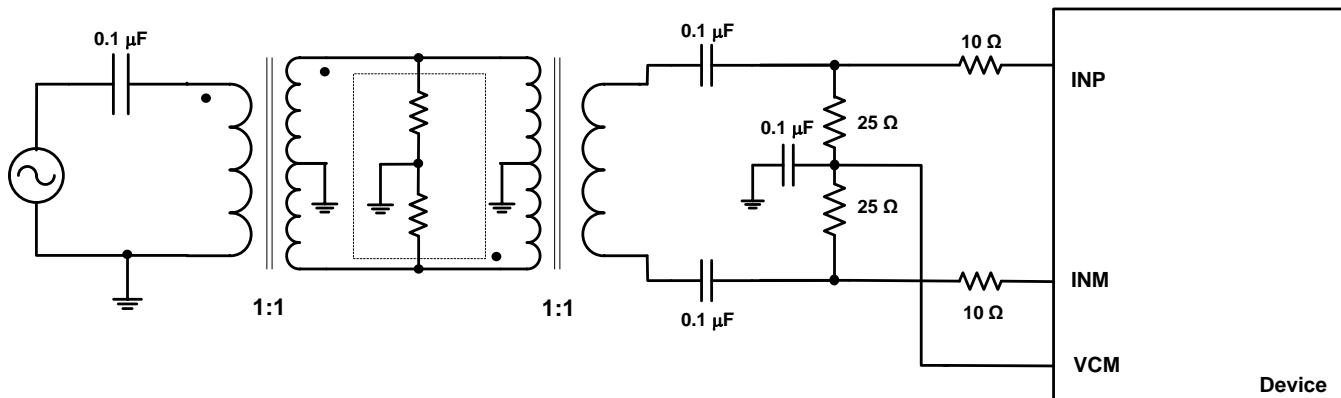


Figure 187. Driving Circuit for High Input Frequencies ( $f_{IN} > 230$  MHz)

#### 10.2.3.1 Design Requirements

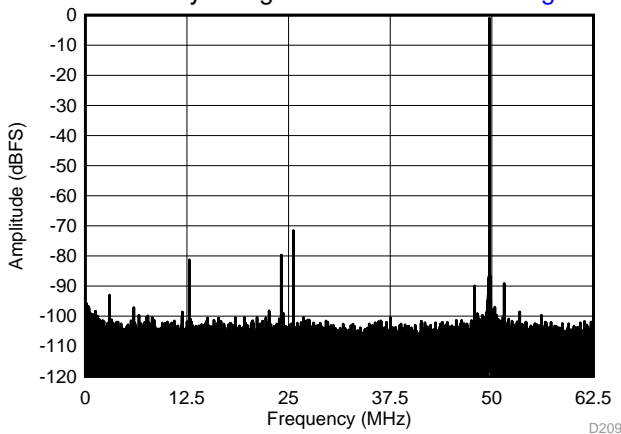
See the [Design Requirements](#) section for further details.

#### 10.2.3.2 Detailed Design Procedure

For high input frequencies ( $> 230$  MHz), using the R-C-R or R-LC-R circuit does not show significant improvement in performance. However, a series resistance of  $10\ \Omega$  can be used as shown in [Figure 187](#).

#### 10.2.3.3 Application Curve

[Figure 188](#) shows the performance obtained by using the circuit shown in [Figure 187](#).



SFDR = 71 dBc, SNR = 67.2 dBFS, SINAD = 66.5 dBFS,  
THD = 74 dBc, HD2 = 71 dBc, HD3 = 79 dBc

Figure 188. Performance FFT at 450 MHz (High Input Frequency)

## 11 Power Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD can power up in any order.

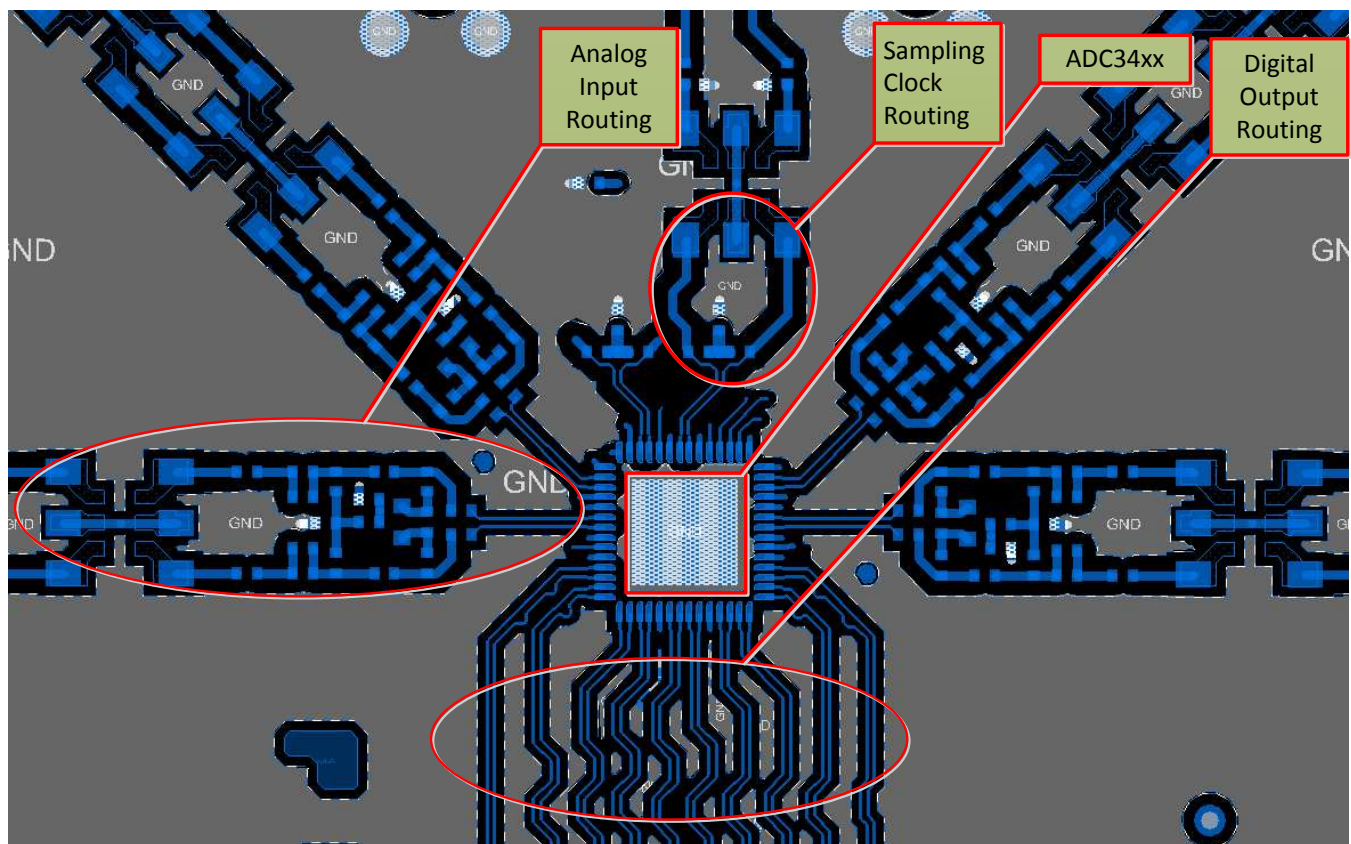
## 12 Layout

### 12.1 Layout Guidelines

The ADC342x EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in [Figure 189](#). Some important points to remember during laying out the board are:

1. Analog inputs are located on opposite sides of the device pin out to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pin out in opposite directions, as shown in the reference layout of [Figure 189](#) as much as possible.
2. In the device pin out, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of [Figure 189](#) as much as possible.
3. Keep digital outputs away from the analog inputs. When these digital outputs exit the pin out, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
4. At each power-supply pin (AVDD and DVDD), keep a 0.1- $\mu$ F decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10- $\mu$ F, 1- $\mu$ F, and 0.1- $\mu$ F capacitors can be kept close to the supply source.

### 12.2 Layout Example



**Figure 189. Typical Layout of the ADC342x Board**

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 44. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADC3421	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ADC3422	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ADC3423	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ADC3424	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.3 Trademarks

E2E is a trademark of Texas Instruments.  
PowerPAD is a trademark of Texas Instruments, Inc.  
All other trademarks are the property of their respective owners.

### 13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC3421IRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3421	<a href="#">Samples</a>
ADC3421IRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3421	<a href="#">Samples</a>
ADC3422IRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3422	<a href="#">Samples</a>
ADC3422IRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3422	<a href="#">Samples</a>
ADC3423IRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3423	<a href="#">Samples</a>
ADC3423IRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3423	<a href="#">Samples</a>
ADC3424IRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3424	<a href="#">Samples</a>
ADC3424IRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3424	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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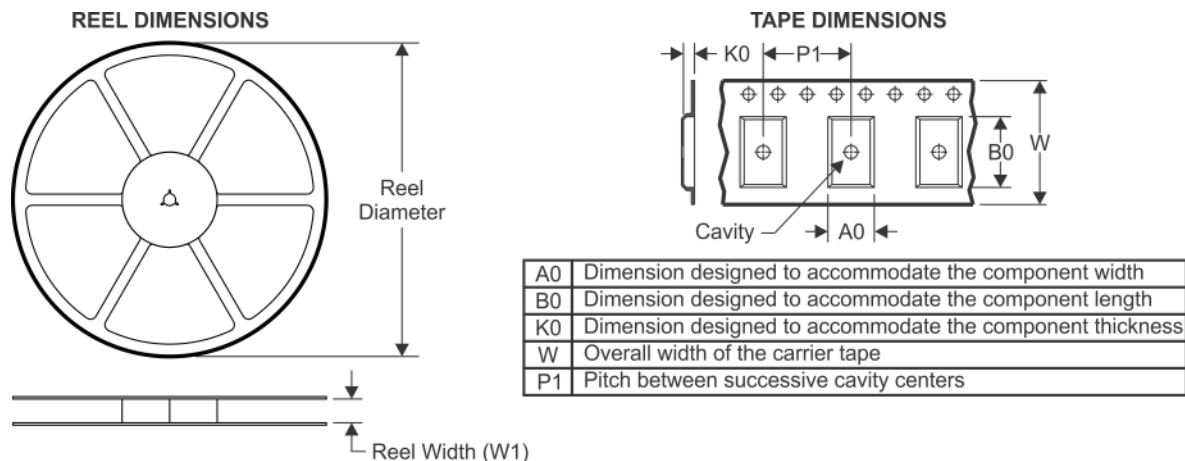
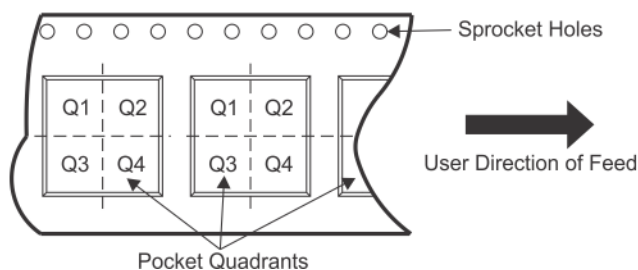
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF ADC3421 :**

- Automotive: [ADC3421-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC3421IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
ADC3422IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
ADC3423IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
ADC3424IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC3421IRTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
ADC3422IRTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
ADC3423IRTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
ADC3424IRTQR	QFN	RTQ	56	2000	350.0	350.0	43.0

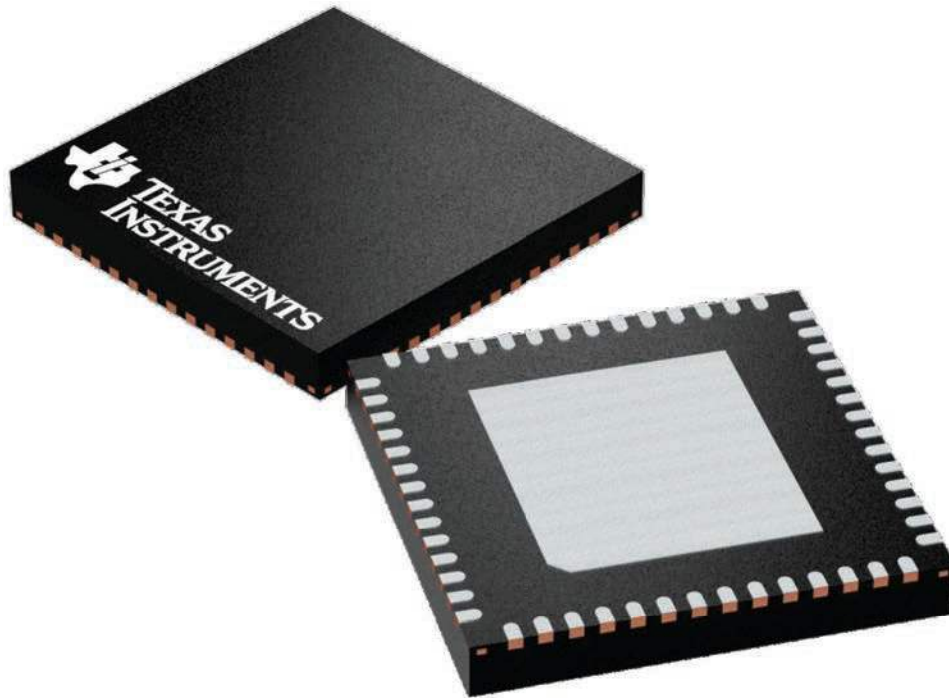
## GENERIC PACKAGE VIEW

**RTQ 56**

**VQFN - 1 mm max height**

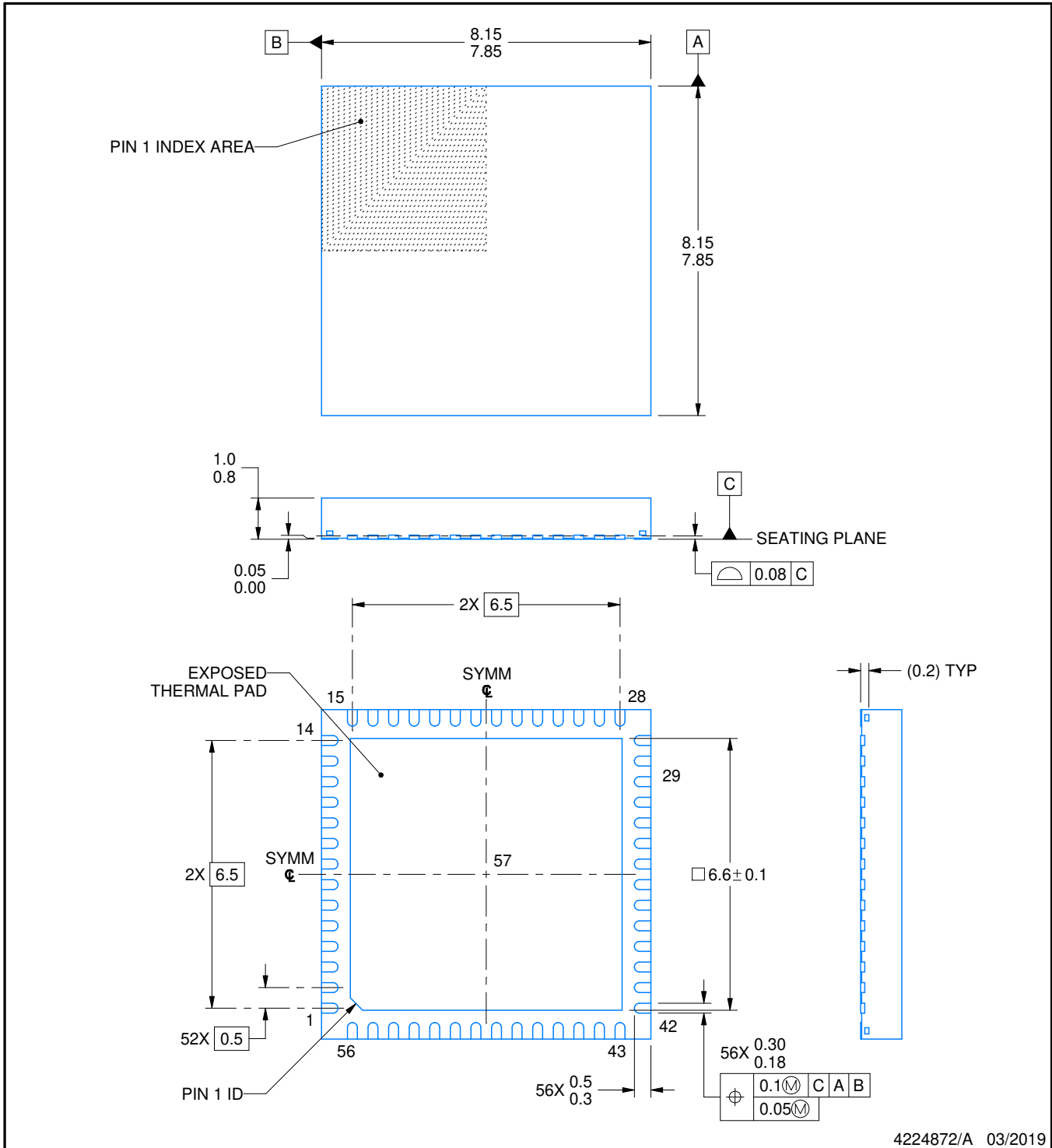
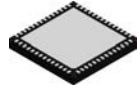
8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224653/A



NOTES:

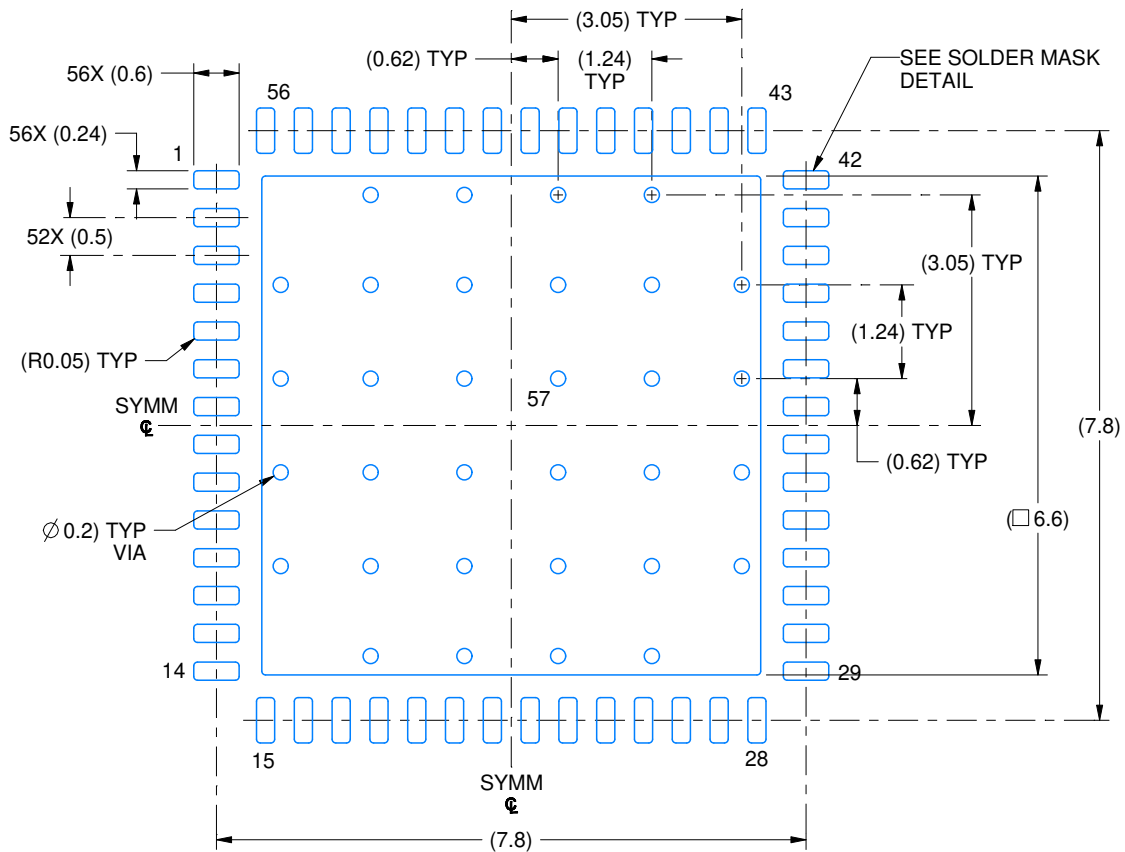
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

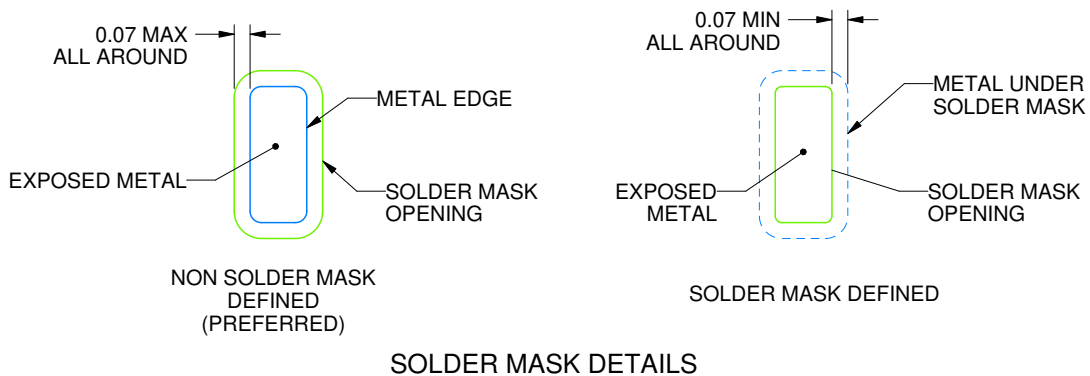
RTQ0056C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4224872/A 03/2019

NOTES: (continued)

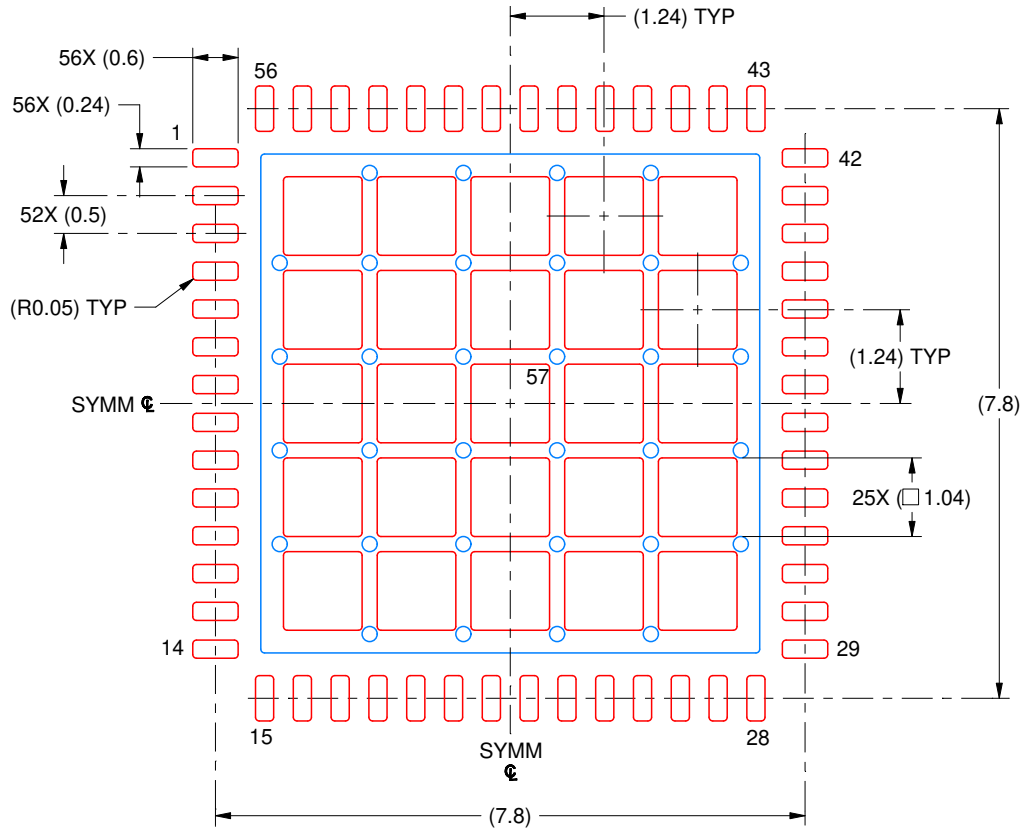
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTQ0056C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 10X

EXPOSED PAD 57  
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224872/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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