Click here to ask about the production status of specific part numbers.

MAX77840

3A Buck Charger with ModelGauge m5 Fuel Gauge and USB BC1.2 Detection

General Description

The MAX77840 is a 3.15A switched-mode charger and ModelGauge™ m5 fuel gauge with integrated USB BC1.2 detection for Li-ion batteries and a SAFEOUT LDO.

The charger integrates all switches and operates at either 4MHz or 2MHz (programmable) switching frequency, allowing selection of the smallest external components or achieving lowest heat dissipation. The MAX77840 is ideally suited for devices such as mobile point-of-sale devices, portable medical electronics, or other handheld devices. It includes the USB BC1.2 detection function to recognize common USB adapters and set the input current limit automatically. The MAX77840 can supply up to 1.5A OTG current with proprietary MAXOTG protection, that limits the OTG output current to prevent system voltage from collapsing under heavy OTG loads.

The ModelGauge m5 provides accurate battery fuel gauging and operates with extremely low battery current (25µA, typ) during standby or sleep mode to extend battery life. The interaction between the ModelGauge m5 and the charger provides end users a superior charging experience in a single IC.

Shipping mode is built into the MAX77840 to minimize battery drain when the device is not in use. The MAX77840 features an I^2C 3.0 compatible serial interface. It is offered in a 3.87mm x 3.96mm, 9 x 9 bump array wafer-level package (WLP) with 0.4mm pitch.

Applications

- Industrial PCs
- Portable Medical Devices
- Mobile Point-of-Sale Devices
- Wireless Speakers
- E-Cigarettes
- Smart Home Automation, Sensors
- Internet of Things (IoT)

Benefits and Features

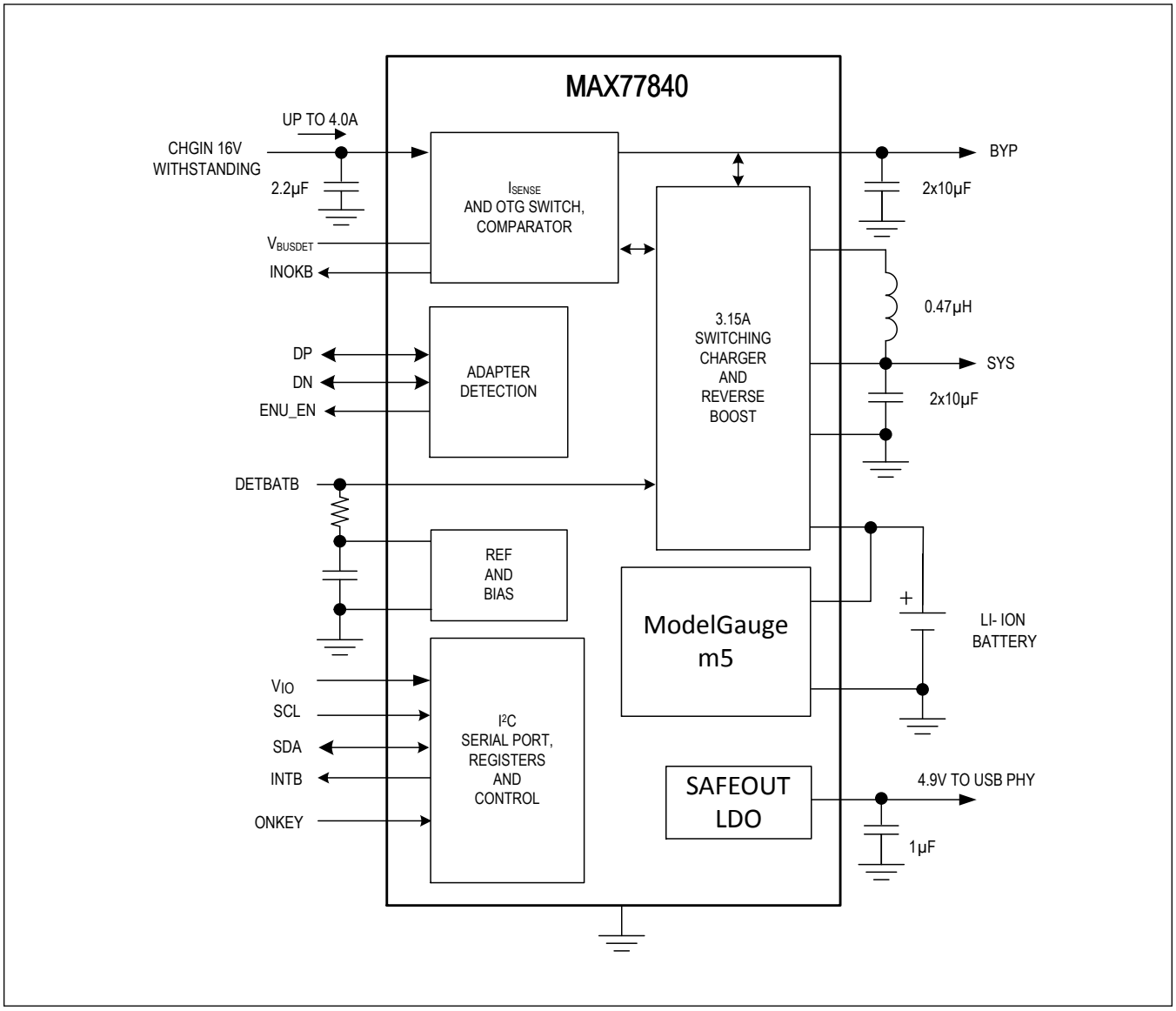
- Single-Input Switch Mode Charger
- Up to 16V Protection
  - Up to 13.4V Input Operating Range
  - Up to 4.0A Input Current Limit with Adaptive Input Current Limiting (AICL)
  - Up to 3.15A Battery Charging Current Limit
  - CC, CV, and Die Temperature Control
  - Small Inductor: 0.47µH or 1µH Package
  - High Efficiency
- Supports USB-OTG Reverse Boost, up to 1.5A Current Limit (Programmable)
- Integrated Battery True-Disconnect FET
  - $R_{DS(ON)}$ = 12.8mΩ
  - Rated Up to $9A_{RMS}$, Discharge Current Limit (Programmable, default 4.5A)
- Adapter Type Detection
  - D+/D- Detection for USB port, USB DCP, and USB HVDCP
  - BC 1.2 Compliant
- ModelGauge m5 Battery Fuel Gauge
  - ±1% SOC Accuracy, No Calibration Cycles, Very Low I_Q
  - Time-to-Empty and Time-to-Full Prediction
- One Safeout LDO
- Control Functions
  - Shipping Mode with ONKEY Pressing Clear
  - True Hardware Reset with ONKEY
- I^2C 3.0 Compatible Interface with Interrupt Output
- 3.87mm x 3.96mm, 9 x 9 Array WLP with 0.4mm Pitch

***Ordering Information* appears at end of data sheet.**

19-7702; Rev 0; 7/21

maxim integrated™

Simplified Block Diagram



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Absolute Maximum Ratings

Switching Charger
- CHGIN to GND_A ..... -0.3V to +16V
- BYP to GND_A ..... -0.3V to +16V
- PVL to GND_A ..... -0.3V to +6V
- AVL to GND_A ..... -0.3V to +6V
- BAT_SP to GND_A ..... -0.3V to +6V
- BAT_SN to GND_A ..... -0.3V to +0.3V
- BATT to GND_A ..... -0.3V to +6V
- SYS to GND_A ..... -0.3V to +6V
- DETBATB to GND_A ..... -0.3V to +6V
- V_{BUSDET} to GND_A ..... -0.3V to +20V
- OVPENB to GND_A ..... -0.3V to AVL + 0.3V
- BST to AVL ..... -0.3V to +16V
- BST to CHGLX ..... -0.3V to +6V
- INOKB to GND_A ..... -0.3V to SYS + 0.3V
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- CHGPG Continuous Current ..... $3.5A_{RMS}$
- SYS Continuous Current ..... $4.5A_{RMS}$
- BATT Continuous Current ..... $4.5A_{RMS}$
- BYP Continuous Current ..... $3.0A_{RMS}$
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- CSN to GND_A ..... -0.3V to BATT + 0.3V
- SLAVE to GND_A ..... -0.3V to SYS_A + 0.3V
- Battery Overvoltage Protection to GND_A ..... -0.3V to BATT + 0.3V
- SWI1, SWI2 to GND_A ..... -0.3V to SYS_A + 0.3V
- GND_D to GND_A ..... -0.3V to +0.3V

Safeout LDO
- SAFEOUT to GND_A ..... -0.3V to VCCINT + 0.3V

Fuel Gauge
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- THMB, THM to GND_A ..... -0.3V to BATT + 0.3V

I^2C and Logic Interface
- V_{IO} to GND_A ..... -0.3V to +6V
- SDA, SCL to GND_A ..... -0.3V to +6V
- SYS_A to GND_A ..... -0.3V to +6V
- SYS_Q to GND_A ..... -0.3V to +6V
- INTB to GND_A ..... -0.3V to SYS_A + 0.3V
- CHGIND to GND_A ..... -0.3V to +6V
- TEST_, V_{CCTEST} to GND_A ..... -0.3V to +6V
- GND_D2 to GND_A ..... -0.3V to +0.3V
- GND_Q to GND_A ..... -0.3V to +0.3V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

21- WLP0775

Package Code	W813C3+1
Outline Number	21-0775
Land Pattern Number	Refer to *Application Note 1891*

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL INFORMATION						
Shutdown Supply Current (BATT and V_{BATTFG})	I_{SHDN}	All circuits off, BATT = V_{BATTFG} = 3.6V		25	50	µA
No Load Supply Current (BATT and V_{BATTFG})	I_{NL}	Fuel Gauge is ON, all other circuits off; BATT = V_{BATTFG} = 3.6V		50	100	µA
SYS INPUT RANGE						
V_{SYS} Operating Voltage	V_{SYS}	Guaranteed by V_{SYS_UVLO} and V_{SYS_OVLO}	2.5		5.5	V
V_{SYS} Undervoltage Lockout Threshold	V_{SYS_UVLO}	V_{BATT} falling, 200mV hysteresis	2.45	2.5	2.55	V
SYS Overvoltage Lockout Threshold	V_{SYS_OVLO}	V_{BATT} rising, 200mV hysteresis	5.20	5.36	5.52	V
Low SYS Thresholds		Range programmable using the LSDAC register, V_{SYS} falling, production tested at 3.60V setting		3.6		V
Low SYS Hysteresis		Range programmable using the LSHYST register, production tested at 100mV setting		100		mV
THERMAL SHUTDOWN						
Thermal ShutdownThreshold	T_{SHDN}	T_J rising		165		°C
Thermal Shutdown Hysteresis				15		°C
LOGIC AND CONTROL INPUTS						
SCL, SDA Input Low Level		T_A = +25°C			0.3 × V_{IO}	V
SCL, SDA Input High Level		T_A = +25°C	0.7 × V_{IO}			V
SCL, SDA Input Hysteresis		T_A = +25°C		0.05 × V_{IO}		V
SCL, SDA Logic Input Current		V_{IO} = +3.6V	-10		+10	µA
SCL, SDA Input Capacitance		(Note 1)		10		pF
SDA Output Low Voltage		Sinking 20mA			0.4	V
Output Low Voltage INTB		I_{SINK} = 1mA			0.4	V
Output High Leakage INTB		V_{SYS} = 5.5V, T_A = +25°C	-1	0	+1	µA
		V_{SYS} = 5.5V, T_A = +85°C		0.1		
Interrupt Debounce Filter Timer		LOWSYS		16		ms

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C INTERFACE FOR STANDARD, FAST, AND FAST-MODE PLUS (Note 1)						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Setup Time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between START and STOP	t_{BUF}		0.5			µs
Pulse Width of Spikes that must be Suppressed by the Input Filter		(Note 1)		50		ns
I²C INTERFACE FOR HS-MODE PLUS (CB = 100pF) (Note 1)						
Clock Frequency	f_{SCL}	CB = 100pF			3.4	MHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
DATA Setup Time	$t_{VD:DAT}$		10			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter		(Note 1)		10		ns
I²C INTERFACE FOR HS-MODE PLUS (CB = 400pF) (Note 1)						
Clock Frequency	f_{SCL}	CB = 400pF			1.7	MHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
DATA Setup Time	$t_{VD:DAT}$		10			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter		(Note 3)		10		ns
CHGIN INPUT						
Operating Voltage			3.2		V_{OVLO}	V
CHGIN Overvoltage Threshold (Note 2)	$V_{CHGIN-OVLO}$	V_{CHGIN} rising	13.4	13.7	14	V
CHGIN Overvoltage-Threshold Hysteresis	$V_{CHGINH-OVLO}$	V_{CHGIN} falling		300		mV
CHGIN Overvoltage Delay (Note 1)	T_{D-OVLO}	V_{CHGIN} rising, 100mV overdrive, not production tested		10		µs
		V_{CHGIN} falling, 100mV overdrive, not production tested		20		
V_{BUSDET} to GND Minimum Turn-On Threshold Range (Note 2)	$V_{VBUSDET\_UVLO}$	$V_{VBUSDET}$ rising, 200mV hysteresis, programmable at 4.5V, 4.9V, 5.0V, and 5.1V (Note 2)	4.5		5.1	V
V_{BUSDET} to GND Minimum Turn-On Threshold Accuracy	$V_{VBUSDET\_UVLO}$	$V_{VBUSDET}$ rising, 4.5V setting	4.4	4.5	4.6	V
V_{BUSDET} to SYS Minimum Turn-On Threshold (Note 2)	$V_{VBUSDET2SYS}$	$V_{VBUSDET}$ rising, 50mV hysteresis when valid V_{BUSDET} input is detected	V_{SYS} + 0.12	V_{SYS} + 0.20	V_{SYS} + 0.28	V
V_{BUSDET} Turn-On Threshold Delay	T_{D-UVLO}	Not production tested		10		µs
CHGIN Adaptive Current Regulation Threshold Range (Note 3)	V_{CHGIN_REG}	Programmable at 4.2V, 4.6V, 4.7V, and 4.8V (Note 3)	4.2		4.8	V
CHGIN Current Limit Range		Programmable, 500mA default, factory programmable option of 100mA, production tested at 500mA, 1800mA, and 4000mA settings only	0.1		4	A
CHGIN Supply Current	I_{IN}	V_{CHGIN} = 2.4V, the input is undervoltage and R_{INSD} is the only loading		0.075		mA
		V_{CHGIN} = 5.0V, Charger disabled		0.17	0.5	
	I_{IN}	V_{CHGIN} = 5.0V, Charger enabled, V_{SYS} = V_{BATT} = 4.5V, (no switching, battery charged)		2.7	4	

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CHGIN} Input Current Limit	$I_{INLIMIT}$	V_{CHGIN} = 5.0V, Charger enabled, V_{BATT} = 3.8V, 500mA input current setting, T_A = +25ºC	462.5	487.5	500	mA
		V_{CHGIN}=5.0V, Charger enabled, V_{BATT} = 3.8V, 1800mA input current setting, T_A = +25°C	1710	1755	1800	
		V_{CHGIN} = 5.0V, Charger enabled, V_{BATT} = 3.8V, 1800mA input current setting, T_A = 0°C to +85°C	1667	1755	1843	
		V_{CHGIN} = 5.0V, Charger enabled, V_{BATT} = 3.8V, 4000mA input current setting, T_A = +25°C	3800	3900	4000	
		V_{CHGIN} = 5.0V, Charger enabled, V_{BATT} = 3.8V, 4000mA input current setting, T_A = 0°C to +85°C	3705	3900	4095	
CHGIN Self-Discharge Down to UVLO Time	t_{INSD}	Time required for the charger input to cause a 10µF input capacitor to decay from 6.0V to 4.3V		100		ms
CHGIN Input Self-Discharge Resistance	R_{INSD}			35		kΩ
CHGINOK to start switching	Tstart			26		ms
CHGIN Adaptive Voltage Regulation Threshold Accuracy	V_{CHGIN_REG}	4.8V setting	4.7	4.8	4.9	V
SWITCH IMPEDANCES AND LEAKAGE CURRENTS						
CHGIN to BYP Resistance	R_{IN2BYP}	Bidirectional		0.0144	0.04	Ω
CHGLX High-Side Resistance	R_{HS}			0.0327	0.1	Ω
CHGLX Low-Side Resistance	R_{LS}			0.0543	0.14	Ω
BATT to SYS Dropout Resistance	$R_{BAT2SYS}$			0.0128	0.04	Ω
CHGIN to BATT Dropout Resistance	R_{IN2BAT}	Calculation estimates a 0.04Ω inductor resistance (R_L) R_{IN2BAT} = R_{IN2BYP} + R_{HS} + R_L + $R_{BAT2SYS}$		0.0999		Ω
CHGLX Leakage Current		CHGLX = CHGPG or BYP, T_A = +25°C		0.01	10	µA
		CHGLX = CHGPG or BYP, T_A = +85°C		1		
BST Leakage Current		BST = 5.5V, T_A = +25°C		0.01	10	µA
		BST = 5.5V, T_A = +85°C		1		
BYP Leakage Current		V_{BYP} = 5.5V, V_{CHGIN} = 0V, V_{CHGLX} = 0V, charger disabled, T_A = +25°C		0.01	10	µA
		V_{BYP} = 5.5V, V_{CHGIN} = 0V, V_{CHGLX} = 0V, charger disabled, T_A = +85°C		1		

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS Leakage Current		V_{SYS} = 0V, V_{BATT} = 4.2V, charger disabled, T_A = +25°C		0.01	10	µA
		V_{SYS} = 0V, V_{BATT} = 4.2V, charger disabled, T_A = +85°C		1		
BATT Quiescent Current (I_{SYS} = 0A, I_{BYP} = 0A)	I_{MBAT}	V_{CHGIN} = 0V, V_{SYS} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is off, T_A = +25°C		20	30	µA
		V_{CHGIN} = 0V, V_{SYS} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is off, T_A = +85°C		20		
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is on, main-battery overcurrent protection disabled, T_A = +25°C		15.3		
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is on, main-battery overcurrent protection disabled, T_A = +85°C		15.3		
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is on, main-battery overcurrent protection enabled, T_A = +25°C		20		
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, external QBAT is on, main-battery overcurrent protection enabled, T_A = +85°C		20		
		V_{SYS} = 4.2V, V_{BATT} = 0V, charger disabled, T_A = +25°C		0.01	10	
		V_{SYS} = 4.2V, V_{BATT} = 0V, charger disabled, T_A = +85°C		1		
	I_{MBDN}	V_{CHGIN} = 5V, V_{BATT} = 4.2V, Q_{BAT} is off, main-battery overcurrent protection disabled, Charger is enabled but in its done mode, T_A = +25°C		3	10	
		V_{CHGIN} = 5V, V_{BATT} = 4.2V, Q_{BAT} is off, main-battery overcurrent protection disabled, Charger is enabled but in its done mode, T_A = +85°C		3		
CHARGER DC-DC BUCK						
Minimum ON Time	t_{ON-MIN}			75		ns
Minimum OFF Time	t_{OFF}			75		ns

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit (Note 5)	I_{LIM}	T_A = 0°C to +85°C, LSEL = 0 (0.47µH inductor option), production tested at I_{LIM} = 00 setting, I_{LIM} = 00 (3.00A out) (Note 4)	4.15	5.05	5.95	A
		T_A = 0°C to +85°C, LSEL = 0 (0.47µH inductor option), production tested at I_{LIM} = 00 setting, I_{LIM} = 01 (2.75A out) (Note 4)		4.75		
		T_A = 0°C to +85°C, LSEL = 0 (0.47µH inductor option), production tested at I_{LIM} = 00 setting, I_{LIM} = 10 (2.50A out) (Note4)		4.45		
		T_A = 0°C to +85°C, LSEL = 0 (0.47µH inductor option), production tested at I_{LIM} = 00 setting, I_{LIM} = 11 (2.25A out) (Note 4)		4.15		
		T_A = 0°C to +85°C, LSEL = 1 (1.0µH inductor option), production tested at I_{LIM} = 11 setting, I_{LIM} = 00 (3.00A out) (Note 4)		4.6		
		T_A = 0°C to +85°C, LSEL = 1 (1.0µH inductor option), production tested at I_{LIM} = 11 setting, I_{LIM} = 01 (2.75A out) (Note 4)		4.3		
		T_A = 0°C to +85°C, LSEL = 1 (1.0µH inductor option), production tested at I_{LIM} = 11 setting, I_{LIM} = 10 (2.50A out) (Note 4)		4		
		T_A = 0°C to +85°C, LSEL = 1 (1.0µH inductor option), production tested at I_{LIM} = 11 setting, I_{LIM} = 11 (2.25A out) (Note 4)	3	3.7	4.4	
REVERSE BOOST						
BYP Voltage Adjustment Range		Adjustable from 3V to 5.5V, min		3		V
		Adjustable from 3V to 5.5V, max (Note 1)		5.5		
Reverse Boost Quiescent Current	I_{BYP}	Not switching: output forced 200mV above its target regulation voltage		1150		µA
Reverse Boost Converter Maximum Output Current		3.6V <V_{BATT} production tested BATT = 3.6V	2			A
Reverse Boost BYP Voltage in OTG Mode	$V_{BYP.OTG}$	5.1V setting	4.94	5.1	5.26	V
CHGIN Output Current Limit	$I_{CHGIN.OTG.LIM}$	3.4V, T_A = +25ºC, OTG_ILIM = 00	500		550	mA
		3.4V, T_A = +25ºC, OTG_ILIM = 01	900		990	
		3.4V, T_A = +25ºC, OTG_ILIM = 10	1200		1320	
		3.4V, T_A = +25ºC, OTG_ILIM = 11	1500		1650	

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Boost Output Voltage Ripple (Note 1)		Discontinuous inductor current (i.e., skip mode) (Note 1)		±150		mV
		Continuous inductor current (Note 1)		±150		
CHARGER						
BATT Regulation Voltage Range	$V_{BATTREG}$	Programmable in 25mV steps (4-bits), production tested at 3.65V and 4.4V only	3.65		4.7	V
BATT Regulation Voltage Accuracy		3.65V and 4.7V settings, T_A = +25°C	-0.75		+0.75	%
		3.65V and 4.7V settings, T_A = 0°C to +85°C	-1		+1	
Fast-Charge Current Program Range		100mA to 3.15A in 50mA steps; production tested at 500mA and 3000mA settings	0.1		3.15	A
Fast-Charge Current Accuracy		Programmed currents ≥ 500mA, V_{BATT} > V_{SYSMIN} (short mode); production tested at 500mA and 3000mA settings, T_A = +25°C	-4		+4	%
		Programmed currents ≥ 500mA, V_{BATT} > V_{SYSMIN} (short mode); production tested at 500mA and 3000mA settings, T_A = 0°C to +85°C	-5		+5	
		Programmed currents ≥ 500mA, V_{BATT} < V_{SYSMIN} (LDO mode); production test at 800mA	-10		+10	
Fast-Charge Currents	I_{FC}	T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 3.0A	2880	3000	3120	mA
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 0.5A	480	500	520	
Low-Battery Prequalification Threshold	V_{PQLB}	V_{BATT} rising	2.8	2.9	3	V
Dead-Battery Prequalification Threshold	V_{PQDB}	V_{BATT} rising	1.9	2	2.1	V
Prequalification Threshold Hysteresis	V_{PQ-H}	Applies to both V_{PQLB} and V_{PQDB}		100		mV
Low-Battery Prequalification Charge Current	I_{PQLB}	Default setting = disabled	187.5	250	350	mA
Dead-Battery Prequalification Charge Current	I_{PQDB}		40	55	80	mA
Charger Restart Threshold Range	V_{RSTRT}	Adjustable, 100, 150, and 200	100	150	200	mV
Charger Restart Deglitch Time		10mV overdrive, 100ns rise time		130		ms

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Top-Off Current Program Range		Programmable from 100 to 350mA	100		350	mA
Top-Off Current Accuracy - Gain (Note 1)		Gain (Note 1)			5	%
Top-Off Current Accuracy - Offset (Note 1)		Offset (Note 1)			20	mA
Charge Termination Deglitch Time	t_{TERM}	2mV overdrive, 100ns rise/fall time		30		ms
Charger State Change Interrupt Deglitch Time	t_{SCIDG}	Excludes transition to timer fault state, watchdog timer state		30		ms
Charger Soft Start Time	t_{SS}	(Note 1)		1.5		ms
BAT TO SYS FET DRIVER						
BATT to SYS Reverse Regulation Voltage	V_{BSREG}	I_{BATT} = 10mA		30		mV
		I_{BATT} = 1A		60		
		Load regulation during the reverse regulation mode		30		mV/A
MINSYS Voltage Accuracy	V_{SYSMIN}	Programmable from 3.4V to 3.7V in 100mV steps, V_{BATT} = 2.8V; tested at 3.4V and 3.7V settings	-3		+3	%
Maximum SYS Voltage	V_{SYSMAX}	The maximum system voltage: V_{SYSMAX} = V_{BATREG} + $R_{BAT2SYS}$ x I_{BATT}, V_{BATREG} = 4.2V, I_{BATT} = 3.0A		4.245	4.32	V
		The maximum system voltage: V_{SYSMAX} = V_{BATREG} + $R_{BAT2SYS}$ x I_{BATT}, V_{BATREG} = 4.7V, I_{BATT} = 3.0A		4.745	4.82	
WATCHDOG TIMER						
Watchdog Timer Period	t_{WD}		80			s
Watchdog Timer Accuracy			-20	0	+20	%
CHARGE TIMER						
Prequalification Time	t_{PQ}	Applies to both low-battery prequalification and dead-battery prequalification modes		35		min
Fast-Charge Constant Current + Fast-Charge Constant Voltage Time	t_{FC}	Adjustable from 4hrs to 16hrs in 2 hour steps including a disable setting (production test at 4hrs and 16hrs)		8		hrs
Top-Off Time	t_{TO}	Adjustable from 0min to 70min in 10min steps		30		min
Timer Accuracy			-20		+20	%

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AVL FILTER						
Internal AVL Filter Resistance				12.5		Ω
THERMAL FOLDBACK						
Junction Temperature Thermal Regulation Loop Setpoint Program Range	T_{JREG}	Junction temperature when charge current is reduced; programmable from 85°C to 130°C in 5°C steps; default value is 115°C	85		130	°C
Thermal Regulation Gain	A_{TJREG}	The charge current is decreased 6.7% of the fast charge current setting for every degree that the junction temperature exceeds the thermal regulation temperature. This slope ensures that the full-scale current of 3.0A is reduced to 0A by the time the junction temperature is 20°C above the programmed loop set point. For lower programmed charge currents such as 500mA, this slope is valid for charge current reductions down to 100mA; below 100mA the slope becomes shallower but the charge current still reduced to 0A if the junction temperature is 20°C above the programmed loop set point		-150		mA/°C
BATTERY OVERCURRENT PROTECTION						
Programmable Battery Overcurrent Threshold Alarm	I_{BOVCR}	Overcurrent from BAT to SYS sensed through internal Q_{BAT} FET; programmable range from 3A to 9A in 0.5A/step; default to 4.5A	3		9	A
Battery Overcurrent Debounce Time	t_{BOVRC}	This is the response time for generating the overcurrent interrupt flag	3	6	10	ms
	t_{BOVRC2}	This is the response time from overcurrent interrupt flag to Q_{BAT} turn off		12		
Battery Overcurrent Protection Quiescent Current	I_{BOVRC}			(3 + I_{BATT})/2 2000		µA
System Power-Up Current	I_{SYSPU}		35	50	80	mA
System Power-Up Voltage	V_{SYSPU}	V_{SYS} rising, 100mV hysteresis	1.9	2.1	2.2	V
System Power-Up Response Time	t_{SYSPU}	Time required for circuit to activate from an unpowered state (i.e., main-battery hot insertion)		1		µs
SYSTEM SELF DISCHARGE WITH NO POWER						
BATT Self-Discharge Resistor				600		Ω
SYS Self-Discharge Resistor				600		Ω

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Self-Discharge Latch Time				300		ms
DETBATB, INOKB						
DETBATB Logic Threshold	V_{IH}	4% Hysteresis		0.8 x V_{IO}		V
Logic Input Leakage Current	$I_{DETBATB}$			0.1	1	µA
Output Low Voltage INOKB		I_{SINK} = 1mA			0.4	V
Output High Leakage INOKB		V_{SYS} = 5.5V, T_A = +25°C	-1	0	+1	µA
		V_{SYS} = 5.5V, T_A = +85°C		0.1		
THERMISTOR MONITOR (The thresholds are calculated for R25 = 10kΩ and β = 3435K)						
T1: THM Threshold, Cold, No Charge (0°C)	T1	V_{THM}/V_{AVL} rising, 2% hysteresis (thermistor temperature falling), default OTP option	71.68	74.18	76.68	%
T1: THM Threshold, Cold, No Charge (-7°C)	T1	V_{THM}/V_{AVL} rising, 2% hysteresis (thermistor temperature falling), OTP Programmable for -7°C	77.51	80.01	82.51	%
T4: THM Threshold, Hot, No Charge (60°C)	T4	V_{THM}/V_{AVL} falling, 2% hysteresis (thermistor temperature rising)	20.44	22.94	25.44	%
OVPDRV INPUT FET						
OVPENB Logic Output Low Threshold	$V_{OL, OVPENB}$	I_{SINK} = 200µA, V_{OVPENB} = GND			0.4	V
OVPENB Logic Output High Threshold	$V_{OH,OVPENB}$	I_{SOURCE} = 200µA, V_{OVPENB} = V_{AVL} = V_{BATT} = 3.6V	0.7 x V_{AVL}			V
CHARGER INDICATOR (GPIO)						
Output Low Voltage		I_{SINK} = 10mA			0.4	V
Output High Leakage		V_{SYS} = 5.5V; T_A = +25ºC	-1	0	+1	µA
		V_{SYS} = 5.5V; T_A = +85ºC		0.1		
ONKEY						
ONKEY Input Leakage Current	$ONKEY_{IL}$	0V < V_{ONKEY} < 5.5V, T_A = +25ºC	-1		+1	µA
ONKEY Rising Threshold	V_{ONKEYR}		0.3 x V_{BAT}			V
ONKEY Falling Threshold	V_{ONKEYF}				0.7 x V_{BAT}	V
ONKEY Debounce Timer	$ONKEY_{TDEB}$	From ONKEY press to buck-on and Q_{BAT} switch ON		800		ms
MASTER-SLAVE CHARGING						
SWI Output High Voltage	V_{OH}	I_{SINK} = 100µA	V_{SYS} - 0.4			V
SWI Output Low Voltage	V_{OL}	I_{SOURCE} = 100µA			0.4	V
SWI Rising Time	T_R	Note 1		200		ns

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWI Falling Time	T_F	Note 1		200		ns
SWI Input Frequency	F_{SWI}	Inferred to scan test		250		kHz
SWI Turn-On Detection Time	Twait_int	Inferred to scan test		200		µs
SWI Turn-Off Detection Time	Toff_dly	Inferred to scan test	50		90	µs
SWI High Time	TsH	Inferred to scan test	5	8	12	µs
SWI Low Time	TsL	Inferred to scan test	5	8	12	µs
SWI Signal Stop Indicate Time	Tstop	Inferred to scan test	100			µs
SWI Interrupt Trigger Current	I_{SWI_FAULT}	T_A = +25ºC			200	µA
SLAVE Input Low Level	V_{IL}	V_{SYS} = 3.6V; T_A= +25ºC			0.3 x V_{SYS}	V
SLAVE Input High Level	V_{IH}	V_{SYS} = 3.6V; T_A= +25ºC	0.7 x V_{SYS}			V
SLAVE Input Hysteresis	V_{IHYS}	V_{SYS} = 3.6V; T_A= +25ºC		0.05 x V_{SYS}		V
SLAVE Input Leakage Current	I_{SLAVE}	T_A = +25ºC	-1	0	+1	µA
CSP Input Leakage Current	I_{CSP}	T_A = +25ºC	-1	0	+1	µA
CSN Input Leakage Current	I_{CSN}	T_A = +25ºC	-1	0	+1	µA
ADAPTER TYPE DETECTION						
COMN1/COMP2 Load Resistor	R_{USB}	Load resistor on COMN1/COMP2	3	6.1	12	MΩ
VDP_SRC Voltage	V_{DP_SRC}	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
VDN_SRC Voltage	V_{DN_SRC}	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
VD33 Voltage	V_{DP}/DM_3p3 VSRC	Tested at zero load and at 365µA load	2.6		3.4	V
VDAT_REF Voltage	V_{DAT_REF}		0.25	0.3	0.35	V
VLGC Voltage	V_{LGC}		1.15	1.25	1.3	V
IDM_SINK Current	I_{DM_SINK}	Accurate over 0.15V to 3.6V	55	80	105	µA
IDP_SRC Current	I_{DP_SRC}	Accurate over 0V to 2.5V	5.5	8	10.5	µA
RDM_DWN Resistor	R_{DM_DWN}		17	20	23.3	kΩ
IWEAK Current	I_{WEAK}		0.004	0.15	0.3	µA
MVBUS25 Ratio	MVBUS25	Reference ratio for Special Charger as a percentage of MVBUS voltage	22.5	25	27.5	%
MVBUS47 Ratio	MVBUS47	Reference ratio for Special Charger as a percentage of MVBUS voltage	42.3	47	51.7	%
MVBUS75 Ratio	MVBUS75	Reference ratio for Special Charger as a percentage of MVBUS voltage	70	75	80	%

Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 5V to $V_{CHGIN-OVLO}$, V_{IO} = 1.8V, T_A = -40°C to +85°C. V_{SYS} = V_{SYS_X} = 3.6V, CHGIN = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB Charger Detect Time	t_{DPSRC_ON}	Option 1 (DChkTm = 0); inferred from SCAN	40	46	60	ms
Charger Detect Delay Time	$t_{CDDelay}$	Option 2 (DChkTm = 1); inferred from SCAN	450	500	550	ms
Charger Detect Current Delay	t_{VDPSRC_HICRNT}	Inferred from SCAN	46		60	ms
Debounce Time	t_{MDEB}	All comparators; inferred from SCAN	20	30	40	ms
DCD Debounce Time		Inferred from SCAN	36	40	44	ms
DCD Time Out		Inferred from SCAN	1.8	2	2.2	s
ENUEN Logic Output Low Threshold	$V_{OL, ENUEN}$	I_{SINK} = 200µA, V_{AVL} = V_{BATT} = 3.6V			0.4 x V_{AVL}	V
ENUENB Logic Output High Threshold	$V_{OH, ENUEN}$	I_{SOURCE} = 200µA, V_{AVL} = V_{BATT} = 3.6V	0.7 x V_{AVL}			V

Electrical Characteristics—SAFEOUT LDO

(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = -40°C to +85°C, unless otherwise noted, T_A for typical values = +25°C.))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SAFEOUT LDO						
Output Voltage (Default ON)		5.0V < V_{CHGIN} < 5.5V, I_{OUT} = 10mA, SAFEOUT = 01 (default)	4.65	4.9	5.15	V
		SAFEOUT = 00		4.85		
		SAFEOUT = 10		4.95		
		SAFEOUT = 11		3.3		
PSRR (Note 1)		V_{CHGIN} = 5.5, f = 100kHz, C_{OUT} = 1µF		60		dB
Maximum Output Current			60			mA
Output Current Limit				150		mA
Dropout Voltage		V_{CHGIN} = 5V, I_{OUT} = 60mA		120		mV
Load Regulation		V_{CHGIN} = 5.5V, 30µA < I_{OUT} < 30mA		50		mV
Quiescent Supply Current		Not production tested		72		µA
Output Capacitor for Stable Operation (Note1)		0µA < I_{OUT} < 30mA, MAX ESR = 50mΩ	0.7	1		µF
Internal Off-Discharge Resistance				1200		Ω

Note 1: Design guidance only, not tested during final test.

Note 2: The CHGIN input must be less than V_{OVLO} and greater than both V_{CHGIN_UVLO} and $V_{CHGIN2SYS}$ for the charger to turn on.

Note 3: Input filters on the SDA and SCL inputs suppress noise spikes of less than 50ns.

Note 4: Production tested in charger DC-DC low-power mode.

Note 5: Production tested to ¼ of the threshold with LPM bit = 1 (¼ FET configuration).

Note 6: Symmetrical error is the sum of odd-order errors in the measured values at two inputs symmetrical around zero. For example, ISERR_0.3A = (Error 0.3A - Error -0.3A)/2/0.3A x 100.

Note 7: Total current measurement error is the sum of the symmetrical and asymmetrical errors. Fuel gauge accuracy is sensitive to asymmetrical error but insensitive to symmetrical error.

Note 8: Current and ratiometric measurement errors are production tested at V_{SYS} = 3.7V and guaranteed by design at V_{SYS} = 2.8V and 4.5V.

Note 9: Asymmetrical error is the sum of even-order errors in the measured values at two inputs symmetrical around zero. For example, IAERR_0.3A = (Error 0.3A + Error -0.3A)/2.

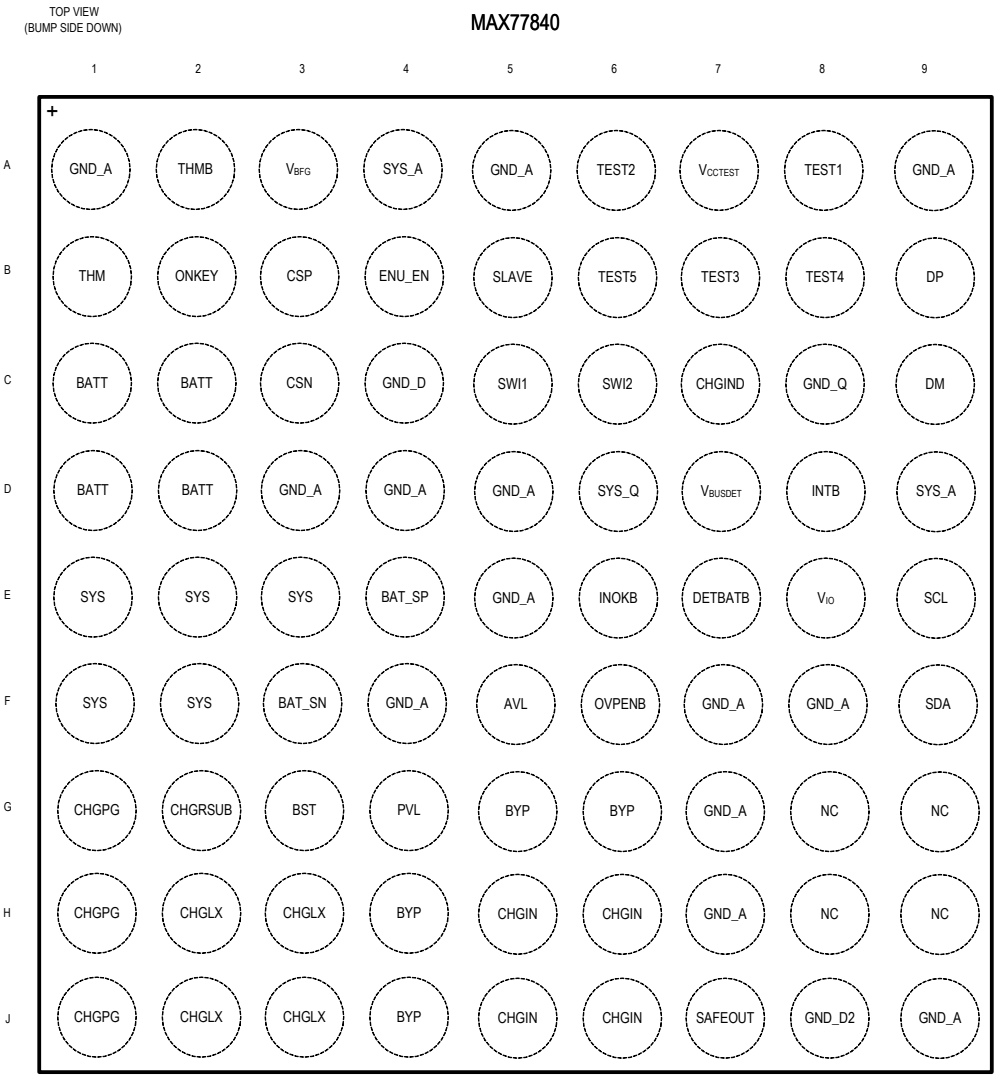
Electrical Characteristics—ModelGauge m5 Fuel Gauge

(V_{SYS} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE CHANNEL						
V_{BATT} Measurement Error	V_{GERR}	V_{BATT} = 2.8V to 4.5V, T_A = +25°C	-7.5		+7.5	mV
		T_A = -40°C to +85°C	-20		+20	
V_{BATT} Measurement Resolution	V_{LSB}			1.25		mV
V_{BATT} Measurement Range	V_{RANGE}		2.8		4.98	V
CURRENT CHANNEL						
Current Measurement Resolution	I_{LSB}			1.25		mA
Current Measurement Range	I_{RANGE}			±3.6		A
Current Measurement Offset	I_{OERR}	Long term average at zero input current		±0.25		mA
Current Measurement Symmetrical Error	I_{SERR}	(Notes 6, 7, and 8)		2		%
Current Measurement Asymmetrical Error	I_{AERR}	±3000mA (Notes 7, 8, and 9)	-150		+150	mA
		±1000mA (Notes 7, 8, and 9)	-20		+20	
		±300mA (Notes 7, 8, and 9)	-9.5		+9.5	

Pin Configuration

MAX77840



WLP
(81 BUMP 9x9 ARRAY 0.4mm PITCH)

NC PINS ARE UNCONNECTED.
ALL TEST PINS (TEST 1-5 AND V_{CCTEST} SHOULD BE GROUNDED IN THE END-USE APPLICATION.
*TOP VIEW = WAFER BACK-SIDE VIEW (BUMPS NOT VIEWABLE)

Pin Description

PIN	NAME	FUNCTION
POWER AND GND		
D6	SYS_Q	Quiet SYS Input
A4, D9	SYS_A	Analog SYS Input
A1, A5, A9, D3, D4, D5, E5, F4, F7, F8, G7, H7, J9	GND_A	Analog Ground. Short to GND_D, GND_D2, and GND_Q.
C4	GND_D	Digital Ground Connection. Short to GND_D2, GND_A, and GND_Q.
C8	GND_Q	Quiet Ground Connection. Short to GND_A, GND_Q, GND_D, and GND_D2.
J8	GND_D2	Digital Ground Connection. Short to GND_D, GND_A, and GND_Q.
H8, H9, G8, G9	NC	No Connect. Leave unconnected on the PCB.
CHGR		
E1, E2, E3, F1, F2	SYS	System Power Connection. Connect system loads to this node. Bypass with 2x10µF ceramic capacitors from SYS to CHGPG ground plane.
H5, H6, J5, J6	CHGIN	High Current Charger Input. Bypass to CHGPG with a 2.2µF/25V ceramic capacitor. This node is also served as OTG output.
G5, G6, H4, J4	BYP	CHGIN Bypass Pin. This pin can see up to OVP limit. This pin is also input to switching charger as well as the output of reverse boost converter when the charger is operating in 'reverse boost' mode. Bypass with 2x10µF/25V ceramic capacitors from BYP to CHGPG ground plane.
H2, H3, J2, J3	CHGLX	Charger Switching Node. Connect the inductor between CHGLX and SYS.
G3	BST	High-Side FET Driver Supply. Bypass BST to CHGLX with a 0.1µF ceramic capacitor.
G1, H1, J1	CHGPG	Charger Power Ground Connection. Star connection to GND_A ground plane.
G2	CHGRSUB	Substrate Charger Ground Connection. Connect this pin to GND_A ground plane.
F5	AVL	Analog Voltage Level. Output of on-chip 5V LDO used to power on-chip, low-noise circuits. Bypass with a 2.2µF/10V ceramic capacitor to GND_A ground plane. Powering external loads from AVL is not recommended, other than pulldown resistors
G4	PVL	Internal Bias Regulator High Current Output Bypass Pin. Supports internal noisy and high current gate drive loads. Bypass to CHGPG plane with a minimum 10µF/10V ceramic capacitor.
C7	CHGIND	Charging Status Indication GPIO Output. Open-drain and active-low option to connect to a LED to a pullup rail with a current limit resistor as charging indicator.
C1, C2, D1, D2	BATT	Battery Power Connection. Connect to the positive terminal of a single-cell (or parallel cell) Li-ion battery. Bypass BATT to CHGPG ground plane with a 10µF ceramic capacitor.
E4	BAT_SP	Battery Positive Differential Sense Connection. If not used, connect to BATT pin on the IC side.
F3	BAT_SN	Battery Negative Differential Sense Connection. If not used, connect to GND_A on the IC side.
E6	INOKB	Charger Input Valid, Active-Low Logic Output Flag. Open-drain output indicates when valid voltage is present at both CHGIN and SYS.
E7	DETBATB	Battery Detection Active-Low Input. Connect this pin to the ID pin on the battery pack. If DETBATB is pulled below 80% of the externally applied V_{IO} voltage, this is an indication that the battery is present and that the charger starts when valid CHGIN is present. If DETBATB is driven high to V_{IO} voltage or left unconnected, this is an indication that the battery is not present and that the charger does not start. DETBATB is pulled high to V_{IO} pin through an off-chip pullup resistor. Ground this pin when DETBATB function is not used.
B2	ONKEY	ONKEY Switch Input.

Pin Description (continued)

PIN	NAME	FUNCTION
OVP DETECT		
F6	OVPENB	Push-Pull Output. Use this pin to enable the external over-voltage protection IC. when V_{BUSDET} > $V_{CHGIN_}$UVLO, OVPENB toggles from H to L.
D7	V_{BUSDET}	BUS Voltage Sensing Input Pin, Used for CHGIN UVLO Detection. Connect a 1µF ceramic capacitor between this pin and CHGPG (ground).
MASTER-SLAVE (Reserved)		
B5	SLAVE	Connect to GND.
C5	SWI1	Leave unconnected.
C6	SWI2	Leave unconnected.
B3	CSP	Connect to BATT.
C3	CSN	Connect to BATT.
SAFEOUT		
J7	SAFEOUT	Safeout LDO Output. Default 4.9V and on when CHGIN power is valid. Bypass with a 1µF ceramic capacitor to GND_A.
E8	V_{IO}	Digital I/O Supply Input for I^2C Interface
I^2C		
F9	SDA	I^2C Serial Data.
E9	SCL	I^2C Serial Clock.
CLOGIC		
D8	INTB	Interrupt Output. Active-low open-drain output. Connect to system IO voltage through a 200kΩ resistor.
CHGR DET		
C9	DM	USB Detection Negative Input. Connect to D- on mini/micro USB connector.
B9	DP	USB Detection Positive Input. Connect to D+ on mini/micro USB connector.
B4	ENU_EN	Logic Output. When bit 6 in register 0x06 (DisENU) = 0, if SDP/CDP is detected, ENU_EN pin stays in logic high. ENU_EN pin is kept at logic low for other adapter types. When bit 6 in register 0x06 (DisENU) = 1, ENU_EN pin always stays at logic low.
FUEL GAUGE		
B1	THM	Thermistor Connection. Determine the battery temperature using the ratio-metric measurement.
A2	THMB	Pullup Voltage for THM Pin Pullup Resistor That Can Be Switched Off to Save Power
A3	V_{BFG}	1.8V Power Supply Output for Fuel Gauge. Bypass V_{BFG} with a 0.1µF ceramic capacitor. V_{BFG} is not intended to power external circuitry.
TEST		
A8	TEST1	Test I/O Pin. Ground this pin in the application.
A6	TEST2	Test I/O Pin. Ground this pin in the application.
B7	TEST3	Test I/O Pin. Ground this pin in the application.
B8	TEST4	Test I/O Pin. Ground this pin in the application.
B6	TEST5	Test I/O Pin. Ground this pin in the application.
A7	V_{CCTEST}	Test Mux Supply. Ground this pin in the application.

Detailed Description

Switching Charger

The MAX77840 includes a full-featured switch-mode charger for a one-cell lithium-ion (Li+) or lithium-polymer (Li-polymer) battery. As shown in Figure 1, the current limit for CHGIN input is independently programmable from 0A to 4.0A in 33.3mA steps allowing the flexibility for connection to either an AC-to-DC wall charger or a USB port. Default CHGIN current limit is set at 500mA.

The synchronous switch-mode DC-DC converter utilizes a 2MHz or 4MHz switching frequency which is ideal for portable devices because it allows the use of small components while eliminating excessive heat generation. The DC-DC has both a buck and a boost mode of operation. When charging the main battery, the converter operates as a buck. The DC-DC buck operates from a 3.2V to 13.4V source and delivers up to 3.15A to the battery. The battery charge current is programmable from 0A to 3.15A. As a boost converter, the DC-DC uses energy from the main-battery to boost the voltage at BYP. The boosted BYP voltage is useful to provide the supply to the USB OTG voltage.

The MAX77840 supports the capability to place an external FET from SYS to BATT while allowing to make the best use of the limited adapter power and the battery's power at all times to supply up to 3.15A continuous current (4A peak) from the buck to the system. (Additionally, supplement mode provides additional current from the battery to the system up to $4.5A_{RMS}$ (typ). Adapter power that is not used for the system goes to charging the battery.

Maxim Integrated's proprietary process technology allows for low $R_{DS(ON)}$ devices in a small solution size. The total dropout resistance from adapter power input to the battery is 99.9mΩ (typ) assuming that the inductor has 0.04Ω of DCR. This 99mΩ typical dropout resistance allows for charging a battery up to 3.15A from a 5V supply.

A multitude of safety features ensures reliable charging. Features include a charge timer, watchdog, junction thermal regulation, over/under voltage protection, and short-circuit protection.

The BATT to SYS switch has overcurrent protection (see the *System Protections* section for more information).

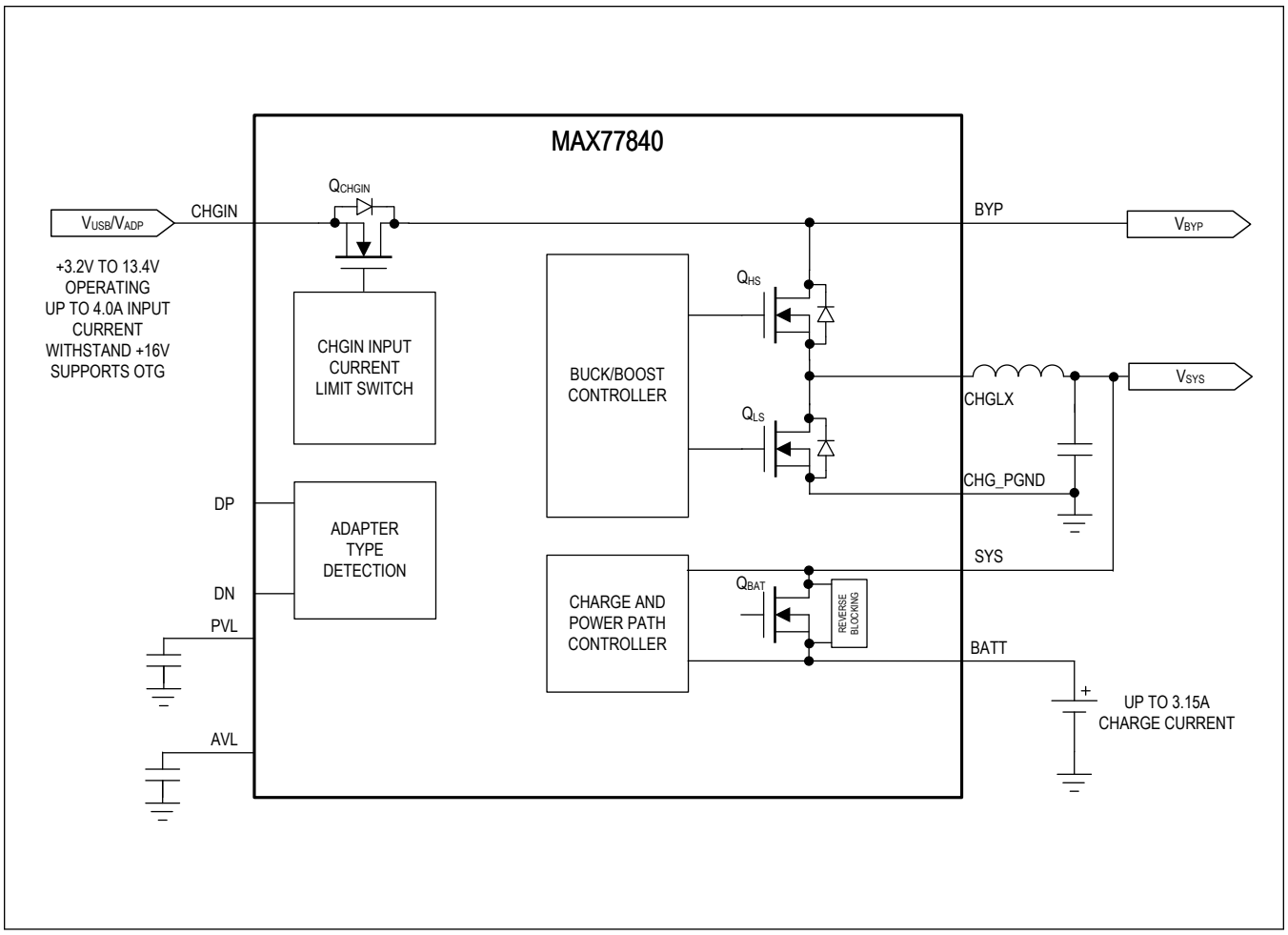


Figure 1. Switching Charger Block Diagram

USB Data Contact Detection

The USB plugs are designed in such a way that the power pins make contact before the data pins make contact when the USB plug is inserted into the receptacle. This allows the circuits to be powered up by V_{BUS} source before data pins are connected. To ensure that the data pins have made contact, BC1.2 makes it optional to allow the data pins to be pre-bias so at least one of the two data pins changes state when USB data pins are connected. After the detection of data pin state change, it can check the type of port being attached. The MAX77840 charger detection supports USB Battery Charger Detection Rev 1.2. The device detects battery-charging sources as defined in BC1.2 (SDP, DCP, CDP) and can also detect Apple 500mA and 1A and Sony 500mA adapters.

The MAX77840 offers ENU_EN pin which asserts high when SDP or CDP is detected. ENU_EN can be used to enable/disable an external USB switch in order to connect/disconnect D+ and D- pins between the USB connector and the MAX77840 and allows the portable device to start enumeration with the host processor.

Features

The MAX77840 supports full USB Battery Charger Detection Rev 1.2 with the following features:

- Data Contact Detection (DCD)
- Detects All USB Defined Sources:
  - Standard USB Port
  - Charging Downstream Port
  - Dedicated Charging Port
- Detects Apple Power Adapters
- Detects Sony/OPPO Adapters
- Manual Restart of Charger Detection

Table 1. Supported Adapter Types

CHGTYP[2:0]	DESCRIPTION	DEFAULT INPUT CURRENT VALUE (A)	COMMENT
000	Nothing connected		
001	USB cable attached	0.5	1 bit to select between 500mA and 100mA. Register 0x07, Bit 0 = USBLowSp '0' CHGDET_CHGIN_ILIM = 0.5A (0x0F) when USB 2.0/SDP detected '1' CHGDET_CHGIN_ILIM = 0.1A (0x01) when USB 2.0/SDP detected
010	Charging downstream port	1.5	1 bit to set between 1500mA and 500mA. Register 0x07, Bit 1 = CDP_500mA '0' CHGDET_CHGIN_ILIM = 1.5A (0x2D) when ChgTyp = CDP '1' CHGDET_CHGIN_ILIM = 0.5A (0x0F) when ChgTyp = CDP
011	Dedicated charger	4.0	1 bit to set to between 1500mA and MAX Register 0x07, Bit 2 = DCP_IN_MAX '0' CHGDET_CHGIN_ILIM = 1.5A (0x2D) when ChgTyp = DCP '1' CHGDET_CHGIN_ILIM = MAX (0x7F) when ChgTyp = DCP
100	Apple 500mA charger	0.5	
101	Apple 1A or 2A charger	2	1 bit to set between 2A and 1A Register 0x07, Bit 3 = Apple_1A '0' CHGDET_CHGIN_ILIM = 2.0A (0x3C) when ChgTyp = 101 '1' CHGDET_CHGIN_ILIM = 1.0A (0x1E) when ChgTyp = 101
110	Sony 0.5A/ OPPO	0.5 or Max if OPPO enabled and fulfilled.	1 bit to enable OPPO charger detection. Register 0x07, Bit 4 = OPPOEn '1' enables OPPO detection. Sets CHGIN current limit to max if DM stays > 3.3V for additional 300ms. '0' disables OPPO detection. When set to 0, charger type 110 = 100 (Sony 0.5A)
111	Reserved		

DP and DM Detection Functions

The internal USB full speed/low speed transceiver is connected to the bidirectional data pins DP and DM. These pins are ESD protected up to ±15kV. Connect these pins to a USB Type-B custom connector through external 20Ω series resistors. The MAX77840 provides an automatic switchable 1.5kΩ pullup resistor for D- for low speed and D+ for high speed.

Table 2. Data Contact Detection Registers

ADDRESS (HEX)	REGISTER NAME	RESET TYPE	RESET VALUE	B7	B6	B5	B4	B3	B2	B1	B0
0x01	CHGDET_INT	S	0x00	RSVD	RSVD	RSVD	VDNMon	DxOVP	DCDTmr	ChgDetRun	ChgTyp
0x02	CHGDET_STATUS	S	0x00	RSVD	VDNMon	DxOVP	DCDTmr	ChgDetRun	ChgTyp<2:0>		
0x03	CHGDET_INT_MASK	S	0x1F	RSVD	RSVD	RSVD	VDNMonM	DxOVPM	DCDTmrM	ChgDetRunM	ChgTypM
0x04	CHGDET_CHGIN_ILIM	VBUS Invalid	0x00	RSVD	CHGDET_CHGIN_ILIM[6:0]						
0x05	CHGDET_CNTRL1	S	0x2C	CDPDet	RSVD	DCDCpl	CDDelay	DCD2sCt	DCDEn	ChgTypMan	RSVD
0x06	CHGDET_CNTRL2	S	0x0A	RSVD	DisENU	NoAutoIBUS	NoBCComp	DxOVPEn	RSVD	SFOutOrd	SFOutAsrt
0x07	CHGDET_CNTRL3	S	0x04	RSVD	RSVD	RSVD	OPPOEn	Apple 1A	DCP_IN_MAX	CDP_500mA	USBLowSp
0x08	CHGDET_QCNTRL	VBUS Invalid	0x00	ENUCtrlEn	ENU_EN	RSVD	DPDNVdEN	DPVd[1:0]		DNVd[1:0]	

Note: Reset Type S = Reset by SYS UV or VBUS UV

Data Contact Detection Registers

CHGDET_INT (0x01)

NAME		FUNCTION	ADDR	TYPE	RESET
CHGDET_INT		Charger Detect interrupt	0x01	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
7:5	R/C	RSVD	000	Reserved	
4	R/C	VDNMon	0	Indicates Change VDNMon Status Bit Valid only if DPDNVdEn is enabled 0 = VDNMon status has not changed 1 = VDNMon status voltage has changed	
3	R/C	DxOVP	0	COMN1/COMP2 OVP Interrupt 0 = No Interrupt 1 = Interrupt	
2	R/C	DCDTmr	0	DCD Timer Interrupt 0 = No Interrupt 1 = Interrupt	
1	R/C	ChgDetRun	0	Charger Detection Running Status Interrupt 0 = No Interrupt 1 = Interrupt	
0	R/C	ChgTyp	0	Charge Type Interrupt 0 = No Interrupt 1 = Interrupt	

CHGDET_STATUS (0x02)

NAME		FUNCTION	ADDR	TYPE	RESET
CHGDET_STATUS		Charger Detect Status	0x02	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R	RSVD	0	Reserved	
6	R	VDNMON	0	Indicates Status of V_{DAT_REF} Voltage Comparator on COMN1. Valid only if DPDNVdEn is enabled 0 = COMN1 < V_{DAT_REF} 1 = COMN1 > V_{DAT_REF}	
5	R	DxOVP	0	COMN1/COMP2 OVP Interrupt. If a high voltage greater than 3.6V is applied to COMN1 or COMP2 when DxOVPEn = 1, this interrupt asserts. In an OVP condition (DxPVP = 1), the charger detection state machine is forced to off if it is currently running and ChgTyp is set to 000. 0 = COMN1 and COMP2 1 = COMN1 or COMP2	
4	R	DCDTmr	0	Data Contact Detect Time Wait 0 = Data Contact Detection timer not expired or not running 1 = Data Contact Detection running for greater than 2s	
3	R	ChgDetRun	0	Charger Detection State Machine Running 0 = Not Running 1 = Running	
2:0	R	ChgTyp[2:0]	0	Charger Type 000 = Nothing connected 001 = USB cable attached (500mA) 010 = Charging downstream port (1.5A) 011 = Dedicated charger (1.5A) 100 = Apple 500mA charger 101 = Apple 1A or 2A charger (2A) 110 = Special charger (3.3V on D+ and D-) 111 = Reserved	

CHGDET_INT_MASK (0x03)

NAME		FUNCTION	ADDR	TYPE	RESET
CHGDET_INT_MASK		Charger Detect Interrupt Mask	0x03	O	0xFF
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:5	R/W	RSVD	111	Reserved	
4	R/W	VDNMonM	1	VDNMon Comparator Interrupt Mask 1 = Mask 0 = Not Masked	
3	R/W	DxOVPM	1	COMN1/COMP2 OVP interrupt Mask 1 = Mask 0 = Not Masked	
2	R/W	DCDTmrM	1	DCD Timer Interrupt Mask 1 = Mask 0 = Not Masked	
1	R/W	ChgDetRunM	1	Charger Detection Running Status Interrupt Mask 1 = Mask 0 = Not Masked	
0	R/W	ChgTypM	1	Charge Type Interrupt Mask 1 = Mask 0 = Not Masked	

CHGDET_CHGIN_ILIM (0x04)

NAME		FUNCTION	ADDR	TYPE	RESET
CHGDET_CHGIN_ILIM		Charger Detect Chargin Ilimit	0x04	Reset by VBUS_VALID	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
7	R	RSVD	0	Reserved	
6:0	R	CHGIN_ILIM[6:0]	0000000	7 Bits Adjustment from 100mA to 4A Setting 0x01 to 0x03 = 100mA Setting 0x04 to 0x78 = Increments of 33mA Setting 0x78 to 0x7F = 4A	

CHGDET_CNTRL1 (0x05)

NAME		FUNCTION	ADDR	TYPE	RESET
CHGDET_CNTRL1		Charger Detect Control 1	0x05	O	0x2C
BIT	MODE	NAME	RESET	DESCRIPTION	
7	R/W	CDPDet	0	USB Charger Downstream Detection Method 0 = Use VDP_SRC to drive D- 1 = Use weak pullup method	
6	R/W	RSVD	0	Reserved	
5	R/W	DCDCpl	1	Data Contact Detection Wait Time 0 = 2000ms 1 = 900ms	
4	R/W	CDDelay	0	Sets Time for Charger Detection Start After Valid VBUS is Found 0 = 0ms 1 = 500ms	
3	R/W	DCD2sCt	1	Automatically Exit Data Contact Detection when 2s Interrupt is Set 0 = Stay in DCD until normal exit 1 = Always exit DCD when 2s interrupt asserts	
2	R/W	RFU	1	Reserved	
1	R/W	ChgTypMan	0	Charger Type Manual Detection. Set to 1 to force the internal logic to open the COM switches and perform a charger type detection. After the detection state machine completes, this bit resets to 0. 0 = Disabled	
0	R/W	RSVD	0	Reserved	

CHGDET_CNTRL2 (0x06)

NAME		FUNCTION	ADDR	TYPE	RESET
CHGDET_CNTRL2		Charger Detect Control 2	0x06	O	0x0A
BIT	MODE	NAME	RESET	DESCRIPTION	
7	R/W	RSVD	0	Reserved	
6	R/W	DisENU	0	Disable Enumeration 0 = ENU_EN depends on charger type. Asserts to high when SDP/CDP found. 1 = Disable enumeration, ENU_EN stays at low.	
5	R/W	NoAutoIBUS	0	Disabling of Automatic Input Current Limit From Adapter Detection 0 = Automatically determined using adapter detection. 1 = Current limit setting controlled manually through I^2C.	

NAME		FUNCTION	ADDR	TYPE	RESET
CHGDET_CNTRL2		Charger Detect Control 2	0x06	O	0x0A
BIT	MODE	NAME	RESET	DESCRIPTION	
4	R/W	NoBCComp	0	Non-BC1.2 Compliance 0 = BC1.2 compliance, 0.6V is forced on D+ for dedicated charging port. 1 = D+ is at Hi-Z after detection regardless of dedicated charging port.	
3	R/W	DxOVPEn	1	Enable COMN1/COMP2 OVP Monitoring. COMN1 and COMP2 are always protected against OVP faults but the interrupt monitor is not enabled unless this bit is set to 1. 0 = Disabled 1 = Enabled	
2	R/W	DPDNVdEn	0	Enable Direct Voltage Control on COMN1/COMP2 0 = Disabled 1 = Enabled. Forces all switches connected to COMN1/COMP2 to Hi-Z and enables DPVd and DNVd voltage control	
1	R/W	SFOutOrd	1	SFOUT Override Control 0 = Force SFOUT to off 1 = SFOUT is automatically controlled by VB voltage present and SFOutAsrt option.	
0	R/W	SFOutAsrt	1	Time When SFOUT Asserts 0 = SFOUT asserts only after a complete run of the charger detection state machine or after a correct detection of a factory cable 1 = SFOUT asserts after a valid VBUS voltage detection with no wait	

CHGDET_CNTRL3 (0x07)

NAME		FUNCTION	ADDR	TYPE	RESET
CHGDET_CNTRL3		Charger Detect Control 3	0x07	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
7:4	R/W	RSVD	0000	Reserved	
3	R/W	Apple 1A	0	Apple 1A Charger 0 = Apple 2A Charger 1 = Apple 1A Charger	
2	R/W	DCP_IN_MAX	0	Dedicated Charger Max Current 0 = DCP 1.5A Charging Current 1 = DCP Max Charging Current	
1	R/W	CDP_500mA	0	Charging Downstream Port 500mA Current 0 = CDP 1.5A Charging Current 1 = CDP 500mA Charging Current	
0	R/W	USBLowSp	0	USB Low Speed 0 = USB high speed port, 500mA current 1 = USB low speed port, 100mA current	

CHGDET_QCNTRL (0x08)

NAME		FUNCTION	ADDR	TYPE	RESET
CHGDET_QCNTRL		Charger Detect QC Control	0x08	Reset by VBUS_VALID	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	ENUCtrlEn	0	Sets to '1' to take over control of ENU_EN pin.	
6	R/W	ENU_EN	0	Enable ENU Only when both ENUCtrl_EN = 1 and ENU_EN = 1, the ENU_EN pin sets to 1, else, it is controlled through the internal adaptor detection state machine (ENU_EN pin goes to 1 only in SDP/CDP found)	
5	R/W	RSVD	0	Reserved	
4	R/W	DPDVdEn	0	Enable Direct Voltage Control on DP/DM. 0 = Disabled 1 = Enabled. Forces all switches connected to DM/DP to Hi-Z and enables DPVd and DNVd voltage control	
3:2	R/W	DPVd[1:0]	00	Voltage Drive on COMP2 00 = Hi-Z 01 = GND 10 = VDN_SRC (typ 0.6V) 11 = VD33 (typ 3.3V)	
1:0	R/W	DNVd[1:0]	00	Voltage Drive on COMN1 00 = Hi-Z 01 = GND 10 = VDP_SRC (typ 0.6V) 11 = VD33 (typ 3.3V)	

ENUCTRLEN (BIT 7)	ENU_EN (BIT 6)	ENU_EN (PIN B4)
0	x	Low
1	0	Low
1	1	High

ModelGauge m5 Fuel Gauge

The MAX77840 is a high-performance battery charger that integrates the Maxim Integrated proprietary ModelGauge m5 algorithm in the same chip. Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance, however they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated thus causing the reported capacity error to increase over time (which then requires periodic corrections). The ModelGauge m5 algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms since tiny continual corrections are distributed over time. The ModelGauge m5 adopts a mixing algorithm that combines the VFG capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way, the VFG capacity result is used to continuously make small adjustments to the battery state thus canceling the coulomb-counter drift. The MAX77840 includes improved age adaptation, improved SOC accuracy to empty, and increased temperature measurement. The device provides two methods for reporting the age of the battery: reduction in capacity and cycle odometer. Moreover, the device provides precision measurements of current, voltage, and temperature. Details are discussed in the *ModelGauge m5 Details* section.

Detailed Description—Charger

Smart Power Selector (SPS)™

The Smart Power Selector architecture includes a network of internal switches and control loops that distributes energy among CHGIN, WCIN, BYP, SYS, and BATT. Figure 2 shows the Smart Power Selector switches QCHGIN, QHS, QLS, and QBAT.

Switch and Control Loop Descriptions

CHGIN Input Switch: QCHGIN is used for input current sensing. It turns completely on when a valid CHGIN is available and does not provide forward blocking. SPS control loops regulate CHGIN input current and voltage.

DC-DC Switches: QHS and QLS are the DC-DC switches that can operate as a buck (step-down) or a boost (step-up). When operating as a buck, energy is delivered from BYP to SYS. When operating as a boost, energy is delivered from SYS to BYP. SPS control loops monitor the DC-DC switch current, the SYS voltage, and the BYP voltage.

Battery-to-System Switch: QBAT controls the battery charging and discharging. Additionally, QBAT allows the battery to be isolated from the system (SYS). SPS control loops regulate battery current and voltage.

Control Bits

MODE[3:0] configures the Smart Power Selector. MINVSYS[1:0] sets the minimum system voltage. VBYPSET[6:0] sets the BYP regulation voltage target. B2SOVRC[2:0] sets the battery overcurrent protection threshold.

Energy Distribution Priority

With a valid external power source (buck operation):

- The external power source is the primary source of energy.
- The battery is the secondary source of energy.
- Energy delivery to SYS is the highest priority.
- Any energy that is not required by SYS is available to the battery charger.

With no valid external power source:

- The battery is the source of energy.
- Energy delivery to SYS is the highest priority.
- Any energy not required by SYS is available for BYP or CHGIN (when boost or OTG is enabled).

BYP Regulation Voltage

When the DC-DC converter is enabled in boost only mode (MODE[3:0] = 0x08), the voltage from BYP to ground (V_{BYP}) is regulated to VBYPSET[6:0]. When the DC-DC converter is enabled in one of its USB OTG modes (MODE[3:0] = 0x0A or 0x0E or 0x0F), V_{BYP} is set for 5.1V (V_{BYPOTG}). When the DC-DC converter is off or in one of its buck modes (MODE[3:0] = 0x00 or 0x04 or 0x05) and there is a valid power source at CHGIN, $V_{BYP} = V_{CHGIN} - I_{CHGIN} \times R_{QCHGIN}$. When the DC-DC converter is off and there is no valid power source at CHGIN, BYP is connected to SYS with an internal 200Ω resistor. This 200Ω resistor keeps BYP biased at V_{SYS} and allows for the system to draw very light loads from BYP. If the system loading on BYP is more than 1mA, then the DC-DC converter should be operated in boost mode. Note that the inductor and the high-side switch's body diode are in parallel with the 200Ω from SYS to BYP.

SYS Regulation Voltage

When the DC-DC converter is enabled as a buck and the charger is disabled (MODE[3:0] = 0x04), V_{SYS} is regulated to V_{BATREG} (CHG_CV_PRM) and QBAT is off. When the DC-DC converter is enabled as a buck and the charger is enabled but in a non-charging state such as done, watchdog suspend, or timer fault (MODE[3:0] = 0x05 and not charging), V_{SYS} is regulated to V_{BATREG} (CHG_CV_PRM) and QBAT is off.

When the DC-DC converter is enabled as a buck and charging in prequalification, fast-charge, or top-off modes (MODE[3:0] = 0x05 and charging), V_{SYS} is regulated to V_{SYSMIN} when the $V_{BATT} < V_{SYSMIN}$; in this mode, the QBAT switch acts like a linear regulator and dissipates power [$P = (V_{SYSMIN} - V_{BATT}) \times I_{BATT}$]. When $V_{BATT} > V_{SYSMIN}$, then $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$; in this mode, the QBAT switch is closed.

In all of the previous modes, if the combined SYS and BYP loading exceeds the input current limit, then the battery provides supplemental current to the system and V_{SYS} is regulated to V_{BATT} - V_{BSREG}. If the fuel gauge requests battery information (voltage and current) during supplement mode, then the QBAT switch is closed (V_{SYS} = V_{BATT} - I_{BATT} x $R_{BAT2SYS}$) during the fuel gauge sampling period. If the fuel gauge requests continuous samples from the battery during supplement mode, then the QBAT switch eventually opens when I_{BATT} decreases below 40mA. When the DC-DC converter is enabled in boost or OTG modes (MODE[3:0] = 0x08, 0x0A, 0x0C, 0x0D, 0x0E, or 0x0F), then the QBAT switch is closed and V_{SYS} = V_{BATT} - I_{BATT} x $R_{BAT2SYS}$.

Charger States

The MAX77840 utilizes several charging states to safely and quickly charge batteries. Figure 2 shows an exaggerated view of a Li+/Li-Poly battery progressing through the following charge states when there is no system load and the die and the battery are close to room temperature: prequalification → fast-charge → top-off → done.

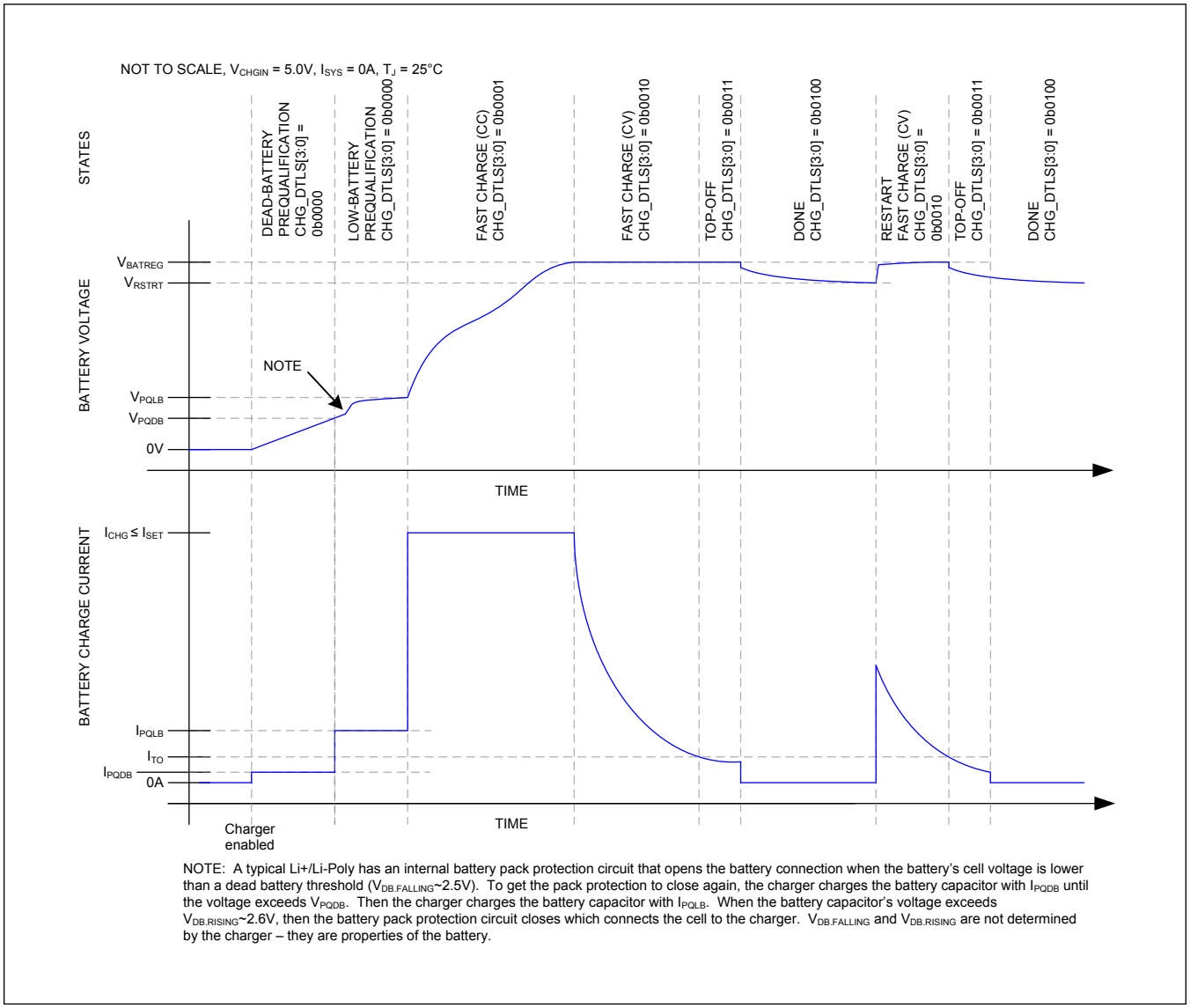


Figure 2. MAX77840 Typical Charging Profile

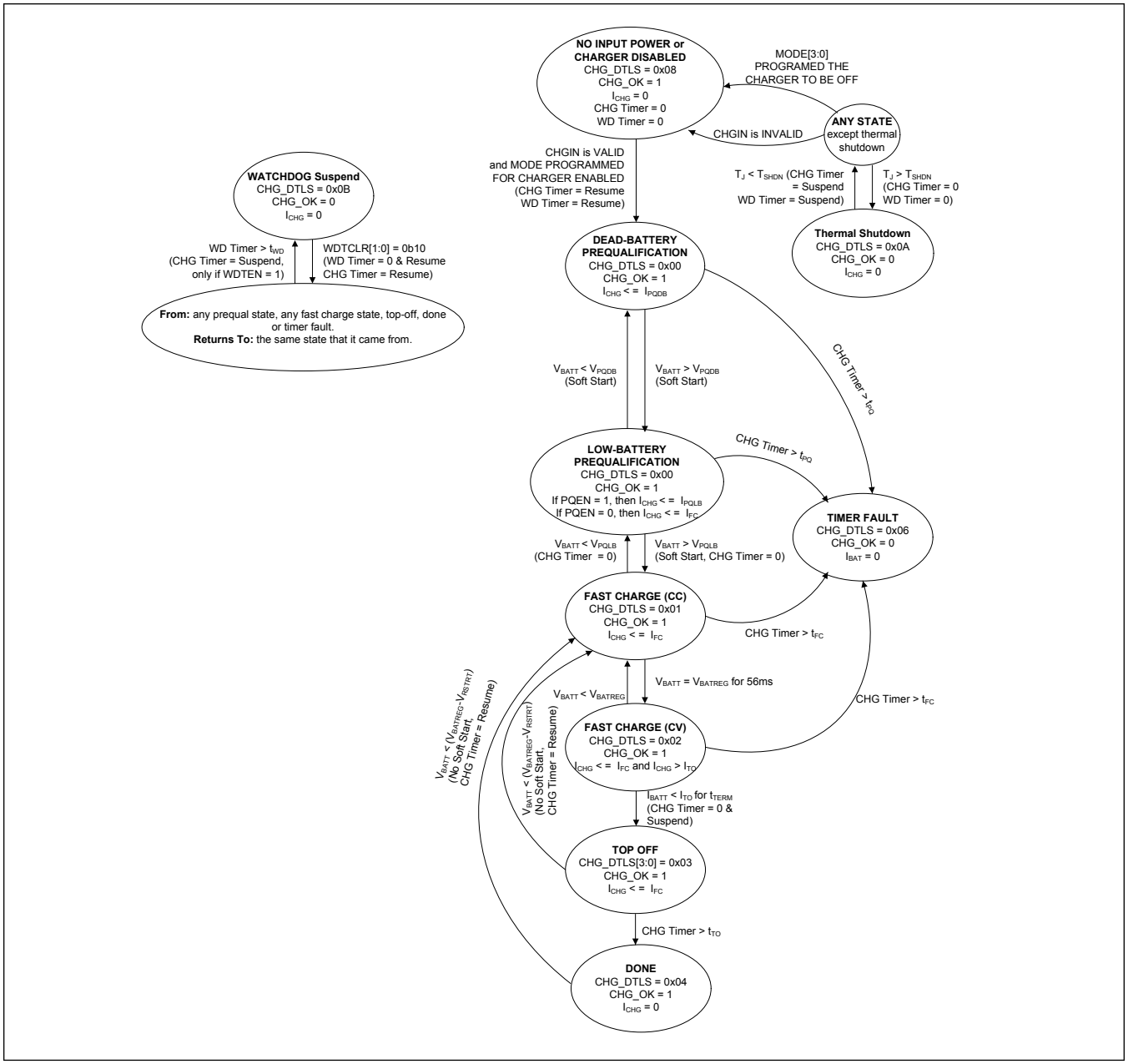


Figure 3. MAX77840 Charger State Diagram

No Input Power or Charger Disabled State

From any state shown in Figure 3 except thermal shutdown, the no input power or charger disabled state is entered whenever the charger is programmed to be off or the charger input CHGIN is invalid. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set, and CHG_DTLS[3:0] is set to 0x08. While in the no input power or charger disabled state, the charger current is 0mA, the watchdog and charge timers are forced to 0, and the power to the system is provided by either the battery or the adapter. When both battery and adapter power are available, the adapter provides primary power to the system and the battery contributes supplemental energy to the system if necessary. To exit the no input power or charger disabled state, the charger input must be valid and the charger must be enabled.

Dead-Battery Prequalification State

The dead-battery prequalification state occurs when the main-battery voltage is less than VPQDB. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set, and CHG_DTLS is set to 0x00. In the dead-battery prequalification state, charge current into the battery is I_{PQDB}.

Note that the dead-battery prequalification state works with battery voltages down to 0V. The low 0V operation typically allows this battery charger to recover batteries that have an “open” internal pack protector. Typically, a pack’s internal protection circuit opens if the battery has detected an overcurrent, undervoltage, or overvoltage condition. When a battery with an “open” internal pack protector is used with this charger, the low-battery prequalification mode current flows into the 0V battery; this current raises the pack’s terminal voltage to the point where the internal pack protection switch closes.

Note that a normal battery typically stays in the low-battery prequalification state for several minutes or fewer; therefore, a battery that stays in low-battery prequalification for longer than t_{PQ} might be experiencing a problem.

Fast-Charge Constant Current State

The fast-charge constant current (CC) state occurs when the main-battery voltage is greater than the low-battery prequalification threshold and less than the battery regulation threshold ($V_{PQLB} < V_{BATT} < V_{BATREG}$). After being in the fast-charge CC state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set and CHG_DTLS = 0x01.

In the fast-charge CC state the current into the battery is less than or equal to I_{FC}. Charge current can be less than I_{FC} for any of the following reasons:

- The charger input is in input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The battery charger dissipates the most power in the fast-charge constant current state. This power dissipation causes the internal die temperature to rise. If the die temperature exceeds TREG, I_{FC} is reduced to maintain preset die temperature and interrupt is created.

Fast-Charge Constant Voltage State

The fast-charge constant voltage (CV) state occurs when the battery voltage rises to V_{BATREG} from the fast-charge CC state. After being in the fast-charge CV state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set and CHG_DTLS = 0x02.

In the fast-charge CV state, the battery charger maintains V_{BATREG} across the battery and the charge current is less than or equal to I_{FC}. As shown in Figure 2, charger current decreases exponentially in this state as the battery becomes fully charged.

TOP-OFF State

The top-off state can only be entered from the fast-charge CV state when the charger current decreases below I_{TO} for t_{TERM}. After being in the top-off state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set and CHG_DTLS = 0x03. In the top-off state the battery charger tries to maintain V_{BATREG} across the battery and typically the charge current is less than or equal to I_{TO}.

DONE State

The battery charger enters its done state after the charger has been in the top-off state for t_{TO}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is cleared and CHG_DTLS = 0x04.

In the done state, the charge current into the battery (I_{CHG}) is 0A. In the done state, the charger presents a very low load (I_{MBDN}) to the battery. If the system load presented to the battery is low (<100µA), then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the restart threshold (V_{RSTRT}) and the charger state machine transitions back into the fast-charge CV state. There is no soft start (di/dt limiting) during the done to fast-charge state transition.

Timer Fault State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. The charge timer prevents the battery from charging indefinitely. The time that the charger can remain in each of its prequalification states is t_{PQ}. The time that the charger can remain in the fast-charge CC and CV states is t_{FC}, which is programmable with FCHGTIME. Finally, the time that the charger is in the top-off state is t_{TO} which is programmable with TO_TIME. Upon entering the timer fault state, a CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS = 0x06.

In the timer fault state, the charger is off. The charger can exit the timer fault state by programming the charger to be off and then programming it to be on again through the MODE bits. Alternatively, the charger input can be removed and reinserted to exit the timer fault state.

Thermal Shutdown State

The thermal shutdown state occurs when the battery charger is in any state and the junction temperature (T_J) exceeds the device's thermal shutdown threshold (TSHDN). When T_J is close to TSHDN, the charger folds back the input current limit to 0A so that the charger and inputs are effectively off. Upon entering this state, CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS = 0x0A.

In the thermal shutdown state, the charger is off and timers are suspended. The charger exits the temperature suspend state and returns to the state it came from once the die temperature has cooled. The timers resume once the charger exits this state.

Power States

The MAX77840 provides five power states and one no power state (see register description CHG_CNFG_00 [3:0]). Under power limited conditions, the Power Path feature maintains SYS and USB-OTG loads at the expense of battery charge current. In addition, the battery will supplement the input power when required. As shown in Figure 3, transitions between power states are initiated by detection/removal of valid power sources, OTG events, and undervoltage conditions. Details of the BYP and SYS voltages are provided for each state.

1. NO INPUT POWER, *MODE = undefined*: No input adapter or battery is detected. The charger and system is off. Battery is disconnected and charger is off.
2. BATTERY-ONLY, *MODE = 0x00*: The adapter voltage is invalid, outside the input voltage operating range (QCHGIN = off). Battery is connected to power the SYS load (QBAT = on), and Boost is ready to power OTG (Boost = standby), see Figure 4.

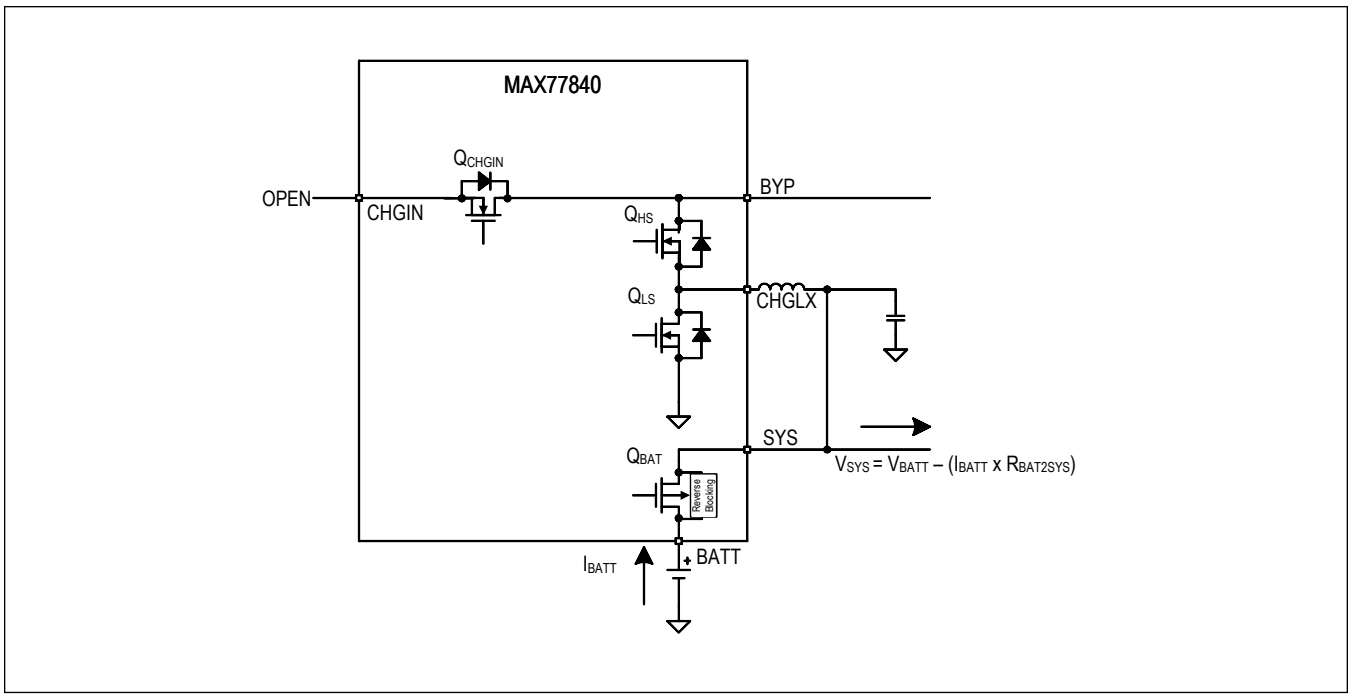


Figure 4. Battery-Only

3. BATTERY-BOOST, ***MODE = 0x08***: The adapter voltage is invalid, outside the input voltage operating range (Q_{CHGIN} = off). Battery is connected to power the SYS load(Q_{BAT} = on), and charger is operating in Boost mode (Boost = on), see Figure 5.

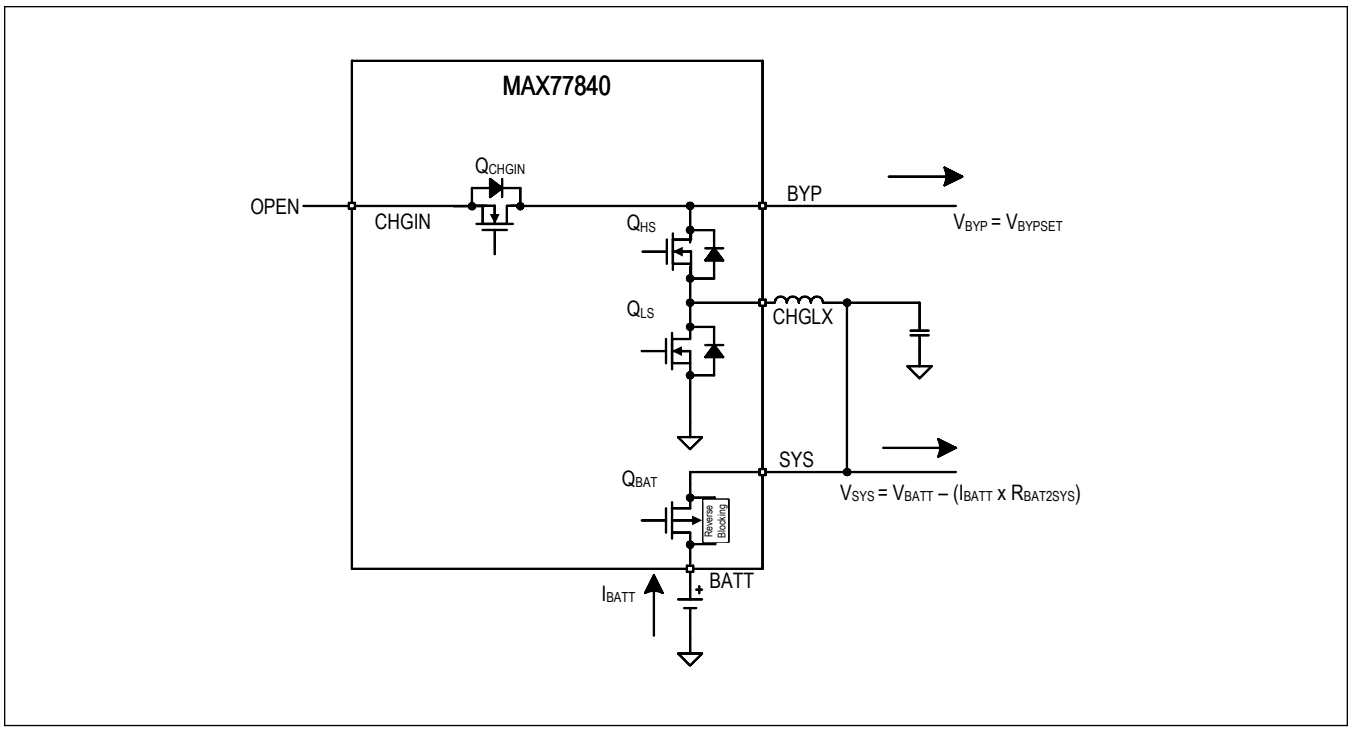


Figure 5. Battery-Boost

4. BATTERY-BOOST (OTG), MODE = 0x0A: OTG is active (Q_{CHGIN} = on). Battery is connected to support SYS and OTG loads (Q_{BAT} = on), and charger is operating in Boost mode (Boost = on), see Figure 6.

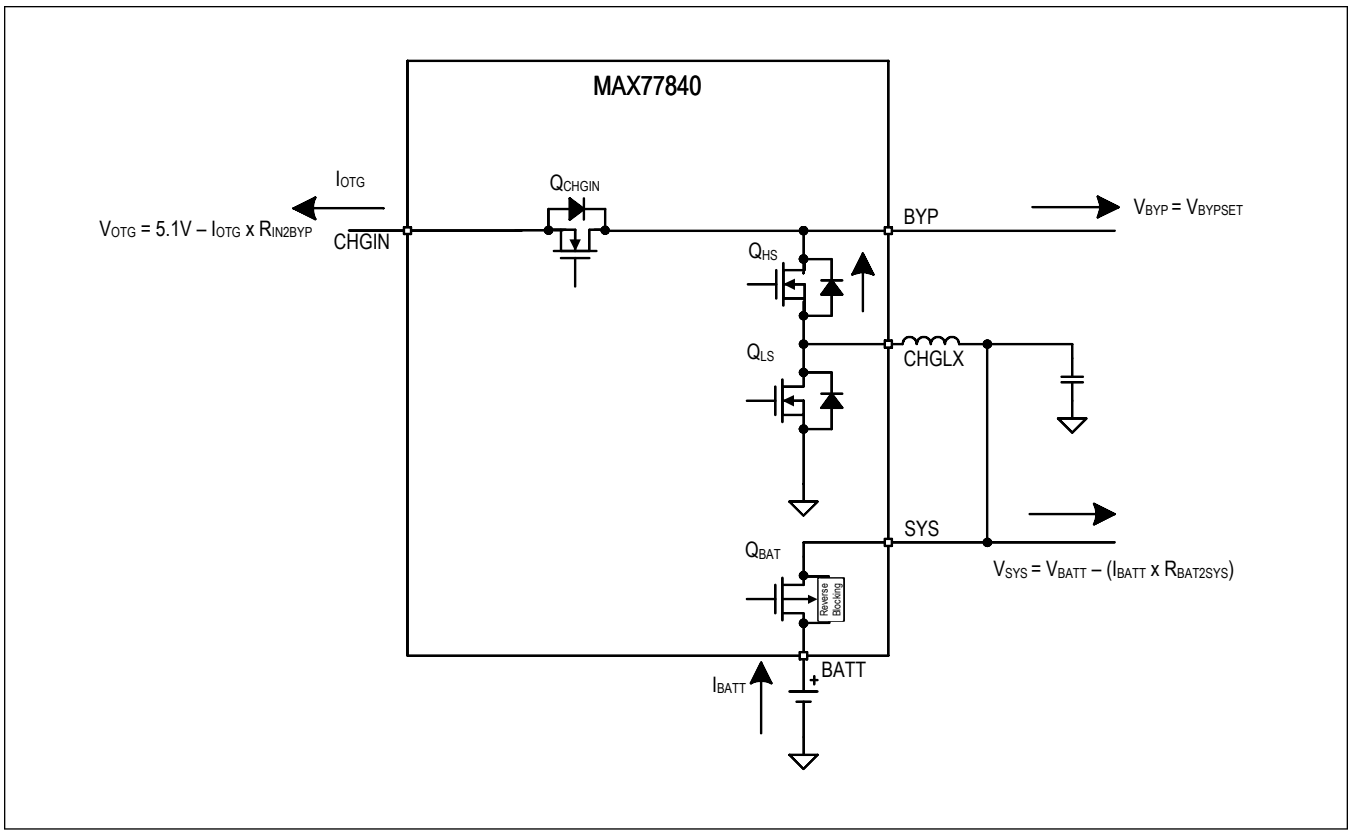


Figure 6. Battery-Boost (OTG)

5. NO CHARGE-BUCK, MODE = 0x0C: The adapter is detected within the input voltage operating range (Q_{CHGIN} = on). Battery is disconnected (Q_{BAT} = off) and the charger is operating in buck mode powering SYS node, see Figure 7.

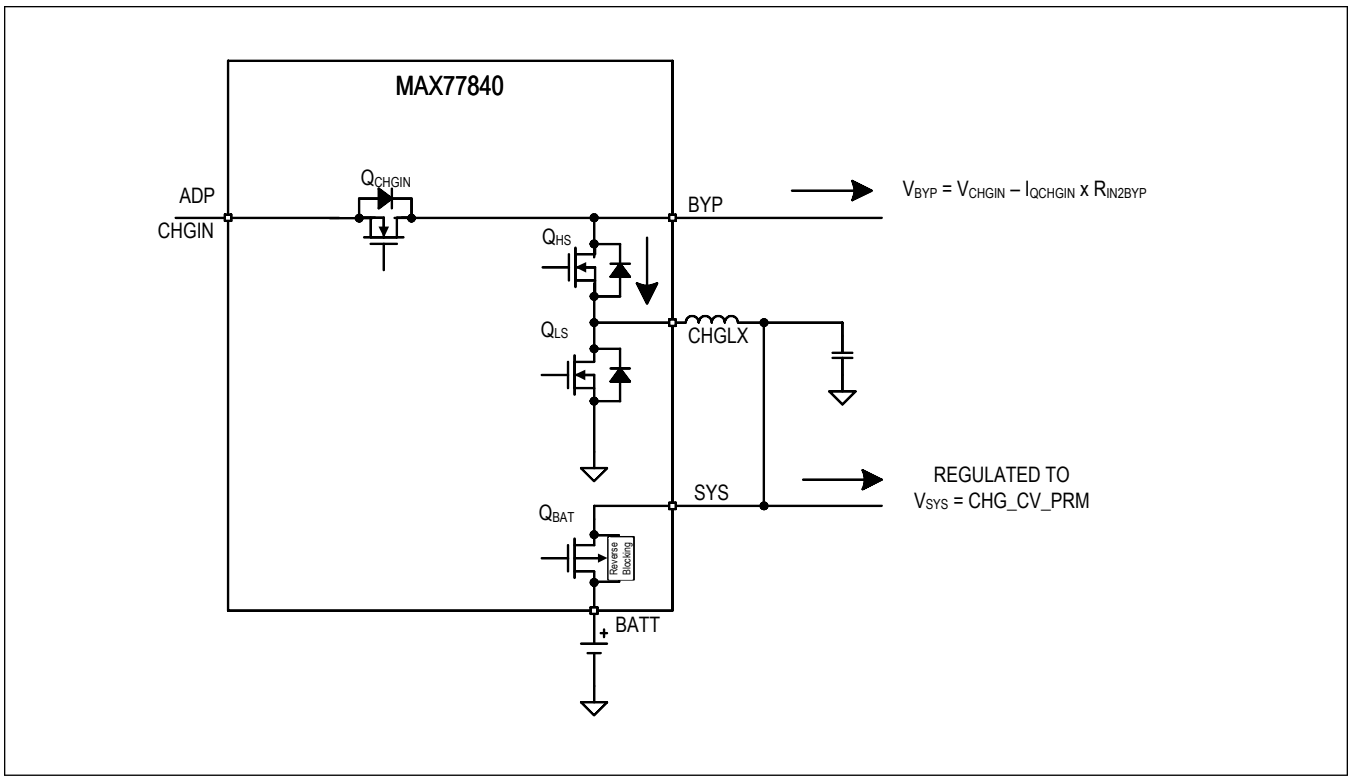


Figure 7. No Charge-Buck

6. CHARGE-BUCK, MODE = 0x0D: The adapter is detected within the input voltage operating range (Q_{CHGIN} = on). Battery is connected in charge mode (Q_{BAT} = on) and charger is operating in buck mode, see Figure 8.

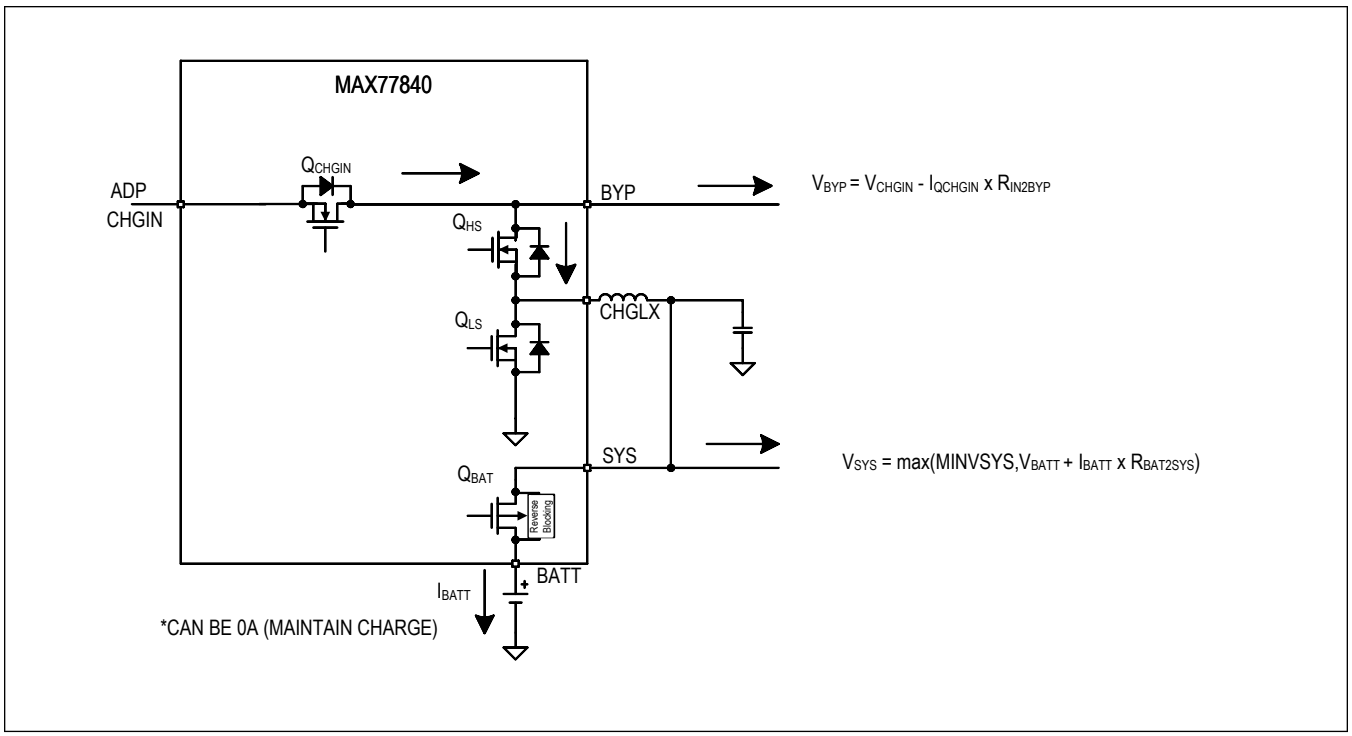


Figure 8. Charge-Buck

Watchdog Timer

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. The watchdog timer protects the battery from charging indefinitely if the host hangs or otherwise cannot communicate correctly. The watchdog timer is disabled by default with WDTEN = 0. To use the watchdog timer feature, enable the feature by setting WDTEN = 1. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01.

Battery Differential Voltage Sense

As shown in the *Typical Application Circuit*, the BAT_SP and BAT_SN pins are differential remote sense lines for the main battery. To improve accuracy and decrease charging times, the battery charger voltage sense is based on the differential voltage between BAT_SP and BAT_SN.

Reverse Boost and On-the-Go (OTG) Modes

The DC-DC converter topology of the MAX77840 allows it to operate as a forward buck converter or as a reverse boost converter.

The modes of the DC-DC converter are controlled with the MODE bits in CHG_CNFG_00 register. When MODE = 0x08 or 0x09, the DC-DC converter operates in reverse boost mode allowing it to source current from the battery to BYP. No current is sourced to CHGIN because CHGIN to BYP FET is turned off. The QBAT FET is turned on to allow the battery to support the system while the BYP voltage is regulated to V_{BYPSET}.

When MODE = 0x0A and DIS_CD_CTRL (CHG_CNFG_00[7]) is enabled, the DC-DC converter operates in OTG mode allowing it to source current from the battery to CHGIN and BYP (the term OTG is based on the Universal Serial Bus' On-The-Go concept). The switch from BYP to CHGIN is closed and the converter regulates V_{CHGIN} and V_{BYP} to $V_{BYP.OTG}$ (5.1V, typ) and V_{BYPSET} is ignored. The current through the BYP to CHGIN switch is limited to the value programmed by OTG_ILIM. The four OTG_ILIM options allow the DC-DC converter to supply up to 1500mA to an external load. When the OTG mode is selected, the unipolar CHGIN transfer function measures current going out of CHGIN. When OTG mode is not selected, the unipolar CHGIN transfer function measures current going into CHGIN.

If the external OTG load at CHGIN exceeds ICHGIN.OTG.ILIM, then a BYP_I interrupt is generated, BYP_OK = 0, and BYP_DTLS = 0bxxx1. In response to an overload at CHGIN during OTG mode operation, the BYP to CHGIN switch is latched off. The BYP to CHGIN switch automatically attempts to retry in approximately 300ms; if the overload at CHGIN persists, then the switch toggles on and off with approximately 1ms on and approximately 300ms off.

Input Validation

As shown in Figure 3, the charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following three criteria to be valid:

1. CHGIN must be above V_{CHGIN_UVLO}.
2. CHGIN must be below its overvoltage-lockout threshold ($V_{CHGIN-OVLO}$).
3. CHGIN must be above the system voltage by $V_{CHGIN2SYS}$.

The CHGIN input generates a CHGIN_I interrupt when its status changes. The input status can be read from the CHGIN_OK and CHGIN_DTLS register bits. Interrupts can be masked with CHGIN_M.

Input Current Limit

The default settings of the CHGIN_ILIM and MODE control bits are such that when a charge source is applied to CHGIN, the MAX77840 turns its DC-DC converter on in BUCK mode, limits V_{SYS} to V_{BATREG}, and limits the charge source current to 500mA. All control bits are reset on global shutdown.

Input Voltage Regulation Loop

An input-voltage regulation loop allows the charger to be well behaved when it is attached to a poor-quality power source (CHGIN pin). The loop improves performance with relatively high resistance charge sources that exist when long cables are used or devices are charged with non-compliant USB hub configurations. Additionally, this input-voltage regulation loop improves performance with current-limited adapters. If the MAX77840's input current limit is programmed above the current limit threshold of given adapter, the input voltage loop allows the MAX77840 to regulate the input voltage at the current limit of the adapter. Finally, the input-voltage regulation loop allows the MAX77840 to perform well with adapters that have poor transient load response times.

After operating with the input-voltage regulation active, a BYP_I interrupt is generated, BYP_OK is cleared, and BYP_DTLS = 0b1xxx. To optimize input power when working with a current limited charge source, monitor the BYP_DTLS while decreasing the input current limit. When the input current limit is set below the limit of the adapter, the input voltage rises. Although the input current limit is lowered, more power can be extracted from the input source when the input voltage rises.

Charging Status Indicator (CHGIND)

The MAX77840 offers an active-low, open-drain GPIO output on the CHGIND pin. This pin can be used as the charging status indicator when connected to a pullup rail with a LED and a current limiting resistor. The charging indicator feature can be enabled or disabled with LEDEN I^2C register bit, as shown in Figure 9.

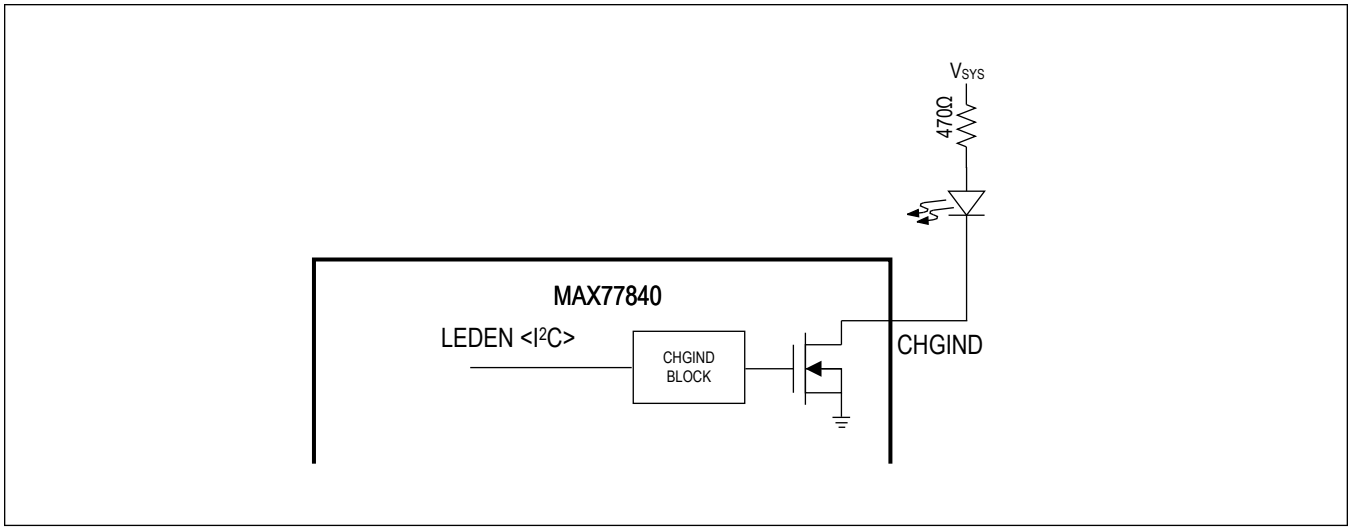


Figure 9. Charging Indicator Circuit

Dead Battery Charging State
When charging is in dead battery state, the CHGIND LED is set up to blink with 50ms ON time in a 1s period.

Battery Prequalification Charging State
When charging is in prequalification state, the CHGIND LED is set up to blink with 50ms ON time in a 1s period.

Fast-Charge Constant Current State
When charging is in the fast-charge constant current state, the CHGIND LED is enabled with 100% ON time.

Fast-Charge Constant Voltage State
When charging is in the fast-charge constant voltage state, the CHGIND LED is enabled with 100% ON time.

Top-Off State
When charging is in the top-off state, the CHGIND LED is set up to blink with 50% ON time in a 1s period.

DONE State
When charging is in the DONE state, the CHGIND LED is disabled.

Battery Detect Input Pin (DETBATB)

The DETBATB is a digital input pin for detecting battery presence. If DETBATB is pulled below 80% of the V_{IO} pin voltage, this indicates that the main battery is present and the battery charger starts with a valid CHGIN. If DETBATB is left unconnected or equal to the V_{IO} voltage, this indicates that the battery is not present and charging is disabled. The DETBATB pin is typically tied to the ID pin of a battery pack. In the absence of a battery ID pin, the DETBATB pin input can be sourced from an application processor that verifies battery presence externally. Alternatively, if battery detection is not necessary, the pin can be kept shorted to ground, as shown in Figure 10. In this scenario, the BATP_DTLS bit states that the battery is always present, and the charging operation cannot be interrupted.

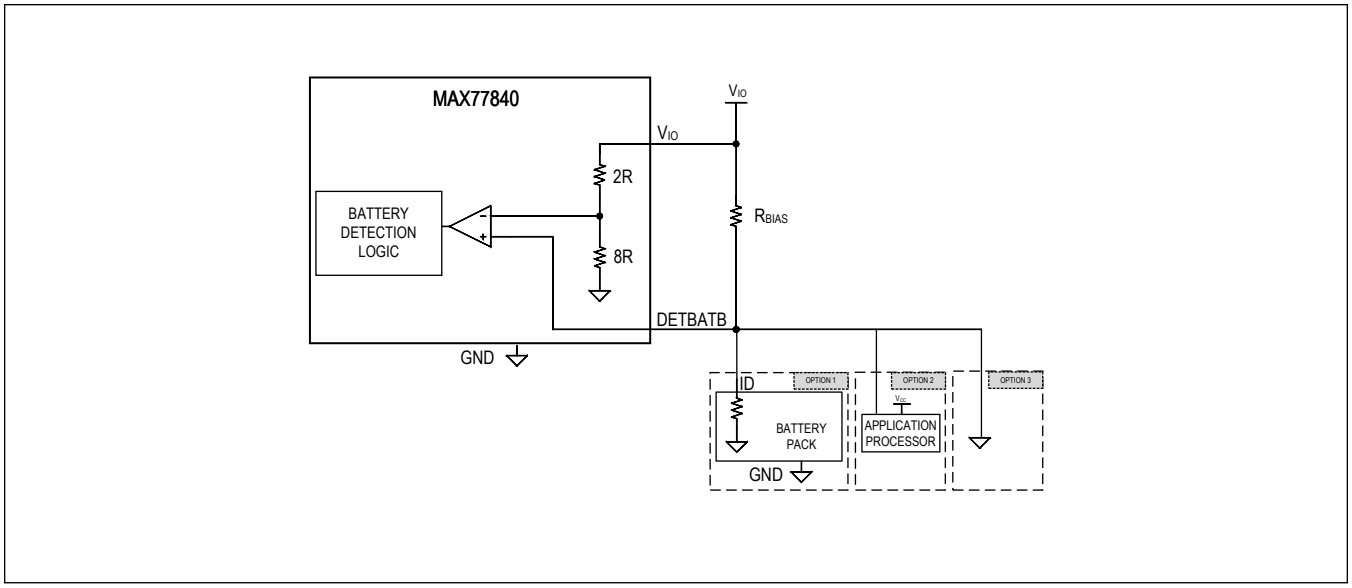


Figure 10. Battery Present Detection Circuit

Interrupt Pin (INTB)

INTB is the hardware pin used to notify the host processor that one or more of the unmasked interrupt bits has toggled. Masking the interrupt by setting INT_MASK_ bit to 1 prevents the INTB from asserting. The INTB pin deasserts (pulled high by off-chip pullup) as soon as the read sequence of the last INT_ register that contains an active interrupt starts. Fuel Gauge interrupts are cleared by setting new threshold values.

The application processor reads the interrupts in two steps. First, the AP reads the INTSRC register; this is a read-only register that indicates which functional block is generating the interrupt (i.e., charger and Fuel Gauge). Depending on the result of the read, the next step is to read the actual interrupt registers pertaining to the functional block.

For example, if the application processor reads 0x02 from register 0x22: INTSRC, it means that the top-level block has an interrupt generated. The next step is to read register 0x24: SYSTEM Interrupt in order to understand the source of the interrupt.

System Protections

V_{SYS} Undervoltage Lockout ($V_{SYSUVLO}$)

When SYS voltage falls below $V_{SYSUVLO}$, the device's Type O registers are reset.

When the charger input is valid, the battery is present, and

$V_{PQDB} < V_{SYS} < V_{SYS\_UVLO}$,

QBAT is on and SYS is shorted to BATT.

When

$0 < V_{SYS} < V_{PQDB}$,

QBAT is off but the charger pulls up SYS from BATT with a constant current of 50mA.

When the charger input is invalid, the battery is present, and

$V_{PQDB} < V_{SYS} < V_{SYSUVLO}$,

Q_{BAT} is on and SYS is shorted to BATT.

When

$0 < V_{SYS} < V_{PQDB}$,

Q_{BAT} is off.

V_{SYS} Overvoltage Lockout ($V_{SYSOVLO}$)

Ideally, V_{SYS} should not exceed the battery charge termination threshold. Systems must be designed so that V_{SYS} never exceeds 4.8V (transient and steady-state). If the V_{SYS} exceeds $V_{SYSOVLO}$ during a fault, the MAX77840 resets the charger and fuel gauge Type O registers.

Battery Overvoltage Protection

The MAX77840 charger features battery overvoltage protection to prevent battery overvoltage. The battery overvoltage threshold is set at 240mV (typ) above the CHG_CV_PRM setting. If the IC detects that the battery voltage rises above CHG_CV_PRM + 240mV unexpectedly in normal charging cycle, the battery overvoltage comparator is activated to trigger the interrupt after 6ms debounce time and battery detail register bits (BAT_DTLS[6:4]) are set to indicate a battery overvoltage event. Further, the QBAT switch is turned off after 56ms debounce time to stop charging and protect the battery. The 56ms delay time allows AP to have enough response time before charging stops.

Battery Overcurrent Protection During System Power-Up

The battery overcurrent protection during system power-up feature limits the battery to system current to I_{SYSPU} as long as V_{SYS} is less than V_{SYSPU}. This feature limits the surge current that typically flows from the main battery to the device's low-impedance system bypass capacitors during a system power-up (system power-up is anytime that energy from the battery is supplied to SYS when $V_{SYS} < V_{SYSPU}$). This system power-up condition typically occurs when a battery is hot-inserted into an otherwise unpowered device. Similarly, the system power-up condition could occur when the DISIBS bit is driven low. When system power-up occurs due to hot insertion into an otherwise unpowered device, a small delay of (t_{SYSPU}) is required in order for this feature's control circuits to activate. A current spike over I_{SYSPU} can occur during this time.

Battery Overcurrent Protection Due to Fault

The MAX77840 protects itself, the battery, and the system from potential damage due to excessive battery discharge current. Excessive battery discharge current can occur due to several reasons such as exposure to moisture, a software problem, an IC failure, a component failure, or a mechanical failure that causes a short circuit. The battery overcurrent protection feature is enabled with B2SOVRC; disabling this feature reduces the main battery current consumption by I_{BOVRC}. When the battery (BATT) to system (SYS) discharge current (I_{BATT}) exceeds the programmed overcurrent threshold for at least t_{BOVRC}, a BAT_I interrupt is generated, BAT_OK is cleared, and BAT_DTLS reports an overcurrent condition. Typically when the system's processor detects this overcurrent interrupt, it executes a housekeeping routine that tries to mitigate the overcurrent situation. If the processor cannot correct the overcurrent, then it can disable the BATT to SYS discharge path (B2S switch) by driving the DISIBS bit to a logic high. There are different scenarios in which the MAX77840 responds to the DISIBS bit being set high depending on the available power source and the state of the charger.

- **The IC is only powered from BATT and DISIBS bit is set:** SYS collapses and is allowed to go to 0V. DISIBS holds state. To exit from this state, plug in a valid input charger which causes the SYS to power up and the system to wake up.
- **The IC is powered from BATT and CHGIN, and the charger buck is not switching and DISIBS bit is set:** To exit from this state, plug in a valid input charger which causes the SYS to power up and the system to wake up.
- **The IC is powered from BATT and CHGIN and the charger buck is switching and DISIBS bit is set:** The DISIBIS bit is ignored.

Battery Thermistor for Charge and Discharge

Battery thermistor is sampled to control the charging state during the charging process. The MAX77840 stops charging when battery temperature is above 60°C or below 0°C. The JEITA standard is also implemented in the MAX77840 through the built-in fuel gauge or can be done with AP's assistance.

Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the MAX77840 junction temperature. As shown in Figure 11, when the die temperature exceeds the value programmed by REGTEMP (T_{JREG}), a thermal limiting circuit reduces the battery charger's target current by 105mA/°C (ATJREG). The target charge current reduction is achieved

with an analog control loop (i.e., not a digital reduction in the input current). When the thermal foldback loop changes state, a CHG_I interrupt is generated and the system's microprocessor might want to read the status of the thermal regulation loop through the TREG status bit. Note that the thermal foldback loop being active is not considered to be abnormal operation and the thermal foldback loop status does not affect the CHG_OK bit (only information contained within CHG_DTLS affects CHG_OK).

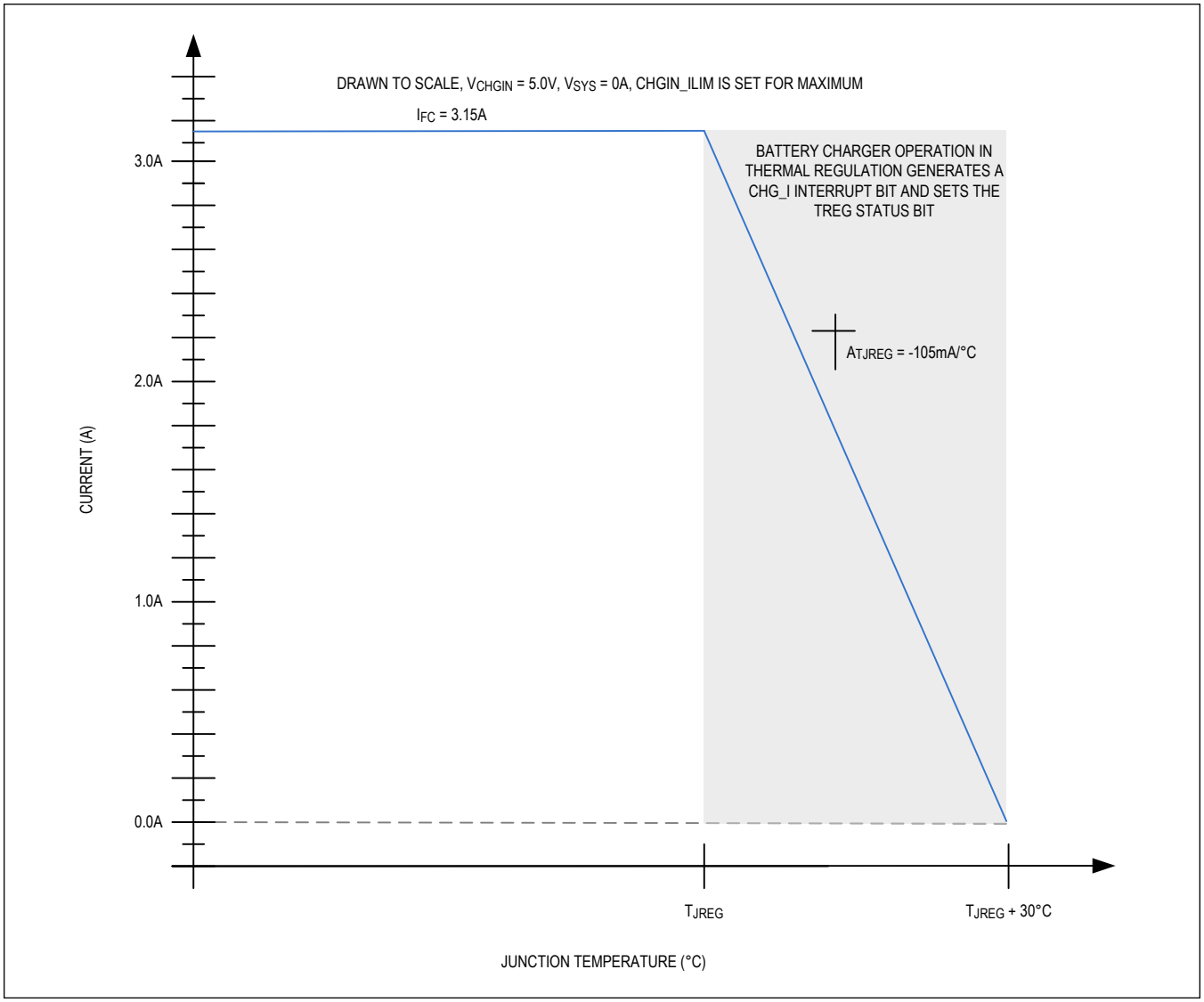


Figure 11. Charge Currents vs. Junction Temperature

Analog Low-Noise Power Input (AVL) and PVL

As shown in Figure 2, AVL is a regulated output from BYP node. AVL is the power input for the MAX77840 charger's analog circuitry. PVL has a 12.5Ω resistor internal to the MAX77840 and a 10µF ceramic capacitor external bypass capacitor to isolate noises from AVL.

Charger Register Details

The MAX77840's charger has convenient default register settings and a complete charger state machine that allows it to be used with minimal software interaction. Software interaction with the register map enhances the charger by allowing a high degree of configurability. An easy-to-navigate interrupt structure and in-depth status reporting allows software to quickly track the changes in the charger's status.

Register Protection

The CHG_CNFG_01, CHG_CNFG_02, CHG_CNFG_03, CHG_CNFG_04, CHG_CNFG_05, and CHG_CNFG_07 registers contain settings for static parameters that are associated with a particular system and battery. These static settings are typically set once each time the system's microprocessor runs its boot-up initialization code; they are not changed again until the microprocessor reboots. CHGPROT allows for blocking the write access to these static settings to protect them from being changed unintentionally. This protection is particularly useful for critical parameters such as the battery charge current CHG_CC and the battery charge voltage CHG_CV_PRM.

Determine the following registers bit settings by considering the characteristics of the battery. It is recommended that CHG_CC be set to the maximum acceptable charge rate for the battery. There is typically no need to actively adjust the CHG_CC setting based on the capabilities of the source at CHGIN, system load, or thermal limitations of the PCB; the smart power selector intelligently manages the following parameters to optimize the power distribution.

- Charger Restart Threshold CHG_RSTRT
- Fast-Charge Timer (t_{FC}) FCHGTIME
- Fast-Charge Current CHG_CC
- Top-Off Time TO_TIME
- Top-Off Current TO_ITH
- Battery Regulation Voltage CHG_CV_PRM

Determine the following register bit settings by considering the characteristics of the system:

- Low-Battery Prequalification Enable PQEN
- Minimum System Regulation Voltage MINVSYS
- Junction Temperature Thermal Regulation Loop Set Point REGTEMP

Interrupt Mask, Okay and Detail Registers

The MAX77840 battery charger section provides detailed information about interrupt generation and status for the following sub-blocks:

- Charger Input
- Charger State Machine
- Battery
- Bypass Node

State changes on any sub-block report interrupts through the CHG_INT register. Interrupt sources are masked from affecting the hardware interrupt pin when bits in the CHG_INT_MASK register are set. The CHG_INT_OK register provides a single-bit status indication of whether the interrupt generating sub-block is okay or not. The full status of each interrupt generating sub-block is provided in the CHG_DTLS_00, CHG_DTLS_01, CHG_DTLS_02, and CHG_DTLS_03 registers. Note that CHG_INT, CHG_INT_MASK, and CHG_INK_OK use the same bit position for each interrupt generating block to simplify software development.

Interrupt bits are automatically cleared upon reading a given interrupt register. When all pending CHG_INT interrupts are cleared, the top-level interrupt bit is deasserted.

CHG_INT Register Bit Description

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_INT		Charger Interrupt	0xB0	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
0	R/C	BYP_I	0	Bypass Node Interrupt 0 = The BYP_OK bit has not changed since the last time this bit was read. 1 = The BYP_OK bit has changed since the last time this bit was read.	
1	R/C	BAT2SOC_I	0	BATT to SYS Overcurrent Interrupt 0 = The BAT2SOC_OK bit has not changed since the last time this bit was read. 1 = The BAT2SOC _OK bit has changed since the last time this bit was read.	
2	R/C	BATP_I	0	Battery Presence Interrupt 0 = The BATP_OK bit has not changed since the last time this bit was read. 1 = The BATP_OK bit has changed since the last time this bit was read.	
3	R/C	BAT_I	0	Battery Interrupt 0 = The BAT_OK bit has not changed since the last time this bit was read. 1 = The BAT_OK bit has changed since the last time this bit was read.	
4	R/C	CHG_I	0	Charger Interrupt 0 = The CHG_OK bit has not changed since the last time this bit was read. 1 = The CHG_OK bit has changed since the last time this bit was read.	
5	R/C	TOPOFF_I	0	TOPOFF Interrupt 0 = The TOPOFF_OK bit has not changed since the last time this bit was read. 1 = The TOPOFF_OK bit has changed since the last time this bit was read.	
6	R/C	CHGIN_I	0	CHGIN Interrupt 0 = The CHGIN_OK bit has not changed since the last time this bit was read. 1 = The CHGIN_OK bit has changed since the last time this bit was read.	
7	R/C	AICL_CHGINI_I	0	AICL_CHGINI Interrupt 0 = The AICL_CHGINI_OK bit has not changed since the last time this bit was read. 1 = The AICL_CHGINI_OK bit has changed since the last time this bit was read.	

CHG_INT_MASK Register Bit Description (0xB1)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_INT_MASK		Charger Interrupt Mask	0xB1	O	0xFF
BIT	MODE	NAME	RESET	DESCRIPTION	
0	R/W	BYP_M	1	Bypass Interrupt Mask 0 = Unmasked 1 = Masked	
1	R/W	BAT2SOC_M	1	Battery to SYS Overcurrent Mask 0 = Unmasked 1 = Masked	
2	R/W	BATP_M	1	Battery Presence Interrupt Mask 0 = Unmasked 1 = Masked	
3	R/W	BAT_M	1	Battery Interrupt Mask 0 = Unmasked 1 = Masked	
4	R/W	CHG_M	1	Charger Interrupt Mask 0 = Unmasked 1 = Masked	
5	R/W	TOPOFF_M	1	TOPOFF Interrupt Mask 0 = Unmasked 1 = Masked	

6	R/W	CHGIN_M	1	CHGIN Interrupt Mask 0 = Unmasked 1 = Masked
7	R/W	AICL_CHGINI_M	1	AICL_CHGINI Interrupt Mask 0 = Unmasked 1 = Masked

CHG_INT_OK Register Bit Description (0xB2)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_INT_OK		Charger Status	0xB2	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
0	R	BYP_OK	0	Single-Bit Bypass Status Indicator. See BYP_DTLS for more information. 0 = Something powered by the bypass node has hit current limit (i.e., BYP_DTLS ≠ 0x00). 1 = The bypass node is okay (i.e., BYP_DTLS = 0x00).	
1	R	BAT2SOC_OK	0	Battery-to-SYS Overcurrent Status Indicator. See BAT2SOC_DTLS for more information. 0 = Battery to SYS has hit overcurrent limit. 1 = Battery to SYS is okay.	
2	R	BATP_OK	0	Battery Present Status Indicator 0 = Main Battery is not present. 1 = Main Battery is present.	
3	R	BAT_OK	0	Single-Bit Battery Status Indicator. See BAT_DTLS for more information. 0 = The battery has an issue or the charger has been suspended, (i.e., BAT_DTLS ≠ 0x03 or 0x04). 1 = The battery is okay (i.e., BAT_DTLS = 0x03 or 0x04).	
4	R	CHG_OK	0	Single-Bit Charger Status Indicator. See CHG_DTLS for more information. 0 = The charger has suspended charging or TREG = 1. (i.e., CHG_DTLS ≠ 0x00, 0x01, 0x02, 0x03, 0x05, or 0x08) 1 = The charger is okay or the charger is off. (i.e., CHG_DTLS = 0x00, 0x01, 0x02, 0x03, 0x05, or 0x08)	
5	R	TOPOFF_OK	0	Single-Bit TOPOFF Indicator. See CHG_DTLS for more information. 0 = The charger is not in TOPOFF state. 1 = The charger is in TOPOFF state.	
6	R	CHGIN_OK	0	Single-Bit CHGIN Input Status Indicator. See CHGIN_DTLS for more information. 0 = The CHGIN input is invalid (i.e., CHGIN_DTLS ≠ 0x03). 1 = The CHGIN input is valid (i.e., CHGIN_DTLS = 0x03).	
7	R	AICL_CHGINI_OK	0	AICL_CHGINI_OK 0 = In AICL or/and CHGINI mode. 1 = Not in AICL mode and not in CHGINI mode.	

CHG_DETAILS_00 Register Bit Description (0xB3)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_00		Charger Details 00	0xB3	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
0	R	BATP_DTLS	0	Battery Detection Details 0 = Battery presence 1 = No battery presence	
1	R	OVPDRV_DTLS	0	OVPDRV FET Details 0 = External OVP FET Off 1 = External OVP FET On	

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_00		Charger Details 00	0xB3	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
2	R	VBUSDET_DTLS	0	V_{BUSDET} Details 1 = V_{BUSDET} below 5.7V 0 = V_{BUSDET} above 5.8V (100mV hysteresis)	
4:3	R	RSVD	00	Reserved	
6:5	R	CHGIN_DTLS	00	CHGIN Details 0x00 = VBUS is invalid. $V_{CHGIN} < V_{CHGIN\_UVLO}$ 0x01 = VBUS is invalid. $V_{CHGIN} < V_{BATT} + V_{CHGIN2SYS}$ and $V_{CHGIN} > V_{CHGIN\_UVLO}$ 0x02 = VBUS is invalid. $V_{CHGIN} > V_{CHGIN\_OVLO}$ 0x03 = VBUS is valid. $VC_{HGIN} > V_{CHGIN\_UVLO}$, $V_{CHGIN} > V_{BATT} + V_{CHGIN2SYS}$, $V_{CHGIN} < V_{CHGIN\_OVLO}$	
7	R	RSVD	0	Reserved	

CHG_DETAILS_01 Register Bit Description (0xB4)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_00		Charger Details 00	0xB3	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
3:0	R	CHG_DTLS	0000	Charger Details 0x00 = Charger is in dead-battery prequalification or low-battery prequalification mode, CHG_OK = 1, $V_{BATT} < V_{PQLB}$, $T_J < T_{SHDN}$ 0x01 = Charger is in fast-charge constant current mode, CHG_OK = 1, $V_{BATT} < V_{BATREG}$, $T_J < T_{SHDN}$ 0x02 = Charger is in fast-charge constant voltage mode, CHG_OK = 1, $V_{BATT} = V_{BATREG}$, $T_J < T_{SHDN}$ 0x03 = Charger is in top-off mode, CHG_OK = 1, $V_{BATT} \geq V_{BATREG}$, $T_J < T_{SHDN}$ 0x04 = Charger is in done mode, CHG_OK = 0, $V_{BATT} > V_{BATREG} - V_{RSTRT}$, $T_J < T_{SHDN}$ 0x05 = Charger is in high temperature charging mode, CHG_OK = 1, $T_J < T_{SHDN}$, T3 < T_{BATT} < T4 0x06 = Charger is in timer fault mode, CHG_OK = 0, $V_{BATT} < V_{BATOV}$, if BAT_DTLS = 0b001 then $V_{BATT} < V_{PQLB}$, $T_J < T_{SHDN}$ 0x07 = Charger is in thermistor suspend mode, CHG_OK = 0, $V_{BATT} < V_{BATOV}$, if BAT_DTLS = 0b001 then $V_{BATT} < V_{PQLB}$, $T_J < T_{SHDN}$ 0x08 = Charger is off, charger input invalid and/or charger is disabled, CHG_OK = 1 0x09 = Reserved 0x0A = Charger is off and the junction temperature is > T_{SHDN}, CHG_OK = 0 0x0B = Charger is off because the watchdog timer expired, CHG_OK = 0 0x0C–0x0F = Reserved	

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_00		Charger Details 00	0xB3	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
6:4	R	BAT_DTLS	000	Battery Details 0x00 = No battery and the charger is suspended. 0x01 = V_{BATT} < V_{PQLB}. This condition is also reported in the CHG_DTLS as 0x00 0x02 = The battery is taking longer than expected to charge. This could be due to high system currents, an old battery, a damaged battery or something else. Charging has suspended and the charger is in its timer fault mode. This condition is also reported in the CHG_DTLS as 0x06 0x03 = The battery is okay, and its voltage is greater than the minimum system voltage (V_{SYSMIN} < V_{BATT}), QBAT is on and V_{SYS} is approximately equal to V_{BATT}. 0x04 = The battery is okay, but its voltage is low: V_{PQLB} < V_{BATT} < V_{SYSMIN}. QBAT is operating like an LDO to regulate V_{SYS} to V_{SYSMIN}. 0x05 = The battery voltage is greater than the battery overvoltage flag threshold (V_{BATTOV}) or it has been greater than this threshold within the last 37.5ms. V_{BATTOV} is set to 240mV above the V_{BATREG} target as programmed by CHG_CV_PRM. Note that this flag is only be generated when there is a valid input or when the DC-DC is operating as a boost 0x06 = The battery is overcurrent or it has been overcurrent for at least 37.5ms since the last time this register has been read. 0x07 = Reserved In the event that multiple faults occur within the battery details category, overcurrent has priority followed by no-battery, then overvoltage, then timer fault, and then below prequal	
7	R	TREG	0	Temperature Regulation Status 0 = The junction temperature is less than the threshold set by REGTEMP and the full charge current limit is available. 1 = The junction temperature is greater than the threshold set by REGTEMP and the charge current limit might be folding back to reduce power dissipation.	

CHG_DETAILS_02 Register Bit Description (0xB5)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_02		Charger details 02	0xB5	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
2:0	R	BYP_DTLS	000	Bypass Node Details. All bits in this family are independent from each other. They are grouped together only because they all relate to the health of the BYP node and any change in these bits generates a BYP_I interrupt. BYP_DTLS0 = OTGILIM = 0bxx1 BYP_DTLS1 = BSTILIM = 0bx1x BYP_DTLS2 = BCKNegILIM = 0b1xx 0bx00 = The bypass node is okay. 0bxx1 = The BYP to CHGIN switch (OTG switch) current limit was reached within the last 28ms. 0bx1x = The BYP reverse boost converter has hit its current limit (this condition persists for 28ms). 0b1xx = The BYP buck converter has hit the maximum negative demand current limit (this condition persists for 446µs).	
3	R	AICL_DTLS	0	AICL Mode Details 0 = Not in AICL mode 1 = In AICL mode	
4	R	CHGINI_DTLS	0	CHGINI Mode Details 0 = Not in CHGINI mode 1 = In CHGINI mode	

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_02		Charger details 02	0xB5	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
7:5	R	RSVD	000	Reserved	

CHG_CNFG_00 Register Bit Description (0xB7)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_00		Charger configuration 00	0xB7	O	0x05
BIT	MODE	NAME	RESET	DESCRIPTION	
3:0	R/W	MODE	0101	Power Selector Configuration 0x00 = 0b0000: Charger = Off, OTG = Off, buck = Off, boost = Off. The FET_DRV switch (QBAT) is on to allow the battery to support the system. BYP could be biased based on the CHGIN availability. 0x01 = 0b0001: Same as 0b0000 0x02 = 0b0010: Same as 0b0000 0x03 = 0b0011: Same as 0b0000 0x04 = 0b0100: Charger = Off, OTG = Off, buck = On, boost = Off. When there is a valid input, the buck converter regulates the system voltage to be V_{BATREG}. 0x05 = 0b0101: Charger = On, OTG = Off, buck = On, boost = Off. When there is a valid input, the battery is charging. V_{SYS} is the larger of V_{SYSMIN} and ~V_{BATT} + I_{BATT} × $R_{BAT2SYS}$. 0x06 = 0b0110: Same as 0b101 0x07 = 0b0111: Same as 0b101 0x08 = 0b1000: Charger = Off, OTG = Off, buck = Off, boost = On. The FET_DRV switch (QBAT) is on to allow the battery to support the system, while the charger's DC-DC operates as a boost converter. The BYP voltage is regulated to V_{BYPSET}. CHGIN to BYP FET is off. OVPDRV FET is off. 0x09 = 0b1001: Same as 0b1000 0x0A = 0b1010: Charger = Off, OTG = On, buck = Off, boost = On. The FET_DRV switch (QBAT) is on to allow the battery to support the system, while the charger's DC-DC operates as a boost converter. CHGIN to BYP FET is on which allows it to source current up to ICHGIN.OTG.MAX. The boost target voltage is 5.1V ($V_{BYP.OTG}$). 0x0B = 0b1011: Reserved 0x0C = 0b1100: Charger = Off, OTG = Off, buck = On, boost = On. When there is a valid input, the system is supported from that input (V_{SYS} = 4.2V). When input is invalid, the boost is on with a target voltage of V_{BYPSET}. 0x0D = 0b1101: Charger = On, OTG = Off, buck = On, boost = On. When there is a valid input, the system is supported from that input (V_{SYS} is the larger of V_{SYSMIN} and ~V_{BATT} + I_{BATT} × $R_{BAT2SYS}$). When input is invalid, the boost is on with a target voltage of V_{BYPSET} 0x0E = 0b1110: Charger = Off, OTG = On, buck = On, boost = On. V_{SYS} = 4.2V and QCHGIN is on, allowing it to source current up to ICHGIN.OTG.MAX. Boost is on with a target voltage of 5.1V ($V_{BYP.OTG}$). 0x0F = 0b1111: Charger = On, OTG = On, buck = On, boost = On. V_{SYS} is the larger of V_{SYSMIN} and ~V_{BATT} + I_{BATT} x $R_{BAT2SYS}$. QCHGIN is on, which allows it to source current up to ICHGIN.OTG.MAX. Boost is on with a target voltage of 5.1V ($V_{BYP.OTG}$).
4	R/W	WDTEN	0	Watchdog Timer Enable Bit. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01. 0 = Watchdog Timer Disabled 1 = Watchdog Timer Enabled

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_00		Charger configuration 00	0xB7	O	0x05
BIT	MODE	NAME	RESET	DESCRIPTION	
5	R/W	SPREAD	0	Spread-Spectrum Feature 0: Disabled 1: Enabled Note: Feature is operational both for 9V and 12V CHGIN input voltage. The feature is not guaranteed to be operational for 5V CHGIN input voltage. When the feature is not operational, it can stay enabled without side effects.	
6	R/W	DISIBS	0	BATT to SYS FET Disable Control 0 = BATT to SYS FET is controlled by the power path state machine 1 = BATT to SYS FET is forced off	
7	R/W	DIS_CD_CTRL	0	Disable Charger Detect Control over CHGR 0 = Enabled 1 = Disabled	

CHG_CNFG_01 Register Bit Description (0xB8)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_01		Charger details 01	0xB8	O R/W (protected with CHGPROT)	0x90
BIT	MODE	NAME	RESET	DESCRIPTION	
2:0	R/W	FCHGTIME	000	Fast-Charge Timer Duration (t_{FC}) 0x00 = Disabled 0x01 = 4hrs 0x02 = 6hrs 0x03 = 8hrs 0x04 = 10hrs 0x05 = 12hrs 0x06 = 14hrs 0x07 = 16hrs	
3	R/W	FSW	1	Switching Frequency Option 0: 4MHz 1: 2MHz (OTP option to default to 1)	
5:4	R/W	CHG_RSTRT	01	Charger Restart Threshold 0x00 = 100mV below the value programmed by CHG_CV_PRM 0x01 = 150mV below the value programmed by CHG_CV_PRM 0x02 = 200mV below the value programmed by CHG_CV_PRM 0x03 = Disabled	
6	R/W	LSEL	0	Inductor Selection 0:0.47µH (for 4MHz option only) 1:1µH (for 2MHz and 4MHz option)	
7	R/W	PQEN	1	Low-Battery Prequalification Mode Enable 0 = Low-Battery Prequalification mode is disabled 1 = Low-Battery Prequalification mode is enabled	

CHG_CNFG_02 Register Bit Description (0xB9)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_CNFG_02</td><td>Charger Configuration 02</td><td>0xB9</td><td>O
R/W (protected with CHGPROT)</td><td>0x09</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>5:0</td><td>R/W</td><td>CHG_CC</td><td>001001 (450mA)</td><td colspan="2">Fast Charge Current Selection. When the charger is enabled, the charge current limit is set by these bits. These bits range from 0.1A (0x01) to 3.0A (0x3C) in 50mA steps. Note that codes 0x01 and 0x02 are both 100mA. Code 0x00 is reserved and must not be used.
<table>
<tr><th>BITS</th><th>(mA)</th><th>BITS</th><th>(mA)</th><th>BITS</th><th>(mA)</th><th>BITS</th><th>(mA)</th></tr>
<tr><td>0x00</td><td>-</td><td>0x10</td><td>800</td><td>0x20</td><td>1600</td><td>0x30</td><td>2400</td></tr>
<tr><td>0x01</td><td>100</td><td>0x11</td><td>850</td><td>0x21</td><td>1650</td><td>0x31</td><td>2450</td></tr>
<tr><td>0x02</td><td>100</td><td>0x12</td><td>900</td><td>0x22</td><td>1700</td><td>0x32</td><td>2500</td></tr>
<tr><td>0x03</td><td>150</td><td>0x13</td><td>950</td><td>0x23</td><td>1750</td><td>0x33</td><td>2550</td></tr>
<tr><td>0x04</td><td>200</td><td>0x14</td><td>1000</td><td>0x24</td><td>1800</td><td>0x34</td><td>2600</td></tr>
<tr><td>0x05</td><td>250</td><td>0x15</td><td>1050</td><td>0x25</td><td>1850</td><td>0x35</td><td>2650</td></tr>
<tr><td>0x06</td><td>300</td><td>0x16</td><td>1100</td><td>0x26</td><td>1900</td><td>0x36</td><td>2700</td></tr>
<tr><td>0x07</td><td>350</td><td>0x17</td><td>1150</td><td>0x27</td><td>1950</td><td>0x37</td><td>2750</td></tr>
<tr><td>0x08</td><td>400</td><td>0x18</td><td>1200</td><td>0x28</td><td>2000</td><td>0x38</td><td>2800</td></tr>
<tr><td>0x09</td><td>450</td><td>0x19</td><td>1250</td><td>0x29</td><td>2050</td><td>0x39</td><td>2850</td></tr>
<tr><td>0x0A</td><td>500</td><td>0x1A</td><td>1300</td><td>0x2A</td><td>2100</td><td>0x3A</td><td>2900</td></tr>
<tr><td>0x0B</td><td>550</td><td>0x1B</td><td>1350</td><td>0x2B</td><td>2150</td><td>0x3B</td><td>2950</td></tr>
<tr><td>0x0C</td><td>600</td><td>0x1C</td><td>1400</td><td>0x2C</td><td>2200</td><td>0x3C</td><td>3000</td></tr>
<tr><td>0x0D</td><td>650</td><td>0x1D</td><td>1450</td><td>0x2D</td><td>2250</td><td>0x3D</td><td>3050</td></tr>
<tr><td>0x0E</td><td>700</td><td>0x1E</td><td>1500</td><td>0x2E</td><td>2300</td><td>0x3E</td><td>3100</td></tr>
<tr><td>0x0F</td><td>750</td><td>0x1F</td><td>1550</td><td>0x2F</td><td>2350</td><td>0x3F</td><td>3150</td></tr>
</table>
Note that the thermal foldback loop can reduce the battery charger’s target current by ATJREG</td></tr>
<tr><td>7:6</td><td>R/W</td><td>OTG_ILIM</td><td>00</td><td colspan="2">CHGIN Output Current Limit in OTG Mode (ICHGIN.OTG.LIM). When MODE = 0x09 or 0x0A, the CHGIN current limit is set at the following current limit:
00 = 500mA
01 = 900mA
10 = 1200mA
11 = 1500mA</td></tr>
</table>

CHG_CNFG_03 Register Bit Description (0xBA)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_03		Charger Configuration 03	0xBA	O R/W (protected with CHGPROT)	0xDA
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
2:0	R/W	TO_ITH	010 (150mA)	Top Off Current Threshold. The charger transitions from its fast-charge constant voltage mode to its top-off mode when the charger current decays to the value programmed by this register. This transition generates a CHG_I interrupt and causes the CHG_DTLS register to report that the charger is in top-off mode. This transition also starts the top-off time as programmed by TO_TIME. 0x00 = 100mA 0x01 = 125mA 0x02 = 150mA (default) 0x03 = 175mA 0x04 = 200mA 0x05 = 250mA 0x06 = 300mA 0x07 = 350mA	
5:3	R/W	TO_TIME	011 (30min)	Top Off Timer Setting 0x00 = 0min 0x01 = 10min 0x02 = 20min 0x03 = 30min 0x04 = 40min 0x05 = 50min 0x06 = 60min 0x07 = 70min	
7:6	R/W	ILIM	11	Programmable Buck Peak Current Limit 00: Support ICHG = 3.00A 01: Support ICHG = 2.75A 10: Support ICHG = 2.50A 11: Support ICHG = 2.25A	

CHG_CNFG_04 Register Bit Description (0xBB)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_04		Charger Configuration 04	0xBB	O R/W (protected with CHGPROT)	0x96
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
5:0	R/W	CHG_CV_PRM	010110 (4.2V)	Primary Charge Termination Voltage Setting. When the charger is enabled and the main-battery temperature is < T3 if JEITA = 1 or < T4 if JEITA = 0, then the charger's battery regulation voltage (V_{BATREG}) is set by CHG_CV_PRM.	
7:6	R/W	MINVSYS	10 (3.6V)	Minimum System Regulation Voltage (V_{SYSMIN}) 0x00 = 3.4V 0x01 = 3.5V 0x02 = 3.6V 0x03 = 3.7V	

BITS	VOLTAGE	BITS	VOLTAGE	BITS	VOLTAGE
0x00	3.650	0x10	4.050	0x20	4.425
0x01	3.675	0x11	4.075	0x21	4.450
0x02	3.700	0x12	4.100	0x22	4.475
0x03	3.725	0x13	4.125	0x23	4.500
0x04	3.750	0x14	4.150	0x24	4.525
0x05	3.775	0x15	4.175	0x25	4.550
0x06	3.800	0x16	4.200	0x26	4.575
0x07	3.825	0x17	4.225	0x27	4.600
0x08	3.850	0x18	4.250	0x28	4.625
0x09	3.875	0x19	4.275	0x29	4.650
0x0A	3.900	0x1A	4.300	0x2A	4.675
0x0B	3.925	0x1B	4.325	0x2B	4.700
0x0C	3.950	0x1C	4.340		
0x0D	3.975	0x1D	4.350		
0x0E	4.000	0x1E	4.375		
0x0F	4.025	0x1F	4.400		

CHG_CNFG_06 Register Bit Description (0xBD)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_06		Charger Configuration 06	0xBD	O	0x80
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
1:0	R/W	WDTCLR	00	Watchdog Timer Clear Bits. Writing 01 to these bits clears the watchdog timer when the watchdog timer is enabled. 0x00 = The watchdog timer is not cleared 0x01 = The watchdog timer is cleared 0x02 = The watchdog timer is not cleared 0x03 = The watchdog timer is not cleared	

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_06		Charger Configuration 06	0xBD	O	0x80
BIT	MODE	NAME	RESET	DESCRIPTION	
3:2	R/W	CHGPROT	00	Charger Settings Protection Bits. Writing 11 to these bits unlocks the write capability for the registers that are "Protected with CHGPROT". Writing any value besides "11" locks these registers. 0x00 = Write capability is locked 0x01 = Write capability is locked 0x02 = Write capability is locked 0x03 = Write capability is unlocked	
4	R/W	MAXOTG_EN	0	MAXOTG Feature Enable Bit 0 = MAXOTG Feature is disabled 1 = MAXOTG Feature is enabled	
5	R/W	OTG_DC	0	OTG Fault Duty Cycle Selection Bit 0 = 10% ON duty cycle when OTG hits current limit 1 = 1% ON duty cycle when OTG hits current limit	
6	R/W	EN_THM	0	Enable Thermistor Control in Charger 0 = No thermistor control in charger 1 = Have thermistor control in charger. Charging stops when battery temperature >60ºC or <0ºC	
7	R/W	LEDEN	1	Charging Status Indicator LED enable 0 = Charging Status Indicator LED is disabled 1 = Charging Status Indicator LED is enabled	

CHG_CNFG_07 Register Bit Description (0xBE)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_07		Charger Configuration 07	0xBE	O R/W (protected with CHGPROT)	0x30
BIT	MODE	NAME	RESET	DESCRIPTION	
1:0	R/W	RSVD	00	Reserved	
2	R/W	DIS_QBATOFF	0	Disable QBATOFF in case of battery overcurrent hit limit. 0 = Charger controls QBAT switch; QBAT is turned off in case the battery overcurrent occurs for 6ms. 1 = QBAT is not turned off when battery overcurrent occurs	
6:3	R/W	REGTEMP	0110	Junction Temperature Thermal Regulation Loop Set point. The charger's target current limit starts to foldback and the TREG bit is set if the junction temperature is greater than the REGTEMP set point. 0x00 = 85°C 0x01 = 90°C 0x02 = 95°C 0x03 = 100°C 0x04 = 105°C 0x05 = 110°C 0x06 = 115°C (default) 0x07 = 120°C 0x08 = 125°C 0x09 = 130°C	
7	R/W	WD_QBATOFF	0	Disable QBAT FET Along with Charger When Watchdog Timer Expires 0: Turn off only the charger 1: Turn off buck, charger, and QBAT switch	

CHG_CNFG_09 Register Bit Description (0xC0)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_09		Charger Configuration 09	0xC0	O	0x0F

BIT	MODE	NAME	RESET	DESCRIPTION
6:0	R/W	CHGIN_ILIM	0x0F (0.50A)	Maximum Input Current Limit Selection. 7-bit adjustment from 100mA to 4A in 33mA steps. Note that the first four codes are all 100mA.
7	R/W	OVPDRV_CTL	0	OVPDRV FET Override Software Control Bit 0: OVPDRV FET is controlled by charger internal logic 1: OVPDRV is forced to be ON regardless of charger internal logic

BITS	UNIT (mA)	BITS	UNIT (mA)	BITS	UNIT (mA)	BITS	UNIT (mA)
0x00	100	0x20	1067	0x40	2133	0x60	3200
0x01	100	0x21	1100	0x41	2167	0x61	3233
0x02	100	0x22	1133	0x42	2200	0x62	3267
0x03	100	0x23	1167	0x43	2233	0x63	3300
0x04	133	0x24	1200	0x44	2267	0x64	3333
0x05	167	0x25	1233	0x45	2300	0x65	3367
0x06	200	0x26	1267	0x46	2333	0x66	3400
0x07	233	0x27	1300	0x47	2367	0x67	3433
0x08	267	0x28	1333	0x48	2400	0x68	3467
0x09	300	0x29	1367	0x49	2433	0x69	3500
0x0A	333	0x2A	1400	0x4A	2467	0x6A	3533
0x0B	367	0x2B	1433	0x4B	2500	0x6B	3567
0x0C	400	0x2C	1467	0x4C	2533	0x6C	3600
0x0D	433	0x2D	1500	0x4D	2567	0x6D	3633
0x0E	467	0x2E	1533	0x4E	2600	0x6E	3667
0x0F	500	0x2F	1567	0x4F	2633	0x6F	3700
0x10	533	0x30	1600	0x50	2667	0x70	3733
0x11	567	0x31	1633	0x51	2700	0x71	3767
0x12	600	0x32	1667	0x52	2733	0x72	3800
0x13	633	0x33	1700	0x53	2767	0x73	3833
0x14	667	0x34	1733	0x54	2800	0x74	3867
0x15	700	0x35	1767	0x55	2833	0x75	3900
0x16	733	0x36	1800	0x56	2867	0x76	3933
0x17	767	0x37	1833	0x57	2900	0x77	3967
0x18	800	0x38	1867	0x58	2933	0x78	4000
0x19	833	0x39	1900	0x59	2967	0x79	4000
0x1A	867	0x3A	1933	0x5A	3000	0x7A	4000
0x1B	900	0x3B	1967	0x5B	3033	0x7B	4000
0x1C	933	0x3C	2000	0x5C	3067	0x7C	4000
0x1D	967	0x3D	2033	0x5D	3100	0x7D	4000
0x1E	1000	0x3E	2067	0x5E	3133	0x7E	4000
0x1F	1033	0x3F	2100	0x5F	3167	0x7F	4000

CHG_CNFG_10 Register Bit Description (0xC1)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_10		Charger Configuration 09	0xC1	O	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
0	R/W	DISSKIP	0	Disable skip mode during buck/charging mode 0 = Buck skip mode is enabled 1 = Disable buck skip mode	
1	R/W	TODEB_EN	0	Enable the MAX77840 top-off long debouncer 0 = MAX77840 top-off debouncer is 56ms 1 = MAX77840 top-off debouncer is set by register TODEB[1:0]	
3:2	R/W	TODEN[1:0]	00	Top-Off Long Debouncer 00 = 112ms 01 = 224ms 10 = 448ms 10 = 896ms	
7:6	R/W	RSVD	00	Reserved	

CHG_CNFG_11 Register Bit Description (0xC2)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_11		Charger Configuration 11	0xC2	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
6:0	R/W	VBYPSET	0x00 (3V)	Bypass Target Output Voltage in Boost Mode. 3.0V (0x00) to 5.8V (0x70) in 0.025V steps. This setting is valid for the boost only mode (MODE = 0x08).
7	R/W	RSVD	0	Reserved

BITS	UNIT (V)	BITS	UNIT (V)	BITS	UNIT (V)	BITS	UNIT (V)
0x00	3.000	0x20	3.800	0x40	4.600	0x60	5.400
0x01	3.025	0x21	3.825	0x41	4.625	0x61	5.425
0x02	3.050	0x22	3.850	0x42	4.650	0x62	5.450
0x03	3.075	0x23	3.875	0x43	4.675	0x63	5.475
0x04	3.100	0x24	3.900	0x44	4.700	0x64	5.500
0x05	3.125	0x25	3.925	0x45	4.725	0x65	5.525
0x06	3.150	0x26	3.950	0x46	4.750	0x66	5.550
0x07	3.175	0x27	3.975	0x47	4.775	0x67	5.575
0x08	3.200	0x28	4.000	0x48	4.800	0x68	5.600
0x09	3.225	0x29	4.025	0x49	4.825	0x69	5.625
0x0A	3.250	0x2A	4.050	0x4A	4.850	0x6A	5.650
0x0B	3.275	0x2B	4.075	0x4B	4.875	0x6B	5.675
0x0C	3.300	0x2C	4.100	0x4C	4.900	0x6C	5.700
0x0D	3.325	0x2D	4.125	0x4D	4.925	0x6D	5.725
0x0E	3.350	0x2E	4.150	0x4E	4.950	0x6E	5.750
0x0F	3.375	0x2F	4.175	0x4F	4.975	0x6F	5.750
0x10	3.400	0x30	4.200	0x50	5.000		
0x11	3.425	0x31	4.225	0x51	5.025		
0x12	3.450	0x32	4.250	0x52	5.050		
0x13	3.475	0x33	4.275	0x53	5.075		
0x14	3.500	0x34	4.300	0x54	5.100		
0x15	3.525	0x35	4.325	0x55	5.125		
0x16	3.550	0x36	4.350	0x56	5.150		
0x17	3.575	0x37	4.375	0x57	5.175		
0x18	3.600	0x38	4.400	0x58	5.200		
0x19	3.625	0x39	4.425	0x59	5.225		
0x1A	3.650	0x3A	4.450	0x5A	5.250		
0x1B	3.675	0x3B	4.475	0x5B	5.275		
0x1C	3.700	0x3C	4.500	0x5C	5.300		
0x1D	3.725	0x3D	4.525	0x5D	5.325		
0x1E	3.750	0x3E	4.550	0x5E	5.350		
0x1F	3.775	0x3F	4.575	0x5F	5.375		

CHG_CNFG_12 Register Bit Description (0xC3)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_12		Charger Configuration 12	0xC3	O	0x44
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
3:0	R/W	B2SOVRC	0100	BATT to SYS Overcurrent Threshold 0x00 = Disabled 0x01 = 3.0A 0x02 = 3.5A 0x03 = 4.0A 0x04 = 4.5A (default) 0x05 = 5.0A 0x06 = 5.5A 0x07 = 6.0A 0x08 = 6.5 0x09 = 7.0A 0x0A = 7.5A 0x0B = 8.0A 0x0C = 8.5A 0x0D = 9.0A 0x0E = 9.0A 0x0F = 9.0A	
5:4	R/W	VCHGIN_REG	00	CHGIN Voltage Regulation Threshold (V_{CHGIN_REG}) Adjustment. The CHGIN to GND minimum turn-on threshold (V_{CHGIN_UVLO}) also scales with this adjustment. 0x00 = V_{CHGIN_REG} = 4.2V and V_{CHGIN_UVLO} = 4.5V 0x01 = V_{CHGIN_REG} = 4.6V and V_{CHGIN_UVLO} = 4.9V 0x02 = V_{CHGIN_REG} = 4.7V and V_{CHGIN_UVLO} = 5.0V 0x03 = V_{CHGIN_REG} = 4.8V and V_{CHGIN_UVLO} = 5.1V	
6	R/W	CHGINSEL	1	CHGIN/USB Input Channel Select 0 = Disabled 1 = Enabled	
7	R/W	CHG_LPM	0	Charger DC-DC Low-Power Mode 0 = Normal Current Capability 1 = Set CHG_LPM to increase efficiency when the DC-DC current is less than 900mA	

Detailed Description—I²C Interface

I²C Interface

The MAX77840 acts as a slave transmitter/receiver.

Slave Addresses

The MAX77840 has a total of four slave addresses. The least significant bit is the read/write indicator (1 for read, 0 for write). The MAX77840 slave addresses for the Top, Charger, Charger Detect, and Fuel Gauge blocks are listed as follows:

- Top, SAFEOUT LDO: 0xCCh / 0xCDh
- Charger: 0xD2h / 0xD3h
- Charger Detect: 0x4Ah /0x4Bh
- Fuel Gauge: 0x6Ch / 0x6Dh

I²C Communication Pins

SCL/SDA are used for I²C communication.

I²C System Configuration

A device on the I²C bus that generates a message is called a transmitter and a device that receives the message is a receiver. The device that controls the message is the master and the devices that are controlled by the master are called slaves.

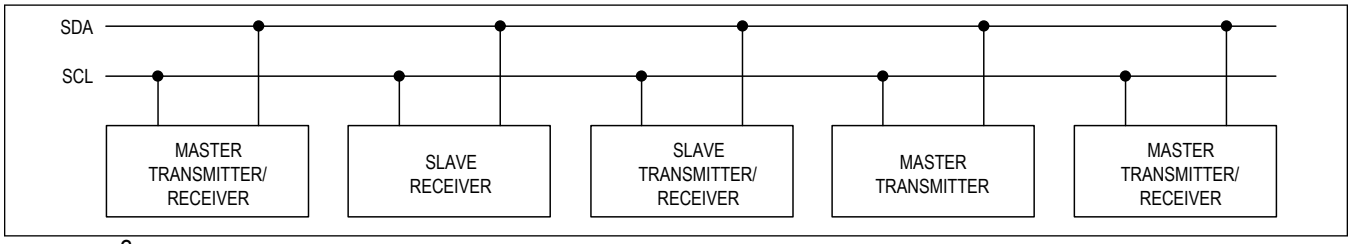


Figure 12. I²C System Configuration

I²C Bit Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as a control signal.

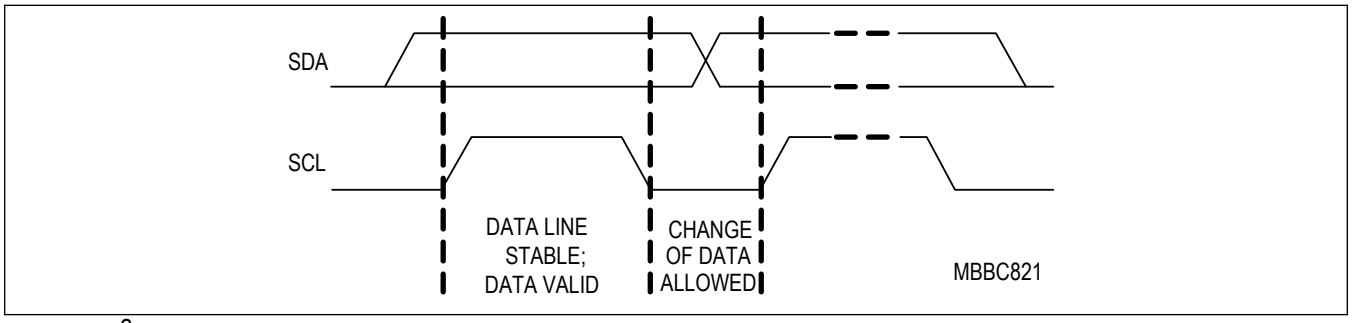


Figure 13. I²C Bit Transfer

I²C Start and Stop Conditions

Both SDA and SCL remain high when the bus is not busy. A high-to-low transition of SDA while SCL is high is defined as the start (S) condition. A low-to-high transition of SDA while SCL is high is defined as the stop (P) condition.

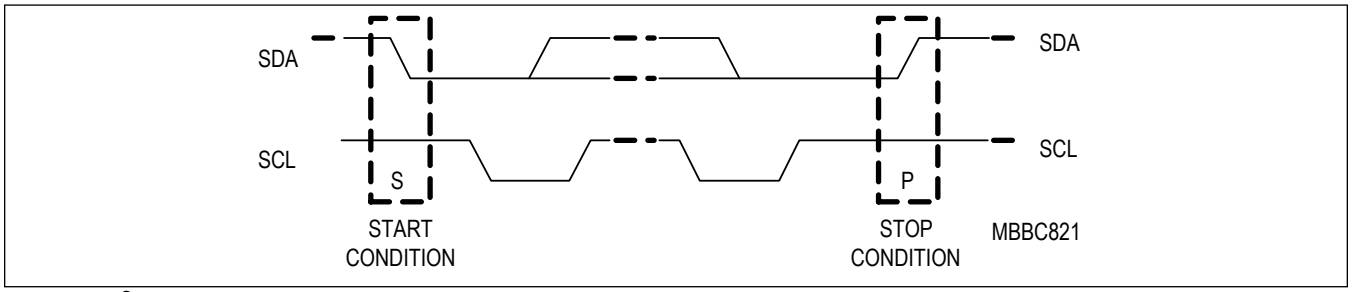


Figure 14. I²C Start and Stop

I²C Acknowledge

The number of data bytes between the start and stop conditions for the transmitter and receiver are unlimited.

Each 8-bit byte is followed by an acknowledge bit. The acknowledge bit is a high-level signal put on SDA by the transmitter during the time the master generates an extra acknowledge-related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge clock pulse (setup and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a stop condition.

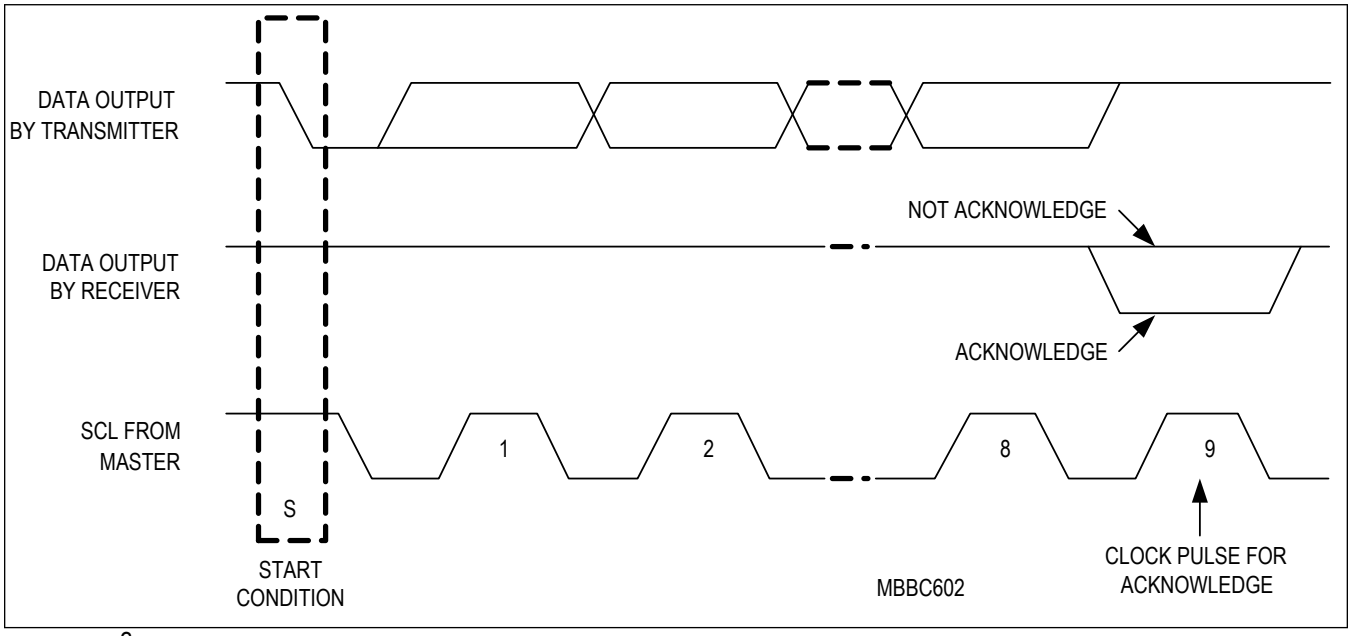


Figure 15. I^2C Acknowledge

Master Transmits (Write Mode)

When master writes to slave, use the format shown in Figure 16.

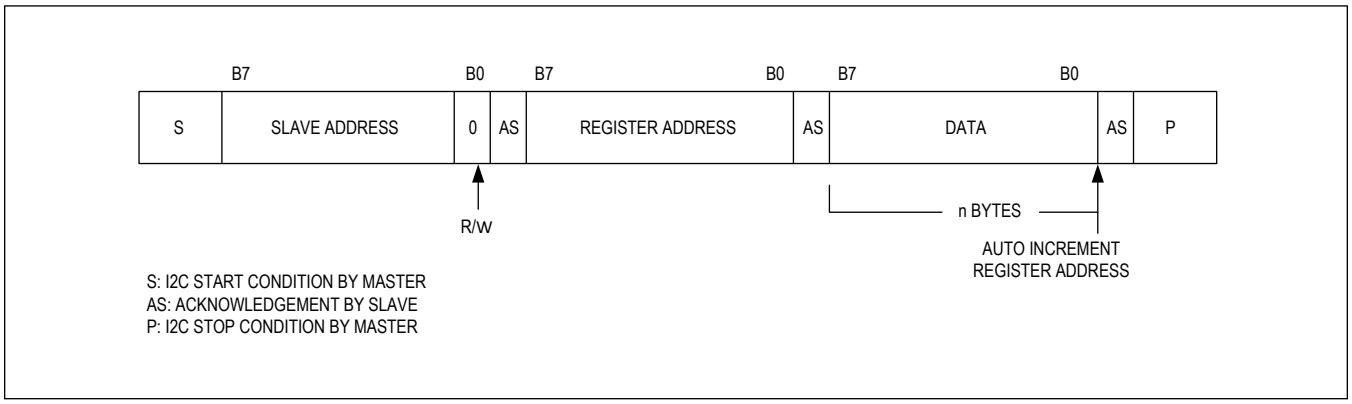


Figure 16. Master Write Operation

Master Reads After Setting Register Address (Write Register Address and Read Data)

When reading a specific register, use the following format:

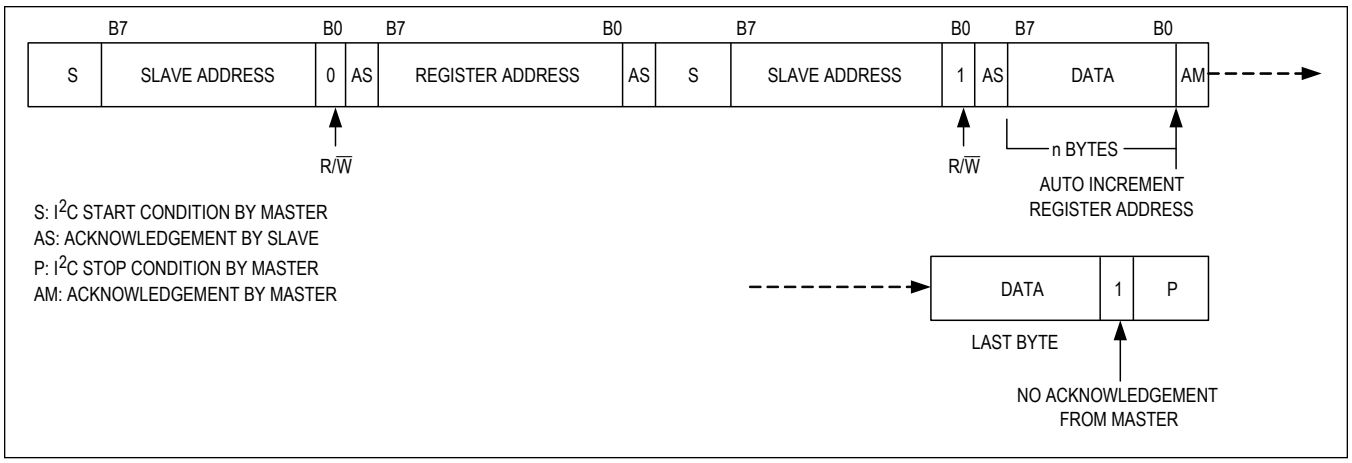


Figure 17. Master Read Operation with Register Addresses

Master Reads Register Data Without Setting Register Address (Read Mode)

When reading registers from the first address, use the following format:

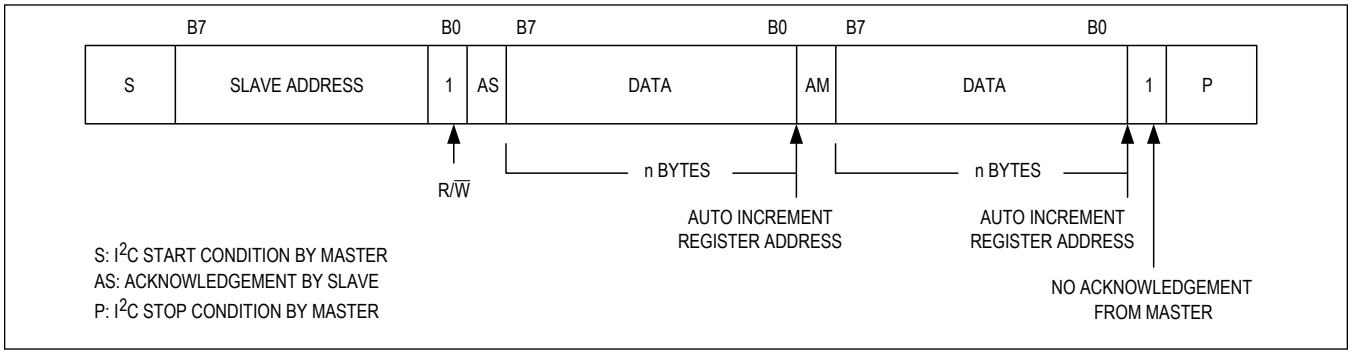


Figure 18. Master Read Operation without Register Address

Register Reset Conditions

Type S: Registers are reset each time when SYS < POR (1.55V typ)

Type O: Registers are reset each time when SYS < SYS UVLO (2.55V max) or SYS > SYS OVLO or die temp > 165°C (or the MAX77840 transitions from on to off state)

Note: RSVD means the register bit is reserved for future use.

I²C Register Details

PMIC ID Register (0x00)

NAME		FUNCTION	ADDR	TYPE	RESET
PMIC ID		PMIC ID	0x00	O	0x40
BIT	MODE	NAME	RESET	DESCRIPTION	
7:4	R	ID_H	0100	ID of the MAX77840	
3:0	R	ID_L	0000		

Interrupt Source (0x22)

NAME		FUNCTION	ADDR	TYPE	RESET
INTSRC		Interrupt Source	0x22	S	0x00
BIT	MODE	NAME	RESET	DESCRIPTION	
7	R	RSVD	0	Reserved	
6	R	RSVD	0	Reserved	
5	R	B2SOVRC_INT	0	Battery to SYS Overvoltage Interrupt 0 = No B2SOVRC Interrupt detected 1 = B2SOVRC Interrupt detected	
4	R	RSVD	0	RSVD	
3	R	CHGDET_INT	0	Charger Detect Interrupt 0 = No interrupt detected in Charger Detect block 1 = Interrupt detected in Charger Detect block	
2	R	FG_INT	0	Fuel Gauge Interrupt 0 = No interrupt detected from FG block 1 = Interrupt from FG block is detected	
1	R	SYS_INT	0	SYS Interrupt 0 = No SYS interrupt detected 1 = SYS interrupt detected	
0	R	CHGR_INT	0	Charger Interrupt 0 = No interrupt detected in Charger block 1 = Interrupt detected in Charger block	

Interrupt Source Mask (0x23)

NAME		FUNCTION	ADDR	TYPE	RESET
INTSRCMASK		Interrupt Source Mask	0x23	S	0xFF
BIT	Mode	Name	Reset	Description	
7	R/W	RSVD	1	Reserved	
6	R/W	RSVD	1	Reserved	
5	R/W	B2SOVRC_INT_MASK	1	Battery to SYS Overvoltage Interrupt Mask 0 = B2SOVRC Interrupt is not masked 1 = B2SOVRC Interrupt is masked	
4	R/W	RSVD	1	RSVD	
3	R/W	CHGDET_INT_MASK	1	Charger Detect Interrupt Mask 0 = Charger Detect Interrupt is not masked 1 = Charger Detect Interrupt is masked	
2	R/W	FG_INT_MASK	1	Fuel Gage Interrupt Mask 0 = FG Interrupt is not masked 1 = FG Interrupt is masked	

NAME		FUNCTION	ADDR	TYPE	RESET
INTSRCMASK		**Interrupt Source Mask**	**0x23**	**S**	**0xFF**
BIT	**Mode**	**Name**	**Reset**	**Description**	
1	R/W	SYS_INT_MASK	1	SYS Interrupt Mask 0 = SYS interrupt is not masked 1 = SYS interrupt is masked	
0	R/W	CHGR_INT_MASK	1	Charger Interrupt 0 = Charger interrupt is not masked 1 = Charger interrupt is masked	

SYSTEM Interrupt (0x24)

NAME		FUNCTION	ADDR	TYPE	RESET
SYSINTSRC		**SYS Interrupt Source**	**0x24**	**S**	**0x00**
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/C	RSVD	0	Reserved	
6	R/C	TSHDN_INT	0	Temp Shutdown Interrupt 0 = No T_{SHDN} interrupt 1 = T_{SHDN} interrupt is detected	
5	R/C	SYSOVLO_INT	0	SYS OVLO Interrupt 0 = No SYSOVLO interrupt 1 = SYSOVLO interrupt is detected	
4	R/C	SYSUVLO_INT	0	SYS UVLO Interrupt 0 = No SYSUVLO interrupt 1 = SYSUVLO interrupt is detected	
3	R/C	LOWSYS_INT	0	LOWSYS Interrupt 0 = No LOWSYS interrupt 1 = LOWSYS interrupt is detected	
2	R/C	RSVD	0	Reserved	
1	R/C	T140C_INT	0	T140°C Interrupt 0 = No T140°C interrupt 1 = T140°C interrupt is detected; die temp > 140°C	
0	R/C	T120C_INT	0	T120°C Interrupt 0 = No T120°C interrupt 1 = T120°C interrupt is detected; die temp > 120°C	

SYSTEM Interrupt Source Mask (0x26)

NAME		FUNCTION	ADDR	TYPE	RESET
SYSINTMASK		**System Interrupt Mask**	**0x26**	**S**	**0xFF**
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	RSVD	1	Reserved	
6	R/W	TSHDN_INT_MASK	1	Temp Shutdown Interrupt Mask 0 = T_{SHDN} interrupt is not masked 1 = T_{SHDN} interrupt is masked	
5	R/W	SYSOVLO_INT_MASK	1	SYS OVLO Interrupt Mask 0 = SYSOVLO interrupt is not masked 1 = SYSOVLO interrupt is masked	
4	R/W	SYSUVLO_INT_MASK	1	SYS UVLO Interrupt Mask 0 = SYSUVLO interrupt is not masked 1 = SYSUVLO interrupt is masked	

NAME		FUNCTION	ADDR	TYPE	RESET
SYSINTMASK		**System Interrupt Mask**	**0x26**	**S**	**0xFF**
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
3	R/W	LOWSYS_INT_MASK	1	LOWSYS Interrupt Mask 0 = LOWSYS interrupt is not masked 1 = LOWSYS interrupt is masked	
2	R/W	RSVD	1	Reserved	
1	R/W	T140C_INT_MASK	1	T140C Interrupt Mask 0 = T140°C interrupt is not masked 1 = T140°C interrupt is masked	
0	R/W	T120C_INT_MASK	1	T120C Interrupt Mask 0 = T120°C interrupt is not masked 1 = T120°C interrupt is masked	

Top SYS Status Register (0x28)

NAME		FUNCTION	ADDR	TYPE	RESET
TOPSYS_STAT		**Top SYS Status**	**0x28**	**O**	**0x00**
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R	RSVD	0	Reserved	
6	R	TSHDN_STAT	0	Thermal Shutdown Status 0 = Not Thermal Shutdown 1 = Thermal Shutdown	
5	R	SYSOVLO_STAT	0	SYS OVLO Status 0 = SYS is below OVLO threshold 1 = SYS is above OVLO threshold	
4	R	SYSUVLO_STAT	0	SYS UVLO Status 0 = SYS is above UVLO threshold 1 = SYS is below UVLO threshold	
3	R	LOWSYS_STAT	0	LOWSYS Status 0 = SYS is above the Low SYS threshold 1 = SYS is below the Low SYS threshold	
2	R	RSVD	0	Reserved	
1	R	T140C_STAT	0	T140C Thermal Status 0 = T_{DIE} < 140°C 1 = T_{DIE} > 140°C	
0	R/C	T120C_INT	0	T120C Thermal Status 0 = T_{DIE} < 120°C 1 = T_{DIE} > 120°C	

Low SYS Detection Configuration (0x2B)

NAME		FUNCTION	ADDR	TYPE	RESET
LSCNFG		**Low SYS Detect Status**	**0x2B**	**S**	**0x1E**
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	LSEN	0	Low SYS DAC enable. With LSEN = 1, the low SYS DAC output is available as an interrupt. 0 = DAC disabled (reduce supply current) 1 = DAC enabled	

NAME		FUNCTION	ADDR	TYPE	RESET
LSCNFG		**Low SYS Detect Status**	**0x2B**	**S**	**0x1E**
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
6:5	R/W	LSHYST	00	Low SYS comparator hysteresis. 00 = 100mV (default) 01 = 200mV 10 = 300mV 11 = 400mV	
4:1	R/W	LSDAC	1101	Low SYS DAC voltage that sets the V_{SYS} falling threshold, programmed in 50mV steps from 2.85V to 3.60V. 0x00 = 2.85V 0x01 = 2.90V 0x02 = 2.95V ... 0x05 = 3.10V ... 0x0D = 3.50V 0x0E = 3.55V 0x0F = 3.60V (default)	
0	R/W	BIASEN	0	BIAS enable. BIAS must be enabled for SYS_OVLO and TSHDN detection. 0: BIAS disabled 1: BIAS enabled	

SAFEOUT Control Register (0xC6)

NAME		FUNCTION	ADDR	TYPE	RESET
SAFEOUTCTRL		**SAFEOUT Linear regulator control**	**0xC6**	**O**	**0x75**
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	RSVD	0	Reserved	
6	R/W	ENSAFEOUT	1	SAFEOUT LDO enable bit 0 = Disable SAFEOUT LDO 1 = Enable SAFEOUT LDO	
5	R/W	RSVD	1	Reserved	
4	R/W	ACTDISSAFEO	1	SAFEOUT LDO active discharge enable bit 0 = No active discharge 1 = Active discharge	
3:2	R/W	RSVD	01	Reserved	
1:0	R/W	SAFEOUT[1:0]	01	SAFEOUT LDO output voltage setting 00 = 4.85V 01 = 4.90V (default) 10 = 4.95V 11 = 3.30V	

Soft-Reset Register (0x50)

NAME		FUNCTION	ADDR	TYPE	RESET
SOFT_RST		**Soft-Reset Register**	**0x50**	**O**	**0x00**
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:0	R/W	SOFT_RST	0	Soft Reset When the register is written to with a value of "0xA5", all other type S and type O functional registers are reset to the default value. When the register is set to any other value other than "0xA5", there is no impact on other type S or type O functional register values.	

Detailed Description—ONKEY

ONKEY

The ONKEY can be used to turn on the device as well as to reset the system. The ONKEY input is active-low and falling-edge triggered.

When the device is powered by battery only and in factory shipping mode, the QBAT switch is open and SYS is isolated from BAT. With a healthy battery, pressing the ONKEY for longer than the device on debounce time (800ms default) closes the QBAT switch and connects SYS to BAT.

The system can be reset by pressing the ONKEY for longer than the hardware reset debounce time (7s), as shown in Figure 19.

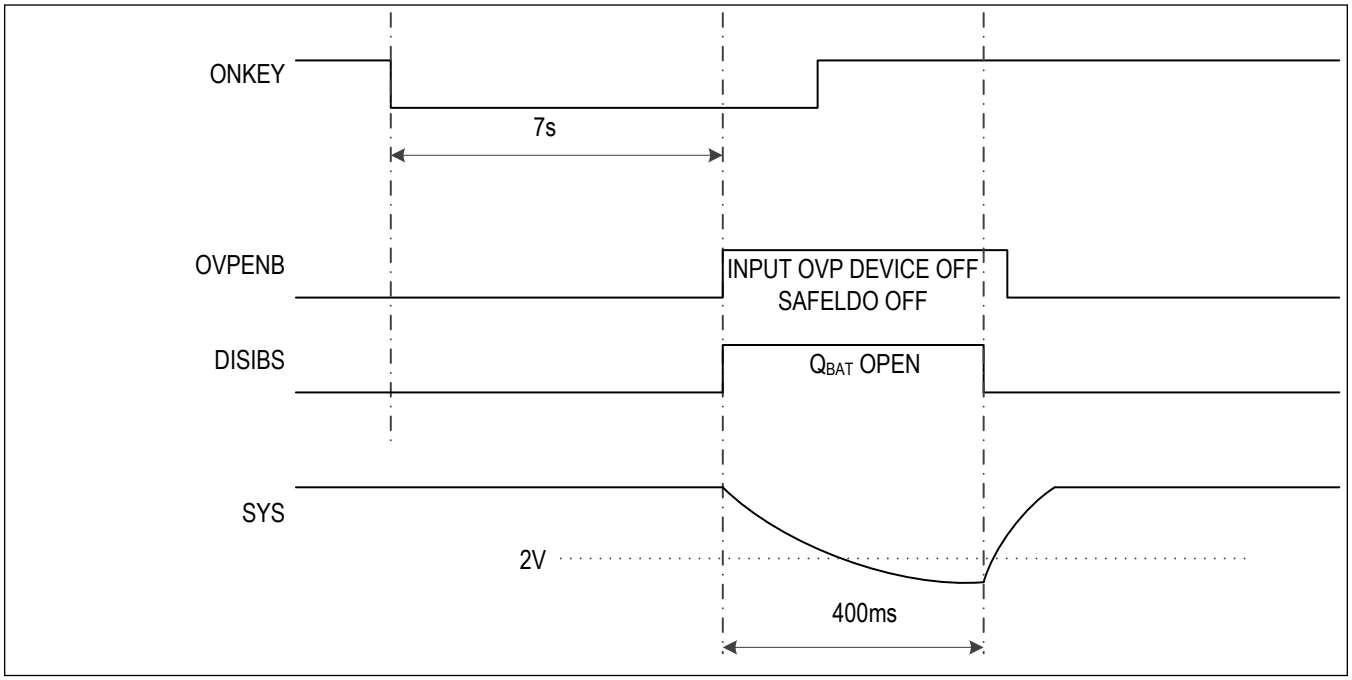


Figure 19. ONKEY Timing Diagram

Detailed Description—SAFEOUT LDO

The SAFEOUT LDO is a linear regulator that provides programmable output voltage of 3.30V/4.85V/4.90V/4.95V using the I^2C register which can be used to supply low-voltage rated USB systems. The SAFEOUT linear regulator turns on when CHGIN ≥ 3.2V regardless if the charger is enabled or disabled. SAFEOUT is disabled when CHGIN is greater than the overvoltage threshold. The SAFEOUT LDO integrates a high-voltage MOSFETs to provide 20V protection at their inputs, which are internally connected to the charger input at CHGIN. SAFEOUT is ON by default at 4.9V.

Detailed Description—ModelGauge m5 Fuel Gauge

ModelGauge m5 Details

The MAX77840 incorporates the Maxim Integrated ModelGauge m5 algorithm that combines the excellent short-term accuracy and linearity of a coulomb counter with the excellent long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel-gauge accuracy. The device also includes Cycle+ charger control, improved age adaptation, improved state-of-charge (SOC) accuracy to empty, and increased temperature measurement accuracy. ModelGauge m5 cancels offset accumulation error in the coulomb counter while providing better short-term accuracy than any purely voltage-based fuel gauge. Additionally, the ModelGauge m5 algorithm does not

suffer from abrupt corrections that normally occur in coulomb-counter algorithms since tiny continual corrections are distributed over time. The device automatically compensates for aging, temperature, and discharge rate and provides accurate SOC in mAh or % over a wide range of operating conditions. The device provides two methods for reporting the age of the battery: reduction in capacity and cycle odometer. The device provides precision measurements of current, voltage, and temperature. Temperature of the battery pack is measured using an external thermistor supported by ratiometric measurements on an auxiliary input. A 2-wire (I^2C) interface provides access to data and control registers.

ModelGauge m5 Algorithm

The ModelGauge m5 algorithm combines a high-accuracy coulomb counter with a voltage fuel gauge (VFG), as described in Figure 20. Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance, however they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated thus causing the reported capacity error to increase over time and require periodic corrections (corrections are usually performed at full or empty).

Some other systems also use the relaxed battery voltage to perform corrections. These systems determine the SOC based on the battery voltage after a long time of no current flow. Both have the same limitation; if the correction condition is not observed over time in the actual application, the error in the system is boundless. The performance of classic coulomb counters is dominated by the accuracy of such corrections. Classical voltage-measurement-based SOC estimation has poor accuracy due to inadequate cell modeling, but does not accumulate offset error over time. The device includes an advanced VFG which estimates open-circuit voltage (OCV) even during current flow and simulates the nonlinear internal dynamics of a lithium-ion (Li+) battery to determine the SOC with improved accuracy.

The model considers the time effects of a battery caused by the chemical reactions and impedance in the battery to determine SOC based on table lookup. This SOC estimation does not accumulate offset error over time. The ModelGauge m5 algorithm combines a high-accuracy coulomb counter with a VFG; the complementary combined result eliminates the weaknesses of both the coulomb counter and the VFG while providing the strengths of both. A mixing algorithm combines the VFG capacity with the coulomb counter and weights each result so that both are used optimally to determine the battery state. In this way, the VFG capacity result is used to continuously make small adjustments to the battery state thus canceling the coulomb-counter drift.

The ModelGauge m5 algorithm uses this battery state information and accounts for temperature, battery current, age, and application parameters to determine the remaining capacity available to the system. The ModelGauge m5 algorithm continually adapts to the cell and application through independent learning routines. As the cell ages, its change in capacity is monitored and updated and the VFG dynamics adapt based on cell voltage behavior in the application.

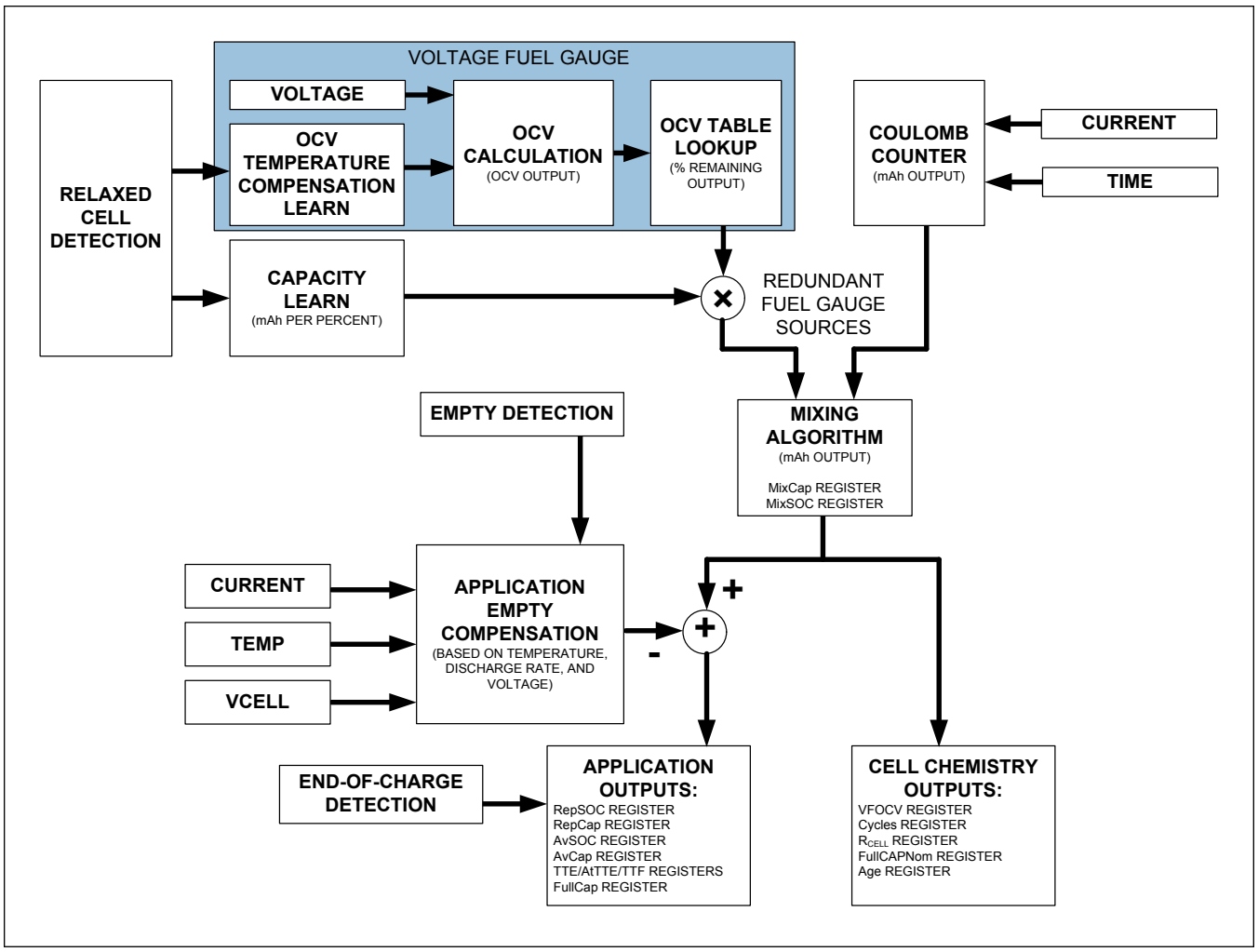


Figure 20. ModelGauge m5 Block Diagram

OCV Estimation and Coulomb-Count Mixing

The core of the ModelGauge m5 algorithm is a mixing algorithm that combines the OCV state estimation with the coulomb counter. After power-on reset of the IC, coulomb-count accuracy is unknown. The OCV state estimation is weighted heavily compared to the coulomb-count output. As the cell progresses through cycles in the application, coulomb-counter accuracy improves and the mixing algorithm alters the weighting so that the coulomb-counter result is dominant. From this point forward, the IC switches to servo mixing; servo mixing provides a fixed magnitude continuous error correction to the coulomb count (up or down) based on the direction of error from the OCV estimation. This allows differences between the coulomb count and OCV estimation to be corrected quickly. The resulting output from the mixing algorithm does not suffer drift from current measurement offset error and is more stable than a stand-alone OCV estimation algorithm. Initial accuracy depends on the relaxation state of the cell. The highest initial accuracy is achieved with a fully relaxed cell.

Fuel-Gauge Empty Compensation

As the temperature and discharge rate of an application changes, the amount of charge available to the application also changes. The ModelGauge m5 algorithm distinguishes between the remaining capacity of the cell (RemCapMIX) and the remaining capacity of the application (RemCapAV) and reports both results to the user.

Fuel-Gauge Learning

The device periodically makes internal adjustments to cell characterization and application information to remove initial error and maintain accuracy as the cell ages. These adjustments always occur as small undercorrections to prevent instability of the system and prevent any noticeable jumps in the fuel-gauge outputs. Learning occurs automatically without any input from the host. To maintain learned accuracy through power loss, the host must periodically save learned information and then restore after power is returned. See the *Power-Up and Power-On Reset* section for details.

- **Full Capacity Available to Application (FullCAP)**: This is the total capacity available to the application when full. FullCAP is updated near the end of charging when termination is detected. See the *End-of-Charge Detection* section.
- **Cell Capacity (FullCapNom)**: This is the total cell capacity at full, according to the VFG. This includes some capacity that is not available to the application at high loads and/or low temperature. The device periodically compares percent change based on OCV measurement versus coulomb-count change as the cell charges and discharges. This information allows the device to maintain an accurate estimation of the cell's capacity in milliamp-hours as the cell ages.
- **Voltage Fuel-Gauge Adaptation:** The device observes the battery's relaxation response and adjusts the dynamics of the VFG. This adaptation adjusts the RCOMP0 register during qualified cell relaxation events.
- **Empty Compensation:** The device updates internal data whenever cell empty is detected (VCELL < V_empty) to account for cell age or other cell deviations from the characterization information.

Determining Fuel-Gauge Accuracy

To determine the true accuracy of a fuel gauge as experienced by end users, the battery should be exercised in a dynamic manner since the end-user accuracy cannot be understood only with simple cycles. To challenge a correction-based fuel gauge such as a coulomb counter, test the battery with partial loading sessions. For example, a typical user can operate a device for ten minutes and then stop use for an hour or more. A robust test method includes these kinds of sessions many times at various loads, temperatures, and duration.

Initial Accuracy

The device uses the first voltage reading after power-up or after cell insertion to determine the starting output of the fuel gauge. It is assumed that the cell is fully relaxed prior to this reading, however this is not always the case. If the cell was recently charged or discharged, the voltage measured by the device might not represent the true state of charge of the cell resulting in initial error in the fuel-gauge outputs. In most cases, this error is minor and is quickly removed by the fuel-gauge algorithm during normal operation.

Cycle+ Charger Control

ModelGauge m5 fuel gauge is internally paired with a programmable high voltage, high current charger. The charger has adjustable JEITA thresholds and works with the Cycle+ scheme to control the charge current versus state-of-charge. In addition, Cycle+ provides SmartFull charge termination which can control charger charge-termination according to the OCV prediction of the fuel gauge. This helps to support more accurate charge termination and is less sensitive to system load transients at the end of charging.

End-of-Charge Detection

The device detects the end of a charge cycle when the application current falls into the band set by the ICHGTerm register value. By monitoring both the current and average current registers, the device can reject false end-of-charge events such as application load spikes or early charge-source removal. When a proper end-of-charge event is detected, the device learns a new FullCAP register value based on the RemCapREP output. If the old FullCAP value was too high, it is adjusted downward after the last valid end-of-charge detection. If the old FullCAP was too low, it is adjusted upward to match RemCapREP. This prevents the calculated state of charge from ever reporting a value greater than 100%.

Power-Up and Power-On Reset

Any power-on reset (POR) of the device resets all memory locations to their default POR value. This removes any custom cell characterization and application data, affects ALRT interrupt and shutdown mode settings, and resets all learned adjustments made by the fuel gauge. To maintain accuracy of the fuel gauge and reset operation settings of the device, the host must reload all application memory data and restore all learned fuel gauge information. Note that the device can

take up to 445ms to completely reset operation after a POR event occurs. Saved data should not be restored until after this period is over. The following procedure is recommended:

- Read Status register. If POR = 0, exit.
- Wait 600ms for POR operation to fully complete.
- Restore all application register values.
- Restore fuel gauge learned-value information (see the *Save and Restore Registers* section).
- Clear POR bit.

Save and Restore Registers

The device is designed to operate outside the battery pack and can therefore be exposed to power loss when in the application. To prevent the loss of learned information during power cycles, a save-and-restore procedure can be used to maintain register values in nonvolatile memory external to the device. The registers (see Table 3) must be stored externally and then rewritten to the device after power-up to maintain a learned state of operation. Note that some registers are application outputs, some registers are for internal calculations, and some are characterization setup registers. Registers that are not internal are described in their own sections. These values should be stored by the application at periodic intervals. Some recommended back-up events are:

- End-of-charge
- End-of-discharge
- Prior to application entering shutdown state

The host is responsible for loading the default characterization data at first power-up of the device and restoring the default characterization data plus learned information on subsequent power-up events.

Cell Insertion (IC Already Powered)

The device is ready to detect a cell insertion if either the ETHRM or FTHRM bits of the CONFIG register are set to enable the THRM pin output. When a cell insertion is detected, the fuel gauge is reset and all fuel-gauge outputs are updated to reflect the SOC of the newly inserted cell. This process can take up to 1.845s (FTHRM = 0) or 620ms (FTHRM = 1) from time of insertion. Note that the device uses the cell voltage as a starting point for the fuel gauge. If the cell voltage is not fully relaxed at time of insertion, the fuel gauge begins with some initial error. See the *Fuel-Gauge Learning* section for details. The device can also be configured to alert the host when cell insertion occurs. When Bei = 1 in the CONFIG register, the device generates an interrupt on the ALRT pin at the start of the first temperature conversion after insertion. This could take up to 1.4s to occur. This feature is useful if the application uses more than one cell type and the device must be reconfigured at each insertion.

Cell Removal

The device detects a cell removal if either the ETHRM or FTHRM bits of the CONFIG register are set to enable the THRM pin output. Cell removal does not affect IC operation and the device continues to update fuel-gauge outputs. The host should monitor the Br and Bst bits of the Status register to determine if the fuel-gauge outputs are valid. The device can also be configured to alert the host when cell removal occurs. When Ber = 1 in the CONFIG register, the device generates an interrupt on the ALRT pin at the start of the first temperature conversion after removal. This could take up to 1.4s to occur. This feature is useful if the application uses more than one cell type and the device must be reconfigured at each insertion.

Fast Detection of Cell Removal

The device can be configured to quickly alert the host of impending power loss on cell removal. This fast response allows the system to quickly and gracefully hibernate to prevent power loss during battery swap. When Ber = 1, FTHRM = 1, and ALRTp = 0 in the CONFIG register, an interrupt on the ALRT pin is generated within 100µs after VAIN becomes greater than VTHRM - VDETR. If fast detection is used, it is recommended that all other IC interrupts are disabled to prevent the host from spending time determining the cause of the interrupt. Fast detection of cell removal has no effect on fuel-gauge operation, but leaving the external resistor-divider active increases current consumption of the application.

Modes of Operation

The device operates in one of two power modes, active or shutdown. While in active mode, the device operates as a high-

precision battery monitor with temperature, voltage, auxiliary inputs, current, and accumulated current measurements acquired continuously and the resulting values are updated in the measurement registers. READ and WRITE access is allowed only in active mode. In shutdown mode, the LDO is disabled and all activity stops although volatile RAM contents remain preserved. All A/D register and fuel-gauge output values are maintained. There are several options for entering shutdown.

Entering shutdown:

- **SHUTDOWN Command:** Write the CONFIG register SHDN = 1 through the I2C interface; wait for longer than the SHDNTIMER register value.
- **Pack Removal:** Pack removal detection is valid for longer than the SHDNTIMER register value and the CONFIG register AINSH = 1.
- **I2C Shutdown:** I2C lines both persist low for longer than the SHDNTIMER register value and the CONFIG register I2CSH = 1.
- **ALRT Shutdown:** Shutdown occurs when the ALRT line is externally driven low for longer than the SHDNTIMER register value (ALSH = 1 and ALRTp = 0), or the ALRT line is externally driven high for longer than the SHDNTIMER register value (ALSH = 1 and ALRTp = 1). See the CONFIG Register (1dh) section.

These shutdown entry modes are all programmable according to the application. Shutdown events are gated by the SHDNTIMER register, which allows a long delay between the shutdown event and the actual shutdown. By behaving this way, the device takes the best reading of the relaxation voltage.

Exiting shutdown:

- **I2C Wakeup:** Any edge on SCL/SDA.
- **ALRT Wakeup:** Any edge on ALRT line and ALSH = 1 or I2CSH = ALSH = 0.
- **Reset:** IC is power cycled.

See the *Status and Configuration Registers* section for detailed descriptions of the SHDNTIMER and CONFIG registers. The state of the device when returning to active mode differs depending on the triggering event. The host software can monitor the POR and Bi status bits to determine what type of event has occurred.

ALRT Function

The Alert Threshold registers allow interrupts to be generated by detecting a high or low voltage, temperature, or SOC. Interrupts are generated on the ALRT pin open-drain output driver. An external pullup is required to generate a logic-high signal. Note that if the pin is configured to be logic-low when inactive, the external pullup increases current drain. The ALRTp bit in the CONFIG register sets the polarity of the ALRT pin output. Alerts can be triggered by any of the following conditions:

- **Battery Removal:** (VAIN > VTHRM - VDETR) and battery removal detection enabled (Ber = 1).
- **Battery Insertion:** (VAIN < VTHRM - VDETF) and battery insertion detection enabled (Bei = 1).
- **Over/Under Voltage:** VALRT threshold violation (upper or lower) and alerts enabled (Aen = 1).
- **Over/Under Temperature:** TALRT threshold violation (upper or lower) and alerts enabled (Aen = 1).
- **Over/Under SOC:** SALRT threshold violation (upper or lower) and alerts enabled (Aen = 1).
- **dSOC:** 1% change in SOC (Config.dSOC = 1).
- **Charger Communication Failure:** Set when FG fails to communicate with the charger. Controlled by Config.FCFE and Config.ICFE.

To prevent false interrupts, the threshold registers should be initialized before setting the Aen bit. Alerts generated by battery insertion or removal can only be reset by clearing the corresponding bit in the status register. Alerts generated by a threshold-level violation can be configured to be cleared only by software or cleared automatically when the threshold level is no longer violated. See the CONFIG (1Dh) register description for details of the alert function configuration.

IC Memory Map

The device has a 256-word linear memory space containing all user-accessible registers. All registers are 16 bits wide and are read and written as 2-byte values. When the MSB of a register is read, the MSB and LSB are latched simultaneously and held for the duration of the Read Data command. This prevents updates to the LSB during the read, ensuring synchronization between the two register bytes. All locations are volatile RAM and lose their data in the event of power loss. Data is retained during device shutdown. Each register has a power-on-reset value that it defaults to at

power-up. Word addresses designated as reserved return an undetermined value when read. These locations should not be written to.

ModelGauge m5 Registers

All ModelGauge m5 registers are shown in Table 3. The register address is composed of two HEX digits shown in the first row and first column. All the registers are grouped by their functions and described in the *ModelGauge m5 Output Registers* section.

Table 3. ModelGauge m5 Registers

0x6C I²C COMMAND ADDRESS	0x0_	0x1_	0x2_	0x3_	0x4_	0x5_ 0x7_	0x8_	0x9_	0xA_	0xB_	0xC_	0xD_	0xE_	0xF_
0x0_0	STATUS	FullCAP	TTF	Reserved	Reserved	Reserved	OCV	CAP	RCOMPseg	Status2	Reserved	Reserved	Reserved	Reserved
0x0_1	VALRT_Th	TTE	DevName	Reserved	Reserved					Reserved		ChargeState0		Reserved
0x0_2	TALRT_Th	QRtable00	QRtable10	QRtable20	QRtable30					TALRT_Th2		ChargeState1		Reserved
0x0_3	SALRT_Th	FullSOCthr	FullCAPNom	Reserved	Reserved					Reserved		ChargeState2		Reserved
0x0_4	AtRate	RSLOW	TempNom	Reserved	Reserved					Reserved		ChargeState3		Reserved
0x0_5	RepCap	Reserved	TempLim	FullCapRep	dQ_acc					TTF_CFG		ChargeState4		Reserved
0x0_6	RepSOC	AvgTA	Reserved	Iavg_empty	dP_acc					CV_MixCap		ChargeState5		Reserved
0x0_7	Age	Cycles	AIN0	FCTC	Reserved					CV_HalfTime		ChargeState6		Reserved
0x0_8	TEMP	DesignCap	LearnCFG	RCOMP0	Reserved					Reserved		ChargeState7		Reserved
0x0_9	VCELL	AvgVCELL	FilterCFG	TempCo	ConvgCfg					Curve		JEITA_Volt		Reserved
0x0_A	Current	MaxMinTemp	RelaxCFG	V_empty	VFRemCap					Reserved		JEITA_Curr		Reserved
0x0_B	AvgCurrent	MaxMinVolt	MiscCFG	Reserved	Reserved					Config2		SmartChgCfg		VFOCV
0x0_C	Qresidual	MaxMinCurr	TGAIN	Reserved	Reserved					Vripple		AtQresidual		Reserved
0x0_D	MixSOC	CONFIG	TOFF	Reserved	QH					RippleCfg		AtTTE		Reserved

Table 3. ModelGauge m5 Registers (continued)

0x6C I²C COMMAND ADDRESS	0x0_	0x1_	0x2_	0x3_	0x4_	0x5_ 0x7_	0x8_	0x9_	0xA_	0xB_	0xC_	0xD_	0xE_	0xF_
0x0_E	AvSOC	ICHGTerm	CGAIN	TIMER	Reserved					TIMERH		AtAvSOC		Reserved
0x0_F	MixCap	AvCap	COFF	SHDNTIMER	Reserved					MaxError		AtAvCap		VFSOC

Register Details

JEITA Charging Registers

TAlrtTh (0x02)

Bitfield	Bits	Description	Decode
MaxTempAlrt	15:8	Sets an alert threshold for maximum temperature.	Set Max = 0x7F to disable. Units of LSB are 1˚C.
MinTempAlrt	7:0	Sets an alert threshold for minimum temperature.	Set Min = 0x80 to disable. Units of LSB are 1˚C.

TAlrtTh2 (0xB2)

Bitfield	Bits	Description	Decode
TempWarm	15:8	Temperature threshold used for smart charging as T4	Units of LSB are 1˚C. Set to 0x7F to disable.
TempCool	7:0	Temperature threshold used for smart charging as T1	Units of LSB are 1˚C. Set to 0x80 to disable.

JEITA_Volt (0xD9)

The Jeita_Volt register defines the charge voltage for each of the temperature ranges. Each bit represents 25mV. Note that hot and cold temperature charge voltage can only be set up to 4.4V, and room temperature charge voltage can be set to 4.7V. The temperature limits are determined by the TALRT_Th and TALRT_Th2 registers.

Name		Function	Addr	Type	Reset
JEITA_Volt		JEITA Charge Termination Voltage Setting	0x0D9	O	0xA516
BIT	Mode	Name	Reset	Description	
15:11	RW	ColdChargeV	0x24	ColdChargeV defines the charge voltage between temperatures T1 and T2 (default 4.150V). See the following bit breakdown.	
10:6	RW	HotChargeV	0x24	HotChargeV defines the charge voltage between temperatures T3 and T4 (default 4.150V). See the following bit breakdown.	
5:0	RW	RoomChargeV	0x16	RoomChargeV defines the charge voltage between temperatures T2 and T3 (default 4.200V). See the following bit breakdown.	

JEITA_Volt Register bit breakdown settings:

Bits	(V)	Bits	(V)	Bits	(V)
0x00	3.650	0x10	4.050	0x20	4.425
0x01	3.675	0x11	4.075	0x21	4.450
0x02	3.700	0x12	4.100	0x22	4.475
0x03	3.725	0x13	4.125	0x23	4.500

0x04	3.750	0x14	4.150	0x24	4.525
0x05	3.775	0x15	4.175	0x25	4.550
0x06	3.800	0x16	4.200	0x26	4.575
0x07	3.825	0x17	4.225	0x27	4.600
0x08	3.850	0x18	4.250	0x28	4.625
0x09	3.875	0x19	4.275	0x29	4.650
0x0A	3.900	0x1A	4.300	0x2A	4.675
0x0B	3.925	0x1B	4.325	0x2B	4.700
0x0C	3.950	0x1C	4.340		
0x0D	3.975	0x1D	4.350		
0x0E	4.000	0x1E	4.375		
0x0F	4.025	0x1F	4.400		

JEITA_Curr (0xDA)

The JEITA_Curr register controls the relative charge current. The relative values scale the charge current specified in the ChargeState registers. The temperature limits are determined by the TALRT_Th and TALRT_Th2 registers.

Name		Function	Addr	Type	Reset
JEITA_Curr		JEITA Charge Current Control	0x0DA	O	0x4350
BIT	**Mode**	**Name**	**Reset**	**Description**	
15:11	RW	ColdCoeff	0x08	Charging current coefficient when the temperature is between T1 and T2 (default 50%). See the following bit breakdown.	
10:6	RW	HotCoeff	0x0D	Charging current coefficient when temperature is between T3 and T4 (default 81%). See the following bit breakdown.	
5:0	RW	RoomCoeff	0x10	Charging current coefficient when temperature is between T2 and T3 (default 100%). See the following bit breakdown.	

JEITA Charge Current Control bit breakdown settings:

Bits	Coefficient (%)	Bits	Coefficient (%)
0x00	0%	0x10	100%
0x01	6%	0x11	106%
0x02	13%	0x12	113%
0x03	19%	0x13	119%
0x04	25%	0x14	125%
0x05	31%	0x15	131%
0x06	38%	0x16	138%
0x07	44%	0x17	144%
0x08	50%	0x18	150%
0x09	56%	0x19	156%
0x0A	63%	0x1A	163%
0x0B	69%	0x1B	169%
0x0C	75%	0x1C	175%
0x0D	81%	0x1D	181%
0x0E	88%	0x1E	188%
0x0F	94%	0x1F	194%

ChargeState(0-7) (0xD1 – 0xD8)

The charge state registers control the charge current in each SOC state. The high byte controls the percentage added to the first state. For example, the ChargeState0 high byte will add to 0% and the ChargeState1 will add the high byte to the ChargeState0 high byte. The low byte controls the charge current for each state.

Name		Function	Addr	Type	Reset
ChargeState (0-7)		Smart Charge Charge State	0x0D1 to 0x0D8	O	0x0C09
BIT	**Mode**	**Name**	**Reset**	**Description**	
15:8	RW	Domain(0-7)_SOC	0x0C	0xnnmm: ChargeState1 = 0x0C36; 2700mA; SOC: 16-28%. 0xnn for percentage to be added to the previous one. 0x0C is 12% to add to 16%, so it becomes 28%. 0xmm for the maxim charge current for that percentage range.	
7:0	RW	Domain(0-7)_ ChargeCurrent	0x09	Fast Charge Current Selection. When the charger is enabled, the charge current limit is set by these bits. These bits range from 0.1A (0x01) to 3.0A (0x3C) in 50mA steps. **Note that the codes 0x01 and 0x02 are both 100mA and 0x09 is the default. Code 0x00 is reserved and must not be used.**	

Bits	(mA)	Bits	(mA)	Bits	(mA)	Bits	(mA)
0x00	-	0x10	800	0x20	1600	0x30	2400
0x01	100	0x11	850	0x21	1650	0x31	2450
0x02	100	0x12	900	0x22	1700	0x32	2500
0x03	150	0x13	950	0x23	1750	0x33	2550
0x04	200	0x14	1000	0x24	1800	0x34	2600
0x05	250	0x15	1050	0x25	1850	0x35	2650
0x06	300	0x16	1100	0x26	1900	0x36	2700
0x07	350	0x17	1150	0x27	1950	0x37	2750
0x08	400	0x18	1200	0x28	2000	0x38	2800
0x09	450	0x19	1250	0x29	2050	0x39	2850
0x0A	500	0x1A	1300	0x2A	2100	0x3A	2900
0x0B	550	0x1B	1350	0x2B	2150	0x3B	2950
0x0C	600	0x1C	1400	0x2C	2200	0x3C	3000
0x0D	650	0x1D	1450	0x2D	2250	0x3D	3000
0x0E	700	0x1E	1500	0x2E	2300	0x3E	3000
0x0F	750	0x1F	1550	0x2F	2350	0x3F	3000

SmartChgCfg (0xDB)

Bitfield	Bits	Description	Decode
DisJEITA	5	Set 1 to disable JEITA battery temperature monitor adjustments	
UseVF	4		0x0: MixSOC is an input SOC for SmartCharging 0x1: VFSOC is an input SOC for SmartCharging
EnsC	1	Set 1 to enable SmartCharing	
EnSF	0	Set 1 to enable SmartFull	

Status and Configuration Registers

Status (0x00)

Interrupt status register for the FG block.

Bitfield	Bits	Description	Decode
Br	15	Battery Removal	This bit is set to 1 when the device detects that a battery has been removed from the system. This bit must be cleared by system software to detect the next removal event. Br is set to 0 at power-up.
Smx	14	Maximum SOCALRT Threshold Exceeded	This bit is set to 1 whenever SOC rises above the maximum SOCALRT value. This bit might not need to be cleared by system software to detect the next event. See SS in the CONFIG register and SACFG in the MiscCFG register. Smx is set to 0 at power-up.
Tmx	13	Maximum TALRT Threshold Exceeded	This bit is set to 1 whenever a Temperature register reading is above the maximum TALRT value. This bit might not need to be cleared by system software to detect the next event. See TS in the CONFIG register. Tmx is set to 0 at power-up.
Vmx	12	Maximum VALRT Threshold Exceeded	This bit is set to 1 whenever a VCELL register reading is above the maximum VALRT value. This bit might not need to be cleared by system software to detect the next event. See VS in the CONFIG register. Vmx is set to 0 at power-up.
Bi	11	Battery Insertion	This bit is set to 1 when the device detects that a battery has been inserted into the system by monitoring the THM pin. This bit must be cleared by system software to detect the next insertion event. Bi is set to 0 at power-up.
Smn	10	Minimum SOCALRT Threshold Exceeded	This bit is set to 1 whenever SOC falls below the minimum SOCALRT value. This bit might not need to be cleared by system software to detect the next event. See SS in the CONFIG register and SACFG in the MiscCFG register. Smn is set to 0 at power-up.
Tmn	9	Minimum TALRT Threshold Exceeded	This bit is set to 1 whenever a Temperature register reading is below the minimum TALRT value. This bit might not need to be cleared by system software to detect the next event. See TS in the CONFIG register. Tmn is set to 0 at power-up.
Vmn	8	Minimum VALRT Threshold Exceeded	This bit is set to 1 whenever a VCELL register reading is below the minimum VALRT value. This bit might not need to be cleared by system software to detect the next event. See VS in the CONFIG register. Vmn is set to 0 at power-up.
dSOCi	7	1% SOC Change Alert	This bit is set to 1 to indicate a 1% SOC change alert. dSOCi is set to 0 at power-up.
ThmHot	6	FG Control Charger Input Current Limit	Set to 1 to indicate a Thermistor Hot alert to allow fuel gauge to control charger input current limit. ThmHot is set to 0 at power-up.
SPR_5	5	Reserved	
Isysmx	4	SYS current is over OCP limit.	Maximum SYS current threshold exceeded.
Bst	3	Battery Status	This bit is set to 0 when a battery is present in the system and set to 1 when the battery is removed. Bst is set to 0 at power-up.
SPR_2	2	Reserved	
POR	1	Power-On Reset	This bit is set to 1 when the device detects that a software or hardware POR event has occurred. If the host detects that the POR bit has been set, the device should be reconfigured (see the *Power-Up and Power-On Reset* section). This bit must be cleared by system software to detect the next POR event. POR is set to 1 at power-up.

Bitfield	Bits	Description	Decode
Imn	0	Minimum ISYS Threshold Exceeded	Minimum SYS current threshold exceeded.

Status2 (0xB0)

The Status 2 register indicates when the battery is full or empty.

Bitfield	Bits	Description	Decode
SPR_15_6	15:6	Reserved	
FullDet	5	Fully_Charged.	Set FullDet = 1 VFSOC > 99%; cleared if VFSOC < 98.5%.
SPR_4_0	4:0	Reserved	

VAlrtTh (0x01)

Bitfield	Bits	Description	Decode
MaxVoltageAlrt	15:8	Sets an alert threshold for maximum voltage.	Set Max = 0xFF to disable. Units of LSB are 20mV.
MinVoltageAlrt	7:0	Sets an alert threshold for minimum voltage.	Set Min = 0x00 to disable. Units of LSB are 20mV.

SAlrtTh (0x03)

Bitfield	Bits	Description	Decode
MaxSocAlrt	15:8	Sets an alert for maximum SOC.	This can be used for charge/discharge termination, or for power-management near empty. Set Max = 0xFF to disable. Units of LSB are 1%.
MinSocAlrt	7:0	Sets an alert for minimum SOC.	This can be used for charge/discharge termination, or for power-management near empty. Set Min = 0x00 to disable. Units of LSB are 1%.

AtRate (0x04)

Bitfield	Bits	Description
AtRate	15:0	Host software should write the AtRate register with a negative two's-complement 16-bit value of a theoretical load current prior to reading any of the at-rate output registers (AtTTE, AtAvSOC, or AtAvCap).

Config (0x1D)

Bitfield	Bits	Description	Decode
FCFE	15	Fuel-Gauge Charger Fail Enable	Set to 1 to enable FGCHGFAIL interrupt to drive the INTB pin. This bit is not accessible by the fuel-gauge firmware.
Ss	14	SOC ALRT Sticky	When SS = 1, SOC alerts can only be cleared through software. When SS = 0, SOC alerts are cleared automatically when the threshold is no longer exceeded. SS is set to 0 at power-up.
Ts	13	Temperature ALRT Sticky	When TS = 1, temperature alerts can only be cleared through software. When TS = 0, temperature alerts are cleared automatically when the threshold is no longer exceeded. TS is set to 1 at power-up.
Vs	12	Voltage ALRT Sticky	When VS = 1, voltage alerts can only be cleared through software. When VS = 0, voltage alerts are cleared automatically when the threshold is no longer exceeded. VS is set to 0 at power-up.
FGCC	11	Fuel-Gauge Charger Control	Set to 1 to enable Cycle+ charge control (fuel-gauge controlled charging).

Bitfield	Bits	Description	Decode
AINSH	10	AIN Pin Shutdown	Set to 1 to enable device shutdown when the battery is removed. The IC enters shutdown if the THM pin remains high (AIN reading > VTHMB - VDETR) for longer than the timeout of the SHDNTIMER register. This also configures the device to wake up when THM is pulled low on cell insertion. AINSH is set to 0 at power-up. Note that if I2CSH and AINSH are both set to 0, the device wakes up on an edge of any of the SDA, SCL, or INTB pins.
Ten	9	Enable Temperature Channel	Set to 1 and set ETHRM or FTHRM to 1 to enable measurements on the THM pin. Ten is set to 1 at power-up.
Tex	8	Temperature External	When set to 1, the fuel gauge requires external temperature measurements to be written from the host. When set to 0, measurements on the THM pin are converted to a temperature value and stored in the Temperature register instead. Tex is set to 1 at power-up.
SHDN	7	Shutdown	Write this bit to logic 1 to force a shutdown of the device after timeout of the SHDNTIMER register. SHDN is reset to 0 at power-up and upon exiting shutdown mode.
I2CSH	6	I^2C Shutdown	Set to logic 1 to force the device to enter shutdown mode if both SDA and SCL are held low for more than timeout of the SHDNTIMER register. This also configures the device to wake up on a rising edge of either SDA or SCL. Set to 1 at power-up. Note that if I2CSH and AINSH are both set to 0, the device wakes up on an edge of any of the SDA, SCL, or INTB pins.
ICFE	5	I^2C Charge Fail Enable	Set to 1 to enable I2CChgFail interrupt to drive the INTB pin. This bit is not accessible by the fuel-gauge firmware.
ETHRM	4	Enable Thermistor	Set to logic 1 to enable the automatic THRM output bias and AIN measurement every 1.4s. This bit is set to 1 at power-up.
FTHRM	3	Force Thermistor Bias Switch. This allows the host to control the bias of the thermistor switch or enable fast detection of battery removal (see the *Fast Detection of Cell Removal* section).	Set FTHRM = 1 to always enable the thermistor bias switch. With a standard 10kΩ thermistor, this adds an additional ~200µA to the current drain of the circuit. This bit is set to 0 at power-up.
Aen	2	Enable alert on fuel-gauge outputs.	When Aen = 1, violation of any of the alert threshold register values by temperature, voltage, or SOC triggers an alert. This bit affects the INTB pin (FG_INT) operation only. The Smx, Smn, Tmx, Tmn, Vmx, and Vmn bits are not disabled. This bit is set to 0 at power-up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.
Bei	1	Enable alert on battery insertion.	When Bei = 1, a battery-insertion condition as detected by the THM pin voltage triggers an alert. Set to 0 at power-up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.
Ber	0	Enable alert on battery removal.	When Ber = 1, a battery-removal condition as detected by the THM pin voltage triggers an alert. Set to 0 at power-up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.

Config2 (0xBB)

Bitfield	Bits	Description	Decode
SPR_15_0	15:8	Reserved	
dSOCen	7	Set to 1 to enable a SOC 1% change alert. If dSCOCen = 0, the alert-on is disabled.	
TAlrtEn	6	Set to 1 to enable a temperature alert. If TAlrtEn = 0, the alert-on is disabled.	

Bitfield	Bits	Description	Decode
LdMdl	5	Host sets this bit to 1 in order to initiate firmware to finish processing a newly loaded model. Firmware clears this bit to zero to indicate that model loading is finished.	
OCVQen	4	Set OCVQen = 1 to enable automatic empty compensation based on VFOCV information.	
SPR_3_0	3:0	Reserved	

DevName (0x21)

Bitfield	Bits	Description
DevName	15:0	Fuel Gauge version information

LearnCfg (0x28)

The LearnCFG register controls all functions relating to adaptation during operation. The LearnCFG register default values should not be changed unless specifically required by the application.

Bitfield	Bits	Description	Decode
Reserved	15:7	Reserved	Set according to custom characterization, or leave as default.
LS	6:4	Learn Stage. The Learn Stage value controls the influence of the voltage fuel gauge on the mixing algorithm. Learn Stage defaults to 0h, making the voltage fuel gauge dominate. Learn Stage then advances to 7h over the course of two full cell cycles to make the coulomb counter dominate. The host software can write the Learn Stage value to 7h to advance to the final stage at any time. Writing any value between 1h and 6h is ignored.	
SPR_3_3	3:0	Reserved	Set according to custom characterization, or leave as default.

FilterCfg (0x29)

Bitfield	Bits	Description	Decode
SPR_15_14	15:14	Reserved	Set according to custom characterization or leave as default.
NTEMP	13:11	Sets the time constant for the AverageTemperature register. The default POR value of 1h gives a time constant of 12min.	The equation setting the period is: AvergeTemperature time constant = 175.8ms x 2(11 + TEMP)
NMIX	10:7	Sets the time constant for the mixing algorithm. The default POR value of Dh gives a time constant of 12.8 hours.	The equation setting the period is: Mixing Period = 175.8ms × 2(5 + NMIX)
NAVGCELL	6:4	Sets the time constant for the AverageVCELL register. The default POR value of 2h gives a time constant of 45s.	The equation setting the period is: AverageVCELL time constant = 175.8ms × 2(6 + NAVGVCELL)
NCURR	3:0	Sets the time constant for the AverageCurrent register. The default POR value of 4h gives a time constant of 11.25 seconds.	The equation setting the period is: AverageCurrent time constant = 175.8ms × 2(2 + NCURR)

RelaxCfg (0x2A)

The RelaxCFG register defines how the device detects if the cell is in a relaxed state. For a cell to be considered relaxed, current flow through the cell must be kept at a minimum while the change in the cell's voltage over time (dV/dt) shows little or no change. If AverageCurrent remains below the load threshold while VCELL changes less than the dV threshold over two consecutive periods of dt, the cell is considered relaxed.

Bitfield	Bits	Description	Decode
LoadThr	15:9	When current magnitude is less than LoadThr, the device is considered to be unloaded.	The LSb is 0.5mA.
dVThr	8:4	dVThr sets the relaxation criteria between VCELL and OCV. If the cell's voltage changes by less than dV over two consecutive periods set by dt, the cell is considered relaxed.	dVThr5 is 1.25mV per LSB. (1.25mV to 40mV range)
dTThr	3:0	dTThr configures the relaxation timer. Sets the time period over which change in VCELL is compared against dV. If the cell's voltage changes by less than dV over two consecutive periods set by dt, the cell is considered relaxed. The default value is 6 minutes.	The AvgVCELL is sampled at every dTThr interval (2^{dTThr} x 0.1758s), and delta-V is checked by comparing to the previous sample.

TGain (0x2C) / TOff (0x2D) / Curve (0xB9)

External NTC Thermistor generate a temperature related voltage to be measured by the THM input. The TGain, TOff, and Curve registers are used to calculate temperature from the measurement with an accuracy of ±3°C over a range of -40°C to 85°C. The table below lists the recommended TGain, TOff, and Curve register values for common NTC thermistors. Contact Maxim for other thermistor options.

TGain (0x2C)

Bitfield	Bits	Description
TGAIN	15:0	TGAIN is a signed value with units of ºC/64.

TOff (0x2D)

Bitfield	Bits	Description
TOFF	15:0	TOFF is a signed value with units of 2^{-7} in the LSb. Note that these units are 2x the TEMP register.

Curve (0xB9)

Bitfield	Bits	Description	Decode
Reserved	15:8	Reserved	Set to 0, or leave at default.
TCURVE	7:0	TCURVE applies the thermistor measurement curvature correction to allow thermistor measurements to be accurate over a wider temperature range. ±3°C accuracy can be achieved over a -40°C to +85°C operating range.	

Register Settings for Common Thermistor Types

THERMISTOR	R_{25C} (kΩ)	BETA	RECOMMENDED TGain	RECOMMENDED TOff	RECOMMENDED Curve
Semitec 103AT-2, Murata NCP15XH103F03RC	10	3435	0xEE56	0x1DA4	0x0025
Fenwal 197-103LAG-A01	10	3974	0xF49A	0x16A1	0x0064
TDK Type F	10	4550	0xF284	0x18E8	0x0035

COff (0x2F)

Bitfield	Bits	Description	Decode
COFF	15:0	Current Offset	LSB is 3.15µA

RippleCfg (0xBD)

Bitfield	Bits	Description	Decode
kDV	15:3	Sets the corresponding amount of capacity to compensate proportional to the ripple. kDV contributes empty compensation as a function of ripple voltage.	The LSB units for kDV are 0.05/256 %/mV.

Bitfield	Bits	Description	Decode
NR	2:0	Sets the filter magnitude for ripple observation.	Set NR[2:0] for the below filter timing (i.e., Ripple Time Range): 0x0 = 1.4s 0x1 = 2.8s 0x2 = 5.6s 0x3 = 11.2s 0x4 = 22.4s 0x5 = 45s 0x6 = 90s 0x7 = 3min

Measurement Registers

Vcell (0x09)

Bitfield	Bits	Description	Decode
VCELL	15:0	This is the most recent trimmed cell voltage result. It represents a FIR average of raw results. The VOLT_Raw is sampled every 175.8ms and gain and offset trim are applied to calculate VCELL.	Bits D15 to D0 represent that 15-bit conversion result. VCELL has 78.125µV per LSB.

AvgVCell (0x19)

Bitfield	Bits	Description	Decode
AvgVCELL	15:0	This reports the 12s to 24min (configurable) IIR average of VCELL. The average is set equal to VCELL at startup.	AvgVCELL has 78.125µV per LSB

MaxMinVolt (0x1B)

Bitfield	Bits	Description	Decode
MaxVoltage	15:8	Records the VCELL maximum voltage.	Units of LSB are 20mV.
MinVoltage	7:0	Records the VCELL minimum voltage.	Units of LSB are 20mV.

Current (0x0A)

Bitfield	Bits	Description
Current	15:0	The IC measures the current between BATT and SYS and the result is stored as a two’s complement value in the Current register. Current outside the minimum and maximum register values are reported as the minimum or maximum value.

AvgCurrent (0x0B)

Bitfield	Bits	Description	Decode
AvgCurrent	15:0	This is the 0.7s to 6.4hr (configurable) IIR average of the current. This register represents the upper 16 bits of the 32-bit shift register that filters current. The average should be set equal to Current upon startup.	Units of LSbit are 156.25µA.

MaxMinCurr (0x1C)

Bitfield	Bits	Description	Decode
MaxChargeCurrent	15:8	Records the maximum charge current.	8-bit values with 40mA resolution.
MaxDisCurrent	7:0	Records the maximum discharge current.	8-bit values with 40mA resolution.

Temp (0x08)

Bitfield	Bits	Description	Decode
TEMP	15:0	This is the most recent trimmed temperature measurement. Temperature is measured every 1.4 seconds.	When using THM for temperature, configure TGAIN, TOFF, and CURVE to adjust the THM measurement to provide values in ºC in the high-byte of Temp. When TGAIN, TOFF, and CURVE are configured properly for the selected thermistor, the TEMP register value is a signed 2's complement number, with 0.0039˚C LSB. The TEMP register is the input to the fuel gauge algorithm.

AvgTA (0x16)

Bitfield	Bits	Description	Decode
AvgTA	15:0	This is the 6min to 12hr (configurable) IIR average of the Temperature. The average is set equal to Temp upon startup.	Units of LSbit are 0.0039˚C. The upper byte has units 1°C.

MaxMinTemp (0x1A)

Bitfield	Bits	Description	Decode
MaxTemperature	15:8	Records the maximum Temperature.	Units of LSB are 1˚C.
MinTemperature	7:0	Records the minimum Temperature.	Units of LSB are 1˚C.

AIN0 (0x27)

Bitfield	Bits	Description	Decode
AIN0	15:0	This is the most recent trimmed ratiometric measurement on THM pin, which is generally used for measuring temperature. THM is measured every 1.4 seconds (if Ten = 1).	AIN0 is an unsigned register where 0xFFFF indicates a 100% ratio between THM/THMB. LSb is 2^{-16}.

Timer (0x3E)

Bitfield	Bits	Description
TIMER	15:0	Timer increments once every task period. With default TaskPeriod, timer has units of 0.1758 seconds per LSbit.

ShdnTimer (0x3F)

The SHDNTIMER register sets the timeout period from when a shutdown event is detected until the device disables the LDO and enters low-power mode.

Bitfield	Bits	Description
SHDN_THR	15:13	Sets the shutdown timeout period from a minimum of 45s to a maximum of 1.6h. The default POR value of 7h gives a shutdown delay of 1.6h. The equation setting the period is: Shutdown Timeout Period = 175.8ms × $2^{(8+THR)}$
SHDNCTR	12:0	Shutdown Counter. This register counts the total amount of elapsed time since the shutdown trigger event. This counter value stops and resets to 0 when the shutdown timeout completes. The counter LSb is 1.4s.

QH0 (0x4C)

Bitfield	Bits	Description
QH0	15:0	Last sampled QH for dQ accumulation.

VRipple (0xBC)

Bitfield	Bits	Description	Decode
Vripple	15:0	It is for the voltage compensation on battery capacity report.	LSB unit = 1.25/16mV.

TimerH (0xBE)

Bitfield	Bits	Description
TIMERH	15:0	TIMERH is a 16-bit high-word extension to the TIMER register. This extension allows time counting up to 24 years. This register can be enabled in the save and restore registers.

ModelGauge m5 Configuration Registers

QRTable00 (0x12)

Bitfield	Bits	Description
QRTable00	15:0	QRTable__ contains characterization information about cell capacity that is not available under certain application conditions.

QRTable10 (0x22)

Bitfield	Bits	Description
QRTable10	15:0	QRTable__ contains characterization information about cell capacity that is not available under certain application conditions.

QRTable20 (0x32)

Bitfield	Bits	Description
QRTable20	15:0	QRTable__ contains characterization information about cell capacity that is not available under certain application conditions.

QRTable30 (0x42)

Bitfield	Bits	Description
QRTable30	15:0	QRTable__ contains characterization information about cell capacity that is not available under certain application conditions.

FullSocThr (0x13)

Bitfield	Bits	Description	Decode
FullSOCThr	15:0	The FullSOCThr register gates detection of end-of-charge. VFSOC must be larger than the FullSOCThr value before nIChgTerm is compared to the AvgCurrent register value. The recommended FullSOCThr register setting for most custom characterized applications is 95%.	LSB unit is 1/ 256%.

IChgTerm (0x1E)

Bitfield	Bits	Description	Decode
ICHGTerm	15:0	The IChgTerm register allows the device to detect when a charge cycle of the cell has completed. nIChgTerm should be programmed to the exact charge termination current used in the application. The device detects end of charge if all the following conditions are met: VFSOC Register > FullSOCThr Register AND IChgTerm x 0.125 < Current Register < IChgTerm x 1.25 AND IChgTerm x 0.125 < AvgCurrent Register < IChgTerm x 1.25.	LSB unit is the same as the register current's LSB unit.

FullCapNom (0x23)

Bitfield	Bits	Description	Decode
FullCapNom	15:0	FullCapNom is the internally measured value of the nominal full capacity estimated for room temperature. It is measured by one of the three defined full capacity learning methods (relax-to-relax, relax-to-relax zigzag, or continual).	0.5mAh per LSB.

DesignCap (0x18)

Bitfield	Bits	Description	Decode
DesignCap	15:0	DesignCap register holds the expected capacity of the cell.	Units are 0.5mAh.

IAvgEmpty (0x36)

Bitfield	Bits	Description	Decode
Iavg_empty	15:0	This register stores the typical current experienced by the Fuel Gauge when Empty has occurred.	Iavg_empty is a signed register with a 156.25µA LSbit.

RComp0 (0x38)

Bitfield	Bits	Description
SPR	15:8	Reserved
RCOMP0	7:0	This holds characterization information critical to computing the open circuit voltage of a cell under loaded conditions.

TempCo (0x39)

Bitfield	Bits	Description
TempCoHot	15:8	Upper byte holds TempCoHot with units of 0.03125 counts/°C.
TempCoCold	7:0	Lower byte holds TempCoCold with units of 0.125 counts/°C

VEmpty (0x3A)

Bitfield	Bits	Description	Decode
V_Empty	15:7	Empty Voltage. Sets the voltage level for detecting empty.	A 10mV resolution gives a 0V to 5.11V range. This value is written to 3.12V at power-up.
V_Recover	6:0	Recovery Voltage. Sets the voltage level for clearing empty detection. Once the cell voltage rises above this point, empty voltage detection is reenabled.	A 40mV resolution gives a 0V to 5.08V range. This value is written to 3.68V at power-up.

ConvgCfg (0x49)

The ConvgCFG register controls the converge to empty function of ModelGauge m5. This feature bends the RepSOC curve to closely match the voltage waveform as the SOC approaches empty, ensuring 0% is reported when V_Empty is reached.

Bitfield	Bits	Description	Decode
RepLow	15:12	Sets the threshold below which RepCap begins to bend upwards.	The LSB for RepLow is 2% and the range is 0% to 30%.
VoltLowOff	11:7	When the AvgVCELL drops below VoltLow, RepCap is bent downwards according to the ratio ((VCELL - Vempty)/VoltLowOff).	The LSB for VoltLowOff is 20mV as the value here is a positive differential value to V_empty.
MinSlopeX	6:3	Sets the amount of slope-shallowing which occurs when RepSOC falls below RepLow.	MinSlopeX = 1 corresponds to a 1/16 ratio, and MinSlopeX = 15 corresponds to 15/16 ratio.
RepL_per_stage	2:0	Adjusts the RepLow threshold by: RepL_per_stage × 1% × (7 - LearnStage). This allows the earlier learn-stages to effectively use a higher RepLow setting, while the final learn-stages are just set to RepLow.	The LSB for Rep_per_stage is 1% and the range is 0% to 7%.

TTF_CFG (0xB5)

Bitfield	Bits	Description
SPR	15:3	Reserved
TTF_CFG	2:0	Configures the filtering rate for learning CV halftime for TTF calculation.

CV_MixCap (0xB6)

Bitfield	Bits	Description
CV_MixCap	15:0	The MixCapacity when CV mode has been observed to begin.

CV_HalfTime (0xB7)

Bitfield	Bits	Description
CV_Halftime	15:0	CV_HalfTime is the observed half-time from CV_Start until AvgCurrent < CC_Current/2. It is the exponential decay half-life of the current curing CV mode charging.

ModelGauge m5 Output Registers

RepCap (0x05)

Bitfield	Bits	Description	Decode
RepCap	15:0	RepCap or reported capacity is a filtered version of the AvCap register that prevents large jumps in the reported value caused by changes in the application such as abrupt changes in temperature or load current.	0.5mAh per LSB.

RepSOC (0x06)

Bitfield	Bits	Description	Decode
RepSOC	15:0	RepSOC is the complete calculation for state-of-charge. This includes all processing, including ModelGauge mixing and empty compensation.	16 bit result. The high byte indicates 1% per LSB. The low byte reports fractional percent.

Age (0x07)

Bitfield	Bits	Description	Decode
Age	15:0	Age represents the percentage of full capacity relative to the design capacity.	The high byte is 1%/LSB, and the low byte is 1/256 %.

QResidual (0x0C)

Bitfield	Bits	Description	Decode
Qresidual	15:0	This is the capacity which is not available because of the battery impedance and load current. This value changes when the load current or temperature changes.	0.5mAh per LSB.

MixCap (0x0F)

Bitfield	Bits	Description	Decode
MixCapH	15:0	The MixCap register holds the calculated remaining capacity of the cell before any empty compensation adjustments are performed.	0.5mAh per LSB.

MixSOC (0x0D)

Bitfield	Bits	Description	Decode
MixSOC	15:0	SOC is the remaining state-of-charge in the battery, including capacity that might be unavailable because of the discharge rate.	16 bit result. The high byte indicates 1% per LSB. The low byte reports fractional percent.

AvCap (0x1F)

Bitfield	Bits	Description	Decode
AvCap	15:0	This is the remaining capacity with coulomb-counter plus voltage-fuel-gauge mixing, after accounting for capacity that is unavailable due to the discharge rate.	16-bit value. 0.5mAh per LSB.

AvSOC (0x0E)

Bitfield	Bits	Description	Decode
AvSOC	15:0	AvSOC is the available state-of-charge. This includes all processing, including: ModelGauge mixing, and empty compensation.	16 bit result. The high byte indicates 1% per LSB. The low byte reports fractional percent.

FullCap (0x10)

Bitfield	Bits	Description	Decode
FullCAP	15:0	This register holds the temperature compensated full capacity value. This also compensates for the temperature dependence of charge termination. The FullCapNom value is multiplied by a temperature correction factor (FCTC) and the result is stored in this register.	0.5mAh per LSB.

TTE (0x11)

Bitfield	Bits	Description	Decode
hr	15:10	Remaining time-to-empty is calculated as (AvCap) / AvgCurrent. When enabled, the AtRate value is substituted for AvgCurrent in this calculation.	LSB unit = 1.6hr
mn	9:4	Remaining time-to-empty is calculated as (AvCap) / AvgCurrent. When enabled, the AtRate value is substituted for AvgCurrent in this calculation.	LSB unit = 1.5min
sec	3:0	Remaining time-to-empty is calculated as (AvCap) / AvgCurrent. When enabled, the AtRate value is substituted for AvgCurrent in this calculation.	LSB unit = 5.625s

Rslow (0x14)

Bitfield	Bits	Description	Decode
RSLOW	15:0	This reports the battery's slow internal resistance.	16-bit value. Units of LSbit are 2Ω to 12Ω.

Cycles (0x17)

Bitfield	Bits	Description	Decode
Cycles	15:0	Odometer style accumulation of battery cycles.	The LSB indicates 1% of a battery cycle (1% charge + 1% discharge). One cycle (Cycles = 100%) indicates 100% charge and discharge.

TTF (0x20)

Bitfield	Bits	Description	Decode
hr	15:10	Remaining time-to-full as calculated by firmware.	LSB unit = 1.6hr
mn	9:4	Remaining time-to-full as calculated by firmware.	LSB unit = 1.5min
sec	3:0	Remaining time-to-full as calculated by firmware.	LSB unit = 5.625s

FullCapRep (0x35)

Bitfield	Bits	Description	Decode
FullCapRep	15:0	This register reports the full capacity that goes with RepCap, generally used for reporting to the user. A new full-capacity value is calculated at the end of every charge cycle in the application.	0.5mAh per LSB.

dQAcc (0x45)

Bitfield	Bits	Description	Decode
dQacc	15:0	This register tracks change in battery charge between relaxation points.	Units of LSb are 16mAh. Maximum range is 8X RemCap register.

dPAcc (0x46)

Bitfield	Bits	Description	Decode
dPacc	15:0	Similar behavior as dQacc, except this is derived from the VF_SOC.	16 bit value. Units of LSb are 0.015625% (1/64%).

VFRemCap (0x4A)

Bitfield	Bits	Description
VFRemCap	15:0	Remaining capacity according to the voltage fuel gauge.

AtQresidual (0xDC)

Bitfield	Bits	Description
AtQresidual	15:0	AtQresidual is calculated as normal Qresidual, except using AtRate instead of current.

AtAvSOC (0xDE)

Bitfield	Bits	Description
AtAvSOC	15:0	AtAvSOC is calculated as normal AvSOC, except using AtRate instead of current.

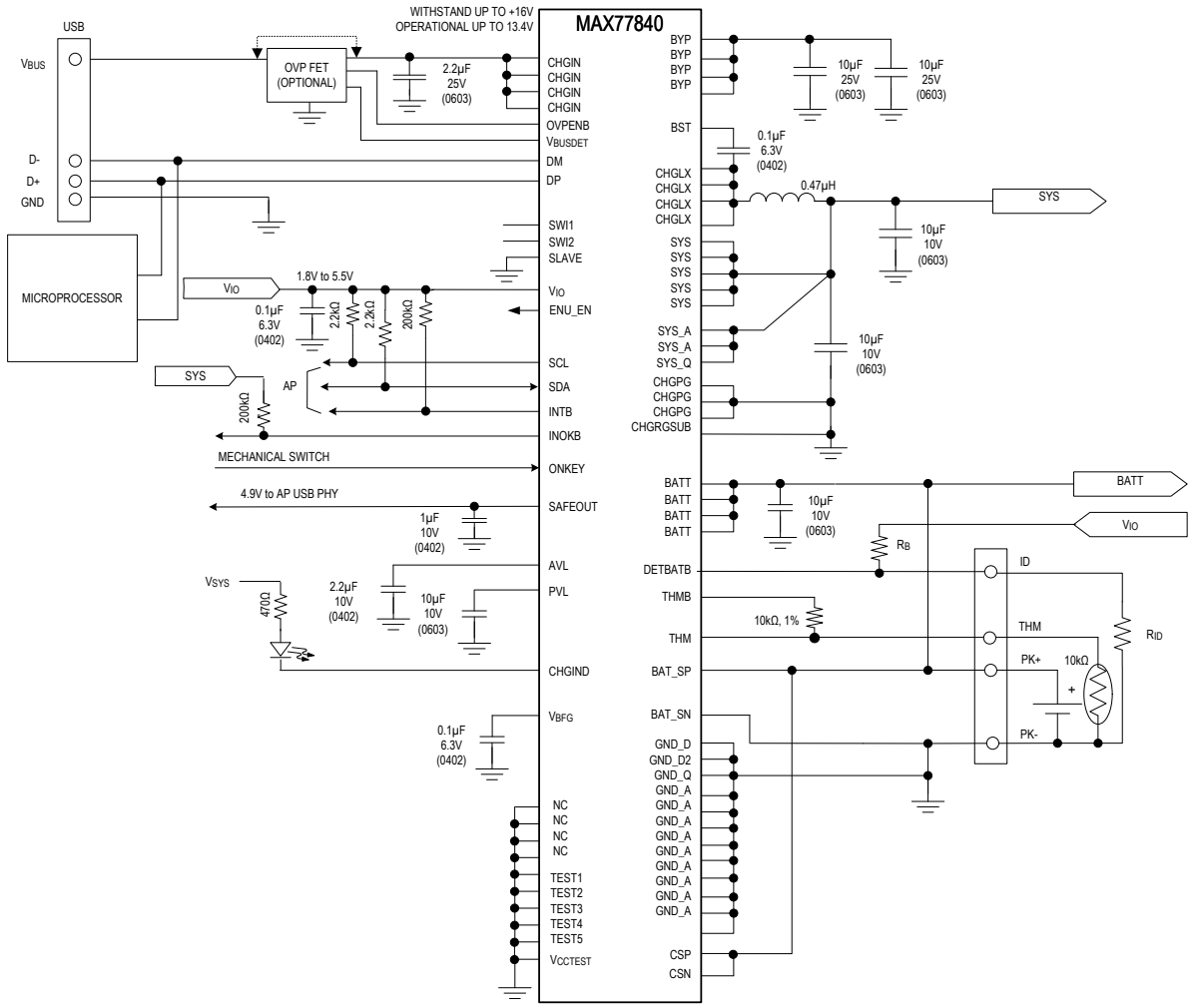
AtAvCap (0xDF)

Bitfield	Bits	Description
AtAvCap	15:0	AtAvCap is calculated as normal AvCap, except using AtQresidual instead of Qresidual.

VFOCV (0xFB)

Bitfield	Bits	Description
VFOCV	15:0	Open-circuit voltage output of the voltage fuel gauge.

Typical Application Circuits



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX77840EWG+	-40°C to 85°C	9x9 Bump Array WLP, 0.4mm pitch, 3.96mm x 3.87mm
MAX77840EWG+T	-40°C to 85°C	9x9 Bump Array WLP, 0.4mm pitch, 3.96mm x 3.87mm

+Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/21	Initial release	—