CP2114

SINGLE-CHIP USB AUDIO TO I2S DIGITAL AUDIO BRIDGE

Single-Chip USB Audio to I2S Digital Audio Bridge
- USB HID to I2C to communicate with DAC/codec
- Supports USB HID Consumer Controls for Volume and Mute Synchronization
- Integrated USB transceiver; no external resistors required
- Integrated clock; no external crystal required
- Integrated One-Time Programmable ROM for product customization
- On-chip voltage regulator: 3.45 V output

Supports a Wide Range of codecs/DACs
- Out-of-box support for three major codecs/DACs
- Internal programmable memory supports additional codec/DAC configurations

USB Audio Class v1.0 support
- I2S Master mode, I2S and left justified PCM outputs
- Supports 48 kHz,16-bit stereo digital audio
- No custom driver required
- Supports Windows 7, Vista, XP, Mac OS-X, Linux
- Supports iPad/iOS (with USB camera kit connector)
- Open access to interface specification

USB Peripheral Function Controller
- USB Specification 2.0 compliant; full-speed (12 Mbps)
- USB Suspend states supported via SUSPEND pins

USB HID to UART Auxiliary Communication Interface
- APIs for quick application development
- Supports Windows 7, Vista, XP, Server 2003, 2000
- Supports Mac OS-X

12 Configurable GPIO Pins with Alternate Functions
- Usable as inputs, open-drain or push-pull outputs
- UART signals, audio playback controls, DAC select pins
- Configurable clock output
- Toggle LEDs upon UART transmission or reception

Supply Voltage
- Self-powered: 3.0 to 3.6 V
- USB bus powered: 4.0 to 5.25 V
- I/O voltage: 1.8 V to V_{DD}

Package
- RoHS-compliant 32-pin QFN (5 x 5 mm)

Ordering Part Number
- CP2114-B01-GM

Temperature Range: –40 to +85 °C

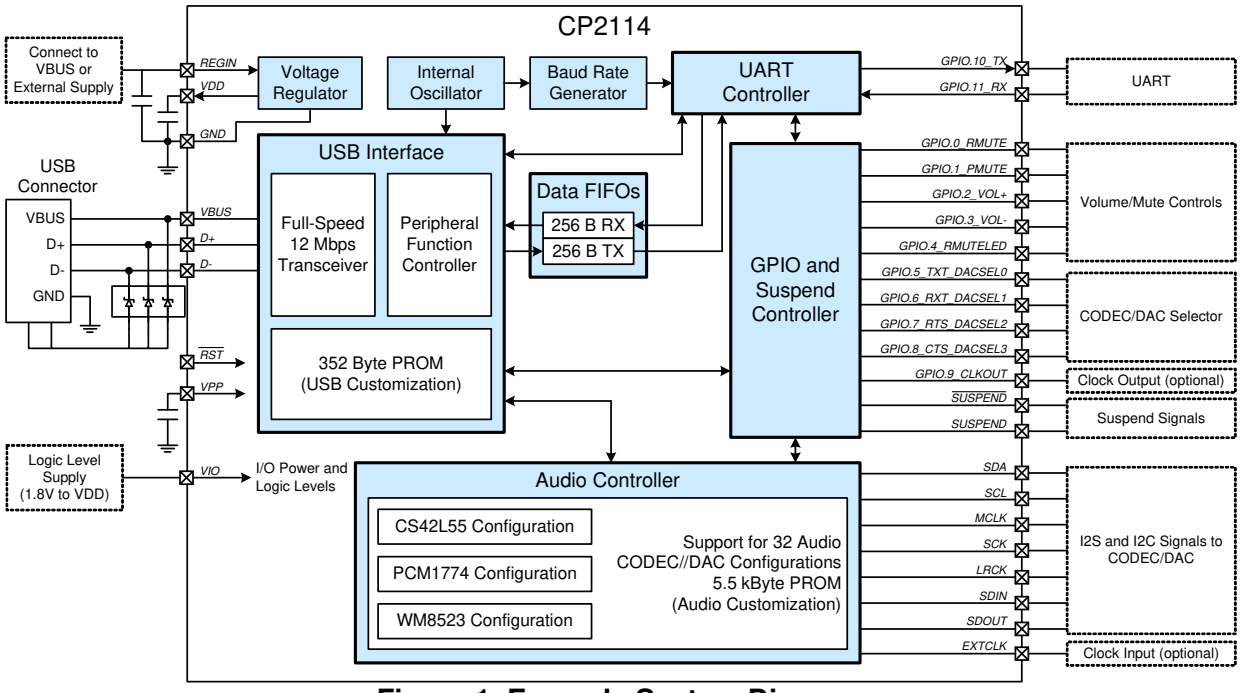

Figure 1. Example System Diagram

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1. System Overview

All major commercial operating systems (Windows, Linux, Mac, iOS) support the standard USB Audio Device class. Codecs and DACs typically have only an I2S (Inter-IC Sound) digital interface, and thus cannot connect directly to a host system. In addition, when a DAC is powered on, it typically needs to be configured by the host via an I2C (inter-integrated-circuit) digital interface, with a non-standard protocol. Finally, in order to support push button volume and mute synchronization with the host system, the target USB device must support the standard USB-HID Consumer Control interface. Thus, adding USB digital audio to an embedded system or as dongle or appliance typically involves complex USB protocol programming as well as I2S and I2C programming capability, prototyping, integration and testing. The CP2114 USB Audio Bridge is specifically designed to overcome all these issues and commoditize USB Audio and DAC configuration for turn-key product development.

Note: Use with an iPad requires a camera kit connector to get USB from the Apple 30-pin connector. USB Audio is not supported on the iPhone.

The CP2114 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, one-time programmable read-only memory (ROM), I2S (audio) interface, I2C (control) interface, and UART interface in a compact 5 x 5 mm QFN-32 package (sometimes called “MLF” or “MLP”). The one-time programmable ROM on the device may be used to customize both product information (including USB fields such as Vendor ID, Product ID, Strings, etc...) and external DAC configuration strings. By default, the CP2114 provides the following features

- Enumerates to the host as a Standard USB Audio Device and HID Consumer Control supporting:
  - USB Digital Audio Out (Audio Playback Device)
  - USB Digital Audio In (Microphone/Recording Device)
  - HID Consumer Control handling standard volume and mute functionality
- Pre-configured support for 3 commercial DACs
  - Handles all I2C configuration of the DAC automatically at boot
  - Handles all volume and mute traffic converting from USB to I2C messages to the DAC
- Tested for USB plug & play and audio quality on all major operating systems
- UART interface using standard USB HID device class which is natively supported by most operating systems
  - No custom driver installation needed
  - Windows and MAC DLLs provided and interface specification is available for development on any operating system
  - Implements transmit (TX), receive (RX), hardware flow control (CTS, RTS)
  - Baud rate support from 300 to 1 Mbps, support for 5-8 data bits, 5 parity options, 3 types of stop bits
  - Note: The CP2114 devices will not enumerate as a standard HID mouse or keyboard.
- 12 GPIO signals which support alternate functions
  - Volume control, UART transmit and receive, UART hardware flow control, UART transmit/receive toggle, configurable clock output, and DAC selection
  - Support for I/O interface voltages down to 1.8 V is provided via a V_{IO} pin.

An evaluation kit for the CP2114 (Part Number: CP2114EK) is available. It includes a CP2114-based USB-to-Audio motherboard, a USB cable, and full documentation. Additional kits with daughter cards are available as well:

- CP2114-CS42L55 evaluation kit (Part Number: CP2114-CS42L55EK) includes:
  - CP2114 USB-to-I2S Digital Audio motherboard
  - Cirrus Logic CS42L55 Codec daughter card (includes a 3.5mm male-to-male audio cable)
- CP2114-WM8523 evaluation kit (Part Number: CP2114-WM8523EK)
  - CP2114 USB-to-I2S Digital Audio motherboard
  - Wolfson Microelectronics WM8523 DAC daughter card
- CP2114-PCM1774 evaluation kit (Part Number: CP2114-PCM1774EK)
  - CP2114 USB-to-I2S Digital Audio motherboard
  - Texas Instruments PCM1774 DAC daughter card

All kits with daughter cards include a USB cable, ear bud headphones, and full documentation.

Contact a Silicon Labs sales representatives or go to www.silabs.com to order a CP2114 Evaluation Kit.

2. Electrical Characteristics

Table 1. Global DC Electrical Characteristics

V_{DD} = 3.0 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Digital Supply Voltage (V_{DD})		3.0	—	3.6	V
Digital Port I/O Supply Voltage (V_{IO})		1.8	—	V_{DD}	V
Digital Supply Current (USB Active Mode)[1]	Bus Powered Mode Self Powered Mode with Regulator enabled Self Powered Mode with Regulator disabled	—	18	28	mA
Digital Supply Current (USB Suspend Mode)[1]	Bus Powered Mode Self Powered Mode with Regulator enabled	—	750	940	µA
	Self Powered Mode with Regulator disabled	—	0.99	1.2	mA
Supply Current - USB Pull-up[2]		—	200	228	µA
Specified Operating Temperature Range		–40	—	+85	°C

Notes:

1. If the device is connected to the USB bus, the USB Pull-up Current should be added to the supply current for total supply current.
2. The USB Pull-up supply current values are calculated values based on USB specifications.

Table 2. I2S, I2C, UART and Suspend I/O DC Electrical Characteristics

V_{DD} = 3.0 to 3.6 V, V_{IO} = 1.8 V to V_{DD}, –40 to +85 °C unless otherwise specified.

Parameters	Condition	Min	Typ	Max	Unit
Output High Voltage (V_{OH})	I_{OH} = –10 µA I_{OH} = –3 mA I_{OH} = –10 mA	V_{IO} – 0.1 V_{IO} – 0.2 —	— — V_{IO} – 0.4	— — —	V
Output Low Voltage (V_{OL})	I_{OL} = 10 µA I_{OL} = 8.5 mA I_{OL} = 25 mA	— — —	— — 0.6	0.1 0.4 —	V
Input High Voltage (V_{IH})		0.7 x V_{IO}	—	—	V
Input Low Voltage (V_{IL})		—	—	0.6	V
Input Leakage Current	Weak Pull-Up Off Weak Pull-Up On, V_{IO} = 0 V	— —	— 25	1 50	µA
Maximum Input Voltage	Open drain, logic high (1)	—	—	5.8	V

Table 3. Reset Electrical Characteristics

–40 to +85 °C unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Units
$\overline{RST}$ Input High Voltage		0.75 x V_{IO}	—	—	V
$\overline{RST}$ Input Low Voltage		—	—	0.6	V
Minimum $\overline{RST}$ Low Time to Generate a System Reset		15	—	—	µs

Table 4. Voltage Regulator Electrical Specifications

–40 to +85 °C unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Input Voltage Range		3.0	—	5.25	V
Output Voltage	Output Current = 1 to 100 mA*	3.3	3.45	3.6	V
VBUS Detection Input Threshold		2.5	—	—	V
Bias Current		—	—	120	µA
***Note:** The maximum regulator supply current is 100 mA. This includes the supply current of the CP2114.					

Table 5. GPIO Output Specifications

–40 to +85 °C unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
GPIO.9 Clock Output		f_{OUT} x 0.985	f_{OUT}	f_{OUT} x 1.015	Hz
TX Toggle Rate		—	20	—	Hz
RX Toggle Rate		—	20	—	Hz

Table 6. One Time Programming Specifications

V_{DD} = 3.3 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Digital Port I/O Supply Voltage (V_{IO}) during programming		3.3		V_{DD}	V
Capacitor on V_{PP} for programming		—	4.7	—	µF

Table 7. System Clock Specifications

V_{DD} = 3.3 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Internal Oscillator	SF = 0 (Register: System_Props, bit: 1) SF = 1 (Register: System_Props, bit: 1)	— —	48 49.152	— —	MHz MHz
External CMOS clock input frequency	SF = 0 (Register: System_Props, bit: 1) SF = 1 (Register: System_Props, bit: 1)	47.880 —	48 49.152	48.120 —	MHz MHz

1. Depending on the requirements of the external DAC, the system clock frequency will be either 48.0 or 49.152 MHz. See Section 5.6 for more information.
2. The USB specification requires a clock accuracy of ±0.25%.

Table 8. I2S Digital Audio Interface Specifications

V_{DD} = 3.3 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Resolution (analog output)		—	16	—	bits
Resolution (analog input)		—	15	—	bits
MCLK frequency	(SYSCLK = 48 MHz)	—	12	—	MHz
	(SYSCLK = 49.152 MHz)	—	12.288	—	MHz
LRCK frequency		—	48	—	kHz
SCK frequency	(SYSCLK = 48 MHz)	—	3.429	—	MHz
	(SYSCLK = 49.152 MHz)	—	3.511	—	MHz
MCLK/LRCK jitter	SCS = 0 (external Si500S clock) (Register: System_Props, bit: 2)	—	20	—	ps RMS*
	SCS = 1 (internal oscillator) (Register: System_Props, bit: 2)	—	140	—	ps RMS*

***Note:** Measurement bandwidth: 100 Hz –40 kHz.

Table 9. I2C Specifications

V_{DD} = 3.3 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
SCL frequency	I2C_CK = 0 (Register: Audio_Props, bit: 5) I2C_CK = 1 (Register: Audio_Props, bit: 5)	— —	400 100	— —	kHz

Table 10. Analog Output/Input Characteristics (CS42L55 daughter card)

25 °C, bus-powered, USB synchronization mode: asynchronous, digital audio interface mode: I2S, DAC/ADC gains set to 0 dB, test signal for analog output: uncompressed WAV file, full-scale sine wave at 997 Hz, measurement bandwidth 20 Hz to 20 kHz
Additional parameters that apply to this table are as follows:

- VA = VCP = VLDO = 2.5 V
- Internal oscillator mode

Parameter	Condition	Min	Typ	Max	Unit
Analog Output (Line Output)					
THD + Noise	0 dB input -20 dB input -60 dB input	— — —	–80 –91 –91	— — —	dB dB dB
Dynamic Range	A-weighted	—	92	—	dB
Noise Level	Output muted	—	–112	—	dB
Frequency response	20 Hz - 20 kHz	—	+0.03, –0.07	—	dB
Analog Input					
THD + Noise	-1 dB input -20 dB input -60 dB input	— — —	–85 –87 –87	— — —	dB dB dB
Dynamic Range	A-weighted	—	90	—	dB
Noise Level	Analog input locally muted	—	0*	—	dB

***Note:** When analog input is locally muted, the CP2114 transmits sample values of 0 to the host.

Table 11. Analog Output Characteristics (WM8523 daughter card)

25 °C, bus-powered, USB synchronization mode: asynchronous, digital audio interface mode: I2S, DAC/ADC gains set to 0 dB, test signal for analog output: uncompressed WAV file, full-scale sine wave at 997 Hz, measurement bandwidth 20 Hz to 20 kHz
Additional parameters that apply to this table are as follows:

- LINEVDD = AVDD = 3.3V
- Internal oscillator mode
- External headphone amplifier disconnected, no lowpass filter on LINEVOUTL/LINEVOUTR

Parameter	Condition	Min	Typ	Max	Unit
THD + Noise	0 dB FS input –20 dB FS input –60 dB FS input	— — —	–83 –91 –91	— — —	dB dB dB
Dynamic Range	A-weighted	—	94	—	dB
Noise Level	Output muted	—	–99	—	dB
Frequency response	20 Hz–20 kHz	—	+0.04, –0.05	—	dB

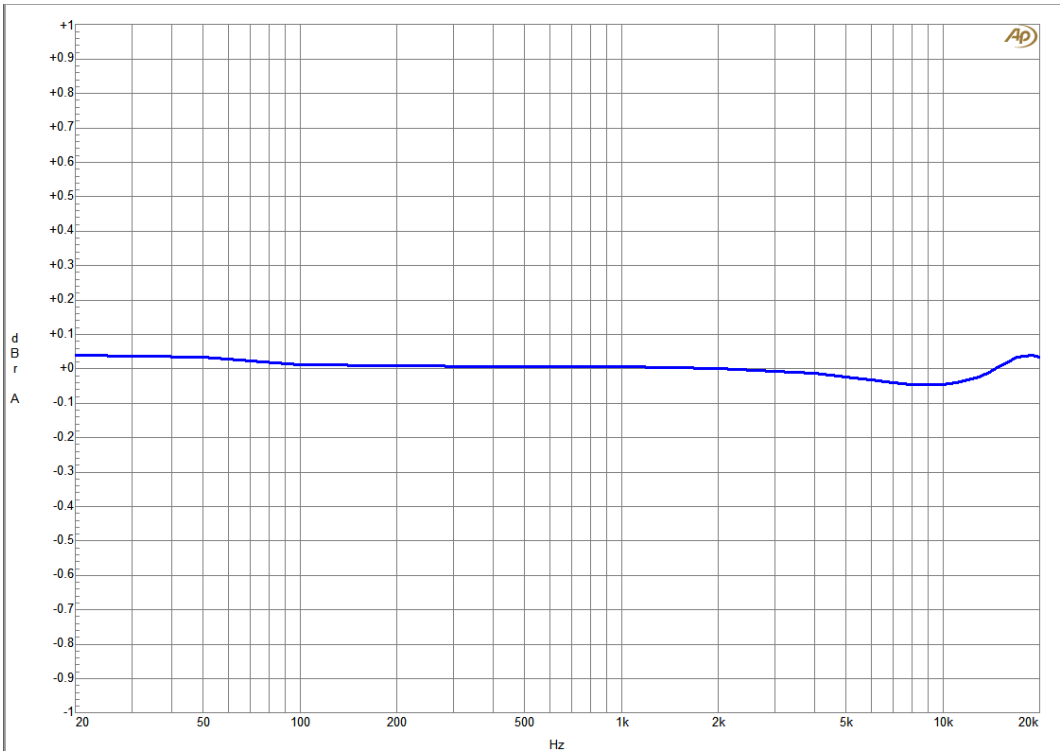


Figure 2. WM8523 Frequency Response (0 dB FS)

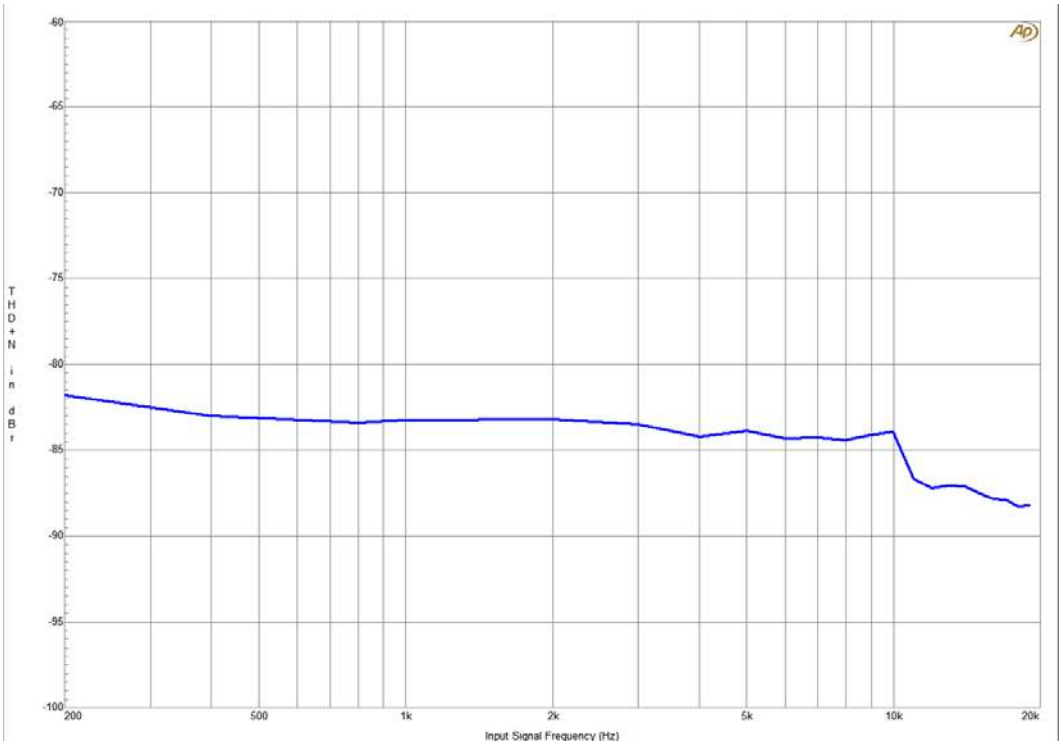


Figure 3. WM8523 THD+N vs. Frequency (0 dB FS)

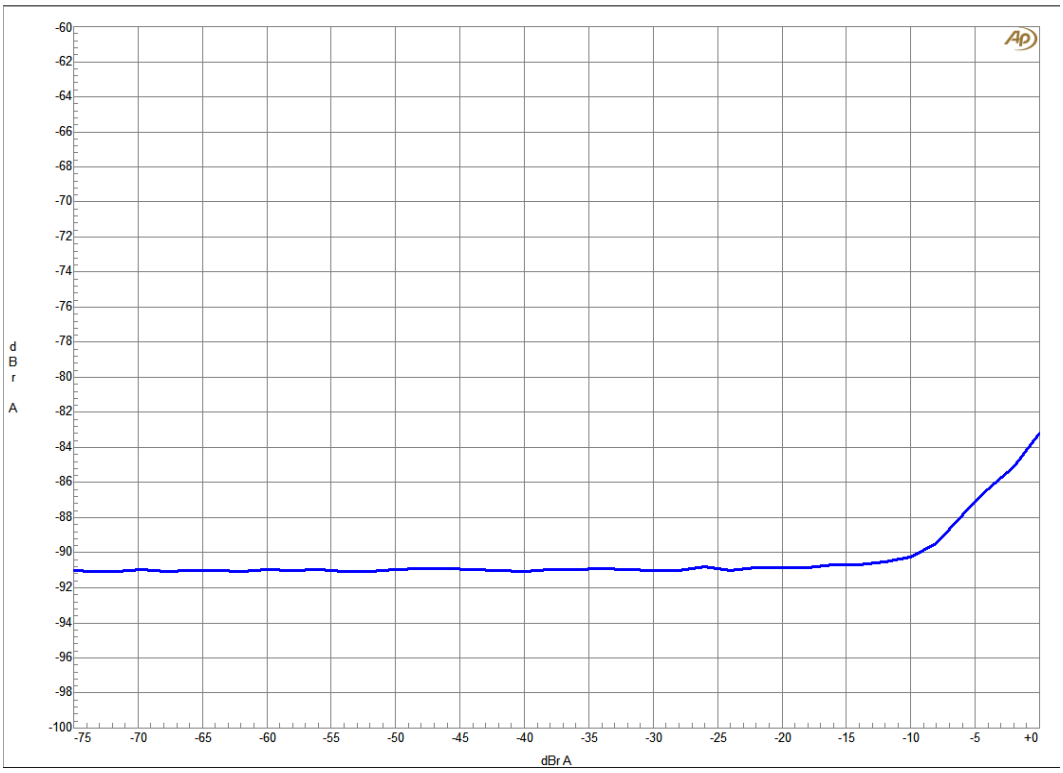


Figure 4. WM8523 THD+N vs. Amplitude (997 Hz)

Table 12. Analog Output/Input Characteristics (PCM1774 daughter card)

25 °C, bus-powered, USB synchronization mode: asynchronous, digital audio interface mode: I2S, DAC/ADC gains set to 0 dB, test signal for analog output: uncompressed WAV file, full-scale sine wave at 997 Hz, measurement bandwidth 20 Hz to 20 kHz
Additional parameters that apply to this table are as follows:

- VIO = VDD = VCC = VPA = 3.3 V.
- AOUT_L and AOUT_R outputs have 4.7 Ω series resistors.
- Internal oscillator mode.

Parameter	Condition	Min	Typ	Max	Unit
THD + Noise	0 dB FS input –20 dB FS input –60 dB FS input	— — —	–82 –89 –89	— — —	dB dB dB
Dynamic Range	A-weighted	—	89	—	dB
Noise Level	Output muted	—	–103	—	dB
Frequency response	20 Hz - 20 kHz	—	+0.04, –0.11	—	dB

Table 13. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Ambient Temperature Under Bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on $\overline{RST}$, GPIO, I2S, I2C, or UART Pins with respect to GND	$V_{IO} \geq 2.2$ V $V_{IO} < 2.2$ V	–0.3 –0.3	— —	5.8 V_{IO} + 3.6	V
Voltage on V_{DD} or V_{IO} with respect to GND		–0.3	—	4.2	V
Maximum Total Current through V_{DD}, V_{IO}, and GND		—	—	500	mA
Maximum Output Current Sunk by $\overline{RST}$ or any I/O pin		—	—	100	mA

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at or exceeding the conditions in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. Pinout and Package Definitions

Table 14. CP2114 Pin Definitions

Name	Pin #	Type	Description
VDD	7	Power In	Power Supply Voltage Input.
		Power Out	Voltage Regulator Output. See Section 10.
VIO	6	Power In	I/O Supply Voltage Input.
GND	3		Ground. Must be tied to ground.
$\overline{\text{RST}}$	10	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for the time specified in Table 3.
REGIN	8	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	9	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network.
D+	4	D I/O	USB D+
D–	5	D I/O	USB D–
VPP	21*	Special	Connect a 4.7 µF capacitor between this pin and ground to support one-time programming via the USB interface.
$\overline{\text{SUSPEND}}$	17*	D Out	This pin indicates whether the device is in the USB Suspend or not (active-low).
SUSPEND	18*	D Out	This pin indicates whether the device is in the USB Suspend or not (active-high).
SCK	2	D Out	Serial clock output signal for the I2S interface.
SDIN	1	D In	Serial data input signal for the I2S interface.
SDOUT	32	D Out	Serial data output signal for the I2S interface.
MCLK	25	D In	Master clock input for the I2S interface.
LRCK	23	D Out	Left-right clock output for the I2S interface.
EXTCLK	31*	D In	External clock input of CP2114 (optional). An external clock is needed if the codec/DAC does not support a 12.000 MHz master clock (MCLK).
SDA	27	D I/O	Serial data signal for the I2C interface.
SCL	26	D I/O	Serial clock signal for the I2C interface.
GPIO.0	30*	D I/O	User-configurable input or output.
RMUTE		D In	Record Mute: Toggles record between mute and un-mute each time this pin is driven low.
GPIO.1	29*	D I/O	User-configurable input or output.
PMUTE		D In	Playback Mute: Toggles playback between mute and un-mute each time this pin is driven low.

***Note:** Pins can be left unconnected when not used.

Table 14. CP2114 Pin Definitions (Continued)

Name	Pin #	Type	Description
GPIO.2	14*	D I/O	User-configurable input or output.
VOL-		D In	Decreases volume each time this pin is driven low.
GPIO.3	13*	D I/O	User-configurable input or output.
VOL+		D In	Increases volume each time this pin is driven low.
GPIO.4	12*	D I/O	User-configurable input or output.
RMUTELED		D Out	Record Mute LED: This pin is driven low while recording is muted.
GPIO.5	28*	D I/O	User-configurable input or output.
TXT		D Out	This pin toggles while the UART is transmitting data and is logic high when the UART is not transmitting data.
DACSEL0		D In	Selects one of the predefined DACs. See Section 8.2 for more information.
GPIO.6	11*	D I/O	User-configurable input or output.
RXT		Out	This pin toggles while the UART is receiving data and is logic high when the UART is not receiving data.
DACSEL1		D In	Selects one of the predefined DACs. See Section 8.2 for more information.
GPIO.7	19*	D I/O	User-configurable input or output.
RTS		D Out	Ready to Send control output (active low) for the UART Interface.
DACSEL2		D In	Selects one of the predefined DACs. See Section 8.2 for more information.
GPIO.8	20*	D I/O	User-configurable input or output.
CTS		D In	Clear To Send control input (active low) for the UART Interface.
DACSEL3		D In	Selects one of the predefined DACs. See Section 8.2 for more information.
GPIO.9	22*	D I/O	User-configurable input or output.
CLKOUT		D Out	Outputs a configurable frequency clock signal.
GPIO.10	16*	D I/O	User-configurable input or output.
TX		D Out	Asynchronous data output (UART Transmit) for the UART Interface.
GPIO.11	15*	D I/O	User-configurable input or output.
RX		D In	Asynchronous data input (UART Receive) for the UART Interface.
NC	24*		This pin should be left unconnected or tied to $V_{IO.}$

***Note:** Pins can be left unconnected when not used.

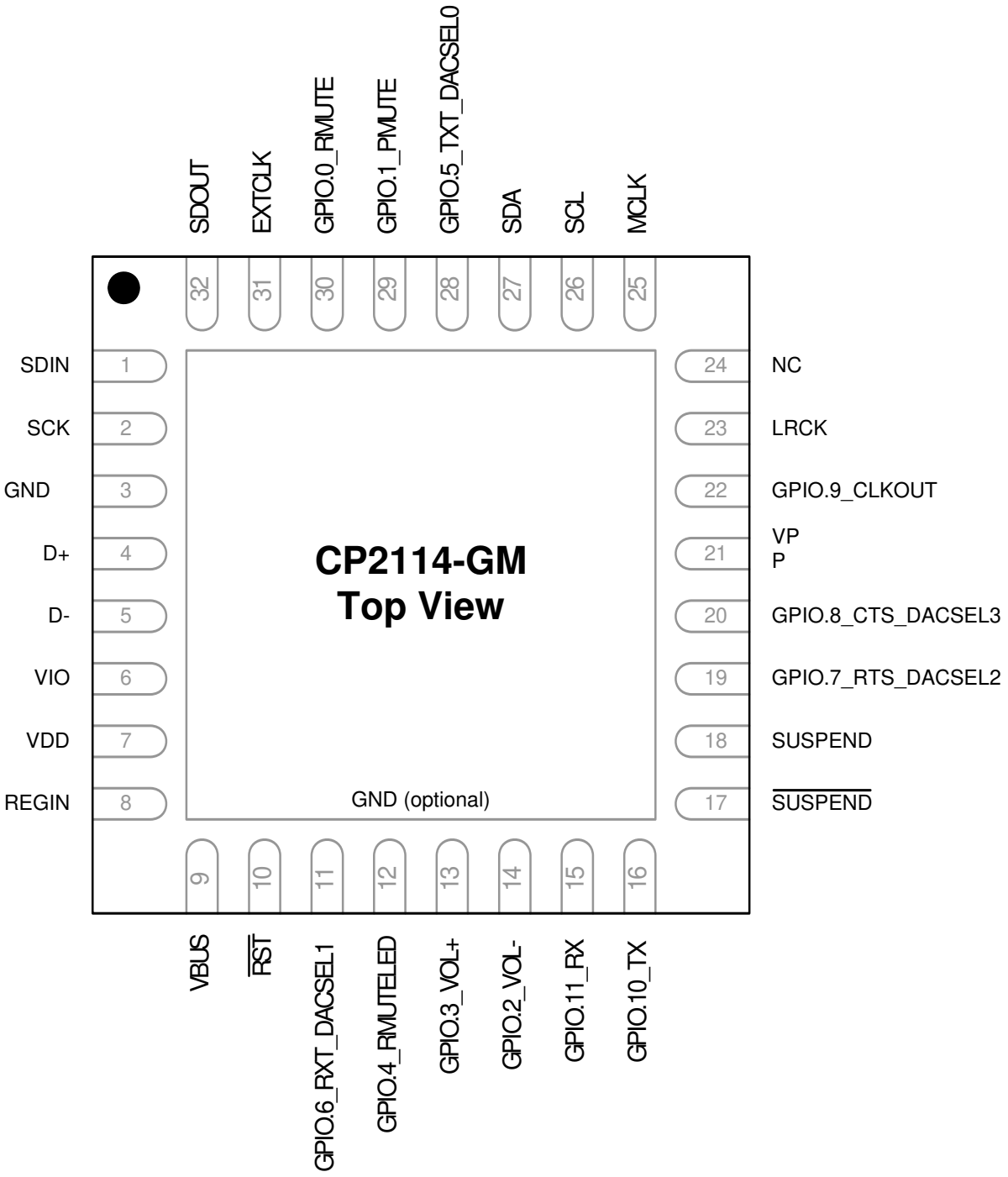


Figure 5. QFN-32 Pinout Diagram (Top View)

4. QFN-32 Package Specifications

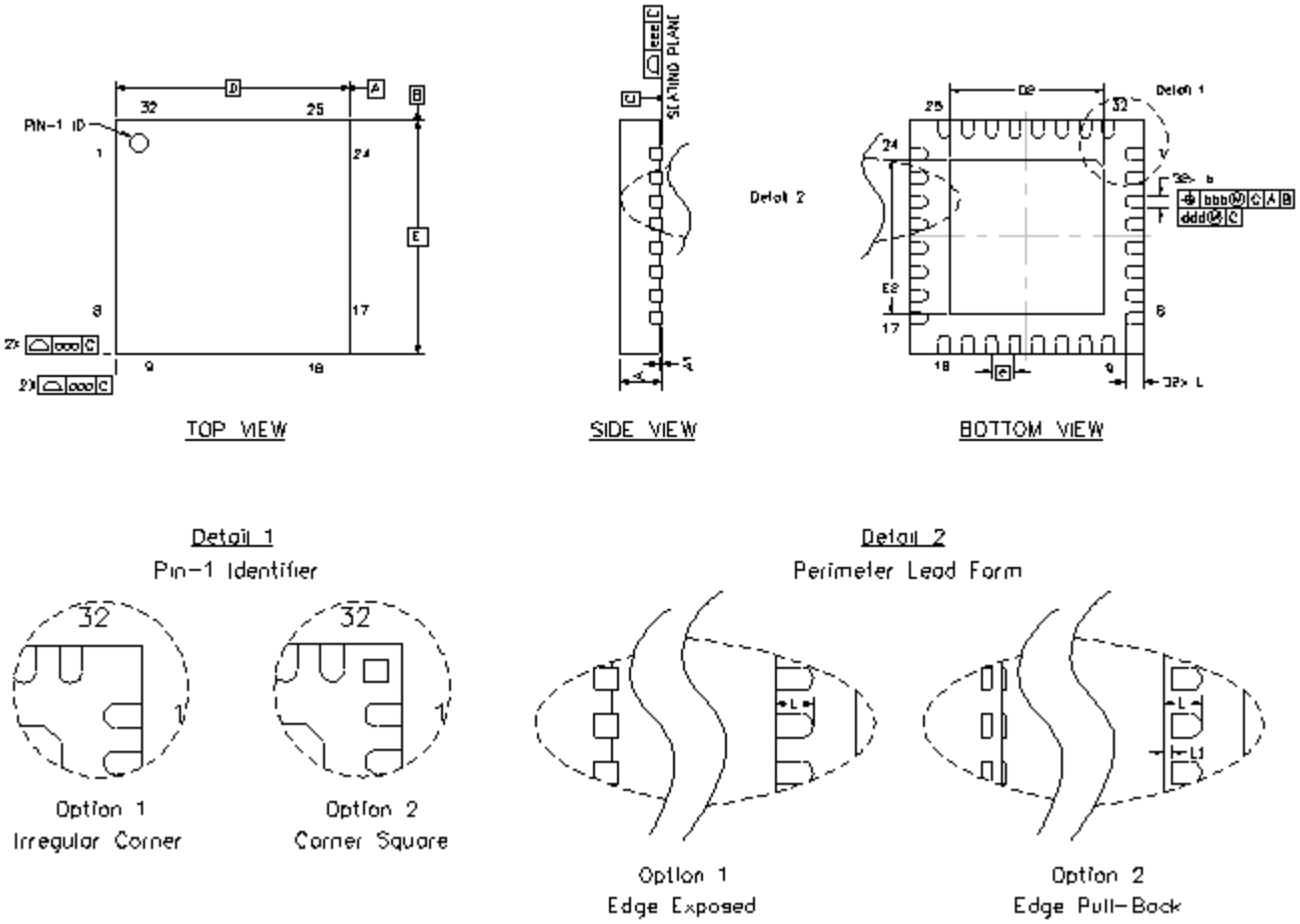


Figure 6. QFN-32 Package Drawing

Table 15. QFN-32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC.	
D2	3.20	3.30	3.40
e		0.50 BSC.	
E		5.00 BSC.	

Dimension	Min	Typ	Max
E2	3.20	3.30	3.40
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

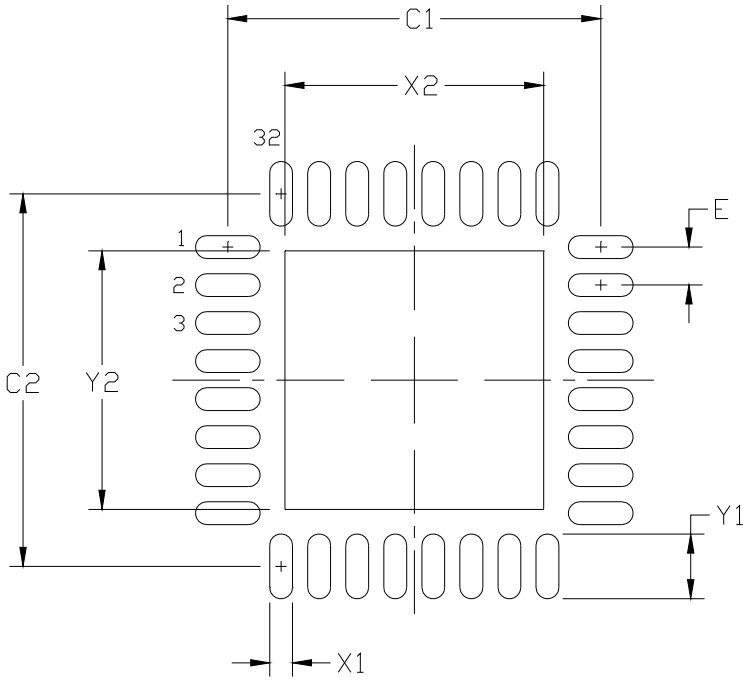


Figure 7. QFN-32 Recommended PCB Land Pattern

Table 16. QFN-32 PCB Land Pattern Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	4.80	4.90	X2	3.20	3.40
C2	4.80	4.90	Y1	0.75	0.85
E	0.50 BSC		Y2	3.20	3.40
X1	0.20	0.30			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3x3 array of 1.0 mm square openings on 1.2 mm pitch should be used for the center ground pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. Audio (I2S and I2C) Interfaces

The I2C interface configures the DAC to output sound and the I2S interface provides the digital audio stream to the DAC. In addition to full-featured off the shelf functionality, the CP2114 can be customized in two ways; via one-time programmable ROM configuration and a real-time API.

5.1. One-Time Programmable ROM Configuration Programming

The CP2114 has 5.5kB of on board one-time programmable ROM available to store up to 29 different custom configurations. Three of the 32 slots are preprogrammed configurations. The configurations can be selected as boot configurations and will automatically configure the CP2114 and the I2C connected DAC when the CP2114 is powered on. Alternatively the custom configurations can be assigned to a DAC select pin selection. The boot configuration is then selected by pin-strapping the DAC select pins. Silicon Labs provides a PC GUI application to program the configuration to the CP2114 one-time programmable ROM. The CP2114 can be programmed on a production line or a configuration file can be provided to Silicon Labs and pre-programmed parts can be supplied directly by Silicon Labs.

5.2. Real-Time Programming

The CP2114 presents the host with a USB HID interface which can be used to send messages directly to the CP2114 for internal configuration or directly to the DAC over the I2C interface. This provides real-time configuration changes to the CP2114 and DAC via host program control. In addition, the USB HID pipe can be used to write and read to the CP2114 GPIO pins as desired.

5.3. CP2114 I2S and Left-Justified Digital Audio

The CP2114 supports “I2S” and “Left Justified” digital audio formats. Note that the difference in the two modes is that for the I2S format, the MSB of the data streams (SDOUT and SDIN) are delayed by one clock (SCK) cycle after the channel clock (LRCK) transitions as compared to the Left Justified format. The digital audio format can be configured in the CP2114 one-time programmable ROM. Figure 8 shows the signals in I2S format, and Figure 9 shows the signals in Left Justified format.

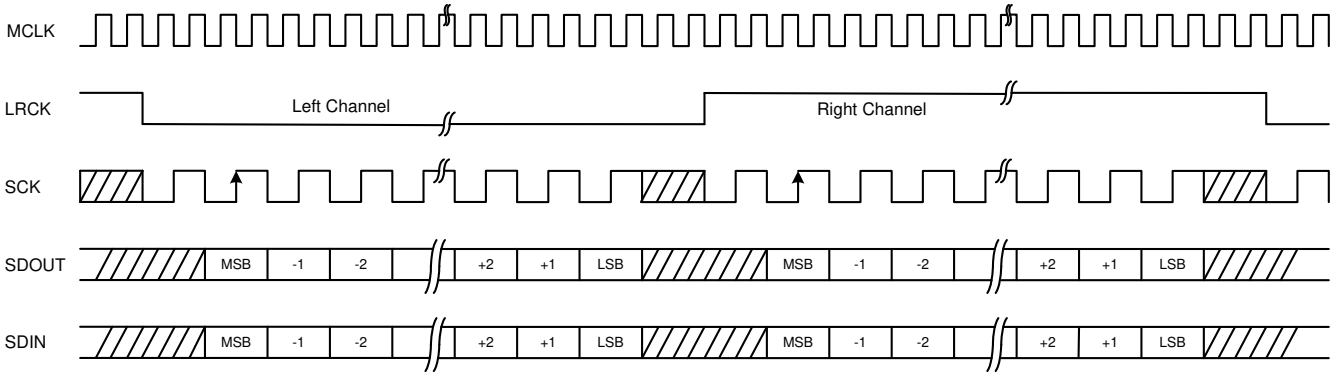


Figure 8. I2S Format

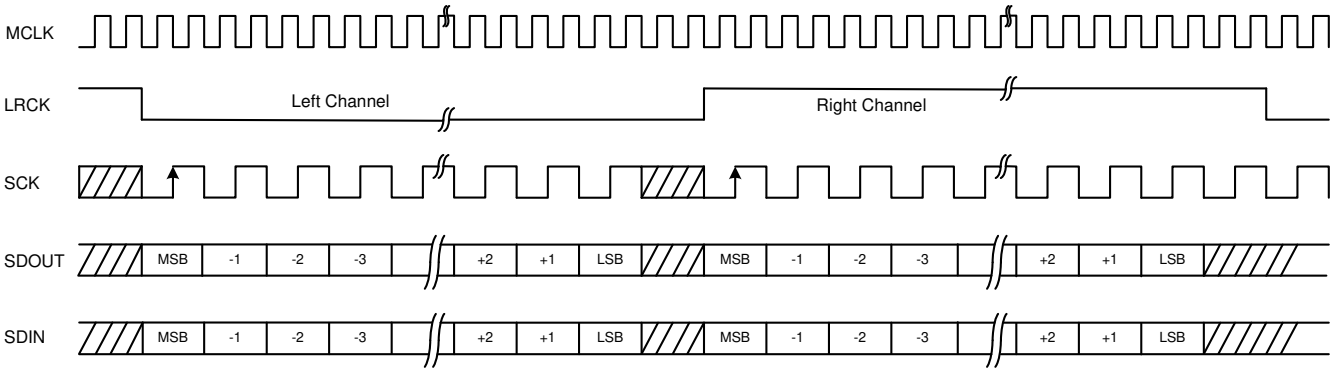


Figure 9. Left-Justified Format

MCLK: Master Clock. This is a high frequency clock to the DAC used for the Digital to Analog conversion process within the DAC. This clock will be a multiple of the LRCK going to the DAC. Typically MCLK = 250*LRCK or MCLK=256*LRCK.

LRCK: Left-Right Clock. This is used to synchronize the DAC audio data word timing with the CP2114 audio data word timing (i.e. edges are used to synchronize the beginning of the left and right audio samples).

SCK: Bit Synchronization Clock (also called BCLK). This provides a timing signal used by the DAC to latch the audio output data bits on SDOUT and assert the audio input data bits on SDIN.

SDOUT: Audio-out data stream going to the DAC.

SDIN: Audio-in data stream coming from the DAC.

Note: MCLK, LRCK, SCK and SDOUT are driven by the CP2114. SDIN is driven by the DAC.

The CP2114 supports only 48 kHz, 16 bit digital audio. This is typically not an issue for source USB audio as the device capabilities are reported to the host and any sample rate conversion (for say 44.1 kHz audio) is done automatically by the host. Some DACs however may require 24 bit digital audio data on the I2S data stream. In this case, the CP2114 will send the useful 16 bit audio to the DAC on SDOUT in the most significant 16 Bits and pad the remaining 8 bits of data with 0s. Likewise the CP2114 will read the MSB 16 bits of data on DIN and throw out the LSB 8 bits from SDIN. The CP2114 can be configured in 16 bit or 24 bit mode via a configuration option in the CP2114 one-time programmable ROM.

5.4. USB and Digital Audio Clock Requirements

The CP2114 supports a number of clock configurations allowing support for a variety of DACs and associated clocking options to optimize cost and quality. The two clocks of consideration are:

USB Clock: Full speed USB requires devices have a 12 MHz clock with tolerance of ±0.25%. This means the USB device (CP2114) must maintain its USB clock in the range of 11.97 MHz < USB Clock < 12.03 MHz. This range is supported by the CP2114 which also has built-in USB clock recovery. However, it does have implications on the audio DAC.

Digital Audio Clock (MCLK): DACs typically require that MCLK must be a multiple of LRCK, and this multiple is typically required to be 250 or 256 (or some sub or super multiple of these values). Given an audio sample rate of LRCK = 48 kHz, the resulting MCLK requirement is shown in Equation 1 or Equation 2.

$$MCLK = 250 \times 48\ kHz = 12.000\ MHz$$

Equation 1. Digital Audio Clock (MCLK) Frequency for a Multiple of 250

$$MCLK = 256 \times 48\ kHz = 12.288\ MHz$$

Equation 2. Digital Audio Clock (MCLK) Frequency for a Multiple of 256

A DAC accepting a multiple of 250 is thus compatible with USB clock requirements, whereas a DAC requiring a 256 multiple is fundamentally incompatible with USB clock requirements. In this case, generally one clock is needed for USB and another clock is needed for audio. The CP2114 supports a variety of configurations to address this issue and is covered in Section 5.6.

5.5. USB Audio Synchronization Modes

The USB standard defines synchronization relative to source and sinks. For audio-out, the host is the source and the device is the sink. For audio-in, the device is the source and the host is the sink. USB defines modes which govern the operation of sources and sinks according to the following table. The CP2114 supports asynchronous and synchronous modes.

Table 17. USB Audio Synchronization Modes

Mode	Source	Sink
Asynchronous	Free running clock Provides implicit feedforward to the sink	Free running clock Provides explicit feedback to the source
Synchronous	Clock locked to USB SOF Uses implicit feedback	Clock locked to the USB SOF Uses implicit feedback
Adaptive	Clock locked to sink Uses explicit feedback	Clock locked to the data flow Uses implicit feedback

Notes:
1. Implicit feedforward means the recipient determines the next data input size according to the current input size (i.e. if 48 samples were sent in the current frame then expect the same number in the next frame).
2. Explicit feedback means the recipient of the feedback will receive an explicit request for the number of samples to send in the next frame.

5.6. CP2114 Clock Configuration

The CP2114 always reports its capabilities to the USB host at a sample rate of 48 kHz and sample size of 16 bits. For source audio files differing from this format the USB host will automatically perform sample rate conversion. The CP2114 has the following configuration options:

Table 18. Clock Configuration Options

Configuration Parameter	Options	
Stream Type	Asynchronous	Synchronous
USB Clock Source	Internal	External
System Clock Source	Internal	External
System Clock Frequency	48 MHz	49.152 MHz
MCLK/LRCK Ratio	250	256

Table 19 shows all possible clock configuration settings for the CP2114. The CP2114 divides the USB source clock by 4 so a clock of 48MHz provides the 12 MHz clock needed for USB. The CP2114 divides the system clock by 4 to derive MCLK. So a 48 MHz system clock will generate MCLK=12 MHz. If the CP2114 is configured to operate in Asynchronous mode, it will automatically use explicit feedback to the host. If it is configured for Synchronous mode, then the sample synchronization method is noted in the table. There are a number of invalid clocking configurations that result from either the USB clock not resulting in 12 MHz or the MCLK/LRCK not being an integer divisor. Operating in asynchronous mode is recommended because it best accommodates any mismatch in host/CP2114 clocks. Operating in synchronous mode requires the CP2114 to adjust its internal oscillator to match the host sample rate, or to periodically drop or repeat an audio sample if SYSCLK is driven by an External Clock.

Table 19. Valid Clock Configuration Modes

Mode	USB Clock (USBCLK) Source	System Clock (SYSCLK) Source	Int Freq (MHz)	MCLK/ LRCK Ratio	Ext Osc Freq (MHz)	Notes
1	Int	Int	48	250	NA	■ Lowest cost - no external clock required ■ DAC must support 12.0 MHz MCLK ■ Sync mode: IntOsc adjusted to accommodate clock mismatch
2	Int	Ext	48	256	49.152	■ Async mode: best audio quality ■ Sync mode: must drop/repeat samples to accommodate clock mismatch
3	Ext	Int	48 49.152	250 256	48	■ IntOsc frequency dictated by DAC MCLK/ LRCK ratio ■ Sync mode: IntOsc adjusted to accommodate clock mismatch
4	Ext	Ext	48	250	48	■ DAC must support 12.0 MHz MCLK ■ Async mode: best audio quality ■ Sync mode: must drop/repeat samples to accommodate clock mismatch

Figure 10 shows the clocking scheme, with the configurable options shown in darker boxes.

- The USB clock frequency must always be 12MHz whether using the internal or an external oscillator.
- MCLK is SYSCLK/4 and so will be 12MHz or 12.288MHz (as determined by the DAC clock requirement).
- LRCK is MCLK divided by 250 or 256 in order to get the correct 48 kHz sample rate conversion.
  - For MCLK = 12.288 MHz, the LRCK divisor must be 256.
  - For MCLK = 12.000 MHz, the LRCK divisor must be 250.
- LRCK gates SCK and SCK is driven at SYSCLK / 14.
- SCK is the clock for SDOUT and SDIN.

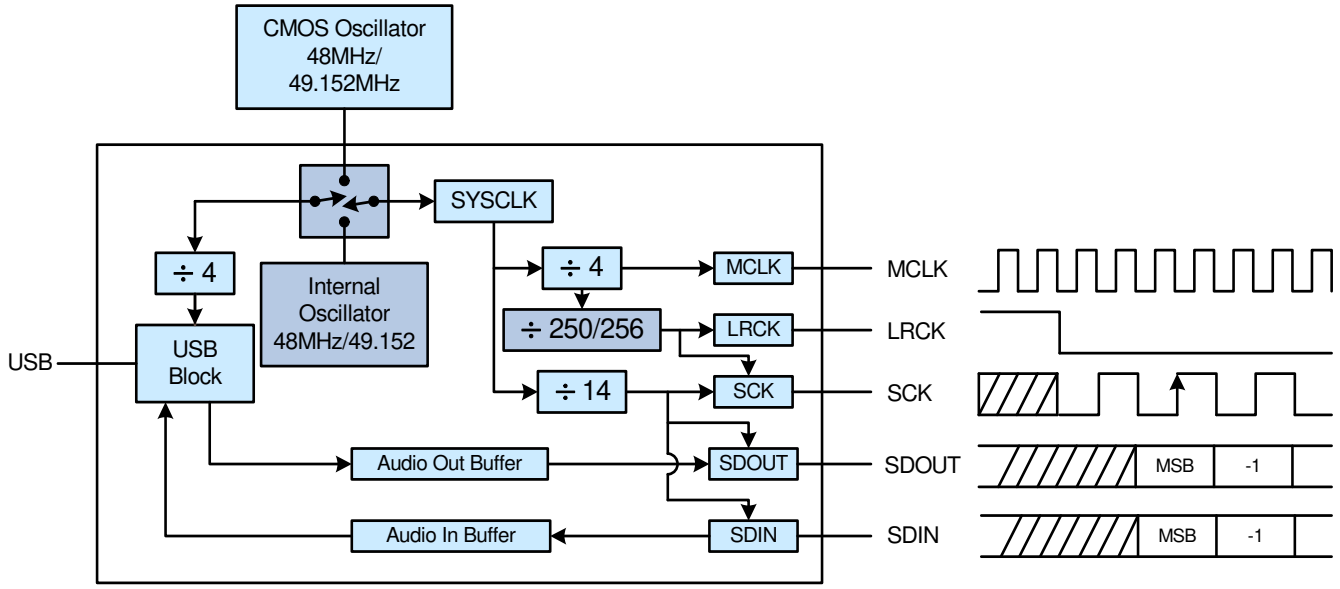


Figure 10. Clock Configuration Block Diagram

The particular setting for configuration 1 (USB and SYSCLK = internal frequency of 48 MHz, MCLK/LRCK divisor = 250) is shown in Figure 11.

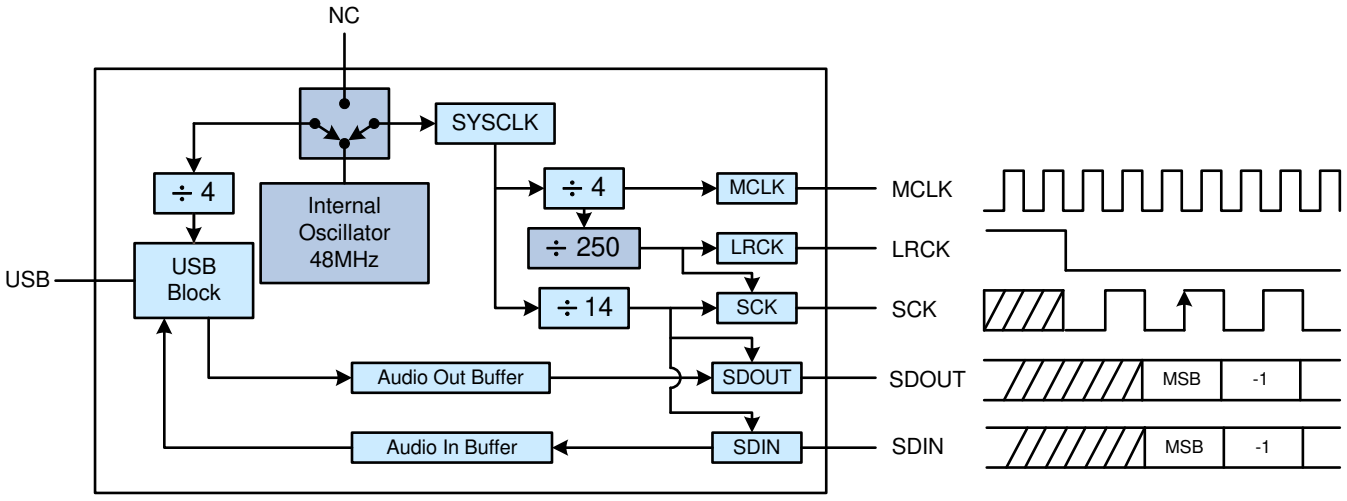


Figure 11. Configuration 1 Example

6. USB Function Controller and Transceiver

The Universal Serial Bus (USB) function controller in the CP2114 is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pullup resistors. The USB function controller manages all control, audio, and UART transfers between the USB and the CP2114. The USB Suspend and Resume modes are supported for power management of both the CP2114 device as well as external circuitry. The CP2114 will enter Suspend mode when Suspend signaling is detected on the bus. On entering Suspend mode, the Suspend signals are asserted. The Suspend signals are also asserted after a CP2114 reset until device configuration during USB enumeration is complete. The SUSPEND pin is logic high when the device is in the Suspend state, and logic low when the device is in the normal mode. The $\overline{\text{SUSPEND}}$ pin has the opposite logic value of the SUSPEND pin.

The CP2114 exits Suspend mode when any of the following occur: Resume signaling is detected or generated, a USB Reset signal is detected, or a device reset occurs. SUSPEND and $\overline{\text{SUSPEND}}$ are weakly pulled to VIO in a high impedance state during a CP2114 reset. If this behavior is undesirable, a strong pulldown (10 kΩ) can be used to ensure $\overline{\text{SUSPEND}}$ remains low during reset.

The logic level and output mode (push-pull or open-drain) of various pins during USB Suspend is configurable in the PROM. See Section 9 for more information.

7. Asynchronous Serial Data Bus (UART) Interfaces

The UART interface consists of the TX (transmit) and RX (receive) data signals as well as RTS (ready to send) and CTS (clear to send) flow control signals. The UART is programmable to support a variety of data formats and baud rates. The data formats and baud rates available are listed in Table 20.

Table 20. Data Formats and Baud Rates

Data Bits	5, 6, 7, and 8
Stop Bits	1, 1.5[1], and 2
Parity Type	None, Even, Odd, Mark, Space
Baud Rate	300 bps to 1 Mbps[2, 3, 4, 5]

Notes:
1. 1.5 stop bits only available when using 5 data bits.
2. Baud rates above 500,000 baud are not supported with 5 or 6 data bits
3. Max of 500 kBaud with flow control, audio playback only
4. Max of 230 kBaud with flow control, audio playback and listening
5. With flow control, audio can support higher baud rates, but throughput is greatly reduced.

The baud rate generator for the UART interface is very flexible, allowing the user to request any baud rate in the range from 300 bps to 1 Mbps. If the baud rate cannot be directly generated from the 48 MHz oscillator, the device will choose the closest possible option. The actual baud rate is dictated by Equation 3 and Equation 4.

$$\text{Clock Divider} = \frac{48\ \text{MHz}}{2 \times \text{Prescale} \times \text{Requested Baud Rate}}$$

$$\text{Prescale} = 4 \text{ if Requested Baud Rate} \leq 300 \text{ bps}$$
$$\text{Prescale} = 1 \text{ if Requested Baud Rate} > 300 \text{ bps}$$

Equation 3. Clock Divider Calculation

$$\text{Actual Baud Rate} = \frac{48\ \text{MHz}}{2 \times \text{Prescale} \times \text{Clock Divider}}$$

$$\text{Prescale} = 4 \text{ if Requested Baud Rate} \leq 300 \text{ bps}$$
$$\text{Prescale} = 1 \text{ if Requested Baud Rate} > 300 \text{ bps}$$

Equation 4. Baud Rate Calculation

Most baud rates can be generated with an error of less than 1.0%. A general rule of thumb for the majority of UART applications is to limit the baud rate error on both the transmitter and the receiver to no more than ±2%. The clock

divider value obtained in Equation 3 is rounded to the nearest integer, which may produce an error source. Another error source will be the 48 MHz oscillator, which is accurate to ±0.25%. Knowing the actual and requested baud rates, the total baud rate error can be found using Equation 5.

$$\text{Baud Rate Error (\%)} = 100 \times \left(1 - \frac{\text{Actual Baud Rate}}{\text{Requested Baud Rate}}\right) \pm 0.25\%$$

Equation 5. Baud Rate Error Calculation

The UART also supports the transmission of a line break. The length of time for a line break is programmable from 1 to 125 ms, or it can be set to transmit indefinitely until a stop command is sent from the application.

8. GPIO Pins

The CP2114 supports twelve user-configurable GPIO pins. Each of these GPIO pins are usable as inputs, open-drain outputs, or push-pull outputs. All of the pins have alternate functions which are listed in Table 21. To use the pin as a GPIO, the pin must first be configured for that mode. More information regarding the configuration and usage of these pins is available in “AN721: CP210x/CP21xx Device Customization Guide” available on the Silicon Labs website. The configuration of the pins is one-time programmable for each device. See Section 9 for more information about programming the GPIO pin functionality.

Table 21. GPIO Alternate Functions

Pin	Default Function	Alternate Function 1 (GPIO Function)	Alternate Function 2
GPIO.0_RMUTE	Record Mute	GPIO.0	
GPIO.1_PMUTE	Playback Mute	GPIO.1	
GPIO.2_VOL-	Volume Down	GPIO.2	
GPIO.3_VOL+	Volume Up	GPIO.3	
GPIO.4_RMUTELED	Record Mute LED	GPIO.4	
GPIO.5_TXT_DACSEL0	DAC Selector 0	GPIO.5	TX Toggle
GPIO.6_RXT_DACSEL1	DAC Selector 1	GPIO.6	RX Toggle
GPIO.7_RTS_DACSEL2	DAC Selector 2	GPIO.7	UART RTS
GPIO.8_CTS_DACSEL3	DAC Selector 3	GPIO.8	UART CTS
GPIO.9_CLKOUT	Clock Output	GPIO.9	
GPIO.10_TX	UART TX	GPIO.10	
GPIO.11_RX	UART RX	GPIO.11	

The difference between an open-drain output and a push-pull output is when the GPIO output is driven to logic high. A logic high, open-drain output pulls the pin to the VIO rail through an internal, pull-up resistor. A logic high, push-pull output directly connects the pin to the VIO voltage. Open-drain outputs are typically used when interfacing to logic at a higher voltage than the VIO pin. These pins can be safely pulled to the higher, external voltage through an external pull-up resistor. The maximum external pull-up voltage is 5 V.

The speed of reading and writing the GPIO pins is subject to the timing of the USB bus. GPIO pins configured as inputs or outputs are not recommended for real-time signalling.

8.1. GPIO.0-4—Audio Playback and Record

The CP2114 includes several audio playback and record signals, such as volume increase, volume decrease, playback mute, and record mute. When connected over USB, the CP2114 can control the host volume settings with these pins via the standard USB HID Consumer Control Interface. On the CP2114 evaluation board, these pins are all connected to buttons. Single-pressing the volume increase (GPIO.3_VOL+) and volume decrease (GPIO.2_VOL-) buttons will increase or decrease the volume; holding the button will continue increasing or decreasing the volume. If playback is muted, changing the volume with either of these buttons will unmute playback. In addition, there are two mute functions implemented as well. Single-pressing the record mute (GPIO.0_RMUTE) and the playback mute (GPIO.1_PMUTE) buttons will toggle between mute and unmute states. When record is muted, the signal GPIO.4_RMUTELED will be driven low (and illuminate an LED on the evaluation board).

8.2. GPIO.5-8—DAC Selection

The state of GPIO.5 through GPIO.8 specify which DAC configuration will be loaded after reset. By default, GPIO.5, GPIO.6, GPIO.7, and GPIO.8 are all configured for the DAC selection function (Alternate Function 1). If the four GPIO.5 through GPIO.8 pins are all configured as DAC Select inputs (their default configuration), the state of these pins specifies which DAC configuration will be loaded after reset (see Table 22). The boot DAC configuration specified by the one-time programmable ROM will be used if the state of these DAC Select pins is 1110b (Index 14), or if any of the four GPIO.5-8 pins have been configured to something other than DAC Select. The No DAC configuration option (1111b, i.e. Index 15) should be used when bringing up a new DAC. Using this configuration, DAC configuration text files can be written to RAM and tested until the DAC configuration string is finalized. At that point, the configuration string can be programmed into the one-time programmable ROM. DAC selection pin mapping is shown in Table 22.

Table 22. DAC Selection Pin Mapping

Index	GPIO.8 DACSEL3	GPIO.7 DACSEL2	GPIO.6 DACSEL1	GPIO.5 DACSEL0	Boot DAC configuration
0	0	0	0	0	Config[0]: CS42L55
1	0	0	0	1	Config[1]: WM8523
2	0	0	1	0	Config[2]: PCM1774
3	0	0	1	1	User-programmed DAC configurations
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	Boot DAC configuration is specified by the one-time programmable ROM
15	1	1	1	1	No DAC configuration

8.3. GPIO.5-6—UART Transmit and Receive Toggle

GPIO.5 and GPIO.6 are configurable as UART Transmit Toggle and Receive Toggle pins. These pins are logic high when a device is not transmitting or receiving data, and they toggle at a fixed rate as specified in Table 5 when UART data transfer is in progress. Typically, these pins are connected to two LEDs to indicate data transfer.

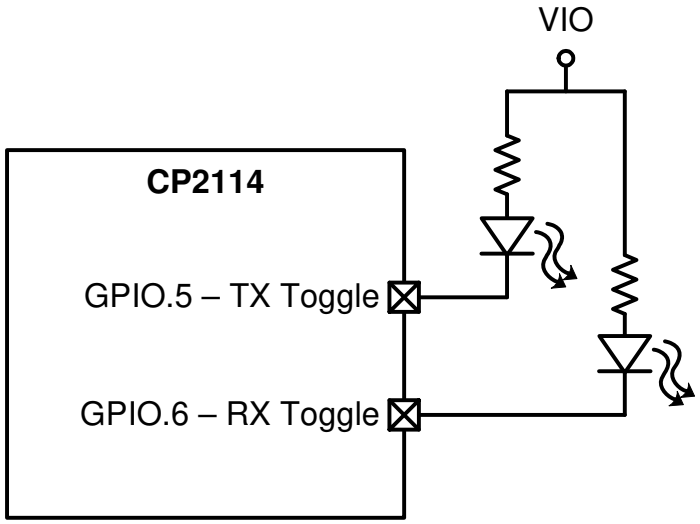


Figure 12. Transmit and Receive Toggle Typical Connection Diagram

8.4. GPIO.7-8—Hardware Flow Control (RTS and CTS)

To utilize the functionality of the RTS and CTS pins of the CP2114, the device must be configured to use hardware flow control.

RTS, or Ready To Send, is an active-low output from the CP2114 and indicates to the external UART device that the CP2114's UART RX FIFO has not reached the watermark level and is ready to accept more data. When the CP2114 is processing audio, the watermark level is 2 bytes. When the CP2114 is not processing audio, the watermark is 226 bytes. When the amount of data in the RX FIFO reaches the watermark, the CP2114 pulls RTS high to indicate to the external UART device to stop sending data.

CTS, or Clear To Send, is an active-low input to the CP2114 and is used by the external UART device to indicate to the CP2114 when the external UART device's RX FIFO is getting full. The CP2114 will not send more than two bytes of data once CTS is pulled high.

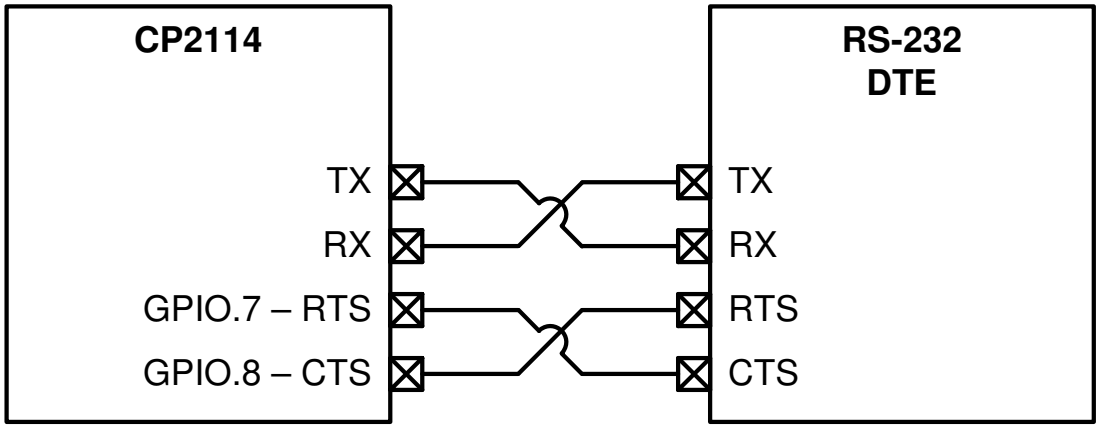


Figure 13. Hardware Flow Control Typical Connection Diagram

8.5. GPIO.9—Clock Output

GPIO.9 is configurable to output a configurable CMOS clock output. The clock output appears at the pin at the same time the device completes enumeration and exits USB Suspend mode. The clock output is removed from the pin when the device enters USB Suspend mode. The output frequency is configurable through the use of a divider and the accuracy is specified in Table 6. The output frequency is 24 MHz when the divider is set to 0 and the system clock is 48 MHz. The output frequency is 24.576 MHz when the divider is set to 0 and the system clock is 49.152 MHz. For divider values between 1 and 255, the output frequency is determined by the formula:

$$\text{GPIO.9 Clock Frequency} = \frac{\text{SYSCLK}}{2 \times \text{ClockDivider}}$$

Equation 6. GPIO.9 Clock Output Frequency

9. One-Time Programmable ROM

The CP2114 has an internal 5.5kB configuration one-time programmable ROM. There are 2 configuration areas in the one-time programmable ROM:

1. Global configuration area. This area stores the USB string descriptors and GPIO pin configuration. The CP2114 ships with default global configuration settings that allow the CP2114 to be used as-is for customer production. There is also a Customer Global Configuration area that provides customization of the device if desired.
2. Audio specific configuration area. This area stores up to 32 different audio configurations. The configurations set behavior of the CP2114 audio functions as well as configuration data for DACs.

The one-time programmable ROM is shown in Figure 14. Note that the CP2114 standard device ships pre-programmed for 3 different DACs, with the desired DAC being selected via the DAC Select pins (DACSEL0, DACSEL1, DACSEL2, DACSEL3). Additional DAC support can be added, and configuration of that DAC controlled by an one-time programmable ROM setting or by the DAC select pins. If the programmable ROM has not been programmed, the device uses the default configuration data shown in Table 26 and Table 27.

The configuration data ROM can be programmed by Silicon Labs prior to shipment with the desired configuration information. It can also be programmed in-system over the USB interface by adding a capacitor to the PCB. If the configuration ROM is to be programmed in-system, a 4.7 µF capacitor must be present between the VPP pin and ground. No other circuitry should be connected to VPP during a programming operation, and VIO must remain at 3.3 V or higher to successfully write to the configuration ROM.

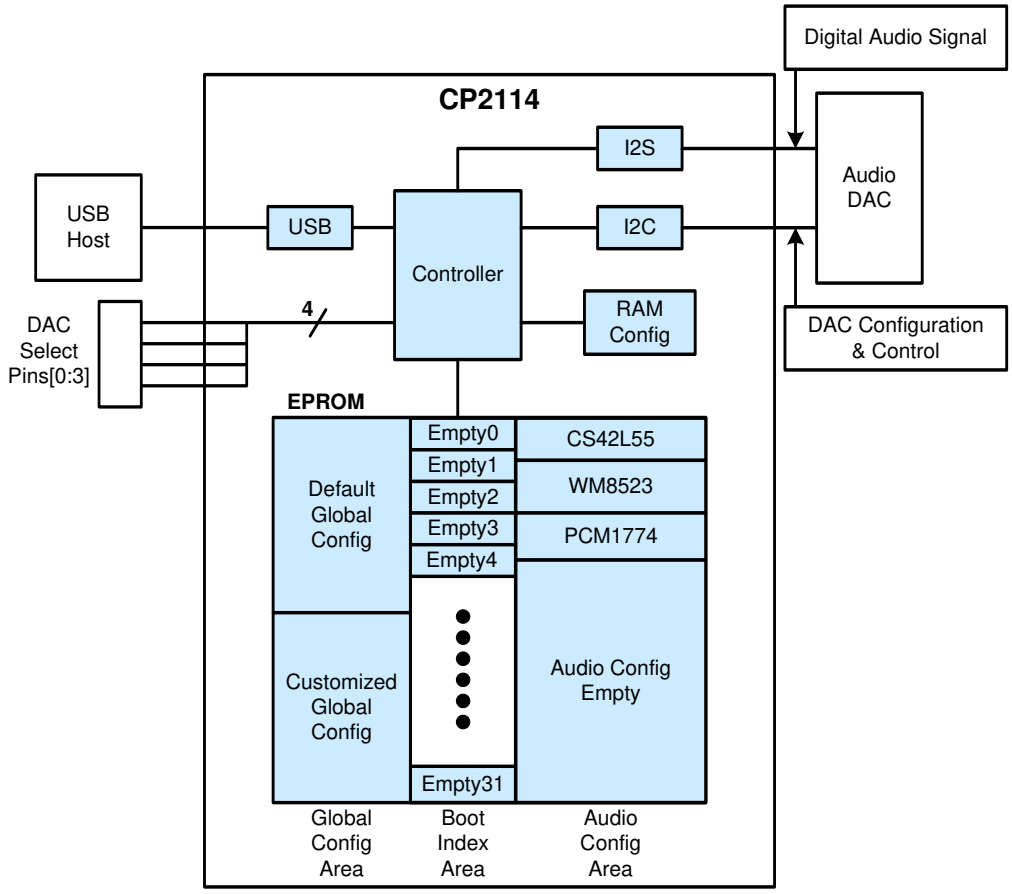


Figure 14. One-Time Programmable ROM Configuration Block Diagram

9.1. Audio Interface Configuration

The Audio configuration area is used to configure the boot index as well as the audio configuration strings. The boot index determines which of the programmed audio configuration strings will be used after reset. The following sections describe the audio interface in more detail.

9.1.1. Audio Interface Boot Configuration Process

The global configurations are automatically loaded when the CP2114 powers up. The audio boot configuration depends on the GPIO DAC select pin settings according to flow chart shown in Figure 15. The audio configuration can be set by a one-time programmable ROM boot index or by reading the boot index from the DAC Select pins. Setting the DAC_Select pins to 0x0F will not boot any DAC configuration. This is needed for adding support for a new DAC. In this case, the Silicon Labs GUI can be used to write the DAC settings. After experimentation and testing, the configuration can be written to the one-time programmable ROM. The one-time programmable ROM can be programmed in-system or Silicon Labs can provide preprogrammed parts with a customer configuration.

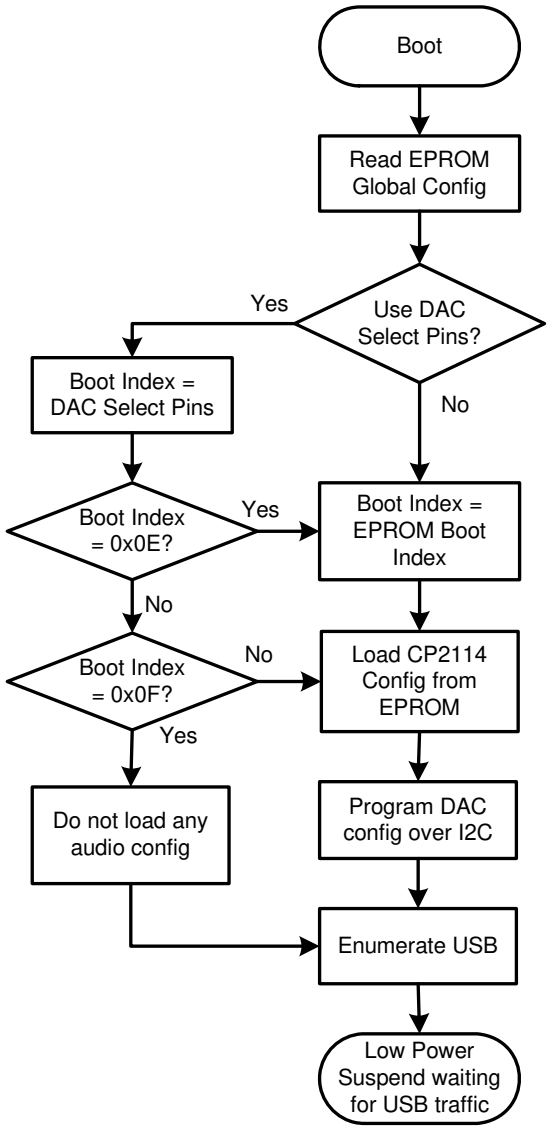


Figure 15. Boot Configuration Flowchart

9.1.2. Audio Configuration String Format

There are 2 components to the audio configuration of the CP2114:

1. Programmability of the CP2114 itself.
2. Programmability of the DAC.

To simplify the configuration of the CP2114 and the attached DAC, a unified configuration string is employed. The first 30 bytes of this configuration string are for the CP2114 audio and control properties. All data after byte 30 is for configuration of the DAC. Table 23 shows the format of the configuration string for the CP2114 and attached DAC. Note also that in the DAC configuration part there may be “in-band” commands. These are special characters that are used to specify delays and are documented in the following sections.

In the one-time programmable ROM, the audio configuration string is preceded by a two-byte length field specifying the total size of the configuration in bytes including the two-byte length field itself. The least significant byte (LSB) of the length field goes first. For example, the audio configuration for the CS42L55 DAC consists of 98-byte configuration. The length field itself is 2-byte long, which makes the total size 100-byte. The audio configuration starts with 0x64, 0x00 followed by the configuration string. The CP2114 configuration program only requires the configuration string. The program will parse the string, calculate the total length, and insert the length field before sending the request to the device.

Table 23. Audio Configuration String

Byte	Name	Description
0	DAC_Version	Identifies revision of DAC
1	User_Defined	User can store any info desired here
2	I2C_Address	Specify the DAC I2C address

Table 23. Audio Configuration String

Byte	Name	Description							
3	Audio_Props	Controls audio properties							
	Bit Position	7	6	5	4	3	2	1	0
	Bit Name	MB	ST	I2C_CK	I2C_PR	DRS	DVC	LJMS	AF
	MB	Mute Bit. 0: No affect 1: CP2114 will handle mute via mute bits at bytes 12,13,14,15 and 17							
	ST	Synchronization Type 0: Asynchronous. Will send feedback to USB host. 1: Synchronous. No feedback to USB host. Audio is synchronized via continuous clock adjustment of sample insert/drop, depending on clock configuration.							
	I2C_CK	Maximum I2C clock rate supported by the DAC. 0: 400 kHz 1: 100 kHz							
	I2C_PR	I2C Protocol for read operations. 0: Stop 1: Repeated Start							
	DRS	DAC Register Size 0: 8 bit 1: 16 bit							
	DVC	DAC Volume Control. 0: No volume control supported by DAC 1: Volume control supported by DAC If set, the CP2114 populates volume control in the feature unit USB descriptor. If clear, 0 is specified in volume control to prevent the host from sending SET_CUR requests.							
	LJMS	I2S Mode. Only applies if using Left Justified format. 0: 16bit Left Justified Mode. 1: 24bit Left Justified Mode							
	AF	Audio Format 0: I2S format 1: Left Justified format							
4	Min_Volume	Minimum Volume in dB, 8-bit signed. This corresponds to the volume control attribute MIN in USB Audio spec.							
5	Max_Volume	Maximum Volume in dB, 8-bit signed. This corresponds to the volume control attribute MAX in USB Audio spec.							
6	Vol_Step	Volume Step Counts per dB. For instance, if volume resolution is 0.25 dB, 4 shall be written. A computed RES is returned in response to volume control attribute query of RES from the host.							

Table 23. Audio Configuration String

Byte	Name	Description							
7	System_Props	System Properties							
	Bit Position	7	6	5	4	3	2	1	0
	Bit Names	DMMF	ARE	SVRP	VUR	UCS	SCS	SF	ACR
	DMMF	DAC Min/Max register Format. 0: Unsigned 1: Signed							
	ARE	Analog Record Enabled 0: Disable 1: Enable							
	SVRP	Secondary Volume Registers Polarity. 0: Secondary volume registers have same polarity as primary registers 1: Secondary volume registers have opposite polarity as primary registers. If only line out is present on the DAC, primary shall be line out; if only headphone is present, primary shall be headphone. If both line out and headphone are present on the DAC, either can be designated as primary. CP2114 updates either or both registers when the host changes volume. Some DACs may require a separate bit as a “take into effect immediately” bit.							
	VUR	Volume Update Registers. Some DACs require a specific register is written for volume updates to take effect. 0: DAC has no volume update registers. 1: DAC has volume update registers.							
	UCS	USB Clock Source 0: USB clock uses internal oscillator 1: USB clock uses external oscillator							
	SCS	System Clock Source. NOTE: Audio clocks will be driven from this source. 0: Audio uses internal oscillator 1: Audio uses external oscillator							
	SF	System Frequency 0: 48MHz 1: 49.152MHz							
	ACR	Audio Clock Ratio. This is the MCLK/LRCK ratio. 0: 250 1: 256							
8	DPVCL	DAC Primary Volume Control Left channel register address.							
9	DPVCR	DAC Primary Volume Control Right channel register address.							
10	DSVCL	DAC Secondary Volume Control Left channel register address.							
11	DSVCR	DAC Secondary Volume Control Right channel register address.							
12	DPMBLC	DAC Primary Mute Bit Left Channel register address. Ignored if MB=0.							
13	DPMBRC	DAC Primary Mute Bit Right Channel register address. Ignored if MB=0.							
14	DSMBLC	DAC Secondary Mute Bit Left Channel register address. Ignored if MB=0.							
15	DSMBRC	DAC Secondary Mute Bit Right Channel register address. Ignored if MB=0.							

Table 23. Audio Configuration String

Byte	Name	Description							
16	DVCB	DAC Volume Control Bits start position and bits count. Some DAC volume registers have limited significant bits. This field lets the significant bits be specified. For example if the volume registers use only bit [6:0] you would set Volume_Bit_Count=7 and Volume_Bit_Start=0.							
	Bit position	7	6	5	4	3	2	1	0
	Bit name	VBC				VBS			
	VBC	Volume Bit Count. Specifies number of significant bits for the volume registers							
	VBS	Volume Bits Start. Specifies the start position of the volume significant bits.							
17	DMBP	DAC Mute Bit Positions.							
	Bit Position	7	6	5	4	3	2	1	0
	Bit Name	DMBPL				DMBPR			
	DMBPL	DAC Mute Bit Position Left channel. Ignored if MB=0.							
	DMBPR	DAC Mute Bit Position Right channel. Ignored if MB=0.							
18	DVMV	DAC Value Minimum Volume. Specifies the value needed for minimum volume from the DAC							
19	DVXV	DAC Value Maximum Volume. Specifies the value needed for maximum volume from the DAC							
20	DVUBP	DAC Volume Update Bit Position. Ignored VUR=0.							
	Bit position	7	6	5	4	3	2	1	0
	Bit name	DVUBPL				RCUBP			
	DVUBPL	DAC Volume Update Bit Position Left channel							
	RCUBP	DAC Volume Update Bit Position Right channel							
21	DPVURL	DAC Primary Volume Update Register Left channel register address. Ignored f VUR=0.							
22	DPVURR	DAC Primary Volume Update Register Right channel register address. Ignored f VUR=0.							
23	DSVURL	DAC Secondary Volume Update Register Left channel register address. Ignored f VUR=0.							
24	DSVURR	DAC Secondary Volume Update Register Right channel register address. Ignored f VUR=0.							

Table 23. Audio Configuration String

Byte	Name	Description							
25	DMP1	DAC Mute Property 1							
	Bit Position	7	6	5	4	3	2	1	0
	Bit Name	GPION				x	x	SWM	MBG
	GPION	GPIO Number (0..11) used for DAC mute. Ignored of MBG=0.							
	SWM	GPIO State When Muted. Ignored of MBG=0. 0: Muted when GPIO is low 1: Muted when GPIO is high.							
	MBG	Mute By GPIO. 0: Do not use GPIO for mute. 1: Use GPIO for Mute.							
26	DMP2	DAC Mute Property 2							
	Bit Position	7	6	5	4	3	2	1	0
	Bit Name	x	x	x	x	x	x	MBZ	MBVR
	MBZ	Mute By Zeros. 0: Do not mute by sending 00's to the DAC 1: Mute by sending 00's to the DAC. This is useful for a DAC that does not support hardware mute or volume functions. Not supported when playback and record are both active.							
	MBVR	Mute By Volume Register. 0: Do not mute via the volume register. 1: Mute via the volume register. Some DACs mute by sending a specific value to the volume register.							
27	DVMV	DAC Volume Mute Value. Mute by sending this value to the volume registers. Ignored if MBVR=0.							
28	Reserved	Reserved							
29	Reserved	Reserved							
30-xx	DAC Config	Start of DAC configuration string and "in-band" commands							

9.1.3. DAC Configuration String

Starting at byte 30, a DAC configuration string is used to communicate with the DAC over the I2C interface. If the DAC register size bit is 0 (indicating 8-bit mode), the DAC register/value pairs should be written in the format of:

Byte[30] = <DAC_Register_Address>
Byte[31] = <DAC_Register_Value>
Byte[32] = <DAC_Register_Address>
Byte[33] = <DAC_Register_Value>
...

If the DAC register size bit is 1 (indicating 16-bit mode), the DAC register/value pairs should be written in the format of:

Byte[30] = <DAC_Register_Address>
Byte[31] = <DAC_Register_Value_MSB>
Byte[32] = <DAC_Register_Value_LSB>
Byte[33] = <DAC_Register_Address>
Byte[34] = <DAC_Register_Value_MSB>
Byte[35] = <DAC_Register_Value_LSB>
...

9.1.4. DAC Configuration In-Band Commands

To support special functions such as GPIO outputs, arbitrary delay in between DAC register access, DAC power off sequence in suspend and power on sequence in active mode, the CP2114 supports special in-band commands starting from byte 30. These commands are identified by command codes 0xFA to 0xFF. When parsing DAC register/value pairs, if CP2114 firmware encounters 0xFA to 0xFF in the <DAC_Register_Address> field, the CP2114 performs the task associated with the command instead of sending it to the DAC.

- SUSPEND_SEQUENCE specifies a sequence of DAC register/value pairs/triplets to power down certain blocks on the DAC in suspend mode to minimize power consumption.
- ACTIVE_SEQUENCE specifies a sequence of DAC register/value pairs/triplets to power up certain blocks on the DAC in active mode.
- The DELAY_MICROSECONDS, SET_GPIO and DELAY_MILLISECONDS in-band commands can be embedded in SUSPEND_SEQUENCE and ACTIVE_SEQUENCE if needed.
- SET_GPIO sets a specified GPIO to high or low.
- DELAY_MICROSECONDS instructs the firmware to introduce a coarse delay of n microseconds as specified in the parameter list. Similarly, DELAY_MILLISECONDS instructs the firmware to introduce a course delay in milliseconds.

The format of most In-band commands except for SUSPEND_SEQUENCE and ACTIVE_SEQUENCE is analogous to DAC register/value pairs/triplets.

Table 24. DAC Configuration In-Band Commands

Name	Identifier	In-Band Parameter List DAC register size = 0 (8bit)	In-Band Parameter List DAC register size = 1(16bit)
SUSPEND_ SEQUENCE	0xFA	<Length in bytes of register/value pairs or other in-band commands> <reg or other in-band commands> <value or in-band command parameter>…	<Reserved> <Length in bytes of register/value triplet pairs or other in-band commands> <reg or other in-band command ID> <Value_Hi or high byte of in-band command parameter> <Value_Lo or low byte of inband command parameter>
ACTIVE_ SEQUENCE	0xFB	<Length in bytes of register/value pairs or other in-band commands> <reg or other in-band commands> <value or in-band command parameter>…	<Reserved> <Length in bytes of register/value triplet pairs or other in-band commands> <reg or other in-band command ID> <Value_Hi or high byte of in-band command parameter> <Value_Lo or low byte of inband command parameter>
REENUMER- ATE	0xFC	<Reserved>	<Reserved><Reserved>
DELAY_ MICROSEC- ONDS	0xFD	<Delay>	<Reserved> <Delay>
SET_GPIO	0xFE	(<GPIO_State> << 7 | <GPIO_Number> & 0x0F)	<Reserved> (<GPIO_State> << 7 | <GPIO_Number> & 0x0F)
DELAY_MIL- LISECONDS	0xFF	<Delay>	<Reserved> <Delay>

The combination of SET_GPIO in-band commands and DELAY commands can be used to send pulses or toggle output GPIOs (assuming that these GPIOs have been configured as output pins). Some DACs may require DAC reset via a GPIO pin, this can be accomplished with in-band commands as well.

9.1.5. DAC Initialization

The DAC configuration string should configure the DAC to initialize with muted playback. DAC volume registers should be set to minimum. This allows CP2114 to synchronize with the host at startup.

9.1.6. Example CP2114 Configuration String

As can be seen in the Audio Configuration String Format, a number of fields are dedicated to defining how the DAC volume and mute function are implemented in the DAC. This is needed for the CP2114 to properly scale the volume from dB to DAC register values using a linear equation and send volume and mute messages from the host to the DAC. As an example of CP2114 configuration string, Table 25 shows the configuration string in one-time programmable ROM as shipped for the CS42L55 codec.

Table 25. CS42L55 Configuration String

Byte	Value	Description
0	01	DAC Version = 01. This can simply be an identifier for the configuration
1	00	User byte – any purpose
2	94	I2C Address of this DAC is 0x94
3	A6	MB = 1 Mute is handled with this DAC. ST = 0. Use Asynchronous mode—provide feedback to the host. I2C_CK = 1. Use 100 kHz I2C clock. I2C_PR = 0. I2C uses stop bit. DRS = 0. DAC has 8bit registers. DVC = 1. DAC volume control is supported LJMS = 1. 24bit Left Justified mode is used. AF = 0. Left Justified format is used.
4	C4	Minimum volume value for the DAC is 0xC4 = -60dB.
5	0C	Maximum volume for the DAC is 0x0C = 12dB
6	01	Volume step per dB is 1.
7	E0	DMMF = 1. DAC min/max registers are signed. ARE = 1. Analog Record is enabled. SVRP = 1. Secondary volume registers have opposite polarity as primary registers. VUR = 0. DAC does not have volume update (take effect) registers. UCS = 0. USB clock uses internal oscillator. SCS = 0. System clock uses internal oscillator. SF = 0. System frequency is 48 MHz. ACR = 0. Audio Clock Ration (MCLK/LRCK) is 250.
8	1C	DPVL = 0x1C. DAC Primary Volume Control Left channel register address is 0x1C
9	1D	DPVR = 0x1D. DAC Primary Volume Control Right channel register address is 0x1D
10	1A	DSVL = 0x1A. DAC Secondary Volume Control Left channel register address is 0x1A
11	1B	DSVR = 0x1B. DAC Secondary Volume Control Right channel register address is 0x1B
12	1C	DPMBLC = 0x1C. DAC Primary Mute Bit Left channel register address is 0x1C
13	1D	DPMBRC = 0x1D DAC Primary Mute Bit Right channel register address is 0x1D
14	1A	DSMBLC = 0x1A. DAC Secondary Mute Bit Left channel register address is 0x1A
15	1B	DSMBRC = 0x1B. DAC Secondary Mute Bit Right channel register address is 0x1B
16	70	DVCB = 0x70. VBC = 7. Volume register has 7 significant bits. VBS = 0. Volume control starts at bit 0.
17	77	DMBP = 0x77. DMBPL = 7. DAC Mute Bit Position Left channel is bit 7 DMBPR = 7. DAC Mute Bit Position Right channel is bit 7

Table 25. CS42L55 Configuration String

Byte	Value	Description
18	44	DVMV = 0x44. DAC value for minimum volume is 0x44.
19	0C	DVXV = 0x0C. DAC value for maximum volume is 0x0C.
20	00	NA - No volume update register.
21	00	NA - No volume update register.
22	00	NA - No volume update register.
23	00	NA - No volume update register.
24	00	NA - No volume update register.
25	00	NA. MBG = 0. No Mute by GPIO.
26	00	MBZ = 0. Do not mute by sending 00's. MBVR = 0. Do not mute but volume register.
27	00	DVMV = 0. Do not mute by sending value to register.
28	00	Reserved
29	00	Reserved

9.2. USB and GPIO Configuration

The global configuration area is used to store USB descriptors and GPIO configuration. If the programmable ROM has not been programmed, the default configuration data shown in Table 26, Table 27, and Table 28 is used. In addition, each field in Table 26, Table 27, and Table 28 may only be customized once.

Table 26. Default USB Configuration Data

Name	Value
Vendor ID	10C4h
Product ID	EAB0h
Power Descriptor (Attributes)	80h (Bus-powered)
Power Descriptor (Max. Power)	32h (100 mA)
Release Number	0100h (Release Version 01.00)
Manufacturer String	“Silicon Laboratories” (62 ASCII characters maximum)
Product Description String	“CP2114 USB-Audio Bridge” (62 characters maximum)
Serial String	Unique 8 character ASCII string (30 characters maximum)

Table 27. Default GPIO Data

Pin Name	Default Function
GPIO.0_RMUTE	Record Mute
GPIO.1_PMUTE	Playback Mute
GPIO.2_VOL-	Volume Down
GPIO.3_VOL+	Volume Up
GPIO.4_RMUTELED	Record Mute LED
GPIO.5_TXT_DACSEL0	DAC Selector 0
GPIO.6_RXT_DACSEL1	DAC Selector 1
GPIO.7_RTS_DACSEL2	DAC Selector 2
GPIO.8_CTS_DACSEL3	DAC Selector 3
GPIO.9_CLKOUT	Clock Output
GPIO.10_TX	UART TX
GPIO.11_RX	UART RX

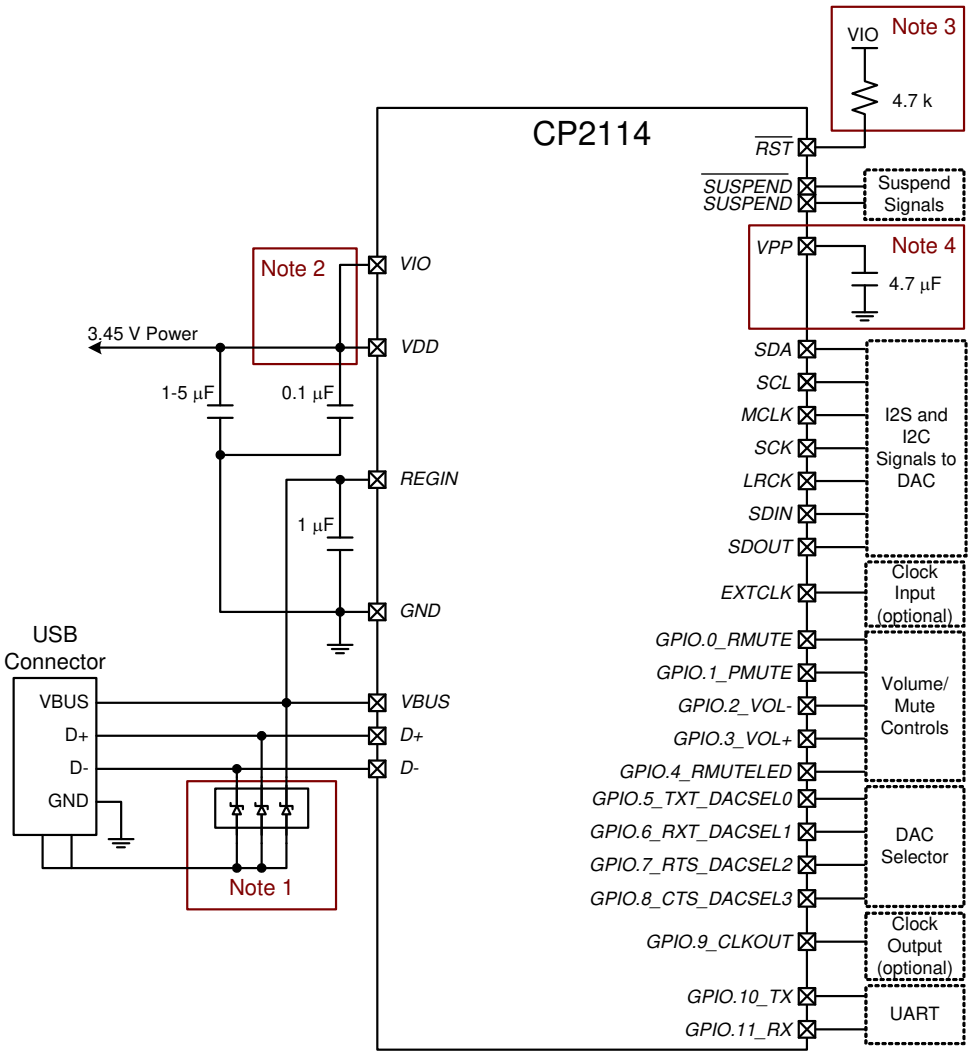
Table 28. Default UART and Suspend Data

Name	Default Function
Flush Buffers	Flush TX and RX FIFO on open
SUSPEND	Output—Push Pull
$\overline{\text{SUSPEND}}$	Output—Push Pull
Suspend Latch	0x0000
Suspend Mode	0x0000
Clock Divider	Divide by 1

While customization of the USB configuration data is optional, customizing the VID/PID combination is strongly recommended. A unique VID/PID will prevent the device from being recognized by any other manufacturer’s software application. A vendor ID can be obtained from www.usb.org or Silicon Labs can provide a free PID for the OEM product that can be used with the Silicon Labs VID. All CP2114 devices are pre-programmed with a unique serial number. It is important to have a unique serial if it is possible for multiple CP2114-based devices to be connected to the same PC.

10. Voltage Regulator

The CP2114 includes an on-chip voltage regulator with a 3.45 V output. This allows the CP2114 to be configured as either a USB bus-powered device or a USB self-powered device. A typical connection diagram of the device in a bus-powered application using the regulator is shown in Figure 16. When enabled, the voltage regulator output appears on the VDD pin and can be used to power external devices. See Table 4 for the voltage regulator electrical characteristics. If it is desired to use the regulator to provide VDD in a self-powered application, the same connections from Figure 16 can be used, but connect REGIN to an on-board 5 V supply, and disconnect it from the VBUS pin.

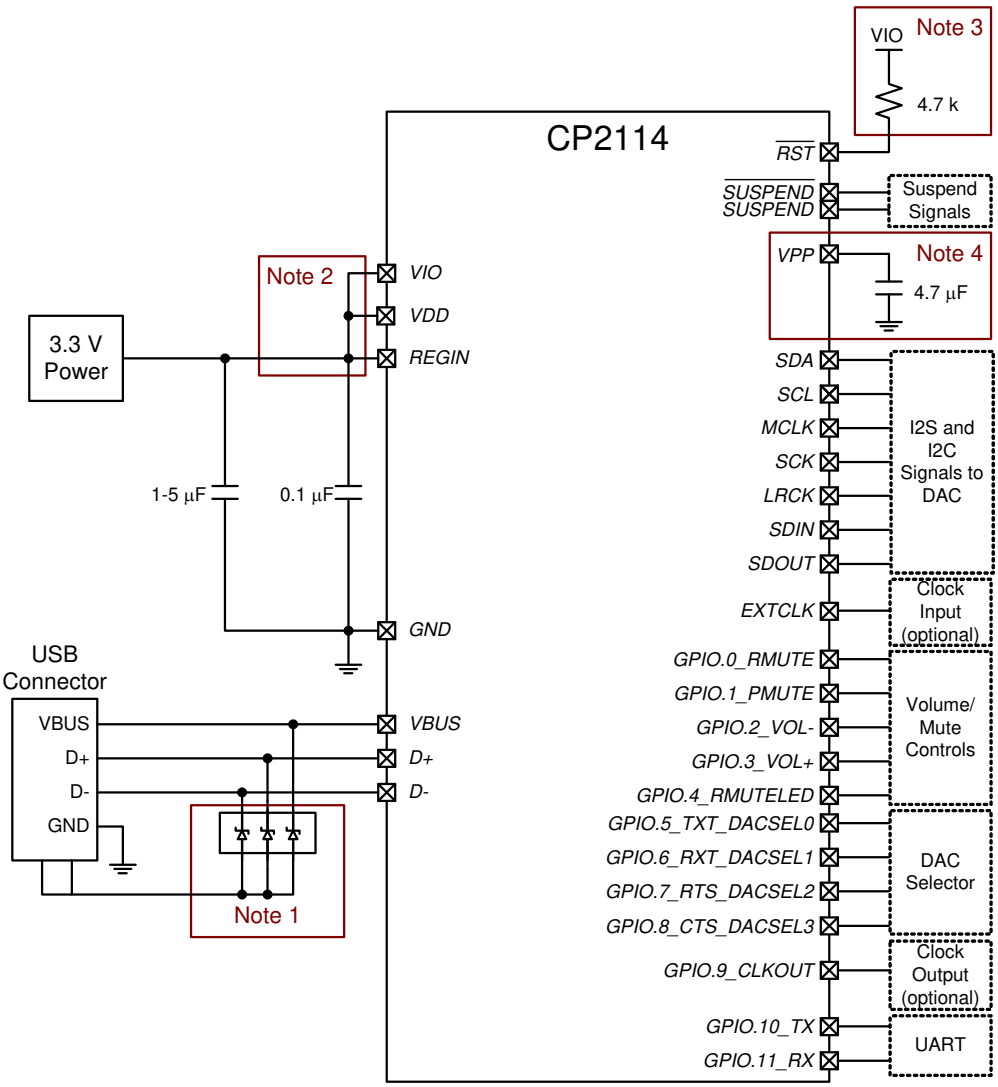


Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : VIO can be connected directly to VDD or to a supply as low as 1.8 V to set the I/O interface voltage.
Note 3 : An external pull-up is not required, but can be added for noise immunity.
Note 4 : If configuration ROM is to be programmed via USB, a 4.7 µF capacitor must be added between VPP and ground. During a programming operation, the pin should not be connected to other circuitry, and VIO must be at least 3.3 V.

Figure 16. Typical Bus-Powered Connection Diagram

Alternatively, if 3.0 to 3.6 V power source is supplied to the VDD pin, the CP2114 can function as a USB self-powered device with the voltage regulator bypassed. For this configuration, the REGIN input should be tied to VDD to bypass the voltage regulator. A typical connection diagram showing the device in a self-powered application with the regulator bypassed is shown in Figure 17.

The USB max power and power attributes descriptor must match the device power usage and configuration. See application note “AN721: CP210x/CP21xx Device Customization Guide” for information on how to customize USB descriptors for the CP2114.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : VIO can be connected directly to VDD or to a supply as low as 1.8 V to set the I/O interface voltage.
Note 3 : An external pull-up is not required, but can be added for noise immunity.
Note 4 : If configuration ROM is to be programmed via USB, a 4.7 µF capacitor must be added between VPP and ground. During a programming operation, the pin should not be connected to other circuitry, and VIO must be at least 3.3 V.

Figure 17. Typical Self-Powered Connection Diagram (Regulator Bypass)

11. CP2114 Interface Specification and Windows Interface DLL

The CP2114 is a USB Human Interface Device (HID), and as most operating systems include native HID drivers, custom drivers do not need to be installed. The CP2114 does not fit one of the standard HID device types, such as a keyboard or mouse, and any CP2114 PC application needs to use the CP2114's HID specification to communicate with the device. The low-level HID specification for the CP2114 is provided in "AN433: CP2110/CP2114 HID Interface Specification." This document describes all of the basic functions for opening, reading from, writing to, and closing the device, as well as the ROM programming functions.

A Windows DLL that encapsulates the CP2114 HID interface and also adds higher level features such as read/write time-outs is provided by Silicon Labs. This DLL is the recommended interface for the CP2114. The Windows DLL is documented in CP2114 Windows DLL Specification.

Both of these documents and the DLL are available online at http://www.silabs.com/.

12. Relevant Application Notes

The following Application Notes are applicable to the CP2114. The latest versions of these application notes and their accompanying software are available at http://www.silabs.com/appnotes.

- **AN721: CP210x/CP21xx Device Customization Guide**. This application note describes how to use the AN721 software CP21xxSetIDs to configure the USB parameters on the CP21xx devices.
- **AN433: CP2110/CP2114 HID to UART API Specification**. This application note describes how to interface to the CP2114 using the Windows Interface DLL and the Max OS-X dylib.

NOTES:

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