Technical Overview

Features

The Harris AC/ACT series of Advanced High Speed CMOS Integrated Circuits is comprised of a broad range of logic types equivalent in performance and speed to FAST, AS (Advanced Schottky), and S (Schottky) bipolar types, but superior in that they require substantially less power in logic operations. Each CMOS circuit function is offered in two basic logic series, as follows:

CD54/74ACTXXX-Series Types. These types feature TTL input-voltage-level compatibility and, using the same standardized pinouts, provide reduced power- consumption alternatives to the very high power consumption of the FAST, AS, and S bipolar logic series types.

CD54/74ACXXX-Series Types. These types feature CMOS input-voltage-level compatibility and, using the same standardized pinouts, provide enhanced system performance (better system noise margin) at speeds similar to those of FAST, AS, and S logic series types.

The AC/ACT family consists of a comprehensive set of octal buffers, octal latches, octal flip-flops, octal transceivers in both the classic 200 series pinout and the newer 500 series flow through pinout. In addition, selected 551 inverters, gates, flip-flops, Schmitt triggers, plus selected MSI counters, registers, multiplexers, decoders and arithmetic functions are included for well over 100 circuits, in both the ACT and AC series.

AC/ACT Family Features

Following is a listing of the features of the AC/ACT family of logic devices.

- Functionally and Pin-Compatible with Industry 54 and 74 Bipolar Types in the FAST, AS, and S Series
- CMOS Rail-To-Rail Output Swing for Maximum Noise Margins
- Fanout (Over Temperature)
  - 2400 AC/ACT Loads
  - 15 FAST Loads
  - 48 AS Loads

NOTE: FAST, AS and S 74 series types are rated for only 0°C to +70°C.

- Wide Operating Temperature Ranges
  - PDIP and SOIC 74 Series . . . . . -55°C to +125°C
  - Chip-Form 54 Series . . . . . -55°C to +125°C
- Balanced Propagation and Output Transition Times
- Significant Power Reduction Compared to FAST, AS, and S TTL Logic, Resulting In Improved Equipment Reliability
- Outputs Reliably Drive 50Ω Lines (at +85°C) and 75Ω Lines (at +125°C) Without Need for Terminations
- Meets JEDEC Standard Number 20A
- Octal Types Have Typically a 1V Peak (DIP Package) Simultaneous Switching Voltage Transient, Similar to FAST Series. Peak is Typically 0.8V in the SOIC Package
- CMOS Input Compatible

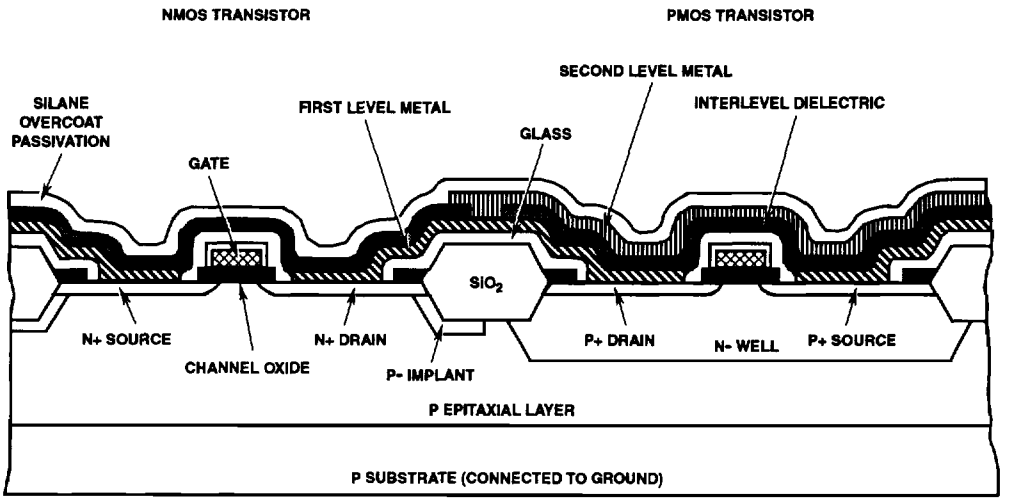


FIGURE 1. CROSS SECTION OF AC/ACT TWO LEVEL METAL CMOS PROCESS

TABLE 1. PERFORMANCE COMPARISON OF AC/ACT AND FAST LOGIC FUNCTIONS

PARAMETERS		SYMBOL	TEST CONDITIONS	74 SERIES AC/ACT			74 SERIES FAST			UNITS
Power Consumption				POWER CONSUMPTION FREQUENCY (MHz)						
				0	1	10	0	1	10	
	Four-Stage Counter (191)			0.44	5.5	55	204	224	306	mW
	Octal Transceiver (245)			0.44	39	390	468	514	702	mW
Operating Voltage	FAST			-			4.75 to 5.25			V
	AC			1.5 to 5.5			-			V
	ACT			4.5 to 5.5			-			V
Operating Temperature Range				-55 to +125			0 to +70			°C
Noise Margin	FAST to FAST		V_{CC} = 4.5V, Rated Load	-			0.4/0.3			V
	AC to AC (High/Low)			1.25/1.25			-			V
	ACT to ACT			1.8/0.36			-			V
Input Switching Voltage Variation over the Operating Temperature Range				$V_S \pm 50$			$V_S \pm 200$			mV
Output Drive Current	SSI/MSI Logic	I_{OL}/I_{OH}	V_{CC} = 4.5V	±24			+20/-1			mA
	Three-State Buffers			±24			+24/-3			mA
	Bus Drivers			±24			+64/-15			mA
Propagation Delay	Octal Buffer (240)	t_{PHL}/t_{PLH}		7.8/7.8			6/9			ns
	Flip-Flop (74)			9.4/9.4			10.5/8.5			ns
Input Current		I_{IL}		+1			+1600			µA
		I_{IH}		-1			-20			µA
Three-State Output Current				±5			±50			µA

Series Features

Following are the special features of the AC series of Advanced CMOS High Speed ICs.

- 1.5V to 5.5V Operation
- High Noise Immunity
  - $N_{IL} = N_{IH} = 30\%$ for $V_{CC} = 3V$ to 5V
  - $N_{IL} = N_{IH} = 20\%$ for $V_{CC} = 1.5V$ to 3V

Following are the special features of the ACT Series of Advanced CMOS High Speed ICs.

- 4.5V to 5.5V Operation
- Direct TTL Input Logic Compatible
  - $V_{IL} = 0.8V$ Max
  - $V_{IH} = 2V$ Min
- Similar to FAST Specifications Except for the 64mA I_{OL} of FAST Drivers. (See FCT Series of Logic Types for Higher-Current Drivers.)

Comparison of AC/ACT Logic Types with FAST/AS Types

Harris AC and ACT types have many outstanding advantages when compared with the conventional high current bipolar FAST and AS logic types. The Advanced CMOS Logic AC and ACT types can replace the bipolar types in existing equipment and in new equipment designs requiring devices that operate at frequencies up to 100MHz. Table 1 compares the significant operating characteristics of the AC and ACT CMOS types with those of the bipolar FAST logic family.

AC/ACT IC Process and Structure

Advanced CMOS high speed products are fabricated with an advanced small geometry CMOS process and design rules that are tailored to meet the specified high speed and high output drive current, and to tame the high switching current transients associated with high speed designs. Figure 1 shows the cross section of an AC/ACT chip. The starting material is a p-substrate topped with a thin p-epitaxial surface layer; hence, this process is an n-well type. The epitaxial surface serves essentially to eliminate SCR latch up and provides for a low impedance surface conduction path that enhances electrostatic discharge capability. The n and p diffusions are ion-implanted. Polysilicon gates having an effective length of 1.5µm are deposited over a thin 300Å gate oxide. Active source and drain areas are automatically aligned to the separate gates with the polysilicon gates acting as a mask. This structure drastically reduces the parasitic capacitances between the gate and the n and p areas (see Figure 2) and, as a result, enhances switching speed. The n and p transistors are isolated by the areas of silicon dioxide, as shown in Figure 1.

A major structural feature of AC/ACT devices is the use of two metallization levels. Logic interconnections are shorter because of the dual interconnect layers, and V_{CC} and ground distribution busing is greatly enhanced to handle the switching transient current, which can exceed one ampere for AC/ACT octal buffer types. When used in chip form, the AC/ACT substrate should not be connected to any potential above ground.

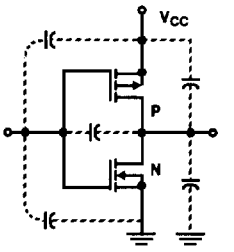


FIGURE 2. PARASITIC CAPACITANCES IN A CMOS INVERTER

Input Characteristics

The inputs of the AC/ACT devices are sensitive to voltage levels. The only input current is the reverse diode leakage (a few picoamperes) of the protection network for electrostatic discharge. The definitive I/O switching characteristics of an input stage is shown in Figure 3 for AC and ACT types. The specified Min/Max input switching voltages are guaranteed over the operating temperature range. Actual shift of the input voltage over the temperature range -55°C to +125°C is 100mV.

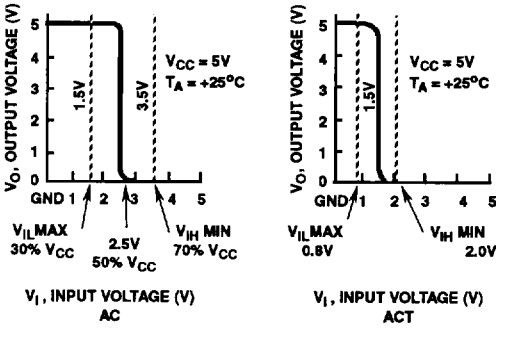


FIGURE 3. AC/ACT I/O SWITCHING CHARACTERISTIC FOR A NOMINAL V_{CC} OF 5V

Noise Immunity and Noise Margin

Table 2 shows the input noise immunity values (V_{IL}Max and V_{IH} Min) for AC and ACT devices, the output voltage specifications, and the calculated noise margins under two conditions: (1) interfacing with like members of the same family, and (2) interfacing with bipolar FAST types. The noise margins shown in Table 2A, for AC and ACT types only, apply for the temperature range of -55°C to +125°C. In Table 2B, the interface noise margins are limited to 0°C to +70°C, the commercial temperature range of FAST types. These tables illustrate one of the most important attributes of the CMOS AC/ACT family when compared to the FAST family; namely, designs that use the AC Series CMOS types have over three times the noise margin of the FAST family in the same design. Hence, new designs taking advantage of the higher speeds of these types should use the 1.4V noise margin of the AC family to gain the extra system noise margin of 1V.

Pulsed input noise immunity is illustrated in Figure 4. This figure shows the typical family DC noise immunity for input pulses having widths of 10ns or more. Below 10ns, the pulse amplitude (V_P) reaches higher values before an input is sufficiently disturbed to cause an output change. Note that for AC types, the values are for V_P amplitudes above ground or below V_{CC} (5V). For ACT types, only the limiting noise immunity above ground (0.8V DC) is shown. DC noise immunity below V_{CC} is 3V for ACT types and is not shown here because it is so high.

Input Current/Voltage Characteristic

The inputs of the AC/ACT devices have the dual-diode clamping circuit shown in Figure 5. This circuit serves two important needs: (1) Ringing voltages above V_{CC} and below ground caused by the RLC interface equivalent circuit are clamped to within one diode drop of V_{CC} and ground, thereby reducing EMI. (2) Electrostatic discharge (ESD) is shunted away from the gate oxide of input transistors. Between -0.5V and V_{CC} plus 0.5V (see Figure 6), the input current is typically under the ±1nA typical leakage of the biased input diodes. Beyond -0.5V and V_{CC} plus 0.5V, the diodes are forward biased and clamping action begins. The diodes can handle large junction currents (±400mA for under one second). For continuous clamping action over the operating temperature range, the aluminum input metallization traces are reliably sized for ±20mA, as shown in Figure 6. Note that it is the aluminum traces and not the diode junctions that are the limiting circuit elements.

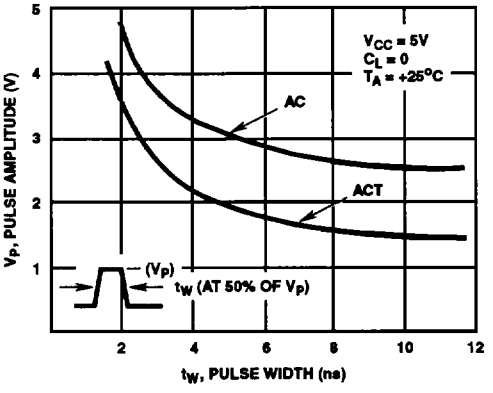


FIGURE 4. TYPICAL DYNAMIC NOISE IMMUNITY

TABLE 2A. NOISE IMMUNITY VALUES AND NOISE MARGIN FOR AC/ACT TYPES (V_{CC} = 5V)

PARAMETERS	SYMBOL	AC TYPES	ACT TYPES	UNITS
Maximum Low-Level Input Voltage	V_{IL} Max	1.5	0.8	V
Minimum High-Level Input Voltage	V_{IH} Max	3.5	2	V
Maximum Low-Level Output Voltage	V_{OL} Max	0.1	0.1	V
Minimum High-Level Output Voltage	V_{OH} Min	4.9	4.9	V
Noise Margin Low-Level	V_{NML}	1.4	0.7	V
Noise Margin High-Level	V_{NMH}	1.4	2.9	V

NOTE:

1. $V_{NML} = V_{IL}$ Max - V_{OL} Max
   $V_{NMH} = V_{OH}$ Min - V_{IH} Min

TABLE 2B. NOISE IMMUNITY VALUES AND NOISE MARGIN OF AC/ACT TYPES DRIVING FAST TYPES AND OF FAST TYPES DRIVING AC/ACT TYPES (V_{CC} = 4.5V)

PARAMETERS	SYMBOL	AC/ACT → FAST		FAST→ AC/ACT		UNITS
Maximum Low-Level Input Voltage	V_{IL} Max	-	0.8	-	0.8	V
Minimum High-Level Input Voltage	V_{IH} Min	-	2	-	2	V
Maximum Low-Level Output Voltage	V_{OL} Max	0.44	-	0.5	-	V
Minimum High-Level Output Voltage	V_{OH} Min	3.8	-	2.4	-	V
Noise Margin Low Level	V_{NML}	0.36		0.3		V
Noise Margin High Level	V_{NMH}	1.8		0.4		V

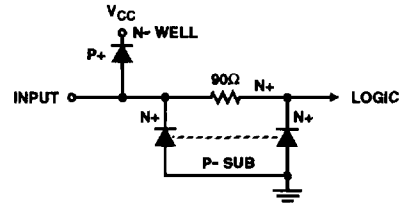


FIGURE 5. AC/ACT DUAL-DIODE INPUT PROTECTION NETWORK

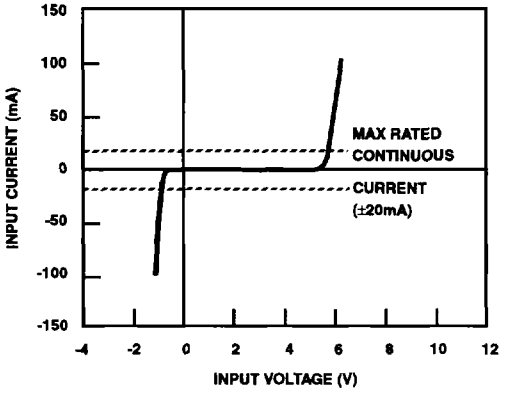


FIGURE 6. AC/ACT INPUT CHARACTERISTIC

Input Termination

The inputs of all AC/ACT types require termination. The input resistance of these types is very high, typically $10^9\Omega$, and the input capacitance is a few picofarads. When unterminated inputs are left floating, they can easily pick up stray charge and move the transistor into the linear operating voltage range between V_{IL} and V_{IH}. When this transfer takes place, logic malfunction could occur, oscillation may occur, and operating current goes up. Consequently, all unused CMOS inputs must be terminated. Terminations may be directly to V_{CC} or to ground or made by means of a shunt resistor. Specification information on Input Termination Design Rules is located on AnswerFAX, document number 7001, "System Design". See Section 8, "How to Use AnswerFAX" of this selection guide.

Input ESD Protection

As mentioned, AC/ACT device inputs have a resistor-diode protection network, shown in Figure 5, that protects the gate oxide from electrostatic discharge (ESD) damage. The network provides protection to levels greater than 2kV in all modes pertaining to the input, as shown in Figure 7. This 2kV figure was arrived at by the testing of devices in the ESD test circuit shown in Figure 8 while conforming to the MIL-STD test requirements. Despite the excellent built-in ESD protection, these device could be exposed to up to 15kV if good handling practice for semiconductor ICs is not followed. Please refer to AN6525 and ICE 402 for more detailed guidance. One special difference between the Harris AC/ACT logic family and older Harris CMOS families is the use of P substrates that are at ground potential (see Figure 1). The Harris CD4000B and HC/HCT families of logic devices use N-substrate material, which is at V_{CC} potential. Because of this difference, the bonding sequence for AC/ACT types is changed so that the ground pin is bonded first. The rule for N-substrate logic is to bond the V_{CC} or V_{DD} pad first.

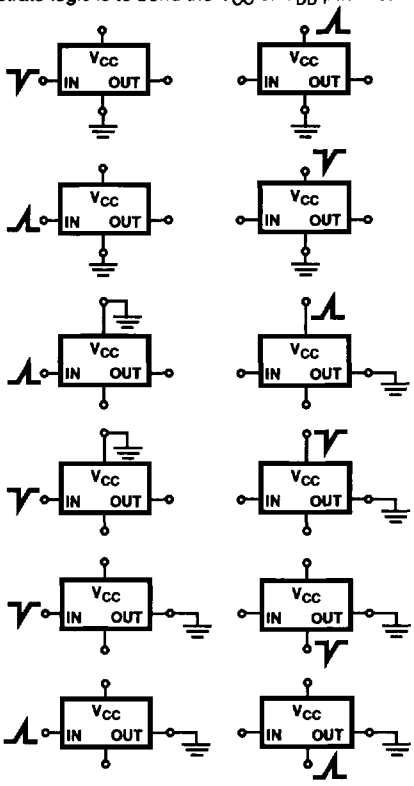
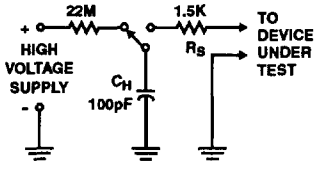


FIGURE 7. ELECTROSTATIC DISCHARGE (ESD) TEST MODES



C_H = HUMAN BODY CAPACITANCE TO GROUND
R_S = BODY SOURCE RESISTANCE

FIGURE 8. TEST CIRCUIT FOR MEASURING ELECTROSTATIC DISCHARGE (ESD) IN AC/ACT CIRCUITS. THE RISE TIME AT THE OUTPUT TERMINAL SHOULD BE 13ns ±2ns

Input Interaction

Another effect of the input protection network is the imposition of a parasitic transistor between adjacent input pins. Figure 9 shows this transistor. This parasitic transistor action may cause undesirable interaction between adjacent inputs

if the input level is less than ground. In AC/ACT devices, gain of the transistor (alpha = I_C/I_E) is minimized to less than 0.001, thereby permitting proper logic operation in the presence of large below ground transient voltages.

An application example in which the knowledge that alpha equals 0.001 is useful is shown in Figure 10. Here, if input A swings between -5V and +5V and the AC/ACT device is operated normally from 5V to ground, it is wanted that the output switch reliably between 0V and 5V. The designer must consider the V_{ILB} at the B input terminal. Calculations show that this is a safe design, because V_{ILB} = 4.3mV.

$I_E = 4.3V/20k\Omega = 0.215mA$
$I_C = \alpha I_E = 0.215\mu A$
$V_{ILB} = I_C \times 20k\Omega = 4.3mV$

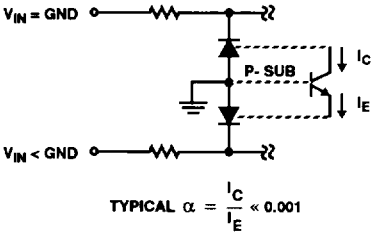


FIGURE 9. PARASITIC N-P-N TRANSISTOR BETWEEN ADJACENT PINS IMPOSED BY INPUT PROTECTION NETWORK

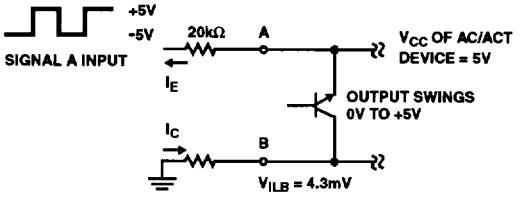


FIGURE 10. EXAMPLE OF USE OF INPUT INTERACTION (A) IN A LEVEL CONVERSION

Input Capacitance

The input capacitance C_I as a function of input voltage is shown in Figure 11 for typical AC and ACT types. Note that C_I has peak values at the respective input-voltage switch point of 1.5V for ACT and 2.5V for AC types. Capacitance on either side of the peak is a summation of package, lead-frame, reverse-biased input diode, and CMOS gate-to source/drain capacitance. The peak capacitance results from the Miller-effect multiplication of the gate-to-drain capacitance in the high-gain linear-transition region. The value of C_I, that most typically represents the average loading effect is 5.0pF for AC and ACT inputs.

Latch-Up Sensitivity

Latch-up is a state in which an unwanted low-impedance path develops in a parasitic four-stage bipolar structure in a CMOS IC. Latch-up may be initiated or triggered by voltage overshoot or undershoot at inputs, outputs, or supply terminals. A high transient voltage or current at any one terminal or at any combination of these terminals may initiate turn on of the parasitic SCR type four-layer diode bipolar device. See Figure 12A.

A simplified diagram of this parasitic structure is shown in Figure 12B. This structure, when triggered on, keeps the supply voltage below the V_{CC} voltage value and thus permits a high supply current of several hundred mA to flow (see IC in Figure 12B). The values of resistors R_P and R_N depend on the circuit layout geometry and on P+ and N+ doping levels. The lower the value of these resistors, the less the voltage drop that will occur and the higher the trigger current needed to induce turn on of the SCR structure.

Also important for minimizing latch-up problems are the established layout rules and process parameters that minimize the current gain (beta) of the parasitic N-P-N and P-N-P transistors shown in Figure 12.

The Harris AC/ACT n-well process uses a thin p-epitaxial layer on the P+ substrate. This layer provides a shunt of very low resistance around R_P. The effective R_P is extremely low, and as a result, very high negative voltage or current transients at the N+ source (V_{SS} point in Figure 12) are required to forward bias the parasitic N-P-N base-emitter junction. Additionally, there are several design rules that also significantly decrease latch-up probability. These rules relate to:

1. Layout spacings to reduce the parasitic N-P-N and P-N-P transistor current gain.
2. N+/N- well doping.
3. Closed structure outputs.
4. Latch plugs liberally used.

The current transient at any input or output terminal that could potentially trigger latch-up of AC/ACT ICs is typically more than ±400mA at +25°C. Measurements are made at all terminals to assure that they have a latch current of over ±100mA at +125°C. The absolute maximum DC rating in AC/ACT data sheets and in the industry JEDEC Standard Number 20A is ±20mA at inputs and ±50mA at outputs.

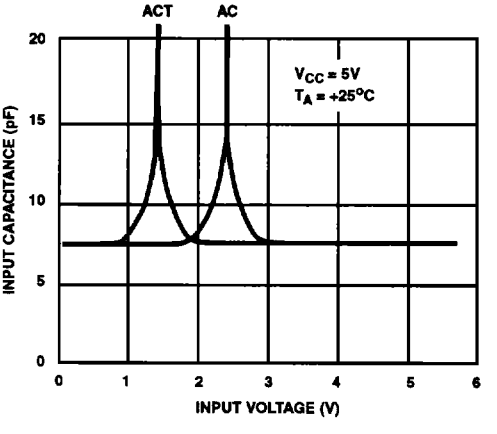


FIGURE 11. VARIATION OF INPUT CAPACITANCE WITH VOLTAGES FOR TYPICAL AC/ACT TYPES

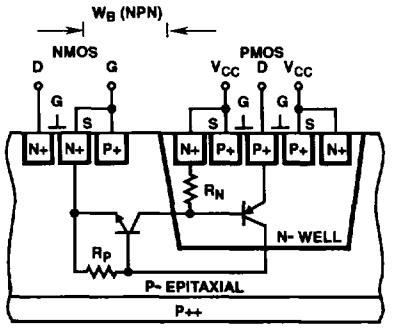


FIGURE 12A. CROSS SECTION OF CMOS STRUCTURE SHOWING SCR LATCH-UP PARASITIC TRANSISTORS

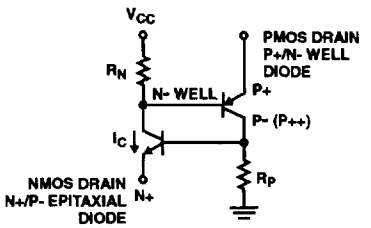


FIGURE 12B. SIMPLIFIED DIAGRAM OF CMOS FOUR-LAYER DIODE STRUCTURE

FIGURE 12.

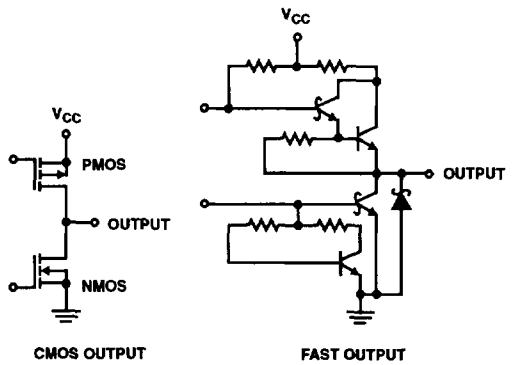


FIGURE 13. AC/ACT OUTPUT, A COMPLEMENTARY-SYMMETRY TRANSISTOR CONFIGURATION, COMPARED WITH FAST OUTPUT, A TOTEM-POLE CONFIGURATION

Output Characteristics

AC/ACT outputs make use of a complementary-symmetry transistor configuration that is different from the FAST totem-pole output. Both outputs are shown in Figure 13. AC/ACT outputs meet the voltage-level requirements necessary to interface AC/ACT inputs and the drive and current requirements needed to interface bipolar inputs such as TTL, LS, ALS, AS, FAST, and the like.

The outputs of all AC/ACT devices have the same drive current capability and meet proposed JEDEC standard drive and current requirements. The outputs may be active (two-state) or three-state in which both the PMOS and NMOS transistors are off.

Another type of AC/ACT output is the open-drain output of the AC/ACT 05 Hex Inverter shown in Figure 14. The AC/ACT 05 is the only advanced high speed CMOS inverter type having outputs that can be used for a "wired-OR" arrangement. There is, however, a very useful group of octal transceiver types having open-drain outputs. These types are listed below.

AC/ACT 647	Octal Bus Transceiver/Register with Open Drain (Non-Inverting)
AC/ACT 653	Octal Bus Transceiver/Register, Open Drain A Side, Three-State B Side (Inverting)
AC/ACT 654	Octal Bus Transceiver/Register, Open Drain A Side, Three-State B Side (Non-Inverting)
AC/ACT 7623	Octal Bus Transceiver; Three-State B Side, Open Drain A Side (Non-Inverting)

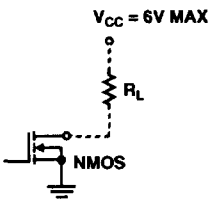


FIGURE 14. AC/ACT HEX INVERTER (05) OPEN-DRAIN OUTPUT CIRCUIT

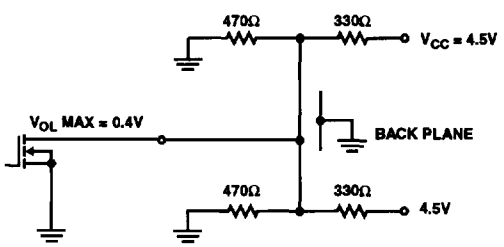


FIGURE 15A. OPEN-DRAIN OUTPUT AC/ACT TYPES EFFECTIVELY DRIVE VME

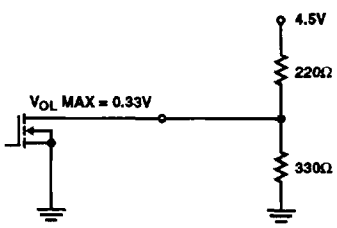


FIGURE 15B OPEN DRAIN AC/ACT TYPES EFFECTIVELY DRIVE SCSI BACKPLANE TERMINATION SCHEMES

FIGURE 15.

These types are especially useful for "wired-OR" -ing of interrupt signals on a backplane. They could also be used for backplane interface using the backplane termination resistors as pull-ups. Figure 15 illustrates two popular backplane termination schemes (VME and SCSI) that are effectively driven with AC/ACT open-drain outputs. In Figure 15A, the dual VME termination scheme is driven, V_{OL} Max is 0.40V at +85°C, and V_{CC} is 4.5V. In Figure 15B, the SCSI termination is driven. In this network, V_{OL} Max is 0.33V. In both examples, the bus pulls up to 2.6V for a V_{OH} Min by means of the resistive terminations. AC/ACT types having three-state outputs may also reliably drive the VME and SCSI termination of Figure 15. With active PMOS pull-ups, the low to high transition of the bus is faster than with the open-drain output interface. See the section on the FCT Bus Interface Family that describes output drives of 64mA and 48mA, required in many backplane applications.

Output ESD Protection

The outputs in AC/ACT devices are protected from electrostatic discharge (ESD) damage by an integral inherent diode structure. Figure 16 shows these diodes. These protective diodes are effective because of the large geometries (widths) of the output transistors. The diodes are comprised of the drain and the n-substrate junction of the p-device and of the drain and the p-well junction of the n-device. This network provides protection to voltage levels greater than 2kV in all electrostatic discharge modes pertaining to the output (for these modes, see Figure 7).

The output clamp diode to V_{CC} must be taken into account in interface and bus applications. For more information on this subject, see AnswerFAX document number 7001, "System Design". See Section 8, "How to Use AnswerFAX" of this selection guide.

Output Current

AC/ACT outputs are specified for both CMOS and bipolar FAST loads. CMOS inputs are voltage sensitive, and the only current is leakage current. The output voltage test for CMOS interfacing is specified for I_O at ±50µA (50 CMOS loads). The outputs are also specified for I_O at ±24mA (15 FAST loads). The corresponding V_{OL} Max and V_{OH} Min for the outputs are given in Table 3.

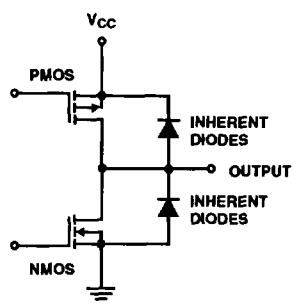


FIGURE 16. INHERENT DIODE STRUCTURE THAT PROTECTS AC/ACT OUTPUTS FROM ELECTROSTATIC DISCHARGE DAMAGE TO LEVELS GREATER THAN 2kV

For output loading of ±50µA, the typical output voltage is only 60mV below V_{CC} or 60mV above ground. As a consequence, CMOS outputs are truly rail-to-rail swings even at 50µA, which is important in many applications. The reason that the guaranteed limits of JEDEC and Table 3 are at 100mV is to facilitate high speed test verification.

Note that for the AC-Series types, operation down to 1.5V is specified. Output current is specified at 1.5V and also at 3V. This worst-case 3V rating is increasingly important because it corresponds to the new low-voltage logic standard (JEDEC Std. No. 8) of 3.3V ± 0.3V. As CMOS technology shrinks to under one micron, reliability, operating power, and most of all, switching noise all point toward more favorable results with a supply voltage of 3.3V than with 5V ones. At 3.3V, AC/ACT types consume only 40% of the operating power of 5V operation, and switching speed is decreased by an average of only 30%. Also, TTL interface is realizable at 3.3V ± 0.3V using AC types.

The maximum current per output pin (I_O) is ±50mA. This maximum current rating is specified when the outputs (V_O) are in their active regions, that is, greater than ±0.5V but less than V_{CC} plus 0.5V. The maximum current rating per power pin, V_{CC} or ground is ±100mA for up to four outputs; for each additional output the rating is increased by ±25mA. When the output voltage exceeds V_{CC} by more than 500mV or is below ground by more than 500mV, the output protection diodes turn on and conduct current. To avoid latch-up, the peak values of the diode current I_{OK} should not exceed ±400mA, as described earlier.

An important contributor to the control of output ringing and electromagnetic interference (EMI) is an output stage design having slow enough output slew rates to allow clamp diode turn-on (about 1ns). This turn-on attenuates ringing that often tries to exceed V_{CC} +0.7V or go more than 0.7V below ground. Control of output slew rates is also a central contributor to reduced output simultaneous switching transients (discussed later).

Output-Current Interfacing Capability

A comparison of the output drive capabilities of AC/ACT types and FAST types follows.

FAST capability is expressed in unit loads (ULs) where the load is specified to be an input of the same family. This specification assures that the worst-case low-input and high-input thresholds will be met and the existing margins of noise immunity preserved.

AC/ACT capability is expressed as source/sink current at a specified output voltage. Because AC/ACT types require virtually no input current, the unit-load concept does not apply.

With a specified output sink current drive of 24mA at 0.44V (at 85°C), each AC/ACT output can drive 24,000 AC/ACT inputs. With a 50µA/0.1V specification, each AC/ACT output can drive 480 AC/ACT inputs. Each AC/ACT output has a drive capability of 15 FAST loads and maintains a V_{OL} under 0.5V over the full temperature range.

The standardized Harris and the JEDEC output characteristics are shown in Table 3.

Output Curves

In Figure 17 and Figure 18 the standardized family output characteristic plots are provided. Both typical and worst-case minimum curves plot the I_{OL} (sink) and I_{OH} (source) current as a function of drain-to-source output transistor voltage drop (V_{DS}). The heavy line at 50mA is the boundary between safe, continuous operating regions of current drain and areas where only transients are permitted.

Output Short-Circuit Current (Backdriving)

Note that in Figure 17 short-circuit currents of ±200mA are typical for AC/ACT outputs at a V_{CC} of 5V. Backdriving these outputs during PC board test by forcing outputs to ground, for example, is permissible with the limitations that only one output per IC be backdriven at any one time and for only one second maximum. For durations longer than one second, the IC may become too hot. Fortunately, because the epitaxial-based process is essentially latch-free, no danger of latch-up results from backdriving.

Output Simultaneous Switching Transients

From Figure 17, it is evident that very large switching transients can be absorbed by AC/ACT output transistors. Figure 19 illustrates how large transient currents are typically generated for the charge or discharge of an AC/ACT output using a 50pF load and a V_{CC} of 5V. The discharge time through the n-device of the output transistor is typically 3ns, even though the capacitor discharge current is typically 83mA, as shown in the following calculation.

$$I_C = C\,(dv/dt) = 50pF\,(5V/3ns) = 83mA \qquad \text{(EQ. 1)}$$

The ON resistance of the p and n channels is 10Ω or more each during peak switching transient periods. Thus, it is possible that switching currents of ±200mA per output may occur. For octal types, where bytes are simultaneously switched at common edges, the total peak switching current could approach 8 x 200mA or 1.6 amperes. In practice. however, the actual current is lower because it spreads somewhat as a result of the deviations in peak switching times. These currents cause device V_{CC} and ground bus voltage drops that vary with each output and hence cause different output delays. These delta delays spread the switching current over 1ns to 2ns.

TABLE 3. STANDARD HARRIS AND JEDEC OUTPUT CHARACTERISTICS AC SERIES

					T_A, AMBIENT TEMPERATURE (°C)						
		TEST CONDITIONS		V_{CC}	+25°C		-40°C TO +85°C		-55°C TO +125°C		
PARAMETERS	SYMBOL	V_I (V)	I_O (mA)	(V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05 (Note 4)	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24 (Note 4)	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Notes 1, 2, 4)	5.5	-	-	3.85	-	-	-	V
			-50 (Notes 1, 2, 4)	5.5	-	-	-	-	3.85	-	V
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05 (Note 4)	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24 (Note 4)	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Notes 1, 2, 4)	5.5	-	-	-	1.65	-	-	V
			50 (Notes 1, 2, 4)	5.5	-	-	-	-	-	1.65	V

NOTES:

1. Test one output at a time for a 1s maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
2. Test verifies a minimum 50Ω transmission-line-drive capability at +85°C, 75Ω at +125°C.
3. Specifications at 1.5V are not part of the JEDEC proposal.
4. For ACT Series, specifications only at V_{CC} = 4.5V and 5.5V apply.

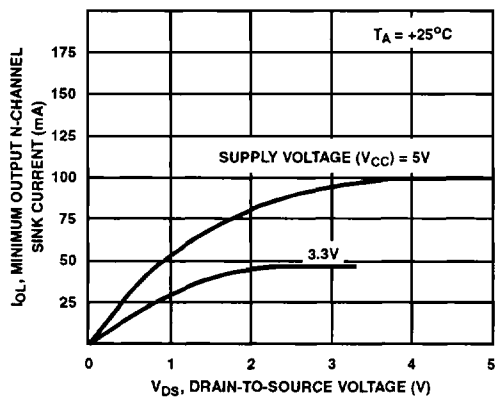


FIGURE 17A.

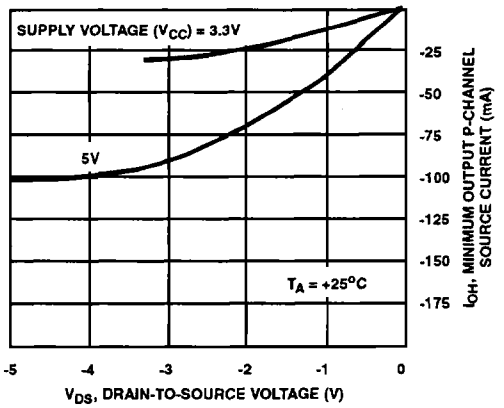


FIGURE 17B.

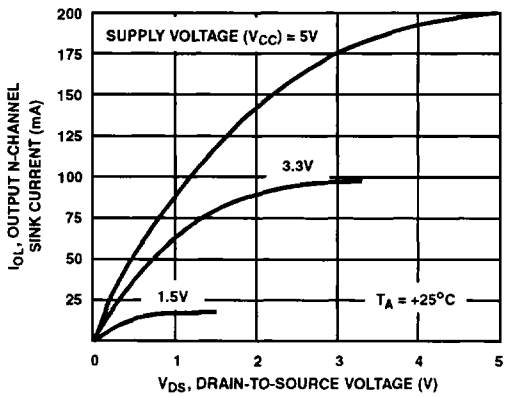


FIGURE 17C.

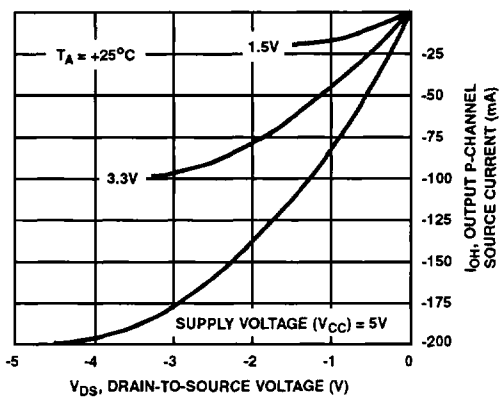


FIGURE 17D.

FIGURE 17. MINIMUM AND TYPICAL OUTPUT CHARACTERISTICS AT +25°C FOR AC/ACT ADVANCED HIGH SPEED CMOS TYPES

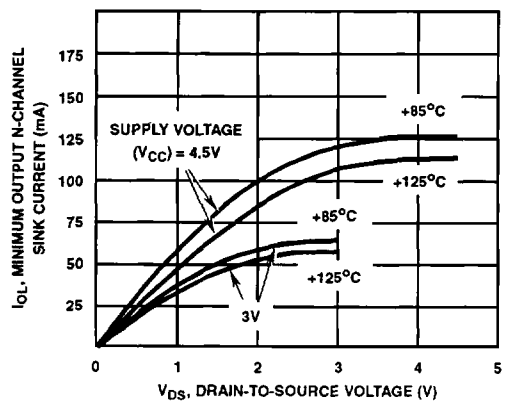


FIGURE 18A.

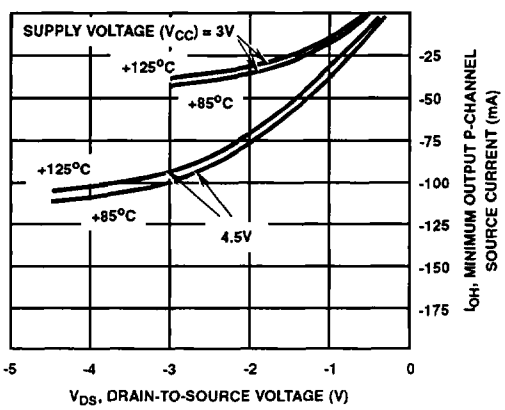


FIGURE 18B.

FIGURE 18. MINIMUM OUTPUT CHARACTERISTIC CURVES AT +85°C AND +125°C FQR AC/ACT ADVANCED HIGH SPEED CMOS TYPES

Figure 20 shows that four inductances contribute to the on-chip ground potential V_G. These inductances are L1 effective on-chip ground path inductance; L2, the chip bondpad/wire/lead-frame inductance; L3, the IC lead inductance; and L4, the printed-circuit board inductance path to earth or reference ground. Figure 21 illustrates the lifting of ground as a result of the inductances L1 though L4 when an AC/ACT device switches. Instantaneously, the chip sees V_G as ground and causes the following IC performance effects.

1. If N outputs switch and one output is a steady-state low, the V_G will reflect onto the unswitched output as the peak low-level output voltage V_{OLP}, as shown in Figure 22B for an eight-output device.
2. The instantaneous gate-to-source voltage decreases by a magnitude of V_G volts. This decrease reduces the transistor g_m, raises the R_{ON}, and increases the transition time of the output stage and the delay time.
3. Input noise immunity is instantaneously decreased by V_G volts, and as a result, internally stored data in latches or flip-flops could be upset.

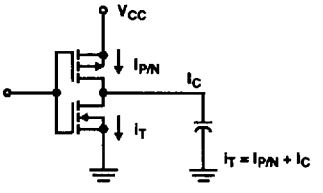


FIGURE 19. GENERATION OF LARGE TRANSIENT CURRENTS FOR CHARGE OR DISCHARGE OF AN AC/ACT OUTPUT. LOAD = 50pF; V_{CC} = 5V

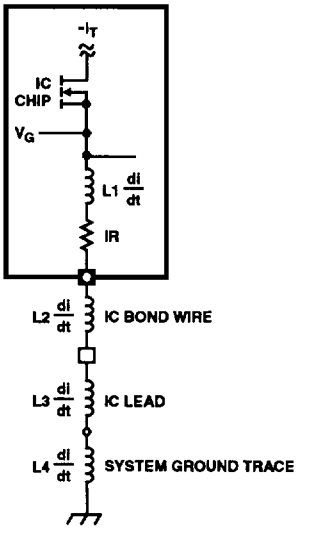


FIGURE 20. IC GOUND PATH AND FOUR CONTRIBUTING INDUCTANCES

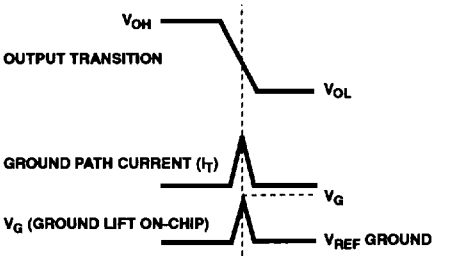


FIGURE 21. GROUND LIFT CAUSED BY SWITCHING CURRENT TRANSIENTS THROUGH INDUCTANCES DESCRIBED IN FIGURE 20

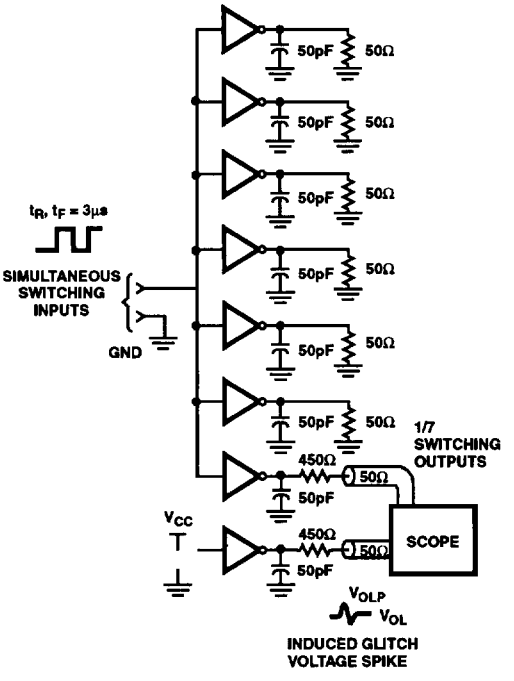


FIGURE 22A. TEST CIRCUIT OF SIMULTANEOUS SWITCHING TRANSIENT

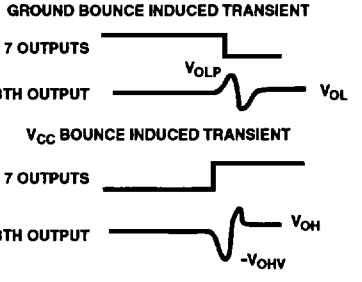


FIGURE 22B. WAVEFORM OF SIMULTANEOUS SWITCHING TRANSIENT

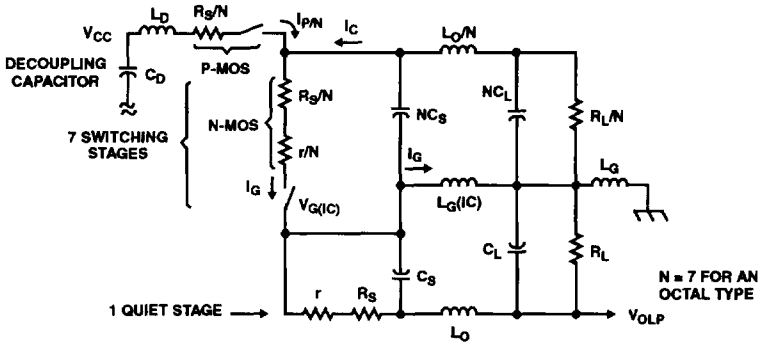


FIGURE 23. EQUIVALENT CIRCUIT OF GROUND-BOUNCE CONFIGURATION FOR AN OCTAL OUTPUT STAGE. DYNAMIC VALUE OF R_S AND TRANSISTOR SWITCH TIMING ARE KEY VARIABLES IN MINIMIZING GROUND BOUNCE (V_{OLP})

Figure 23 shows the equivalent IC circuit for the octal-type ground-bounce test configuration. Although this circuit shows the several RLC components involved in the development of both the transient ground lift (V_G) and the resultant quiet output voltage bounce (V_{OLP}), some key variables that complicate analysis are not readily apparent. These variables include:

1. Design of transistors to increase effective R_S, which will increase turn-on time or output slew rate dv/dt. The actual value of R_S is about 15Ω.
2. Design of chip to equalize the on-chip L and R of all eight output-stage metal runs to ground.
3. Design of the plastic package lead-frame to reduce the ground pin inductance L_G by one half. For the DIP package this inductance is 7.5nH.
4. Design of small break-before-make capability to reduce $I_{P/N}$ through current. Time difference is a nominal 0.5ns.
5. Design of transistor turn-on time of a nominal 0.75ns.

Of these five variables, the vast majority of ground-bounce minimization is achieved by control of the output dv/dt. It is of so little benefit to change the position of the ground pin or add additional ground pins that users get excellent performance and minimization of ground bounce and EMI without incurring significant extra cost and the reduced reliability of bigger packages that would result from such changes.

Sample Measurement of V_{OLP}

Figure 24 shows actual sample measurement values of the peak low-level output voltage V_{OLP} measured on an ACT240, an Octal-Buffer Line Driver, three-state device. The worst-case V_{OLP}, 1.06V, occurs at pin 18, which is furthest from pin 10 ground. The best-case V_{OLP}, 0.720V, occurs at pin 9, closest to pin 10. Waveforms for the ACT240 in the dual-in-line package (DIP) are given in Figure 25 and in the small outline package (SOP) in Figure 26. These waveforms are measured at pin 18, the worst-case pin. All Harris octals now have controlled output edge rates with ground-bounce performance similar to that shown in Figure 25 and Figure 26.

This performance is very reasonable for a buffer having a typical delay of 3.5ns. Harris advanced high speed CMOS octal logic devices have been designed to minimize the effective on-chip L1 (Figure 20) and also to minimize L2, the dual bond-wire inductance. L3 is the inductance of a "corner-pin" dual-in-line (DIP) or small outline (SOP) package, and L4 is the inductance of the fixture ground-return path. This last value must be kept small (see next section on V_{OLP} Measurement Method). For comparison, a bipolar FAST F240 type was identically measured. Its V_{OLP} is nearly identical, the worst-case value being 1.05V.

Type: AC240
Worst-Case Value.....1.06V
Best-Case Value..... 0.72V DIP
Worst-Case Value..... 0.75V SOP

Type: FAST F240
Worst-Case Value.....1.05V

FIGURE 24. MEASURED VALUES OF V_{OLP} MADE ON A 240 OCTAL BUFFER LINE DRIVER, THREE-STATE DEVICE

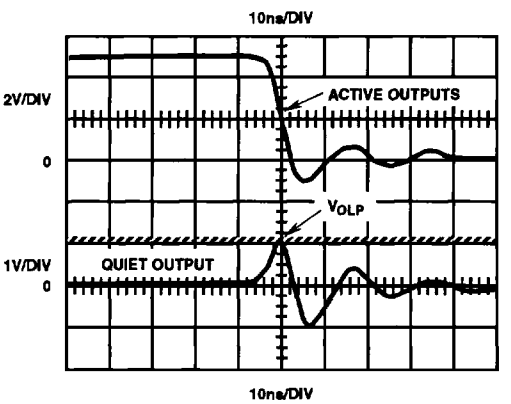


FIGURE 25. SIMULTANEOUS SWITCHING TRANSIENT PERFORMANCE OF AN AC240 OCTAL-TYPE IC IN A DUAL-IN-LINE (DIP) PACKAGE. SEE FIGURE 22 FOR TEST CONDITIONS

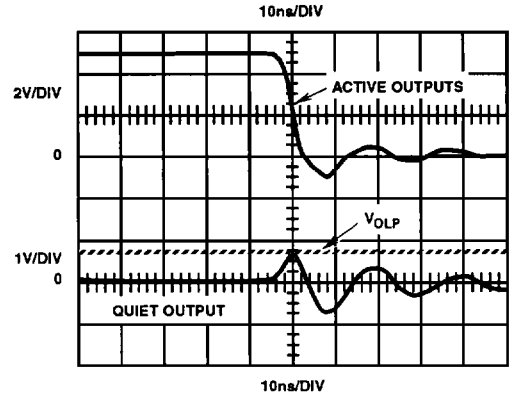


FIGURE 26. SIMULTANEOUS SWITCHING TRANSIENT PERFORMANCE OF AN AC240 OCTAL-TYPE IC IN A SMALL-OUTLINE (SOP) PACKAGE. SEE FIGURE 22 FOR TEST CONDITIONS

V_{OLP} Measurement Method

The method for measuring V_{OLP}, also referred to as the simultaneous switching transient or ground-bounce effect, is a radio-frequency-type measurement and requires a good rf quality test fixture. A schematic of the fixture is given in Figure 22A. It utilizes seven outputs switching into a standard AC/ACT load, considered to be a worst-case condition. The eighth input is held low or high, thereby placing the output in a high or low state. The eighth output is monitored with a scope, and the peak amplitude of the positive transient (V_{OLP}) above V_{OL} is measured. The peak amplitude of the negative transient below V_{OH} is V_{OHV} Figure 22B shows the waveforms of the ground-bounce-induced transients, both positive and negative.

The major concern of the design engineer in making these measurements is the V_{OLP}. Tolerance of this unwanted noise voltage is highly dependent on the switching threshold and noise margin of the logic circuits connected to the outputs of the device. With the CMOS switching threshold, which is typically 50% of V_{CC}, the energy of the transient pulse is usually insufficient to cause false switching. More critical is when the logic inputs connected to the device switch at TTL thresholds, typically 1.5V.

Dynamic Characteristics

Switching Speed

Significant speed improvement distinguishes the new AC/ACT Advanced High Speed CMOS Logic Family from the HC/HCT High Speed CMOS Logic Family. Table 4 positions each CMOS logic family with the speed-equivalent TTL family. From the standpoint of speed, the AC/ACT family substitutes very adequately for the TTL FAST, AS, and S families. It is not recommended, however, to directly substitute AC/ACT, FAST, AS, S, or ALS logic for HC/HCT or LSTTL logic because of the three times faster switching edges of the former group compared to the latter. These faster families require transmission-line interconnect considerations, terminations, superior decoupling, and careful PC board layout to keep switching noise generation under control so that FCC emission specifications may be met with good margin.

TABLE 4. GUIDE FOR SUBSTITUTING CMOS LOGIC FAMILY TYPES FOR TTL FAMILIES

CMOS LOGIC FAMILY	TTL FAMILY					
	TTL	LSTTL	ALS	S	FAST	AS
HC/HCT	X	X	X (Note 1)	-	-	-
AC/ACT	(Note 2)	(Note 2)	X (Note 2)	X	X	X

NOTES:

1. HC/HCT substitutes when ALS is used vs LS for lower power. AC/ACT substitutes when ALS is used vs LS for higher speed.
2. There is too large a difference in speed and noise/EMI generation for AC/ACT to reliably substitute for TTL, LSTTL, or HC/HCT.

Propagation Delays

The useful speed of a logic family is essentially the I/O propagation delay of both low-to-high and high-to-low signal transitions from input to output.

Table 5 provides a comparison of AC and bipolar FAST device propagation delays for three familiar logic types; namely, a NAND gate (00), a flip-flop (74), and an octal buffer (240). Also shown is the input clock rate. For 74-series devices, the delays and also the clock rate are very nearly the same, not withstanding that for AC types V_{CC} is 4.5V and T_A is +85°C and for FAST types V_{CC} is 4.75V and T_A is +70°C. These test conditions are clearly in favor of FAST by about 5%. Also evident from the data sheet extractions in Table 5 are the balanced delay of AC types and the unbalanced (t_{PLH} vs t_{PHL}) delay of the bipolar types.

TABLE 5. COMPARISON OF SWITCHING SPEED FOR THREE 74-SERIES AC AND FAST LOGIC FUNCTIONS

PRODUCT	PARAMETER	AC	FAST	UNIT
Two-Input NAND (00)	t_{PLH}/t_{PHL}	6.2	6/5.3	ns
Flip-Flop (74)	t_{PLH}/t_{PHL}	9	7.8/9.2	ns
	f_{MAX}	125	100	MHz
Buffer (240)	t_{PLH}/t_{PHL}	6.5	8/5.7	ns

Useful delay is only as good as the worst or slowest delay mode or path. For the entire AC/ACT family covering over 50 different logic functions, the speed comparison illustrated in Table 5 holds up within a window of plus or minus a few nanoseconds. There are, however, a few exceptions going in both directions. Where speed right up to the limit of the device capability is a critical design element, the designer should precisely use published data sheet limits for either AC/ACT or FAST types. Table 6A lists three ACT types in which two extra buffer stages are designed in to reduce the incremental change in I_{CC} caused by switching of the input state at 1.5V instead of 2.5V, the optimum value for CMOS devices.

As shown in Table 6B, the 6ns delay of the AC04 Hex Inverter type matches the delay of FAST types. The two extra ACT buffer stages, however, extend the delay limit to 8.8ns. These three SSI types are the only ones having extra ACT stages, and hence, their delay limits are a few nanoseconds slower than those of their AC or FAST counterparts.

TABLE 6A. DEVICES HAVING EXTRA STAGES FOR REDUCING POWER CONSUMPTION

TYPE	NUMBER OF LOGIC STAGES	
	AC	ACT
04/05 Hex Inverter	3	5
00 Quad Two-Input NAND	3	5
86 Quad Two-Input Exclusive-OR	4	5

TABLE 6B. PROPAGATION DELAY AND ΔI_{CC} VALUES FOR HEX INVERTER TYPE 04

PARAMETER	AC	ACT	FAST	UNIT
t_{PLH}/t_{PHL}	6/6	8.8/8.8	6/5.3	ns
ΔI_{CC} per Input	-	0.5 (Note 1)	-	mA

NOTE:

1. For three stages instead of five this value would be about 3mA per input.

Data sheets give a finite number of specified values of switching speed at specific test conditions. The system design engineer, however, often needs to know speed limits at other conditions. For example, the propagation delay of a 74 dual D-type flip-flop clock to $Q/\overline{Q}$ is specified as:

t_{PLH}, t_{PHL} = 9.1ns Max, V_{CC} = 4.5V, T_A = +85°C
= 2.65ns Min, V_{CC} = 5.5V, T_A = -40°C

There are two dichotomies: (1) The PCB V_{CC} value is fixed at a given time, probably close to 5.0V, and (2) the temperature is fixed at a given time, probably close to 55°C. Thus, the 9.1ns to 2.65ns spread, shown above, is unrealistically large. To ease this problem, Figure 27 is provided. Using this set of normalized delay curves, the system designer can easily narrow the Min/Max delay for use in estimating system timing. For the 74 dual D-type flip-flop if operation is assumed at V_{CC} = 5.0V, and T_A = 55°C, the Min/Max delay spread is narrower.

t_{PLH}, t_{PHL} = 8.3ns Max
= 3.6ns Min

Use of Figure 27 is as follows:

1. Select the maximum delay from the device data sheet for V_{CC} = 4.5V, T_A = +125°C. Call this value X.
2. Multiply X by the normalized multiplier fractions of X shown on the vertical axis for a given value of V_{CC} and temperature.

Each AC/ACT data sheet now contains speed limits at two temperature ranges for commercial/industrial plastic packaged product. These ranges are -40°C to +85°C and -55°C to +125°C. The latter temperature range limits are also applicable to MIL product packaged in ceramic packages. Historically, commercial TTL logic types use a limited temperature range for plastic (74 series) of 0°C to +70°C. To readily determine Harris AC/ACT speed for 0°C to 70°C operation, the following multipliers (from Figure 27) are used:

Max Limit = 0.855 X, T_A = 70°C, V_{CC} = 4.75V
Min Limit = 0.25 X, T_A = 0°C, V_{CC} = 5.25V

Where X is the Max Data Sheet limit for T_A = +125°C, V_{CC} = 4.5V.

Also shown in Figure 27 is the typical curve of speed vs temperature for V_{CC} = 5V. The exact value at T_A = +25°C is 0.487 X.

Propagation Delay Performance Curves

Figure 28 shows the typical normalized propagation delay as a function of capacitance loading at supply voltages of 1.5V, 3.3V, and 5V. The reference load is 50pF, the rated value given in the device data sheet. Figure 29 shows the typical normalized propagation delay as a function of supply voltage. This curve shows that AC-Series types are typically 30% slower at 3.3V than at the referenced 5V. At a supply voltage of 1.5V, the speed is four times slower compared to the speed at 5V but still is quite fast. In Figure 30, the normalized AC/ACT propagation delay variation with chip operating ambient temperature is given for operation at 1.5V, 3.3V, and 5V. From the 5V curve, it can be concluded that AC/ACT types slow down by 0.3% per °C, a useful number to have available for reference.

Behavioral Models

Behavioral models for Harris AC/ACT types are available from Logic Automation, Inc. These models contain the Min/Max speed limits specified in the Harris data sheets. See AnswerFAX document 7002, "Behavioral Models". See Section 8, "How to Use AnswerFAX" of this selection guide.

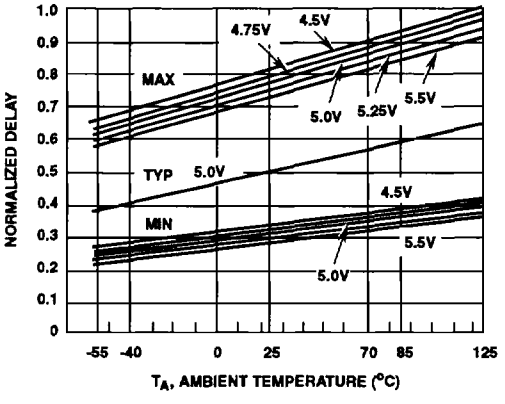


FIGURE 27. NORMALIZED AC/ACT MIN/MAX DELAY AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE

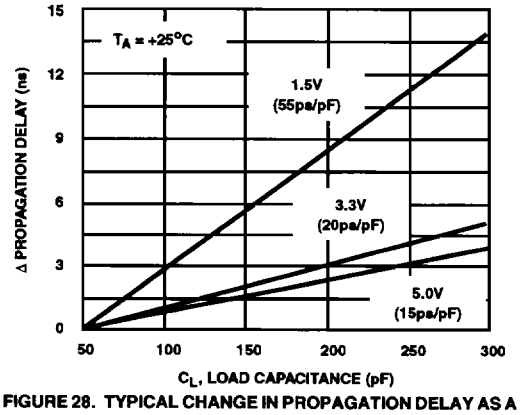


FIGURE 28. TYPICAL CHANGE IN PROPAGATION DELAY AS A FUNCTION OF LOAD CAPACITANCE FOR AC/ACT TYPES

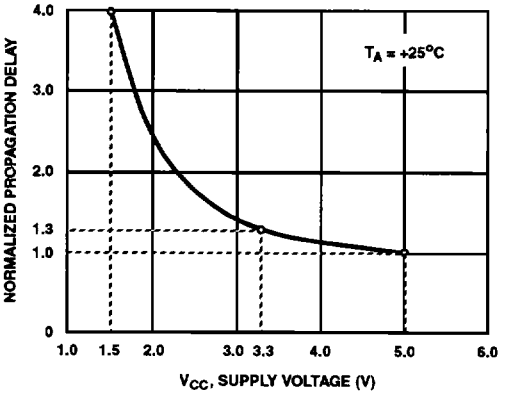


FIGURE 29. NORMALIZED PROPAGATION DELAY AS A FUNCTION OF SUPPLY VOLTAGE FOR AC TYPES

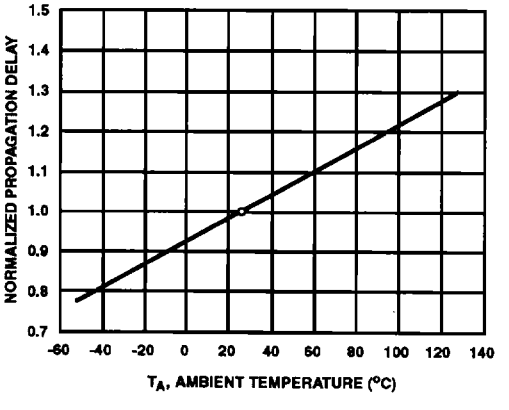


FIGURE 30. NORMALIZED PROPAGATION DELAY AS A FUNCTION OF AMBIENT TEMPERATURE FOR AC/ACT TYPES

Output Edge Rates/Transition Times

The typical propagation delay of an AC/ACT gate or buffer is 3.5ns (at V_{CC} = 5V, T_A = +25°C, C_L = 50pF), and the high speed of all AC/ACT types necessitates quick and predictable output transition times. Typical AC/ACT output transition times are shown in Table 7. Note that octal types have longer output transition times so as to reduce simultaneous switching transients and ringing.

TABLE 7. TYPICAL OUTPUT TRANSITION TIME (t_{TLH}, t_{THL}). MEASURED BETWEEN THE 10% AND 90% TRANSITION POINTS. T_A = +25°C

C_L (pF)	V_{CC} (V)	TYPICAL t_{THL}, t_{TLH} (ns)	
		LOGIC	OCTAL
50	1.5	8	10
	3.3	3	4
	5	2.5	3.3
150	1.5	20	26
	3.3	8	10
	5	6	8
300	1.5	35	46
	3.3	11	15
	5	10	13

Fortunately, unlike bipolar FAST logic, the design engineer may insert series resistors (R_S) in the output circuit, as shown in Figure 31, to reduce the spectral content, dampen ringing, and act as a series terminator. Propagation delay, however, will increase as a result of the series resistor and the associated total shunt capacitance C_S. For CMOS loads, an R_S, even up to several kΩ in value, will not affect input switching because the input resistance (R_I) is greater than 1000MΩ. For bipolar FAST devices, however, adding a series resistor results in increased values of V_{IL} because I_{IL} is 1.6mA. Hence, 100Ω is probably the maximum value for R_S with FAST ICs. This topic is covered in more detail in AnswerFAX document number 7001, "System Design". See Section 8 "How to Use AnswerFAX" of this selection guide.

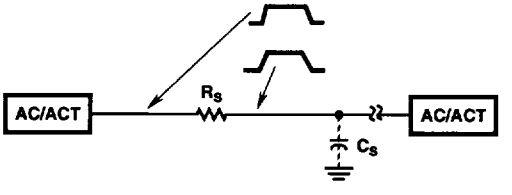


FIGURE 31. USE OF SERIES TERMINATION RESISTOR TO INCREASE OUTPUT EDGE RATES

Three-State Ratings and Test Conditions

AC/ACT logic types that have three-state output stage design also have the necessary three-state propagation delay parameters that are uniquely tested to optimize AC/ACT performance. Figure 32A shows an 85°C equivalent ac test circuit for all propagation delay parameters. The three "Thevininized" loads show the load board configuration for testing the six applicable delay parameters. In Figure 32B,

the active-to-high-impedance test waveforms are shown. Take particular notice of the RC symmetry for t_{PLZ} and t_{PHZ}, which is specially suited to CMOS rail-to-rail outputs with switching at 50% of V_{CC} (AC family). Also, note that the test switch point is at 20% of the rail - not 10%. The reason for this increase is that 10% of 4.5V would leave practically no room for the test set comparator because the 250Ω load pulls rails close to 10% of 4.5V.

There are two factors that must be highlighted:

1. The t_{PHZ} test load is different from the FAST test load. For FAST, R is 500Ω for t_{PHZ} and 250Ω for t_{PLZ}. These test loads are very satisfactory for the bipolar totem-pole output offset to 1.5V for V_S and a limited swing of 3V to 4V, but the unbalanced loads are unsatisfactory for AC/ACT outputs.
2. FAST test points are at 10% of the output swing, not 20%. Because of this difference, AC/ACT t_{PHZ} and t_{PLZ} parameters are specified a few nanoseconds larger than for FAST types. This change gives the appearance that AC/ACT types are slower than FAST types, but in actual operation, they are very comparable.

Incremental Propagation Delay Caused by Simultaneous Switching

Table 8 illustrates the effects of ground and V_{CC} "bounce" resulting from the simultaneous switching of eight Octal Buffer outputs. Note that the incremental delay added to t_{PHL} is less than that added to t_{PLH}. The reason for this difference is that the Harris chip design and the design of the bond-pad-to-lead frame are geared heavily to reducing the very critical ground loop inductance because of the 0.8V V_{IL} of ACT and FAST inputs. On the high side, where V_{IH} is 2V and the loaded V_{OH} is 3.8V, the V_{CC} bounce is not so critical. Also shown in Table 8 is the shift in skew due to V_{CC} and ground-bounce effects. The cause of these effects is described earlier in this Manual starting under the heading Output Simultaneous Switching Transients.

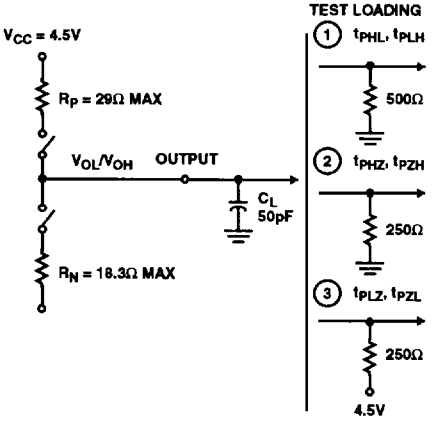


FIGURE 32A. AC/ACT THREE-STATE TEST CIRCUIT. OUTPUT STAGE AND THE THREE JEDEC AND HARRIS TEST LOAD CIRCUITS, T_A = +85°C

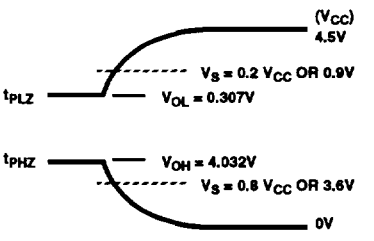


FIGURE 32B. THREE-STATE OUTPUT WAVEFORMS AND TEST POINTS. THE RC TIME CONSTANT IS A BALANCED 250Ω AND 50pF

FIGURE 32.

TABLE 8. INCREMENTAL PROPAGATION DELAY OF AN AC244 OCTAL NON-INVERTING BUFFER TYPE

TEST CONDITIONS V_{CC} = 5V; C_L = 50pF; T_A = +25°C	NUMBER OF OUTPUTS SWITCHING 1 (BEST)	8 (WORST)
Buffer Measured Input Pin	2	2 (Note 1)
Output Pin	18	18
Data (ns)		
t_{PLH}	4.9	6.41
t_{PHL}	4.88	6.04
Incremental Delay (ns) Referred To One Buffer Switching		
t_{PLH}	0	+1.51
t_{PHL}	0	+1.16
Skew Of t_{PHL}/t_{PLH} Ratio	0.996	0.942

NOTE:

1. Two synchronized pulse generators are used to maintain input pulse-edge integrity for precise measurement fidelity. Generator 1 is used for driving only the measured buffer. Generator 2 is used for driving the other buffers.

Clock Pulse Considerations

All AC/ACT flip-flops and counters contain master-slave devices having level-sensitive clock inputs. As the voltage at the clock input reaches the threshold level of the device, data in the master (input) section is transferred to the slave (output) section. The use of threshold levels for clocking is an improvement over ac-coupled clock inputs. These levels, however, make these devices somewhat sensitive to clock edge rates. The threshold level is typically 50% of V_{CC} for AC devices, and 30% of V_{CC} for ACT devices (1.5V at V_{CC} = 5V). Temperature has little effect on the clock threshold levels.

When clocking occurs, the internal gates and output circuits of the device dump current to ground, as previously mentioned. This condition results in a noise transient that is equal to the algebraic sum of internal and external ground-plane noise. When a number of loaded outputs change at the same time, it is possible for the chip ground reference level (and, therefore, the clock reference level) to rise by as much as 1V. If the clock input of a positive-edge-triggered

device is at or near its threshold during a noise-transient period, multiple triggering can occur. To prevent this condition, the rise and fall slew rates of the clock inputs should be limited to the maximum ratings specified on the data sheet for the AC/ACT type. The AC/ACT 14 Hex Schmitt Trigger type is recommended for sharpening up slow transitions. Under the heading Power Consumption, the family rating for input rise and fall time is provided, and this topic is further expanded.

Maximum permissible input-clock frequency ratings on the data sheet for each clocked device require an input clock having a 50% duty cycle. At these rated frequencies, the outputs will swing rail to rail, assuming no DC load on the outputs. This feature provides a very conservative and highly reliable method of rating clock-input-frequency limits that, for the AC/ACT devices, equal or exceed the ratings for FAST types.

Low-Output Skew Flip-Flop Performance

AC/ACT flip-flop types such as the 74 dual D-type flip-flop are specially designed to have near equal delay from clock to Q and clock to $\overline{Q}$ as illustrated in Figure 33. Dual slave sections are used to achieve this highly desirable performance. Actual delay skew between Q and $\overline{Q}$ is typically 0.05ns and a Min/Max spread of 0.4ns at 85°C and a supply voltage (V_{CC}) of 5V. Figure 34 illustrates how this unique Harris flip-flop benefit can be used to drive a twisted pair. A termination R of about 300Ω is desirable to match the line and reduce reflections. The key element is near-zero skew at the Q and $\overline{Q}$ output edges.

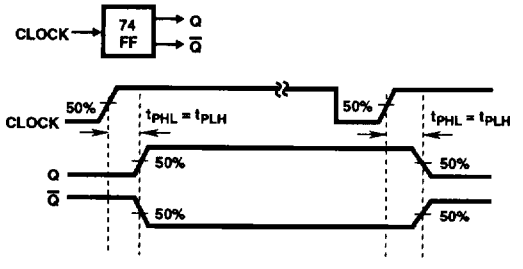


FIGURE 33. DELAY BALANCE OF DUAL D-TYPE FLIP-FLOP (AC/ACT74)

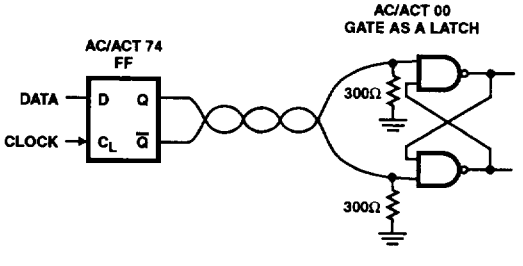


FIGURE 34. DUAL D-TYPE FLIP-FLOP (AC/ACT74) USED TO DRIVE A TWISTED PAIR

Metastability

Harris AC/ACT clocked devices are designed to minimize the probability of output states being at an undefined or unallowable condition because of violation of Clock/Data Setup time and Hold time specifications when used in asynchronous systems. Specifically, Setup and Hold times are kept small, typically 0ns to 2ns. Also, internal flip-flop feedback paths are very fast with little delay. These design features serve to make metastability much less prevalent than for slower-speed CMOS or TTL Logic types.

Power Consumption

The power consumption of an AC/ACT device is composed of two components: one static, the other dynamic. The static component is the result of quiescent current caused principally by reverse junction leakage. The dynamic component results from the transient currents required to charge and discharge the capacitive loads on logic elements, that is, the transients resulting from the overlapping of active p and n transistors. Internal chip power consumption is determined by the device equivalent power dissipation capacitance, C_{PD}; this parameter is defined below.

Power Calculations

Two equations are used to compute the total IC power consumption. Equation 2 is applicable to AC or ACT devices when the inputs are driven from ground to V_{CC} (rail to rail).

For AC types (EQ. 2)

$$P = P_{DC} + P_{AC}$$

$$P = I_{CC}V_{CC} + C_{PD}V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_O$$

Where:

I_{CC} = Quiescent Current (from Data Sheet Ratings)
V_{CC} = Supply Voltage
f_i = Input Frequency
f_O = Output Frequency Per Output
C_{PD} = Device Equivalent Power Dissipation Capacitance; Used for Computing Internal Chip Power (from Data Sheet)
C_L = Load Capacitance; Used for Computing Output Stage Power

Equation 3 is applicable only to an ACT device where specific input pins are driven at TTL levels defined as $V_I = 3.4V$ for a V_{CC} Max of 5.5V

For ACT types (EQ. 3)

$$P = P_{DC} + P_{AC}$$
$$P = I_{CC}V_{CC} + \Sigma (\Delta I_{CC}V_{CC}D + C_{PD}V_{CC}^2 f_i + C_L V_{CC}^2 f_O)$$

Where:

ΔI_{CC} = Added direct current per input when $V_I = V_{CC} - 2.1V$ (TTL input high level) (from data sheet)
D = Duty cycle of clock (% of time high)

The temperature-dependent ratings for I_{CC} are given in Tables 9 and 10.

TABLE 9. TEMPERATURE-DEPENDENT RATING LIMITS

	V_I (V)	V_{CC} (V)	+25°C TYP (mA)	+25°C MAX (mA)	-40°C TO +85°C MAX (mA)	-55°C TO +125°C MAX (mA)
ΔI_{CC} (Note 1)	V_{CC}-2.1	4.5 to 5.5	0.2	2.4	2.8	3

NOTE:

1. Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. ACT load table by type shown on each data sheet. Example: Type ACT191 input: clock unit load = 0.85 ΔI_{CC} = 0.85(2.4mA) = 2.04mA Max at +25°C.

TABLE 10. MAXIMUM QUIESCENT CURRENT AT V_{CC} = 5V FOR AC/ACT AND FAST TYPES

DEVICE COMPLEXITY	AC/ACT LIMIT +25°C	AC/ACT LIMIT +85°C	AC/ACT LIMIT +125°C	FAST +125°C
SSI/FF	4µA	40µA	80µA	15mA
MSI	8µA	80µA	160µA	100mA

The dynamic power due to outputs is the sum of the AC power at each output. The user must independently determine the C_L and the average frequency of each output. The latter requires estimating the average frequency of data nodes in a logic system. For example, for AC/ACT counter types, each output is inherently operating at different frequencies.

The C_{PD}, or device equivalent-power-dissipation capacitance, is determined by two sources of internal device power consumption:

1. Power consumed by charge and discharge of the internal device capacitance.
2. Power consumed through current switching transients.

Figure 35 illustrates the typical I_{CC} as a function of V_I for AC devices. Note in Figure 35C that when V_{IN} equals 0V to 0.5V or 4.5V to 5V, zero current flows. Thus, no ΔI_{CC} component is required for computing the power consumption of AC device types. The transient switching currents of an IC, however, consume power and are part of the C_{PD} value. The plots of I_{CC} and V_I of Figure 35 show peak I_{CC} of up to 12mA. For a few nanoseconds, however, up to 100mA could flow if the plotter resolution permitted. Note that the switching points (peak current points) in the AC devices occur at approximately 50% of V_{CC}. For the ACT devices (shown in Figure 36) the switching point is at approximately 30% of V_{CC}.

Figure 36 illustrates the typical I_{CC} as a function of V_I for ACT devices. Again, if the input voltage equals 0V to 0.5V or 4.5V to 5.5V, no ΔI_{CC} value exists. If V_I, however, is a TTL logic high level of 2.9V with a V_{CC} of 5V, then significant ΔI_{CC} does exist (0.2mA) and is indicated in Equation 3 as the ΔI_{CC} component.

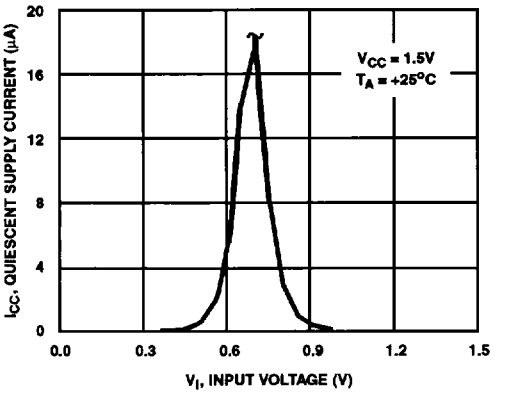


FIGURE 35A.

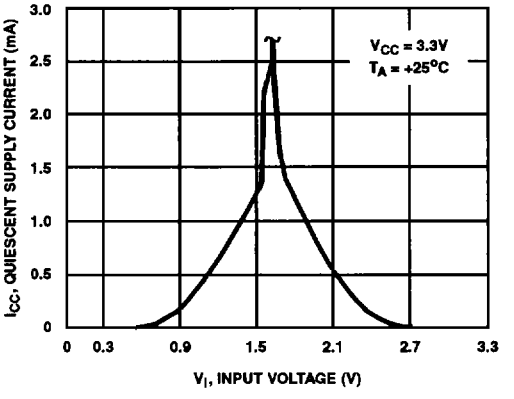


FIGURE 35B.

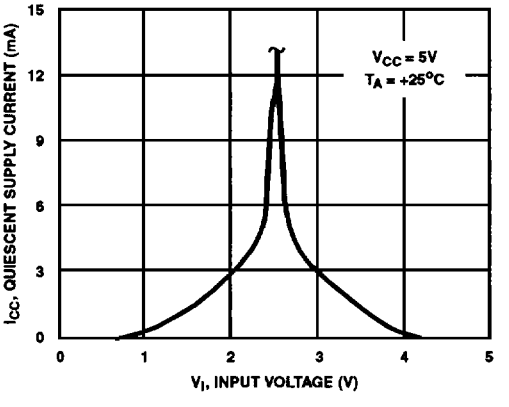


FIGURE 35C.

FIGURE 35. QUIESCENT SUPPLY CURRENT (I_{CC}) AS A FUNCTION OF INPUT VOLTAGE (V_I) FOR AC TYPES

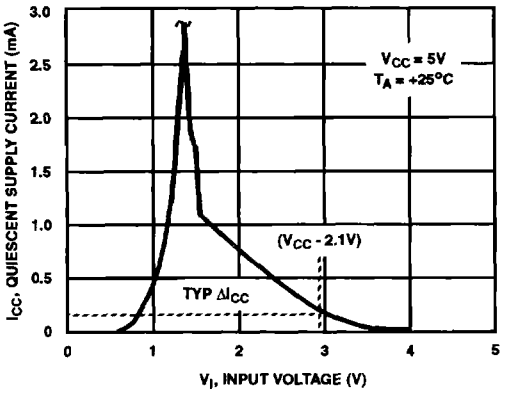


FIGURE 36. QUIESCENT SUPPLY CURRENT (I_{CC}) AS A FUNCTION OF INPUT VOLTAGE (V_I) FOR ACT TYPES

In many TTL to CMOS ACT input interface applications only CMOS loads are driven and V_{OH} is 4V or more. As illustrated in Figure 36, ΔI_{CC} is 0 for TTL outputs only driving CMOS inputs. Only if a TTL output is fully loaded would the output V_{OH} be as low as 3V. Thus, ΔI_{CC} is usually negligible except in rare interfaces where full (15 fan out) TTL loading is present along with an ACT input.

Because the special input design of Harris ACT types reduces the value of ΔI_{CC}, the added power is small and is usually minimal compared to FAST power. If this special input circuitry were not used, the ΔI_{CC} values would be much higher.

Because appreciable current flows during device input switching, as shown in Figure 35 and Figure 36, it is important to maintain the fast input rise and fall times shown below.

INPUT RISE AND FALL SLEW RATE, dt/dv	MAX	UNITS	INPUTS
1.5V to 3V (AC Types)	50	ns/V	0 to V_{CC}
3.6V to 5.5V (AC Types)	20	ns/V	0 to V_{CC}
4.5V to 5.5V (ACT Types)	10	ns/V	0 to 3V

Because the typical output transition time is 3ns for AC/ACT types, a designer need only be concerned with exceeding the rise and fall slew rates shown above for interfacing or linear mode operation in applications such as RC oscillators, crystal oscillators, and the like.

When the Schmitt-Trigger type AC/ACT 14 is used either for shaping up slow signals or as an RC oscillator, power is increased by the prolonged through-current.

The adverse effect of power transitions is another reason to maintain input rise and fall slew rates under the recommended limits. Longer transitions may cause oscillations of logic circuits (and, hence, logic errors) or premature triggering, depending on the system V_{CC} and ground noise, which are amplified when input signals hover near the switching voltages illustrated in Figure 35 and Figure 36. To reduce the effects of slower transitions, the use of Schmitt-Trigger types is recommended.

Simultaneous switching transients affect the maximum input t_R, t_F. Figure 37 illustrates a worst case but feasible condition for either a hex inverter type (04 or 05) or a hex inverting Schmitt-Trigger type (14). Using a printed circuit board designed for a ground-bounce measurement, five of six outputs are switched simultaneously causing the internal power or ground point bounce as discussed previously under the heading Simultaneous Switching Transients.

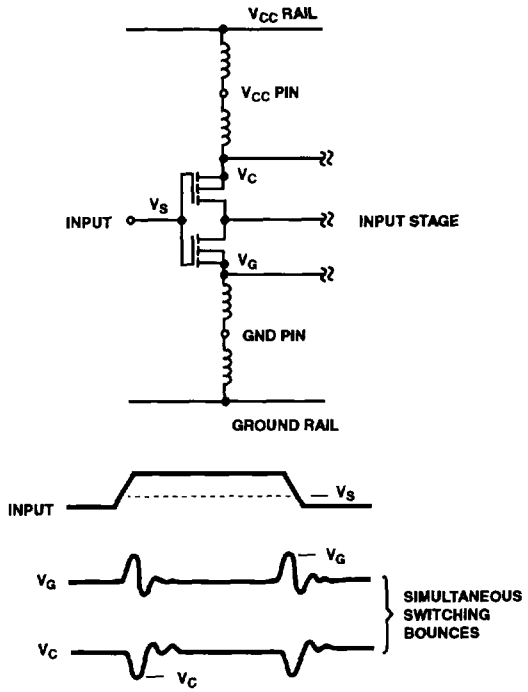


FIGURE 37. INPUT CIRCUIT AND SIMULTANEOUS SWITCHING BOUNCES THAT REDUCE NOISE IMMUNITY

Examination of the input stage and waveforms in Figure 37 shows clearly that typical noise immunity at the input is significantly reduced during the presence of the ground or V_{CC} bounce time as quantified below:

DC Noise Immunity Low V_S - 0V = 2.5V (AC)
= 1.5V (ACT)

AC Noise Immunity Low V_S - V_G = 2.5V - 0.75V
= 1.75V (AC)
= 0.75V (ACT)

DC Noise Immunity High V_{CC} - V_S = 2.5V (AC)
= 3.5V (ACT)

AC Noise Immunity High During V_{CC} Bounce V_C - V_S = 1.5V (AC)
= 2.5V (ACT)

Test results for the AC/ACT 04 and AC/ACT 14 types are illustrated in Figure 38. The results show that the real limiting values for input t_R, t_F slew rate times must take into account simultaneous switching effects. The Schmitt-Trigger type would ordinarily be considered to have nearly infinite slew rates for one-channel-only switching. For simultaneously switching five of six outputs, there is a probably finite limitation to slew rate times. However, tests for up to 150ms per volt for AC14 and 20ns per volt for ACT14 input slew rates (simultaneously on five inputs) did not affect the output.

V_{CC} = 5V, T_A = +25°C

TYPE	MAXIMUM SLEW RATES	
	MEASURED (t_R)	PUBLISHED (t_F)
AC04	> 20ns/V	20ns/V
ACT04	>10ns/V	10ns/V
AC14	290ms/V	150ms/V
ACT14	40ns/V	20ns/v

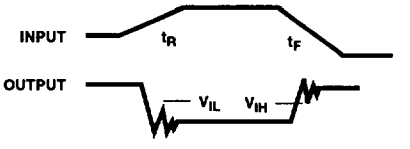


FIGURE 38. RESULTS OF TYPICAL INPUT t_R, t_F TESTS ON AC/ACT04/14 TYPES. V_{CC} = 5V, T_A = +25°C. THE MAXIMUM VALUE OF t_R, t_F IS DEFINED FOR CONDITION THAT OUTPUT RINGING EXCEEDS V_{IL} OR GOES BELOW V_{IH}. FIVE OF SIX OUTPUTS ARE SWITCHING SIMULTANEOUSLY

Power Consumption of FAST and AC/ACT Types Compared

As the equations for operating power indicate, CMOS power is directly proportional to switching frequency. At standby, AC/ACT power is negligible compared to bipolar FAST power. In Table 11, one of the most widely used MSI counters (the 191 4-Bit Binary Counter) is used to illustrate that even at a continuous 10MHz switching rate, AC/ACT power is a fraction of the power of FAST types. By way of illustration, consider an application employing 25 such types. At an overall average switching rate of 10MHz, with FAST types the power is 7.7W; with AC/ACT types, the power is only 1.4W for AC types and 2.6W for ACT types.

TABLE 11. AVERAGE OPERATING POWER COMPARISON FOR FAST AND AC/ACT TYPE 191, A 4-BIT UP/DOWN BINARY COUNTER (V_{CC} = 5.5V; T_A = 70°C)

FAMILY	NOTES	SWITCHING RATE			UNITS
		0MHz	1MHz	10MHz	
AC	1	0.44	5.5	55	mW
ACT	2	49.4	59.9	104	mW
FAST	3	204	224	306	mW

NOTES:

2. $P = P_{DC} + P_{AC}$
   Where: $P_{DC} = 5.5 \times 80\mu A$
   and $P_{AC} = 133pF(5.5)^2f_i + 50pF(5.5)^2 + (1/2 + 1/4 + 1/8 + 1/16 + 1/16)f_O$ (See Equation 2)
3. $P = P_{DC} + P_{AC}$
   Where: $P_{DC} = 5.5 \times 80\mu A + 8 \times 2.8mA \times 0.8 \times 1/2 \times 5.5$ (See Equation 3)
   and $P_{AC} = 133pF(5.5)^2f_i + 50pF(5.5)^2 + (1/2 + 1/4 + 1/8 + 1/16 + 1/16)f_O$ (See Equation 2)
4. P = 5.5 x 55mA (0Hz)
   P = 5.5 x 55mA x 1.1 (1MHz)
   P = 5.5 x 55mA x 1.5 (10MHz)

Special Harris AC/ACT Types

The Harris line of AC/ACT has some unique types that are tailored for specific high speed applications. Each is highlighted below.

CD54/74 AC/ACT7623 - Octal-Bus Transceiver, Three-State (B-Side), Open-Drain (A-Side), Non-Inverting.

The only difference from the generic bipolar type 623 is that the 7623 has an open drain on the A-side; the 623 is three-state for both sides. The 7623 permits bus interfacing on the A-side without concern about bus contention. Also, the bus termination resistance is used to pull up the bus to a high state.

CD54/74 AC/ACT7060 - 14-Stage Binary Counter with Oscillator.

The 7060 type is a 14-stage binary ripple counter having a built-in oscillator section (typically 200MHz) for either an RC design or an accurate crystal referenced design. A Master Reset input resets all binary stages to the all "0" state and also disables the oscillator when the Master Reset is high in the 7060 version.

References

JEDEC Standard No. 8. "Standard for Reduced Operating Voltages and Interface Levels for Integrated Circuits."

JEDEC Standard No. 20A, "Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High Speed CMOS Devices".