



FDD3670

# FDD3670

## 100V N-Channel PowerTrench<sup>®</sup> MOSFET

### General Description

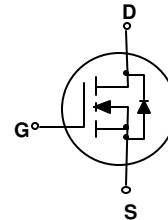
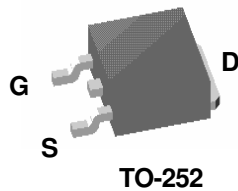
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable  $R_{DS(ON)}$  specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

### Features

- 34 A, 100 V.  $R_{DS(ON)} = 32\text{ m}\Omega @ V_{GS} = 10\text{ V}$   
 $R_{DS(ON)} = 35\text{ m}\Omega @ V_{GS} = 6\text{ V}$
- Low gate charge (57 nC typical)
- Fast switching speed
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	100	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1)	34	A
	Drain Current – Pulsed (Note 3)	100	
$P_D$	Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ (Note 1)	83	W
	@ $T_A = 25^\circ\text{C}$ (Note 1a)	3.8	
	@ $T_A = 25^\circ\text{C}$ (Note 1b)	1.6	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	1.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD3670	FDD3670	13"	16mm	2500 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Drain-Source Avalanche Ratings (Note 2)

$W_{DSS}$	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 50\text{ V}, I_b = 7.3\text{ A}$			360	mJ
$I_{AR}$	Maximum Drain-Source Avalanche Current				7.3	A

### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_b = 250\ \mu\text{A}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_b = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		92		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_b = 250\ \mu\text{A}$	2	2.5	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_b = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-7.2		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_b = 7.3\text{ A}$ $V_{GS} = 10\text{ V}, I_b = 7.3\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 6\text{ V}, I_b = 7.0\text{ A}$		22 39 24	32 56 35	m $\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	25			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_b = 7.3\text{ A}$	15	31		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		2490		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		265		pF
$C_{rss}$	Reverse Transfer Capacitance			80		pF

### Switching Characteristics (Note 2)

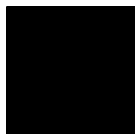
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_b = 1\text{ A}$		16	26	ns
$t_r$	Turn-On Rise Time	$V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		10	18	ns
$t_{d(off)}$	Turn-Off Delay Time			56	84	ns
$t_f$	Turn-Off Fall Time			25	40	ns
$Q_g$	Total Gate Charge	$V_{DS} = 50\text{ V}, I_b = 7.3\text{ A}$		57	80	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 10\text{ V}$		11		nC
$Q_{gd}$	Gate-Drain Charge			15		nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current				2.7	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.7\text{ A}$ (Note 2)		0.72	1.2	V

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $R_{\theta JA} = 40^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2oz copper.



b)  $R_{\theta JA} = 96^\circ\text{C/W}$  on a minimum mounting pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width <  $300\ \mu\text{s}$ , Duty Cycle < 2.0%
- Pulse  $I_d$  refers to Figure.9 Forward Bias Safe Operation Area.

Typical Characteristics

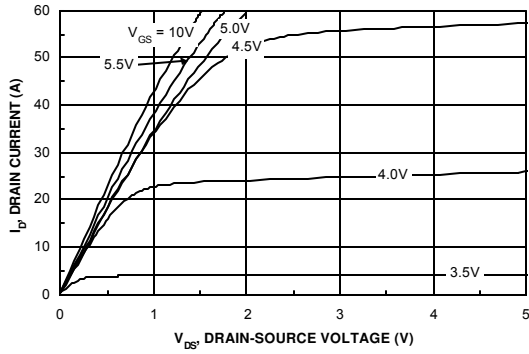


Figure 1. On-Region Characteristics.

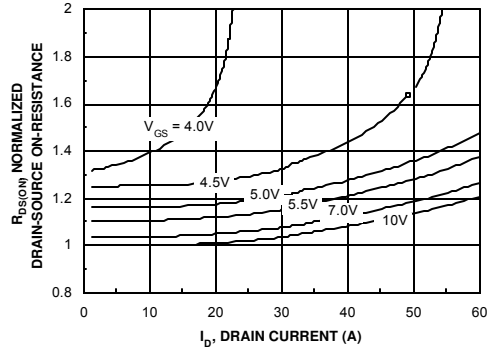


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

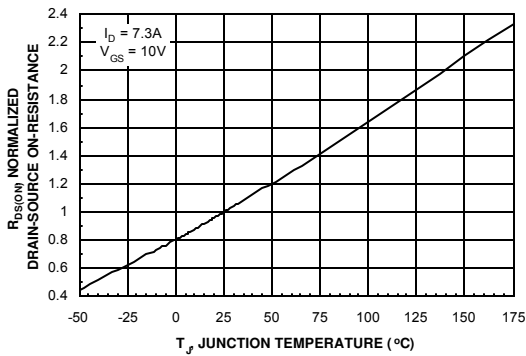


Figure 3. On-Resistance Variation with Temperature.

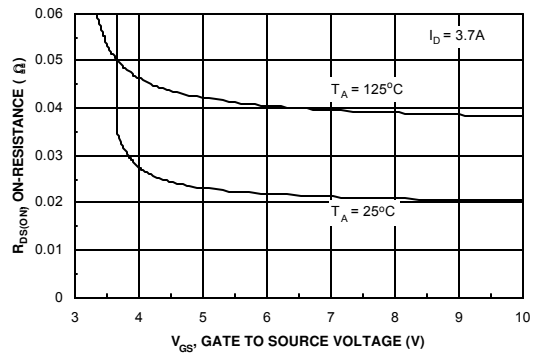


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

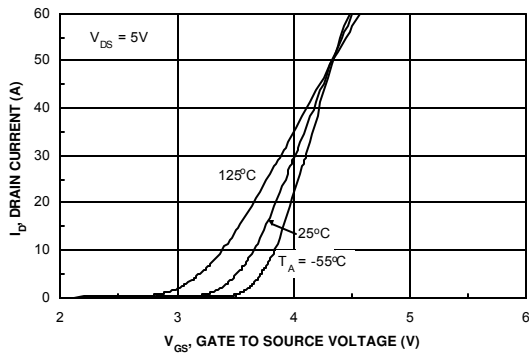


Figure 5. Transfer Characteristics.

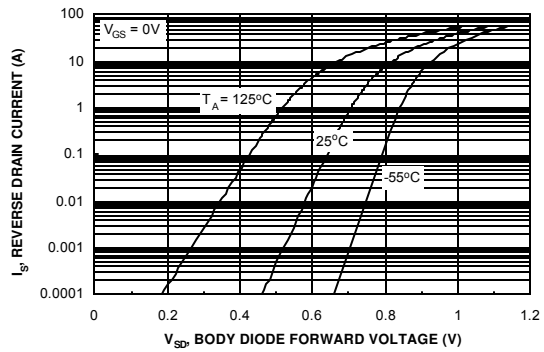


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

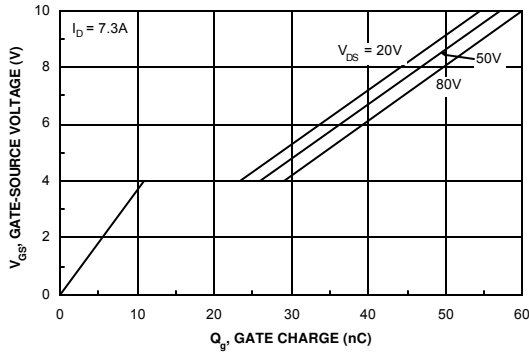


Figure 7. Gate Charge Characteristics.

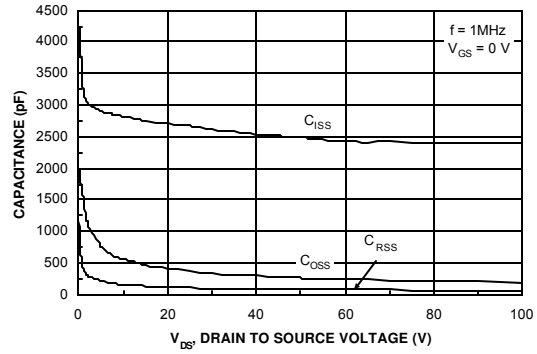


Figure 8. Capacitance Characteristics.

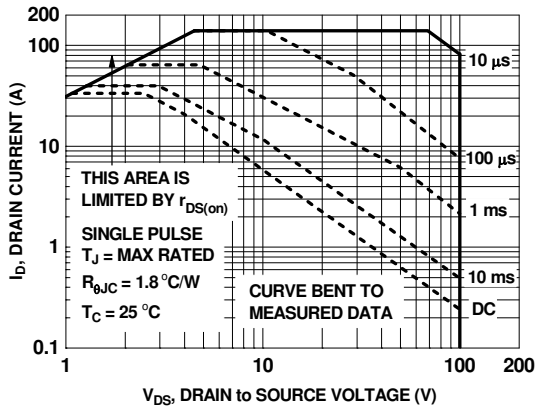


Figure 9. Forward Bias Safe Operating Area.

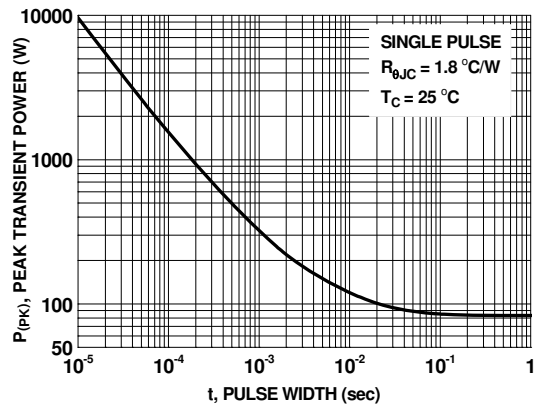


Figure 10. Single Pulse Maximum Power Dissipation.

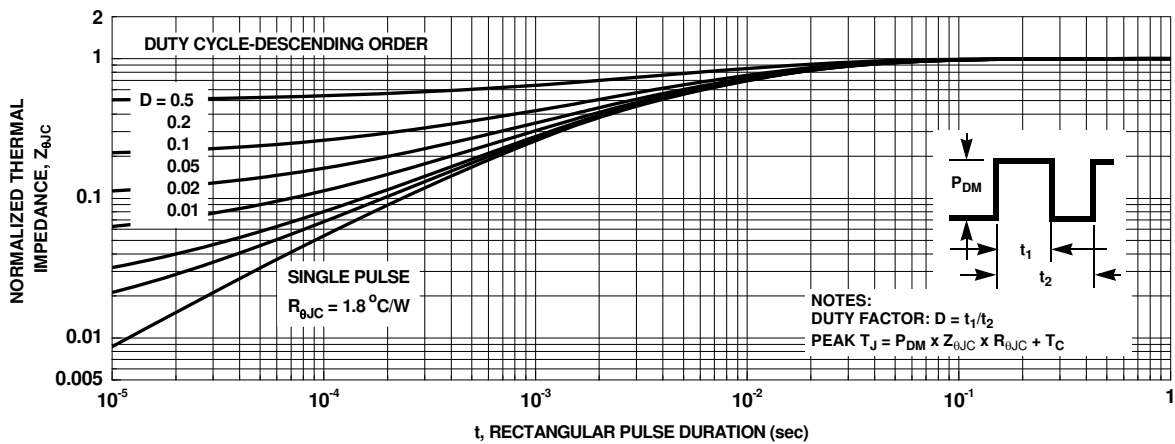
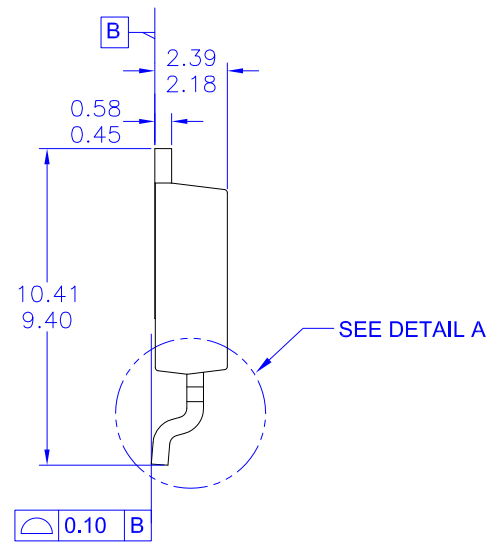
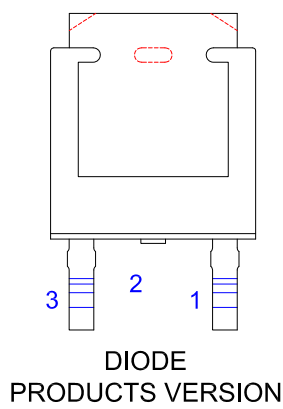
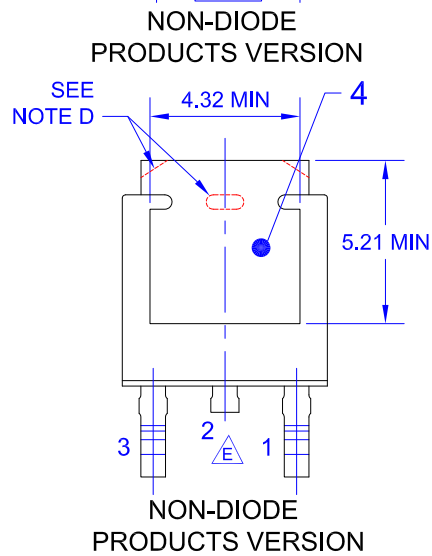
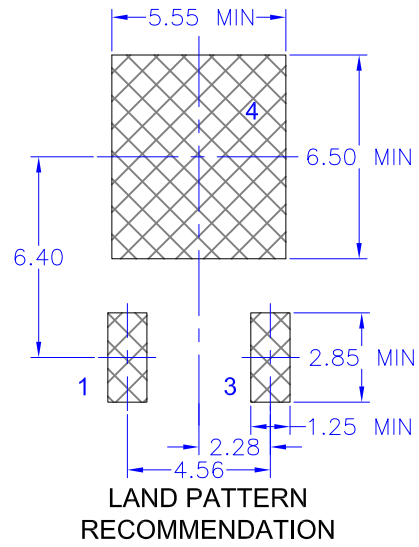
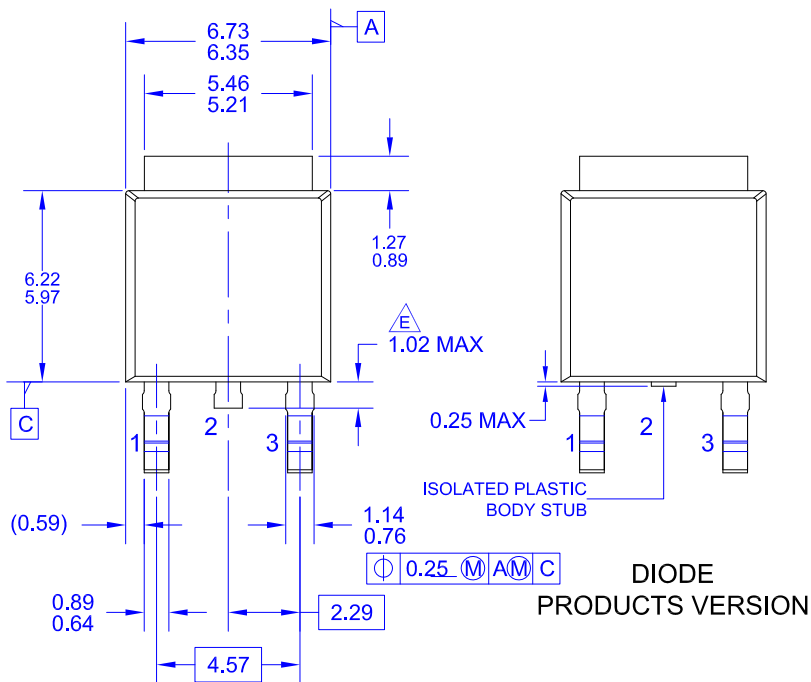
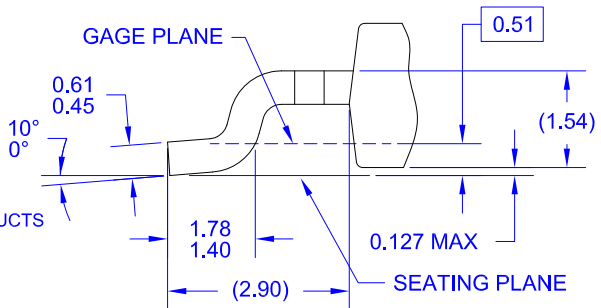


Figure 11. Junction-to-Case Transient Thermal Response Curve



**NOTES: UNLESS OTHERWISE SPECIFIED**

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



**DETAIL A**  
(ROTATED -90°)  
SCALE: 12X







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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I77