1 OUTPUT PCIE GEN1/2/3 SYNTHESIZER

5V41234

Typical Applications

One output synthesizer for PCIe Gen1/2/3

Description

The 5V41234 is a PCIe Gen2/3 compliant spread spectrum capable clock generator. The device has 1 differential HCSL output and can be used in communication or embedded systems to substantially reduce electro-magnetic interference (EMI). Spread spectrum can be enabled via a select pin.

Output Features

- 1 - 0.7V current mode differential HCSL output pairs

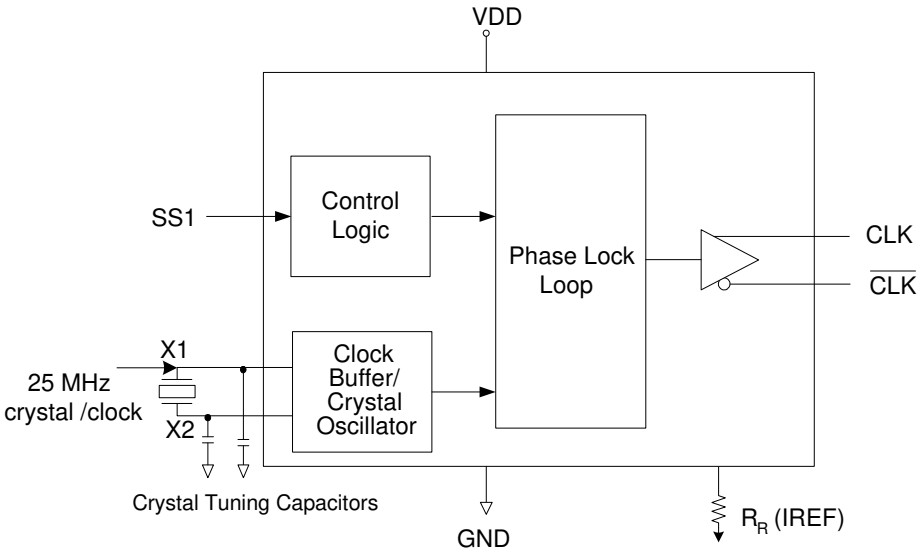
Features

- 3 x 3 mm 16-QFN package; very small board footprint
- Spread-spectrum capable; reduces EMI
- Outputs can be terminated to LVDS; can drive a wider variety of devices
- Spread enable via pin selection; no software required to configure device
- Industrial temperature range available; supports demanding embedded applications

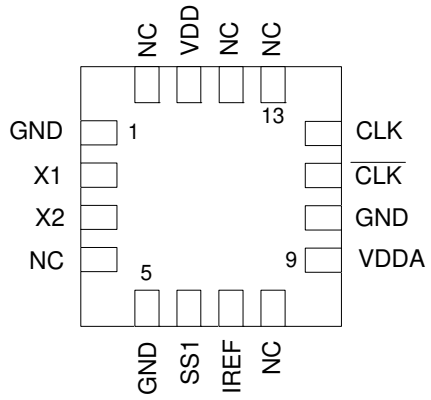
Key Specifications

- Cycle-to-cycle jitter < 100 ps
- PCIe Gen2 phase jitter < 3.0ps RMS
- PCIe Gen3 phase jitter < 1.0ps RMS

Block Diagram



Pin Assignment



16-pin QFN

Spread Spectrum Select Table

SS1	Spread%
0	-0.5% down
1	No spread

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	GND	Power	Connect to ground.
2	X1	XI	Crystal or clock input. Connect to 25MHz crystal or single-ended clock.
3	X2	XO	Crystal connection. Connect to parallel mode crystal. Leave floating if X1 is driven by single-ended clock.
4	NC	–	No connect.
5	GND	Power	Connect to ground.
6	SS1	Input	Spread Select 1. See table above. Internal pull-up resistor.
7	IREF	Output	475Ω precision resistor must be attached to this pin, which is connected to internal current source.
8	NC	–	No connect.
9	VDDA	Power	Connect to 3.3V and filter as analog supply.
10	GND	Power	Connect to ground.
11	$\overline{\text{CLK}}$	Output	HCSL complementary output clock.
12	CLK	Output	HCSL true output clock.
13	NC	–	No connect.
14	NC	–	No connect.
15	VDD	Power	Connect to 3.3V for OSC and digital circuits.
16	NC	–	No connect.

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01µF should be connected between VDD and the ground plane (pin 4) as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into IDT pin.

Crystal

A 25 MHz fundamental mode parallel resonant crystal with C_L = 16pF should be used. This crystal must have less than 300 ppm of error across temperature in order for the 5V41234 to meet PCI Express specifications.

Crystal Capacitors

Crystal capacitors are connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

C_L= Crystal's load capacitance in pF

Crystal Capacitors (pF) = (C_L- 8) * 2

For example, for a crystal with a 16 pF load cap, each external crystal cap would be 16pF. (16-8)*2=16.

Current Source (Iref) Reference Resistor - R_R

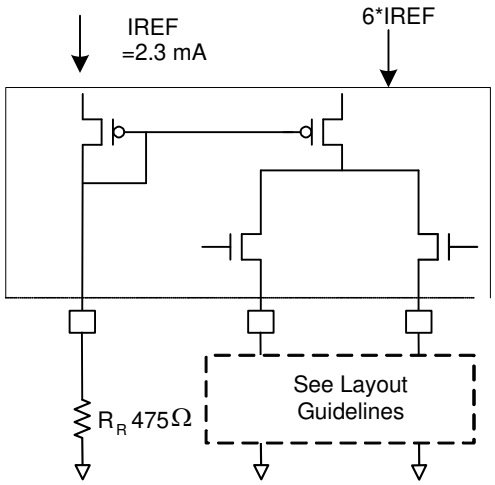
If board target trace impedance (Z) is 50Ω, then R_R = 475Ω (1%), providing IREF of 2.32mA. The output current (I_{OH}) is equal to 6*IREF.

Output Termination

The PCI-Express differential clock outputs of the 5V41234 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The 5V41234 can also be terminated to LVDS compatible voltage levels. See Layout Guidelines section.

Output Structures



General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.

2. No vias should be used between decoupling capacitor and VDD pin.

3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the 5V41234.This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Layout Guidelines for PCI Express

PCIe Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

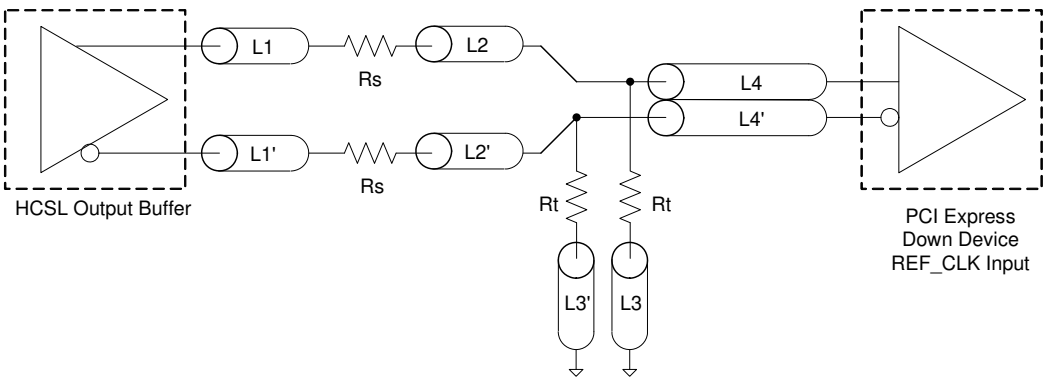
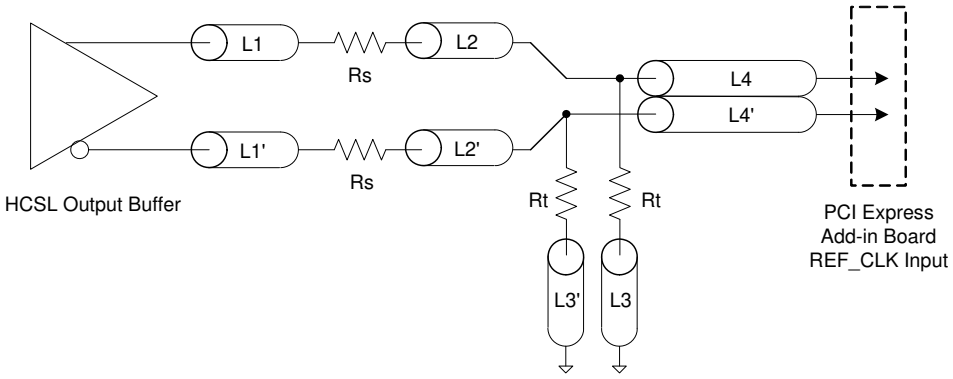


Figure 2: PCI Express Connector Routing

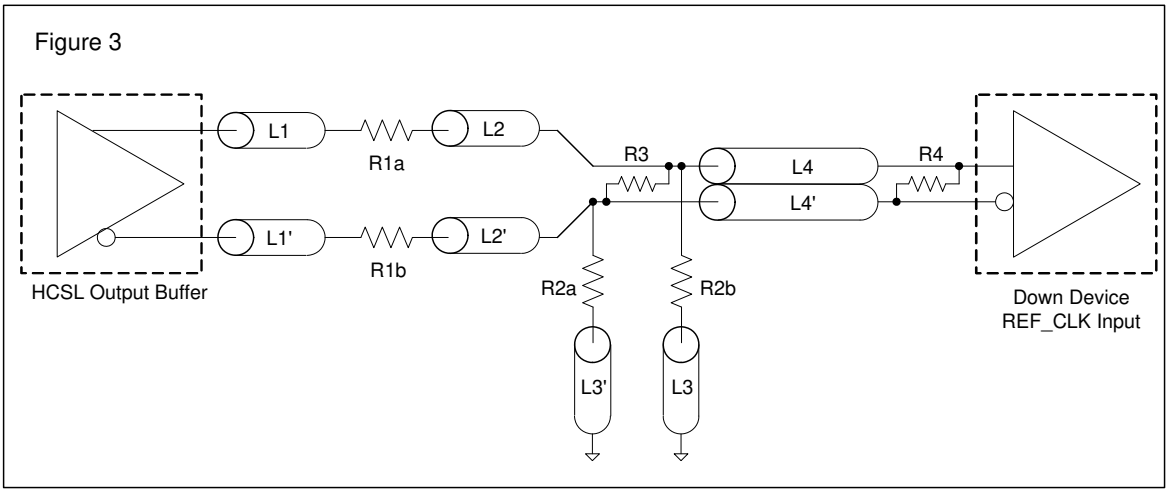


Layout Guidelines for LVDS and Other Applications

Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

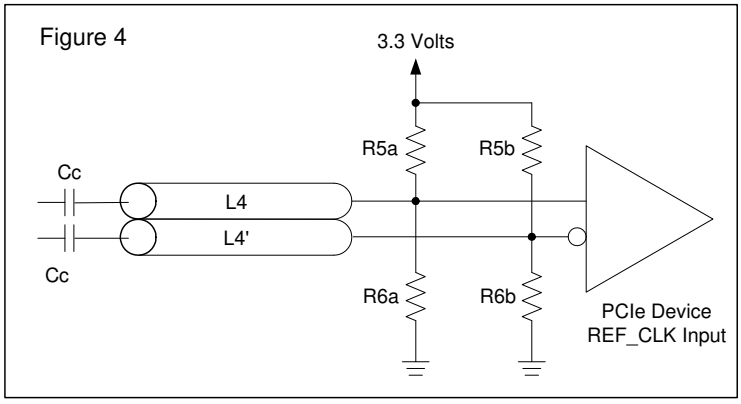
R1a = R1b = R1
R2a = R2b = R2

Figure 3

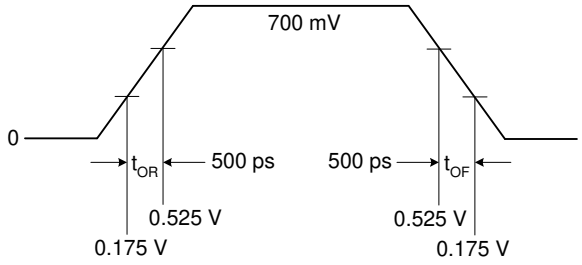


Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

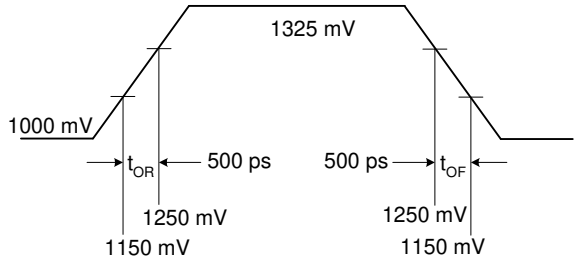
Figure 4



Typical PCI-Express (HCSL) Waveform



Typical LVDS Waveform



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5V41234. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD, VDDA	5.5V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature (commercial)	0 to +70°C
Ambient Operating Temperature (industrial)	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD Protection (Input)	2000V min. (HBM)

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3V ±5%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V		3.135		3.465	
Input High Voltage[1]	V_{IH}		2.2		VDD +0.3	V
Input Low Voltage[1]	V_{IL}		VSS-0.3		0.8	V
Input Leakage Current[2]	I_{IL}	0 < Vin < VDD	-5		5	µA
Operating Supply Current	I_{DD}	2pF load			70	mA
Input Capacitance	C_{IN}	Input pin capacitance			7	pF
Output Capacitance	C_{OUT}	Output pin capacitance			6	pF
Pin Inductance	L_{PIN}				5	nH
Output Resistance	Rout	CLK outputs	3.0			kΩ
Pull-up Resistor	R_{PUP}	SS1		100		kΩ

1. Single edge is monotonic when transitioning through region.
2. Inputs with pull-ups/-downs are not included.

AC Electrical Characteristics - CLK/$\overline{CLK}$

Unless stated otherwise, **VDD=3.3V ±5%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				25		MHz
Output Frequency				100		MHz
Output High Voltage[1,2]	V_{OH}		660	700	850	mV
Output Low Voltage[1,2]	V_{OL}		-150	0	27	mV
Crossing Point Voltage[1,2]		Absolute	250	350	550	mV
Crossing Point Voltage[1,2,4]		Variation over all edges		40	140	mV
Jitter, Cycle-to-Cycle[1,3]				25	100	ps
Rise Time[1,2]	t_{OR}	From 0.175V to 0.525V	175	332	700	ps
Fall Time[1,2]	t_{OF}	From 0.525V to 0.175V	175	344	700	ps
Rise/Fall Time Variation[1,2]				75	125	ps
Duty Cycle[1,3]			45	51	55	%
Stabilization Time	t_{STABLE}	From power-up VDD = 3.3V		1.2	3.0	ms
Spread Change Time	t_{SPREAD}	Settling period after spread change		3.0		ms

[1] Test setup is R_S=33 ohms R_P=50 ohms with 2pF, R_R = 475Ω (1%).

[2] Measurement taken from a single-ended waveform.

[3] Measurement taken from a differential waveform.

[4] Measured at the crossing point where instantaneous voltages of both CLK and $\overline{CLK}$ are equal.

Electrical Characteristics - Differential Phase Jitter

T_A = Commercial and Industrial, Supply Voltage VDD = 3.3 V +/-5%			SPEC				
PARAMETER	Symbol	Conditions	Min	Typ	Max	Units	Notes
Jitter, Phase	$t_{jphaseG1}$	PCIe Gen 1		28	86	ps (p-p)	1,2,3
	$t_{jphaseG2Lo}$	PCIe Gen 2 10kHz < f < 1.5MHz		1.1	3	ps (RMS)	1,2,3
	$t_{jphaseG2High}$	PCIe Gen 2 1.5MHz < f < Nyquist (50MHz)		1.8	3.1	ps (RMS)	1,2,3
	$t_{jphaseG3}$	PCIe Gen 3		0.48	1	ps (RMS)	1,2,3

[1]Guaranteed by design and characterization, not 100% tested in production.

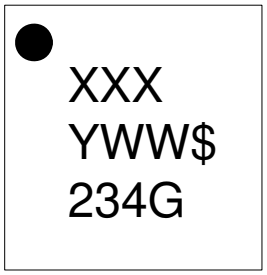
[2]See http://www.pcisig.com for complete specs

[3]Applies to 100MHz, spread off and 0.5% down spread only.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		69.4		°C/W
	θ_{JA}	1 m/s air flow		60.7		°C/W
	θ_{JA}	2.5 m/s air flow		54.4		°C/W
Thermal Resistance Junction to Case	θ_{JC}			9.7		°C/W

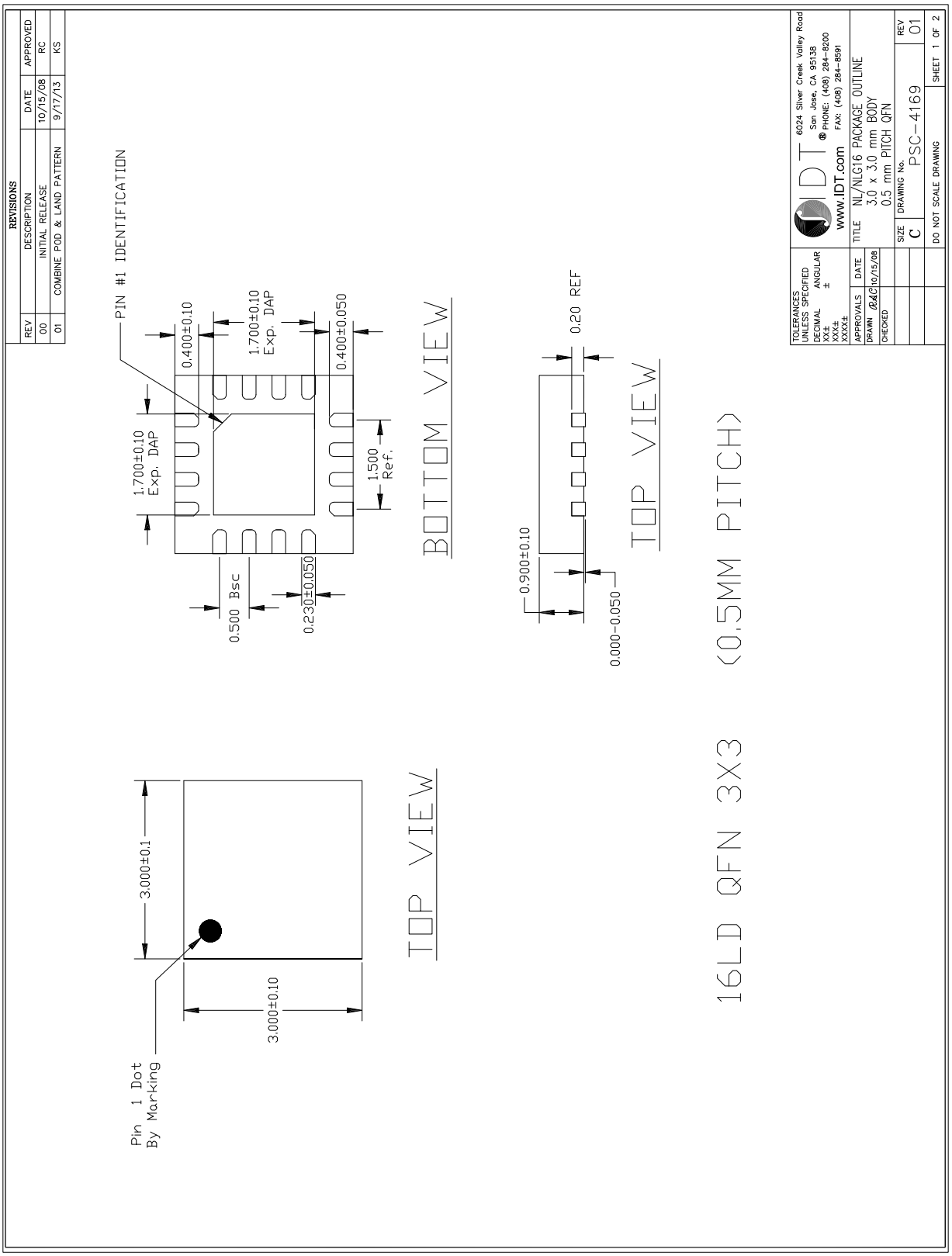
Marking Diagrams



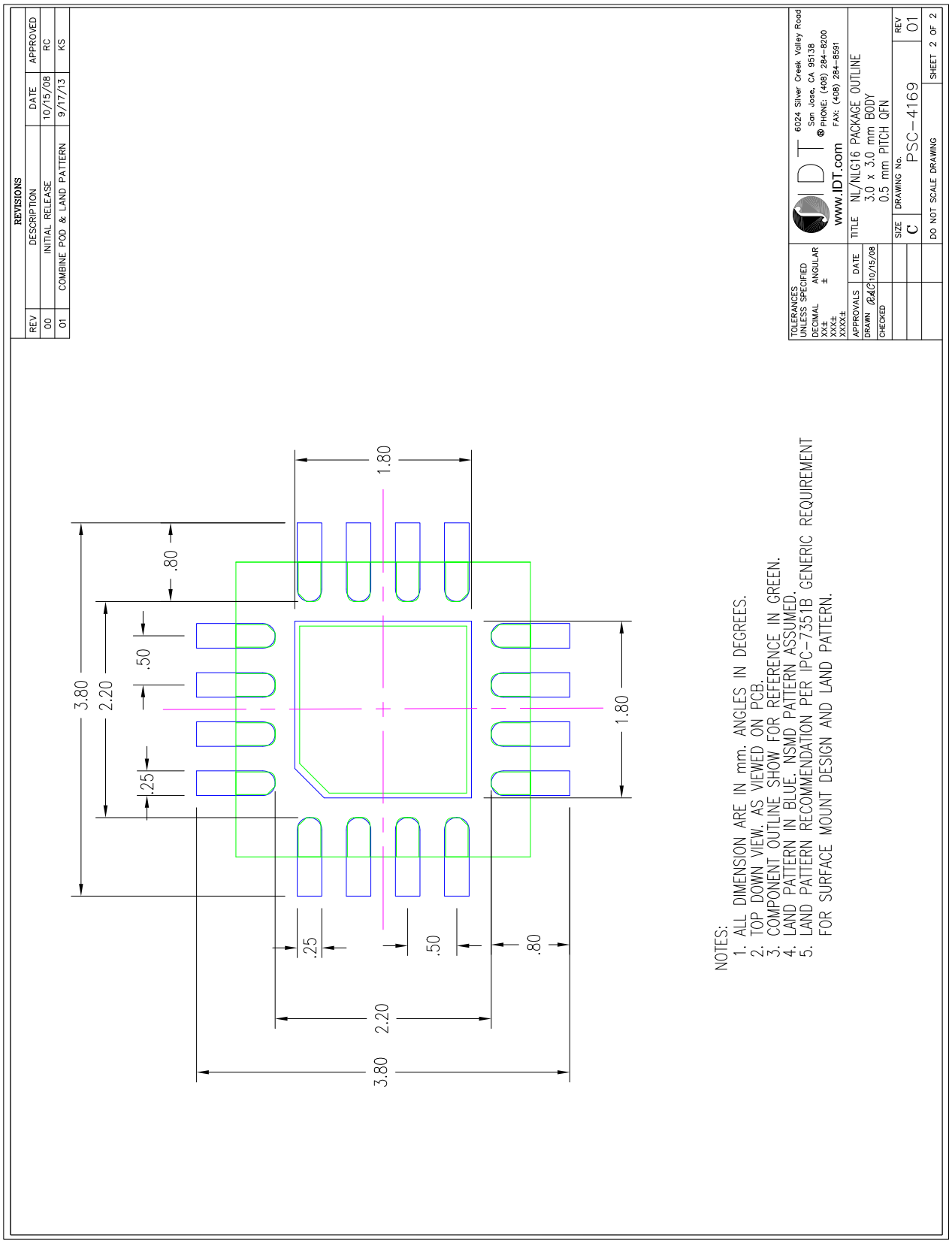
Notes:

1. Line 1: “XXX” is the lot traceability (last numeric character of the assembly lot number).
2. Line 2: “YYW” – date code; “$” – assembly location.
3. Line 3: truncated IDT part number.
4. “G” designates RoHS compliant package.
5. “I” within the part number indicates industrial temperature range.

Package Outline and Package Dimensions (3 x 3 mm 16-QFN)



Package Outline and Package Dimensions (3 x 3 mm 16-QFN), cont.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5V41234NLG	See Page 9	Tubes	3 x 3 mm 16-QFN	0 to +70°C
5V41234NLG8		Tape and Reel	3 x 3 mm 16-QFN	0 to +70°C
5V41234NLGI		Tubes	3 x 3 mm 16-QFN	-40 to +85°C
5V41234NLGI8		Tape and Reel	3 x 3 mm 16-QFN	-40 to +85°C

"G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	09/26/11	RDW	Initial release.
B	11/22/11	RDW	1. Changed title to "1 Output PCIe GEN1/2/3 Synthesizer" 2. Updated Differential Phase Jitter table.
B	03/20/14	S. Lou	Corrected typo in shipping packaging section of Ordering Information table - changed "Trays" to "Tubes".
C	05/05/17	C.P.	1. Updated package drawing to the latest NLG16 version. 2. Updated legal disclaimer.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.