

AN-1449 LM2747 Evaluation Board

1 Introduction

This document describes the LM2747 printed circuit board (PCB) design and provides an example typical application circuit. The demo board allows component design flexibility in order to demonstrate the versatility of the LM2747 IC.

The demo board contains a voltage-mode, high-speed synchronous buck regulator controller. Though the control sections of the IC are rated for 3 V to 6 V (V_{CC}), the driver sections are designed to accept input supply rails (V_{IN}) as high as 14 V.

The demo board design regulates to an output voltage of 1.2 V at 3.5A with a switching frequency of 1MHz from a 1 MHz clock source that has an amplitude from 0 V to V_{CC} . Note, the demo board is optimized for a 1MHz, 14 V input voltage compensation design with $V_{CC} = 3.3$ V. If a slower switching frequency and input voltage is desired, please consult the device data sheet for control loop compensation procedures. For additional design modifications, see the *Design Consideration* section of the *LM2747 Synchronous Buck Controller With Pre-Bias Startup, and Optional Clock Synchronization Data Sheet* ([SNVS370](#)).

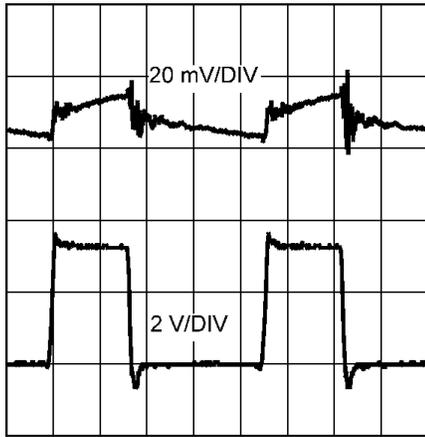
The demo board accommodates the use of banana clips to clip onto pads on the board, if preferred, the pads inner diameters are 100mils, for which a solder terminal can be placed (Newark 40F6004). The PCB is designed on two layers with 1oz. copper on a 62mil FR4 laminate.

2 Additional Footprints

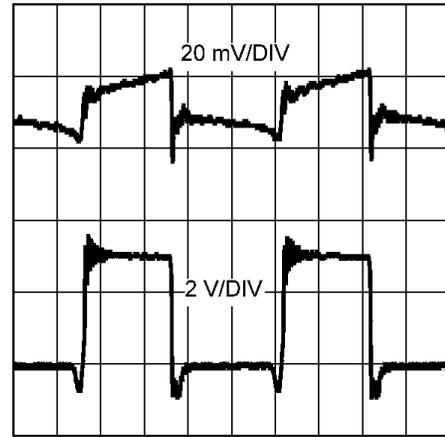
An additional footprint D1 is available for a Schottky diode to be placed in parallel with the low side MOSFET. This component can improve efficiency, due to the lower forward drop than the low side MOSFET body diode conducting during the anti-shoot through period. Select a Schottky diode that maintains a forward drop around 0.4 to 0.6 V at the maximum load current (consult the I-V curve). In addition select the reverse breakdown voltage to have sufficient margin above the maximum input voltage.

Footprint C13 is available for a multilayer ceramic capacitor (MLCC) connected flush to the source of the low side MOSFET and drain of the high side MOSFET, in order to provide low supply impedance. For example, component C13 is used in combination with aluminum electrolytic input filter capacitors, placed in designators C12 and C14. If MLCCs are used in designators C12 and C14 component C13 is not necessary.

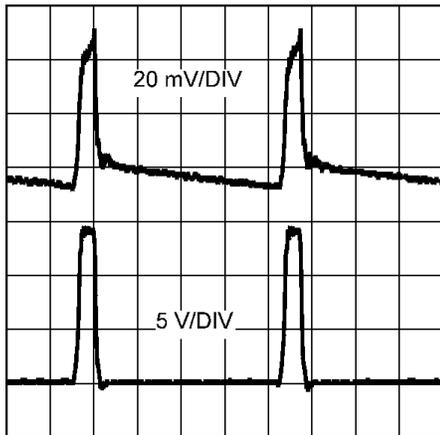
4 Performance Characteristics (Output Ripple Voltage and Switch Node Voltage)



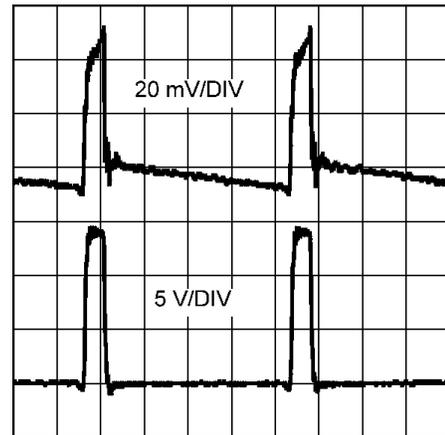
200 ns/DIV
Figure 2. $V_{IN} = V_{CC} = 3.3\text{ V}$,
 $V_{OUT} = 1.2\text{ V}$, $I_{LOAD} = 0\text{ A}$, $f_{SW} = 1\text{ MHz}$
 20 MHz Bandwidth Limit



200 ns/DIV
Figure 3. $V_{IN} = V_{CC} = 3.3\text{ V}$,
 $V_{OUT} = 1.2\text{ V}$,
 $I_{LOAD} = 3.5\text{ A}$, $f_{SW} = 1\text{ MHz}$.
 20 MHz Bandwidth Limit



200 ns/DIV
Figure 4. $V_{IN} = 14\text{ V}$, $V_{CC} = 5\text{ V}$,
 $V_{OUT} = 1.2\text{ V}$, $I_{LOAD} = 0\text{ A}$, $f_{SW} = 1\text{ MHz}$.
 20 MHz Bandwidth Limit



200 ns/DIV
Figure 5. $V_{IN} = 14\text{ V}$, $V_{CC} = 5\text{ V}$,
 $V_{OUT} = 1.2\text{ V}$, $I_{LOAD} = 3.5\text{ A}$, $f_{SW} = 1\text{ MHz}$.
 20 MHz Bandwidth Limit

5 PCB Layout Diagrams

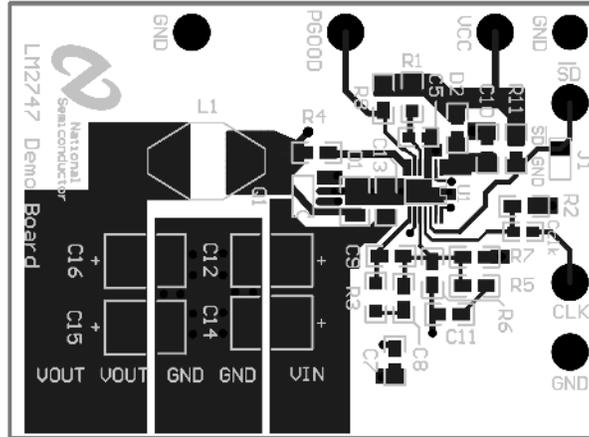


Figure 7. Top Layer and Top Overlay

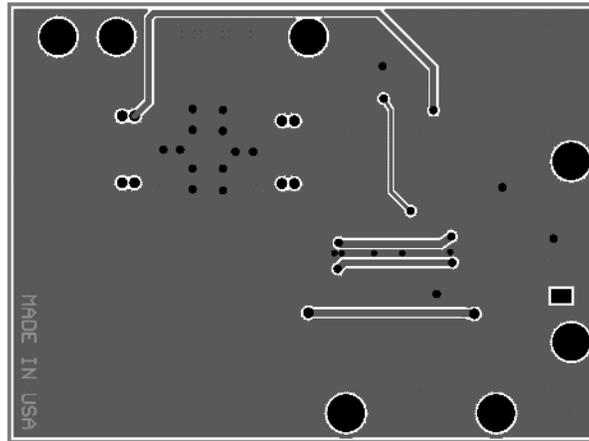


Figure 8. Bottom Layer

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