General Description

The IDTF1200 is a Digitally Controlled Intermediate Frequency Differential Variable Gain Amplifier for BaseStation and other commercial applications with a low IF frequency. The device offers extremely low Noise Figure over the entire gain control range. The device is packaged in compact 5x5 Thin QFNs with 200 ohm differential input and output impedances for ease of integration into the receiver lineup. Versions covering IF frequencies up to 300 MHz with low distortion are available.

Competitive Advantage

The F1200 acts to enhance system SNR when VGA gain is reduced. The F1200 noise figure (NF) degrades only slightly (NF slope ~ -0.16 $^{dB}/_{dB}$) over a 13 dB control range while holding the Output IP3 approximately constant. The resultant improvement in noise can enhance the system SNR up to 2 decibels at low gain settings relative to a standard VGA.

The device has excellent DNL and INL simplifying digital compensation. The device also offers the extremely low Harmonic, IM2, and IM3 distortion necessary to drive an ADC directly in an IF sub-sampling application.

Applications

- BaseStation Diversity Receivers
- Digital Pre-Distortion
- µWave Point-to-Point Radios
- Public Safety Receivers

Part# Matrix

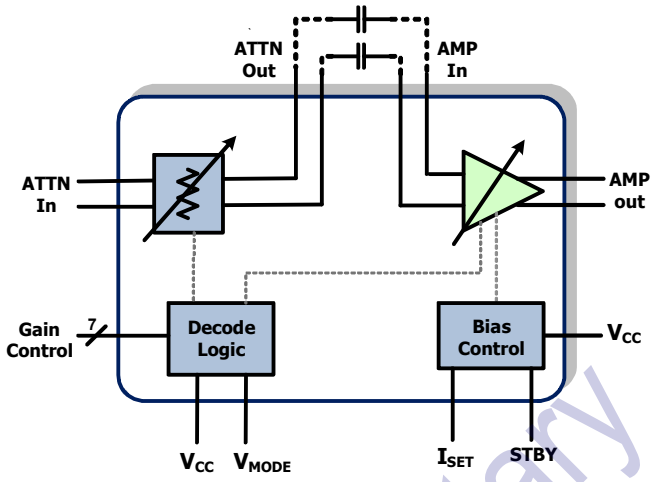
Part#	Gain Range	$IP3_O$	IF freq range	NF
F1200	**22 to -1**	**48**	**50 - 160**	**2.6**
F1206*	20 to -11	47	150 - 250	3.6
F1207*	20 to -11	46	230 - 300	3.7

*Future Product

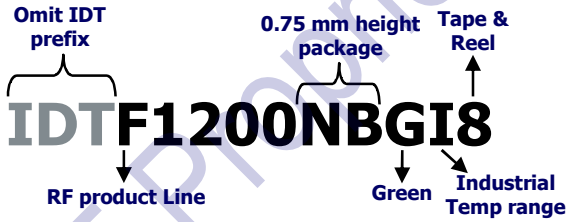
Features

- Ideal for high SNR systems
- 22 dB typ Maximum Gain
- 23 dB gain control range
- 7 bit parallel control
- 0.25 dB Gain Steps
- Excellent **Noise Figure < 3.0 dB**
- 5mm x 5mm 28 pin package
- 200 Ω Differential Input
- 200 Ω Differential Output
- **NF degrades < 2dB @ 12dB reduced gain**
- 50 MHz – 160 MHz frequency range
- Ultra-Linear: **$IP3_O$ +48 dBm typical**
- External current setting resistor
- Fast Gain Step Settling < 20 nsec

Device Block Diagram



Ordering Information

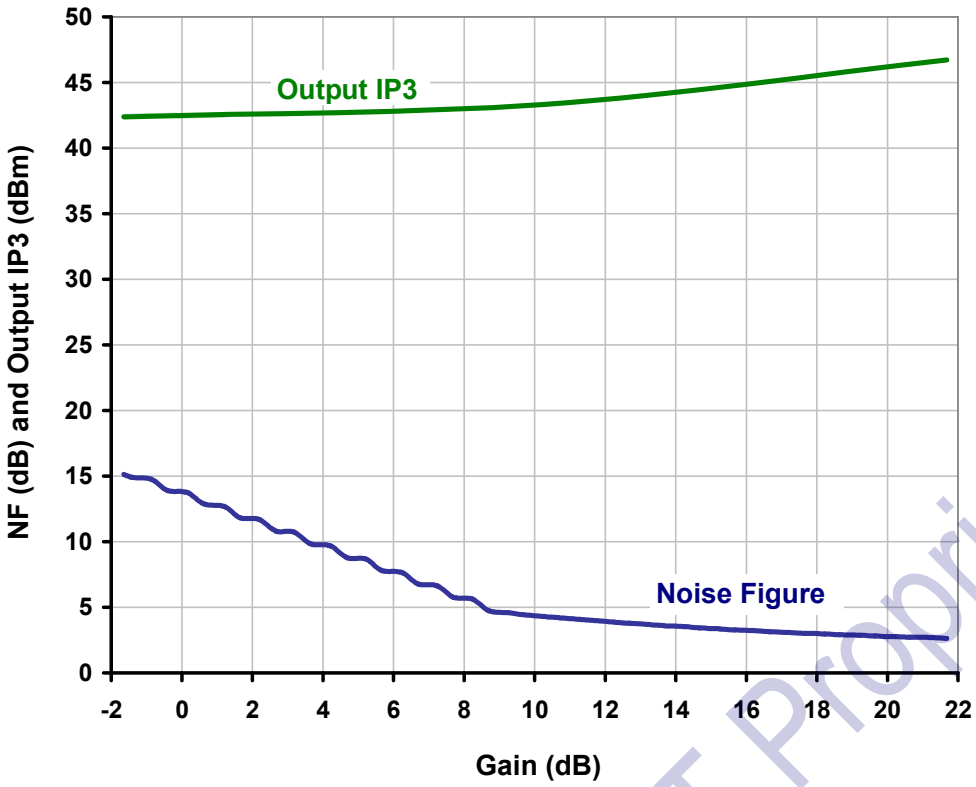


ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND	-0.3V to +5.5V
All other Pins to GND	-0.3V to (V_{CC} +0.25V)
I_{SET} to GND	-0.3V to +2.2V
RF Input Power (ATTN_IN+, ATTN_IN-) @G_{MAX}	+10 dBm
Continuous Power Dissipation	1.5W
θ_{JA} (Junction – Ambient)	+41°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+4°C/W
Operating Temperature Range (Case Temperature)	T_C = -40°C to +85°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s) .	+260°C

KEY FEATURE – NOISE FIGURE SLOPE

Standard Variable Gain amplifiers exhibit a [NF/Gain] slope of -1 dB/dB. Practically speaking, as gain is reduced, Noise Figure degrades dB for dB. The F1200 utilizes new technology that flattens the Noise Figure response (~ -0.16 dB/dB) for most of the gain control range while keeping distortion (Output IP3) constant. The result is that NF is improved up to 16 dB vs. a standard VGA at low gain settings. The graph below illustrates this by showing the IDTF1200 NF and IP3O vs. Gain setting contours.



IDTF1200 SPECIFICATION

V_{CC} = +5.0V, **f_{RF} = 100MHz**, T_C= +25°C, STBY = GND, R6 = **2.87K +/-1%,** P_{OUT} = +3 dBm, unless otherwise noted in the condition column. EVkit trace, transformer & matching losses are de-embedded for specification purposes (note: de-embedded losses = 0.4dB input and 0.4dB output at 100MHz).

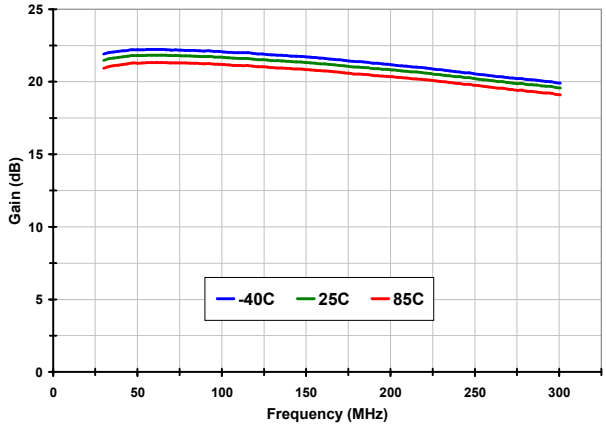
Parameter	Condition	Symbol	min	typ	max	units
Operating Temp. Range	Case Temperature Measured at the exposed paddle	T_C		-40 to +85		C
Logic Input High		V_{IH}	***2.0***[1]			V
Logic Input Low		V_{IL}			***0.8***	V
Logic Current		I_{IH}, I_{IL}	***-1***		***+1***	µA
Operating voltage range	Analog & Digital Supplies	V_{CC}		4.75 to 5.25		V
Supply Current	Total, All V_{CC}; R6= 2.87K +/-1%	I_{SUPP}	***103***	***110***	***117***	mA
Standby Current	Total, All V_{CC} ▪ All digital inputs at 2.0VDC ▪ VCC=5.25VDC	I_{STBY}			***2.5***	mA
Frequency Range	Output IP3 > +40 dBm	f_{RF}		50 to 160		MHz
Input Resistance	Differential	R_{IN}		200		Ω
Output Resistance	Differential	R_{OUT}		200		Ω
Maximum Gain	GC = [0000000]	G_{MAX}	***20.7***	***21.7***	***22.6***	dB
Minimum Gain	GC = [1011101]	G_{MIN}	***-2.8***	***-1.7***	***-0.7***	dB
Gain Step		LSB		0.25		dB
Phase Slope	ΔΦ due to change in gain	Φ_{SLOPE}		0.3		deg/dB
Differential Gain Error	Between adjacent 1dB steps	DNL		.05		dB
Integral Gain Error	Error vs. straight line	INL		+/-0.20		dB
Noise Figure	At Maximum Gain	NF		2.6		dB
Noise Figure	GC = [0110100] (gain = 9dB)	NF_{BACK}		4.55		dB
Output IP3	▪ Set code = 0000000, (G_{MAX}) ▪ Pout = +3 dBm per tone ▪ 800 KHz Tone Separation	$IP3_{O1}$		48		dBm
Output IP3 – at Gback	▪ Set code = 0110100, (Gain = 9dB) ▪ Pout = +3 dBm per tone ▪ 800 KHz Tone Separation	$IP3_{O2}$		44		dBm
Settling Time	▪ Gain Step from 22 to 21 dB setting ▪ Settles to within 0.1 dB of final value ▪ F_{RF} = 100 MHz	T_{1dB}		15[2]		nsec
2nd Harmonic	▪ Set code = 0000000, (G_{MAX}) ▪ Pout = +3 dBm	H2		-82		dBc
# Control Bits	Parallel	CB		7		#
1 dB Compression	▪ Set code = 0000000, (G_{MAX}) ▪ Single Tone Test	$P1dB_O$	***+16.7***	***+19.4***		dBm

1 –Items in ***bold italics*** are Guaranteed by Test

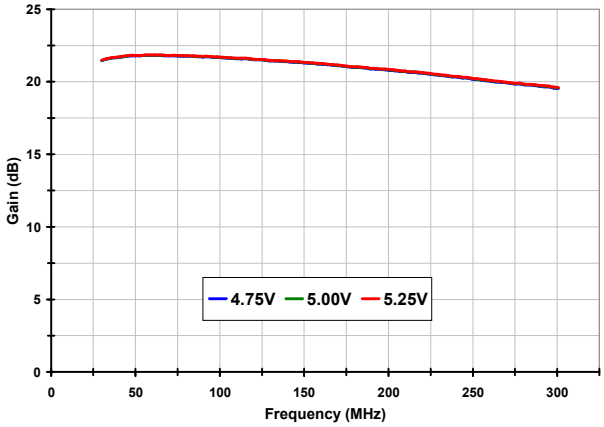
2 – See Graph on Page 8

TYPICAL OPERATING PARAMETRIC CURVES (G_{MAX}, 5.00V, 25C, P_{OUT} +3 dBm, 100MHz unless otherwise noted)

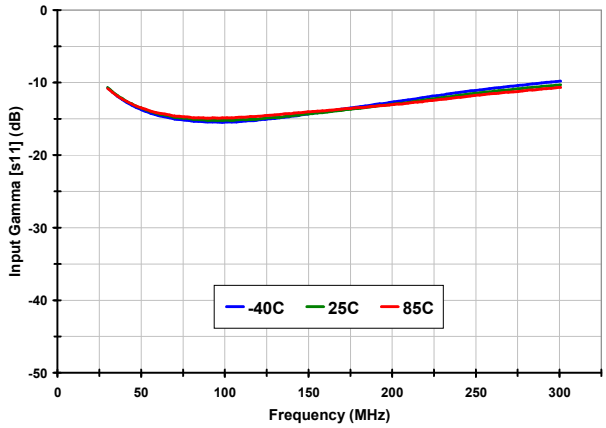
Gain vs. Temperature



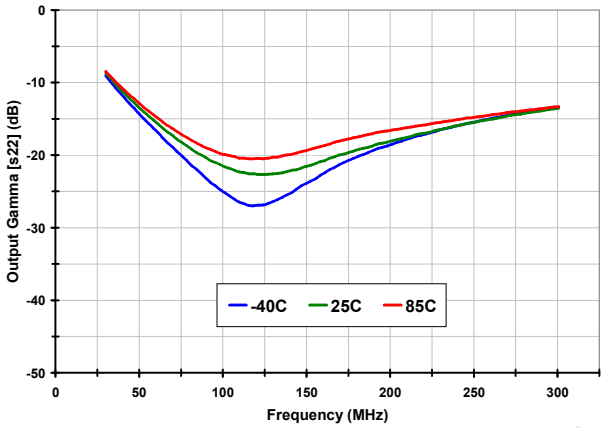
Gain vs. Voltage



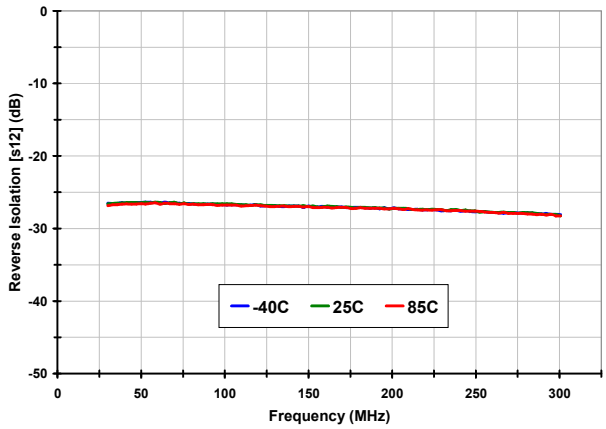
S11 vs. Temperature



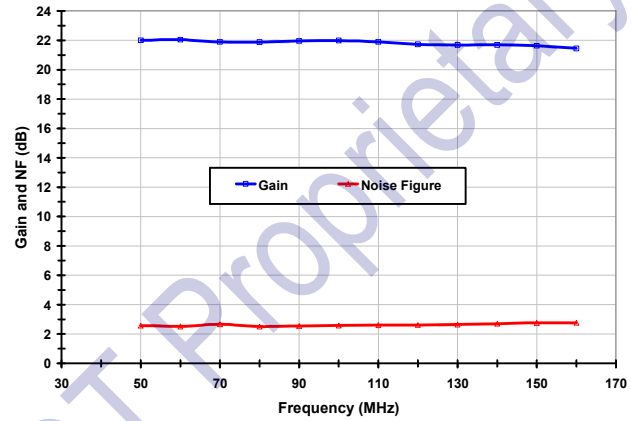
S22 vs. Temperature



S12 vs. Temperature

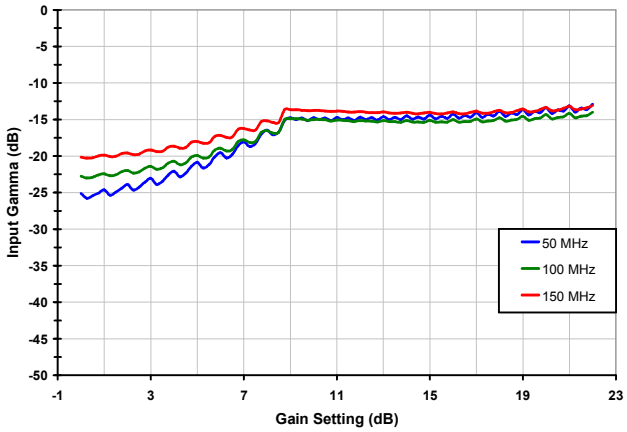


Gain and NF vs. Frequency (measured w/NF meter)

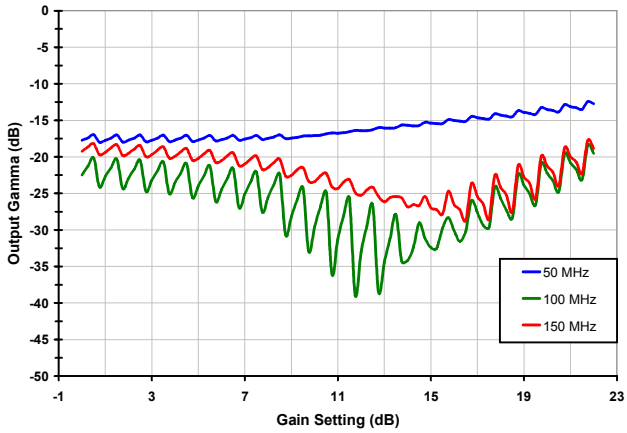


TOCs CONTINUED

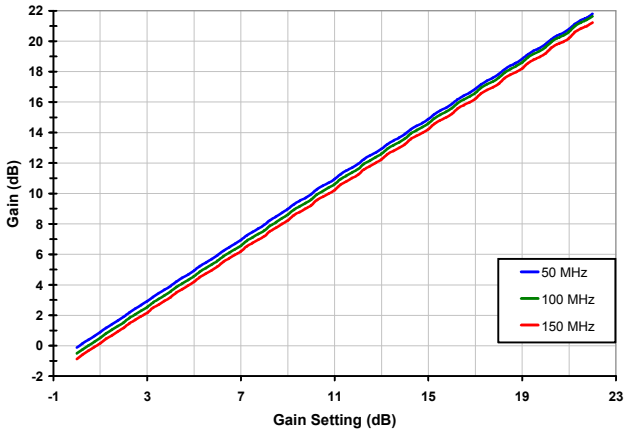
S11 vs. Gain Setting



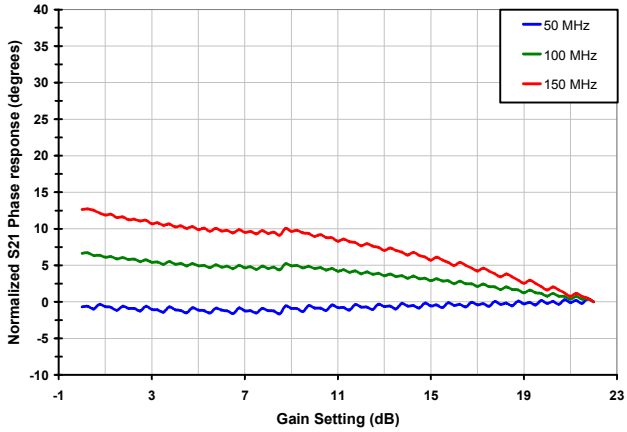
S22 vs. Gain Setting



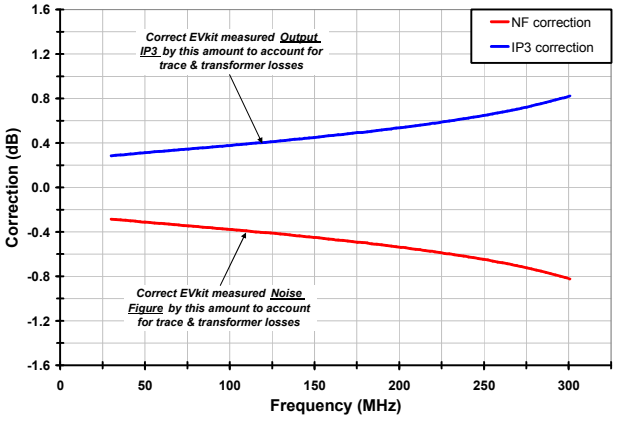
S21 vs. Gain Setting



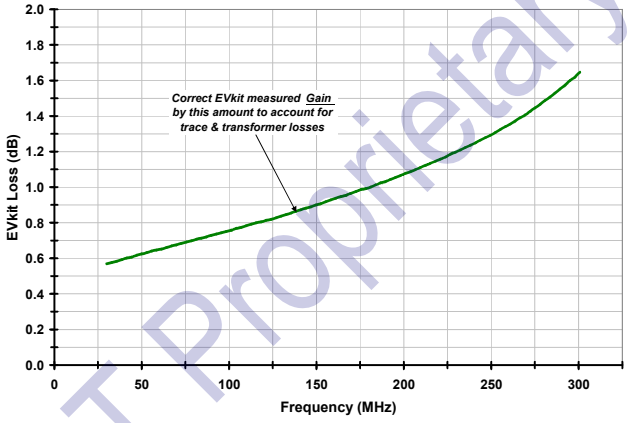
S21 Phase vs. Gain Setting



EVKit NF & Output IP3 Correction

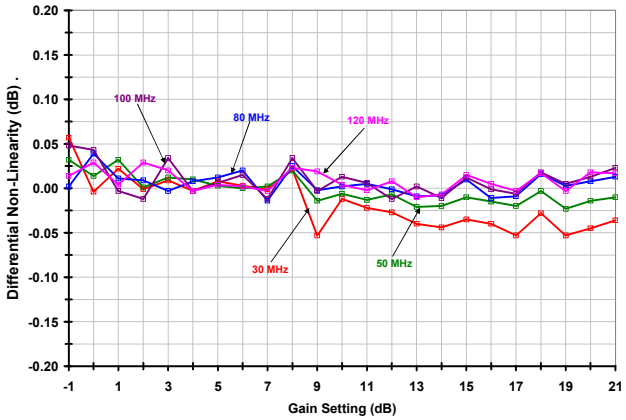


EVKit Gain Correction

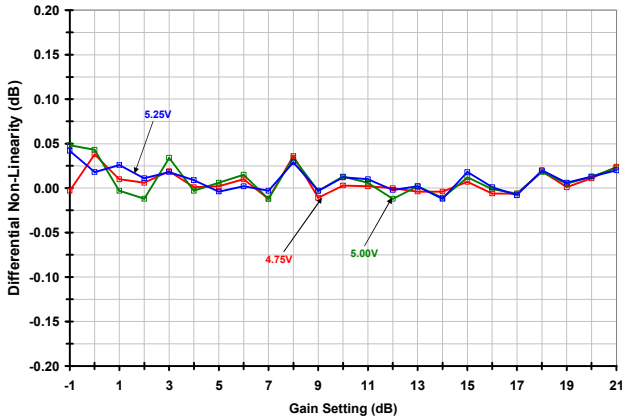


TOCs CONTINUED

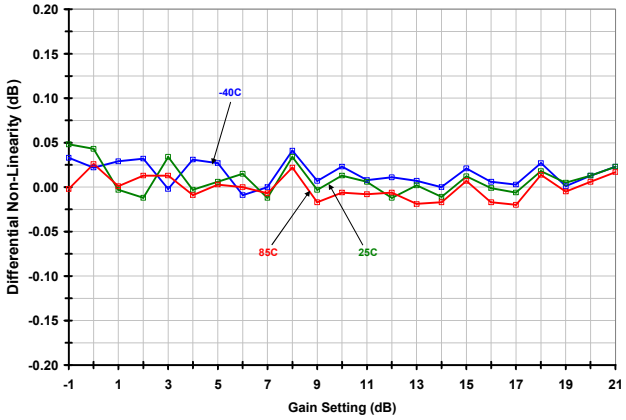
DNL vs. Frequency (1dB Steps)



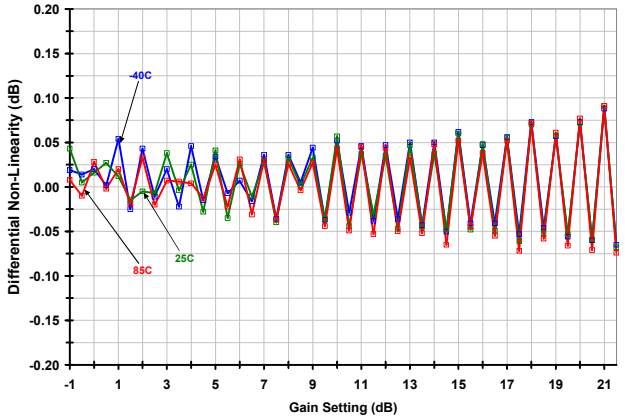
DNL vs. Voltage (100 MHz, 1dB Steps)



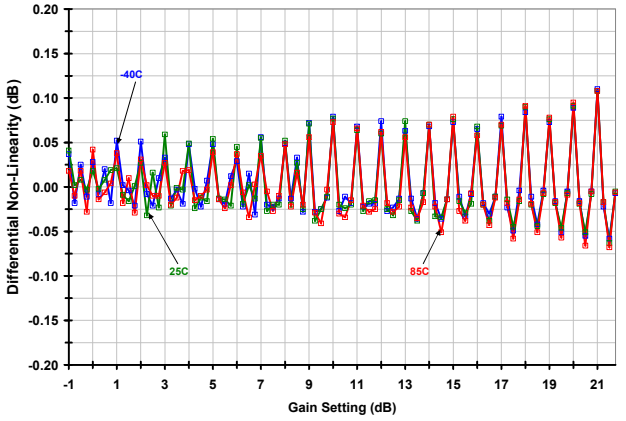
DNL vs. Temperature (100 MHz, 1dB Steps)



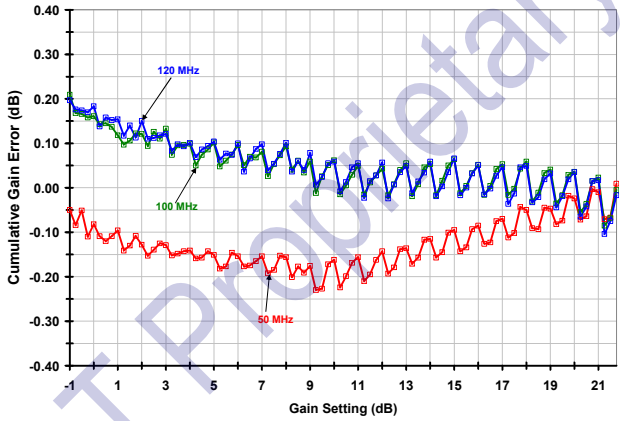
DNL vs. Temperature (100 MHz, 0.5dB Steps)



DNL vs. Temperature (100 MHz, 0.25dB Steps)

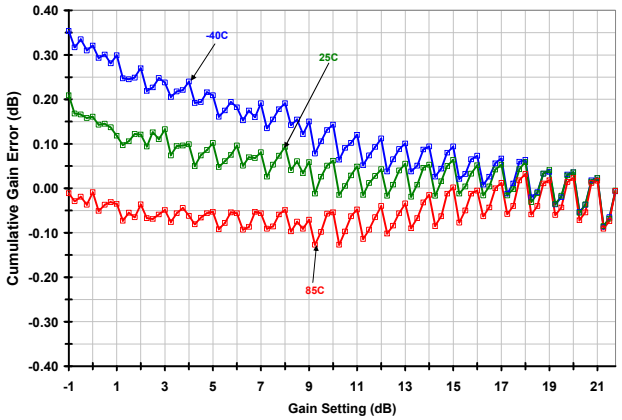


INL vs. Frequency

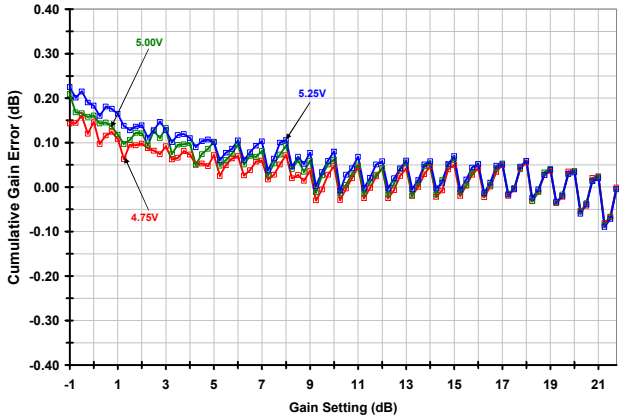


TOCs CONTINUED

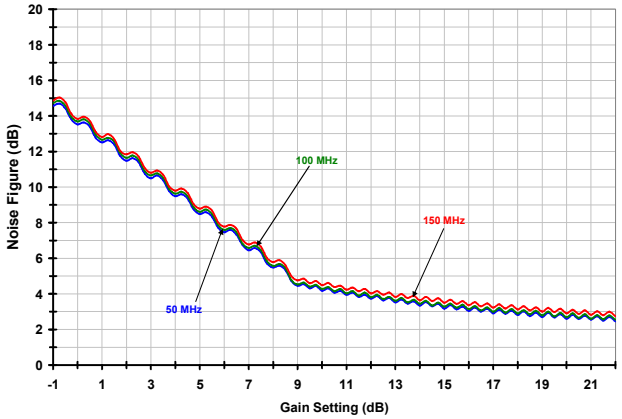
INL vs. Temperature (100 MHz)



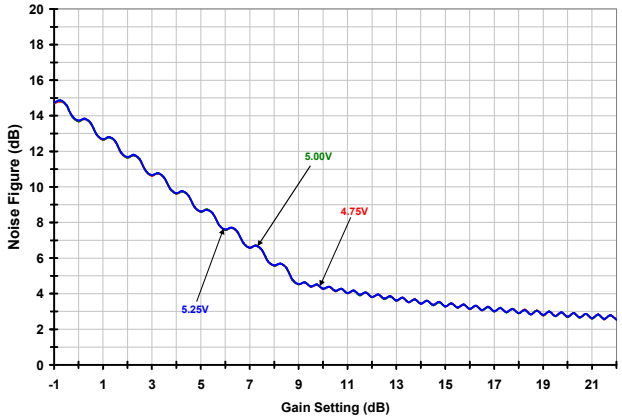
INL vs. Voltage (100 MHz)



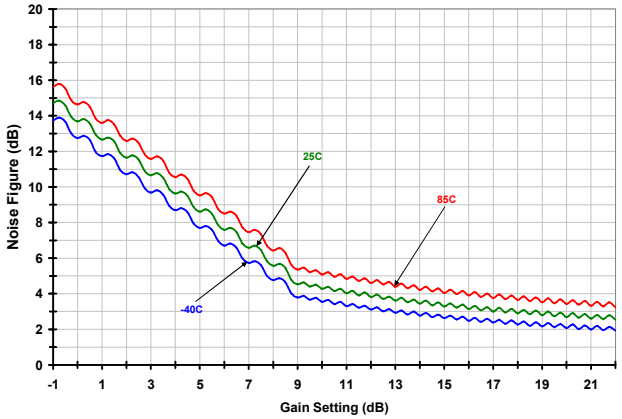
Noise Figure vs. Frequency



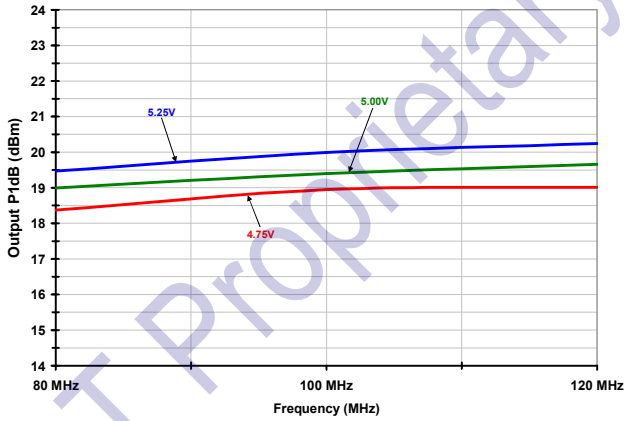
Noise Figure vs. Voltage (100 MHz)



Noise Figure vs. Temperature (100 MHz)

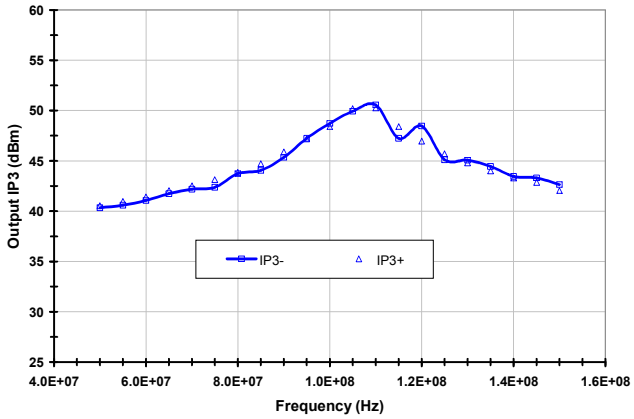


Output P1dB vs. Voltage

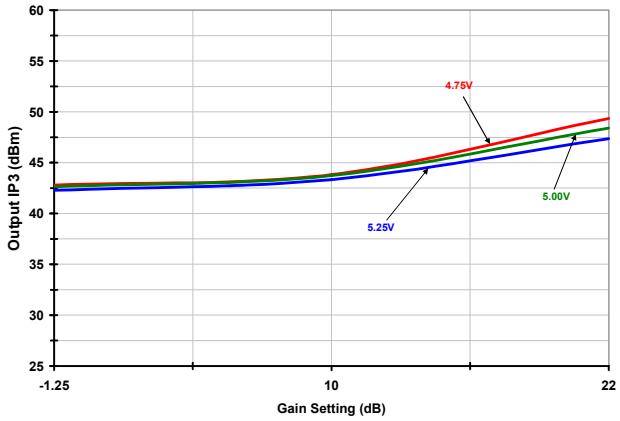


TOCs CONTINUED

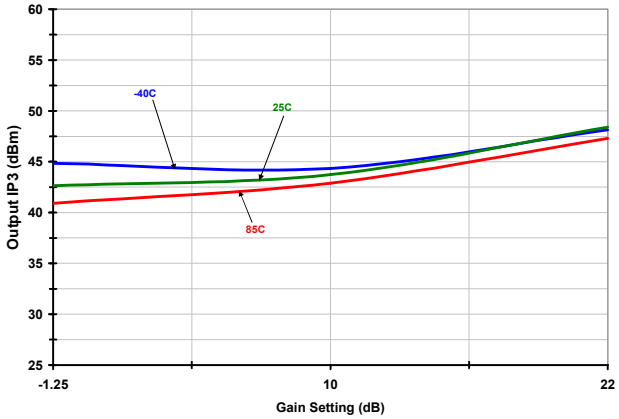
Output IP3 vs. Frequency



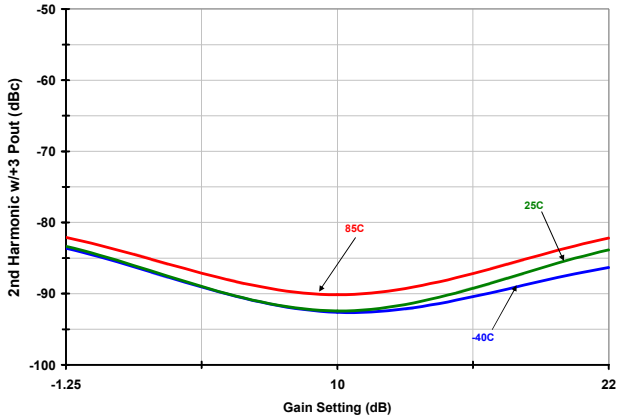
Output IP3 vs. Voltage (100 MHz)



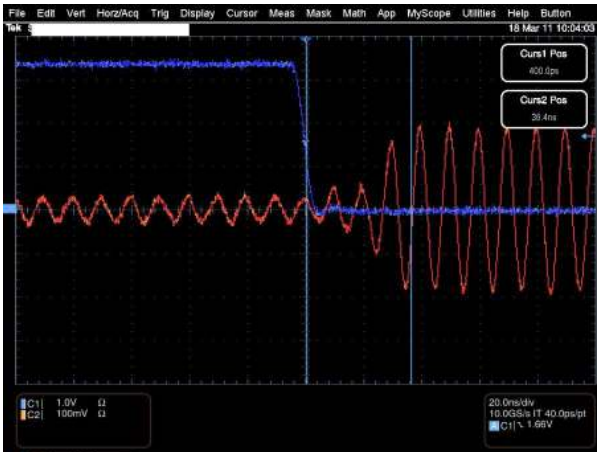
Output IP3 vs. Temperature (100 MHz)



2nd Harmonic vs. Temperature (100 MHz)



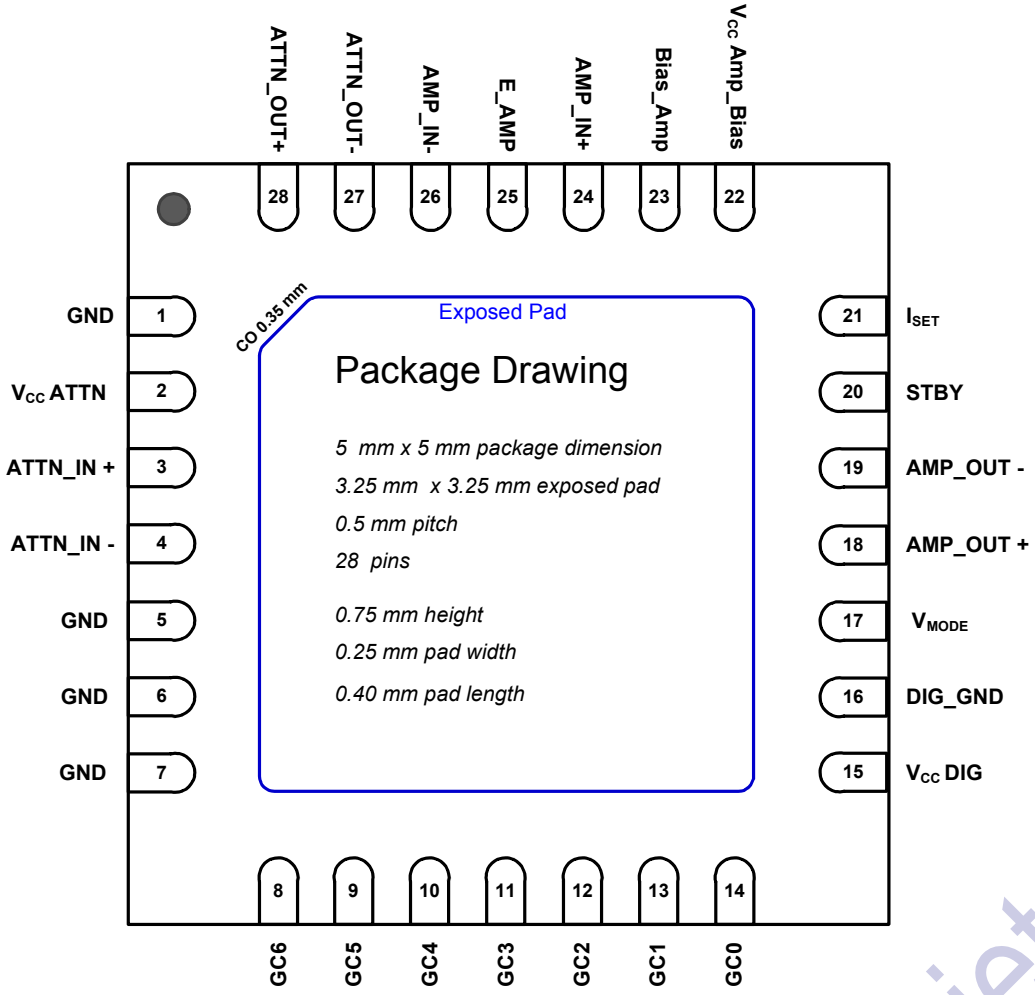
Settling Time (16dB Step, 100 MHz)



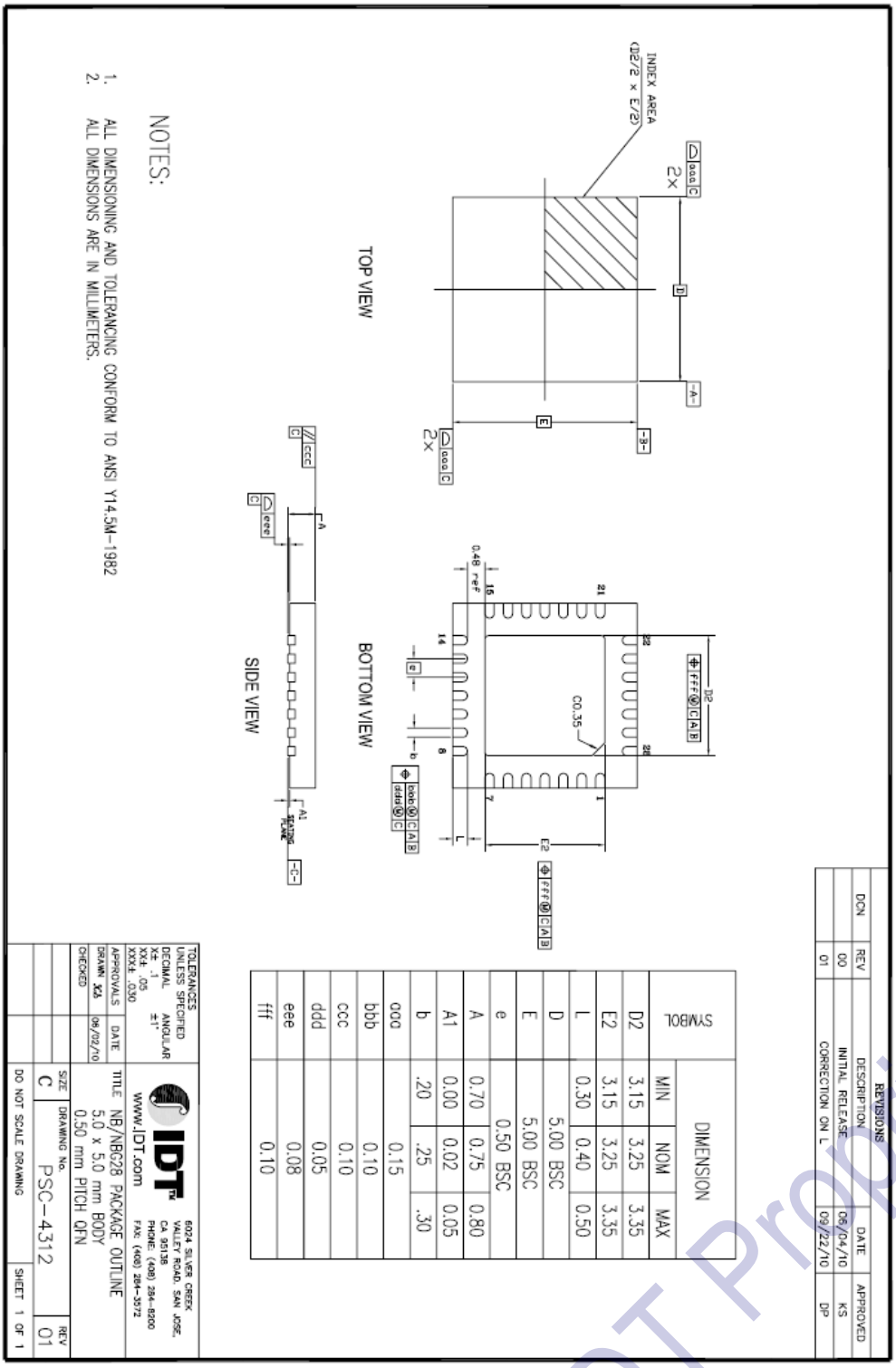
Settling Time (1 dB Step, 100 MHz)

PIN DIAGRAM

TOP View
(looking through the top of the package)



PACKAGE DRAWING

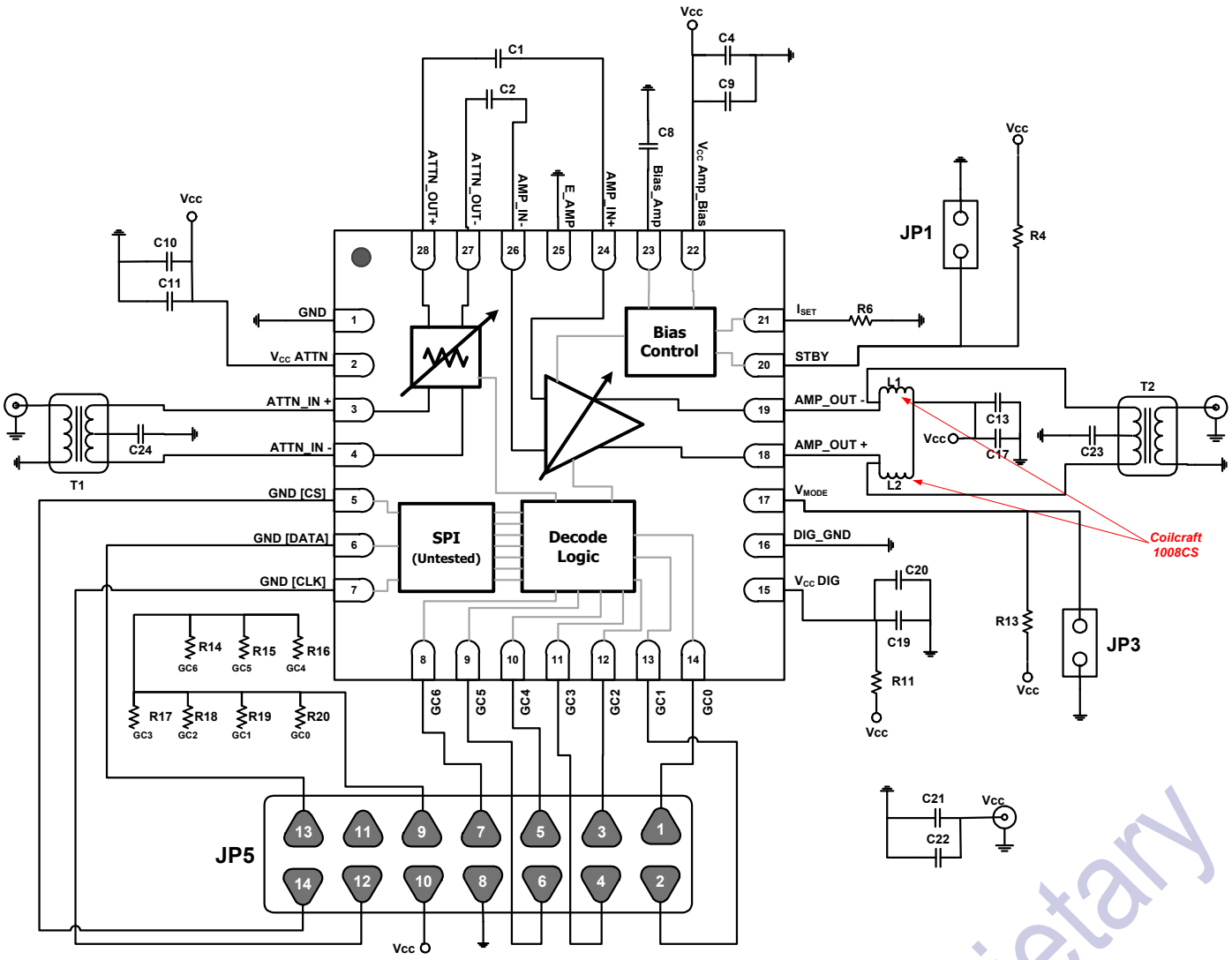


PIN DESCRIPTIONS

Pin #	Pin Name	Function
1	GND	
2	V_{CC}_ATTN	Attenuator Power Supply
3	ATTN_IN+	Attenuator_0 Differential Input P
4	ATTN_IN-	Attenuator_0 Differential Input M
5	Ground	Untested - SPI Chip Select Input
6	Ground	Untested - SPI Data Input
7	Ground	Untested - SPI Clock Input
8	GC6	Parallel Gain Control Input – MSB (16 dB step)
9	GC5	Parallel Gain Control Input
10	GC4	Parallel Gain Control Input
11	GC3	Parallel Gain Control Input
12	GC2	Parallel Gain Control Input
13	GC1	Parallel Gain Control Input
14	GC0	Parallel Gain Control Input – LSB (0.25 dB step)
15	V_{CC}_DIG	Digital Circuit Power Supply
16	DIG_GND	Connect directly to Ground
17	V_{MODE}	Untested – SPI Enable Connect to PCB GND for normal parallel operation
18	AMP_OUT+	Amplifier Differential Output P
19	AMP_OUT-	Amplifier Differential Output M
20	STBY	Amplifier Power Down. Ground for Normal operation
21	I_{SET}	Current Setting Resistor. Connect recommended value (2.87K) to ground. Use 1% tolerance
22	V_{CC}_Amp_Bias	Amplifier and Bias Circuit Power Supply
23	Bias_Amp	Amplifier Bias External Pin for Decoupling Capacitor
24	AMP_IN+	Amplifier Differential Input P
25	E_Amp	Amplifier Common Emitter
26	AMP_IN-	Amplifier Differential Input M
27	ATTN_OUT-	Attenuator_0 Differential Output M
28	ATTN_OUT+	Attenuator_0 Differential Output P
	Exposed Paddle	

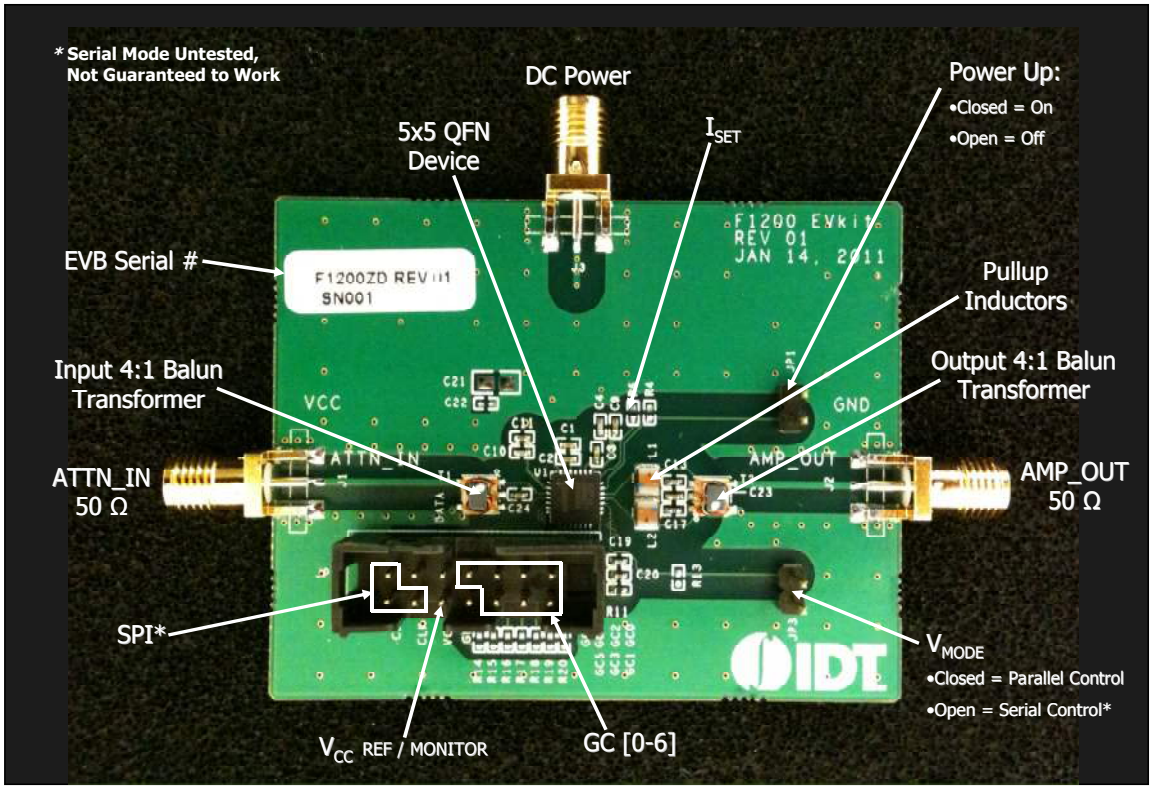
EVKIT / APPLICATIONS CIRCUIT SCHEMATIC

The diagram below describes the recommended applications / EVkit circuit:



EVKIT & BOM (Email: RFsupport@IDT.com to request Controller SW and Cable)

The picture and table below describes the recommended EVkit operation and BOM



Item #	Value	Size	Desc	Mfr. Part #	Mfr.	Ref Des
1	4:1 Balun	SM-22	4:1 Center Tap Balun	TC4-1TG2+	Mini Circuits	T1,T2
2	2.87k	0402	RES 2.87K OHM 1/10W 1% 0402 SMD	ERJ-2RKF2871X	Panasonic	R6
3	47k	0402	Pullup resistors for STBY and VMODE jumpers	RC0402FR-0747KL	Yageo	R4, R13
4	0	0402	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic	R11
5	680 nH	1008	RF inductor, ceramic core, 5% tol, SMT, RoHS	1008CS-681XJLC	Coilcraft	L1,L2
6	10 nF	0402	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01D	MURATA	C1,C2,C8,C23,C24
7	1000 pF	0402	CAP CER 1000PF 50V C0G 0402	GRM1555C1H102JA01D	MURATA	C4,C10,C13,C19
8	0.1uF	0402	CAP CER .1UF 10V 10% X5R 0402	GRM155R61A104KA01D	MURATA	C9,C11,C17,C20
9	SMA	.062	SMA_END_LAUNCH	142-0711-821	Emerson Johnson	J1,J2,J3
10	Header_2Pin	TH_2	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M	JP1,JP3
11	Header_14Pin	TH_7x2	CONN HEADER 14 POS STRGHT GOLD	N2514-6002-RB	3M	JP5
12	F1200ZD	QFN-28	IF VGA	Q01B005M	IDT	U1
13	PCB			F1200 EV Kit Rev 1		
14	DNP	0402	Resistors to ground on Gain ctrl lines			R14 thru R20

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

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