MC33502

1.0 V, Rail-to-Rail, Dual Operational Amplifier

The MC33502 operational amplifier provides rail−to−rail operation on both the input and output. The output can swing within 50 mV of each rail. This rail−to−rail operation enables the user to make full use of the entire supply voltage range available. It is designed to work at very low supply voltages (1.0 V and ground), yet can operate with a supply of up to 7.0 V and ground. Output current boosting techniques provide high output current capability while keeping the drain current of the amplifier to a minimum.

Features

- Low Voltage, Single Supply Operation (1.0 V and Ground to 7.0 V and Ground)
- High Input Impedance: Typically 40 fA Input Current
- Typical Unity Gain Bandwidth @ 5.0 V = 5.0 MHz, @ 1.0 V = 4.0 MHz
- High Output Current (I_{SC} = 40 mA @ 5.0 V, 13 mA @ 1.0 V)
- Output Voltage Swings within 50 mV of Both Rails @ 1.0 V
- Input Voltage Range Includes Both Supply Rails
- High Voltage Gain: 100 dB Typical @ 1.0 V
- No Phase Reversal on the Output for Over−Driven Input Signals
- Input Offset Trimmed to 0.5 mV Typical
- Low Supply Current (I_D = 1.2 mA/per Amplifier, Typical)
- 600 Ω Drive Capability
- Extended Operating Temperature Range (−40 to 105°C)
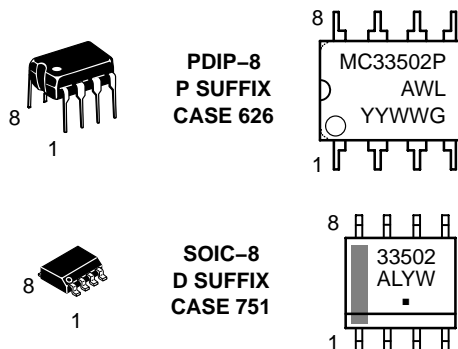- Pb−Free Packages are Available

Applications

- Single Cell NiCd/Ni MH Powered Systems
- Interface to DSP
- Portable Communication Devices
- Low Voltage Active Filters
- Telephone Circuits
- Instrumentation Amplifiers
- Audio Applications
- Power Supply Monitor and Control
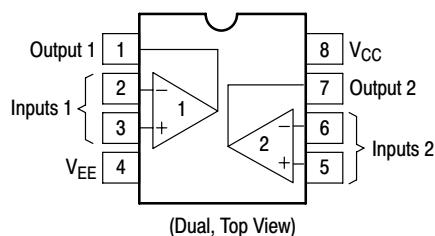- Compatible with VCX Logic

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS

PDIP−8
P SUFFIX
CASE 626

```
MC33502P
   AWL
 YYWWG
```

SOIC−8
D SUFFIX
CASE 751

```
33502
ALYW
  ▪
```

A   = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
▪ or G = Pb−Free Package

PIN CONNECTIONS

Output 1 — 1	8 — V$_{CC}$
Inputs 1 — 2, 3	7 — Output 2
V$_{EE}$ — 4	6, 5 — Inputs 2

(Dual, Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC33502P	PDIP−8	50 Units/Rail
MC33502PG	PDIP−8 (Pb−Free)	50 Units/Rail
MC33502D	SOIC−8	98 Units/Rail
MC33502DG	SOIC−8 (Pb−Free)	98 Units/Rail
MC33502DR2	SOIC−8	2500 Tape & Reel
MC33502DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC33502
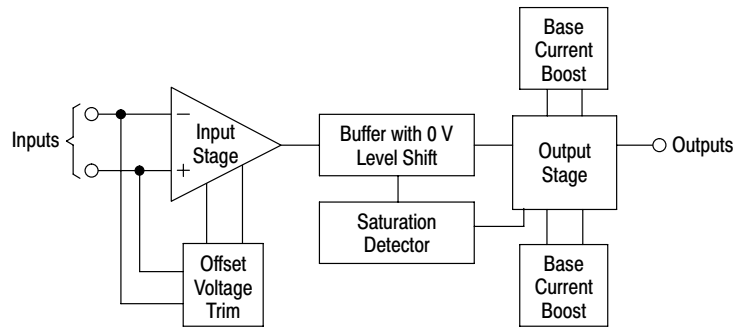
This device contains 98 active transistors per amplifier.

Figure 1. Simplified Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	7.0	V
ESD Protection Voltage at any Pin Human Body Model	V_{ESD}	2000	V
Voltage at Any Device Pin	V_{DP}	$V_S \pm 0.3$	V
Input Differential Voltage Range	V_{IDR}	V_{CC} to V_{EE}	V
Common Mode Input Voltage Range	V_{CM}	V_{CC} to V_{EE}	V
Output Short Circuit Duration	t_S	Note 1	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C
Maximum Power Dissipation	P_D	Note 1	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
2. ESD data available upon request.

MC33502

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{CM} = V_O = V_{CC}/2, R_L to V_{CC}/2, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit

Input Offset Voltage (V_{CM} = 0 to V_{CC})
  V_{CC} = 1.0 V
    T_A = 25°C
    T_A = −40° to 105°C
  V_{CC} = 3.0 V
    T_A = 25°C
    T_A = −40° to 105°C
  V_{CC} = 5.0 V
    T_A = 25°C
    T_A = −40° to 105°C
	V_{IO}	
		
		−5.0
		−7.0
		
		−5.0
		−7.0
		
		−5.0
		−7.0
			
			0.5
			−
			
			0.5
			−
			
			0.5
			−
				
				5.0
				7.0
				
				5.0
				7.0
				
				5.0
				7.0
					mV

Input Offset Voltage Temperature Coefficient (R_S = 50 Ω) T_A = −40° to 105°C	$\Delta V_{IO}/\Delta T$	−	8.0	−	μV/°C
Input Bias Current (V_{CC} = 1.0 to 5.0 V)	I I_{IB} I	−	0.00004	10	nA
Common Mode Input Voltage Range	V_{ICR}	V_{EE}	−	V_{CC}	V

Large Signal Voltage Gain
  V_{CC} = 1.0 V (T_A = 25°C)
    R_L = 10 kΩ
    R_L = 1.0 kΩ
  V_{CC} = 3.0 V (T_A = 25°C)
    R_L = 10 kΩ
    R_L = 1.0 kΩ
  V_{CC} = 5.0 V (T_A = 25°C)
    R_L = 10 kΩ
    R_L = 1.0 kΩ
	A_{VOL}	
		
		25
		5.0
		
		50
		25
		
		50
		25
			
			100
			50
			
			500
			100
			
			500
			200
				
				−
				−
				
				−
				−
				
				−
				−
					kV/V

Output Voltage Swing, High (V_{ID} = ±0.2 V)
  V_{CC} = 1.0 V (T_A = 25°C)
    R_L = 10 kΩ
    R_L = 600 Ω
  V_{CC} = 1.0 V (T_A = −40° to 105°C)
    R_L = 10 kΩ
    R_L = 600 Ω
  V_{CC} = 3.0 V (T_A = 25°C)
    R_L = 10 kΩ
    R_L = 600 Ω
  V_{CC} = 3.0 V (T_A = −40° to 105°C)
    R_L = 10 kΩ
    R_L = 600 Ω
  V_{CC} = 5.0 V (T_A = 25°C)
    R_L = 10 kΩ
    R_L = 600 Ω
  V_{CC} = 5.0 V (T_A = −40° to 105°C)
    R_L = 10 kΩ
    R_L = 600 Ω
	V_{OH}	
		
		0.9
		0.85
		
		0.85
		0.8
		
		2.9
		2.8
		
		2.85
		2.75
		
		4.9
		4.75
		
		4.85
		4.7
			
			0.95
			0.88
			
			−
			−
			
			2.93
			2.84
			
			−
			−
			
			4.92
			4.81
			
			−
			−
				
				−
				−
				
				−
				−
				
				−
				−
				
				−
				−
				
				−
				−
				
				−
				−
					V

MC33502

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ V, $V_{EE} = 0$ V, $V_{CM} = V_O = V_{CC}/2$, R_L to $V_{CC}/2$, $T_A = 25°C$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage Swing, Low ($V_{ID} = \pm0.2$ V)	V_{OL}				V
$V_{CC} = 1.0$ V ($T_A = 25°C$)					
$R_L = 10$ kΩ		0.05	0.02	–	
$R_L = 600$ Ω		0.1	0.05	–	
$V_{CC} = 1.0$ V ($T_A = -40°$ to $105°C$)					
$R_L = 10$ kΩ		0.1	–	–	
$R_L = 600$ Ω		0.15	–	–	
$V_{CC} = 3.0$ V ($T_A = 25°C$)					
$R_L = 10$ kΩ		0.05	0.02	–	
$R_L = 600$ Ω		0.1	0.08	–	
$V_{CC} = 3.0$ V ($T_A = -40°$ to $105°C$)					
$R_L = 10$ kΩ		0.1	–	–	
$R_L = 600$ Ω		0.15	–	–	
$V_{CC} = 5.0$ V ($T_A = 25°C$)					
$R_L = 10$ kΩ		0.05	0.02	–	
$R_L = 600$ Ω		0.15	0.1	–	
$V_{CC} = 5.0$ V ($T_A = -40°$ to $105°C$)					
$R_L = 10$ kΩ		0.1	–	–	
$R_L = 600$ Ω		0.2	–	–	
Common Mode Rejection ($V_{in} = 0$ to 5.0 V)	CMR	60	75	–	dB
Power Supply Rejection $V_{CC}/V_{EE} = 5.0$ V/Ground to 3.0 V/Ground	PSR	60	75	–	dB
Output Short Circuit Current (V_{in} Diff $= \pm1.0$ V)	I_{SC}				mA
$V_{CC} = 1.0$ V					
Source		6.0	13	26	
Sink		10	13	26	
$V_{CC} = 3.0$ V					
Source		15	32	60	
Sink		40	64	140	
$V_{CC} = 5.0$ V					
Source		20	40	140	
Sink		40	70	140	
Power Supply Current (Per Amplifier, $V_O = 0$ V)	I_D				mA
$V_{CC} = 1.0$ V		–	1.2	1.75	
$V_{CC} = 3.0$ V		–	1.5	2.0	
$V_{CC} = 5.0$ V		–	1.65	2.25	
$V_{CC} = 1.0$ V ($T_A = -40$ to $105°C$)		–	–	2.0	
$V_{CC} = 3.0$ V ($T_A = -40$ to $105°C$)		–	–	2.25	
$V_{CC} = 5.0$ V ($T_A = -40$ to $105°C$)		–	–	2.5	

MC33502

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{CM} = V_O = $V_{CC}/2$, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit

Slew Rate (V_S = ±2.5 V, V_O = −2.0 to 2.0 V, R_L = 2.0 kΩ, A_V = 1.0)
  Positive Slope
  Negative Slope
	SR	
		2.0
		2.0
			
			3.0
			3.0
				
				6.0
				6.0
					V/μs

Gain Bandwidth Product (f = 100 kHz)
  V_{CC} = 0.5 V, V_{EE} = −0.5 V
  V_{CC} = 1.5 V, V_{EE} = −1.5 V
  V_{CC} = 2.5 V, V_{EE} = −2.5 V
	GBW	
		3.0
		3.5
		4.0
			
			4.0
			4.5
			5.0
				
				6.0
				7.0
				8.0
					MHz

Gain Margin (R_L =10 kΩ, C_L = 0 pF)	Am	–	6.5	–	dB
Phase Margin (R_L = 10 kΩ, C_L = 0 pF)	ϕ_m	–	60	–	Deg
Channel Separation (f = 1.0 Hz to 20 kHz, R_L = 600 Ω)	CS	–	120	–	dB
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 1.0 kΩ, THD ≤1.0%)	BW_P	–	200	–	kHz

Total Harmonic Distortion (V_O = 4.5 V_{pp}, R_L = 600 Ω, A_V = 1.0)
  f = 1.0 kHz
  f = 10 kHz
	THD	
		–
		–
			
			0.004
			0.01
				
				–
				–
					%

Differential Input Resistance (V_{CM} = 0 V)	R_{in}	–	>1.0	–	terraΩ
Differential Input Capacitance (V_{CM} = 0 V)	C_{in}	–	2.0	–	pF

Equivalent Input Noise Voltage (V_{CC} = 1.0 V, V_{CM} = 0 V, V_{EE} = Gnd,
  R_S = 100 Ω)
  f = 1.0 kHz
	e_n	
		
		–
			
			30
				
				–
					nV/√Hz
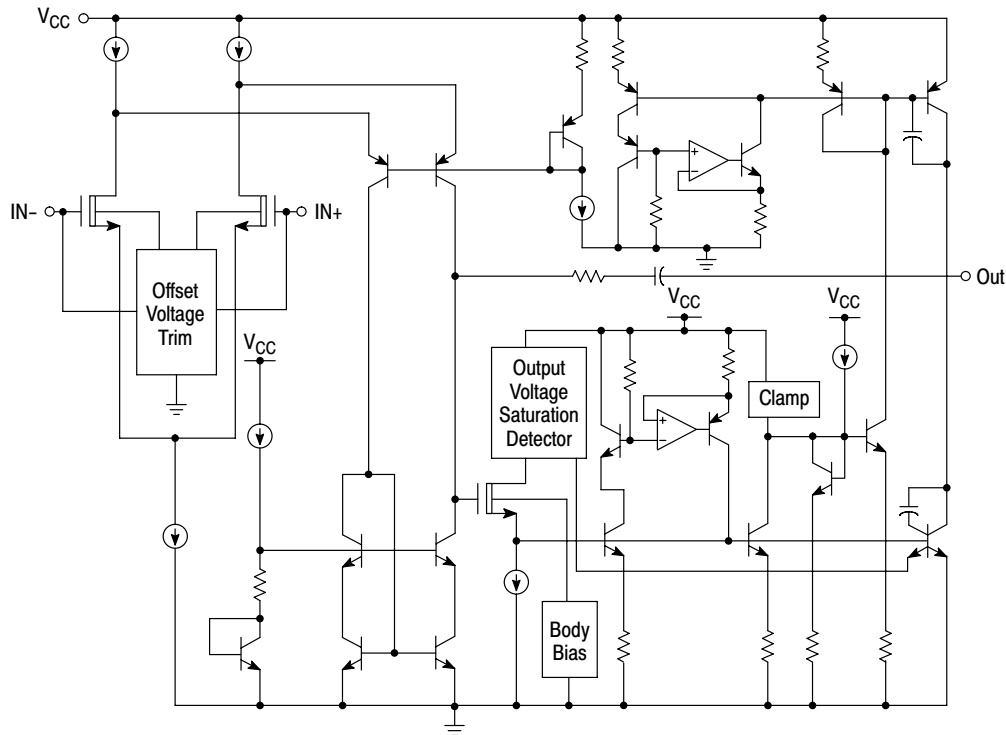
Figure 2. Representative Block Diagram

General Information

The MC33502 dual operational amplifier is unique in its ability to provide 1.0 V rail–to–rail performance on both the input and output by using a SMARTMOS™ process. The amplifier output swings within 50 mV of both rails and is able to provide 50 mA of output drive current with a 5.0 V supply, and 10 mA with a 1.0 V supply. A 5.0 MHz bandwidth and a slew rate of 3.0 V/μs is achieved with high speed depletion mode NMOS (DNMOS) and vertical PNP transistors. This device is characterized over a temperature range of −40°C to 105°C.

Circuit Information
Input Stage

One volt rail–to–rail performance is achieved in the MC33502 at the input by using a single pair of depletion mode NMOS devices (DNMOS) to form a differential amplifier with a very low input current of 40 fA. The normal input common mode range of a DNMOS device, with an ion implanted negative threshold, includes ground and relies on the body effect to dynamically shift the threshold to a positive value as the gates are moved from ground towards the positive supply. Because the device is manufactured in a p–well process, the body effect coefficient is sufficiently large to ensure that the input stage will remain substantially saturated when the inputs are at the positive rail. This also applies at very low supply voltages. The 1.0 V rail–to–rail input stage consists of a DNMOS differential amplifier, a folded cascode, and a low voltage balanced mirror. The low voltage cascoded balanced mirror provides high 1st stage gain and base current cancellation without sacrificing signal integrity. Also, the input offset voltage is trimmed to less than 1.0 mV because of the limited available supply voltage. The body voltage of the input DNMOS differential pair is internally trimmed to minimize the input offset voltage. A common mode feedback path is also employed to enable the offset voltage to track over the input common mode voltage. The total operational amplifier quiescent current drop is 1.3 mA/amp.

Output Stage

An additional feature of this device is an "on demand" base current cancellation amplifier. This feature provides base drive to the output power devices by making use of a buffer amplifier to perform a voltage–to–current conversion. This is done in direct proportion to the load conditions. This "on demand" feature allows these amplifiers to consume only a few micro–amps of current when the output stage is in its quiescent mode. Yet it provides high output current when required by the load. The rail–to–rail output stage current boost circuit provides 50 mA of output current with a 5.0 V supply (For a 1.0 V supply output stage will do 10 mA) enabling the operational amplifier to drive a 600 Ω load. A buffer is necessary to isolate the load current effects in the output stage from the input stage. Because of the low voltage conditions, a DNMOS follower is used to provide an essentially zero voltage level shift. This buffer isolates any load current changes on the output stage from loading the input stage. A high speed vertical PNP transistor provides excellent frequency performance while sourcing current. The operational amplifier is also internally compensated to provide a phase margin of 60 degrees. It has a unity gain of 5.0 MHz with a 5.0 V supply and 4.0 MHz with a 1.0 V supply.

Low Voltage Operation

The MC33502 will operate at supply voltages from 0.9 to 7.0 V and ground. When using the MC33502 at supply voltages of less than 1.2 V, input offset voltage may increase slightly as the input signal swings within approximately 50 mV of the positive supply rail. This effect occurs only for supply voltages below 1.2 V, due to the input depletion mode MOSFETs starting to transition between the saturated to linear region, and should be considered when designing high side dc sensing applications operating at the positive supply rail. Since the device is rail–to–rail on both input and output, high dynamic range single battery cell applications are now possible.
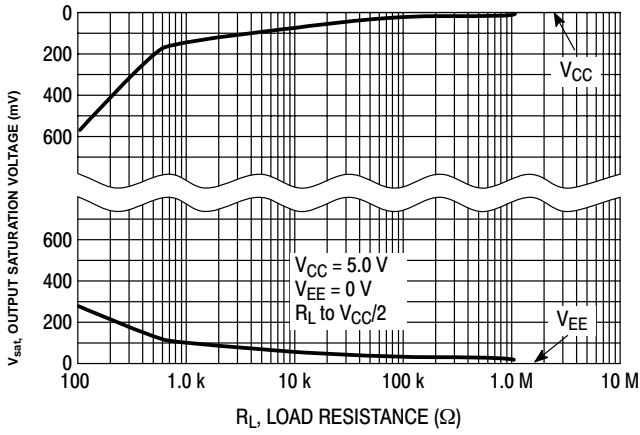
Figure 3. Output Saturation versus Load Resistance
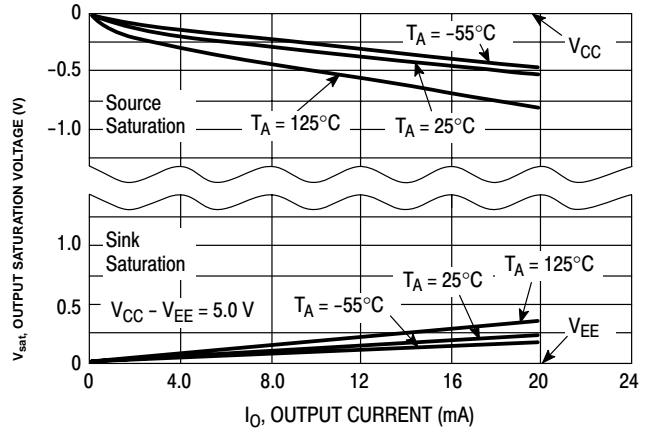
Figure 4. Drive Output Source/Sink Saturation Voltage versus Load Current
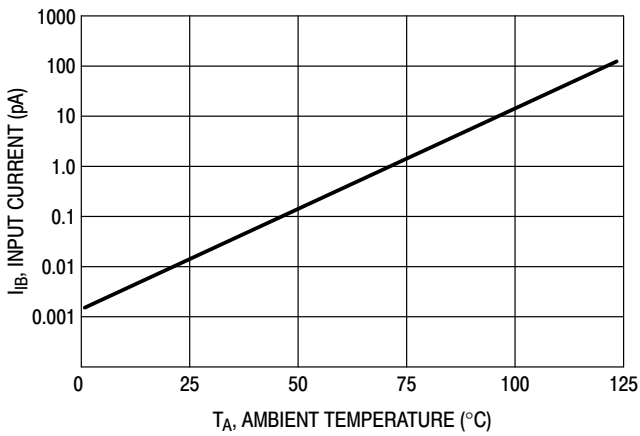
Figure 5. Input Current versus Temperature
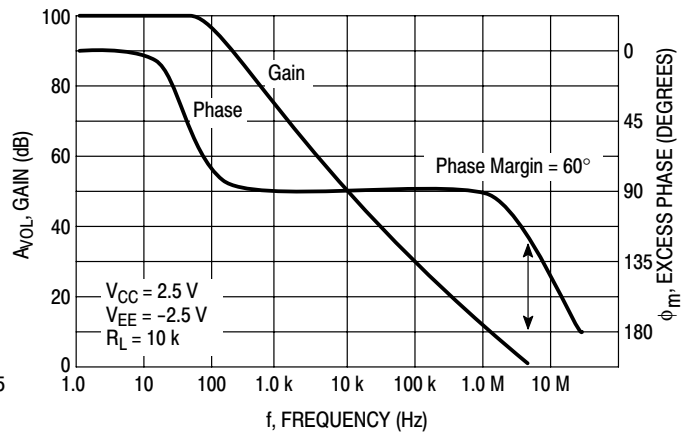
Figure 6. Gain and Phase versus Frequency

t, TIME (500 μs/DIV)
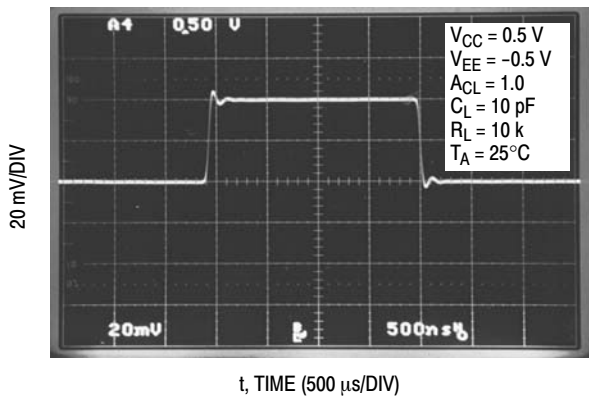
Figure 7. Transient Response
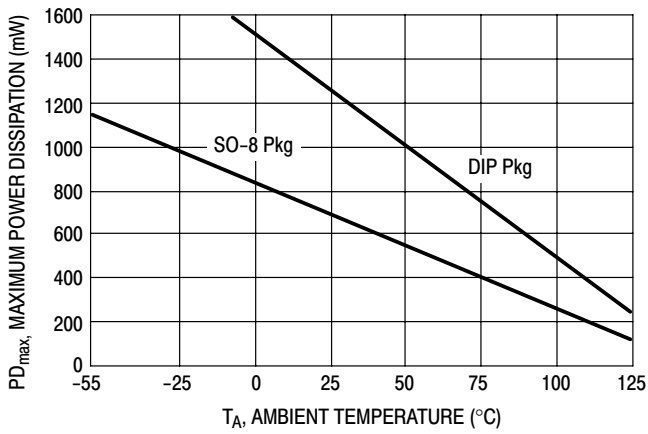

t, TIME (1.0 μs/DIV)
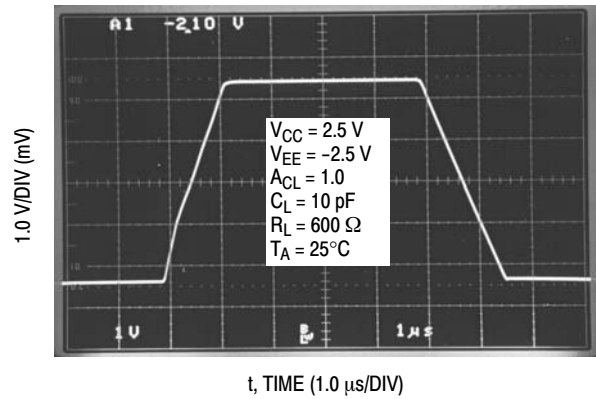
Figure 8. Slew Rate

**Figure 9. Maximum Power Dissipation
versus Temperature**
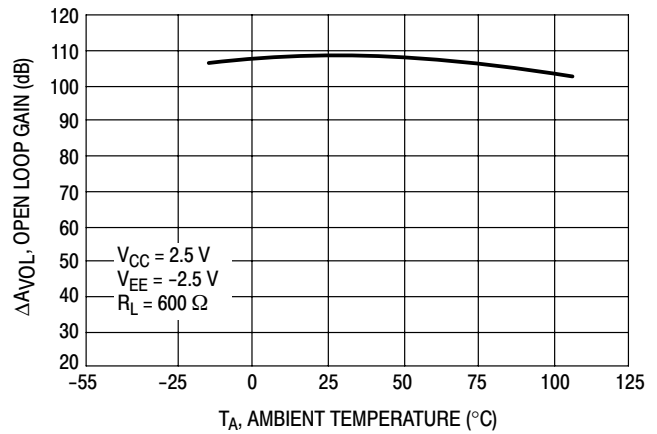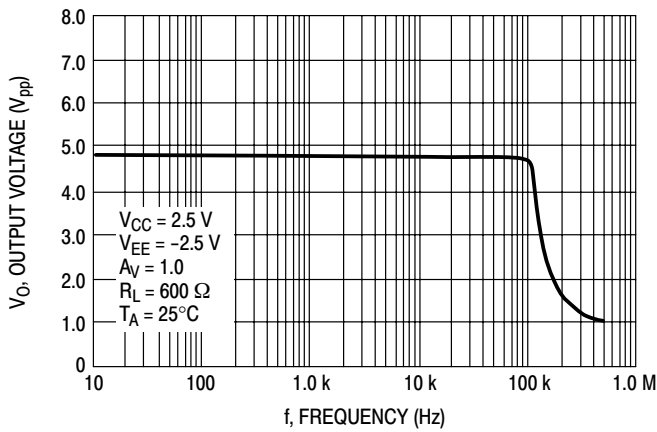

**Figure 10. Open Loop Voltage Gain
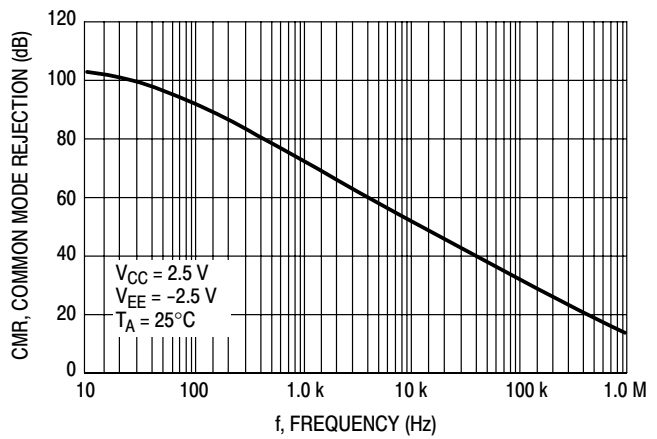versus Temperature**

Figure 11. Output Voltage versus Frequency

**Figure 12. Common Mode Rejection
versus Frequency**
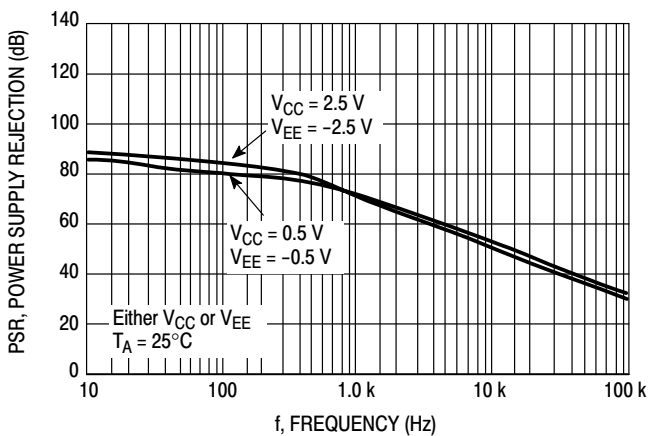
**Figure 13. Power Supply Rejection
versus Frequency**
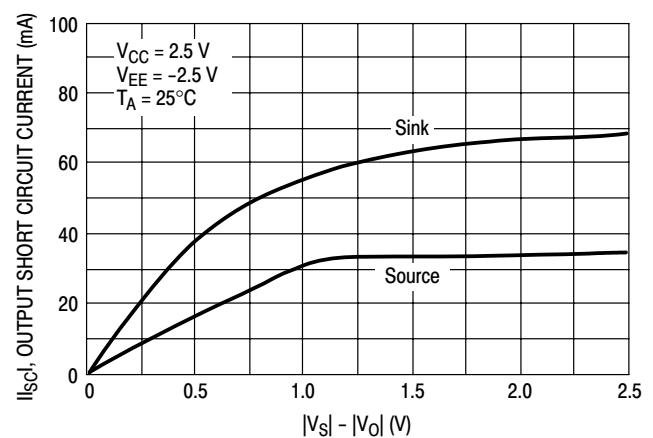
**Figure 14. Output Short Circuit Current
versus Output Voltage**
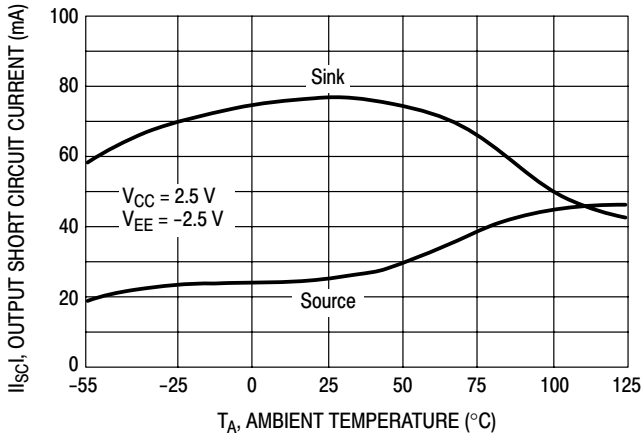
**Figure 15. Output Short Circuit Current
versus Temperature**
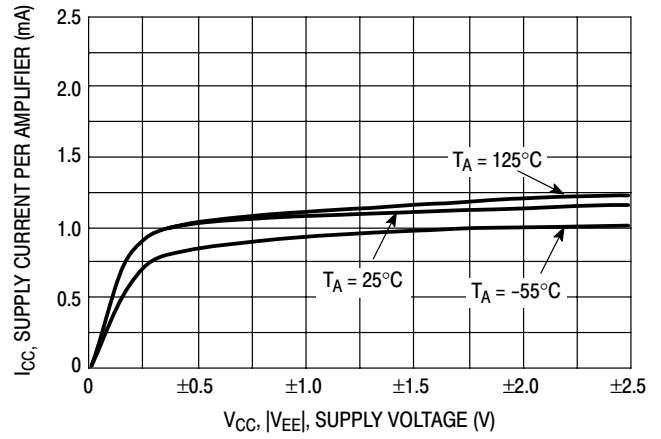
**Figure 16. Supply Current per Amplifier
versus Supply Voltage with No Load**
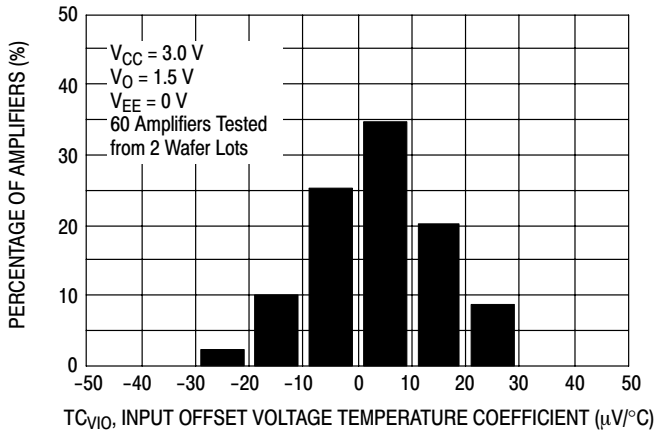
**Figure 17. Input Offset Voltage
Temperature Coefficient Distribution**
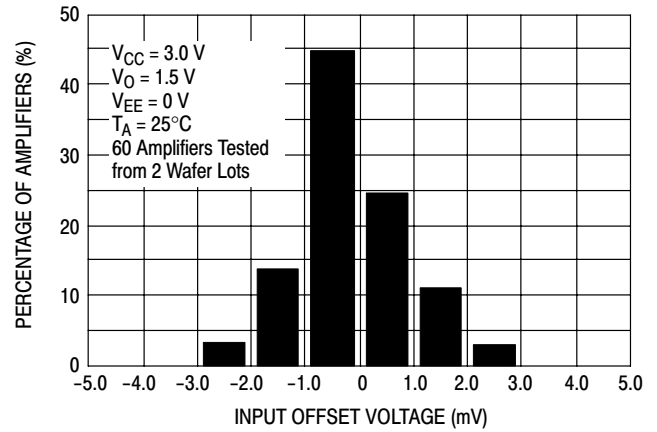
Figure 18. Input Offset Voltage Distribution
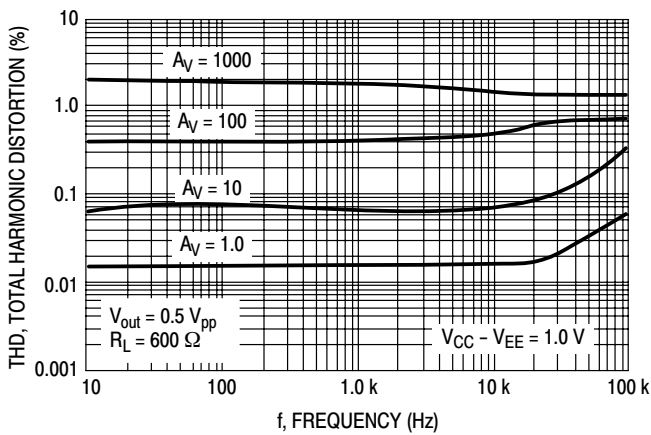
**Figure 19. Total Harmonic Distortion
versus Frequency with 1.0 V Supply**
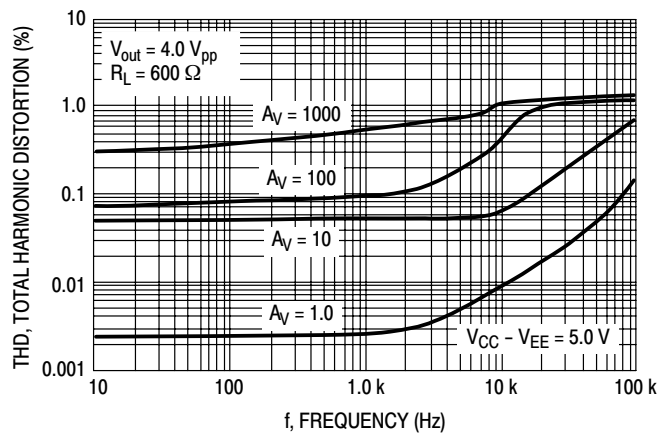
**Figure 20. Total Harmonic Distortion
versus Frequency with 5.0 V Supply**

MC33502
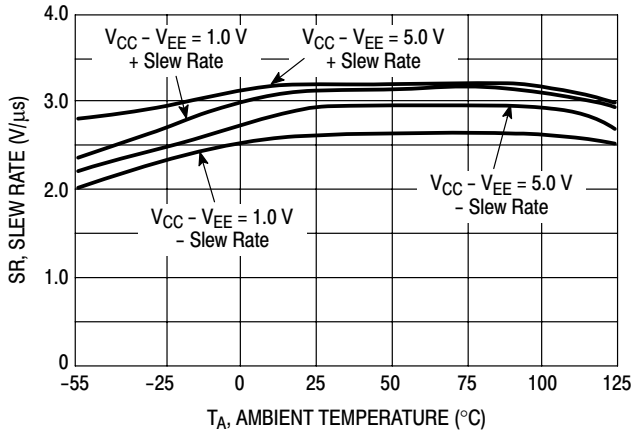
Figure 21. Slew Rate versus Temperature
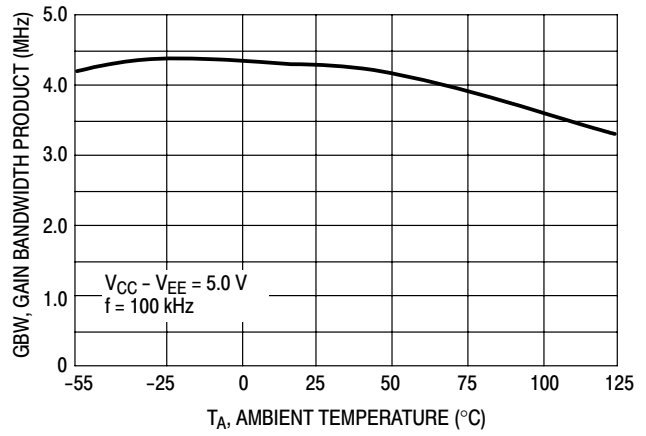
Figure 22. Gain Bandwidth Product versus Temperature
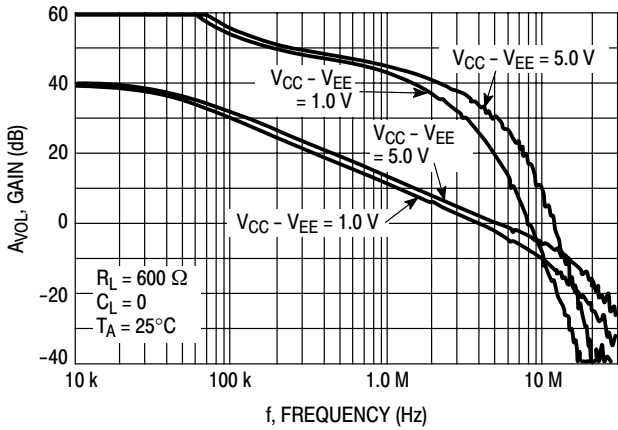
Figure 23. Voltage Gain and Phase versus Frequency
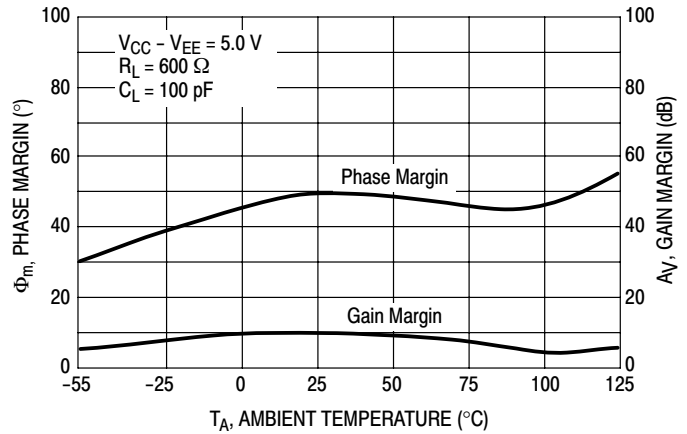
Figure 24. Gain and Phase Margin versus Temperature
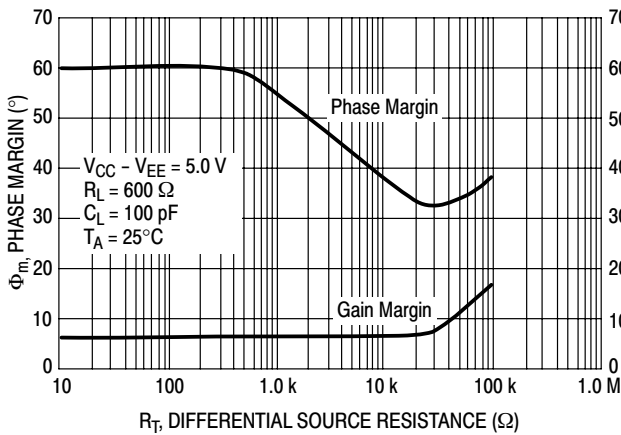
Figure 25. Gain and Phase Margin versus Differential Source Resistance
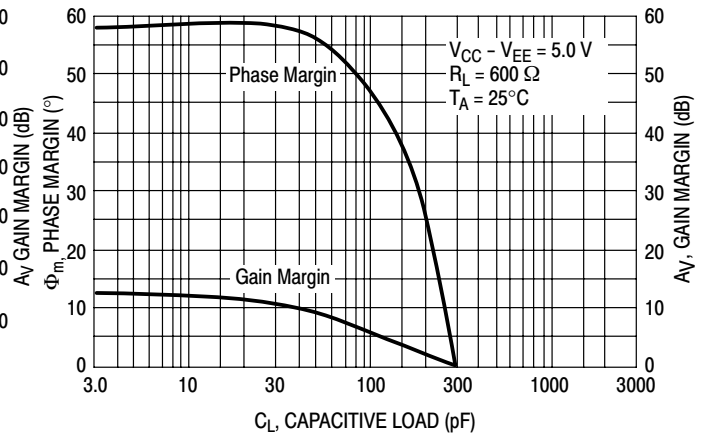
Figure 26. Feedback Loop Gain and Phase versus Capacitive Load
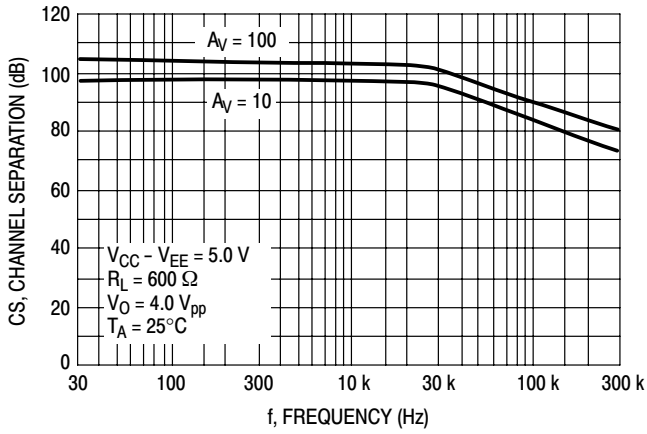
**Figure 27. Channel Separation
versus Frequency**
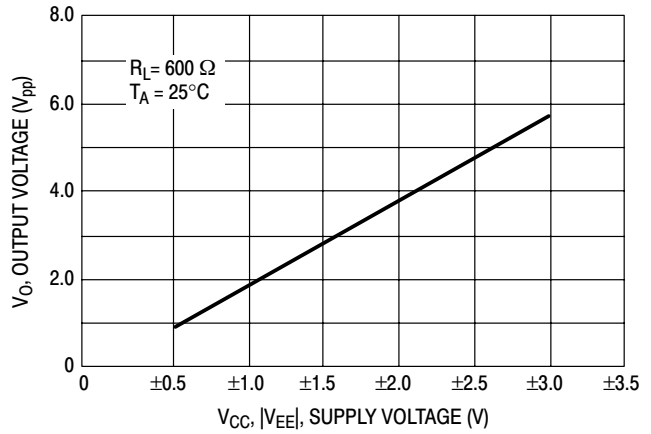
**Figure 28. Output Voltage Swing
versus Supply Voltage**
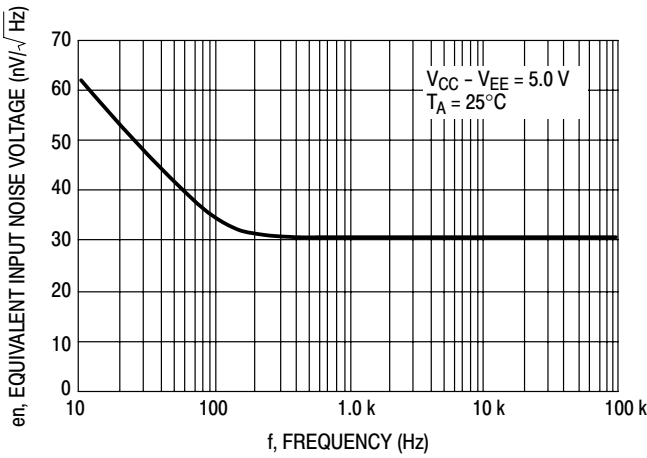
**Figure 29. Equivalent Input Noise Voltage
versus Frequency**
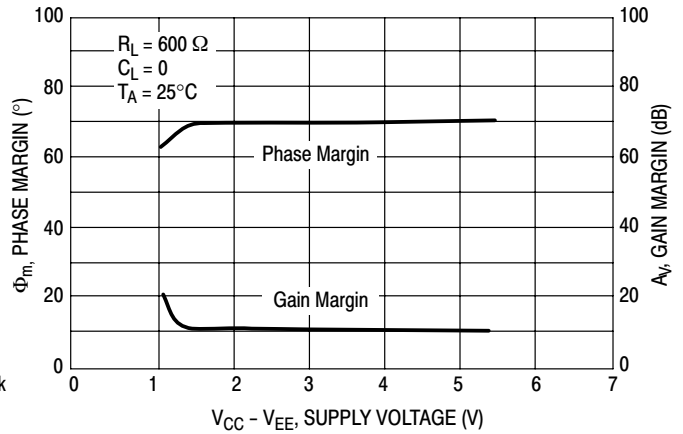
**Figure 30. Gain and Phase Margin
versus Supply Voltage**
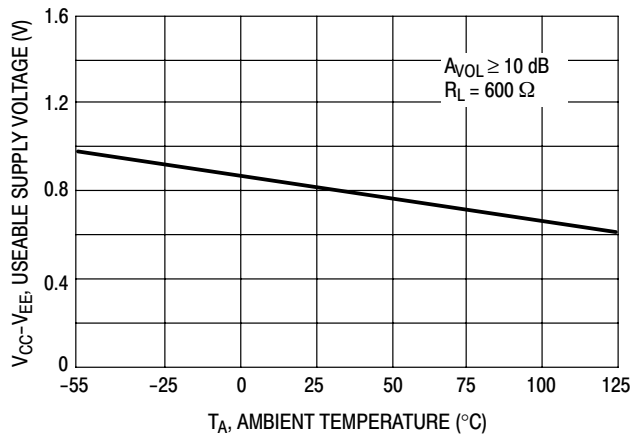
**Figure 31. Useable Supply Voltage
versus Temperature**
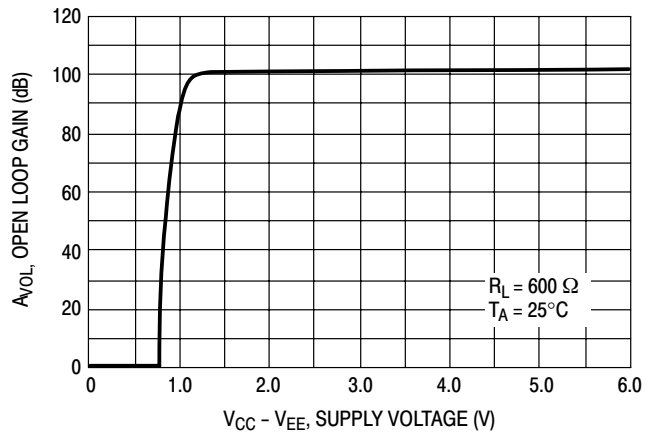
**Figure 32. Open Loop Gain
versus Supply Voltage**

MC33502
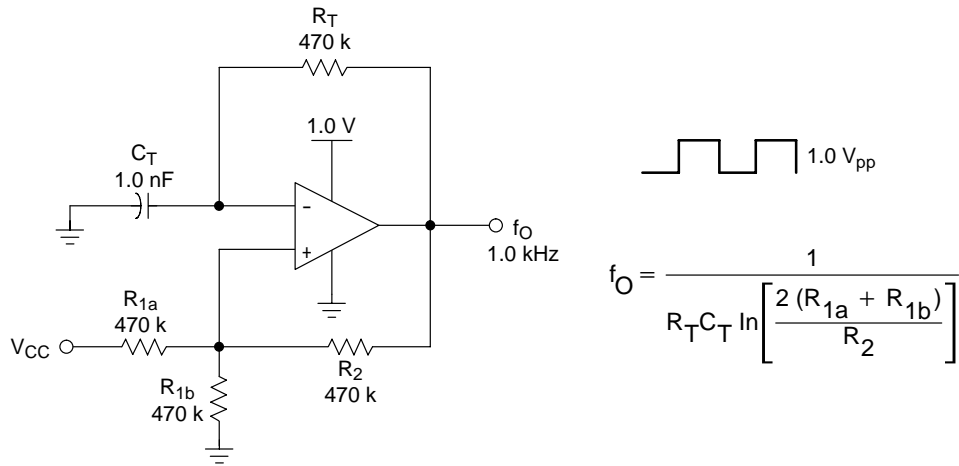
Figure 33. 1.0 V Oscillator

$$f_O = \frac{1}{R_T C_T \ln\left[\dfrac{2\,(R_{1a} + R_{1b})}{R_2}\right]}$$

$$f_L = \frac{1}{2\,\pi\,R_1 C_1} \approx 200 \text{ Hz}$$

$$f_H = \frac{1}{2\,\pi\,R_f C_f} \approx 4.0 \text{ kHz}$$

$$A_f = 1 + \frac{R_f}{R_2} = 11$$
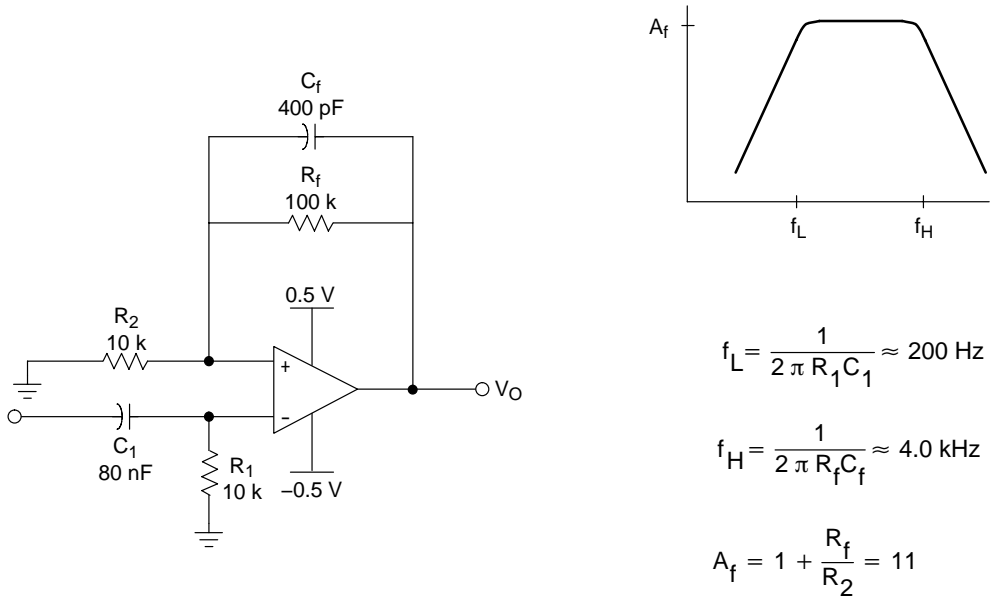
Figure 34. 1.0 V Voiceband Filter

MC33502
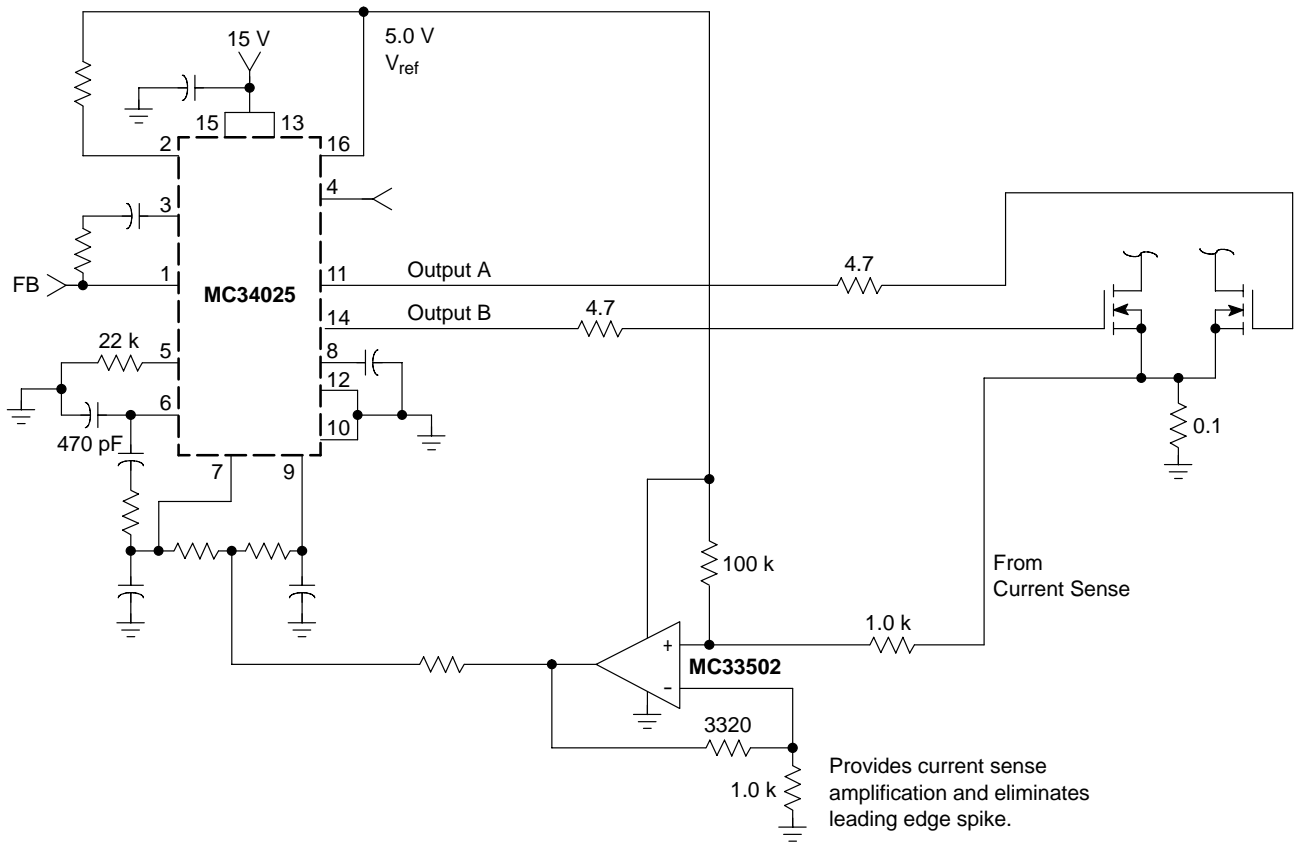
Figure 35. Power Supply Application
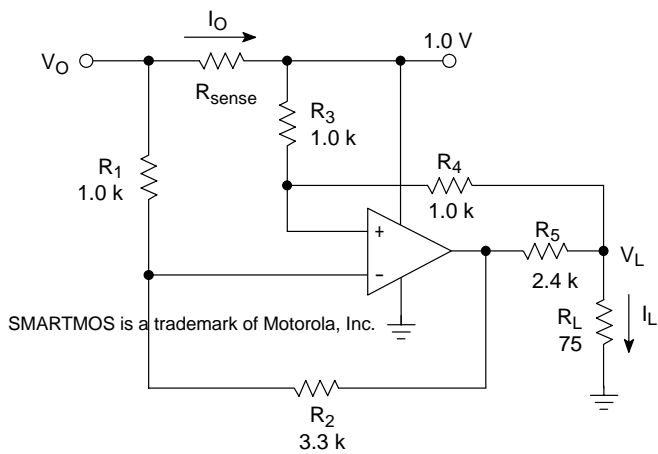
I_O	I_L	$\Delta I_O/\Delta I_L$
435 mA	463 μA	-120×10^{-6}
212 mA	492 μA	

For best performance, use low tolerance resistors.

Figure 36. 1.0 V Current Pump

SMARTMOS is a trademark of Motorola, Inc.

PDIP−8
CASE 626−05
ISSUE P

DATE 22 APR 2015

SCALE 1:1

TOP VIEW

NOTE 8

END VIEW
WITH LEADS CONSTRAINED
NOTE 5

SIDE VIEW

⊕ 0.010 Ⓜ C A Ⓜ B Ⓜ

END VIEW
NOTE 6
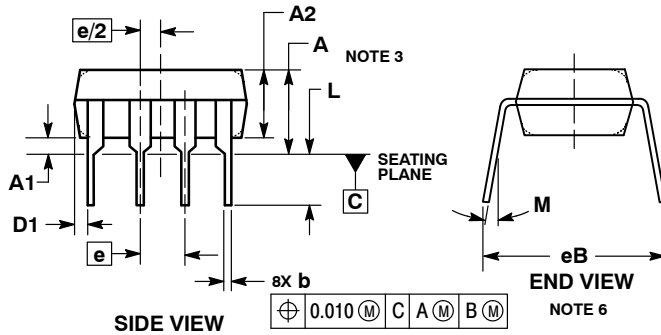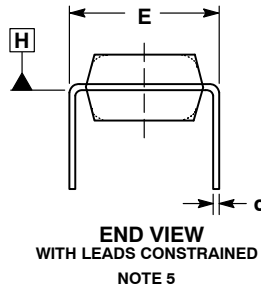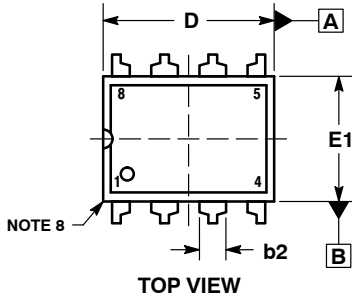
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-AGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V$_{CC}$

GENERIC
MARKING DIAGRAM*

XXXXXXXXX
AWL
YYWWG
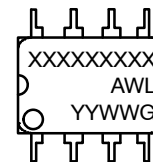
XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

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DESCRIPTION:	PDIP−8		PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

onsemi™

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

8
1
SCALE 1:1

−X−

A

−Y−

B

S

G

⊕ | 0.25 (0.010) Ⓜ | Y | Ⓜ

K

C

SEATING PLANE

−Z−

⌓ | 0.10 (0.004)

H   D

N X 45°

M   J

⊕ | 0.25 (0.010)Ⓜ | Z | Y Ⓢ | X Ⓢ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

1.52
0.060

7.0
0.275

4.0
0.155

0.6
0.024

1.270
0.050

SCALE 6:1   (mm / inches)
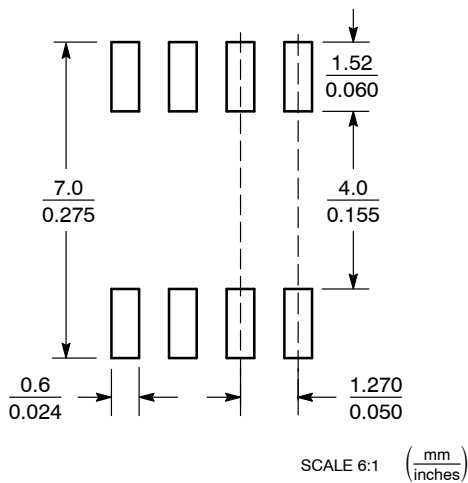
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

8 XXXXX ALYWX
1
IC

8 XXXXX ALYWX ▪
1
IC (Pb−Free)

8 XXXXXX AYWW
1
Discrete

8 XXXXXX AYWW ▪
1
Discrete (Pb−Free)
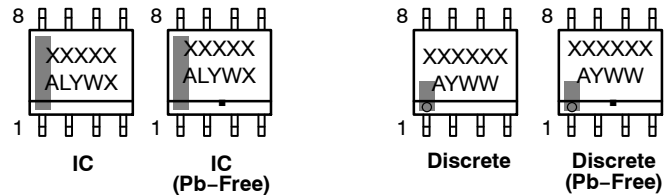
XXXXX = Specific Device Code
A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
▪   = Pb−Free Package

XXXXXX = Specific Device Code
A   = Assembly Location
Y   = Year
WW   = Work Week
▪   = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B		
DESCRIPTION:	SOIC−8 NB		PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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ADDITIONAL INFORMATION

◊