

1.55V DDR2 FBDIMM

MT36RTF51272FZ – 4GB

Features

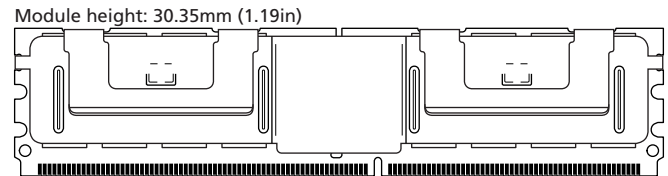
- 240-pin, fully buffered DIMM (FBDIMM)
- Very low power DDR2 operation
- $1.5V \leq V_{DD} \leq 1.9V$ for DDR2 SDRAM
- $1.5V \leq V_{DD} \leq 1.9V$ for advanced memory buffer (AMB) DRAM I/O
- $V_{DD} = 1.55V$
- Backward compatible with systems designed for the standard (1.8V) FBDIMM
- Dual rank
- Component configuration: 256 Meg x 4

Functionality

This 1.55V FBDIMM consumes less power than a standard 1.8V FBDIMM. However, it has the same timing and operating parameters as a standard FBDIMM. This enables backward compatibility with systems designed for use with standard FBDIMMs.

Information in the 1.8V DDR2 FBDIMM data sheet is directly applicable to this 1.55V DDR2 FBDIMM, except where stated otherwise in this data sheet.

Figure 1: 240-Pin FBDIMM (MO-256 R/C E)



Options

- Package
 - 240-pin DIMM (halogen-free)
- Frequency/CL¹
 - 3.0ns @ CL = 5 (DDR2-667)

Marking

Z
-667

Note: 1. CL = CAS (READ) latency.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			t _{RCD} (ns)	t _{RP} (ns)	t _{RC} (ns)
		CL = 5	CL = 4	CL = 3			
-667	PC2-5300	667	553	400	15	15	55
-53E	PC2-4200	–	553	400	15	15	55



Table 2: Addressing

Parameter	4GB
Refresh count	8K
Device bank address	8 BA[2:0]
Device page size per bank	1KB
Device configuration	1Gb (256 Meg x 4)
Row address	16K A[13:0]
Column address	2K A[11, 9:0]
Module rank address	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 4GB

Base device: MT47R256M4,¹ 1Gb DDR2 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)	Link Transfer Rate
MT36RTF51272FZ-667__	4GB	512 Meg x 72	PC2-5300	3.0ns/667 MT/s	5-5-5	4.0 GT/s

- Notes:
1. The data sheet for the base device can be found on Micron's Web site.
 2. All part numbers end with a four-place code (not shown) that designates component, PCB, and AMB revisions. Consult factory for current revision codes. Example: MT36RTF51272FZ-667H1D6.



4GB (x72, DR) 240-Pin DDR2 SDRAM 1.55V FBDIMM Pin Assignments and Descriptions

Pin Assignments and Descriptions

Table 4: Pin Assignments

240-Pin FBDIMM Front								240-Pin FBDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{DD}	31	PN3	61	PN9#	91	PS9# ¹	121	V _{DD}	151	SN3	181	SN9#	211	SS9# ¹
2	V _{DD}	32	PN3#	62	V _{SS}	92	V _{SS}	122	V _{DD}	152	SN3#	182	V _{SS}	212	V _{SS}
3	V _{DD}	33	V _{SS}	63	PN10	93	PS5	123	V _{DD}	153	V _{SS}	183	SN10	213	SS5
4	V _{SS}	34	PN4	64	PN10#	94	PS5#	124	V _{SS}	154	SN4	184	SN10#	214	SS5#
5	V _{DD}	35	PN4#	65	V _{SS}	95	V _{SS}	125	V _{DD}	155	SN4#	185	V _{SS}	215	V _{SS}
6	V _{DD}	36	V _{SS}	66	PN11	96	PS6	126	V _{DD}	156	V _{SS}	186	SN11	216	SS6
7	V _{DD}	37	PN5	67	PN11#	97	PS6#	127	V _{DD}	157	SN5	187	SN11#	217	SS6#
8	V _{SS}	38	PN5#	68	V _{SS}	98	V _{SS}	128	V _{SS}	158	SN5#	188	V _{SS}	218	V _{SS}
9	V _{CC}	39	V _{SS}	69	V _{SS}	99	PS7	129	V _{CC}	159	V _{SS}	189	V _{SS}	219	SS7
10	V _{CC}	40	PN13 ¹	70	PS0	100	PS7#	130	V _{CC}	160	SN13 ¹	190	SS0	220	SS7#
11	V _{SS}	41	PN13# ¹	71	PS0#	101	V _{SS}	131	V _{SS}	161	SN13# ¹	191	SS0#	221	V _{SS}
12	V _{CC}	42	V _{SS}	72	V _{SS}	102	PS8	132	V _{CC}	162	V _{SS}	192	V _{SS}	222	SS8
13	V _{CC}	43	V _{SS}	73	PS1	103	PS8#	133	V _{CC}	163	V _{SS}	193	SS1	223	SS8#
14	V _{SS}	44	DNU	74	PS1#	104	V _{SS}	134	V _{SS}	164	DNU	194	SS1#	224	V _{SS}
15	V _{TT}	45	DNU	75	V _{SS}	105	DNU	135	V _{TT}	165	DNU	195	V _{SS}	225	DNU
16	DNU	46	V _{SS}	76	PS2	106	DNU	136	DNU	166	V _{SS}	196	SS2	226	DNU
17	RESET#	47	V _{SS}	77	PS2#	107	V _{SS}	137	M_TEST (DNU)	167	V _{SS}	197	SS2#	227	V _{SS}
18	V _{SS}	48	PN12 ¹	78	V _{SS}	108	V _{DD}	138	V _{SS}	168	SN12 ¹	198	V _{SS}	228	SCK
19	DNU	49	PN12# ¹	79	PS3	109	V _{DD}	139	DNU	169	SN12# ¹	199	SS3	229	SCK#
20	DNU	50	V _{SS}	80	PS3#	110	V _{SS}	140	DNU	170	V _{SS}	200	SS3#	230	V _{SS}
21	V _{SS}	51	PN6	81	V _{SS}	111	V _{DD}	141	V _{SS}	171	SN6	201	V _{SS}	231	V _{DD}
22	PN0	52	PN6#	82	PS4	112	V _{DD}	142	SN0	172	SN6#	202	SS4	232	V _{DD}
23	PN0#	53	V _{SS}	83	PS4#	113	V _{DD}	143	SN0#	173	V _{SS}	203	SS4#	233	V _{DD}
24	V _{SS}	54	PN7	84	V _{SS}	114	V _{SS}	144	V _{SS}	174	SN7	204	V _{SS}	234	V _{SS}
25	PN1	55	PN7#	85	V _{SS}	115	V _{DD}	145	SN1	175	SN7#	205	V _{SS}	235	V _{DD}
26	PN1#	56	V _{SS}	86	DNU	116	V _{DD}	146	SN1#	176	V _{SS}	206	DNU	236	V _{DD}
27	V _{SS}	57	PN8	87	DNU	117	V _{TT}	147	V _{SS}	177	SN8	207	DNU	237	V _{TT}
28	PN2	58	PN8#	88	V _{SS}	118	SA2	148	SN2	178	SN8#	208	V _{SS}	238	V _{DDSPD}
29	PN2#	59	V _{SS}	89	V _{SS}	119	SDA	149	SN2#	179	V _{SS}	209	V _{SS}	239	SA0
30	V _{SS}	60	PN9	90	PS9 ¹	120	SCL	150	V _{SS}	180	SN9	210	SS9 ¹	240	SA1

Note: 1. The following signals are cyclical redundancy code (CRC) bits and thus appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, and SS9/SS9#.



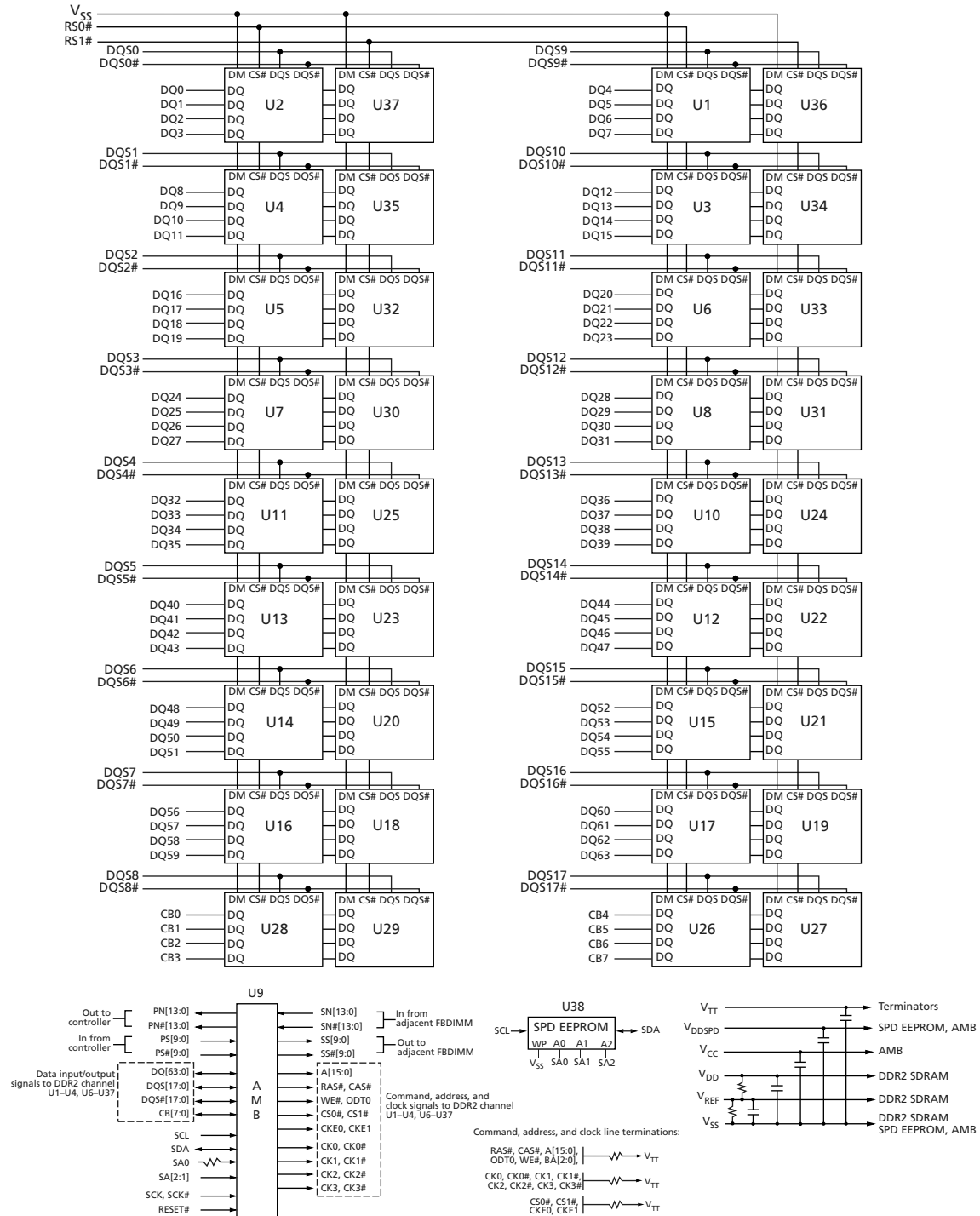
4GB (x72, DR) 240-Pin DDR2 SDRAM 1.55V FBDIMM Pin Assignments and Descriptions

Table 5: Pin Descriptions

Symbol	Type	Description
PS[9:0]	Input	Primary southbound data, positive lines.
PS#[9:0]	Input	Primary southbound data, negative lines.
SCK	Input	System clock input, positive line.
SCK#	Input	System clock input, negative line.
SCL	Input	Serial presence-detect (SPD) clock input.
SS[9:0]	Input	Secondary southbound data, positive lines.
SS#[9:0]	Input	Secondary southbound data, negative lines.
PN[13:0]	Output	Primary northbound data, positive lines.
PN#[13:0]	Output	Primary northbound data, negative lines.
SN[13:0]	Output	Secondary northbound data, positive lines.
SN#[13:0]	Output	Secondary northbound data, negative lines.
VID0	Output	Voltage identification, connected to V_{SS} . Indicates 1.5V DRAM present on module.
SA[2:0]	I/O	SPD address inputs, also used to select the FBDIMM number in the AMB.
SDA	I/O	SPD data input/output.
RESET#	Supply	AMB reset signal.
V_{CC}	Supply	AMB core power and AMB channel interface power (1.5V).
V_{DD}	Supply	DRAM power and AMB DRAM I/O power (1.5V).
V_{TT}	Supply	DRAM clock, command, and address termination power ($V_{DD}/2$).
V_{DDSPD}	Supply	SPD/AMB SMBus power.
V_{SS}	Supply	Ground.
M_TEST	–	The M_TEST pin provides an external connection for testing the margin of V_{REF} , which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time.
DNU	–	Do not use.

Functional Block Diagram

Figure 2: Functional Block Diagram



Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Voltage on any signal pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.3	1.75	V	1
Voltage on V_{CC} pin relative to V_{SS}	V_{CC}	-0.3	1.75	V	
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.5	2.3	V	
Voltage on V_{TT} pin relative to V_{SS}	V_{TT}	-0.5	2.3	V	
DDR2 SDRAM device operating case temperature	T_C	0	95	°C	2, 3
AMB device operating case temperature		0	110	°C	

- Notes:
- V_{IN} should not be greater than V_{CC} .
 - T_C is specified at 95°C only when using 2X refresh timing ($t_{REFI} = 7.8\mu s$ at or below 85°C; $t_{REFI} = 3.9\mu s$ above 85°C); DDR2 SDRAM component data sheet.
 - See applicable DDR2 SDRAM component data sheet for t_{REFI} and extended mode register settings. The t_{REFI} parameter is used to specify the doubled refresh interval necessary to sustain <85°C operation.

Table 7: Input DC Voltage and Operating Conditions

Parameter	Symbol	Min	Nom	Max	Units	Notes
AMB supply voltage	V_{CC}	1.455	1.50	1.575	V	
DDR2 SDRAM supply voltage	V_{DD}	1.5	1.55	1.9	V	
Termination voltage	V_{TT}	$0.48 \times V_{DD}$	$0.50 \times V_{DD}$	$0.52 \times V_{DD}$	V	
EEPROM supply voltage	V_{DDSPD}	3.0	-	3.6	V	1
SPD input high (logic 1) voltage	$V_{IH(DC)}$	2.1	-	V_{DDSPD}	V	2
SPD input low (logic 0) voltage	$V_{IL(DC)}$	-0.6	-	0.8	V	2
RESET input high (logic 1) voltage	$V_{IH(DC)}$	1.0	-	-	V	3
RESET input low (logic 0) voltage	$V_{IL(DC)}$	-	-	0.5	V	2
Leakage current (RESET)	I_L	-90	-	90	μA	3
Leakage current (link)	I_L	-5	-	5	μA	4

- Notes:
- Applies to AMB and SPD.
 - Applies to SMBus and SPD bus signals.
 - Applies to AMB CMOS signal RESET#.
 - For all other AMB related DC parameters, refer to the high-speed differential link interface specification.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.



IDD Specifications and Conditions

Table 8: I_{DD} Conditions

Symbol	Condition
I _{DD_IDLE_0}	Idle current, single, or last DIMM: L0 state; Idle (0% bandwidth); Primary channel enabled; Secondary channel disabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
I _{DD_IDLE_1}	Idle current, first DIMM: L0 state; Idle (0% bandwidth); Primary and secondary channels enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
I _{DD_ACTIVE_1}	Active power: L0 state; 50% DRAM bandwidth; 67% READ; 33% WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH
I _{DD_ACTIVE_2}	Active power, data pass through: L0 state; 50% DRAM bandwidth to downstream DIMM; 67% READ; 33% WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH; Command and address lines stable
I _{DD_TRAINING}	Training: Primary and secondary channels enabled; 100% toggle on all channel lanes; DRAMs idle; 0% bandwidth; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
I _{DD_IBIST}	IBIST over all IBIST modes: DRAM idle (0% bandwidth); Primary channel enabled; Secondary channel enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
I _{DD_EI}	Electrical idle: DRAM idle (0% bandwidth); Primary channel disabled; Secondary channel disabled; CKE LOW; Command and address lines floated; DDR2 SDRAM clock active; ODT and CKE driven LOW

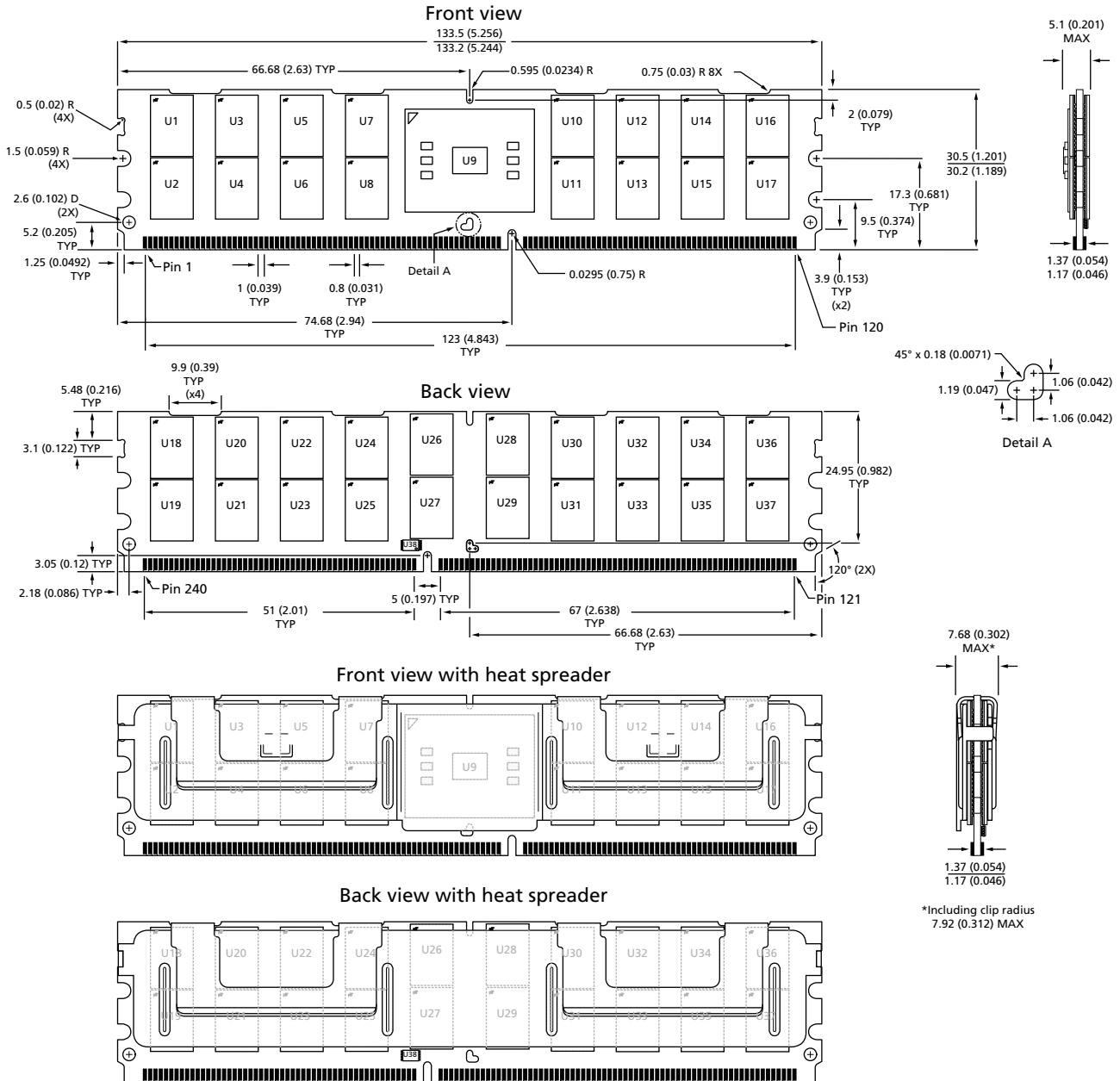
Note: 1. Actual test conditions may vary from published JEDEC test conditions.

Table 9: I_{DD} Specifications – 4GB DDR2-667

Symbol	I _{DD_IDLE_0}	I _{DD_IDLE_1}	I _{DD_ACTIVE_1}	I _{DD_ACTIVE_2}	I _{DD_TRAINING}	I _{DD_IBIST}	I _{DD_EI}	Units
I _{CC}	2600	3400	3900	3700	4000	4500	2500	mA
I _{DD}	1800	1800	3320	1800	1800	1800	452	mA
Total power	7.5	8.8	12.4	9.2	9.7	10.5	4.8	W

Module Dimensions

Figure 3: 240-Pin DDR2 FBDIMM



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.



4GB (x72, DR) 240-Pin DDR2 SDRAM 1.55V FBDIMM Module Dimensions

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Although considered final, these specifications are subject to change, as further product development and data characterization some-
times occur.