MAX14851

Six-Channel Digital Isolator

General Description

The MAX14851 is a six-channel digital isolator utilizing Maxim's proprietary process technology, whose monolithic design provides a compact and low-cost transfer of digital signals between circuits with different power domains. The technology enables low power consumption and high channel density.

The four unidirectional channels are each capable of DC to 50Mbps, with two of the four channels passing data across the isolation barrier in each direction. The two bidirectional channels are open-drain, each capable of data rates from DC to 2Mbps.

Independent 3.0V to 5.5V supplies on each side of the isolator also make it suitable for use as a level translator. The MAX14851 can be used for isolating SPI buses, I^2C buses, RS-232, RS-485/RS-422 buses, and general-purpose isolation. When used as a bus isolator, extra channels are available for power monitoring and reset signals.

The MAX14851 is available in a 16-pin QSOP (3.9mm x 4.94mm) package. The device is specified over the -40°C to +125°C temperature range.

The MAX14851 is a functional replacement for the MAX14850, and shares the same pin configurations as the MAX14850.

Applications

- Industrial Control Systems
- I^2C, SPI, SMBus, PMBus™ Interfaces
- Isolated RS-232, RS-485/RS-422
- Telecommunication Systems
- Battery Management
- Medical Systems

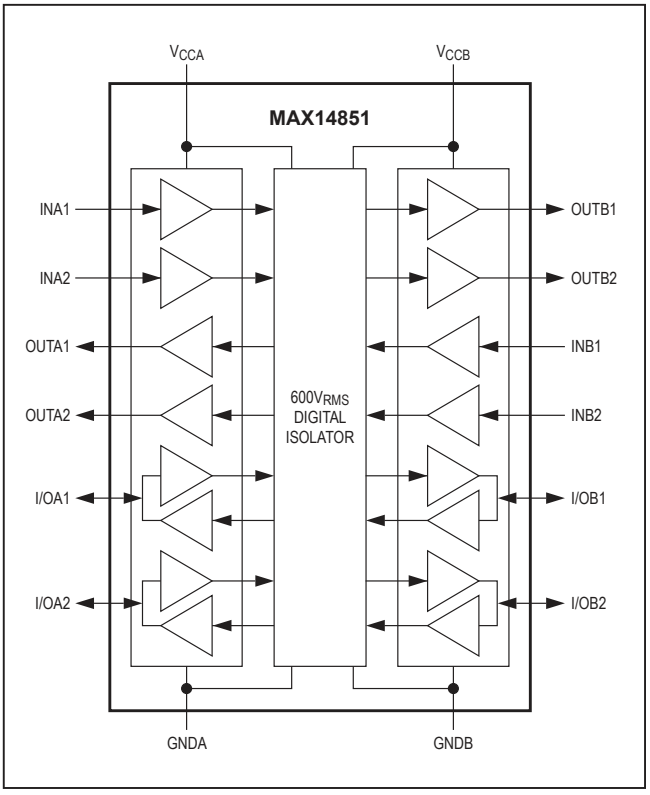
PMBus is a trademark of SMIF, Inc.

Benefits and Features

- Complete Digital Isolation Solution
  - $600V_{RMS}$ Isolation for 60 Seconds
  - Short-Circuit Protection on Unidirectional Outputs
  - $200V_{RMS}$ Working Isolation Voltage
  - Four Unidirectional Signal Paths: 2-In/2-Out
  - Two Bidirectional Open-Drain Signal Paths
  - 50Mbps (max) Unidirectional Data Rate
  - 2Mbps (max) Bidirectional Data Rate
- Compatible with Many Interface Standards
  - I^2C
  - SPI
  - RS-232, RS-485/RS-422
  - SMBus, PMBus Interfaces

***Ordering Information* appears at end of data sheet.**

Functional Diagram



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Absolute Maximum Ratings

V_{CCA} to GNDA .....-0.3V to +6V
V_{CCB} to GNDB .....-0.3V to +6V
OUTA1, OUTA2 to GNDA.....-0.3V to (V_{CCA} + 0.3V)
OUTB1, OUTB2 to GNDB.....-0.3V to (V_{CCB} + 0.3V)
INA1, INA2 to GNDA.....-0.3V to +6V
I/OA1, I/OA2 to GNDA.....-0.3V to (V_{CCA} + 0.3V)
INB1, INB2, I/OB1, I/OB2 to GNDB .....-0.3V to +6V
OUTA1, OUTA2, OUTB1, OUTB2 Continuous Current ...±30mA
I/OA1, I/OA2 Continuous Current.....±30mA
I/OB1, I/OB2 Continuous Current.....±100mA
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 9.6mW/°C above +70°C).....771.5mW
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Package Thermal Characteristics (Note 1)

QSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....103.7°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{CCA} - V_{GNDA} = 3.0V to 5.5V, V_{CCB} - V_{GNDB} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CCA} - V_{GNDA} = 3.3V, V_{CCB} - V_{GNDB} = 3.3V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
VOLTAGE SUPPLY							
Supply Voltage	V_{CCA}	Relative to GNDA		3.0		5.5	V
	V_{CCB}	Relative to GNDB		3.0		5.5	
Supply Current	I_{CCA}, I_{CCB}	All inputs static at GND_ or VCC_. No load.	V_{CCA} = 5V		4	6.9	mA
			V_{CCB} = 5V		3.6	6.1	
			V_{CCA} = 3.3V		3.6	6.2	
			V_{CCB} = 3.3V		3.2	5.5	
		All inputs switching (INA_, INB_ at 50Mbps and I/OA_ at 2Mbps). No load. (Note 3)	V_{CCA} = 5V		6.4	10.2	
			V_{CCB} = 5V		5.8	9.2	
			V_{CCA} = 3.3V		4.6	7.6	
			V_{CCB} = 3.3V		4.1	6.7	
Undervoltage Lockout Threshold	$V_{UVLO\_}$	$V_{CC\_}$ rising (Note 4)		2.45	2.6	2.85	V
Undervoltage Lockout Hysteresis	$V_{UVLOHYS}$	(Note 4)			55		mV

DC Electrical Characteristics (continued)

(V_{CCA} - V_{GNDA} = 3.0V to 5.5V, V_{CCB} - V_{GNDB} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CCA} - V_{GNDA} = 3.3V, V_{CCB} - V_{GNDB} = 3.3V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
UNIDIRECTIONAL LOGIC INPUTS AND OUTPUTS (INA_, INB_, OUTA_, OUTB_)						
Input Logic-High Voltage	V_{IH}	INA_ relative to GNDA	0.7 x V_{CCA}			V
		INB_ relative to GNDB	0.7 x V_{CCB}			
Input Logic-Low Voltage	V_{IL}	INA_ relative to GNDA			0.8	V
		INB_ relative to GNDB			0.8	
Input Hysteresis	V_{HYST}	INA_ relative to GNDA		0.45		V
		INB_ relative to GNDB		0.45		
Input Leakage Current	I_L	INA_/INB_ = 0 or $V_{CC\_}$	-1		+1	µA
Input Capacitance	C_{IN}	INA_, INB_, f = 1MHz		2		pF
Output Logic-High Voltage	V_{OH}	OUTA_ relative to GNDA, source current = 4mA	V_{CCA} - 0.4			V
		OUTB_ relative to GNDB, source current = 4mA	V_{CCB} - 0.4			
Output Logic-Low Voltage	V_{OL}	OUTA_ relative to GNDA, sink current = 4mA			0.4	V
		OUTB_ relative to GNDB, sink current = 4mA			0.4	
BIDIRECTIONAL LOGIC INPUTS AND OUTPUTS (I/OA_, I/OB_)						
Input Threshold Voltage	V_{IT}	I/OA_ relative to GNDA	0.5		0.7	V
Input Logic-High Voltage	V_{IH}	I/OA_ relative to GNDA	0.7			V
		I/OB_ relative to GNDB	0.5 x V_{CCB}			
Input Logic-Low Voltage	V_{IL}	I/OA_ relative to GNDA			0.5	V
		I/OB_ relative to GNDB			0.3 x V_{CCB}	
Input/Output Logic-Low Threshold Difference	ΔV_{TOL}	I/OA_ relative to GNDA, 0.5mA ≤ I_{OUT} ≤ 3.5mA sink current (Note 6)	50			mV
Input Hysteresis	V_{HYST}	I/OA_ relative to GNDA		75		mV
		I/OB_ relative to GNDB		200		
Input Leakage Current	I_L	I/OA_ = V_{CCA}	-2		+10	µA
		I/OB_ = V_{CCB}	-1		+1	
Output Logic-Low Voltage	V_{OL}	I/OA_ relative to GNDA, 0.5mA ≤ I_{OUT} ≤ 3.5mA sink current	0.65		0.8	V
		I/OB_ relative to GNDB, I_{OUT} = 35mA sink current			0.4	

Switching Electrical Characteristics

(V_{CCA} - V_{GNDA} = 3.0V to 5.5V, V_{CCB} - V_{GNDB} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CCA} - V_{GNDA} = 3.3V, V_{CCB} - V_{GNDB} = 3.3V, and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Common-Mode Transient Immunity	CMTI	$V_{IN\_, I/O\_}$ = $V_{CC\_}$ or $V_{GND\_}$ (Note 7)			3.2		kV/µs
UNIDIRECTIONAL DYNAMIC SWITCHING CHARACTERISTICS (INA_, INB_, OUTA_, OUTB_)							
Maximum Data Rate	DR_{MAX}	INA_ to OUTB_, INB_ to OUTA_		50			Mbps
Minimum Pulse Width	PW_{MIN}	INA_ to OUTB_, INB_ to OUTA_				20	ns
Propagation Delay	t_{DPLH}	INA_ to OUTB_, INB_ to OUTA_, R_L = 1MΩ, C_L = 15pF, Figure 1	4.5V ≤ $V_{CC\_}$ ≤ 5.5V	4.0		11.8	ns
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V	4.0		13.3	
	t_{DPHL}		4.5V ≤ $V_{CC\_}$ ≤ 5.5V	4.3		11.6	
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V	4.4		13.4	
Pulse-Width Distortion $\lvert t_{DPLH} - t_{DPHL} \rvert$	PWD	INA_ to OUTB_, INB_ TO OUTA_, R_L = 1MΩ, C_L = 15pF, Figure 1 (Note 8)	4.5V ≤ $V_{CC\_}$ ≤ 5.5V			2.9	ns
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V			2.6	
Channel-to-Channel Skew	$t_{DSKEWCC}$	OUTB1 to OUTB2 output skew, Figure 1 (Note 8)				2	ns
		OUTA1 to OUTA2 output skew, Figure 1 (Notes 8)				2	
Part-to-Part Skew	$t_{DSKEWPP}$	Δt_{DPLH}, Δt_{DPHL} (Note 8)				8	ns
Rise Time	t_R	OUTA_, OUTB_, 10% to 90%, C_L = 15pF, Figure 1				5	ns
Fall Time	t_F	OUTA_, OUTB_, 90% to 10%, C_L = 15pF, Figure 1				5	

Switching Electrical Characteristics (continued)

(V_{CCA} - V_{GNDA} = 3.0V to 5.5V, V_{CCB} - V_{GNDB} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CCA} - V_{GNDA} = 3.3V, V_{CCB} - V_{GNDB} = 3.3V, and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
BIDIRECTIONAL DYNAMIC SWITCHING CHARACTERISTICS (I/OA_, I/OB_)							
Maximum Data Rate	DR_{MAX}	I/OA_ to I/OB_, I/OB_ to I/OA_		2			Mbps
Propagation Delay	t_{PLHAB}	I/OA_ = 0.5V to I/OB_ = 0.7 x V_{CCB}, C_A = C_B = 10pF, Figure 2	4.5V ≤ $V_{CC\_}$ ≤ 5.5V, R_A = 1430Ω, R_B = 143Ω	25.4		85.8	ns
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V, R_A = 953Ω, R_B = 95.3Ω	26.3		93.0	
	t_{PHLAB}	I/OA_ = 0.5V to I/OB_ = 0.4V, C_A = C_B = 10pF, Figure 2	4.5V ≤ $V_{CC\_}$ ≤ 5.5V, R_A = 1430Ω, R_B = 143Ω	42.2		144.3	
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V, R_A = 953Ω, R_B = 95.3Ω	49.5		189.0	
	t_{PLHBA}	I/OB_ = 0.5V x V_{CCB} to I/OA_ = 0.7 x V_{CCA}, C_A = C_B = 10pF, Figure 2	4.5V ≤ $V_{CC\_}$ ≤ 5.5V, R_A = 1430Ω, R_B = 143Ω	43.7		122.9	
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V, R_A = 953Ω, R_B = 95.3Ω	32.1		94.2	
	t_{PHLBA}	I/OB_ = 0.3V x V_{CCB} to I/OA_ = 0.9V, C_A = C_B = 10pF, Figure 2	4.5V ≤ $V_{CC\_}$ ≤ 5.5V, R_A = 1430Ω, R_B = 143Ω	28.9		133.8	
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V, R_A = 953Ω, R_B = 95.3Ω	29.6		117.2	
Pulse-Width Distortion	PWD_{AB}	$\lvert t_{PLHAB} - t_{PHLAB} \rvert$ (Note 8)	4.5V ≤ $V_{CC\_}$ ≤ 5.5V			62.2	ns
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V			100.4	
	PWD_{BA}	$\lvert t_{PLHBA} - t_{PHLBA} \rvert$ (Note 8)	4.5V ≤ $V_{CC\_}$ ≤ 5.5V			32.0	
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V			37.0	

Switching Electrical Characteristics (continued)

(V_{CCA} - V_{GNDA} = 3.0V to 5.5V, V_{CCB} - V_{GNDB} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CCA} - V_{GNDA} = 3.3V, V_{CCB} - V_{GNDB} = 3.3V, and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Fall Time	t_{FA}	I/OA_ = 0.7 x V_{CCA} to 0.3 x V_{CCA}, C_A = 40pF, Figure 2	4.5V ≤ $V_{CC\_}$ ≤ 5.5V, R_A = 1430Ω	8.3		33.4	ns
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V, R_A = 953Ω	8.8		43.8	
	t_{FB}	I/OB_ = 0.7 x V_{CCB} to 0.3 x V_{CCB}, C_B = 400pF, Figure 2	4.5V ≤ $V_{CC\_}$ ≤ 5.5V, R_B = 143Ω	10.5		33.2	
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V, R_B = 95.3Ω	12.9		48.3	
	t_{FA}	I/OA_ = 0.9 x V_{CCA} to 900mV, C_A = 40pF Figure 2	4.5V ≤ $V_{CC\_}$ ≤ 5.5V, R_A = 1430Ω	16.1		86.7	
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V, R_A = 953Ω	14.5		67.4	
	t_{FB}	I/OB_ = 0.9 x V_{CCB} to 400mV, C_B = 400pF, Figure 2	4.5V ≤ $V_{CC\_}$ ≤ 5.5V, R_B = 143Ω	23.0		75.1	
			3.0V ≤ $V_{CC\_}$ ≤ 3.6V, R_B = 95.3Ω	26.9		104.7	

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design. All voltages of side A are referenced to GNDA. All voltages of side B are referenced to GNDB, unless otherwise noted.

Note 3: Guaranteed by design. Not production tested.

Note 4: The undervoltage lockout threshold and hysteresis guarantee that the outputs are in a known state during a slump in the supplies. See the *Detailed Description* section for more information.

Note 5: $\Delta V_{TOL} = V_{OL} - V_{IL}$. This is the minimum difference between the output logic-low voltage and the input logic threshold for the same I/O pin. This ensures that the I/O channels are not latched low when any of the I/O inputs are driven low (see the *Bidirectional Channels* section).

Note 6: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB.

Note 7: Pulse-width distortion is defined as the difference in propagation delay between low-to-high and high-to-low transitions on the same channel. Channel-to-channel skew is defined as the difference in propagation delay between different channels on the same device. Part-to-part skew is defined as the difference in propagation delays (for unidirectional channels) between different devices, when both devices operate with the same supply voltage, at the same temperature and have identical package and test circuits.

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human Body Model, all pins		±4		kV

Insulation and Safety Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 8)	282	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 8)	200	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s	850	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Notes 8, 9)	600	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic insulation, 1.2/50µs pulse per IEC 61000-4-5	1	kV
Insulation Resistance	R_S	T_A = 150ºC, V_{IO} = 500V	$>10^9$	Ω
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (Note10)	12	pF
External Tracking (Creepage)	CPG	QSOP	3.2	mm
External Air Gap (Clearance)	CLR	QSOP	3.2	mm
Internal Clearance		Distance through insulation	0.0026	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	>400	V
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 8: V_{ISO}, V_{IOWM}, and V_{IORM} are defined by the IEC 60747-5-5 standard.
Note 9 Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 10: Capacitance is measured with all pins on the field-side and logic-side tied together.

Test Circuits/Timing Diagrams

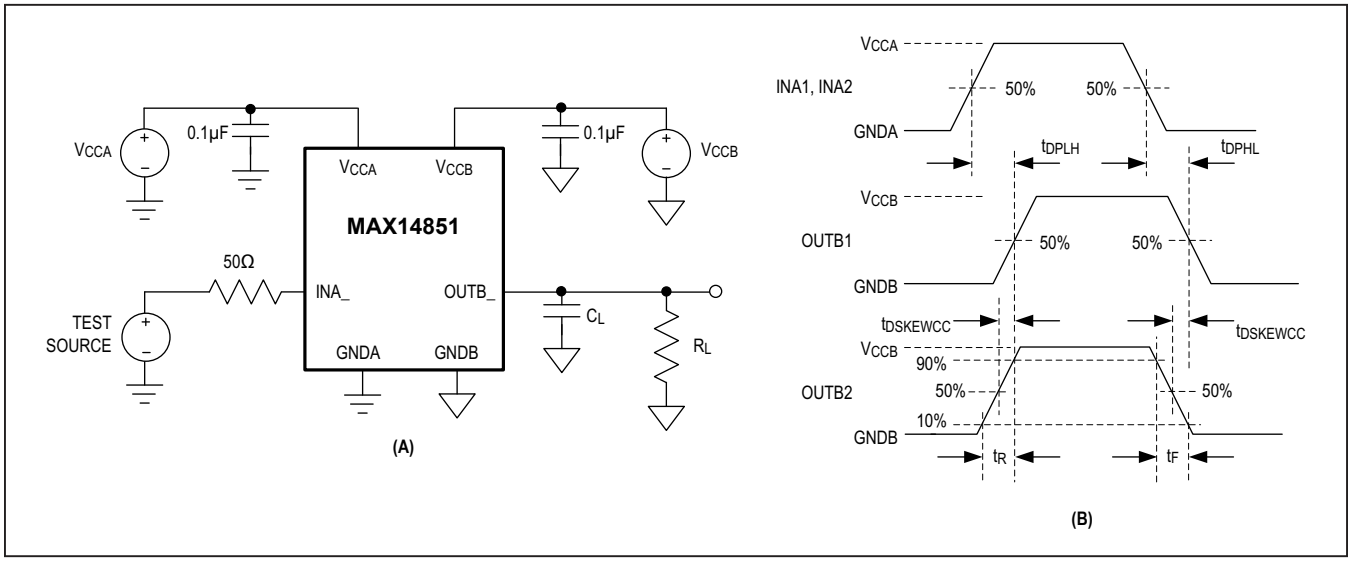


Figure 1. Test Circuit (A) and Timing Diagram (B) for Unidirectional Channels

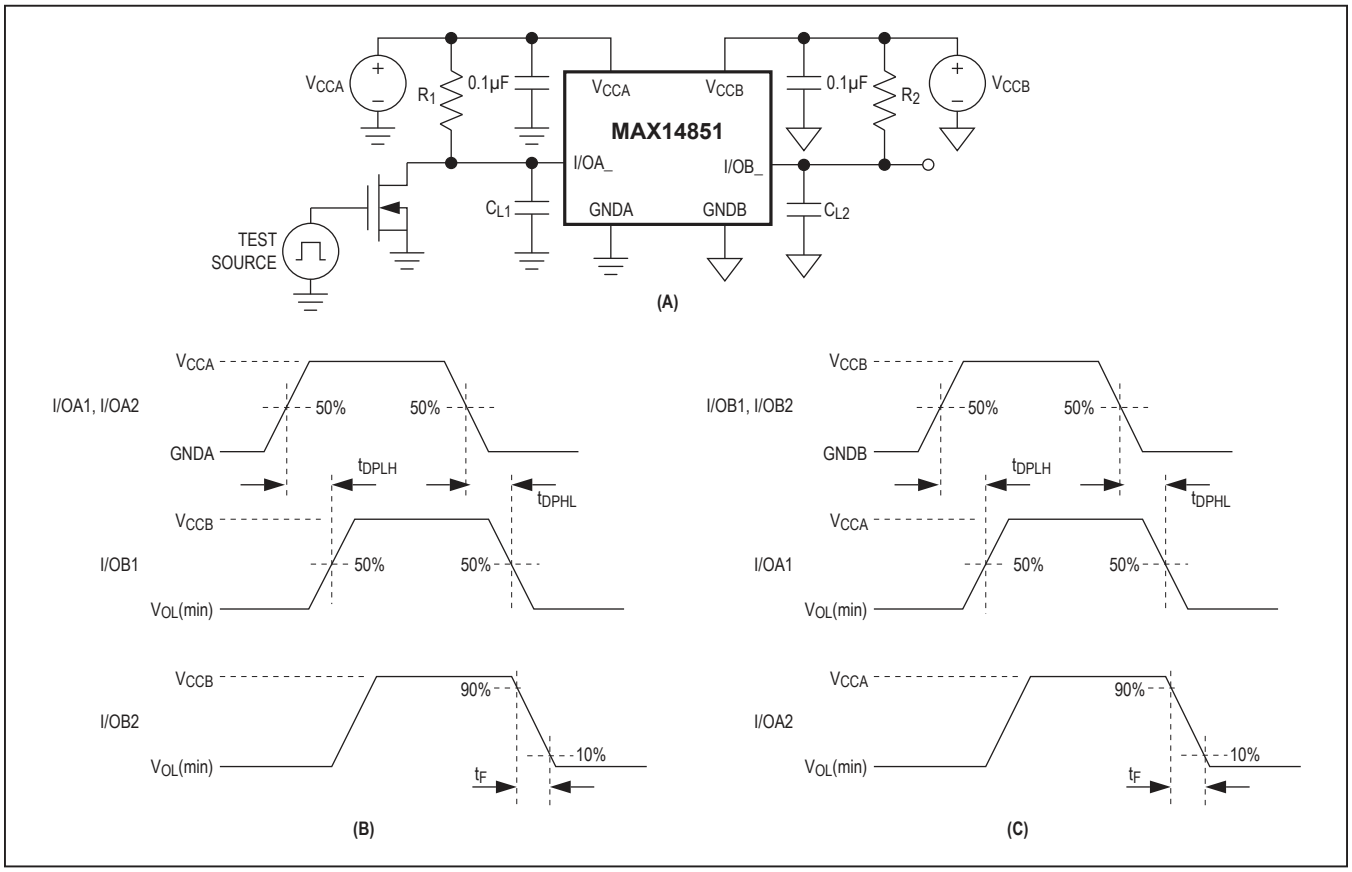
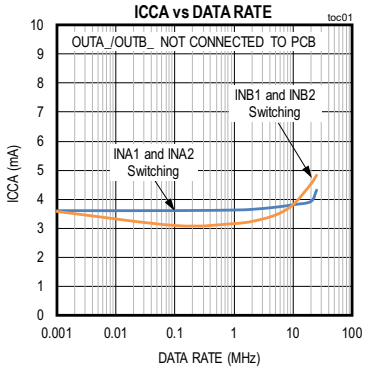
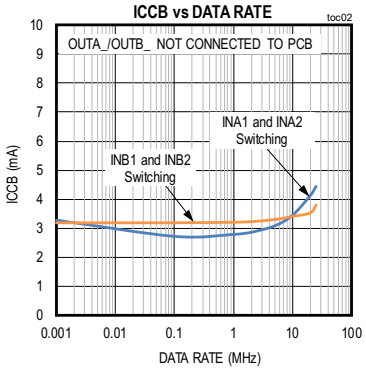


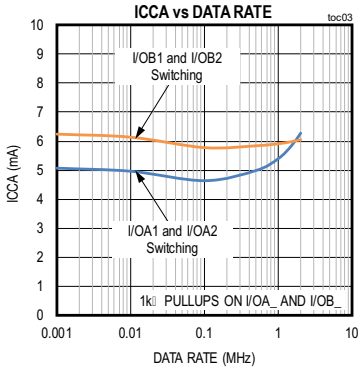
Figure 2. Test Circuit (A) and Timing Diagrams (B) and (C) for Bidirectional Channels

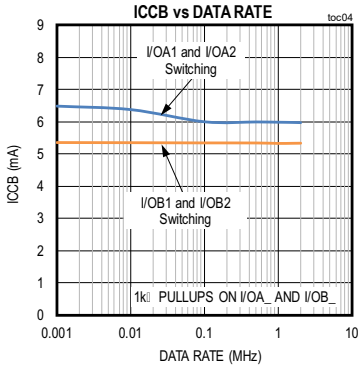
Typical Operating Characteristics

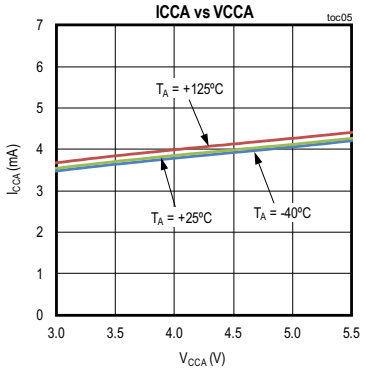
(V_{CCA} – V_{GNDA} = 3.3V, V_{CCB} – V_{GNDB} = 3.3V, all inputs idle, T_A = +25°C, unless otherwise noted.)

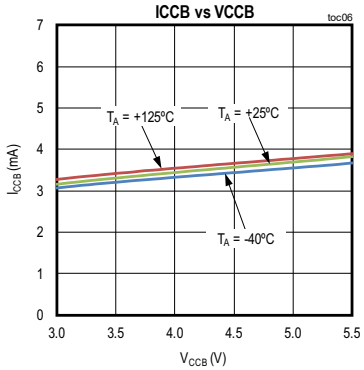


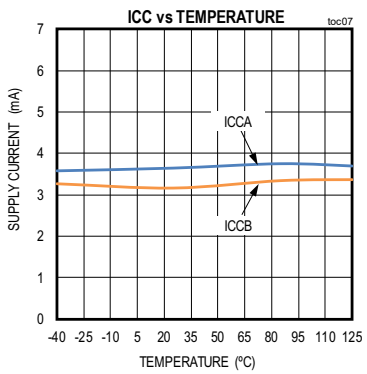


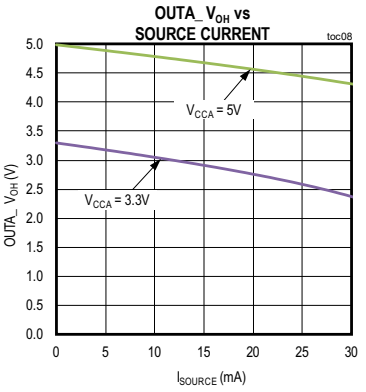


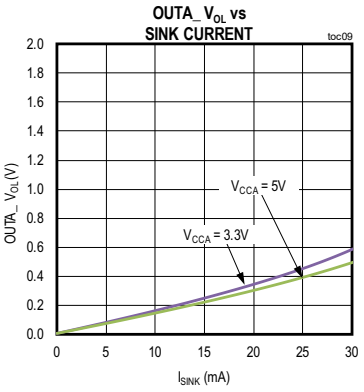






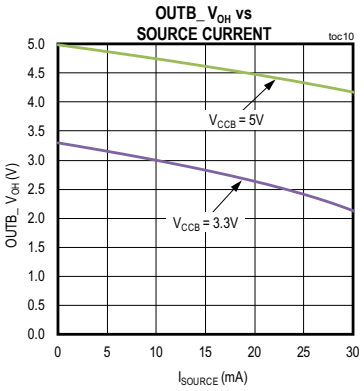


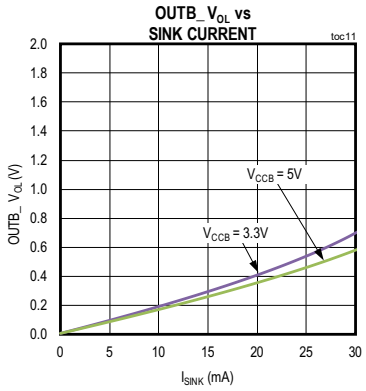


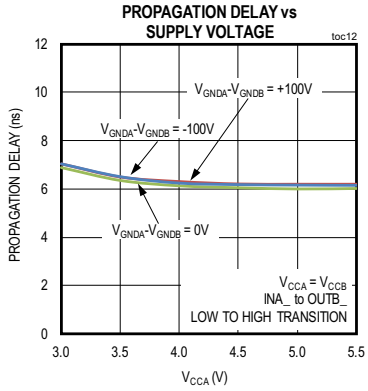


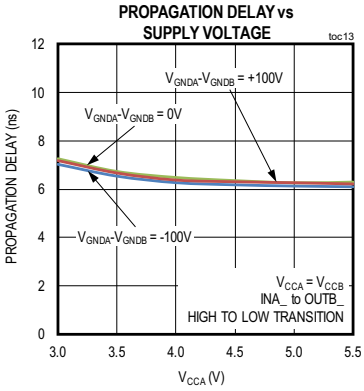
Typical Operating Characteristics (continued)

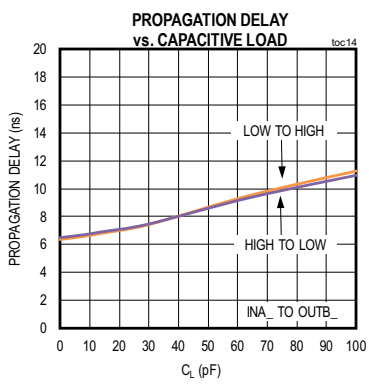
(V_{CCA} – V_{GNDA} = 3.3V, V_{CCB} – V_{GNDB} = 3.3V, all inputs idle, T_A = +25°C, unless otherwise noted.)

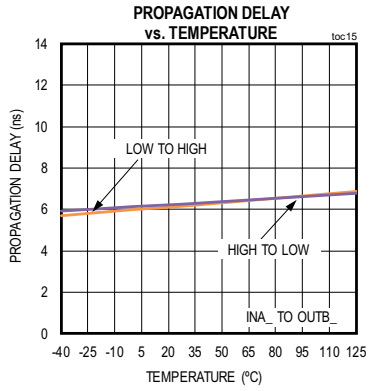


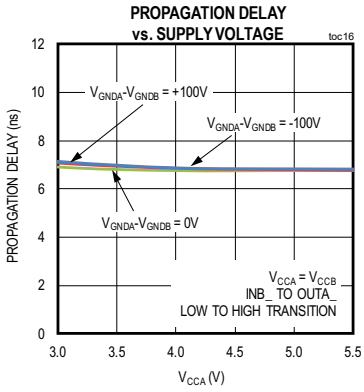


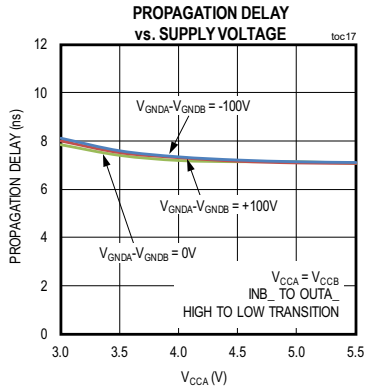


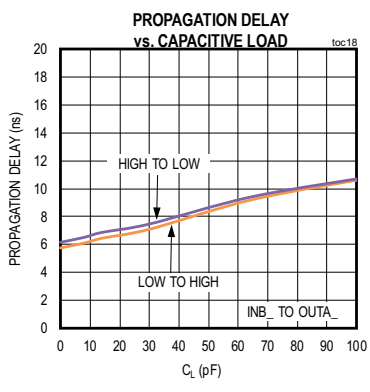








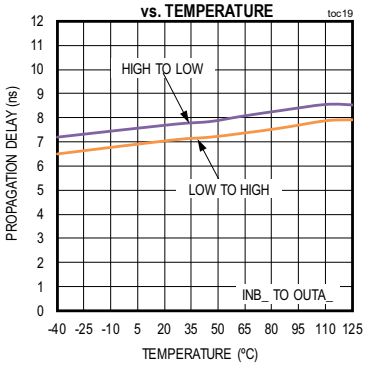




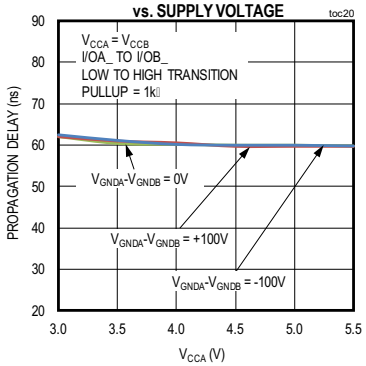
Typical Operating Characteristics (continued)

(V_{CCA} – V_{GNDA} = 3.3V, V_{CCB} – V_{GNDB} = 3.3V, all inputs idle, T_A = +25°C, unless otherwise noted.)

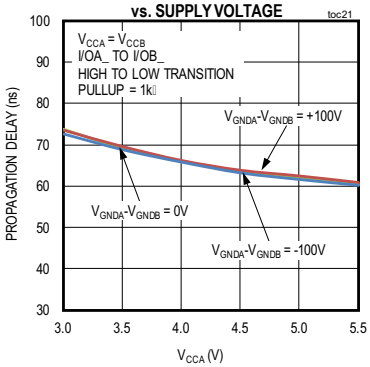
PROPAGATION DELAY vs. TEMPERATURE



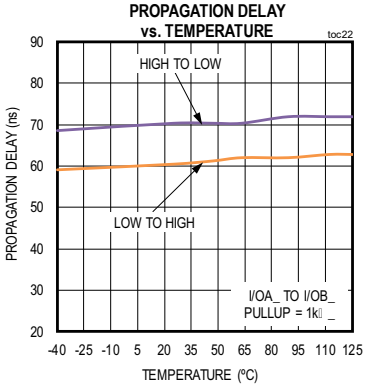
PROPAGATION DELAY vs. SUPPLY VOLTAGE



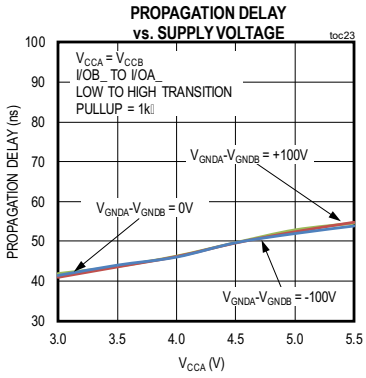
PROPAGATION DELAY vs. SUPPLY VOLTAGE



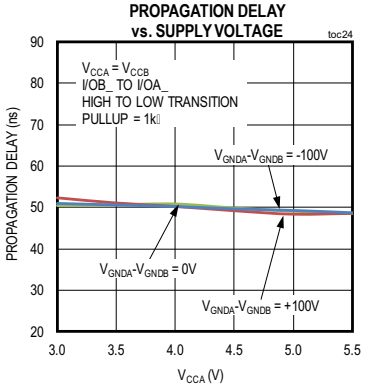
PROPAGATION DELAY vs. TEMPERATURE



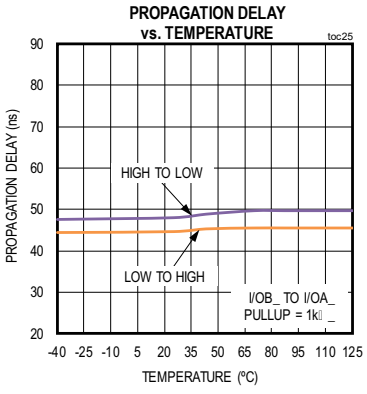
PROPAGATION DELAY vs. SUPPLY VOLTAGE



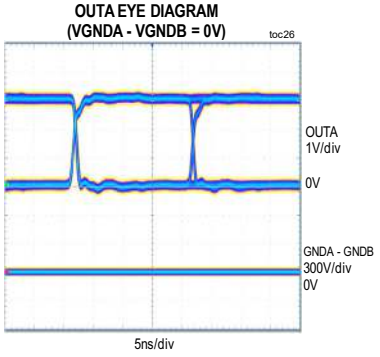
PROPAGATION DELAY vs. SUPPLY VOLTAGE



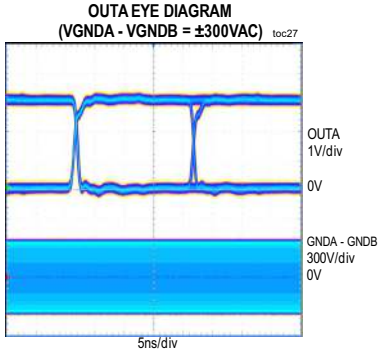
PROPAGATION DELAY vs. TEMPERATURE



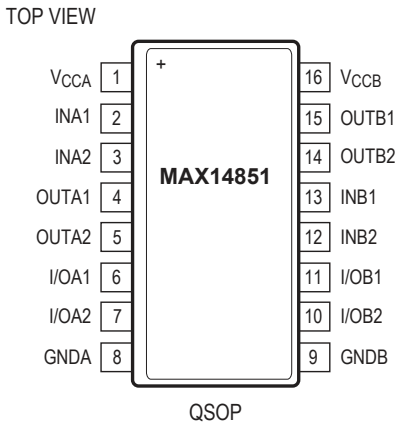
OUTA EYE DIAGRAM (VGNDA - VGNDB = 0V)



OUTA EYE DIAGRAM (VGNDA - VGNDB = ±300VAC)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION	REFERENCE
1	V_{CCA}	Supply Voltage of Logic Side A. Bypass V_{CCA} with a 0.1µF ceramic capacitor to GNDA.	GNDA
2	INA1	Logic Input 1 on Side A. INA1 is translated to OUTB1.	GNDA
3	INA2	Logic Input 2 on Side A. INA2 is translated to OUTB2.	GNDA
4	OUTA1	Logic Output 1 on Side A. OUTA1 is a push-pull output.	GNDA
5	OUTA2	Logic Output 2 on Side A. OUTA2 is a push-pull output.	GNDA
6	I/OA1	Bidirectional Input/Output 1 on Side A. I/OA1 is translated to/from I/OB1 and is an open-drain output.	GNDA
7	I/OA2	Bidirectional Input/Output 2 on Side A. I/OA2 is translated to/from I/OB2 and is an open-drain output.	GNDA
8	GNDA	Ground Reference for Side A	—
9	GNDB	Ground Reference for Side B	—
10	I/OB2	Bidirectional Input/Output 2 on Side B. I/OB2 is translated to/from I/OA2 and is an open-drain output.	GNDB
11	I/OB1	Bidirectional Input/Output 1 on Side B. I/OB1 is translated to/from I/OA1 and is an open-drain output.	GNDB
12	INB2	Logic Input 2 on Side B. INB2 is translated to OUTA2.	GNDB
13	INB1	Logic Input 1 on Side B. INB1 is translated to OUTA1.	GNDB
14	OUTB2	Logic Output 2 on Side B. OUTB2 is a push-pull output.	GNDB
15	OUTB1	Logic Output 1 on Side B. OUTB1 is a push-pull output.	GNDB
16	V_{CCB}	Supply Voltage of Logic Side B. Bypass V_{CCB} with a 0.1µF ceramic capacitor to GNDB.	GNDB

Detailed Description

The MAX14851 is a six-channel digital isolator. The device is rated for 600V_{RMS} isolation voltage for 60 seconds. This digital isolator offers a low power, low-cost, and high electromagnetic interference (EMI) immunity through Maxim's proprietary process technology. The device uses a monolithic solution to isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. Four of the six channels are unidirectional, two in each direction. All four unidirectional channels support data rates of up to 50Mbps. The other two channels are bidirectional with data rates up to 2Mbps.

Isolation of I^2C, SPI/MICROWIRE, and other serial busses can be achieved with the MAX14851. The device features two supply inputs, V_{CCA} and V_{CCB}, that independently set the logic levels on either side of the device. V_{CCA} and V_{CCB} are referenced to GNDA and GNDB, respectively. The MAX14851 also features a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The MAX14851 provides galvanic isolation for digital signals that are transmitted between two ground domains. Up to 200V_{RMS} of continuous isolation is supported as well as transient differences of up to 850V.

Level Shifting

In addition to isolation, the MAX14851 can be used for level translation. V_{CCA} and V_{CCB} can be independently set to any voltage from 3.0V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional and Bidirectional Channels

The MAX14851 operates both as a unidirectional device and bidirectional device simultaneously. Each unidirectional channel can only be used in the direction shown in the functional diagram. The bidirectional channels function without requiring a direction control input.

Unidirectional Channels

The device features four unidirectional channels that operate independently with guaranteed data rates from DC to 50Mbps. The output driver of each unidirectional channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Bidirectional Channels

The device features two bidirectional channels that have open-drain outputs. The bidirectional channels do not require a direction control input. A logic-low on one side causes the corresponding pin on the other side to be pulled low while avoiding data latching within the device. I/OA1 and I/OA2 outputs comprise special buffers that regulate the logic-low voltage at approximately 0.7V. The input logic-low threshold (V_{IT}) of I/OA1 and I/OA2 is at least 50mV lower than the output logic-low voltage of I/OA1 and I/OA2. This prevents an output logic-low on side A from being accepted as an input low and subsequently transmitted to side B; thus, preventing a latching action. I/OB1 and I/OB2 are conventional outputs that do not regulate the logic-low output voltage.

Due to their nature, the A-side output buffers of the MAX14851 cannot be connected together, or to a device with similar buffers or rise-time accelerators. The B-side output buffers of the MAX14851, instead can be connected together, or to any other bidirectional buffer or level translator.

The I/OA1, I/OA2, I/OB1, and I/OB2 pins have open-drain outputs, requiring pullup resistors to their respective supplies for logic-high outputs. The output low voltages are guaranteed for sink currents of up to 35mA for side B, and 3.5mA for side A (see the *DC Electrical Characteristics* table).

Startup and Undervoltage Lockout

The V_{CCA} and V_{CCB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a slump in the supplies. When an undervoltage event is detected on either of the supplies, all

Table 1. Output Behavior During Undervoltage Conditions

V_{IN}	V_{CCA}	V_{CCB}	$V_{OUTA\_}$	$V_{OUTB\_}$
1	Powered	Powered	1	1
0	Powered	Powered	0	0
X	Undervoltage	Powered	Follows V_{CCA}	1
X	Powered	Undervoltage	1	Follows V_{CCB}

outputs on both sides are automatically controlled, regardless of the status of the inputs (Table 1). The bidirectional outputs become high impedance and are pulled high by the external pullup resistor on the open-drain output. The unidirectional outputs are pulled high internally to the voltage of the V_{CCA} or V_{CCB} supply during undervoltage conditions.

Figure 3 shows an example of the behavior of the outputs during power-up and power-down. This behavior is symmetrical for V_{CCA} and V_{CCB} rising/falling.

Safety Regulatory Approvals

The MAX14851AEE+ is safety certified by UL. Per UL1577, the MAX14851 is 100% tested at an equivalent V_{ISO} of 720V_{RMS} for one second (see Table 2).

Applications Information

Effect of Continuous Isolation on Lifetime

High-voltage conditions cause insulation to degrade over time. Higher voltages result in faster degradation. Even the high-quality insulating material used in the MAX14851 can degrade over long periods of time with a constant high-voltage across the isolation barrier. Figure 4 shows the life expectancy of the MAX14851 vs. working isolation voltage.

Power Supply Sequencing

The MAX14851 does not require special power-supply sequencing. The logic levels are set independently on either side by V_{CCA} and V_{CCB}. Each supply can be present over the entire specified range regardless of the level or presence of the other.

Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{CCA} and V_{CCB} with 0.1µF ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power-supply input pins as possible.

Table 2. Safety Regulatory Approvals

SAFETY AGENCY	STANDARD	ISOLATION NUMBER	FILE NUMBER
UL	UL1577 Recognized	600V_{RMS} isolation voltage for 60 seconds	E351759

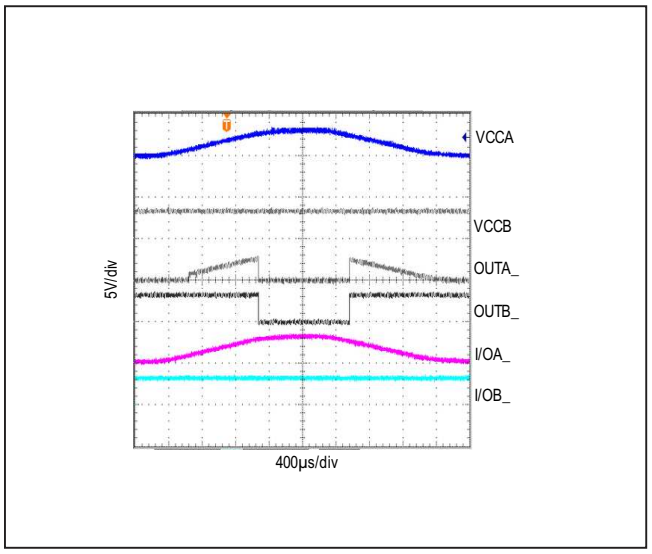


Figure 3. Undervoltage Lockout Behavior

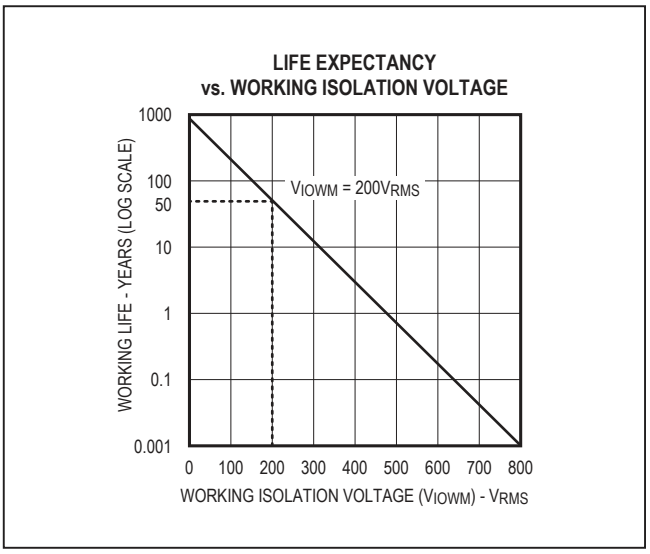


Figure 4. Life Expectancy vs. Working Isolation Voltage

Calculating Power Dissipation

The MAX14851 dissipates power based on the switching data rate of the input and output channels, and loads on the channel outputs. The required current for a given supply (V_{CCA} or V_{CCB}) can be estimated by summing the current required for each channel. The supply current for a channel depends on whether the channel is an input or an output, the channel's data rate, and the capacitive or resistive load, if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in Figure 5 and Figure 6. Please note the data in Figure 5 and Figure 6 are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the "no load" current (shown in Figure 5 and Figure 6) which is a function of Voltage and Data Rate, and the "load current" which depends upon the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{CC}$$

where

I_{CL} is the current required to drive the capacitive load.

C_L is the load capacitance on the isolator's output pin.

f_{SW} is the switching frequency (bits per second / 2).

V_{CC} is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, the supply voltage and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{CC} / R_L$$

where

I_{RL} is the current required to drive the resistive load.

V_{CC} is the supply voltage on the output side of the isolator.

R_L is the load resistance on the isolator's output pin.

The required supply current for switching bidirectional open-drain inputs/outputs is negligible, and can be ignored when calculating power dissipation. Some current, however, will be pulled from the supply through the pull-up resistors on those pins. To calculate that current under worst-case conditions, assume that the I/O is always low and calculate the current as:

$$I_{IO} = V_{CC} / R_{PU}$$

where

I_{IO} is the current through the pull-up resistor.

V_{CC} is the supply voltage on the side of the bidirectional input/output.

R_{PU} is the pull-up resistance on the input/output.

Example (shown in Figure 7): A MAX14851 is operating with V_{CCA} = 3.3V, V_{CCB} = 5V.

The bidirectional channels (I/O_1 and I/O_2), in this application channel 1 (SCL) and channel 2 (SDA), implement an isolated I^2C Bus, operating at Fast Mode Plus (FM+) with a clock rate of 1MHz. As noted previously, the power dissipated in these channels during switching is negligible and will be ignored for further calculations.

The other 4 channels are unidirectional;

- INA1 is a 10MHz input driving an output OUTB1 which has a 10pF capactive load.
- INA2 is held low and the channel is not in use and the resistive load is negligible since the isolator is driving a CMOS input.
- Similarly, INB1 is held low and the channel is not in use and the load current from OUTA1 is considered negligible.
- INB2 is a 5MHz input driving an output OUTA2 which has a with a 10kΩ resistive load.

Refer to Table 3 and Table 4 for the V_{CCA} and V_{CCB} supply current calculation worksheets.

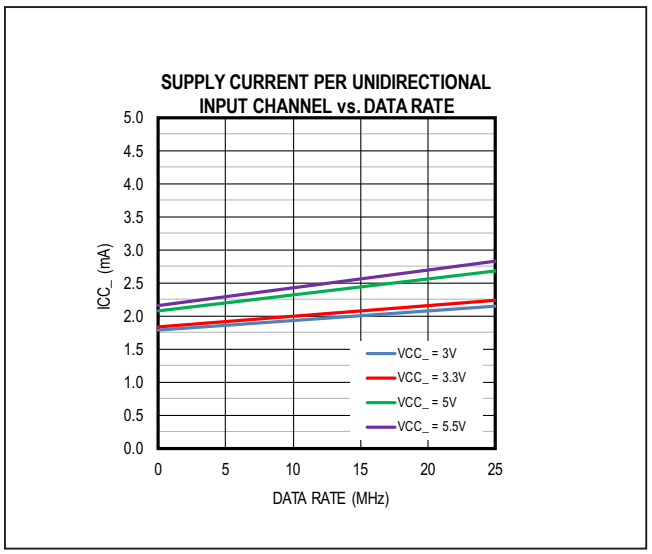


Figure 5. Supply Current per Input Channel (Estimated)

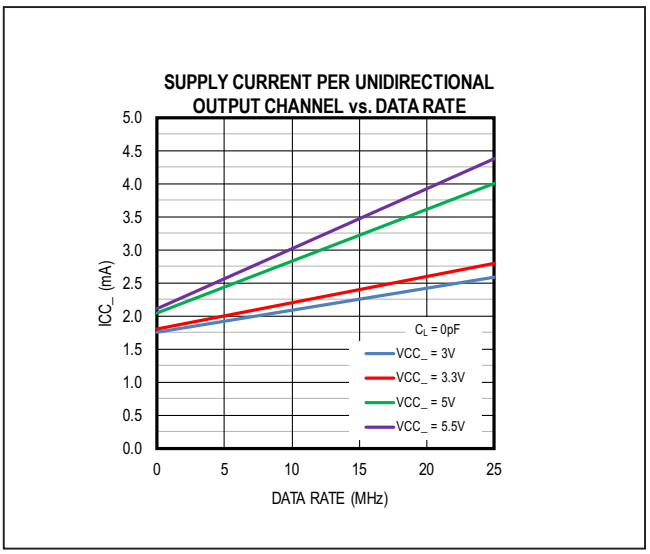


Figure 6. Supply Current per Output Channel (Estimated)

Table 3. Side A Power Dissipation Calculation Worksheet

SIDE A	VCCA = 3.3V					
Channel	**IN/OUT**	**Data Rate (MHz)**	**Load Type**	**Load**	**"No Load" Current (mA)**	**Load Current (mA)**
INA1	IN	10	—	—	1	—
INA2	IN	0	—	—	1.8	—
OUTA1	OUT	0	—	—	1.8	—
OUTA2	OUT	5	Resistive	10kΩ	2	0.33
				TOTAL	6.6	0.33
				TOTAL CURRENT	6.93	
				CALCULATED POWER DISSIPATION FOR SIDE A	VCCA x ICCA = 3.3V x 6.93mA = 22.9mW	

Table 4. Side B Power Dissipation Calculation Worksheet

SIDE B	VCCB = 5.0V					
Channel	**IN/OUT**	**Data Rate (MHz)**	**Load Type**	**Load**	**"No Load" Current (mA)**	**Load Current (mA)**
OUTB1	OUT	10	Capacitive	10pF	2.8	0.5
OUTB2	OUT	0	—	—	2.1	—
INB1	IN	0	—	—	2.2	—
INB2	IN	5	—	10kΩ	2.3	0.5
				TOTAL	9.4	1.0
				TOTAL CURRENT	10.4	
				TOTAL POWER DISSIPATION FOR SIDE B	VCCB x ICCB = 5V x 10.4mA = 52mW	

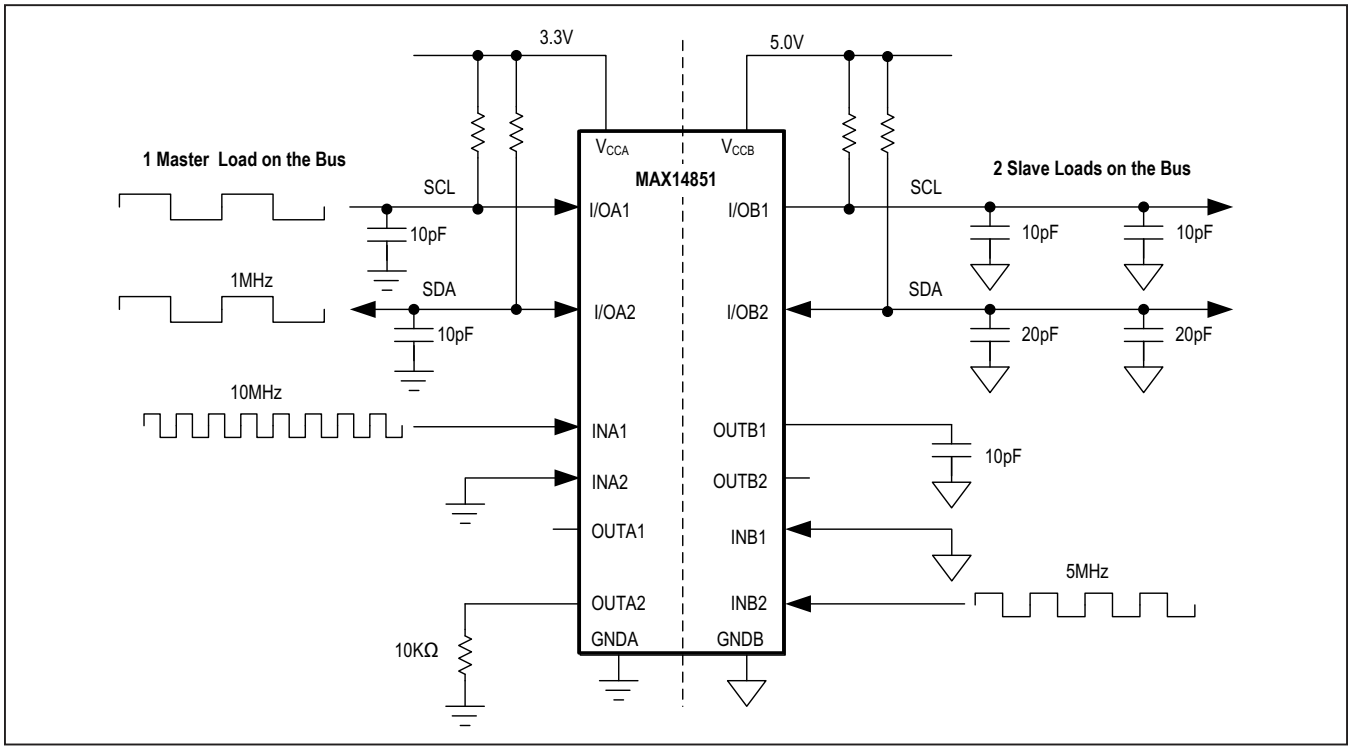
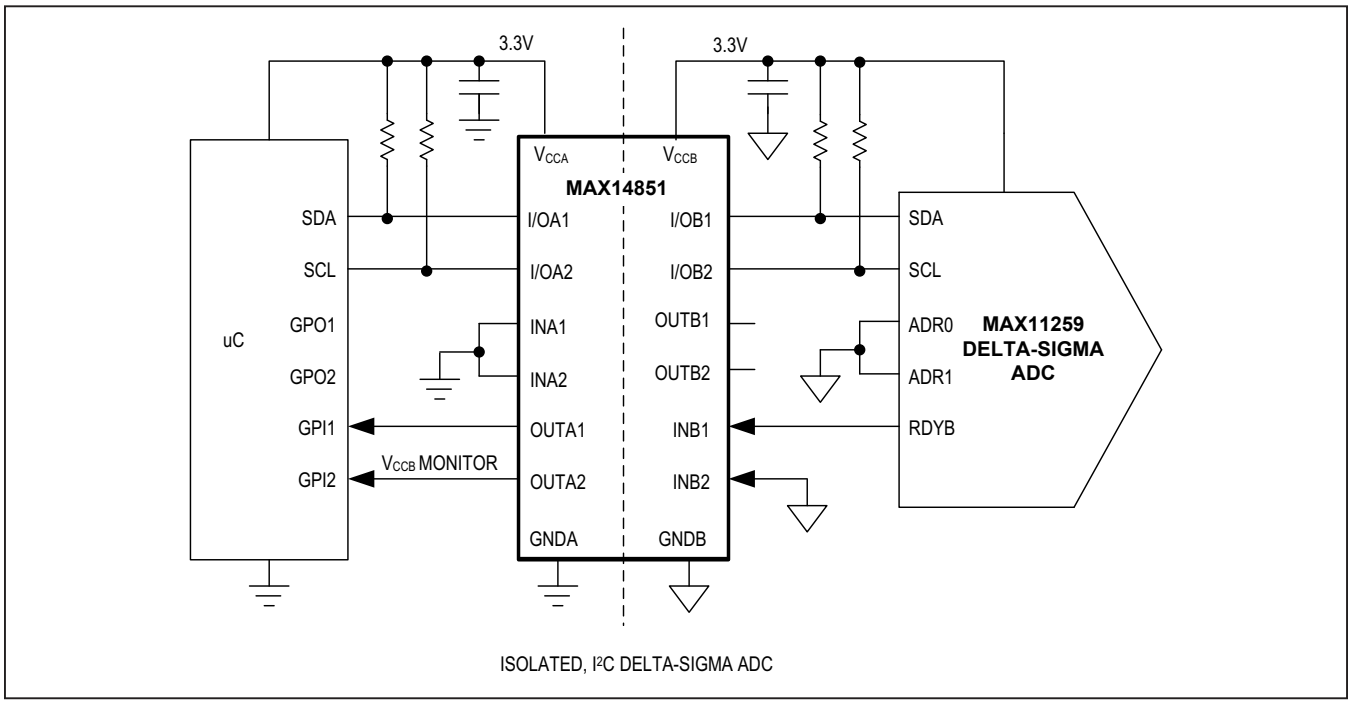
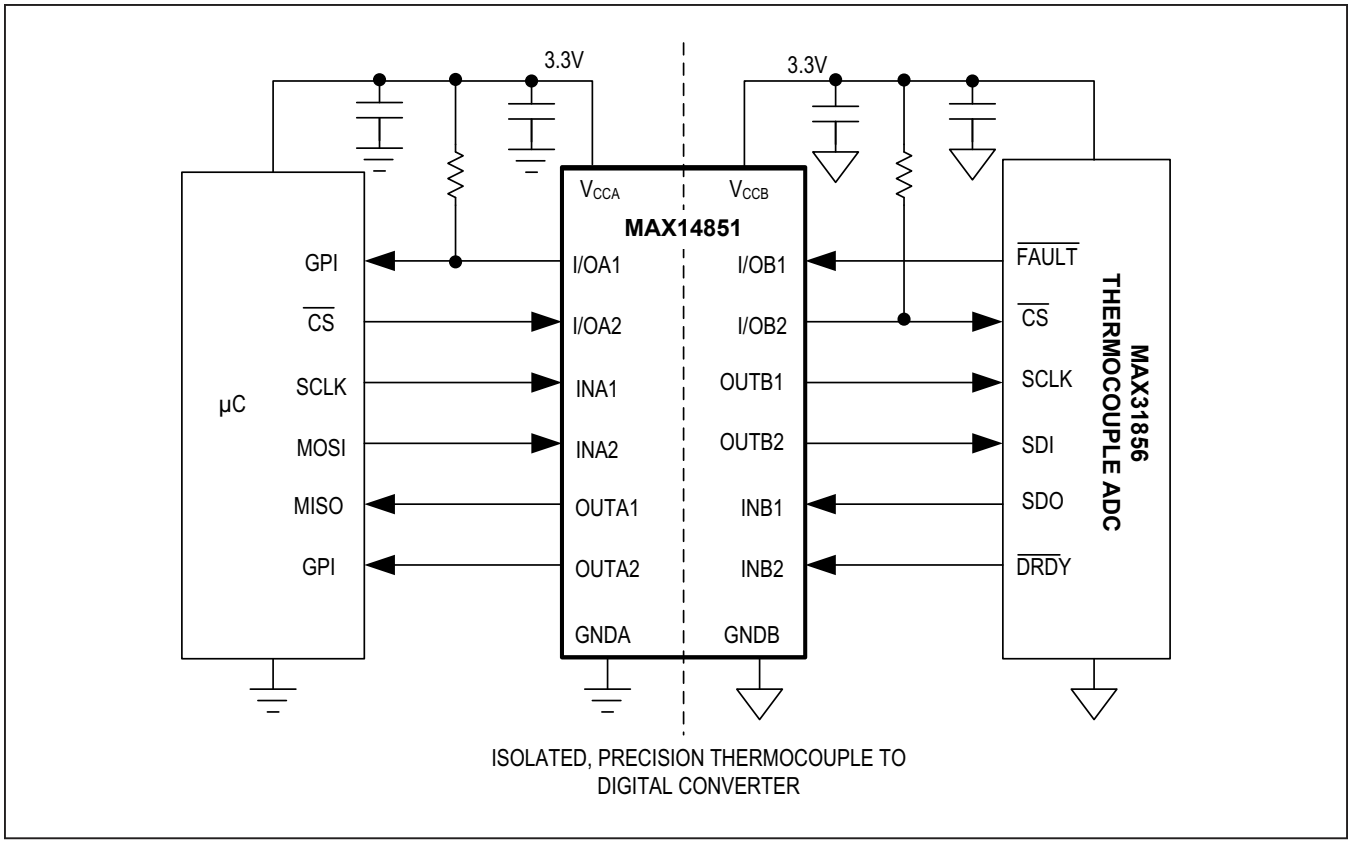


Figure 7. Example Circuit for Supply Current Calculation

Typical Operating Circuits



Typical Operating Circuits (continued)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14851AEE+	-40°C to +125°C	16 QSOP
MAX14851AEE+T	-40°C to +125°C	16 QSOP

+Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape and Reel

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+1	21-0055	90-0167

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	7/19	Updated the *General Description*, *Electrical Characteristics* and *Bidirectional Channels* sections, and Table 1	1–2, 4–6, 13

