PLL AUDIO CLOCK SYNTHESIZER

MK2704

Description

The MK2704 is a low cost, low jitter, high-performance PLL clock synthesizer designed to replace oscillators and PLL circuits in set-top box and multimedia systems. Using IDT's patented analog Phase Locked Loop (PLL) techniques, the device uses a 27 MHz crystal or clock input to produce a buffered reference clock and a selectable audio clock.

The audio clock is frequency locked to the 27 MHz clock, assuring that the audio with zero ppm error and video will track perfectly.

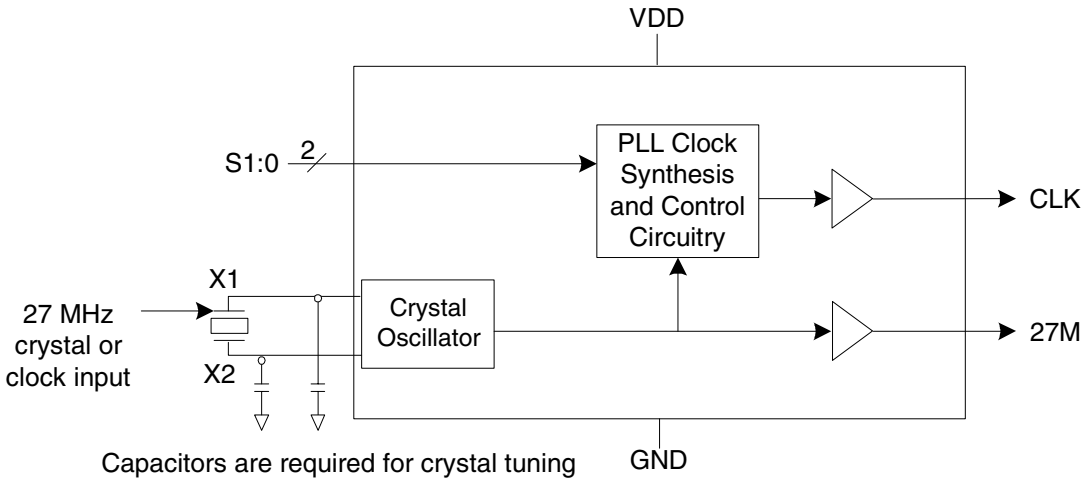
IDT manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. Consult IDT to eliminate VCXOs, crystals and oscillators from your board.

Features

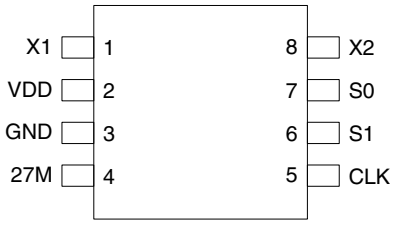
- Packaged in 8-pin SOIC
- Available in Pb-free packaging
- Uses an inexpensive, fundamental crystal or clock
- Selectable audio output clock of 16.9344 MHz, 18.432 MHz, or 36.864 MHz
- Supports MPEG sampling rates of 384x, 44.1 kHz, 48 kHz, and 96 kHz
- Patented zero ppm synthesis error in all clocks
- All frequencies are frequency locked
- 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3 V or 5 V

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



8-pin (150 mil) SOIC

AUDIO CLOCK OUTPUT SELECT TABLE

S1	S0	CLK (MHz)
0	0	36.864
0	1	Test
1	0	16.9344
1	1	18.432

Key: 0 = Connect pin directly to ground

1 = Connect pin directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	XI	Crystal Connection. Connect to a 27 MHz fundamental crystal or clock.
2	VDD	Power	Connect to +3.3 V or +5 V.
3	GND	Power	Connect to ground.
4	27M	Output	27.00 MHz buffered reference clock output.
5	CLK	Output	Audio clock output per table above.
6	S1	Input	Audio clock frequency select input #1. Determines CLK output per table above. Internal pull-up resistor.
7	S0	Input	Audio clock frequency select input #0. Determines CLK output per table above. Internal pull-up resistor.
8	X2	XO	Crystal connection to a 27 MHz crystal, or leave unconnected for clock output.

External Components

Decoupling Capacitor

As with any high performance mixed-signal IC, the MK2704 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and GND on pins 2 and 3. It must be connected close to the MK2704 to minimize lead inductance. No external power supply filtering is required for the MK2704.

Series Termination Resistor

A 33Ω terminating resistor can be used next to the clock outputs for trace lengths over one inch.

Crystal Load Capacitors

The total on-chip capacitance is approximately 16 pF. A parallel resonant, fundamental mode, AT cut 27 MHz crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the

stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -16 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with an 18 pF load capacitance, each crystal capacitor would be 4 pF [(18-16) x 2] = 4.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2704. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.13		+5.50	V

DC Electrical Characteristics

VDD=3.3 V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.13		5.50	V
Input High Voltage	V_{IH}	X1 pin only Note 1	(VDD/2)+1	VDD/2		V
Input Low Voltage	V_{IL}	X1 pin only Note 1		VDD/2	(VDD/2)-1	V
Input High Voltage	V_{IH}	S0, S1 pins	2.0			V
Input Low Voltage	V_{IL}	S0, S1 pins			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No load VDD = 3.3.V		10		mA
		No load VDD = 5 V		18		mA
Short Circuit Current		CLK output		±50		mA
Input Capacitance	C_{IN}	S0, S1 pins		5		pF
Nominal Output Impedance				20		Ω
Frequency Synthesis Error		All Clocks			0	ppm

Note 1: CMOS level input. Nominal trigger point is VDD/2 for 3.3 V or 5 V operation

AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Crystal or Clock Frequency	F_{IN}			27		MHz
Input Crystal Accuracy					±30	ppm
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V, Note 1			1.5	ns
Output Clock Fall Time	t_{OF}	2.0 to 8.0 V, Note 1			1.5	ns
Output Clock Duty Cycle		at VDD/2, Note 1	45		55	%
Maximum Absolute Jitter, short	t_{ja}	Deviation from mean		±225		ps

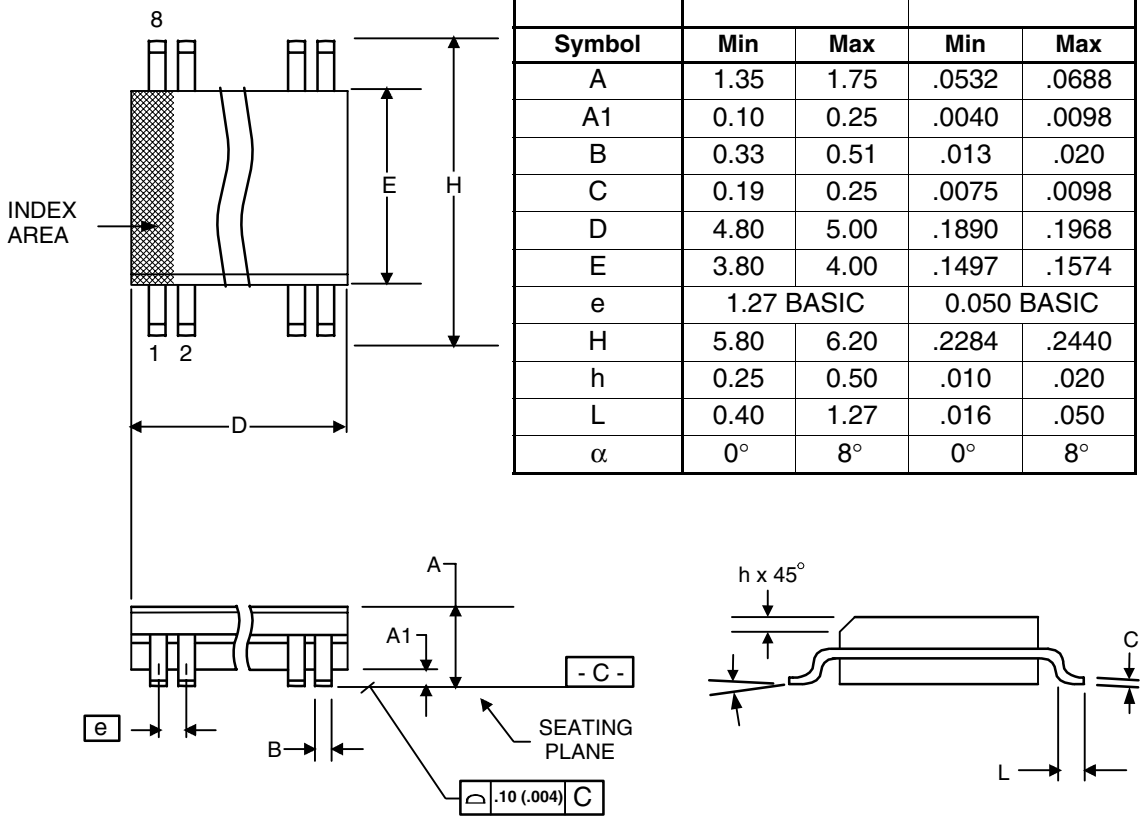
Note 1: Measured with 15 pF load.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
MK2704S*	2704S	Tubes	8-pin SOIC	0 to +70° C
MK2704STR*	2704S	Tape and Reel	8-pin SOIC	0 to +70° C
MK2704SLF	2704SL	Tubes	8-pin SOIC	0 to +70° C
MK2704SLFTR	2704SL	Tape and Reel	8-pin SOIC	0 to +70° C

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