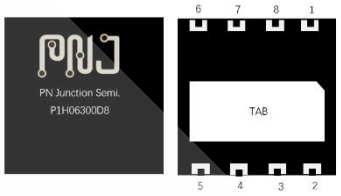
GaN HEMT P1H06300D8

650V GaN Enhancement Mode Power Transistor



Features

- Ultra Fast Switching
- No Reverse-Recovery Charge
- Capable of Reverse Conduction
- Low Gate Charge, Low Output Charge

Gate	5
Source	2, 3, 4, TAB
Drain	1, 6, 7, 8

Standards Benefits

- Improves System Efficiency
- Improves Power Density
- Enable Higher Operating Frequency
- System Cost Reduction Savings

RoHS

Halogen

Application

- Consumer SMPS
- High Density Chargers Based on the Half-Bridge Topology
- Totem Pole PFC, High Frequency LLC and Flyback

Order Information

Part number	Package	Marking
P1H06300D8	DFN 8 X 8	P1H06300D8

Contents

1. Maximum Ratings

At T_J=25 ℃, unless specified otherwise

Parameter	Symbol	Value	Unit	Test Conditions
Drain - Source Voltage	V_{DSmax}	650	V	V_{GS}= 0 V
Gate - Source Voltage (Dynamic)	V_{GSmax}	-20 / +10	V	AC (F >1 Hz)
Gate - Source Voltage (Static)	V_{GSop}	-8/ +6	V	Static
Continuous Drain Current	I_D	10	A	V_{GS}= 6 V, T_C= 25 ℃
		6		V_{GS}= 6 V, T_C= 100 ℃
Power Dissipation	P_{tot}	55.5	W	T_C=25℃
Operating Junction Temperature	T_J	-55 To +150	℃	
Storage Temperature	T_{stg}	-55 To +150	℃	

2. Thermal Characteristics

Parameter	Symbol	Value		Unit	Test Conditions
		Typ.	Max.		
Thermal Resistance from Junction to Case	$R_{\theta JC}$	/	2.25	℃/W	
Thermal Resistance from Junction to Case	$R_{\theta JA}$	/	60		

3. Electrical Characteristics

At T_J=25℃, unless specified otherwise

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Breakdown Voltage	V_{BV}	650	/	/	V	V_{GS}=0V
Threshold Voltage	V_{TH}	/	1.3	/	V	V_{DS}=5V, I_{DS}=1mA
On-state Resistance	$R_{DS(on)}$	230	240	300	mΩ	V_{GS}=6V, I_{DS}=5A
Drain-Source leakage current	I_{DSS}	/	15	200	nA	V_{GS}=0V, V_{DS}=650V
Gate leakage current	I_{GSS}	/	4.9	16.9	μA	V_{GS}=6V, V_{DS}=0V
Input Capacitance	C_{ISS}	/	66.8	/	pF	V_{DS} = 400 V V_{GS} = 0 V, f = 1MHz
Output Capacitance	C_{OSS}	/	27.3	/	pF	
Reverse Transfer Capacitance	C_{RSS}	/	0.7	/	pF	
Total Gate Charge	Q_G	/	3.1	/	nC	V_{DS} = 400 V V_{GS} = 6V
Gate-to-Source Charge	Q_{GS}	/	0.46	/	nC	
Gate-to-Drain Charge	Q_{GD}	/	1.7	/	nC	
Output Charge	Q_{OSS}	/	3.1	/	nC	V_{DS} = 400 V V_{GS} = 6V, f = 1MHz
Reverse Recovery Charge	Q_{RR}	/	0	/		
Output Capacitance Stored Energy	E_{OSS}	/	0.44	/	μJ	V DS = 400 V V GS = 0 V, f = 1MHz

4. Typical Performance

At T_J=25℃, unless specified otherwise

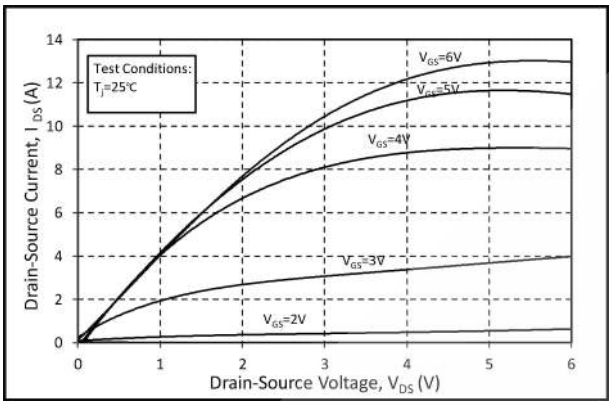


Fig.1 Output Characteristics TJ= 25℃

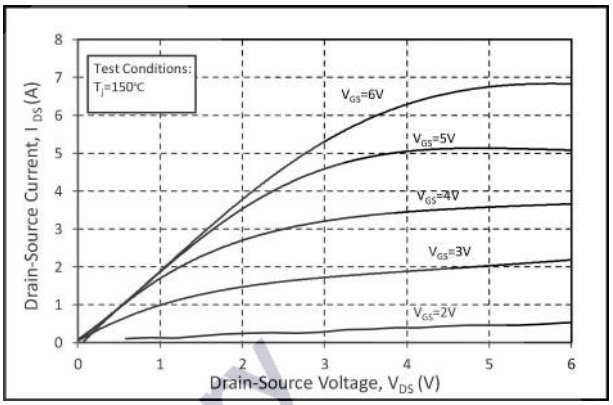


Fig.2 Output Characteristics TJ= 150℃

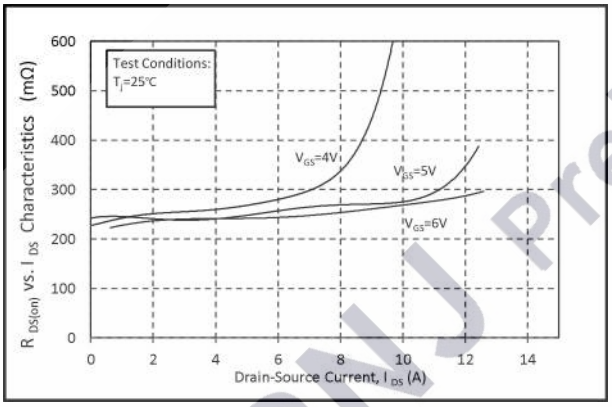


Fig.3 On-Resistance For Various Gate Voltage

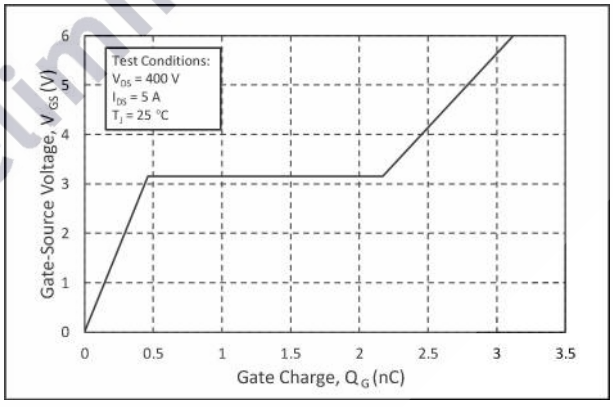


Fig.4 Gate Charge Characteristics

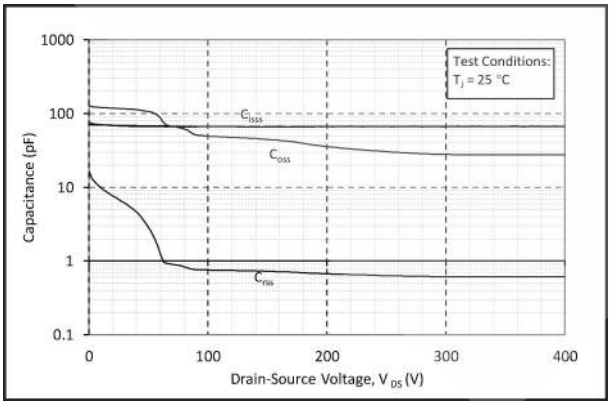


Fig.5 Capacitances vs. Drain-Source Voltage

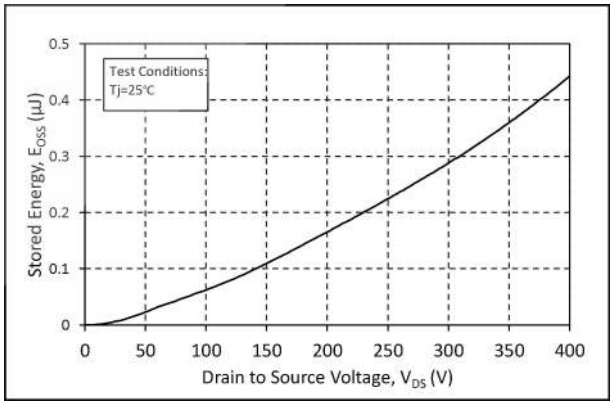


Fig.6 Output Capacitor Stored Energy

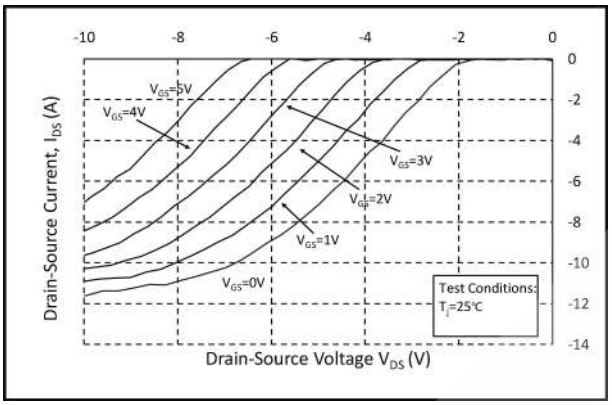


Fig.7 Reverse Conduction Characteristics

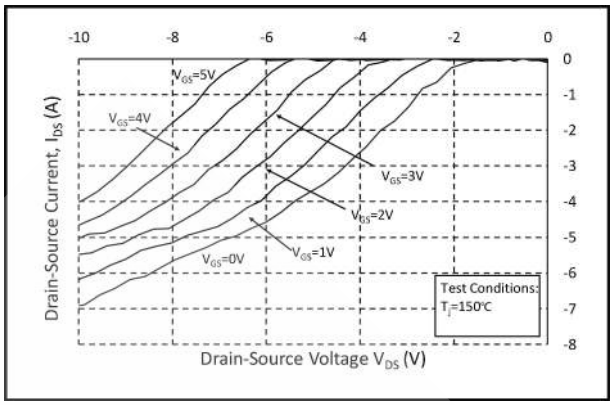


Fig.8 Reverse Conduction Characteristics

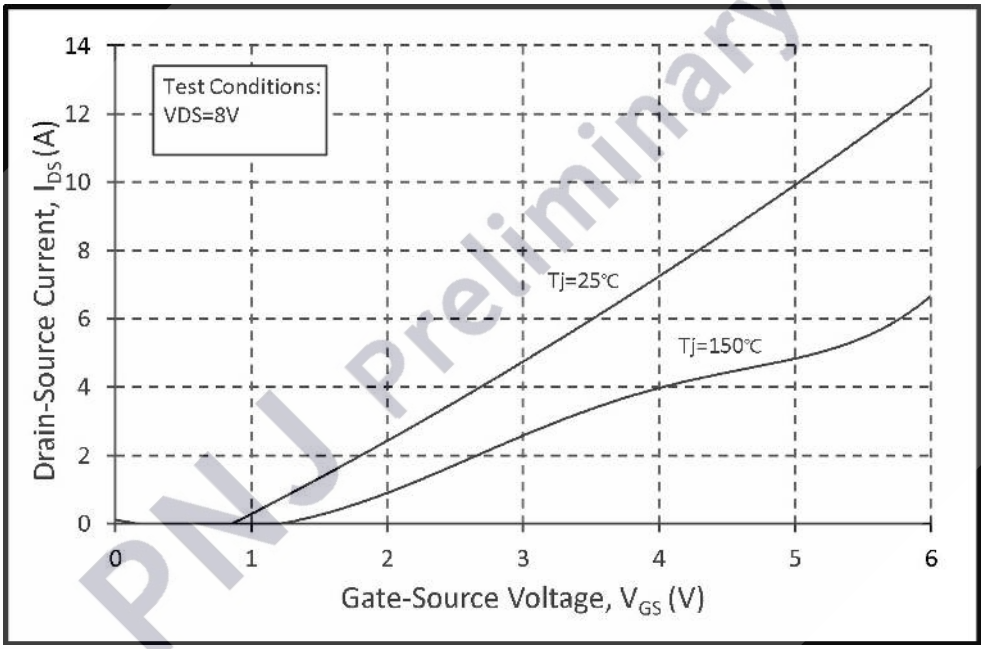


Fig.9 Transfer Characteristic for
Various Junction Temperatures

5. Package Outlines

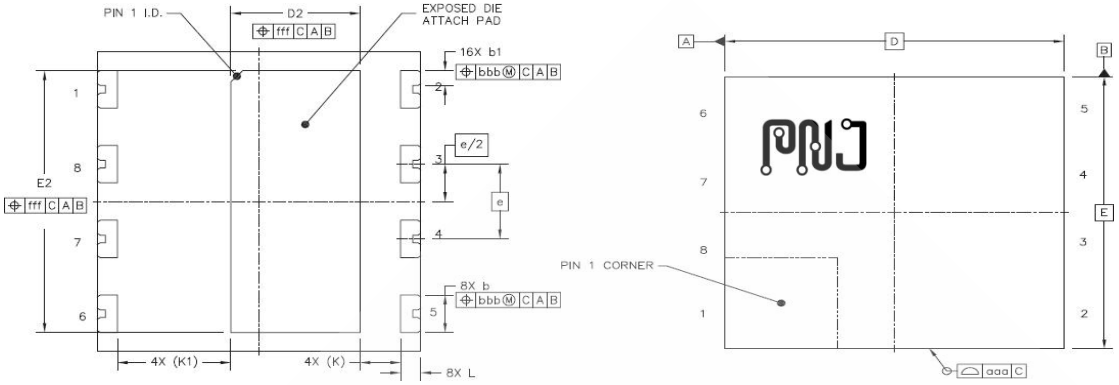
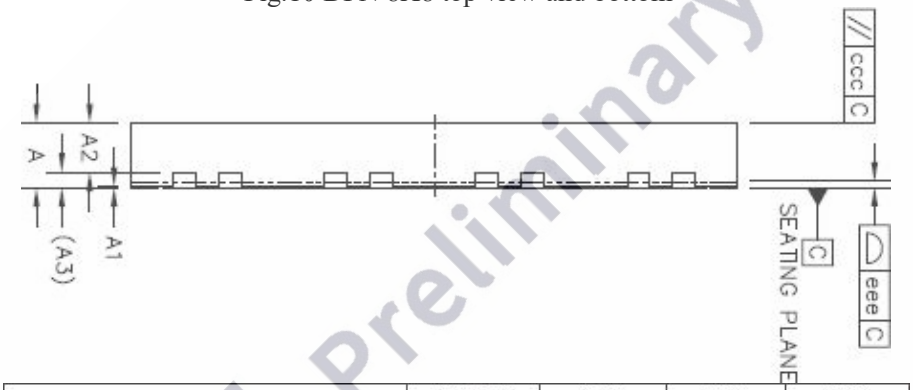


Fig.10 DFN 8X8 top view and bottom



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.9	1	1.1
LEAD WIDTH		b1	0.35	0.4	0.45
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		2 BSC	
EP SIZE	X	D2	3.1	3.2	3.3
	Y	E2	6.9	7	7.1
LEAD LENGTH		L	0.4	0.5	0.6
LEAD TIP TO EXPOSED PAD EDGE		K		1 REF	
LEAD TIP TO EXPOSED PAD EDGE		K1		2.8 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Fig.11 DFN 8X8 side view and dimensions (mm)