

TPS60204, TPS60205 Regulated 3.3-V, 100-mA Low-Ripple Charge Pump Low-Power DC/DC Converters

1 Features

- Regulated 3.3-V output voltage with up to 100-mA output current from a 1.8-V to 3.6-V input voltage
- Less than 5-mV_(PP) output voltage ripple achieved with push-pull topology
- Integrated low-battery and power-good detector
- Switching frequency can be synchronized to external clock signal
- Extends battery usage with up to 90% efficiency and 35- μ A quiescent supply current
- Easy-to-design, low cost, low EMI power supply since no inductors are used
- 0.05- μ A shutdown current, battery is isolated from load in shutdown mode
- Compact converter solution in ultrasmall 10-pin MSOP with only four external capacitors required
- Evaluation module available (TPS60200EVM-145)

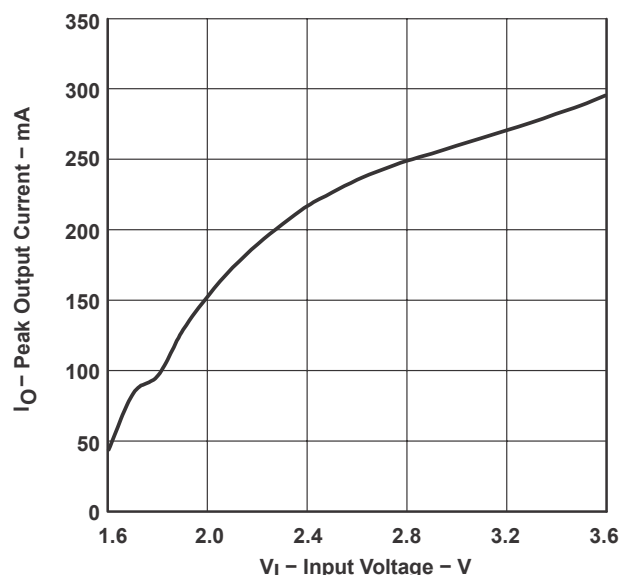
2 Applications

Replaces DC/DC converters with inductors in battery powered applications like:

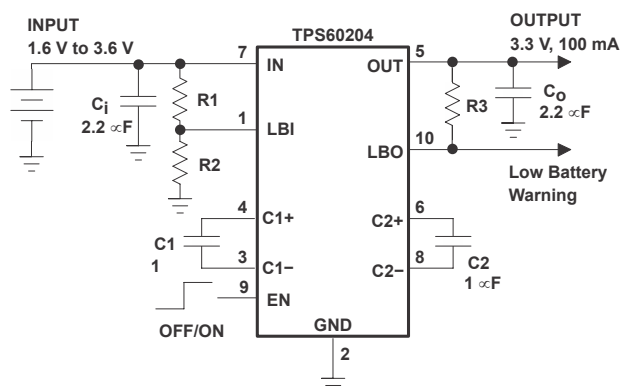
- Two battery cells to 3.3-V conversion
- MP3 portable audio players
- Battery-powered microprocessor systems
- Backup-battery boost converters
- PDA's, organizers, and cordless phones
- Handheld instrumentation
- Glucose meters and other medical instruments

3 Description

The TPS6020x step-up, regulated charge pumps generate a 3.3-V \pm 4% output voltage from a 1.8-V to 3.6-V input voltage. The devices are typically powered by two Alkaline, NiCd, or NiMH battery cells and operate down to a minimum supply voltage of 1.6 V. Continuous output current is a minimum of 100 mA from a 2-V input. Only four external capacitors are needed to build a complete low-ripple dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple, as current is continuously transferred to the output.



TPS60204 Peak Output Current Input Voltage



Typical Application Circuit With Low-Battery Warning



Table of Contents

1 Features	1	9.1 Application Information.....	16
2 Applications	1	9.2 Typical Application.....	18
3 Description	1	9.3 Power Dissipation.....	18
4 Revision History	2	9.4 Layout and Board Space.....	19
5 Description (continued)	3	10 Device and Documentation Support	20
6 Pin Configuration and Functions	4	10.1 Device Support.....	20
7 Specifications	5	10.2 Documentation Support.....	20
7.1 Absolute Maximum Ratings.....	5	10.3 Receiving Notification of Documentation Updates..	20
7.2 Dissipation Rating.....	5	10.4 Support Resources.....	20
7.3 Recommended Operating Conditions.....	5	10.5 Trademarks.....	20
7.4 Electrical Characteristics.....	5	10.6 Electrostatic Discharge Caution.....	20
7.5 Electrical Characteristics TPS60204.....	6	10.7 Glossary.....	20
7.6 Electrical Characteristics TPS60205.....	6	11 Mechanical, Packaging, and Orderable	
7.7 Typical Characteristics.....	7	Information	20
8 Detailed Description	11	11.1 Package Option Addendum.....	21
8.1 Functional Block Diagrams.....	15	11.2 Tape and Reel Information.....	22
9 Application and Implementation	16		

4 Revision History

Changes from Revision A (September 2001) to Revision B (May 2023)

Page

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| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
|--|---|

5 Description (continued)

The devices operate in the newly developed LinSkip mode. In this operating mode, the device switches seamlessly from the power saving pulse-skip mode at light loads to the low-noise constant-frequency, linear-regulation mode once the output current exceeds the LinSkip threshold of about 7 mA. Even in pulse-skip mode, the output ripple is maintained at a very low level because the output resistance of the charge pump is still regulated.

Three operating modes can be programmed using the EN pin. EN = low disables the device, shuts down all internal circuits, and disconnects the output from the input. EN = high enables the device and programs it to run from the internal oscillator. The devices operate synchronized to an external clock signal if EN is clocked; thus, switching harmonics can be controlled and minimized. The devices include a low-battery detector that issues a warning if the battery voltage drops below a user-defined threshold voltage, or a power-good detector that goes active when the output voltage reaches about 90% of its nominal value.

Device options with either a low-battery or power good detector are available. This dc/dc converter requires no inductors, therefore, EMI of the system is reduced to a minimum. It is available in the small 10-pin MSOP package (DGS).

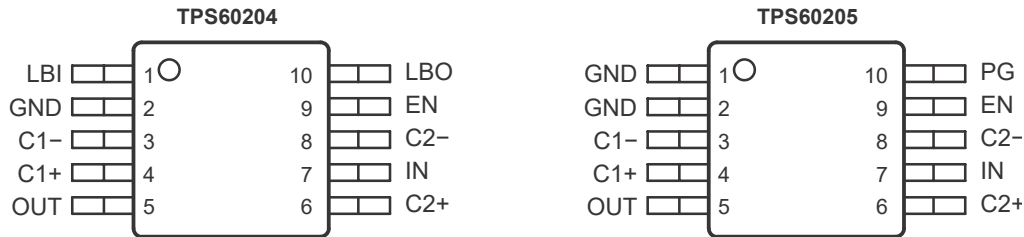
Table 5-1. Available Options

T _A	PART NUMBER ⁽¹⁾	MARKING DGS PACKAGE	OUTPUT CURRENT (mA)	OUTPUT VOLTAGE	DEVICE FEATURES
-40°C to 85°C	TPS60204DGS	AFB	100	3.3	Low-battery detector
	TPS60205DGS	AFC	100	3.3	Power-good detector

(1) The DGS package is available taped and reeled. Add R suffix to device type (e.g., TPS60204DGSR) to order quantities of 2500 devices per reel.

6 Pin Configuration and Functions

DGS PACKAGES



ACTUAL SIZE
3.05 mm x 4.98 mm

Table 6-1. Pin Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
C1+	4		Positive terminal of the flying capacitor C1
C1-	3		Negative terminal of the flying capacitor C1
C2+	6		Positive terminal of the flying capacitor C2
C2-	8		Negative terminal of the flying capacitor C2
EN	9	I	Device-enable input. Three operating modes can be programmed with the EN pin. – EN = Low disables the device. Output and input are isolated in the shutdown. – EN = High lets the device run from the internal oscillator. – If an external clock signal is applied to the EN pin, the device is in syncmode and runs synchronized at the frequency of the external clock signal.
GND	2		Ground
IN	7	I	Supply input. Bypass IN to GND with a capacitor of the same size as C_o .
LBI/GND	1	I	Low-battery detector input for the TPS60204. A low-battery warning is generated at the LBO pin when the voltage on LBI drops below the threshold of 1.18 V. Connect LBI to GND if the low-battery detector function is not used. For the TPS60205, this pin has to be connected to ground (GND pin).
LBO/PG	10	O	Open-drain low-battery detector output for the TPS60204. This pin is pulled low if the voltage on LBI drops below the threshold of 1.18 V. A pullup resistor should be connected between LBO and OUT or any other logic supply rail that is lower than 3.6 V. Open-drain power-good detector output for the TPS60205. As soon as the voltage on OUT reaches about 90% of its nominal value this pin goes active high. A pullup resistor should be connected between PG and OUT or any other logic supply rail that is lower than 3.6 V.
OUT	5	O	Regulated 3.3-V power output. Bypass OUT to GND with the output filter capacitor C_o .

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	IN to GND	-0.3	3.6	V
	EN, PG to GND	-0.3	3.6	
	LBI, LBO to GND	-0.3	3.6	
Output voltage	OUT to GND	-0.3	3.6	V
	C1+, C2+ to GND	-0.3	$V_O + 0.3$	V
	C1-, C2- to GND	-0.3	$V_I + 0.3$	
Output current	OUT		150	mA
Storage temperature	T_{stg}	-55	150	°C
Maximum junction temperature	T_J		150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Dissipation Rating

PACKAGE ⁽¹⁾	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DGS	424mW	3.4mW/°C	187mW	136mW

- (1) The thermal resistance junction to ambient of the DGS package is $R_{TH-JA} = 294^\circ\text{C/W}$

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Input voltage range	V_I	1.6		3.6	V
Input capacitor	C_i		2.2		μF
Flying capacitors	C1, C2		1		μF
Output capacitor	C_o		2.2		μF
Operating junction temperature	T_J	-40		125	°C

7.4 Electrical Characteristics

electrical characteristics at $C_i = 2.2 \mu\text{F}$, $C_1 = C_2 = 1 \mu\text{F}$, $C_o = 2.2 \mu\text{F}$, $T_A = -40^\circ\text{C}$ to 85°C , $V_I = 2.4 \text{ V}$, $\text{EN} = V_I$ (unless otherwise noted) over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O(\text{MAX})}$	Maximum continuous output current $V_I = 2 \text{ V}$	100			mA
V_O	Output voltage	$1.6 \text{ V} < V_I < 1.8 \text{ V}$, $0 < I_O < 0.25 \times I_{O(\text{MAX})}$	3		V
		$1.8 \text{ V} < V_I < 2 \text{ V}$, $0 < I_O < 0.5 \times I_{O(\text{MAX})}$	3.17	3.43	
		$2 \text{ V} < V_I < 3.3 \text{ V}$, $0 < I_O < I_{O(\text{MAX})}$	3.17	3.43	
		$3.3 \text{ V} < V_I < 3.6 \text{ V}$, $0 < I_O < I_{O(\text{MAX})}$	3.17	3.47	
V_{PP}	Output voltage ripple $I_O = I_{O(\text{MAX})}$		5		mV _{PP}
$I_{(Q)}$	Quiescent current (no-load input current) $I_O = 0 \text{ mA}$, $V_I = 1.8 \text{ V}$ to 3.6 V		35	70	μA
$I_{(SD)}$	Shutdown supply current $\text{EN} = 0 \text{ V}$		0.05	1	

7.4 Electrical Characteristics (continued)

electrical characteristics at $C_i = 2.2 \mu\text{F}$, $C_1 = C_2 = 1 \mu\text{F}$, $C_O = 2.2 \mu\text{F}$, $T_A = -40^\circ\text{C}$ to 85°C , $V_I = 2.4 \text{ V}$, $\text{EN} = V_I$ (unless otherwise noted) over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(\text{OSC})}$	Internal switching frequency		200	300	400	kHz
$f_{(\text{SYNC})}$	External clock signal frequency		400	600	800	
	External clock signal duty cycle		30%		70%	
V_{IL}	EN input low voltage	$V_I = 1.6 \text{ V}$ to 3.6 V			$0.3 \times V_I$	V
V_{IH}	EN input high voltage	$V_I = 1.6 \text{ V}$ to 3.6 V	$0.7 \times V_I$			
$I_{\text{kg(EN)}}$	EN input leakage current	$\text{EN} = 0 \text{ V}$ or V_I		0.01	0.1	μA
	Output capacitor auto discharge time	EN is set from V_I to GND, Time until $V_O < 0.5 \text{ V}$		0.6		ms
	Output leakage current in shutdown	$\text{EN} = 0 \text{ V}$, $T_A = -40$ to 85°C			5	μA
		$\text{EN} = 0 \text{ V}$, $T_A \leq 65^\circ\text{C}$			3	
	LinSkip threshold	$V_I = 2.2 \text{ V}$		7		mA
	Output load regulation	$10 \text{ mA} < I_O < I_{O(\text{MAX})}$; $T_A = 25^\circ\text{C}$			0.01	%/mA
	Output line regulation	$2 \text{ V} < V_I < 3.3 \text{ V}$, $I_O = 0.5 \times I_{O(\text{MAX})}$, $T_A = 25^\circ\text{C}$		0.6		%/V
$I_{(\text{SC})}$	Short circuit current	$V_I = 2.4 \text{ V}$, $V_O = 0 \text{ V}$		60		mA

7.5 Electrical Characteristics TPS60204

electrical characteristics for low-battery comparator of device TPS60204 at $T_A = -40^\circ\text{C}$ to 85°C , $V_I = 2.4 \text{ V}$ and $\text{EN} = V_I$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(\text{LBI})}$	LBI trip voltage	$V_I = 1.6 \text{ V}$ to 2.2 V , $T_C = 0^\circ\text{C}$ to 70°C	1.13	1.18	1.23	V
	LBI trip voltage hysteresis	For rising voltage at LBI		10		mV
$I_{(\text{LBI})}$	LBI input current	$V_{(\text{LBI})} = 1.3 \text{ V}$		2	50	nA
$V_{O(\text{LBO})}$	LBO output voltage low	$V_{(\text{LBI})} = 0 \text{ V}$, $I_{(\text{LBO})} = 1 \text{ mA}$			0.4	V
$I_{\text{kg(LBO)}}$	LBO leakage current	$V_{(\text{LBI})} = 1.3 \text{ V}$, $V_{(\text{LBO})} = 3.3 \text{ V}$		0.01	0.1	μA

Note

During start-up of the converter the LBO output signal is invalid for the first 500 μs .

7.6 Electrical Characteristics TPS60205

electrical characteristics for power-good comparator of device TPS60205 at $T_A = -40^\circ\text{C}$ to 85°C , $V_I = 2.4 \text{ V}$ and $\text{EN} = V_I$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(\text{PG})}$	Power-good trip voltage	$T_C = 0^\circ\text{C}$ to 70°C	$0.87 \times V_O$	$0.91 \times V_O$	$0.95 \times V_O$	V
$V_{\text{hys(PG)}}$	Power-good trip voltage hysteresis	V_O decreasing, $T_C = 0^\circ\text{C}$ to 70°C		1%		
$V_{O(\text{PG})}$	Power-good output voltage Low	$V_O = 0 \text{ V}$, $I_{(\text{PG})} = 1 \text{ mA}$			0.4	V
$I_{\text{kg(PG)}}$	Power-good leakage current	$V_O = 3.3 \text{ V}$, $V_{(\text{PG})} = 3.3 \text{ V}$		0.01	0.1	μA

Note

During start-up of the converter the PG output signal is invalid for the first 500 μs .

7.7 Typical Characteristics

Table 7-1. Table of Graphs

			FIGURES
η	Efficiency	vs Output current (TPS60204, TPS60205)	7-1
		vs Input voltage	7-2
I_Q	Quiescent supply current	vs Input voltage	7-3
V_O	Output voltage	vs Output current	7-4
		vs Input voltage	7-5
V_O	Output voltage ripple	vs Time	7-6, 7-7, 7-8
	Start-up timing		7-9
	Load transient response		7-10, 7-11
I_O	Peak output current	vs Input voltage	7-12

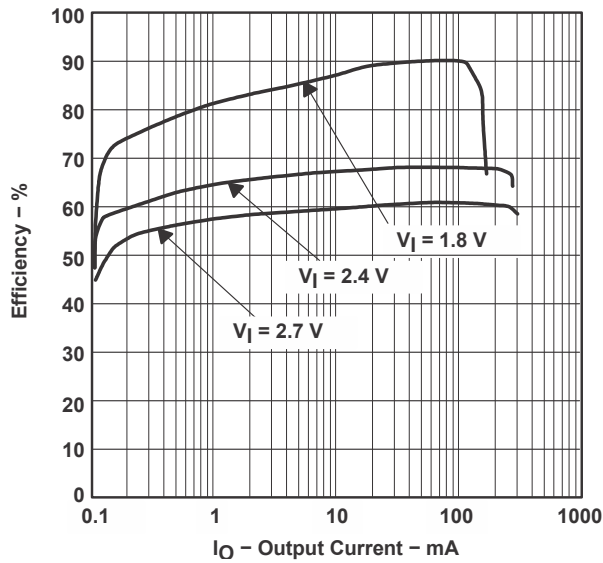


Figure 7-1. TPS60204, TPS60205 Efficiency vs Output Current

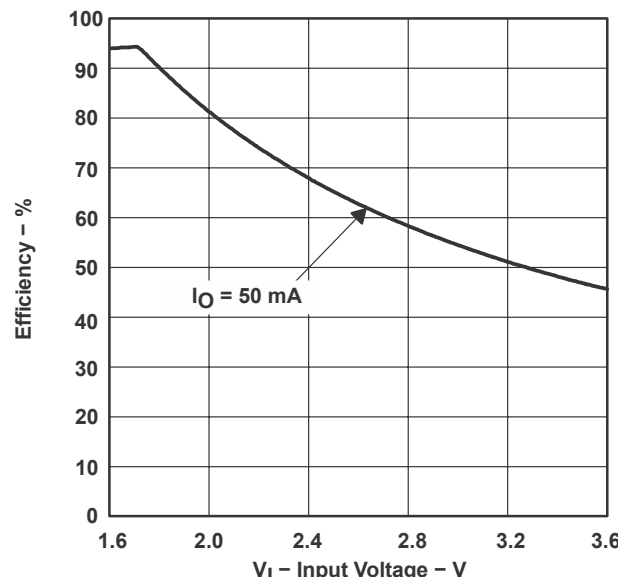


Figure 7-2. Efficiency vs Input Voltage

7.7 Typical Characteristics (continued)

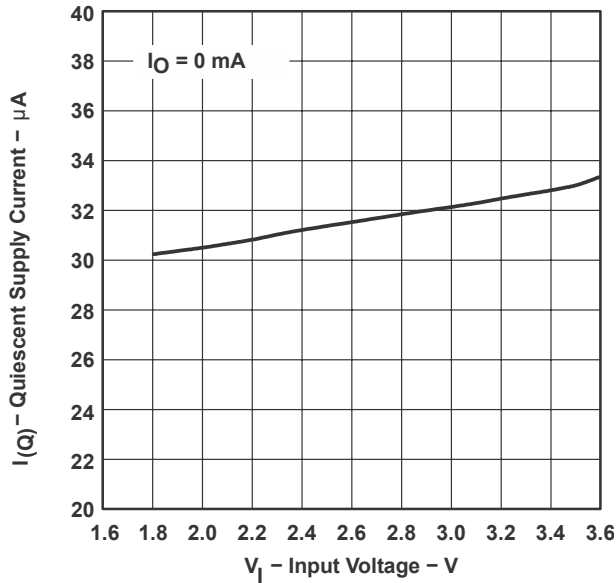


Figure 7-3. Quiescent Supply Current vs Input Voltage

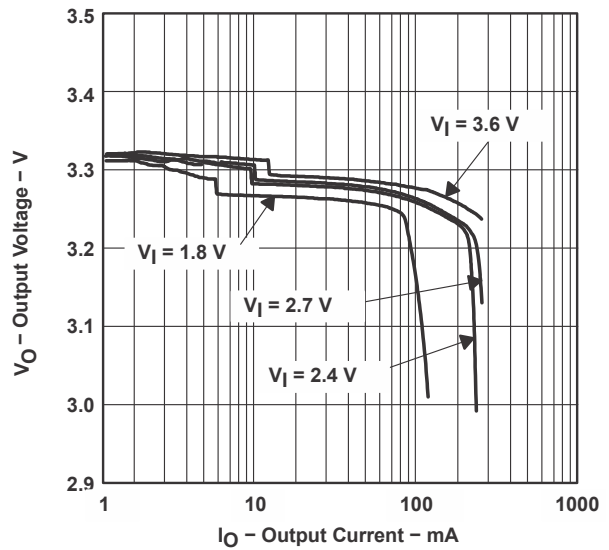


Figure 7-4. Output Voltage vs Output Current

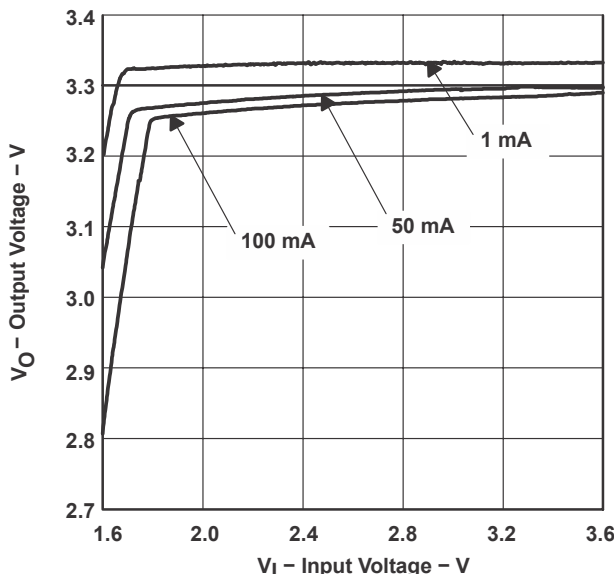


Figure 7-5. Output Voltage vs Input Voltage

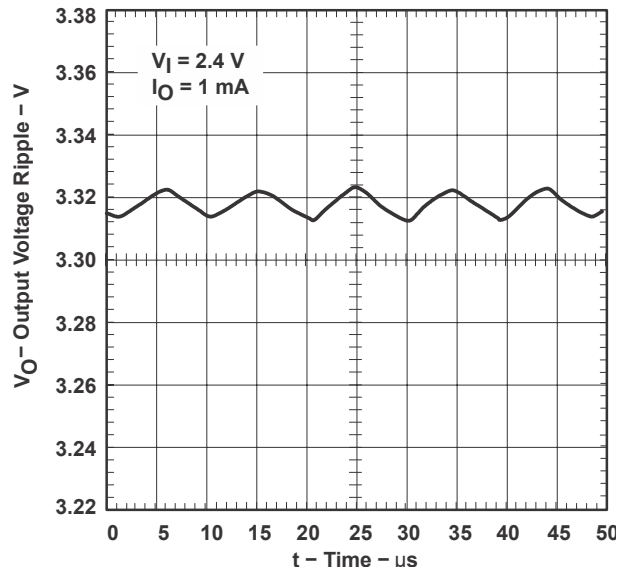


Figure 7-6. Output Voltage Ripple vs Time

7.7 Typical Characteristics (continued)

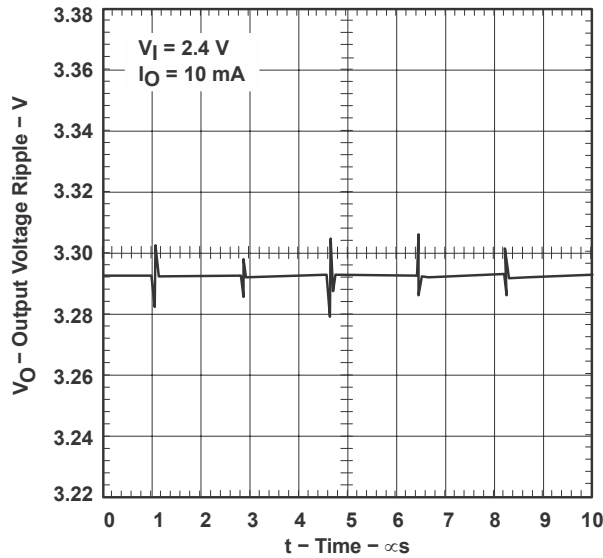


Figure 7-7. Output Voltage Ripple vs Time

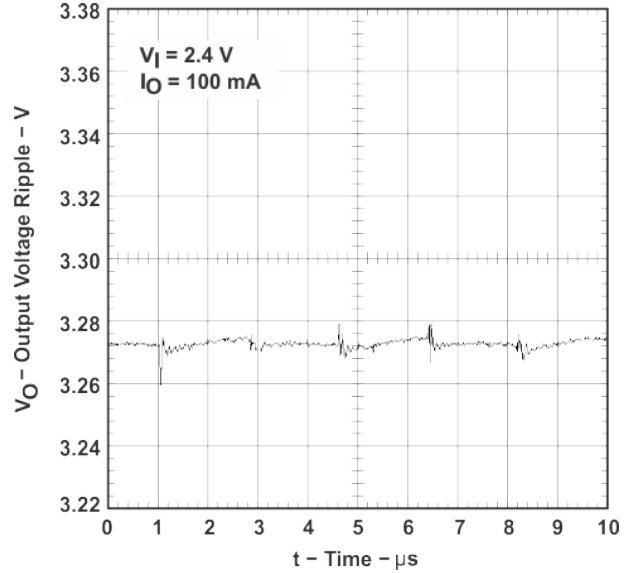


Figure 7-8. Output Voltage Ripple vs Time

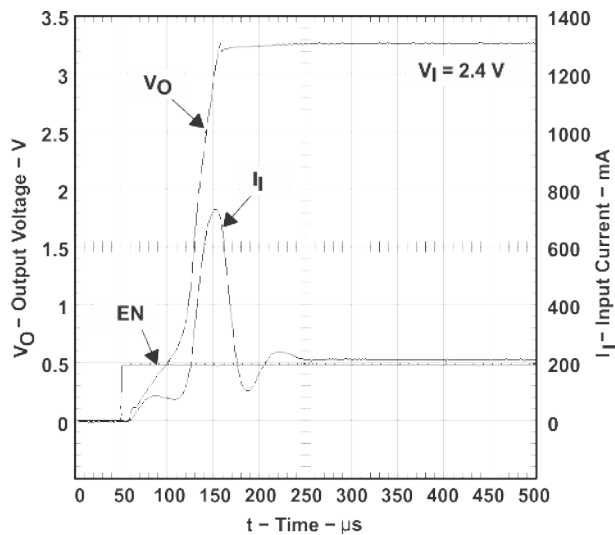


Figure 7-9. Start-Up Timing

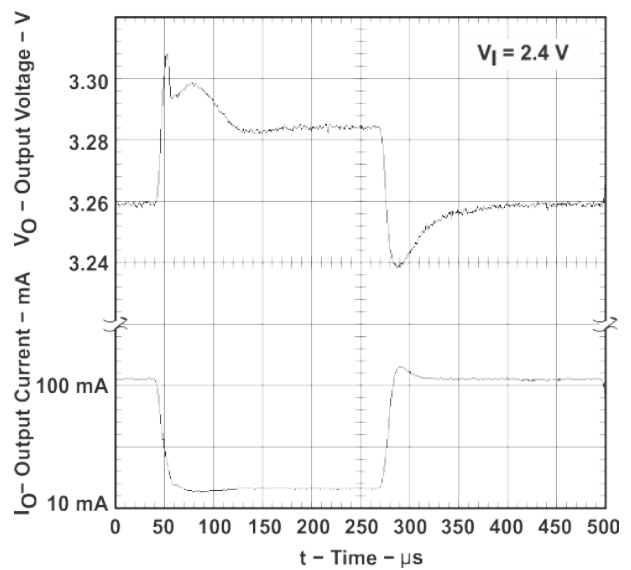


Figure 7-10. Load Transient Response

7.7 Typical Characteristics (continued)

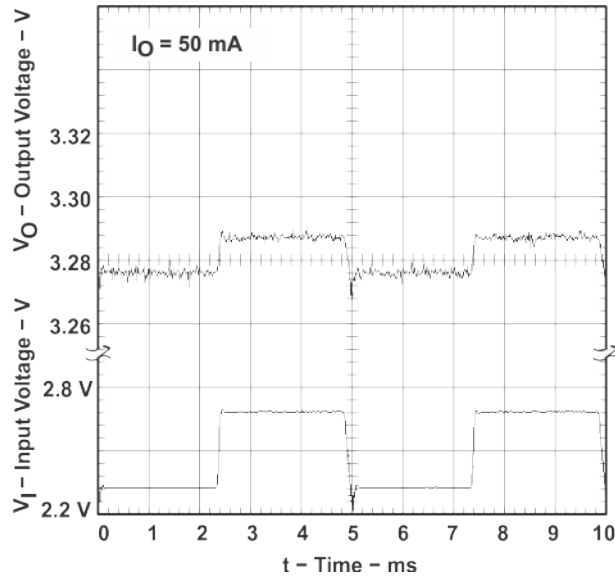


Figure 7-11. Line Transient Response

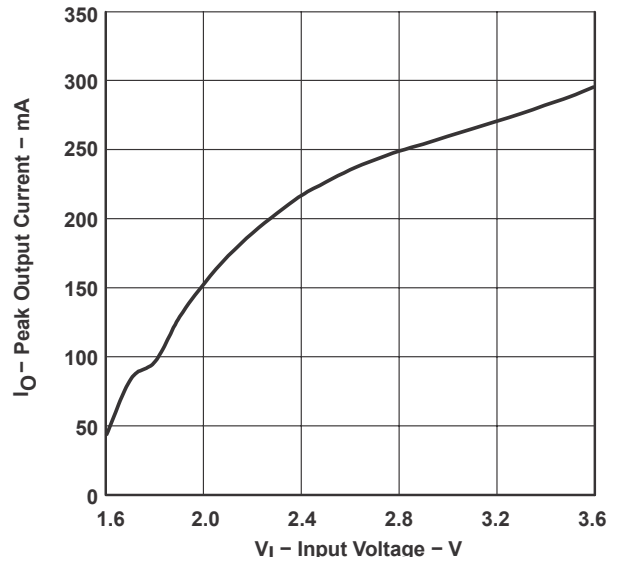


Figure 7-12. Peak Output Current vs Input Voltage

8 Detailed Description

Operating Principle

The TPS6020x charge pumps provide a regulated 3.3-V output from a 1.8-V to 3.6-V input. They deliver up to 100-mA load current while maintaining the output at 3.3 V $\pm 4\%$. Designed specifically for space critical battery powered applications, the complete converter requires only four external capacitors. The device is using the push-pull topology to achieve lowest output voltage ripple. The converter is also optimized for smallest board space. It makes use of small sized capacitors, with the highest output current rating per output capacitance and package size.

The TPS6020x circuits consist of an oscillator, a 1.18-V voltage reference, an internal resistive feedback circuit, an error amplifier, two charge pump power stages with high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (see functional block diagrams).

Push-pull Operating Mode

The two single-ended charge pump power stages operate in the so-called push-pull operating mode, i.e., they operate with a 180° phase shift. Each single-ended charge pump transfers charge into its transfer capacitor (C1 or C2) in one half of the period. During the other half of the period (transfer phase), the transfer capacitor is placed in series with the input to transfer its charge to Co. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation assures an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name voltage doubler). In order to provide a regulated fixed output voltage of 3.3 V, the TPS6020x devices use either pulse-skip or constant-frequency linear-regulation control mode. The mode is automatically selected based on the output current. If the load current is below the LinSkip current threshold, it switches into the power-saving pulse-skip mode to boost efficiency at low output power.

Constant-frequency Mode

When the output current is higher than the LinSkip current threshold, the charge pump runs continuously at the switching frequency $f_{(OSC)}$. The control circuit, fed from the error amplifier, controls the charge on C1 and C2 by controlling the gates and hence the $r_{DS(ON)}$ of the integrated MOSFETs. When the output voltage decreases, the gate drive increases, resulting in a larger voltage across C1 and C2. This regulation scheme minimizes output ripple. Since the device switches continuously, the output signal contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads. For this reason, the device switches seamlessly into the pulse-skip mode when the output current drops below the LinSkip current threshold.

Pulse-skip Mode

The regulator enters the pulse-skip mode when the output current is lower than the LinSkip current threshold of 7 mA. In the pulse-skip mode, the error amplifier disables switching of the power stages when it detects an output voltage higher than 3.3 V. The controller skips switching cycles until the output voltage drops below 3.3 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. A 30-mV output voltage offset is introduced in this mode.

The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except the voltage reference and error amplifier when the output is higher than 3.3 V. Even in pulse-skip mode the $r_{DS(ON)}$ of the MOSFETs is controlled. This way the energy per switching cycle that is transferred by the charge pump from the input to the output is limited to the minimum that is necessary to sustain a regulated output voltage, with the benefit that the output ripple is kept to a minimum. When switching is disabled from the error amplifier, the load is also isolated from the input.

Start Up and Shutdown

During start-up, i.e. when EN is set from logic low to logic high, the output capacitor is directly connected to IN and charged up with a limited current until the output voltage V_O reaches $0.8 \times V_I$. When the start-up comparator detects this limit, the converter begins switching. This precharging of the output capacitor guarantees a short start-up time. In addition, the inrush current into an empty output capacitor is limited. The converter can start into a full load, which is defined by a 33- Ω or 66- Ω resistor, respectively.

Driving EN low disables the converter. This disables all internal circuits and reduces the supply current to only 0.05 μA . The device exits shutdown once EN is set high. When the device is disabled, the load is isolated from the input. This is an important feature in battery operated products because it extends the products shelf life.

Synchronization to an External Clock Signal

The operating frequency of the charge pump is limited to 400 kHz in order to avoid interference in the sensitive 455-kHz IF band. The device can either run from the integrated oscillator, or an external clock signal can be used to drive the charge pump. The maximum frequency of the external clock signal is 800 kHz. The switching frequency used internally to drive the charge pump power stages is half of the external clock frequency. The external clock signal is applied to the EN pin. The device will switch off if the signal on EN is hold low for more than 10 μs .

When the load current drops below the LinSkip current threshold, the devices will enter the pulse-skip mode but stay synchronized to the external clock signal.

Low-battery Detector (TPS60204)

The low-battery comparator trips at $1.18 \text{ V} \pm 4\%$ when the voltage on pin LBI ramps down. The voltage $V_{(\text{TRIP})}$ at which the low-battery warning is issued can be adjusted with a resistive divider as shown in Figure 2. The sum of resistors R1 and R2 is recommended to be in the 100-k Ω to 1-M Ω range. When choosing R1 and R2, be aware of the input leakage current into the LBI pin.

LBO is an open drain output. An external pullup resistor to OUT, or any other voltage rail in the appropriate range, in the 100-k Ω to 1-M Ω range is recommended. During start-up, the LBO output signal is invalid for the first 500 μs . LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground and leave LBO unconnected. The low-battery detector is disabled when the device is switched off.

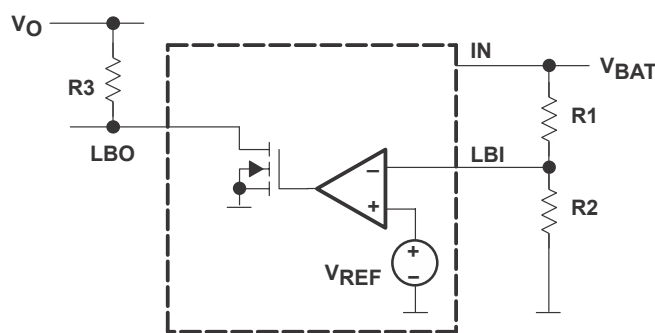


Figure 8-1. Programming of the Low-Battery Comparator Trip Voltage

A 100-nF ceramic capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO pin.

Formulas to calculate the resistive divider for low-battery detection, with $V_{\text{LBI}} = 1.13 \text{ V}$ to 1.23 V and the sum of resistors R1 and R2 equal 1 M Ω :

$$R2 = 1\text{ M}\Omega \times \frac{V_{LBI}}{V_{Bat}} \quad (1)$$

$$R1 = 1\text{ M}\Omega - R2 \quad (2)$$

Formulas to calculate the minimum and maximum battery voltage:

$$V_{Bat(min)} = V_{LBI(min)} \times \frac{R1(min) + R2(max)}{R2(min)} \quad (3)$$

$$V_{Bat(max)} = V_{LBI(max)} \times \frac{R1(max) + R2(min)}{R2(min)} \quad (4)$$

Table 8-1. Recommended Values for the Resistive Divider From the E96 Series ($\pm 1\%$)

V_{IN} / V	$R1 / k\Omega$	$R2 / k\Omega$	$V_{TRIP(MIN)}/V$	$V_{TRIP(MAX)}/V$
1.6	267	750	1.524	1.677
1.7	301	681	1.620	1.785
1.8	340	649	1.710	1.887
1.9	374	619	1.799	1.988
2.0	402	576	1.903	2.106

Power-good Detector (TPS60205)

The power-good output is an open-drain output that pulls low when the output is out of regulation. When the output rises to within 90% of its nominal voltage, the power-good output is released. Power-good is high impedance in shutdown. In normal operation, an external pullup resistor must be connected between PG and OUT, or any other voltage rail in the appropriate range. The resistor should be in the 100-k Ω to 1-M Ω range. If the PG output is not used, it should remain unconnected.

8.1 Functional Block Diagrams

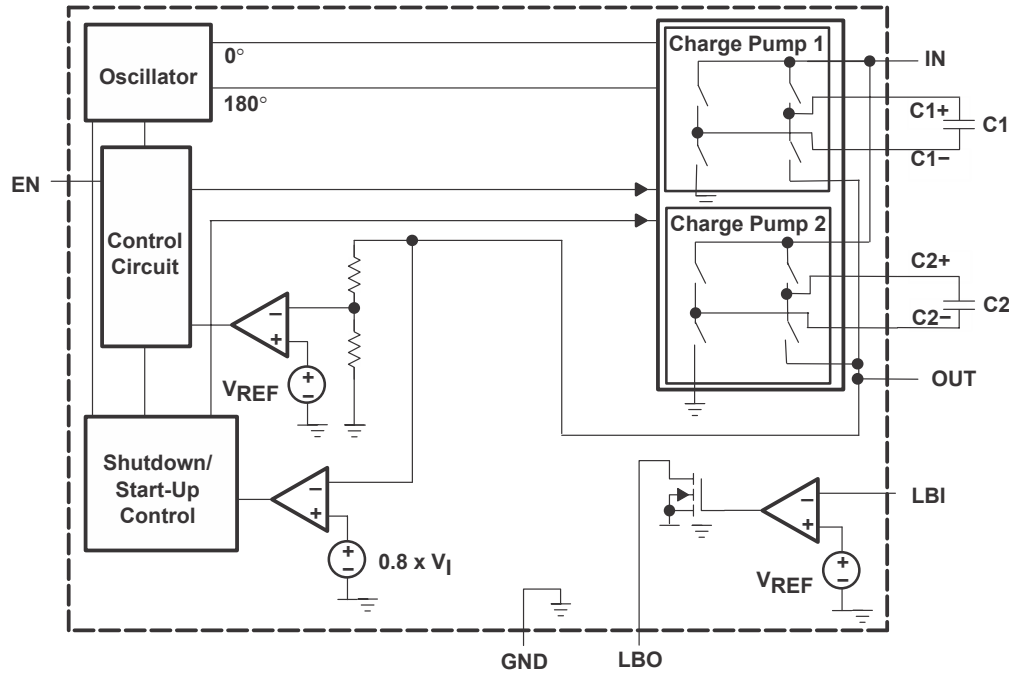


Figure 8-2. TPS60204 With Low-Battery Detector

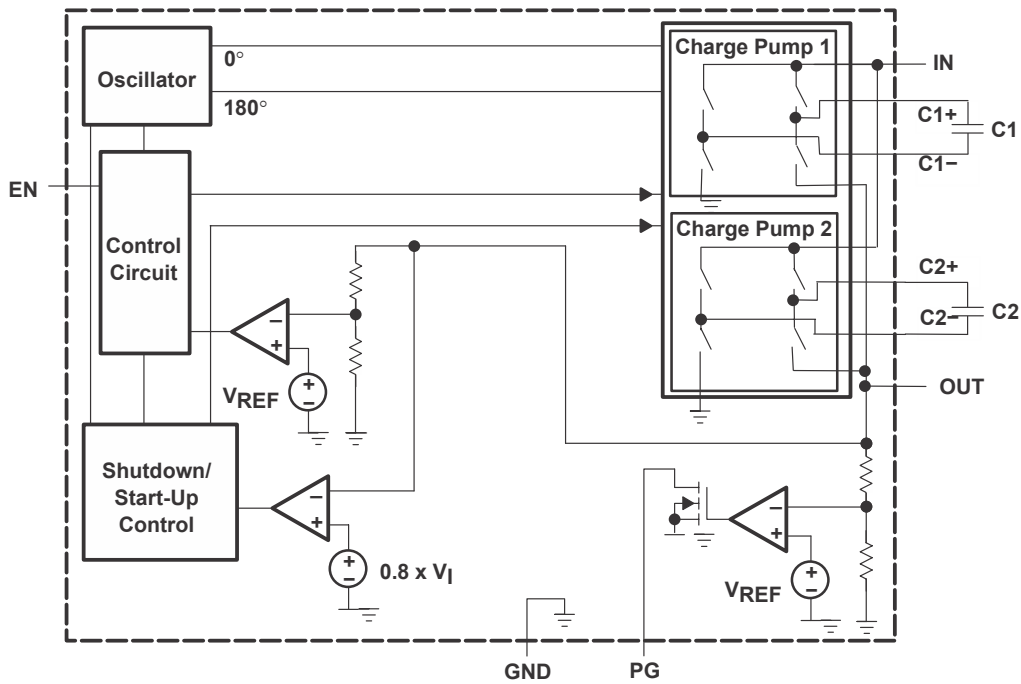


Figure 8-3. TPS60205 With Power-Good Detector

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Capacitor Selection

The TPS6020x devices require only four external capacitors to achieve a very low output voltage ripple. The capacitor values are closely linked to the required output current. Low ESR ($<0.1 \Omega$) capacitors should be used at input and output. In general, the transfer capacitors (C1 and C2) will be the smallest; a 1- μF value is recommended for maximum load operation. With smaller capacitor values, the maximum possible load current is reduced and the LinSkip threshold is lowered.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used and the distance from the power source to the converter IC. C_i is recommended to be about two to four times as large as the flying capacitors C1 and C2.

The output capacitor (C_o) should be at minimum the size of the input capacitor. The minimum required capacitance is 2.2 μF . Larger values will improve the load transient performance and will reduce the maximum output ripple voltage.

Only ceramic capacitors are recommended for input, output, and flying capacitors. Depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature and voltage. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U- or Y5V-type capacitors will decrease in capacitance. Table 2 lists the recommended capacitor values.

Table 9-1. Recommended Capacitor Values (Ceramic X5R and X7R)

LOAD CURRENT, I_L /mA	FLYING CAPACITORS, C1/C2 / μF	INPUT CAPACITOR, C_i / μF	OUTPUT CAPACITOR, C_o / μF	OUTPUT VOLTAGE RIPPLE IN LINEAR MODE, $V_{(P-P)}$ /mV	OUTPUT VOLTAGE RIPPLE IN SKIP MODE, $V_{(P-P)}$ /mV
0-100	1	2.2	2.2	3	20
0-100	1	4.7	4.7	3	10
0-100	1	2.2	10	3	7
0-100	2.2	4.7	4.7	3	10
0-50	0.47	2.2	2.2	3	20
0-25	0.22	2.2	2.2	5	15
0-10	0.1	2.2	2.2	5	15

Table 9-2. Recommended Capacitor Types

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	UMK212BJ104MG	0805	0.1 μ F	Ceramic
	EMK212BJ224MG	0805	0.22 μ F	Ceramic
	EMK212BJ474MG	0805	0.47 μ F	Ceramic
	LMK212BJ105KG	0805	1 μ F	Ceramic
	LMK212BJ225MG	0805	2.2 μ F	Ceramic
	EMK316BJ225KL	1206	2.2 μ F	Ceramic
	LMK316BJ475KL	1206	4.7 μ F	Ceramic
	JMK316BJ106ML	1206	10 μ F	Ceramic
AVX	0805ZC105KAT2A	0805	1 μ F	Ceramic
	1206ZC225KAT2A	1206	2.2 μ F	Ceramic

Table 9-3. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET SITE
Taiyo Yuden	X7R/X5R ceramic	Website
AVX	X7R/X5R ceramic	Website

Device Family Products

Other charge pump dc-dc converters in this family are:

Table 9-4. Product Identification

PART NUMBER	DESCRIPTION
TPS60100	2-cell to regulated 3.3 V, 200-mA low-noise charge pump
TPS60101	2-cell to regulated 3.3 V, 100-mA low-noise charge pump
TPS60110	3-cell to regulated 5.0 V, 300-mA low-noise charge pump
TPS60111	3-cell to regulated 5.0 V, 150-mA low-noise charge pump
TPS60120	2-cell to regulated 3.3 V, 200-mA high efficiency charge pump with low battery comparator
TPS60121	2-cell to regulated 3.3 V, 200-mA high efficiency charge pump with power-good comparator
TPS60122	2-cell to regulated 3.3 V, 100-mA high efficiency charge pump with low battery comparator
TPS60123	2-cell to regulated 3.3 V, 100-mA high efficiency charge pump with power-good comparator
TPS60130	3-cell to regulated 5.0 V, 300-mA high efficiency charge pump with low battery comparator
TPS60131	3-cell to regulated 5.0 V, 300-mA high efficiency charge pump with low battery comparator
TPS60132	3-cell to regulated 5.0 V, 150-mA high efficiency charge pump with low battery comparator
TPS60133	3-cell to regulated 5.0 V, 150-mA high efficiency charge pump with power-good comparator
TPS60140	2-cell to regulated 5.0 V, 100-mA charge pump voltage tripler with low battery comparator
TPS60141	2-cell to regulated 5.0 V, 100-mA charge pump voltage tripler with power-good comparator

9.2 Typical Application

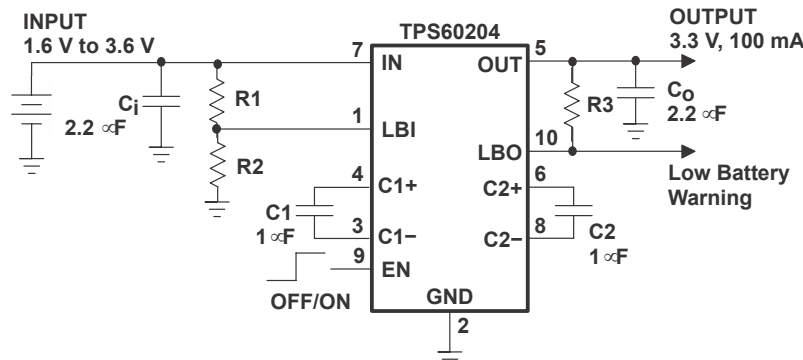


Figure 9-1. Typical Operating Circuit TPS60204 With Low-Battery Detector

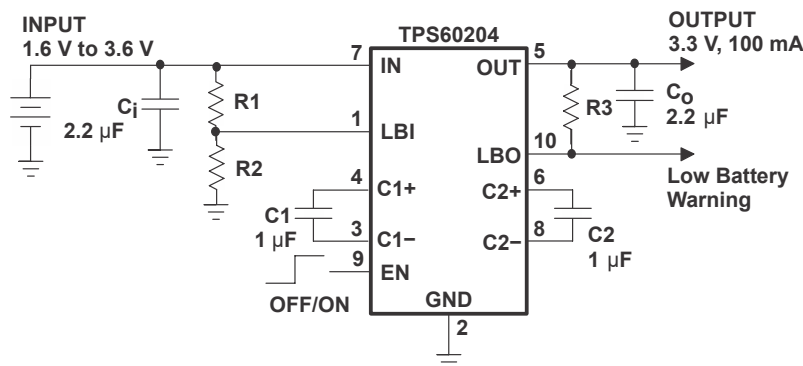


Figure 9-2. Typical Operating Circuit TPS60205 With Power-Good Detector

9.3 Power Dissipation

The power dissipated in the TPS6020x devices depends mainly on input voltage and output current and is approximated by:

$$P_{(DISS)} = I_O \times (2 \times V_I - V_O) \quad (5)$$

for

$$I_{(Q)} < I_O \quad (6)$$

By observing equation 5, it can be seen that the power dissipation is worst for highest input voltage V_I and highest output current I_O . For an input voltage of 3.6 V and an output current of 100 mA the calculated power dissipation $P_{(DISS)}$ is 390 mW. This is also the point where the charge pump operates with its lowest efficiency.

With the recommended maximum junction temperature of 125°C and an assumed maximum ambient operating temperature of 85°C, the maximum allowed thermal resistance junction to ambient of the system can be calculated.

$$R_{\theta JA(max)} = \frac{T_{J(MAX)} - T_A}{P_{DISS(max)}} = \frac{125^\circ\text{C} - 85^\circ\text{C}}{390 \text{ mW}} = 102^\circ\text{C/W} \quad (7)$$

P_{DISS} must be less than that allowed by the package rating. The thermal resistance junction to ambient of the used 10-pin MSOP is 294°C/W for an unsoldered package. The thermal resistance junction to ambient with the IC soldered to a printed circuit using a board layout as described in the application information section, the $R_{\theta JA}$ is typically 200°C/W, which is higher than the maximum value calculated above. However, in a battery powered

application, both V_I and T_A will typically be lower than the worst case ratings used in equation 6 , and power dissipation should not be a problem in most applications.

9.4 Layout and Board Space

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be placed in close proximity to the device. A PCB layout proposal for a one-layer board is given in Figure 17. There is no specific EVM available for the TPS60204. However, the TPS60200EVM-145 can be used to evaluate the device.

The evaluation module for the TPS60200 can be ordered under product code TPS60200EVM-145. The EVM uses the layout shown in Figure 17. All components including the pins are shown. The EVM is built so that it can be connected to a 14-pin dual inline socket, therefore, the space needed for the IC, the external parts, and eight pins is 17,9 mm x 10,2 mm = 182,6 mm².

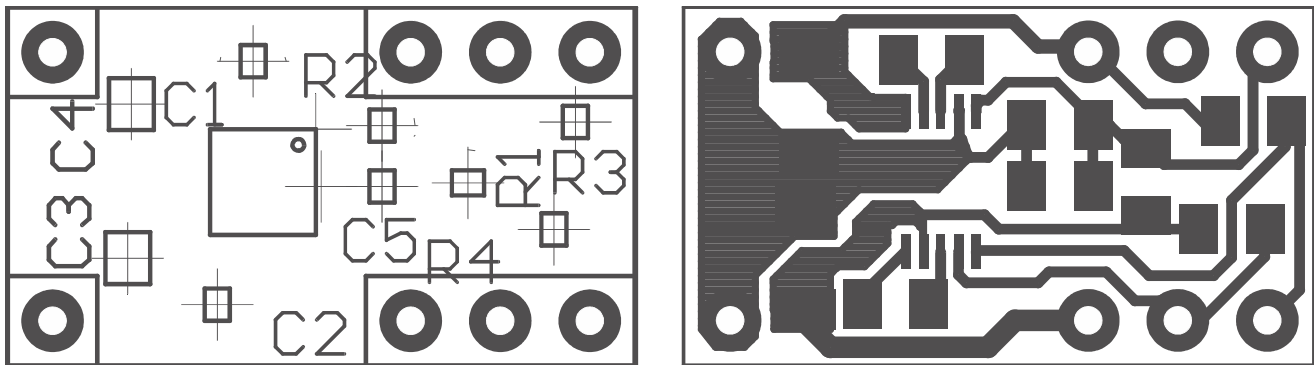


Figure 9-3. Recommended Component Placement and Board Layout

Table 9-5. Component Identification

IC1	TPS60204	
	C1, C2	Flying capacitors
	C3	Input capacitors
	C4	Output capacitors
	C5	Stabilization capacitor for LBI
	R1, R2	Resistive divider for LBI
	R3	Pullup resistor for LBO
	R4	Pullup resistor for EN

Capacitor C5 should be included if large line transients are expected. This capacitor suppresses toggling of the LBO due to these line changes.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Support

10.2 Documentation Support

10.2.1 Related Documentation

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Package Option Addendum

Packaging Information

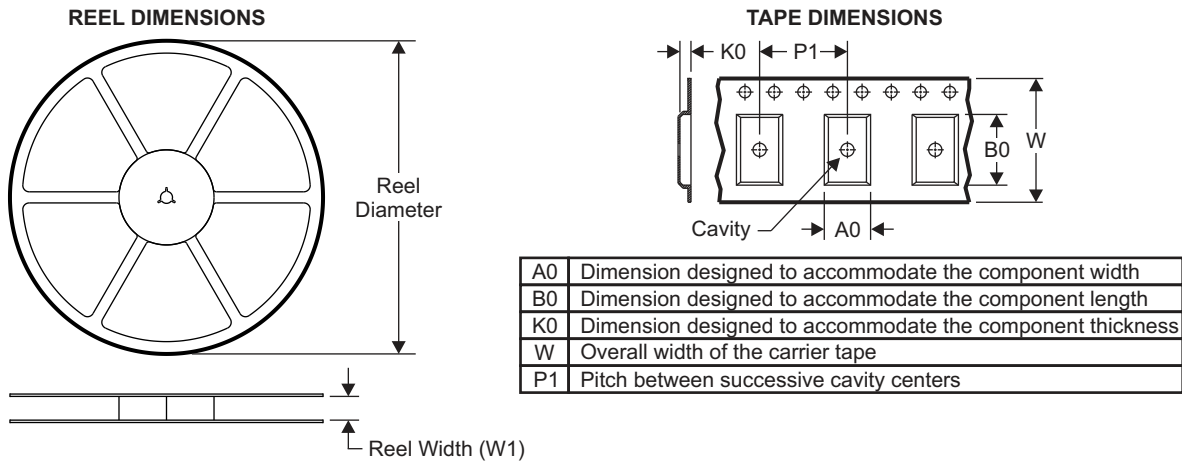
Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(4) (5)}
TPS60204DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFB
TPS60204DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFB
TPS60205DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFC
TPS60205DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFC

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

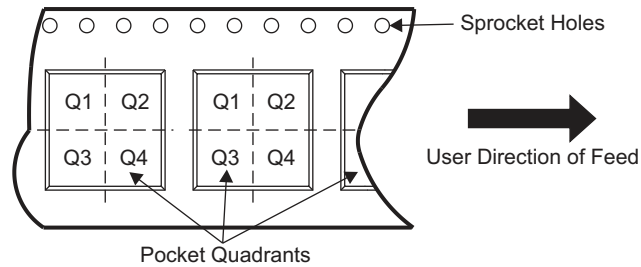
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11.2 Tape and Reel Information

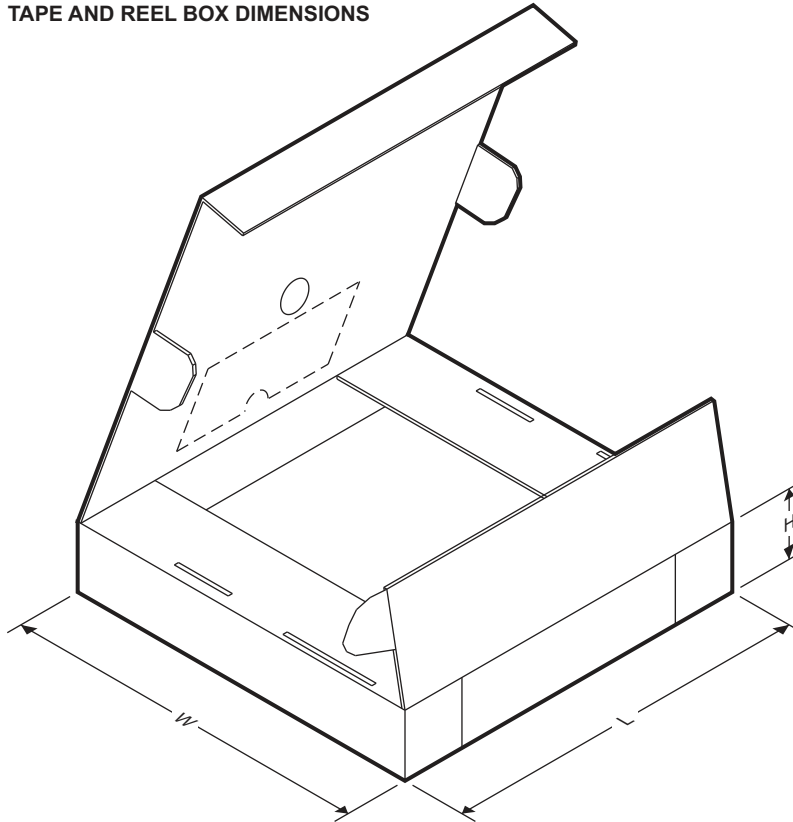


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60204DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60205DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60204DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60205DGSR	VSSOP	DGS	10	2500	350.0	350.0	

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60204DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFB	Samples
TPS60204DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFB	Samples
TPS60205DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFC	Samples
TPS60205DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFC	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60204DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60205DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60204DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60205DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS60204DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60205DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88

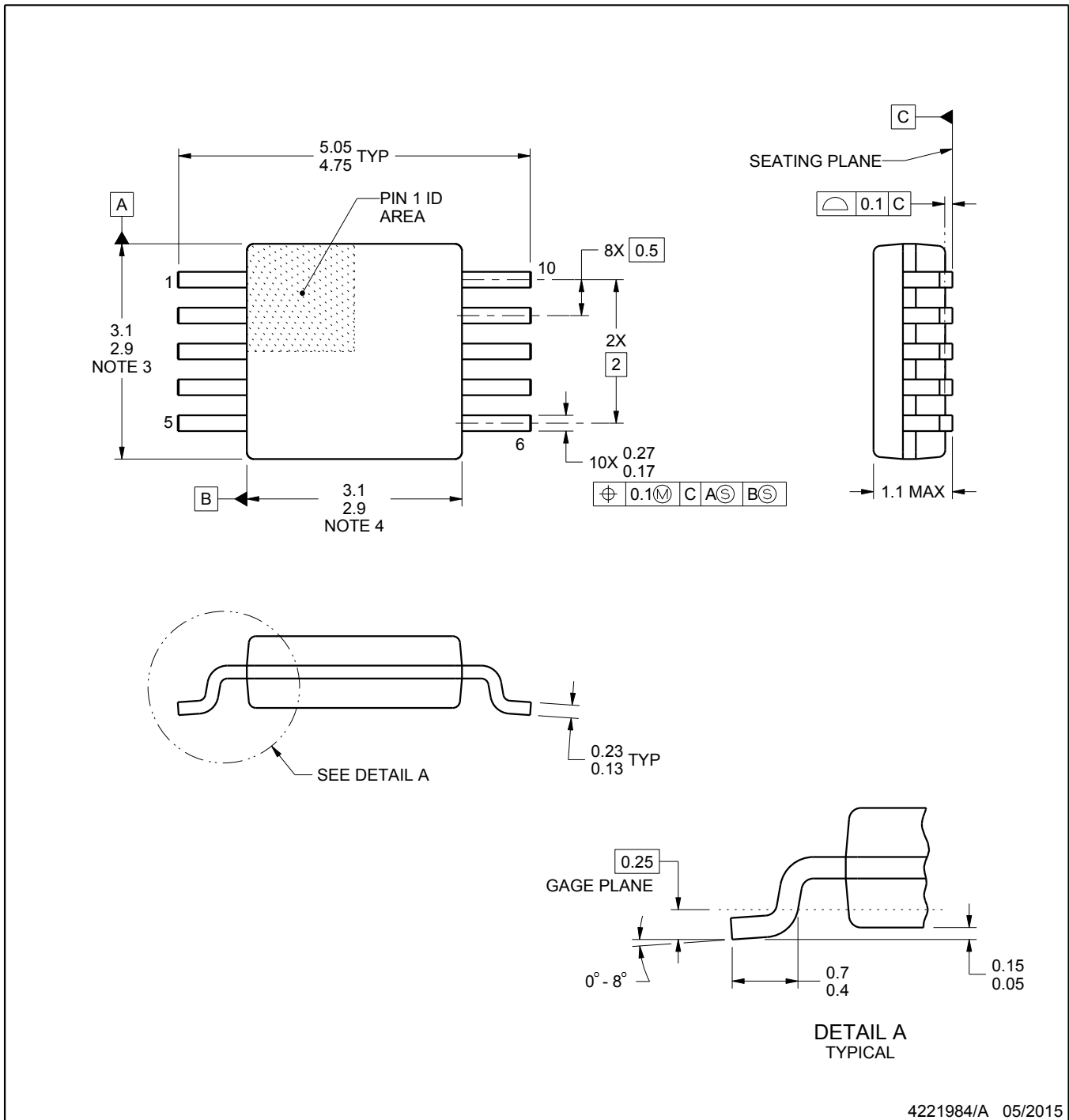
DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

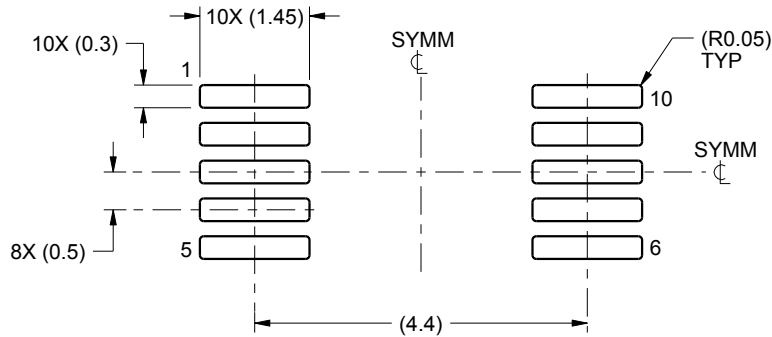
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

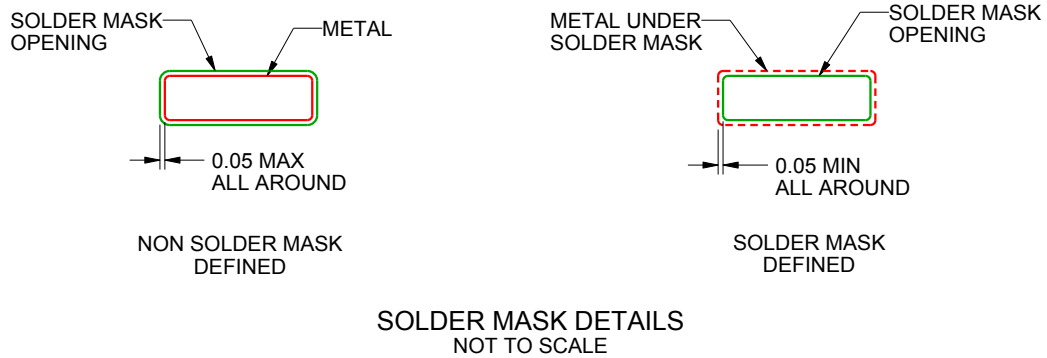
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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