

N-channel 650 V, 0.093 Ω typ., 32 A MDmesh™ DM2 Power MOSFET in a TO-220 package

Datasheet - production data

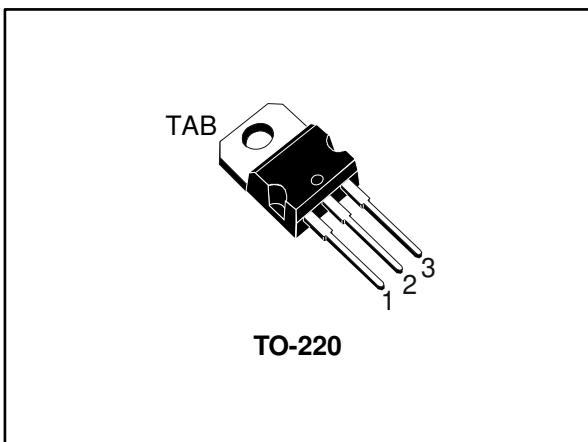
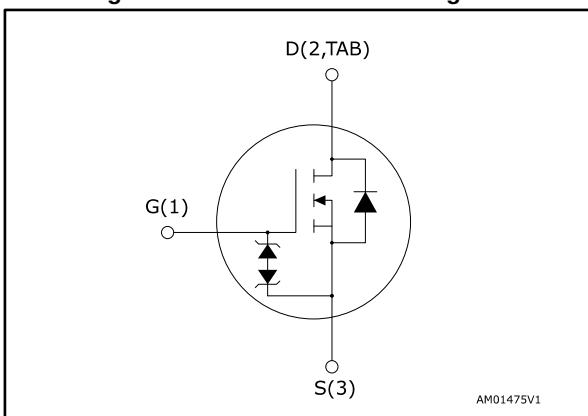


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STP35N65DM2	650 V	0.110 Ω	32 A	250 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STP35N65DM2	35N65DM2	TO-220	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_{case} = 25^\circ C$	32	A
	Drain current (continuous) at $T_{case} = 100^\circ C$	20	
$I_{DM}^{(1)}$	Drain current (pulsed)	90	A
P_{TOT}	Total dissipation at $T_{case} = 25^\circ C$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	$^\circ C$
T_j	Operating junction temperature range		

Notes:

(1) Pulse width is limited by safe operating area.

(2) $I_{SD} \leq 32 A$, $di/dt=900 A/\mu s$, V_{DS} peak < $V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$ (3) $V_{DS} \leq 520 V$ **Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^\circ C/W$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive	4	A
$E_{AS}^{(1)}$	Single pulse avalanche energy	1150	mJ

Notes:(1) Starting $T_j = 25^\circ C$, $I_D = I_{AR}$, $V_{DD} = 50 V$.

2 Electrical characteristics

($T_{case} = 25^\circ C$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 V$, $I_D = 1 mA$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0 V$, $V_{DS} = 650 V$			1	μA
		$V_{GS} = 0 V$, $V_{DS} = 650 V$, $T_{case} = 125^\circ C$ ⁽¹⁾			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0 V$, $V_{GS} = \pm 25 V$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 V$, $I_D = 16 A$		0.093	0.110	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100 V$, $f = 1 MHz$, $V_{GS} = 0 V$	-	2540	-	pF
C_{oss}	Output capacitance		-	115	-	
C_{rss}	Reverse transfer capacitance		-	2.5	-	
$C_{oss\ eq.}$ ⁽¹⁾	Equivalent output capacitance	$V_{DS} = 0$ to $520 V$, $V_{GS} = 0 V$	-	204	-	pF
R_G	Intrinsic gate resistance	$f = 1 MHz$, $I_D = 0 A$	-	4.2	-	Ω
Q_g	Total gate charge	$V_{DD} = 520 V$, $I_D = 32 A$, $V_{GS} = 0$ to $10 V$ (see Figure 15: "Test circuit for gate charge behavior")	-	56.3	-	nC
Q_{gs}	Gate-source charge		-	12.7	-	
Q_{gd}	Gate-drain charge		-	27.6	-	

Notes:

⁽¹⁾ $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325 V$, $I_D = 16 A$, $R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	23.4	-	ns
t_r	Rise time		-	23	-	
$t_{d(off)}$	Turn-off delay time		-	72	-	
t_f	Fall time		-	10.4	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		32	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		90	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 32 \text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 32 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i>)	-	100		ns
Q_{rr}	Reverse recovery charge		-	0.42		μC
I_{RRM}	Reverse recovery current		-	8.4		A
t_{rr}	Reverse recovery time	$I_{SD} = 32 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i>)	-	205		ns
Q_{rr}	Reverse recovery charge		-	1.8		μC
I_{RRM}	Reverse recovery current		-	17.6		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

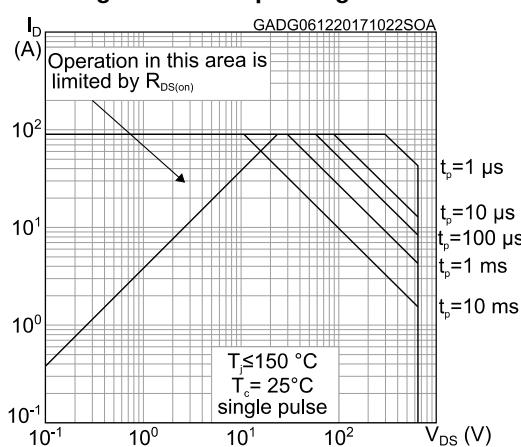


Figure 3: Thermal impedance

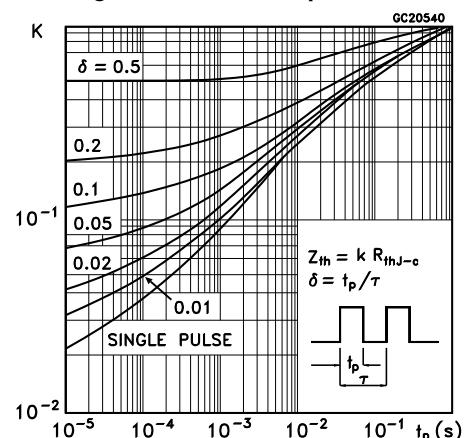


Figure 4: Output characteristics

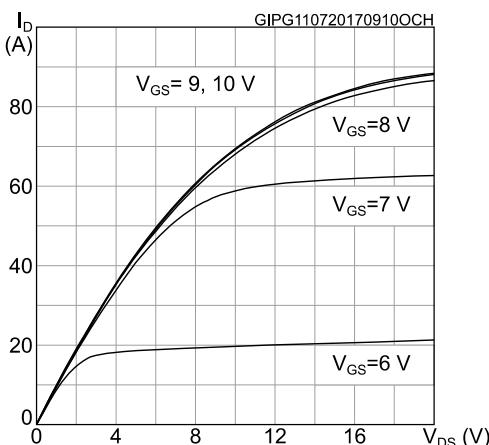


Figure 5: Transfer characteristics

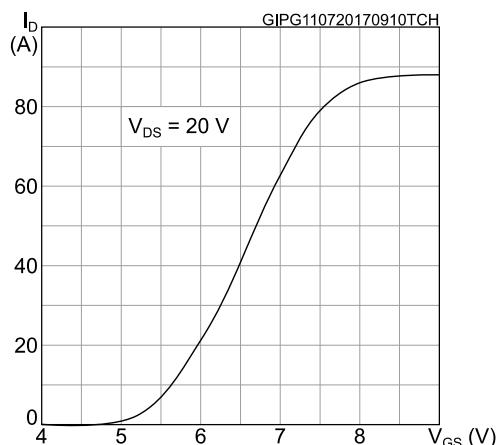


Figure 6: Gate charge vs gate-source voltage

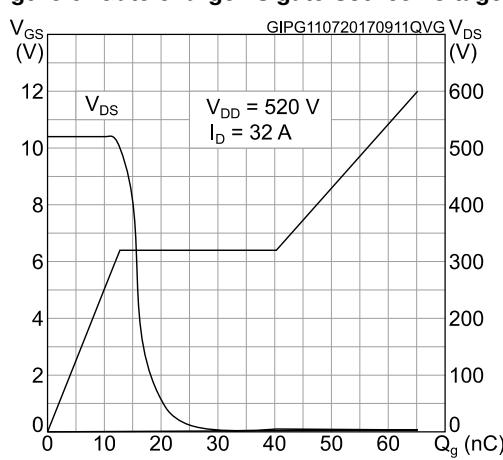


Figure 7: Static drain-source on-resistance

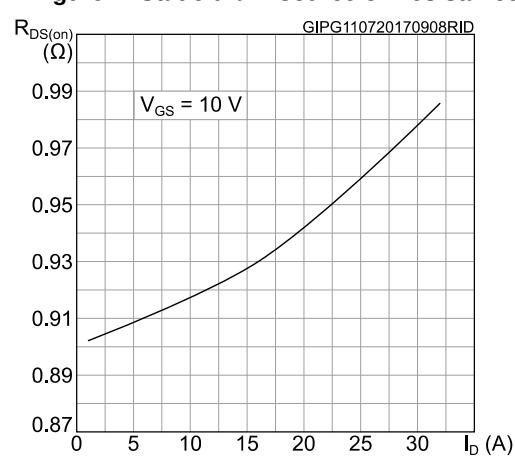
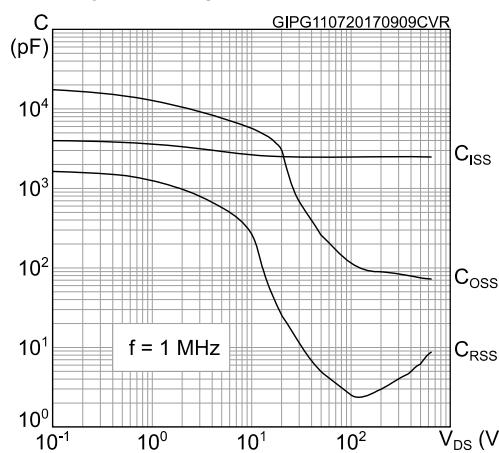
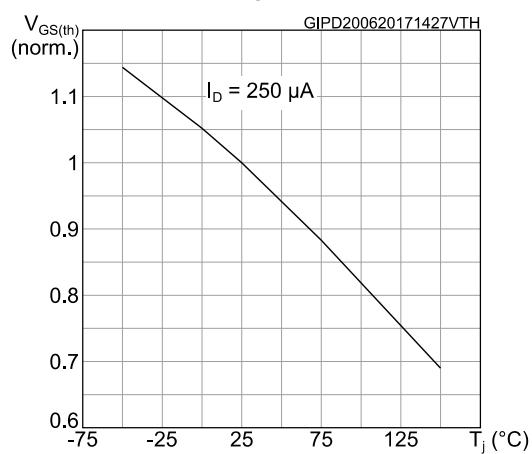
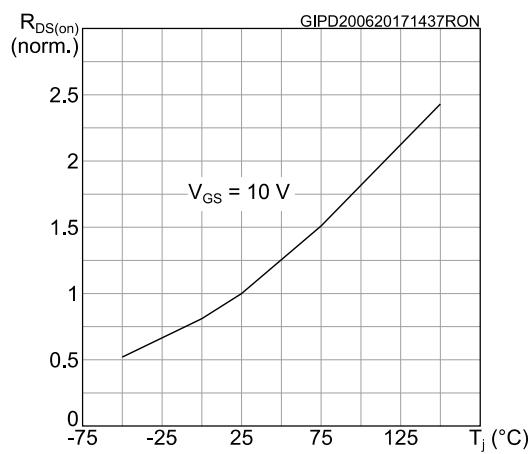
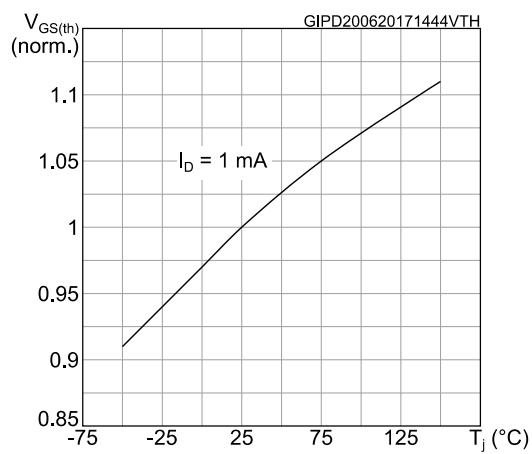
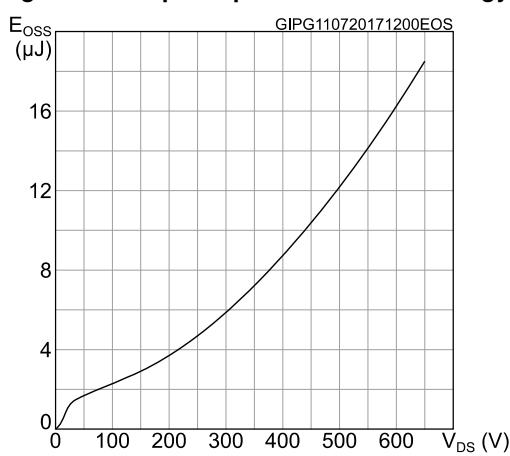
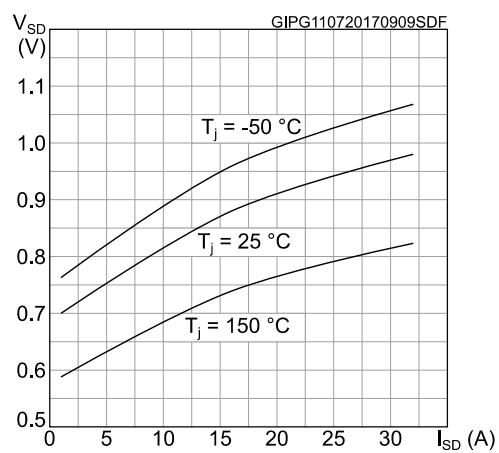


Figure 8: Capacitance variations**Figure 9: Normalized gate threshold voltage vs temperature****Figure 10: Normalized on-resistance vs temperature****Figure 11: Normalized $V_{(BR)DSS}$ vs temperature****Figure 12: Output capacitance stored energy****Figure 13: Source- drain diode forward characteristics**

3 Test circuits

Figure 14: Test circuit for resistive load switching times

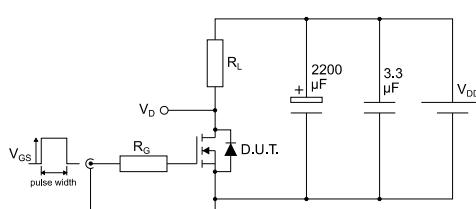


Figure 15: Test circuit for gate charge behavior

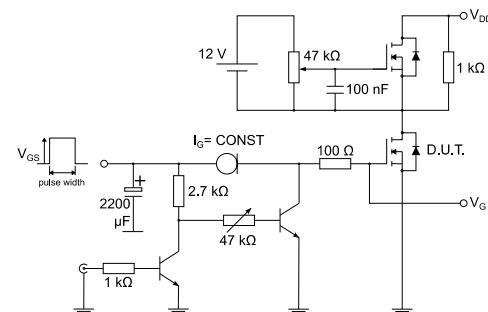


Figure 16: Test circuit for inductive load switching and diode recovery times

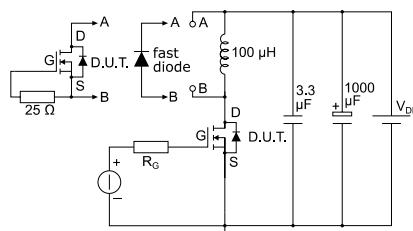


Figure 17: Unclamped inductive load test circuit

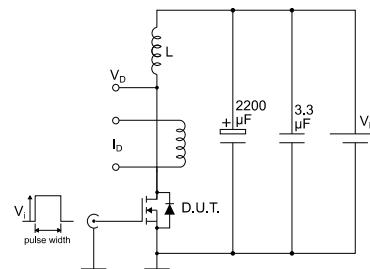


Figure 18: Unclamped inductive waveform

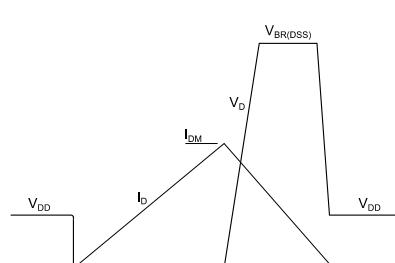
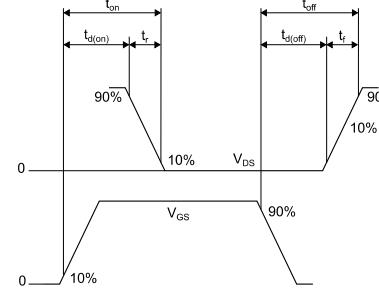


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
ECOPACK® is an ST trademark.

4.1 TO-220 type A package information

Figure 20: TO-220 type A package outline

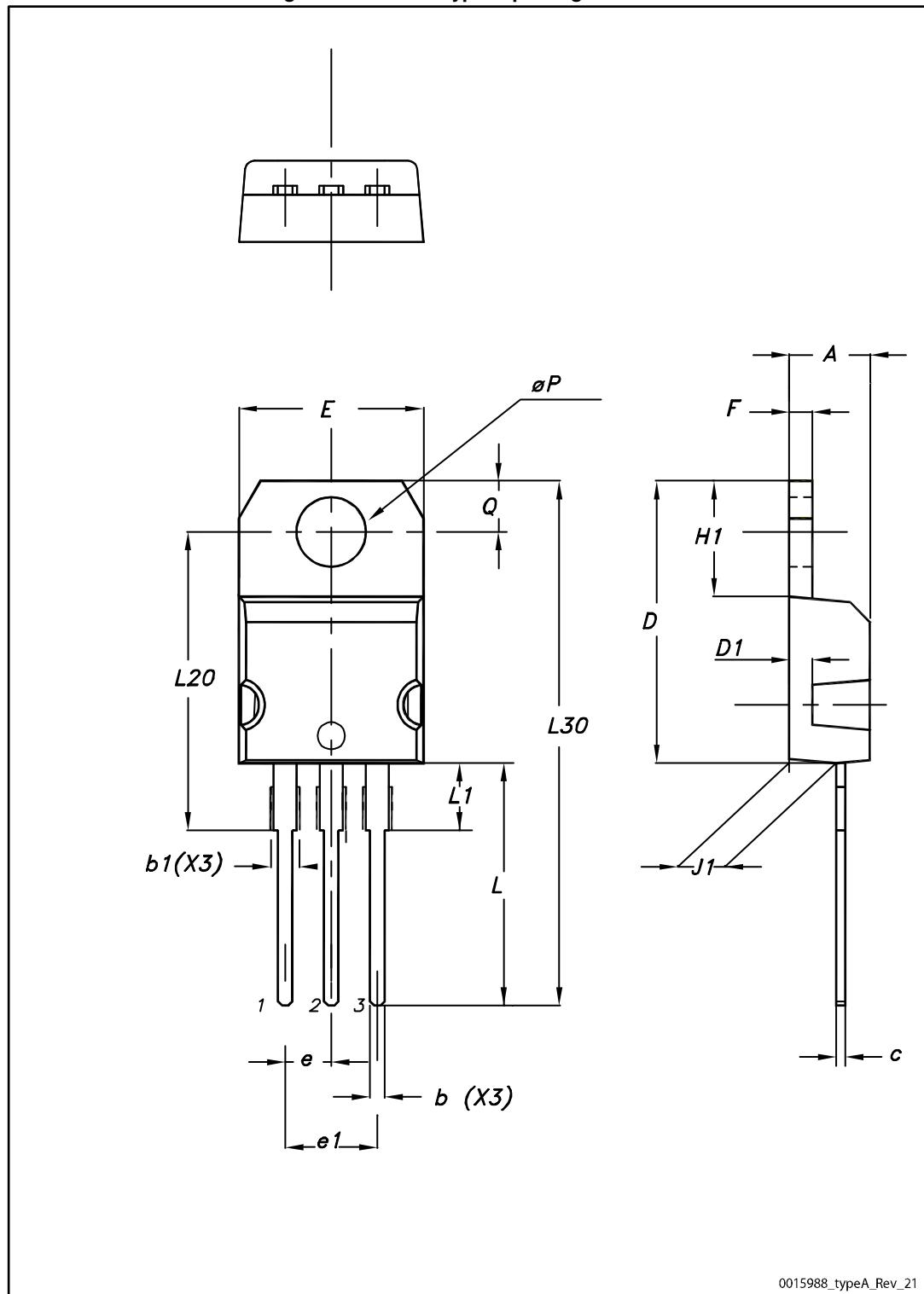


Table 9: TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 10: Document revision history

Date	Revisi on	Changes
21-Jul-2017	1	Initial release
6-Dec-2017	2	Document status changed from preliminary to production data. Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Table 8: "Source-drain diode"</i> . Updated <i>Figure 2: "Safe operating area"</i> . Minor text changes.

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