SIPMOS® Small-Signal-Transistor **BSP320S**

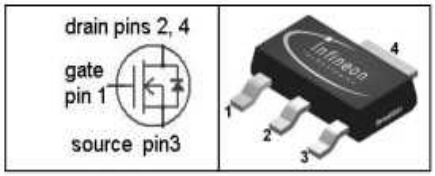
Features

- N channel
- Enhancement mode
- Avalanche rated
- Pb-free lead plating; RoHS compliant
- Qualified according to AEC Q101
- Halogen-free according to IEC61249-2-21

Product Summary

Drain source voltage	V_{DS}	60	V
Drain-Source on-state resistance	$R_{DS(on)}$	0.12	Ω
Continuous drain current	I_D	2.9	A

PG-SOT223



Type	Package	Tape and Reel	Packaging
BSP320S	PG-SOT223	H6327: 1000pcs/r	Non dry
BSP320S	PG-SOT223	H6433: 4000pcs/r	Non dry

Maximum Ratings , at Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current	I_D	2.9	A
Pulsed drain current T_A = 25 °C	I_{Dpulse}	11.6	
Avalanche energy, single pulse I_D = 2.9 A, V_{DD} = 25 V, R_{GS} = 25 Ω	E_{AS}	60	mJ
Avalanche current,periodic limited by T_{jmax}	I_{AR}	2.9	A
Avalanche energy, periodic limited by T_{jmax}	E_{AR}	0.18	mJ
Reverse diode dv/dt I_S = 2.9 A, V_{DS} = 20 V, di/dt = 200 A/µs, T_{jmax} = 150 °C	dv/dt	6	kV/µs
Gate source voltage	V_{GS}	±20	V
Power dissipation T_A = 25 °C	P_{tot}	1.8	W
Operating temperature	T_j	-55 ... +150	°C
Storage temperature	T_{stg}	-55 ... +150	
IEC climatic category; DIN IEC 68-1		55/150/56	

Electrical Characteristics

Parameter at T_j = 25 °C, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	
Thermal Characteristics					
Thermal resistance, junction - soldering point (Pin 4)	R_{thJS}	-	17	-	K/W
SMD version, device on PCB:	R_{thJA}				K/W
@ min. footprint		-	110	-	
@ 6 cm^2 cooling area[1)]		-	-	70	

Static Characteristics

Drain- source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	60	-	-	V
Gate threshold voltage, V_{GS} = V_{DS} I_D = 20 µA	$V_{GS(th)}$	2.1	3	4	
Zero gate voltage drain current	I_{DSS}				µA
V_{DS} = 60 V, V_{GS} = 0 V, T_j = 25 °C		-	0.1	1	
V_{DS} = 60 V, V_{GS} = 0 V, T_j = 150 °C		-	-	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	-	10	100	nA
Drain-Source on-state resistance V_{GS} = 10 V, I_D = 2.9 A	$R_{DS(on)}$	-	0.09	0.12	Ω

1 Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics

Parameter at T_j = 25 °C, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic Characteristics					
Transconductance $V_{DS}\geq 2*I_D*R_{DS(on)max}$, I_D = 2.9 A	g_{fs}	2.5	5.8	-	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	275	340	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	90	120	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	50	65	
Turn-on delay time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_G = 33 Ω	$t_{d(on)}$	-	11	17	ns
Rise time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_G = 33 Ω	t_r	-	25	40	
Turn-off delay time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_G = 33 Ω	$t_{d(off)}$	-	25	40	
Fall time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_G = 33 Ω	t_f	-	35	55	

Electrical Characteristics

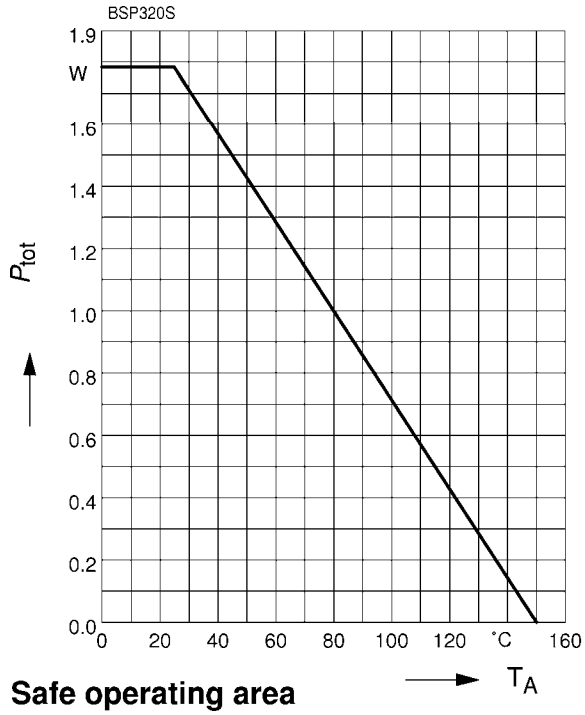
Parameter at T_j = 25 °C, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic Characteristics					
Gate charge at threshold V_{DD} = 40 V, I_D = 0.1 A, V_{GS} = 1 V	$Q_{G(th)}$	-	0.25	0.3	nC
Gate charge at V_{gs}=7V V_{DD} = 40 V, I_D = 2.9 A, V_{GS} = 0 to 7 V	$Q_{g(7)}$	-	7.4	9.3	nC
Gate charge total V_{DD} = 40 V, I_D = 2.9 A, V_{GS} = 0 to 10 V	Q_g	-	9.7	12	
Gate plateau voltage V_{DD} = 40 V, I_D = 2.9 A	$V_{(plateau)}$	-	4.7	-	V

Reverse Diode

Inverse diode continuous forward current T_A = 25 °C	I_S	-	-	2.9	A
Inverse diode direct current,pulsed T_A = 25 °C	I_{SM}	-	-	11.6	
Inverse diode forward voltage V_{GS} = 0 V, I_F = 5.8 A	V_{SD}	-	0.95	1.2	V
Reverse recovery time V_R = 30 V, I_F=I_S , di_F/dt = 100 A/µs	t_{rr}	-	45	56	ns
Reverse recovery charge V_R = 30 V, I_F=I_S , di_F/dt = 100 A/µs	Q_{rr}	-	0.08	0.12	µC

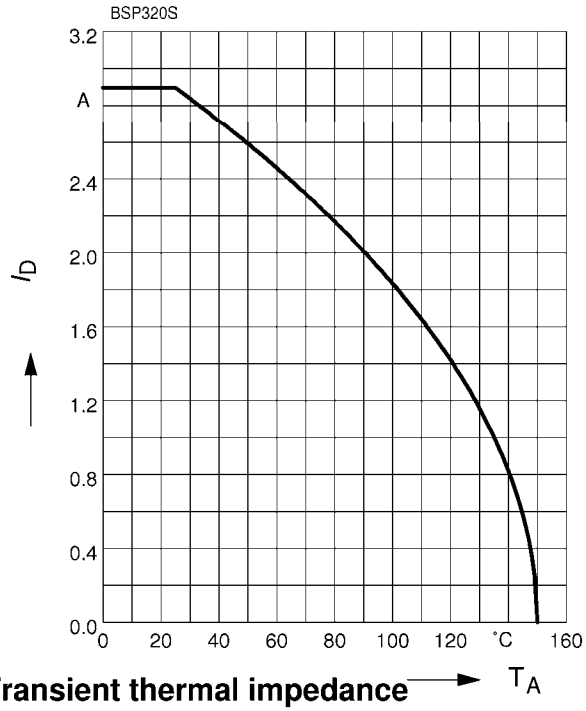
Power Dissipation

$P_{tot} = f(T_A)$



Drain current

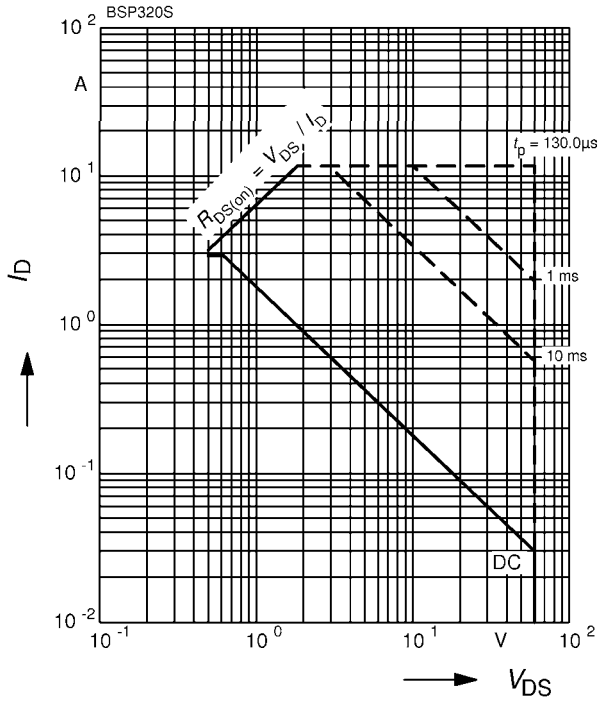
$I_D = f(T_A)$



Safe operating area

$I_D = f(V_{DS})$

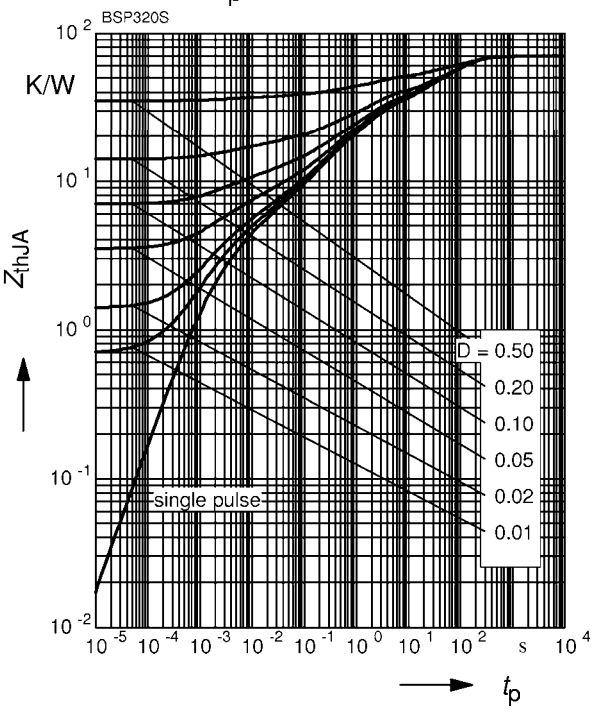
parameter : $D = 0$, $T_A = 25$ °C



Transient thermal impedance

$Z_{thJA} = f(t_p)$

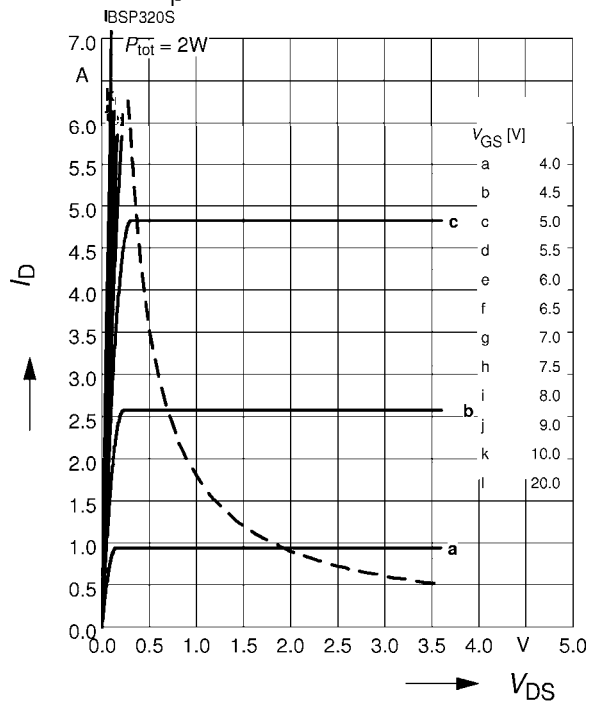
parameter : $D = t_p/T$



Typ. output characteristics

$I_D = f(V_{DS})$

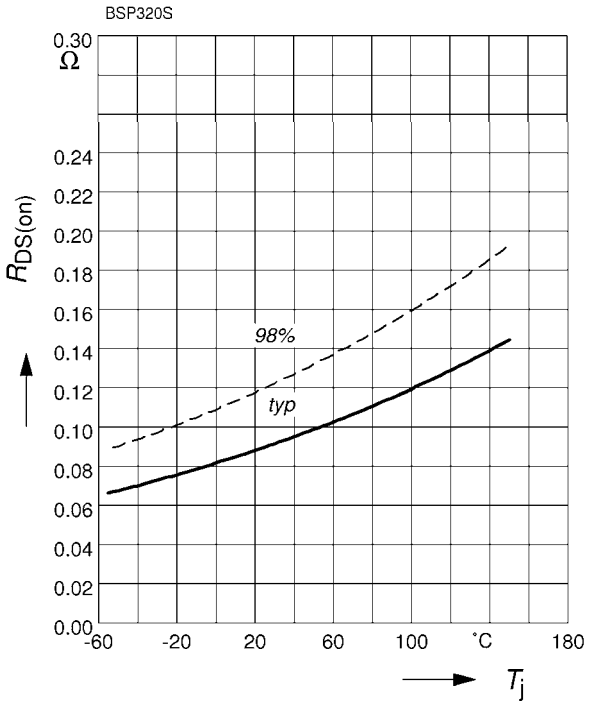
parameter: t_p = 80 µs



Drain-source on-resistance

$R_{DS(on)} = f(T_j)$

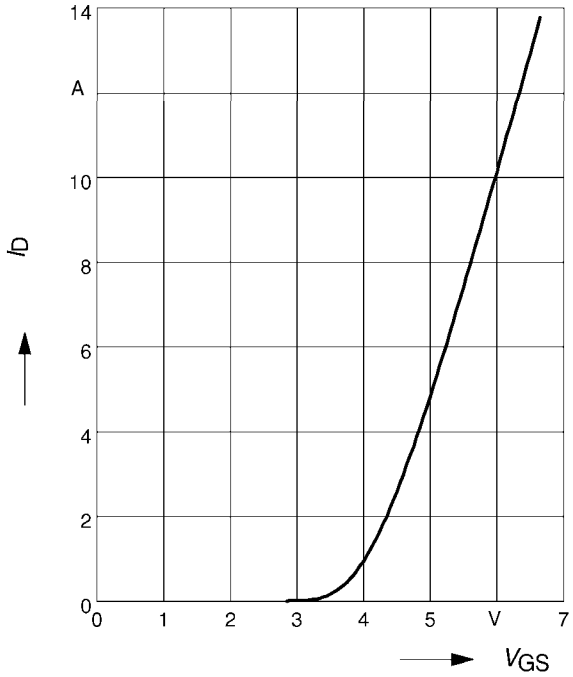
parameter : I_D = 2.9 A, V_{GS} = 10 V



Typ. transfer characteristics $I_D = f(V_{GS})$

parameter: t_p = 80 µs

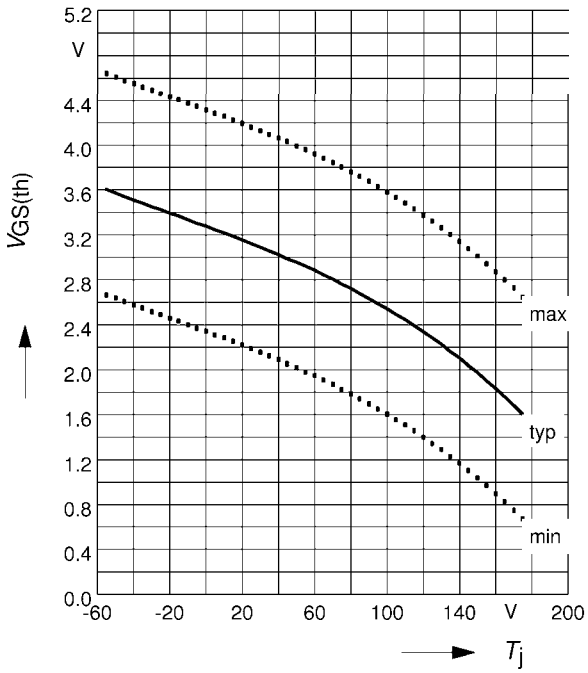
$V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$



Gate threshold voltage

$V_{GS(th)} = f(T_j)$

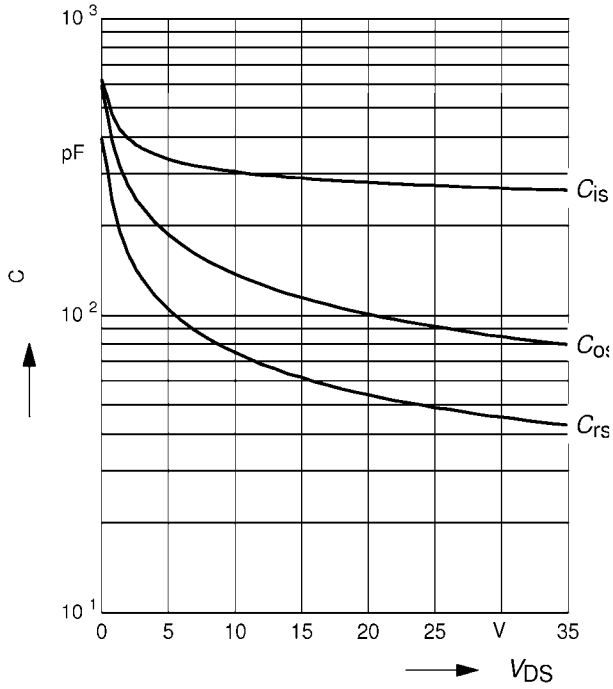
parameter : $V_{GS} = V_{DS}$, I_D = 20 µA



Typ. capacitances

$C = f(V_{DS})$

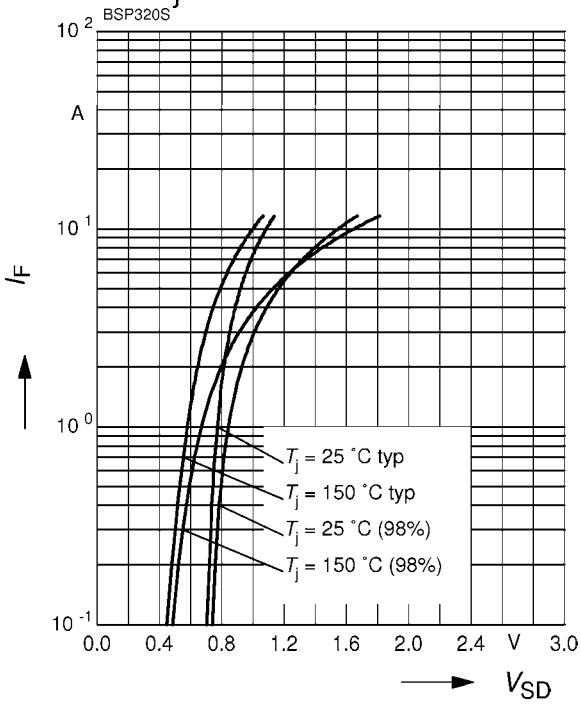
Parameter: V_{GS}=0 V, f=1 MHz



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

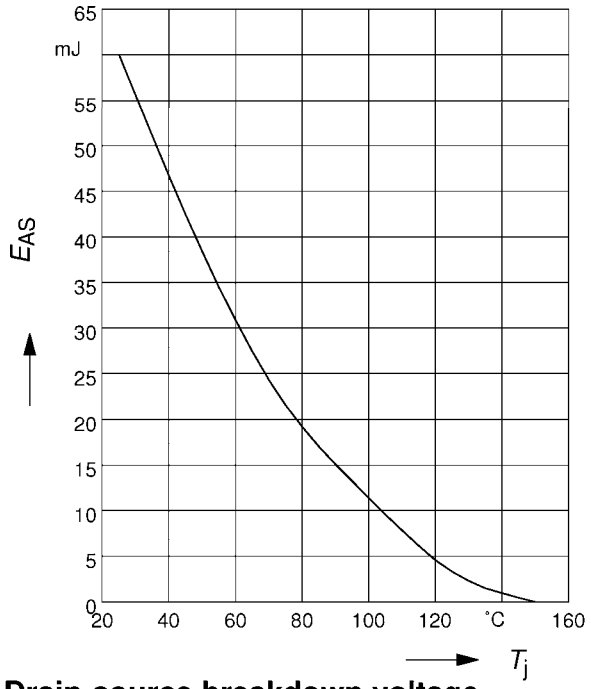
parameter: T_j , tp = 80 µs



Avalanche Energy $E_{AS} = f(T_j)$

parameter: I_D = 2.9 A, V_{DD} = 25 V

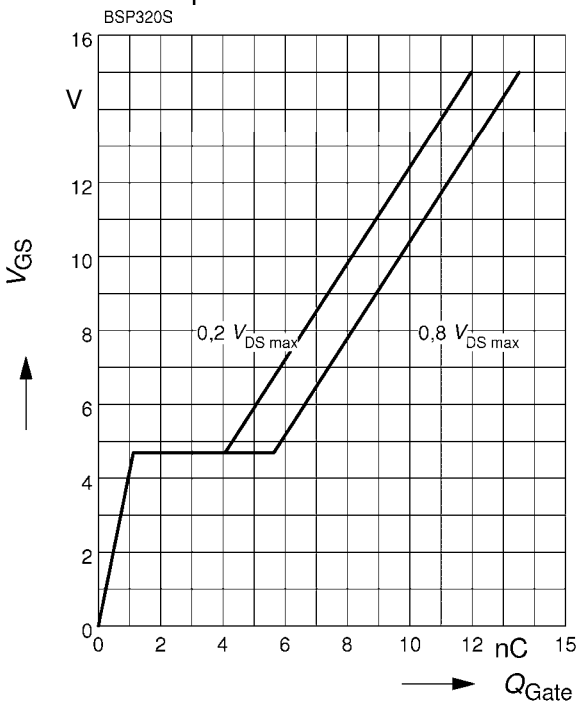
R_{GS} = 25 Ω



Typ. gate charge

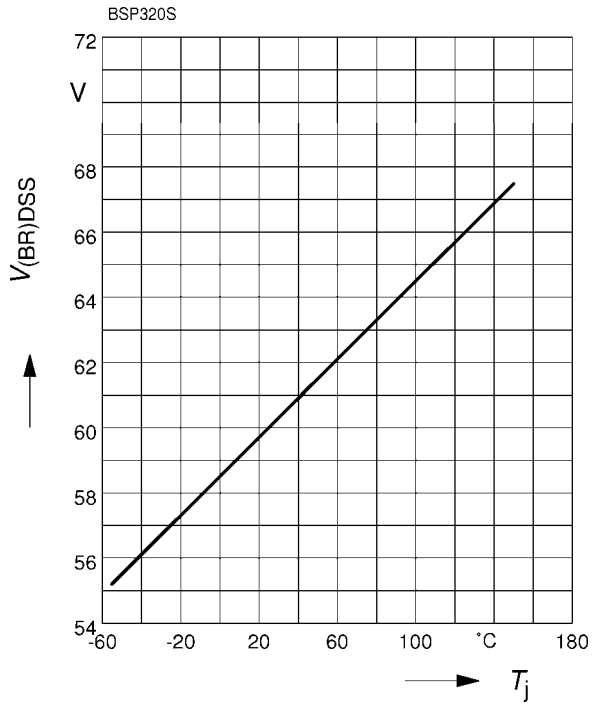
$V_{GS} = f(Q_{Gate})$

parameter: $I_{D\ puls}$ =2.9A



Drain-source breakdown voltage

$V_{(BR)DSS} = f(T_j)$



Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information
For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.