# PGY-I3C-EX-PD and PGY-I3C-EX-PD Lite I3C Protocol Exerciser and Analyzer

I3C and I3C LITE Protocol Exerciser and Analyzer

I3C Serial bus interface is emerging as a chosen interface for all future sensor connectivity in mobile phone and automotive Industry. This could also be chosen for low cost, reliable interface for future embedded electronic applications to address the new data intensive applications.

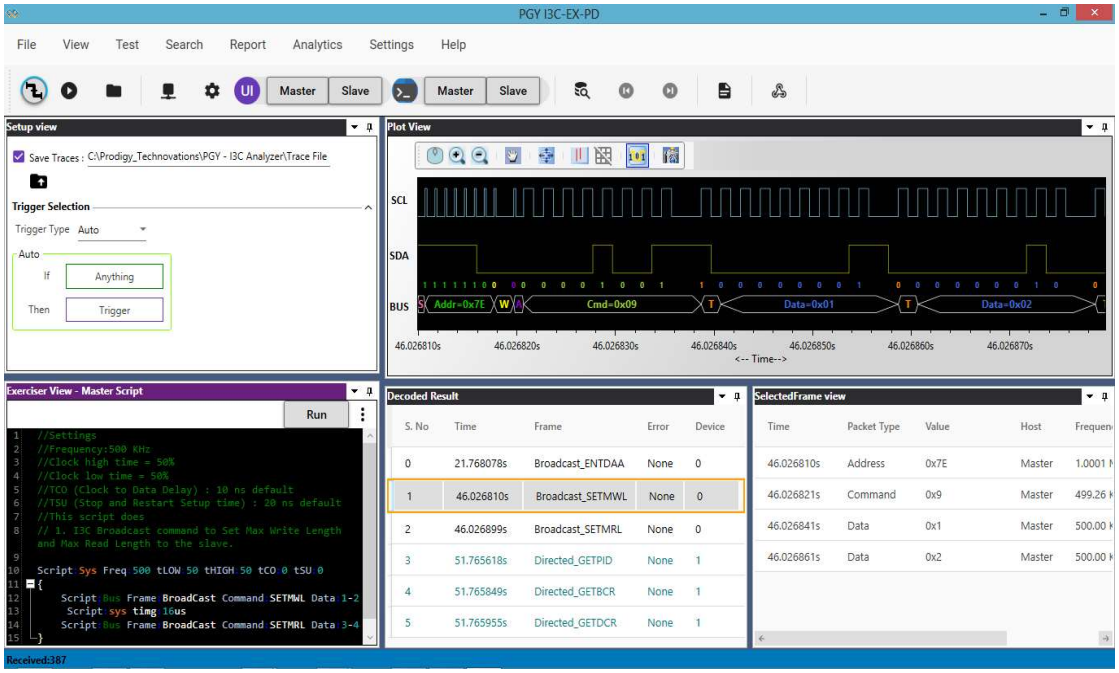
PGY-I3C-EX-PD is the leading instrument that enables the design and test engineers to test the I3C designs for its specifications by configuring PGY-I3C-EX-ED as master/slave, generating I3C traffic with error injection capability and decoding I3C Protocol decode packets.

**Features:**

- Supports v1.0/v1.1 Specifications[1]
- Ability to configure it as Master or Slave
- Ability to configure BCR, LVR and DCR registers
- Simultaneously generate I3C traffic and Protocol decode of the Bus
- Optional Compliance Test Specifications (CTS) test script support
- Supports legacy I2C slaves and Master
- Generate different I3C SDR and HDR Packets
- Supports IBI and Hot Plug capabilities
- Error Injection such CRC errors, parity errors and ACK/NACK errors
- Variable I3C data speeds and duty cycle
- PMIC device support as per JEDEC DDR5 spec requirement
- Margin test capability: Voltage and timing variation
- Continuous streaming of protocol data between instrument and host computer.
- Timing diagram of Protocol decoded bus
- Listing view of Protocol activity
- Error Analysis in Protocol Decode
- Ability to write exerciser script to combine multiple data frame generation at different data speeds
- USB2/3 host computer interface
- API support for automation in Python or C++

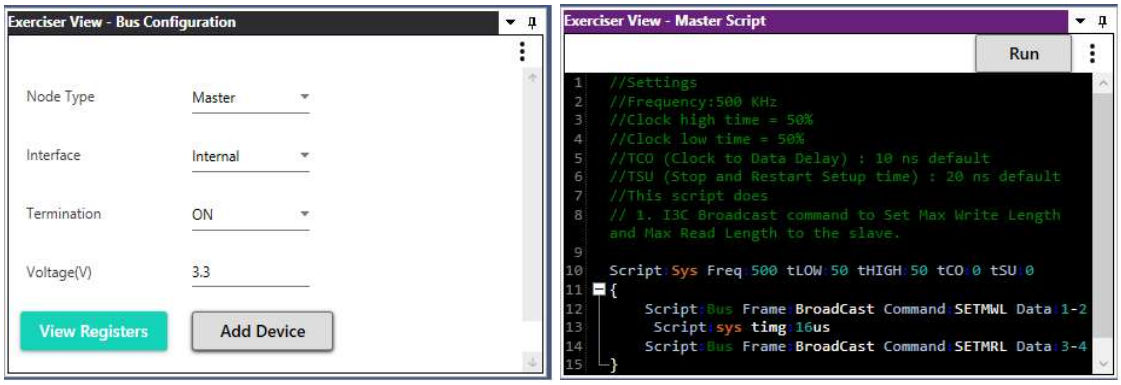
[1] v1.1 supports only one lane commands

## Multi-domain View




Multidomain View provides the complete view of I3C Protocol activity in single GUI. User can easily setup the analyzer to generate I3C/I2C traffic using a GUI or script. User can set different trigger conditions from the setup menu to capture Protocol activity at specific event and decode the transition between Master and Slave. The decoded results can be viewed in timing diagram and Protocol listing window with autocorrelation. State machine view provides switching of state machine between master and slave for design validation. This comprehensive view of information makes it industry best, offering an easy to use solution to debug the I3C protocol activity.

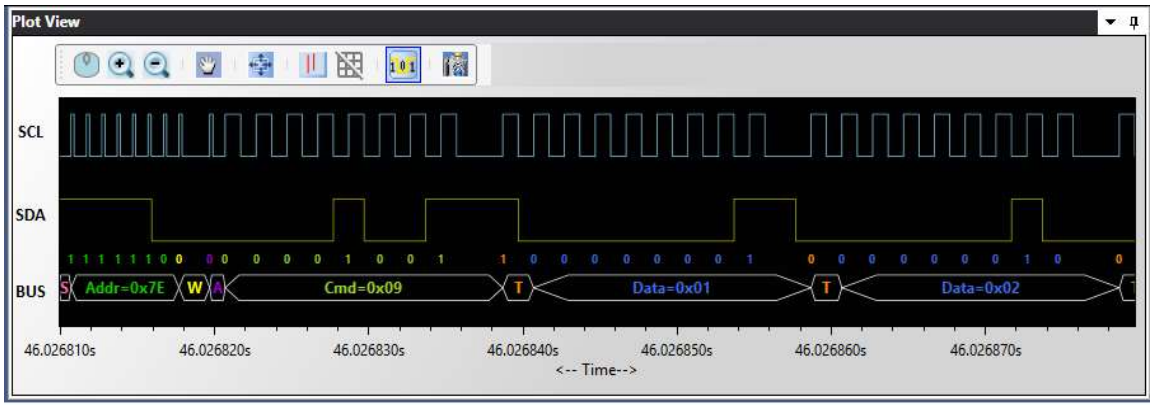
## Exerciser



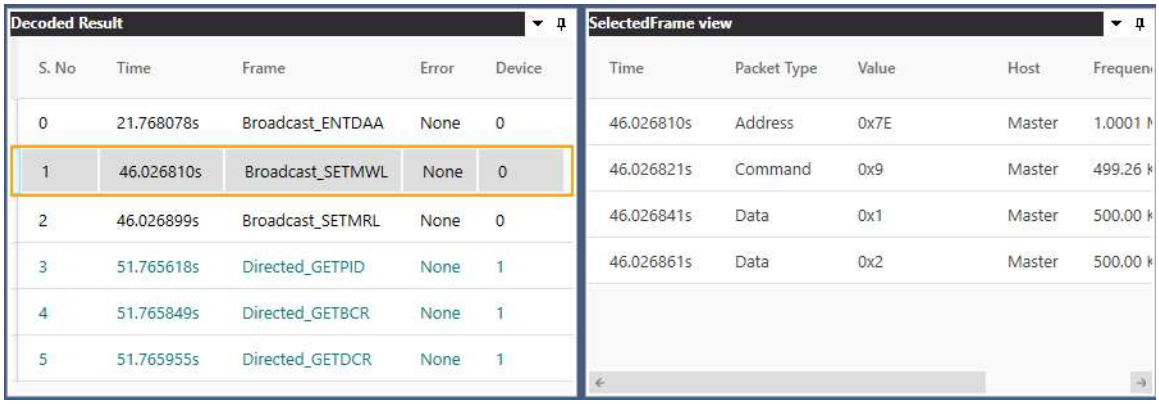
PGY-I3C-EX-PD supports I3C traffic generation using GUI and Script. User can generate simple traffic generation using the GUI to test the DUT. Script based GUI provides flexibility to emulate the complete expected traffic in real world including error injections. In this sample script user can generate I3C traffic as below:

Script line #10: Set system Frequency 500KHz, Duty cycle to 50%, clk to data delay to 10ns (default), start to restart setup time to 20ns (default)
Script line #12: SETMWL
Script line #13: Set system inter message gap to 16us
Script line #14: SETMRL

**Timing Diagram and Protocol Listing View**

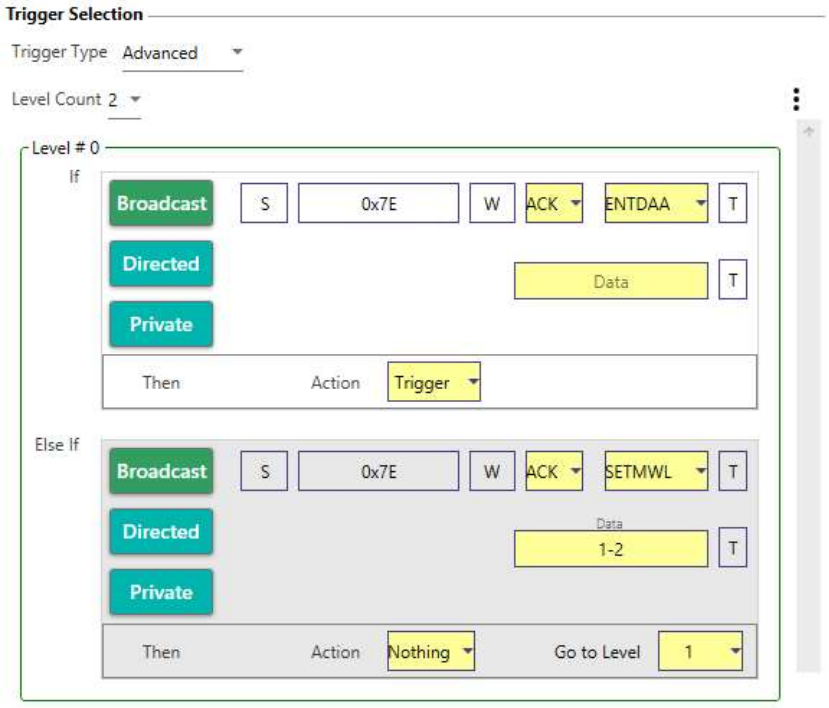



Timing view provides the plot of SCL and SDA signals with bus diagram. Overlaying of Protocol bits on the digital timing waveform will help easy debugging of Protocol decoded data. Cursor and Zoom features will make it convenient to analyze Protocol in timing diagram for any timing errors.




Protocol window provides the decoded packet information in each state and all packet details with error info in packet. Selected frame in Protocol listing window will be auto correlated in timing view to view the timing information of the packet.

**Powerful Trigger Capabilities**




PGY-I3C-EX-PD supports Auto, simple and advanced trigger capabilities. Analyzer can trigger on any of the Protocol packets such as Broadcast, Directed or Private message. Advanced Trigger provides the flexibility to monitor Multiple trigger conditions and can set multiple state trigger machine.

| PGY-I3C Specification | Features | PGY-I3C-EX-PD | PGY-I3C-EX-PD-Lite |
|---|---|---|---|
| **Exerciser:** | | | |
| Configurable | 1 Master + 3 Slaves<br>OR<br>1 Secondary Master + 2 Slaves | ✔ | ✔<br>1 Master + 1 Slave |
| I3C / I2C Traffic Generation | Custom I3C / I2C traffic generation | ✔ | ✔ |
| | Simulate real world network traffic | ✔ | ✕ |
| SCL Frequency | 400KHz to 13.5MHz | ✔ | ✔ |
| Voltage Drive Level | 1V to 3.3V at steps of 100mV | ✔ | ✕<br>Fixed to 1.2V, 1.8V, 2.5V & 3.3V |
| Hot Join | Yes, supported | ✔ | ✔ |
| IBI | Yes, supported | ✔ | ✔ |
| CCC Support | All CCC are supported in Master.<br>All CCC are supported in Slave except SETXTIME, ENTTM, ENTAS* | ✔ | ✔ |
| SCL Duty Cycle variation | User Defined | ✔ | ✕ |
| SCL & SDA Delay | User Defined | ✔ | ✕ |
| Delay between two messages | User Defined | ✔ | ✕ |
| Error injection | S0 to S5 types of errors specified in I3C specifications<br>CRC errors in DDR traffic<br>Preamble errors in DDR traffic<br>ACK / NACK Errors (Slave)<br>Master Abort<br>Non-Standard Frames<br>Non-Standard Start, Stop and HDR exit patterns, slave reset<br>Save and Load Scripts | ✔ | ✕ |
| API Support | Support for Automation of operation using Python or C++ | ✔ | ✕ |
| **Protocol Analysis:** | | | |
| Supports | I3C & I2C protocol decode | ✔ | ✔ |
| Protocol Views | Timing Diagram View<br>Protocol Listing View<br>Bus-Diagram to display Protocol packets with timing diagram plot | ✔ | ✔ |
| Protocol Trigger | Auto (Trigger on any packet)<br>Simple (Trigger on user defined I3C or I2C packet)<br>Advanced (Multistate & Multilevel trigger with timer capability) | ✔ | ✔ (No Advanced Trigger Support) |
| Capture Duration | Continuous streaming Protocol Data to host HDD/SSD | ✔ | ✔ |
| Protocol Error Report | S0 to S5 types of errors specified in the I3C specifications<br>CRC errors in DDR traffic<br>Preamble errors in DDR traffic<br>ACK /NACK Errors (Slave)<br>Master Abort<br>Non-Standard frames<br>Non-standard Start, Stop and HDR exit patterns. | ✔ | ✔ |
| Host Connectivity | USB 3.0 / 2.0 interface | ✔ | ✔ |

## Ordering Information

PGY-I3C-EX-PD **(v 1.0):** I3C Protocol Exerciser and Analyzer (supports v 1.0 specifications)
PGY-I3C-EX-PD **(v 1.1):** I3C Protocol Exerciser and Analyzer (supports v 1.1 specifications)
-Opt CTS **(v1.1):** Compliance test specifications for v 1.1 specifications
PGY-I3C-UPG **(v1.0 to v 1.1):** Upgrade Option from version 1.0 to version 1.1 specifications

PGY-I3C-EX-PD-**Lite (v 1.0):** I3C Protocol Exerciser and Analyzer (lite version supports v 1.0 specifications)
PGY-I3C-EX-PD-**Lite (v 1.1):** I3C Protocol Exerciser and Analyzer (lite version supports v 1.1 specifications)
PGY-I3C-UPG-**Lite (v1.0 to v 1.1):** Upgrade Option from version 1.0 to version 1.1 specifications

## Deliverables for PGY-I3C-EX-PD

PGY-I3C-EX-PD Unit
USB3.0 cable
PGY-I3C-EX-PD Software in CD
12V DC adopter
Flying lead probe cable with female connector to connect to DUT

## Deliverables for PGY-I3C-EX-PD-Lite

PGY-I3C-EX-PD-Lite unit
USB3.0 cable
PGY-I3C-EX-PD-Lite Software in CD
Flying Lead probe cable with connector

## Contact Information

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|---|---|
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## About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical Layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.