SST25PF020B

2-Mbit 2.3V-3.6V SPI Serial Flash

Features

- Single Voltage Read and Write Operations:
  - 2.3V-3.6V
- Serial Interface Architecture:
  - SPI Compatible: Mode 0 and Mode 3
- High-Speed Clock Frequency:
  - 80 MHz (2.7V-3.6V operation)
  - 50 MHz (2.3V-2.7V operation)
- Superior Reliability:
  - Endurance: 100,000 cycles (typical)
  - Greater than 100 years data retention
- Low-Power Consumption:
  - Active Read current: 10 mA (typical)
  - Standby current: 5 µA (typical)
- Flexible Erase Capability:
  - Uniform 4-Kbyte sectors
  - Uniform 32-Kbyte overlay blocks
  - Uniform 64-Kbyte overlay blocks
- Fast Erase and Byte Program:
  - Chip Erase time: 35 ms (typical)
  - Sector/Block Erase time: 18 ms (typical)
  - Byte Program time: 7 µs (typical)
- Auto Address Increment (AAI) Programming:
  - Decrease total chip programming time over Byte Program operations
- End-of-Write Detection:
  - Software polling the BUSY bit in STATUS register
  - Busy Status readout on SO pin in AAI Mode
- Hold Pin (HOLD#):
  - Suspends a serial sequence to the memory without deselecting the device
- Write Protection (WP#):
  - Enables/Disables the Lock-Down function of the STATUS register
- Software Write Protection:
  - Write protection through Block Protection bits in STATUS register
- Temperature Range:
  - Commercial: 0°C to +70°C
- All devices are RoHS compliant

Packages

- 8-Lead SOIC (150 mils), 8-Contact USON (3 mm x 2 mm) and 8-Contact WSON (6 mm x 5 mm)

Product Description

The 25 series Serial Flash family features a four-wire, SPI compatible interface that allows for a low pin-count package which occupies less board space and ultimately lowers total system costs. The SST25PF020B devices are enhanced with improved operating frequency and even lower power consumption.

SST25PF020B SPI serial Flash memories are manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

The SST25PF020B devices significantly improve performance and reliability, while lowering power consumption. The devices write (Program or Erase) with a single power supply of 2.3V-3.6V for SST25PF020B. The total energy consumed is a function of the applied voltage, current and time of application. Since for any given voltage range the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any erase or program operation is less than alternative Flash memory technologies.

See Figure 2-1 for pin assignments.

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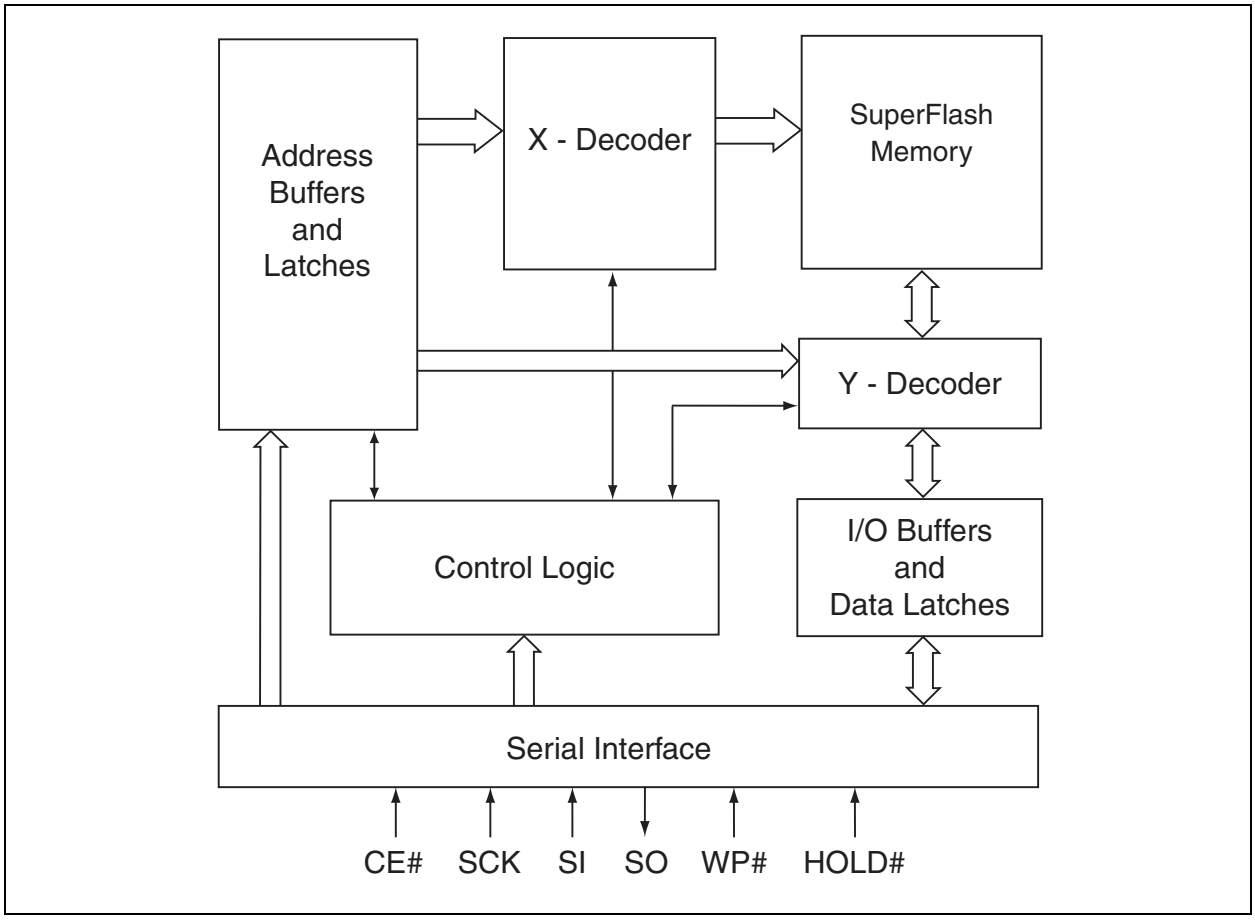
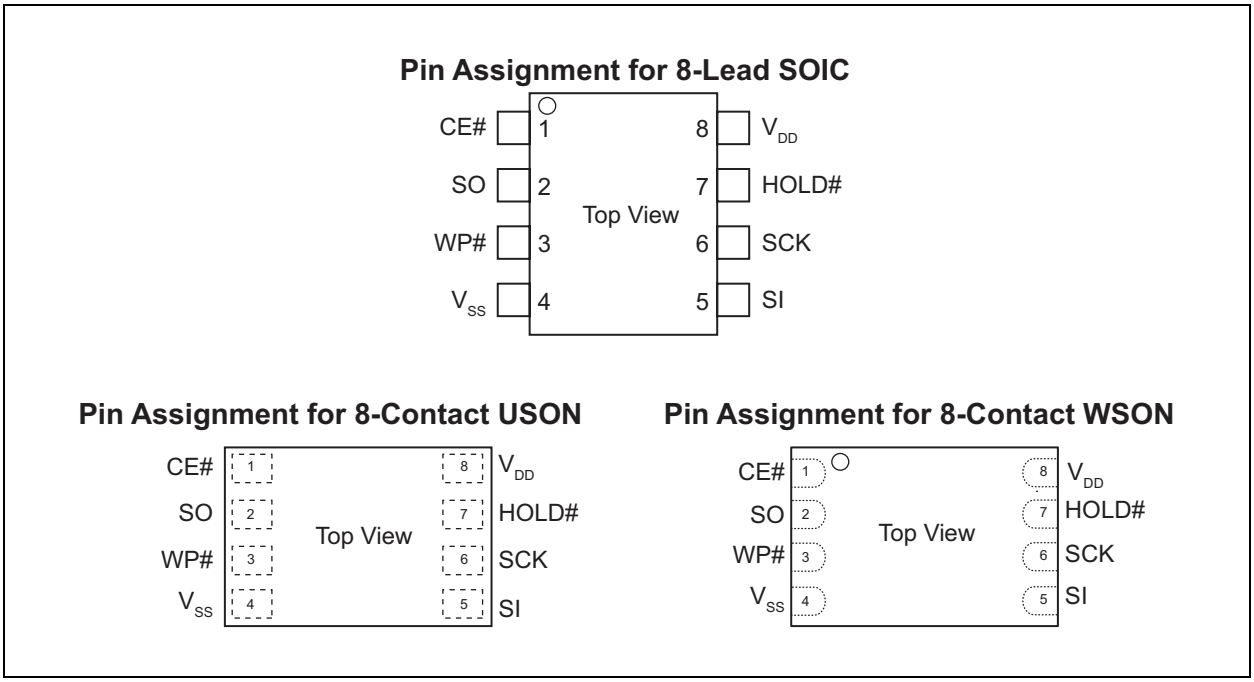
1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION

FIGURE 2-1: PIN DESCRIPTIONS



PIN DESCRIPTION

Symbol	Pin Name	Functions
CE#	Chip Enable	The device is enabled by a high-to-low transition on CE#. CE# must remain low for the duration of any command sequence.
SO	Serial Data Output	Transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. Outputs Flash busy status during AAI Programming when reconfigured as RY/BY# pin. See **Section 5.5 "End-of-Write Detection"** for details.
WP#	Write-Protect	The Write-Protect (WP#) pin is used to enable/disable BPL bit in the STATUS register.
SI	Serial Data Input	Transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SCK	Serial Clock	Provide the timing of the serial interface. Commands, addresses or input data are latched on the rising edge of the input, while output data is shifted out on the falling edge of the clock input.
HOLD#	Hold	Temporarily stop serial communication with SPI Flash memory without resetting the device.
VDD	Power Supply	Provide power supply voltage: 2.3V-3.6V.
VSS	Ground	

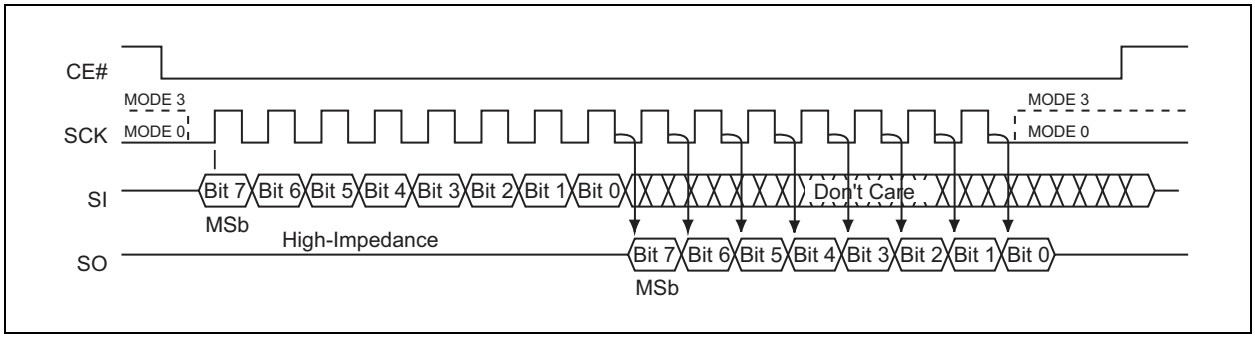
3.0 MEMORY ORGANIZATION

The SST25PF020B SuperFlash memory array is organized in uniform 4-Kbyte erasable sectors with 32-Kbyte overlay blocks and 64-Kbyte overlay erasable blocks.

4.0 DEVICE OPERATION

The SST25PF020B is accessed through the Serial Peripheral Interface (SPI) bus compatible protocol. The SPI bus consists of four control lines: Chip Enable (CE#) is used to select the device and data is accessed through the Serial Data Input (SI), Serial Data Output (SO) and Serial Clock (SCK). The SST25PF020B supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 4-1, is the state of the SCK signal when the bus master is in Standby mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data Input (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

FIGURE 4-1: SPI PROTOCOL



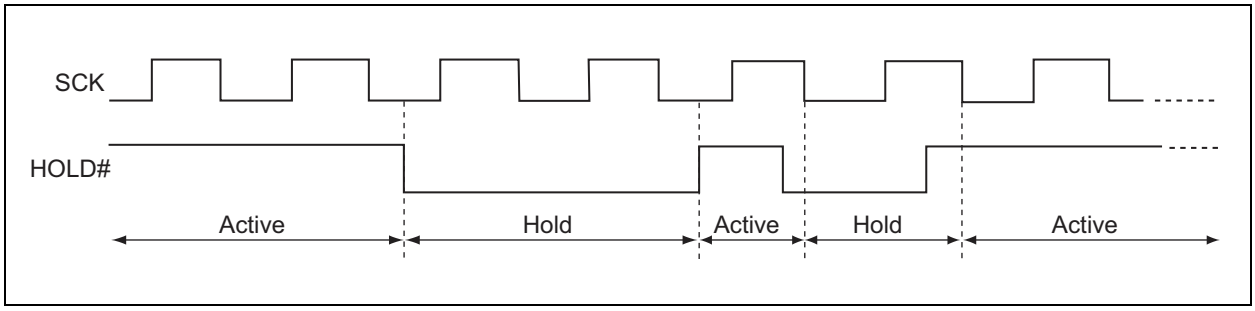
4.1 Hold Operation

The HOLD# pin is used to pause a serial sequence underway with the SPI Flash memory without resetting the clocking sequence. To activate the HOLD# mode, CE# must be in active-low state. The HOLD# mode begins when the SCK active-low state coincides with the falling edge of the HOLD# signal. The HOLD mode ends when the HOLD# signal's rising edge coincides with the SCK active-low state.

If the falling edge of the HOLD# signal does not coincide with the SCK active-low state, then the device enters Hold mode when the SCK next reaches the active-low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active-low state, then the device exits in Hold mode when the SCK next reaches the active-low state (see Figure 4-2). Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven high during a Hold condition, the device returns to Standby mode. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active-high and CE# must be driven active-low (see Figure 4-2).

FIGURE 4-2: HOLD CONDITION WAVEFORM



4.2 Write Protection

SST25PF020B provides software write protection. The Write-Protect pin (WP#) enables or disables the lock-down function of the STATUS register. The Block Protection bits (BP1, BP0 and BPL) in the STATUS register and the Top/Bottom Sector Protection STATUS bits (TSP and BSP) in STATUS register 1 provide write protection to the memory array and the STATUS register. See Table 4-4 for the Block Protection description.

4.2.1 WRITE-PROTECT PIN (WP#)

The Write-Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the STATUS register. When WP# is driven low, the execution of the Write STATUS Register (WRSR) instruction is determined by the value of the BPL bit (see Table 4-1). When WP# is high, the lock-down function of the BPL bit is disabled.

TABLE 4-1: CONDITIONS TO EXECUTE WRSR INSTRUCTION

WP#	BPL	Execute WRSR Instruction
L	1	Not allowed
L	0	Allowed
H	X	Allowed

4.3 STATUS Register

The software STATUS register provides status on whether the Flash memory array is available for any read or write operation, whether the device is write enabled and the state of the memory write-protected. During an internal erase or program operation, the STATUS register may be read only to determine the completion of an operation in progress. Table 4-2 describes the function of each bit in the software STATUS register.

TABLE 4-2: SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-Up	Read/Write
0	BUSY	1 = Internal write operation is in progress 0 = No internal write operation is in progress	0	R
1	WEL	1 = Device is memory write enabled 0 = Device is not memory write enabled	0	R
2	BP0	Indicate current level of block write protection (see)	1	R/W
3	BP1	Indicate current level of block write protection (see)	1	R/W
4:5	RES	Reserved for future use	0	N/A
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte Program mode	0	R
7	BPL	1 = BP1, BP0 are read-only bits 0 = BP1, BP0 are read/writable	0	R/W

4.4 Software STATUS Register 1

The Software STATUS Register 1 is an additional register that contains Top Sector and Bottom Sector Protection bits. These register bits are read/writable and determine the lock and unlock status of the top and bottom sectors. Table 4-3 describes the function of each bit in the Software STATUS Register 1.

TABLE 4-3: SOFTWARE STATUS REGISTER 1

Bit	Name	Function	Default at Power-Up	Read/Write
0:1	RES	Reserved for future use	0	N/A
2	TSP	Top Sector Protection status 1 = Indicates higher sector is write-locked 0 = Indicates highest sector is write-accessible	0	R/W
3	BSP	Bottom Sector Protection status 1 = Indicates lowest sector is write-locked 0 = Indicates lowest sector is write-accessible	0	R/W
4:7	RES	Reserved for future use	0	N/A

4.4.1 BUSY

The BUSY bit determines whether there is an internal erase or program operation in progress. A '1' for the BUSY bit indicates the device is busy with an operation in progress. A '0' indicates the device is ready for the next valid operation.

4.4.2 WRITE ENABLE LATCH (WEL)

The Write Enable Latch bit indicates the status of the internal memory Write Enable Latch. If the Write Enable Latch bit is set to '1', it indicates the device is write enabled. If the bit is set to '0' (Reset), it indicates the device is not write enabled and does not accept any memory write (program/erase) commands. The Write Enable Latch bit is automatically reset under the following conditions:

- Power-Up
- Write Disable (WRDI) instruction completion
- Byte Program instruction completion
- Auto Address Increment (AAI) programming is completed or reached its highest unprotected memory address
- Sector Erase instruction completion
- Block Erase instruction completion
- Chip Erase instruction completion
- Write STATUS Register instructions

4.4.3 AUTO ADDRESS INCREMENT (AAI)

The Auto Address Increment Programming Status bit provides status on whether the device is in AAI programming mode or Byte Program mode. The default at power-up is Byte Program mode.

4.4.4 BLOCK PROTECTION (BP1, BP0)

The Block Protection (BP1, BP0) bits define the size of the memory area, as defined in Table 4-4, to be software protected against any memory write (program or erase) operation. The Write STATUS Register (WRSR) instruction is used to program the BP1 and BP0 bits as long as WP# is high or the Block Protect Lock (BPL) bit is '0'. Chip Erase can only be executed if Block Protection bits are all '0'. After power-up, BP1 and BP0 are set to '1'.

4.4.5 BLOCK PROTECTION LOCK-DOWN (BPL)

WP# pin driven low (V_{IL}) enables the Block Protection Lock Down (BPL) bit. When BPL is set to '1', it prevents any further alteration of the BPL, BP1 and BP0 bits of the STATUS register and BSP and TSP of STATUS register 1. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect and its value is "don't care". After power-up, the BPL bit is reset to '0'.

TABLE 4-4: SOFTWARE STATUS REGISTER BLOCK PROTECTION(1)

Protection Level	STATUS Register Bit(2)		Protected Memory Address
	BP1	BP0	2 Mbit
0	0	0	None
1 (1/4 Memory Array)	0	1	030000H-03FFFFH
1 (1/2 Memory Array)	1	0	020000H-03FFFFH
1 (Full Memory Array)	1	1	000000H-03FFFFH

Note 1: x = "don't care" (RESERVED) default is '0'

2: Default at power-up for BP1 and BP0 is '11' (all blocks protected)

4.4.6 TOP SECTOR PROTECTION/BOTTOM SECTOR PROTECTION

The Top Sector Protection (TSP) and Bottom Sector Protection (BSP) bits independently indicate whether the highest and lowest sector locations are write locked or write accessible. When TSP or BSP is set to '1', the respective sector is write locked; when set to '0,' the respective sector is write accessible. If TSP or BSP is set to '1' and if the top or bottom sector is within the boundary of the target address range of the program or erase instruction, the initiated instruction (Byte program, AAI Word program, Sector Erase, Block Erase and Chip Erase) will not be executed. Upon power-up, the TSP and BSP bits are automatically reset to '0'.

5.0 INSTRUCTIONS

Instructions are used to read, write (erase and program) and configure the SST25PF020B. The instruction bus cycles are 8 bits each for commands (Op Code), data and addresses. Prior to executing any Byte program, Auto Address Increment (AAI) programming, Sector Erase, Block Erase, Write STATUS Register or Chip Erase instructions, the Write Enable (WREN) instruction must be executed first. The complete list of instructions is provided in Table 5-1. All instructions are synchronized from a high-to-low transition of CE#. Inputs will be accepted on the rising edge of SCK starting with the Most Significant bit (MSb). CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID and Read STATUS Register instructions). Any low-to-high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to Standby mode. Instruction commands (Op Code), addresses and data are all input from the Most Significant bit first.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS

Instruction	Description	Op Code Cycle(1)	Address Cycle(s)(2)	Dummy Cycle(s)	Data Cycle(s)
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞
High-Speed Read	Read Memory at Higher Speed	0000 1011b (0BH)	3	1	1 to ∞
4-Kbyte Sector-Erase(3)	Erase 4 Kbytes of Memory Array	0010 0000b (20H)	3	0	0
32-Kbyte Block Erase(4)	Erase 32-Kbyte Block of Memory Array	0101 0010b (52H)	3	0	0
64-Kbyte Block Erase(5)	Erase 64-Kbyte Block of Memory Array	1101 1000b (D8H)	3	0	0
Chip Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0
Byte Program	Program One Data Byte	0000 0010b (02H)	3	0	1
AAI Word Program(6)	Auto Address Increment Programming	1010 1101b (ADH)	3	0	2 to ∞
RDSR(7)	Read STATUS Register	0000 0101b (05H)	0	0	1 to ∞
RDSR1	Read STATUS Register 1	0011 0101b (35H)	0	0	1 to ∞
EWSR	Enable Write STATUS Register	0101b 0000b (50H)	0	0	0
WRSR	Write STATUS Register	0000 0001b (01H)	0	0	1 or 2
WREN	Write Enable	0000 0110b (06H)	0	0	0
WRDI	Write Disable	0000 0100b (04H)	0	0	0
RDID(8)	Read ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞
JEDEC ID	JEDEC ID Read	1001 1111b (9FH)	0	0	3 to ∞
EBSY	Enable SO to Output RY/BY# Status during AAI Programming	0111 0000b (70H)	0	0	0
DBSY	Disable SO as RY/BY# Status during AAI Programming	1000 0000b (80H)	0	0	0

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS (CONTINUED)

Instruction	Description	Op Code Cycle(1)	Address Cycle(s)(2)	Dummy Cycle(s)	Data Cycle(s)

Note 1: One bus cycle is eight clock periods.

2: Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.

3: 4-Kbyte Sector Erase addresses: use A_{MS}-A_{12}, remaining addresses are “don’t care” but must be set either at V_{IL} or V_{IH}.

4: 32-Kbyte Block Erase addresses: use A_{MS}-A_{15}, remaining addresses are “don’t care” but must be set either at V_{IL} or V_{IH}.

5: 64-Kbyte Block Erase addresses: use A_{MS}-A_{16}, remaining addresses are “don’t care” but must be set either at V_{IL} or V_{IH}.

6: To continue programming to the next sequential address location, enter the 8-bit command, ADH, followed by 2 bytes of data to be programmed. Data Byte 0 will be programmed into the initial address [A_{23}-A_1] with A_0 = 0, Data Byte 1 will be programmed into the initial address [A_{23}-A_1] with A_0 = 1.

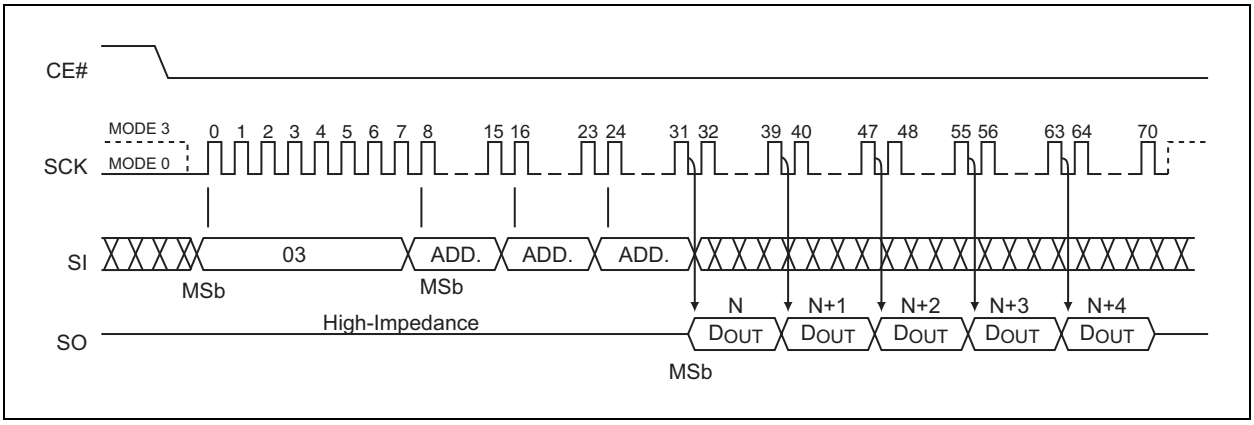
7: The Read STATUS Register is continuous with ongoing clock cycles until terminated by a low-to-high transition on CE#.

8: Manufacturer’s ID is read with A_0 = 0 and Device ID is read with A_0 = 1. All other address bits are 00H. The Manufacturer’s ID and device ID output stream is continuous until terminated by a low-to-high transition on CE#.

5.1 Read

During the READ instruction, the device outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer will automatically increment to the beginning (wrap-around) of the address space. Once the data from address location 3FFFFH has been read, the next output will be from address location 000000H. The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits [A_{23}-A_0]. CE# must remain active-low for the duration of the Read cycle. See Figure 5-1 for the Read sequence.

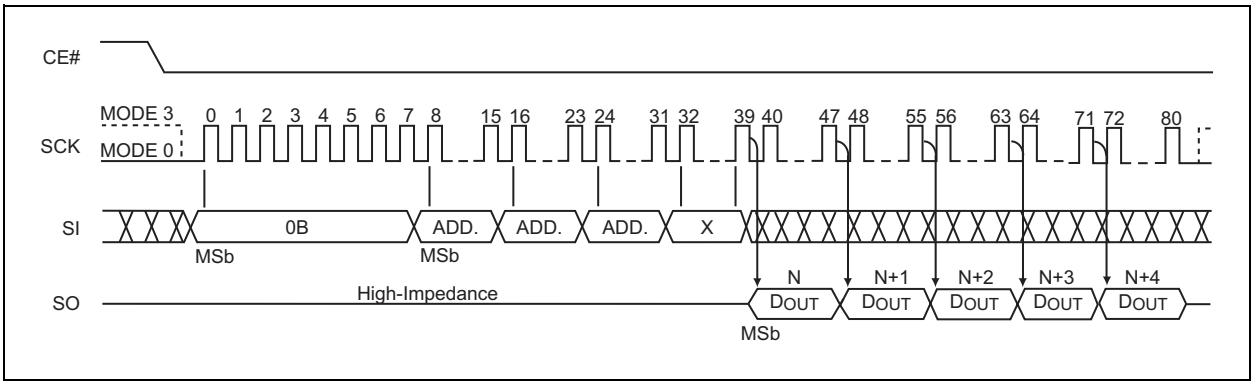
FIGURE 5-1: READ SEQUENCE



5.2 High-Speed Read

The High-Speed Read instruction is initiated by executing an 8-bit command, 0BH, followed by address bits [A23-A0] and a dummy byte. CE# must remain active-low for the duration of the High-Speed Read cycle. See Figure 5-2 for the High-Speed Read sequence. Following a dummy cycle, the High-Speed Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer will automatically increment to the beginning (wrap-around) of the address space. Once the data from address location 3FFFH has been read, the next output will be from address location 00000H.

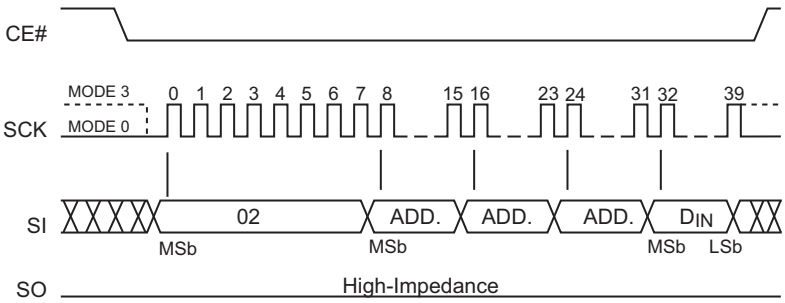
FIGURE 5-2: HIGH-SPEED READ SEQUENCE



5.3 Byte Program

The Byte Program instruction programs the bits in the selected byte to the desired data. The selected byte must be in the erased state (FFH) when initiating a Program operation. A Byte Program instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Byte Program instruction. The Byte Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits [A23-A0]. Following the address, the data is input in order from MSb (bit 7) to LSb (bit 0). CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait TBP for the completion of the internal self-timed Byte Program operation. See Figure 5-3 for the Byte Program sequence.

FIGURE 5-3: BYTE PROGRAM SEQUENCE



5.4 Auto Address Increment (AAI) Word Program

The AAI program instruction allows multiple bytes of data to be programmed without reissuing the next sequential address location. This feature decreases total programming time when multiple bytes or entire memory array is to be programmed. An AAI Word program instruction pointing to a protected memory area will be ignored. The selected address range must be in the erased state (FFH) when initiating an AAI Word Program operation. While within AAI Word Programming sequence, only the following instructions are valid:

- for software end-of-write detection – AAI Word (ADH), WRDI (04H) and RDSR (05H)
- for hardware end-of-write detection – AAI Word (ADH) and WRDI (04H)

There are three options to determine the completion of each AAI Word program cycle: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the software STATUS register or wait TBP (see **Section 5.5 "End-of-Write Detection"** for details).

Prior to any write operation, the Write Enable (WREN) instruction must be executed. Initiate the AAI Word Program instruction by executing an 8-bit command, ADH, followed by address bits [A23-A0]. Following the addresses, two bytes of data are input sequentially, each one from MSb (Bit 7) to LSb (Bit 0). The first byte of data (D0) is programmed into the initial address [A23-A1] with A0 = 0, the second byte of data (D1) is programmed into the initial address [A23-A1] with A0 = 1. CE# must be driven high before executing the AAI Word Program instruction. Check the Busy status before entering the next valid command. Once the device indicates it is no longer busy, data for the next two sequential addresses may be programmed, followed by the next two, and so on. When programming the last desired word or the highest unprotected memory address, check the Busy status using either the hardware or software (RDSR instruction) method to check for program completion.

Once programming is complete, use the applicable method to terminate AAI. If the device is in Software End-of-Write Detection mode, execute the Write Disable (WRDI) instruction, 04H. If the device is in AAI Hardware End-of-Write Detection mode, execute the Write Disable (WRDI) instruction, 04H, followed by the 8-bit DBSY command, 80H. There is no wrap mode during AAI programming once the highest unprotected memory address is reached. See Figures 5-6 and 5-7 for the AAI Word programming sequence.

5.5 End-of-Write Detection

There are three methods to determine completion of a program cycle during AAI Word programming: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the Software STATUS register or wait TBP. The Hardware End-of-Write detection method is described in **Section 5.6 "Hardware End-of-Write Detection"**

5.6 Hardware End-of-Write Detection

The Hardware End-of-Write detection method eliminates the overhead of polling the BUSY bit in the Software STATUS register during an AAI Word program operation. The 8-bit command, 70H, configures the Serial Output (SO) pin to indicate Flash Busy status during AAI Word programming (see Figure 5-4). The 8-bit command, 70H, must be executed prior to initiating an AAI Word-Program instruction. Once an internal programming operation begins, asserting CE# will immediately drive the status of the internal Flash status on the SO pin. A '0' indicates the device is busy and a '1' indicates the device is ready for the next instruction. De-asserting CE# will return the SO pin to tri-state. While in AAI and Hardware End-of-Write detection mode, the only valid instructions are AAI Word (ADH) and WRDI (04H). To exit AAI Hardware End-of-Write detection, first execute WRDI instruction, 04H, to reset the Write Enable Latch bit (WEL = 0) and AAI bit. Then execute the 8-bit DBSY command, 80H, to disable RY/BY# status during the AAI command (see Figures 5-5 and 5-6).

FIGURE 5-4: ENABLE SO AS HARDWARE RY/BY# DURING AAI PROGRAMMING

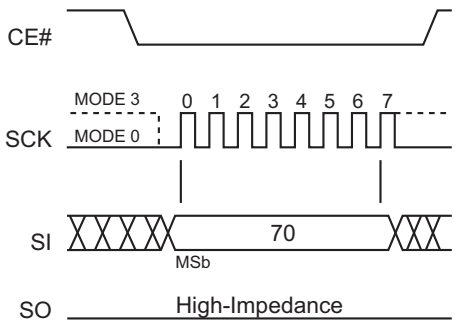


FIGURE 5-5: DISABLE SO AS HARDWARE RY/BY# DURING AAI PROGRAMMING

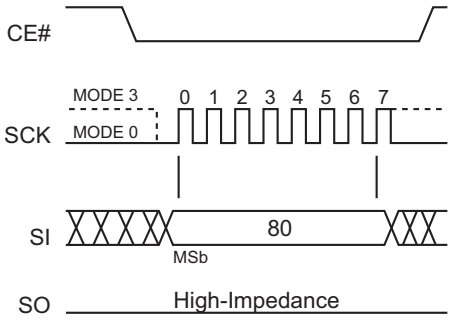
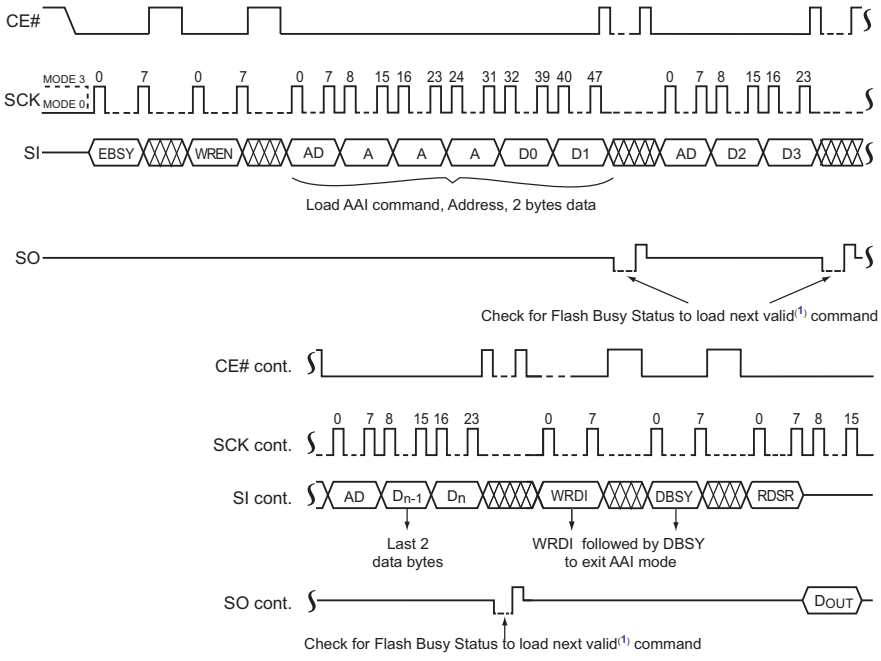
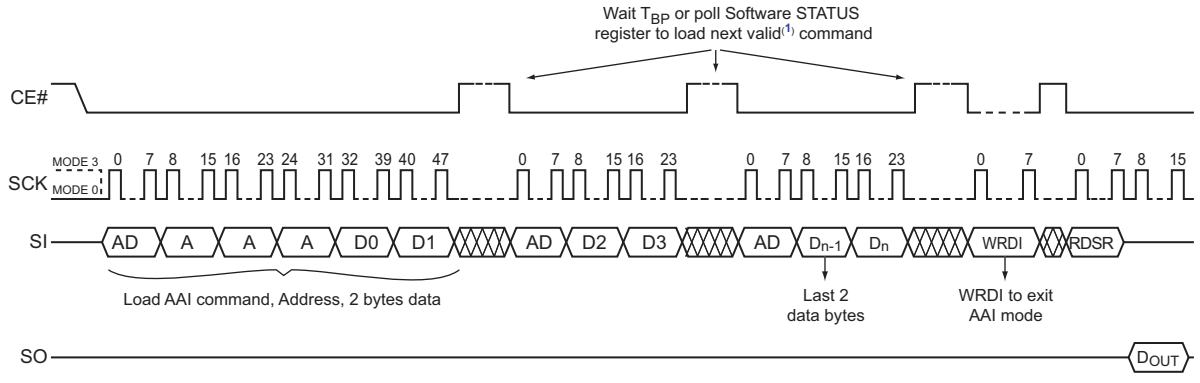


FIGURE 5-6: AUTO ADDRESS INCREMENT (AAI) WORD PROGRAM SEQUENCE WITH HARDWARE END-OF-WRITE DETECTION



Note: 1. Valid commands during AAI programming: AAI command or WRDI command
2. User must configure the SO pin to output Flash Busy status during AAI programming

FIGURE 5-7: AUTO ADDRESS INCREMENT (AAI) WORD PROGRAM SEQUENCE WITH SOFTWARE END-OF-WRITE DETECTION

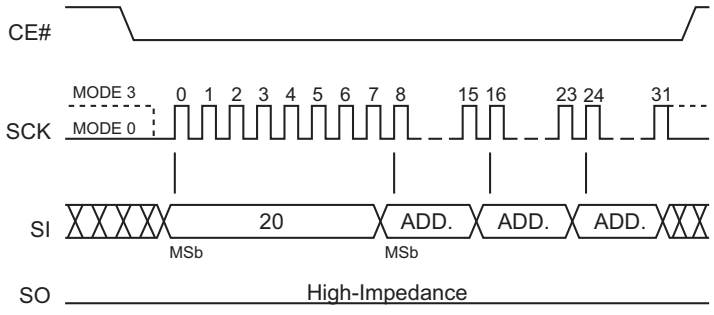


Note: 1. Valid commands during AAI programming: AAI command, RDSR command, or WRDI command

5.7 4-Kbyte Sector Erase

The Sector Erase instruction clears all bits in the selected 4-Kbyte sector to FFH. A Sector Erase instruction applied to a protected memory area will be ignored. Prior to any write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of any command sequence. The Sector Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{12}] (A_{MS} = Most Significant address) are used to determine the sector address (SAX), remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait T_{SE} for the completion of the internal self-timed Sector Erase cycle. See Figure 5-8 for the Sector Erase sequence.

FIGURE 5-8: SECTOR ERASE SEQUENCE



5.8 32-Kbyte and 64-Kbyte Block Erase

The 32-Kbyte Block Erase instruction clears all bits in the selected 32-Kbyte block to FFH. A Block Erase instruction applied to a protected memory area will be ignored. The 64-Kbyte Block Erase instruction clears all bits in the selected 64-Kbyte block to FFH. A Block Erase instruction applied to a protected memory area will be ignored. Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of any command sequence. The 32-Kbyte Block Erase instruction is initiated by executing an 8-bit command, 52H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{15}] (A_{MS} = Most Significant Address) are used to determine block address (BAX), remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The 64-Kbyte Block Erase instruction is initiated by executing an 8-bit command D8H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{15}] are used to determine block address (BAX), remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait T_{BE} for the completion of the internal self-timed 32-Kbyte Block Erase or 64-Kbyte Block Erase cycles. See Figures 5-9 and 5-10 for the 32-Kbyte Block Erase and 64-Kbyte Block Erase sequences.

FIGURE 5-9: 32-KBYTE BLOCK ERASE SEQUENCE

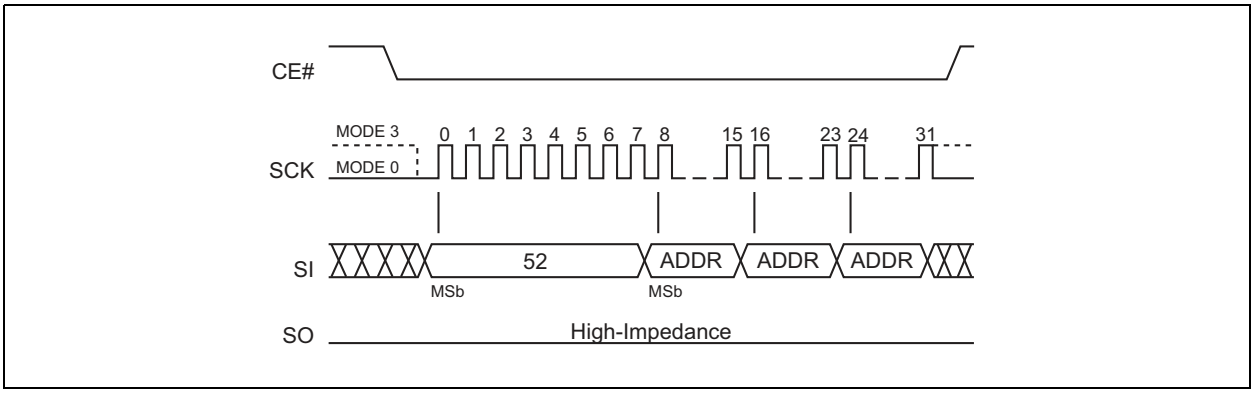
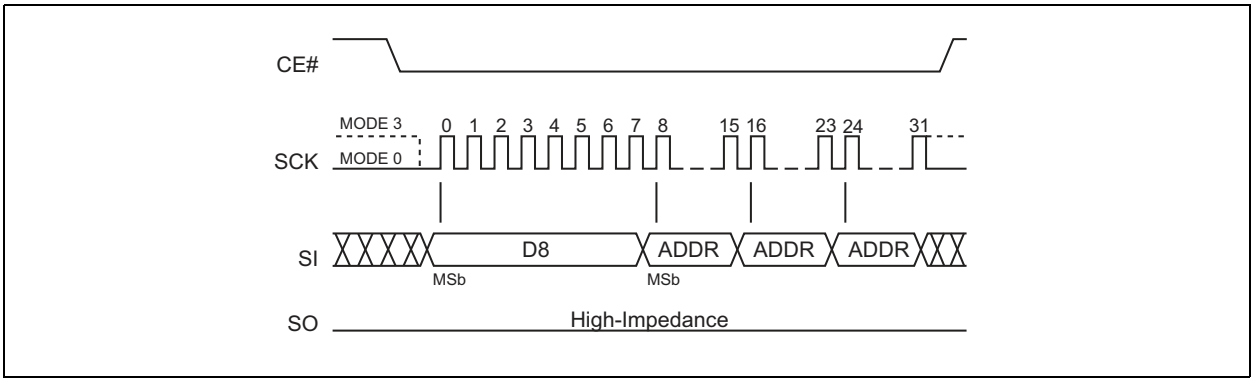


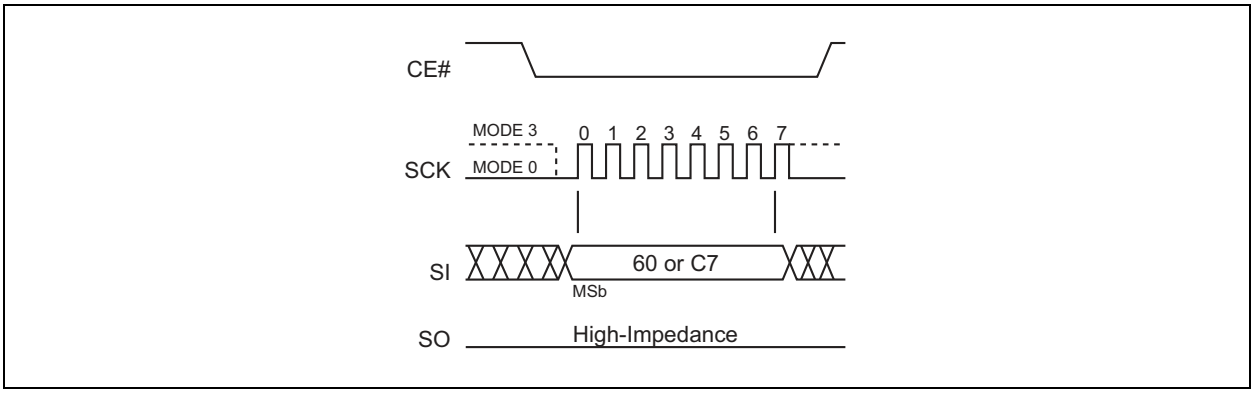
FIGURE 5-10: 64-KBYTE BLOCK ERASE SEQUENCE



5.9 Chip Erase

The Chip Erase instruction clears all bits in the device to FFH. A Chip Erase instruction will be ignored if any of the memory area is protected. Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Chip Erase instruction sequence. The Chip Erase instruction is initiated by executing an 8-bit command, 60H or C7H. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait TCE for the completion of the internal self-timed Chip Erase cycle (see Figure 5-11).

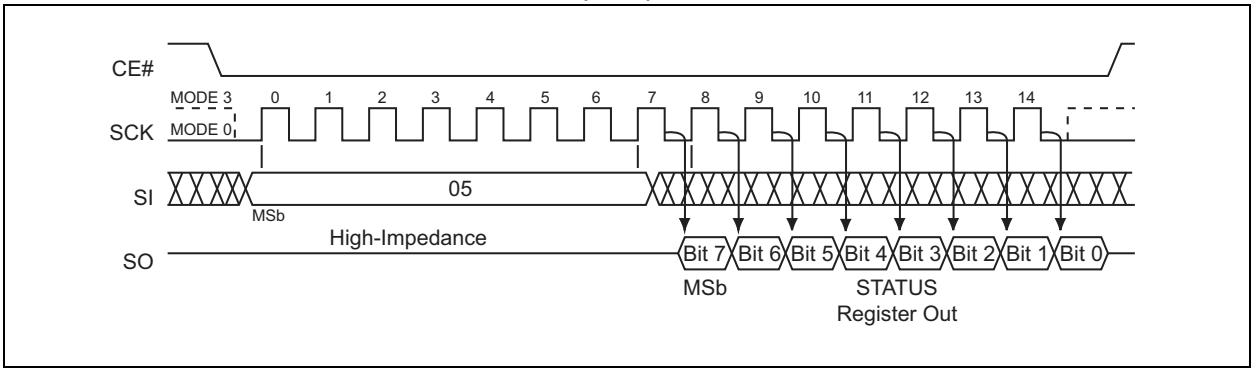
FIGURE 5-11: CHIP-ERASE SEQUENCE



5.10 Read STATUS Register (RDSR)

The Read STATUS Register (RDSR) instruction allows reading of the STATUS register. The STATUS register may be read at any time even during a write (program/erase) operation. When a write operation is in progress, the BUSY bit may be checked before sending any new commands to assure that the new commands are properly received by the device. CE# must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read STATUS Register is continuous with ongoing clock cycles until it is terminated by a low-to-high transition of the CE# (see Figure 5-12).

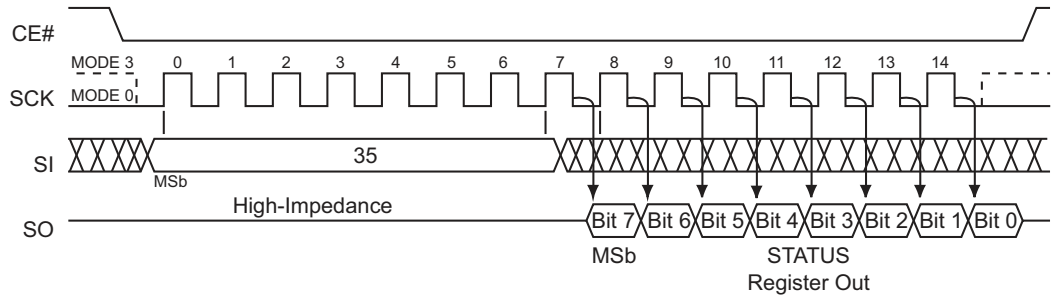
FIGURE 5-12: READ STATUS REGISTER (RDSR) SEQUENCE



5.11 Read STATUS Register (RDSR1)

The Read STATUS Register 1 (RDSR1) instruction allows reading of the STATUS register 1. CE# must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read STATUS Register 1 is continuous with ongoing clock cycles until it is terminated by a low-to-high transition of the CE# (see Figure 5-13).

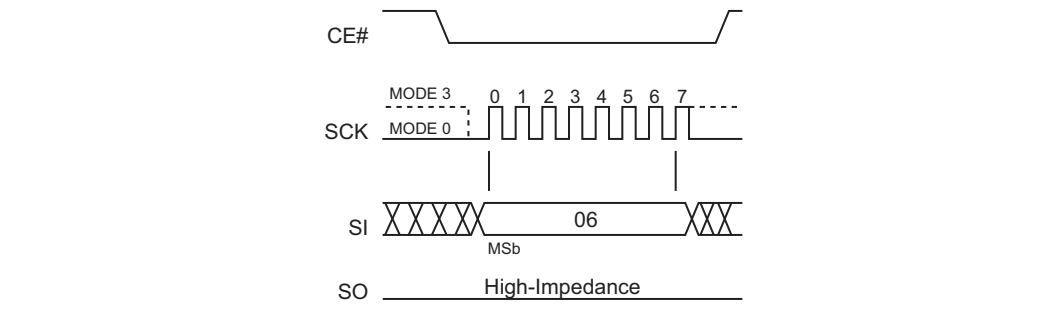
FIGURE 5-13: READ STATUS REGISTER 1 (RDSR1) SEQUENCE



5.12 Write Enable (WREN)

The Write Enable (WREN) instruction sets the Write Enable Latch bit in the STATUS register to 1 allowing write operations to occur. The WREN instruction must be executed prior to any write (program/erase) operation. The WREN instruction may also be used to allow execution of the Write STATUS Register (WRSR) instruction; however, the Write Enable Latch bit in the STATUS register will be cleared upon the rising edge CE# of the WRSR instruction. CE# must be driven high before the WREN instruction is executed.

FIGURE 5-14: WRITE ENABLE (WREN) SEQUENCE

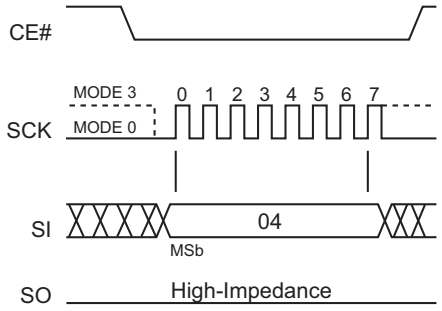


5.13 Write Disable (WRDI)

The Write Disable (WRDI) instruction resets the Write Enable Latch bit and AAI bit to '0' disabling any new write operations from occurring. The WRDI instruction will not terminate any programming operation in progress.

Any program operation in progress may continue up to TBP after executing the WRDI instruction. CE# must be driven high before the WRDI instruction is executed.

FIGURE 5-15: WRITE DISABLE (WRDI) SEQUENCE



5.14 Enable Write STATUS Register (EWSR)

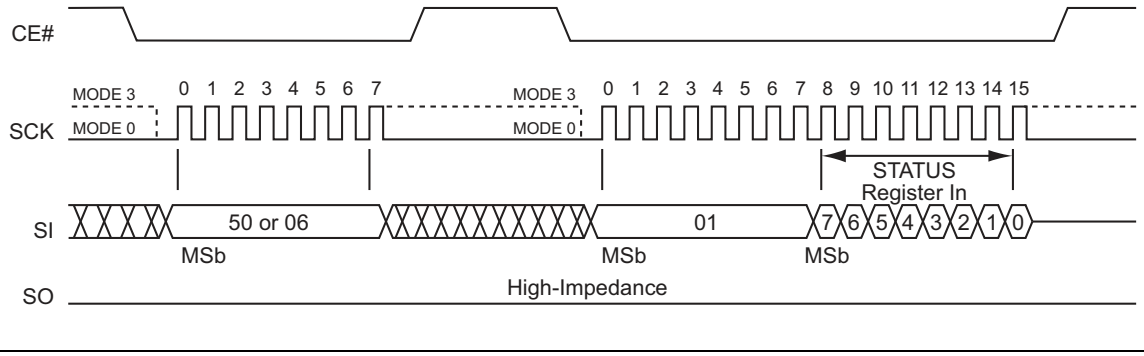
The Enable Write STATUS Register (EWSR) instruction arms the Write STATUS Register (WRSR) instruction and opens the STATUS register for alteration. The Write STATUS Register instruction must be executed immediately after the execution of the Enable Write STATUS Register instruction. This two-step instruction sequence of the EWSR instruction followed by the WRSR instruction works like Software Data Protection (SDP) command structure which prevents any accidental alteration of the STATUS register values. CE# must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.

Executing the Write STATUS Register instruction will be ignored when WP# is low and BPL bit is set to '1'. When the WP# is low, the BPL bit can only be set from '0' to '1' to lock down the STATUS register, but cannot be reset from '1' to '0'. When WP# is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, and BP1 bits in the STATUS register can all be changed. As long as BPL bit is set to '0' or WP# pin is driven high (V_{IH}) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the bits in the STATUS register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to '1' to lock down the STATUS register as well as altering the BP0, BP1, and BP2 bits at the same time. See Table 4-1 for a summary description of WP# and BPL functions.

5.15 Write STATUS Register (WRSR)

The Write STATUS Register instruction writes new values to the BP1, BP0, and BPL bits of the STATUS register. CE# must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 5-16 for EWSR or WREN and WRSR for byte data input sequences.

FIGURE 5-16: ENABLE WRITE STATUS REGISTER (EWSR) OR WRITE ENABLE (WREN) AND WRITE STATUS REGISTER (WRSR) BYTE DATA INPUT SEQUENCE

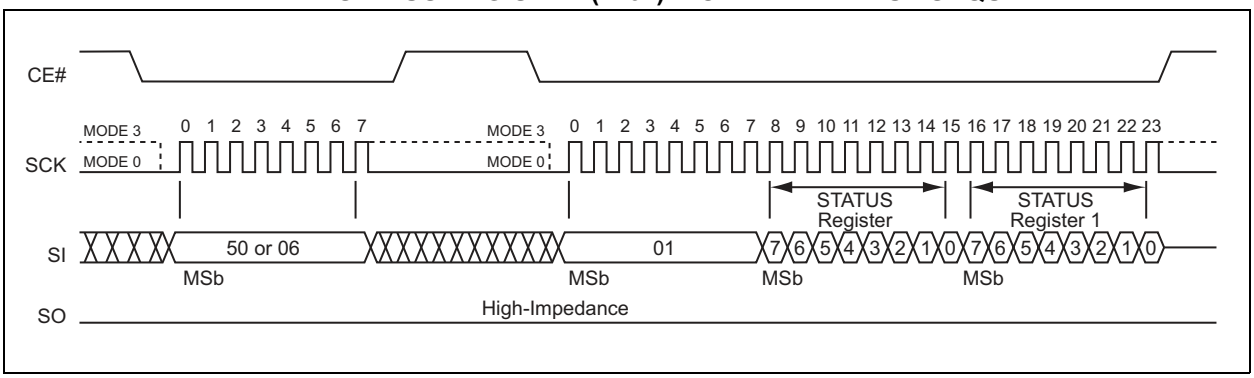


The Write STATUS Register instruction also writes new values to the STATUS Register 1. To write values to STATUS Register 1, the WRSR sequence needs a word data input – the first byte being the STATUS register bits, followed by the second byte STATUS Register 1 bits. CE# must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 5-17 for EWSR or WREN and WRSR instruction word data input sequences.

Executing the Write STATUS Register instruction will be ignored when WP# is low and BPL bit is set to '1'.

When the WP# is low, the BPL bit can only be set from '0' to '1' to lock down the status registers, but cannot be reset from '1' to '0'. When WP# is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, BP1, TSP, and BSP bits in the STATUS register can all be changed. As long as BPL bit is set to '0' or WP# pin is driven high (V_{IH}) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the bits in the STATUS register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to '1' to lock down the STATUS register as well as altering the BPL, BP0, BP1, TSP and BSP bits at the same time. See Table 4-1 for a summary description of WP# and BPL functions.

FIGURE 5-17: ENABLE WRITE STATUS REGISTER (EWSR) OR WRITE ENABLE (WREN) AND WRITE STATUS REGISTER (WRSR) WORD DATA INPUT SEQUENCE



The WRSR instruction can either execute a byte data or a word data input. Extra data/clock input or within byte data/word data input will not be executed. The reason for the byte support is for backward compatibility to products where WRSR instruction sequence is followed by only a byte data.

5.16 JEDEC Read ID

The JEDEC Read ID instruction identifies the device as SST25PF020B and the manufacturer as SST. The device information can be read from executing the 8-bit command, 9FH.

Following the JEDEC Read ID instruction, the 8-bit manufacturer's ID, BFH, is output from the device. After that, a 16-bit device ID is shifted out on the SO pin. Byte 1, BFH, identifies the manufacturer as SST. Byte 2, 25H, identifies the memory type as SPI Serial Flash. Byte 3, 8CH, identifies the device as SST25PF020B. The instruction sequence is shown in Figure 5-18. The JEDEC Read ID instruction is terminated by a low-to-high transition on CE# at any time during data output.

FIGURE 5-18: JEDEC READ ID SEQUENCE

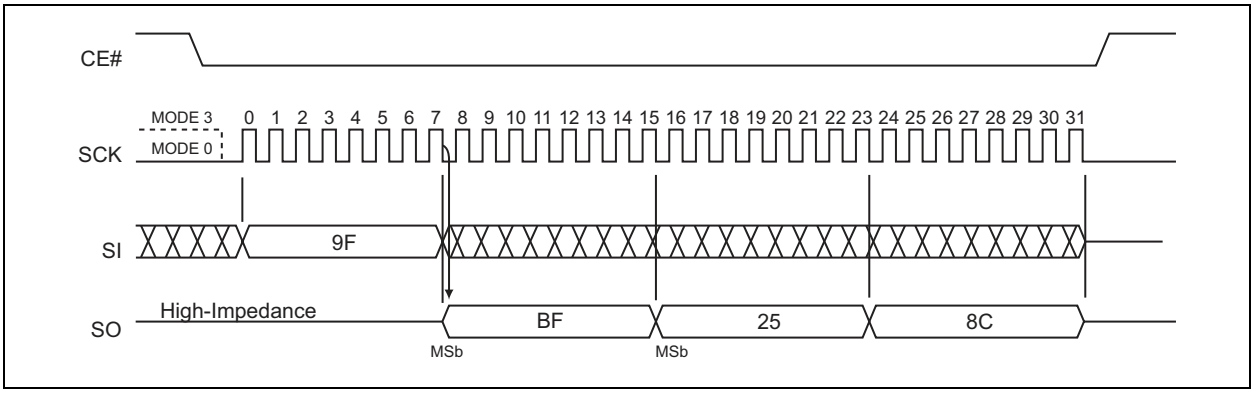


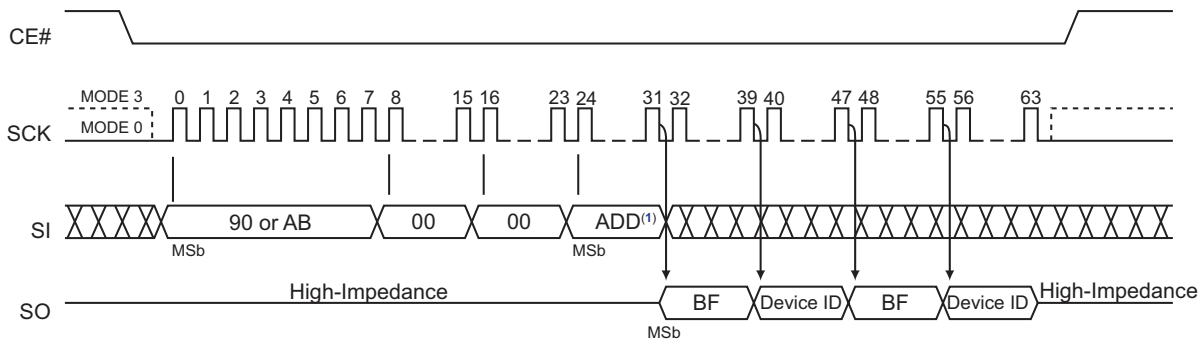
TABLE 5-2: JEDEC READ ID DATA

Manufacturer's ID	Device ID	
	Memory Type	Memory Capacity
Byte 1	Byte 2	Byte 3
BFH	25H	8CH

5.17 Read ID (RDID)

The Read ID (RDID) instruction identifies the devices as SST25PF020B and manufacturer as SST. The device information can be read from executing an 8-bit command, 90H or ABH, followed by address bits [A_{23}-A_0]. Following the Read ID instruction, the manufacturer's ID is located in address 00000H and the device ID is located in address 00001H. Once the device is in Read ID mode, the manufacturer's and device ID output data toggles between address 00000H and 00001H until terminated by a low-to-high transition on CE#. Refer to Tables 5-2 and 5-3 for device identification data.

FIGURE 5-19: READ ID SEQUENCE



Note: 1. 00H will output the manfacturer's ID first and 01H will output device ID first before toggling between the two.
2. The manufacturer's and device ID output stream is continuous until terminated by a low-to-high transition on CE#.
Device ID = 8CH for SST25VF020B

TABLE 5-3: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	00000H	BFH
Device ID	00001H	8CH

6.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

DC voltage on any pin to ground potential ..... -0.5V to V_{DD}+0.5V

Transient voltage (<20 ns) on any pin to ground potential ..... -2.0V to V_{DD}+2.0V

Package power dissipation capability (T_A = 25°C) 1.0W

Surface mount solder reflow temperature ..... 260°C for 10 seconds

Output short circuit current[1] ..... 50 mA

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 6-1: OPERATING RANGE

Range	Ambient Temp.	V_{DD}
Commercial	0°C to +70°C	2.3V-3.6V

TABLE 6-2: AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	Output Load
5 ns	C_L = 30 pF

Note 1: See Figures 6-6 and 6-7.

TABLE 6-3: DC CHARACTERISTICS

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{DDR}	Read Current	—	12	mA	CE# = 0.1 V_{DD}/0.9 V_{DD}@33 MHz, SO = Open
I_{DDR3}	Read Current	—	20	mA	CE# = 0.1 V_{DD}/0.9 V_{DD}@80 MHz, SO = Open
I_{DDW}	Program and Erase Current	—	30	mA	CE# = V_{DD}
I_{SB}	Standby Current	—	30	µA	CE# =V_{DD}, V_{IN} = V_{DD} or V_{SS}
I_{LI}	Input Leakage Current	—	1	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{LO}	Output Leakage Current	—	1	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} Max
V_{IL}	Input Low Voltage	—	0.7	V	V_{DD} = V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}	—	V	V_{DD} = V_{DD} Max
V_{OL}	Output Low Voltage	—	0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min
V_{OL2}	Output Low Voltage	—	0.4	V	I_{OL} = 1.6 mA, V_{DD} = V_{DD} Min
I_{OH}	Output High Voltage	V_{DD}-0.2	—	V	I_{OH} = -100 µA, V_{DD} = V_{DD} Min

TABLE 6-4: CAPACITANCE (T_A = 25°C, F = 1 MHZ, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-5: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Unit	Test Method
N_{END}(1)	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-6: AC OPERATING CHARACTERISTICS, 2.3V-2.7V

Symbol	Parameter	25 MHz		50 MHz		Units
		Min.	Max.	Min.	Max.	
F_{CLK}	Serial Clock Frequency(1)	—	25	—	50	MHz
T_{SCKH}	Serial Clock High Time	18	—	9	—	ns
T_{SCKL}	Serial Clock Low Time	18	—	9	—	ns
T_{SCKR}	Serial Clock Rise Time (slew rate)(2)	0.1	—	0.1	—	V/ns
T_{SCKF}	Serial Clock Fall Time (slew rate)	0.1	—	0.1	—	V/ns
T_{CES}	CE# Active Setup Time(3)	5	—	5	—	ns
T_{CEH}	CE# Active Hold Time(3)	5	—	5	—	ns
T_{CHS}	CE# Not Active Setup Time(3)	5	—	5	—	ns
T_{CHH}	CE# Not Active Hold Time(3)	5	—	5	—	ns
T_{CPH}	CE# High Time	50	—	50	—	ns
T_{CHZ}	CE# High-to-High Z Output	—	7	—	7	ns
T_{CLZ}	SCK Low-to-Low Z Output	0	—	0	—	ns
T_{DS}	Data In Setup Time	2	—	2	—	ns
T_{DH}	Data In Hold Time	4	—	4	—	ns
T_{HLS}	HOLD# Low Setup Time	5	—	5	—	ns
T_{HHS}	HOLD# High Setup Time	5	—	5	—	ns
T_{HLH}	HOLD# Low Hold Time	5	—	5	—	ns
T_{HHH}	HOLD# High Hold Time	5	—	5	—	ns
T_{HZ}	HOLD# Low-to-High Z Output	—	7	—	7	ns
T_{LZ}	HOLD# High-to-Low Z Output	—	7	—	7	ns
T_{OH}	Output Hold from SCK Change	0	—	0	—	ns
T_{V}	Output Valid from SCK	—	12	—	8	ns
T_{SE}	Sector Erase	—	25	—	25	ms
T_{BE}	Block Erase	—	25	—	25	ms
T_{SCE}	Chip Erase	—	50	—	50	ms
T_{BP}	Byte Program	—	10	—	10	µs

Note 1: Maximum clock frequency for Read instruction, 03H, is 25 MHz.

2: Maximum Rise and Fall time may be limited by T_{SCKH} and T_{SCKL} requirements.

3: Relative to SCK.

TABLE 6-7: AC OPERATING CHARACTERISTICS, 2.7V-3.6V

Symbol	Parameter	33 MHz		80 MHz		Units
		Min.	Max.	Min.	Max.	
FCLK	Serial Clock Frequency(1)	—	33	—	80	MHz
TSCKH	Serial Clock High Time	13	—	6	—	ns
TSCKL	Serial Clock Low Time	13	—	6	—	ns
TSCKR	Serial Clock Rise Time (slew rate)(2)	0.1	—	0.1	—	V/ns
TSCKF	Serial Clock Fall Time (slew rate)	0.1	—	0.1	—	V/ns
TCES	CE# Active Setup Time(3)	5	—	5	—	ns
TCEH	CE# Active Hold Time(3)	5	—	5	—	ns
TCHS	CE# Not Active Setup Time(3)	5	—	5	—	ns
TCHH	CE# Not Active Hold Time(3)	5	—	5	—	ns
TCPH	CE# High Time	50	—	50	—	ns
TCHZ	CE# High-to-High Z Output	—	15	—	7	ns
TCLZ	SCK Low-to-Low Z Output	0	—	0	—	ns
TDS	Data In Setup Time	2	—	2	—	ns
TDH	Data In Hold Time	4	—	4	—	ns
THLS	HOLD# Low Setup Time	5	—	5	—	ns
THHS	HOLD# High Setup Time	5	—	5	—	ns
THLH	HOLD# Low Hold Time	5	—	5	—	ns
THHH	HOLD# High Hold Time	5	—	5	—	ns
THZ	HOLD# Low-to-High Z Output	—	7	—	7	ns
TLZ	HOLD# High-to-Low Z Output	—	7	—	7	ns
TOH	Output Hold from SCK Change	0	—	0	—	ns
TV	Output Valid from SCK	—	10	—	6	ns
TSE	Sector Erase	—	25	—	25	ms
TBE	Block Erase	—	25	—	25	ms
TSCE	Chip Erase	—	50	—	50	ms
TBP	Byte Program	—	10	—	10	µs

Note 1: Maximum clock frequency for Read instruction, 03H, is 33 MHz.

2: Maximum Rise and Fall time may be limited by TSCKH and TSCKL requirements.

3: Relative to SCK.

FIGURE 6-1: SERIAL INPUT TIMING DIAGRAM

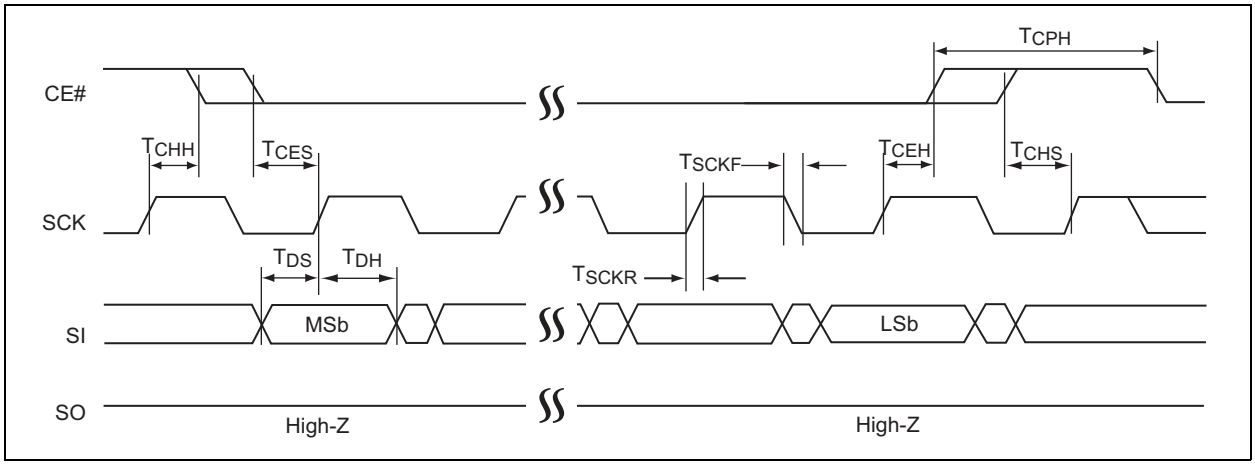


FIGURE 6-2: SERIAL OUTPUT TIMING DIAGRAM

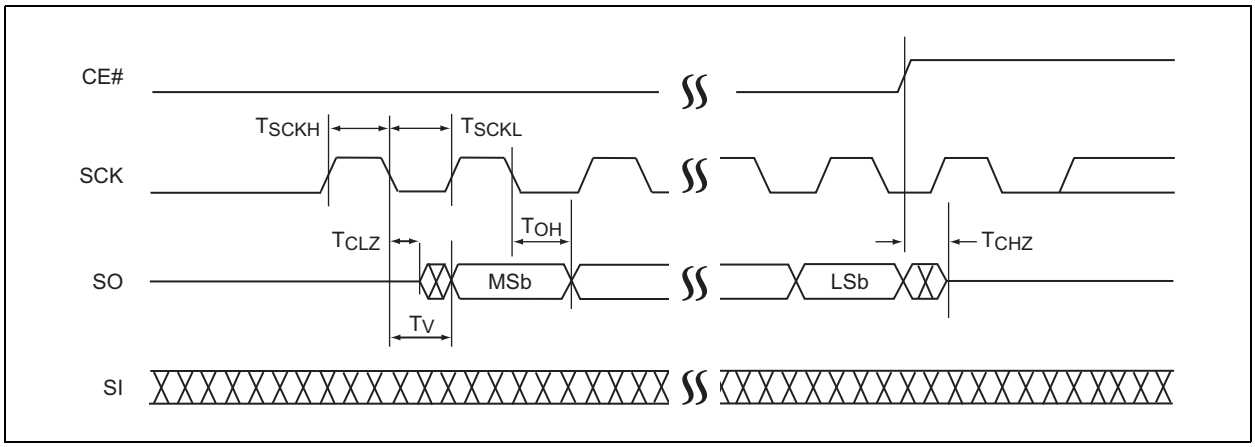
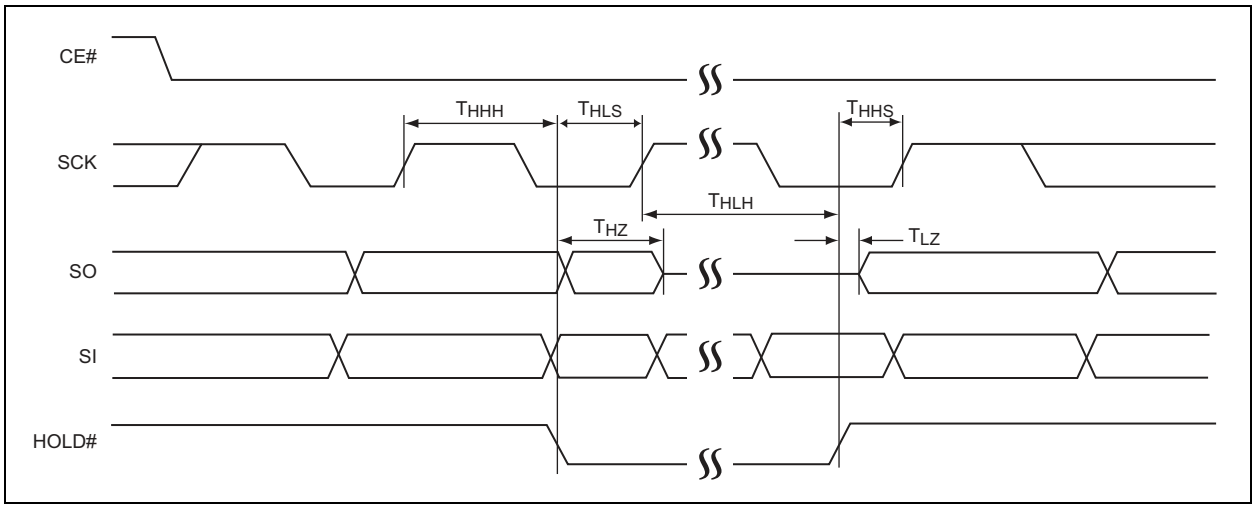


FIGURE 6-3: HOLD TIMING DIAGRAM



6.1 Power-Up Specifications

All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3.0V in less than 300 ms). See Table 6-8 and Figure 6-4 for more information.

TABLE 6-8: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$(1)	V_{DD} Minimum to Read Operation	100	µs
$T_{PU-WRITE}$(1)	V_{DD} Minimum to Write Operation	100	µs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 6-4: POWER-UP TIMING DIAGRAM

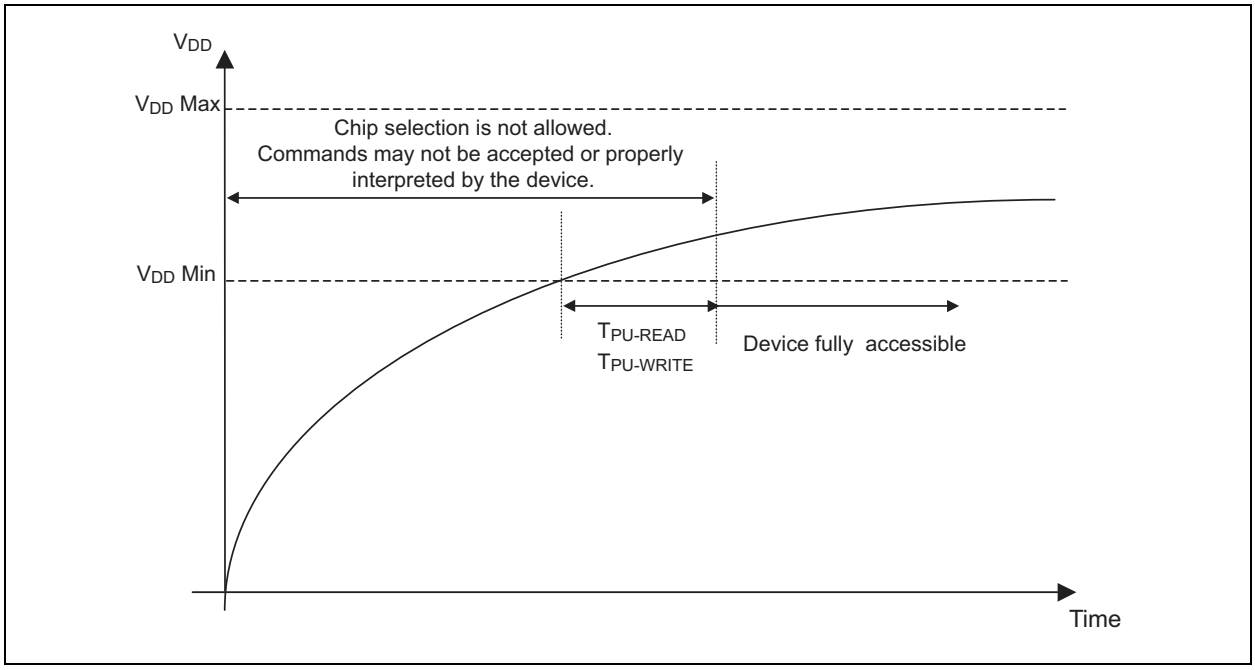


TABLE 6-9: RECOMMENDED POWER-UP/POWER-DOWN LIMITS

Symbol	Parameter	Limits		Units	Condition
		Minimum	Maximum		
T_{PF}	V_{DD} Falling Time	1	100	ms/V	
T_{PR}	V_{DD} Rising Time	0.033	100	ms/V	
T_{OFF}	V_{DD} Off Time	100	—	ms	
V_{OFF}	V_{DD} Off Level	—	0.3	V	0V recommended

FIGURE 6-5: RECOMMENDED POWER-UP/POWER-DOWN WAVEFORM

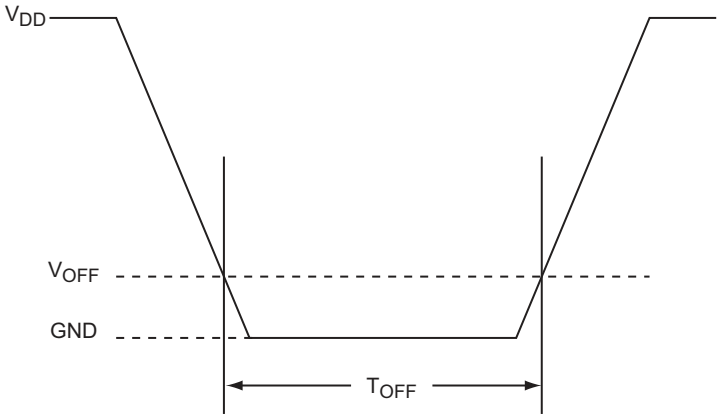
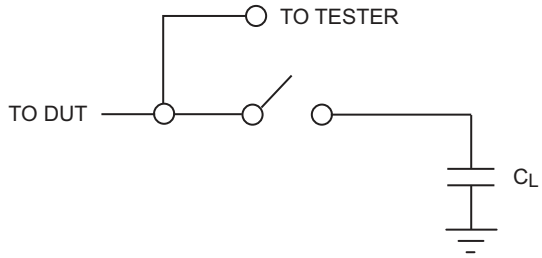


FIGURE 6-6: AC INPUT/OUTPUT REFERENCE WAVEFORMS

AC test inputs are driven at VIHT (0.9VDD) for a logic '1' and VILT (0.1VDD) for a logic '0'. Measurement reference points for inputs and outputs are VHT (0.6VDD) and VLT (0.4VDD). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: VHT - VHIGH Test
VLT - VLOW Test
VIHT - VINPUT HIGH Test
VILT - VINPUT LOW Test

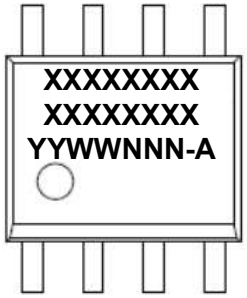
FIGURE 6-7: TEST LOAD EXAMPLE



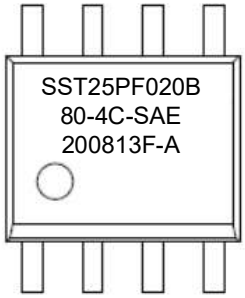
7.0 PACKAGING INFORMATION

7.1 Package Marking

8-Lead SOIC (3.90 mm)

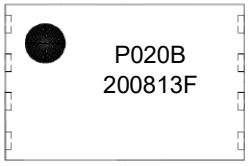


Example

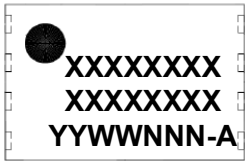


8-Contact USON

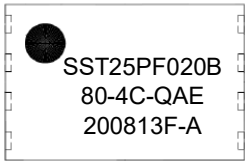
Example



8-Contact WSON



Example



Part Number	1st Line Marking Codes		
	SOIC	USON	WSON
SST25PF020B	SST25PF020B	P020B	SST25PF020B

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)

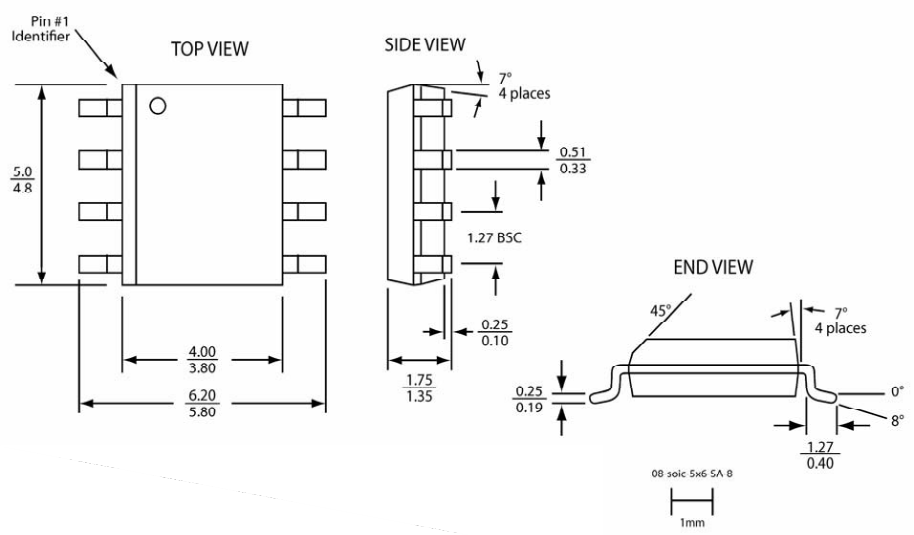
Note: For very small packages with no room for the Pb-free JEDEC® designator (e3) , the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

7.2 Packaging Diagrams

8-Lead Small Outline Integrated Circuit (SAE/F) - 5x6 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

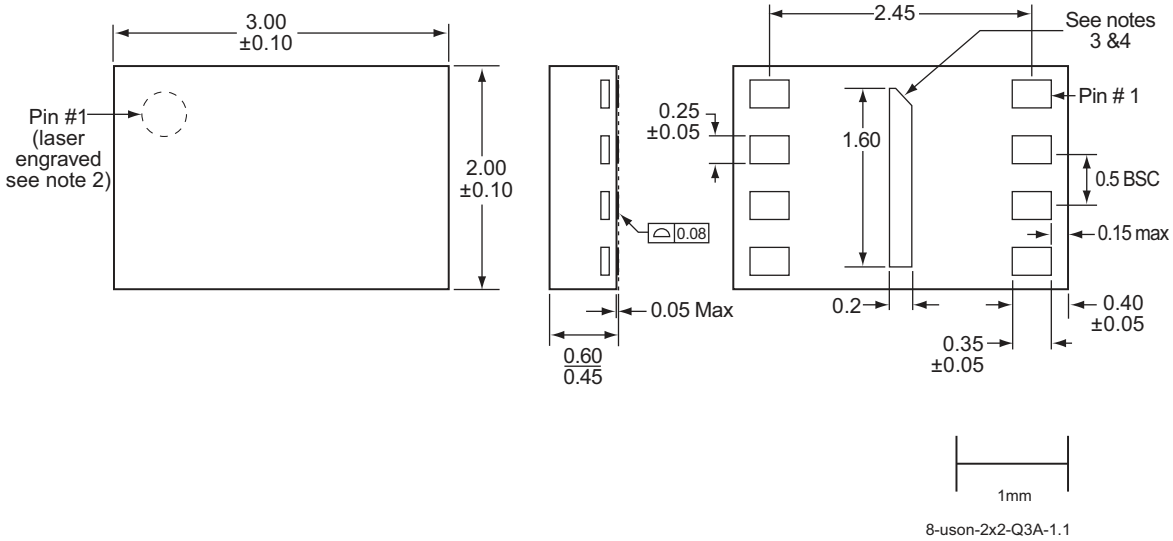


Note:

1. Complies with JEDEC publication 95 MS-012 AA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends and 0.25 mm between leads.

Microchip Technology Drawing C04-14003A Sheet 1 of 1

8-Contact Ultra-Thin Small Outline No-Lead (USON) Package Code: Q3A

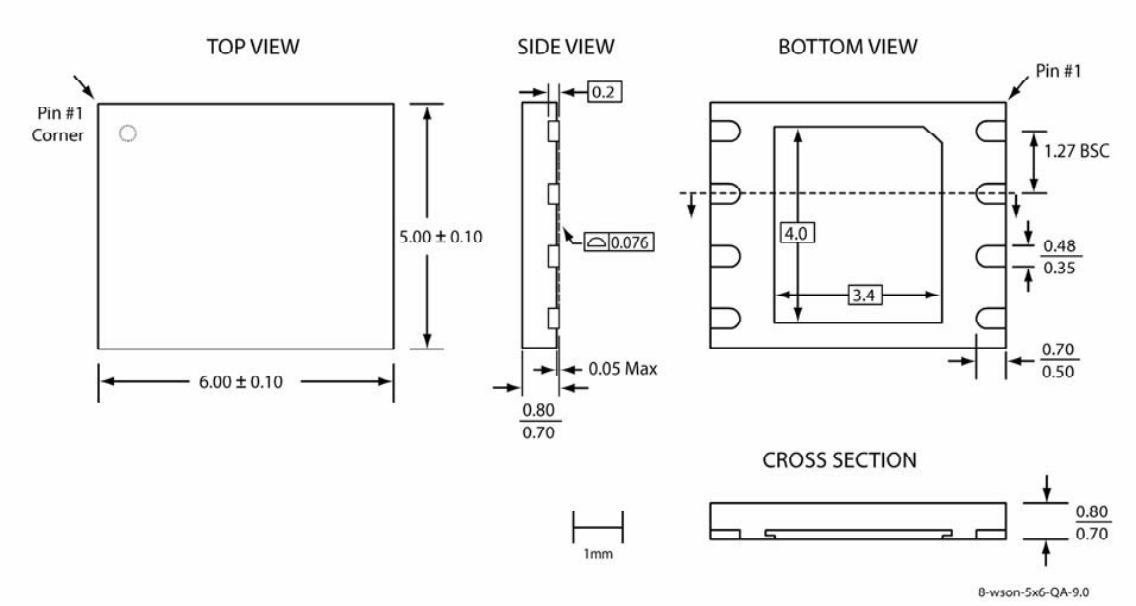


Note: 1. Similar to JEDEC JEP95 MO-252 variant U2030D, though number of contacts and some dimensions may be different.
2. The topside pin #1 indicator is laser engraved; its approximate shape and location is as shown.
3. From the bottom view, the pin #1 indicator may be either a curved indent or a 45-degree chamfer.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).
6. Lead-frame nominal thickness 0.127mm or 0.15mm (supplier-dependent).

Note 1: For the most current package drawings, please see the Microchip Packaging Specification located at http;//www.microchip.com/packaging.

8-Lead Very, Very Thin Small Outline No-Leads (QAE/F) - 5x6 mm Body [WSON]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Note:

1. All linear dimensions are in millimeters (max/min).
2. Untoleranced dimensions (shown with box surround) are nominal target dimensions.
3. The external paddle is electrically connected to the die back-side and possibly to certain VSS leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.

Microchip Technology Drawing C04-14008A Sheet 1 of 1

APPENDIX A: REVISION HISTORY

Revision C (March 2020)

Updated standby current; Updated formatting to current template; Added package marking section.

Revision B (May 2013)

Updated “Product Identification System”.

Revision A (November 2012)

Removed duplicate Power-up table; Updated Endurance information; Released document under new letter revision; Updated Spec number from S71417 to DS25054.

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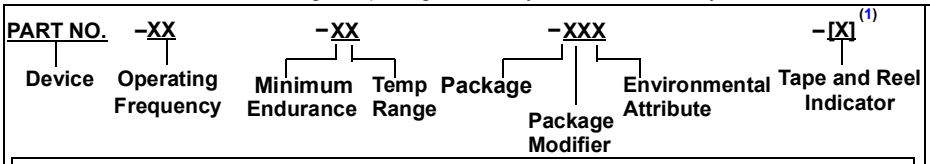

Device:	SST25PF020B	= 2 Mbit, 2.3V-3.6V, SPI Serial Flash
Operating Frequency:	80	= 80 MHz
Minimum Endurance:	4	= 10,000 cycles
Temperature Range:	C	= 0°C to +70°C (Commercial)
Package:	S Q3 Q	= SOIC (150 mil Body), 8-lead = USON (3 mm x 2 mm Body), 8-contact = WSON (6 mm x 5 mm Body), 8-contact
Package Modifier:	A	= 8 leads or contacts
Environmental Attribute:	E	= RoHS compliant
Tape and Reel Indicator:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)

Valid Combinations:

a) SST25PF020B-80-4C-SAE
b) SST25PF020B-80-4C-SAE-T

c) SST25PF020B-80-4C-Q3AE
d) SST25PF020B-80-4C-Q3AE-T

e) SST25PF020B-80-4C-QAE
f) SST25PF020B-80-4C-QAE-T

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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