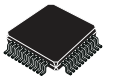
ST7538

FSK POWER LINE TRANSCEIVER

1 FEATURES

- HALF DUPLEX FREQUENCY SHIFT KEYING (FSK) TRANSCEIVER
- INTEGRATED POWER LINE DRIVER WITH PROGRAMMABLE VOLTAGE AND CURRENT CONTROL
- PROGRAMMABLE INTERFACE:
  – SYNCHRONOUS
  – ASYNCHRONOUS
- SINGLE SUPPLY VOLTAGE (FROM 7.5 UP TO 12.5V)
- VERY LOW POWER CONSUMPTION (Iq=5 mA)
- INTEGRATED 5V VOLTAGE REGULATOR (UP TO 100mA) WITH SHORT CIRCUIT PROTECTION
- 8 PROGRAMMABLE TRANSMISSION FREQUENCIES
- PROGRAMMABLE BAUD RATE UP TO 4800BPS
- RECEIVING SENSITIVITY 250µVRMS
- SUITABLE TO APPLICATION IN ACCORDANCE WITH EN 50065 CENELEC SPECIFICATIONS
- CARRIER OR PREAMBLE DETECTION
- BAND IN USE DETECTION
- PROGRAMMABLE REGISTER WITH SECURITY CHECKSUM
- MAINS ZERO CROSSING DETECTION AND SYNCHRONIZATION

Figure 1. Package



TQFP44 Slug Down

Table 1. Order Codes

Part Number	Package
ST7538P	TQFP44 (Slug down)

- WATCHDOG TIMER

2 DESCRIPTION

The ST7538 is a Half Duplex synchronous/asynchronous FSK Modem designed for power line communication network applications. It operates from a single supply voltage and integrates a line driver and a 5V linear regulator. The device operation is controlled by means of an internal register, programmable through the synchronous serial interface. Additional functions as watchdog, clock output, output voltage and current control, preamble detection, time-out, band in use are included. Realized in Multipower BCD5 technology that allows to integrate DMOS, Bipolar and CMOS structures in the same chip.

Figure 2. Block Diagram

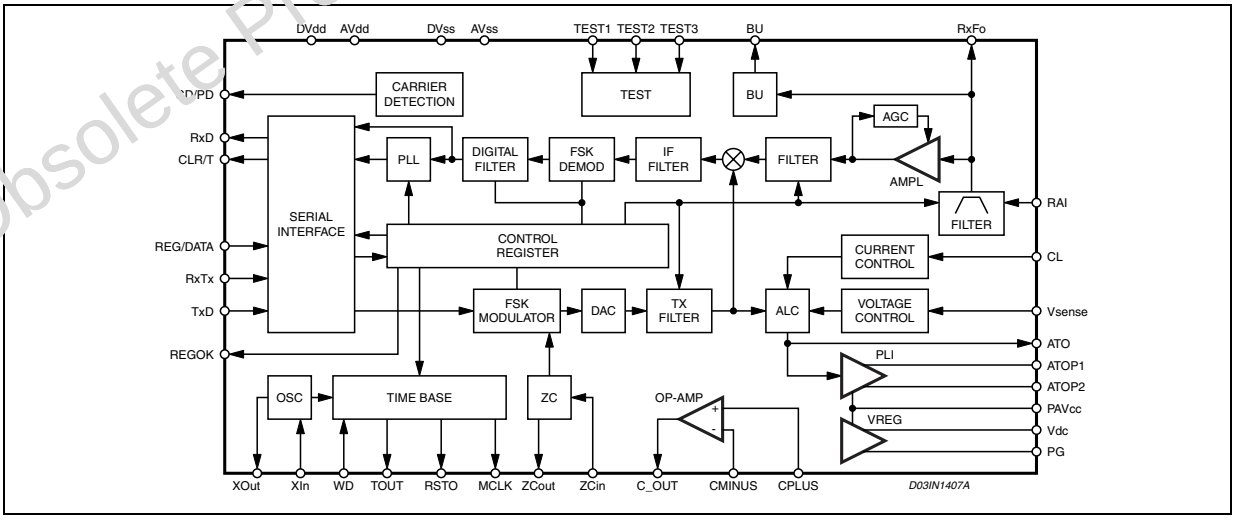


Figure 3. Pin Connection (Top view)

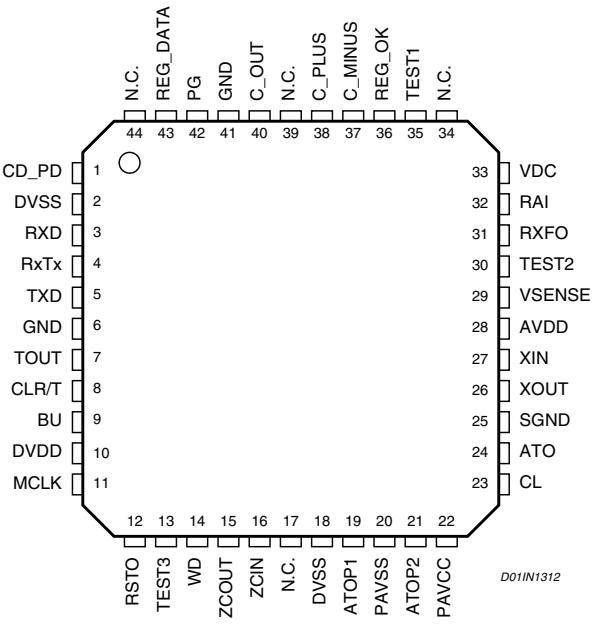


Table 2. Pin Description

N°	Name	Type	Description
1	CD_PD	Digital/Output	Carrier or Preamble Detect Output. "1" No Carrier or Preamble Detected "0" Carrier or Preamble Detected
2	DVss	Supply	Digital Ground
3	RxD	Digital/Output	RX Data Output.
4	RxTx	Digital/Input with internal pull-up	Rx or Tx mode selection input. "1" - RX Session "0" - TX Session
5	TxD	Digital/Input with internal pull-down	TX Data Input.
6	GND	Supply	Substrate Ground (same function as PIN 41)
7	TOUT	Digital/Output	TX Time Out Event Detection "1" - Time Out Event Occurred "0" - No Time-out Event Occurred
8	CLR/T	Digital/Output	Synchronous Mains Access Clock or Control Register Access Clock
9	BU	Digital/Output	Band in use Output. "1" Signal within the Programmed Band "0" No Signal within the Programmed Band
10	DVdd	Supply	Digital Supply Voltage
11	MCLK	Digital/Output	Master Clock Output
12	RSTO	Digital/Output	Power On or Watchdog Reset Output

Table 2. Pin Description (continued)

N°	Name	Type	Description
13	TEST 3	Digital/Input with internal pull-down	Test Input. Must be connected to DVss during Normal Operation
14	WD	Digital/Input with internal pull-up	Watchdog input. The Internal Watchdog Counter is cleared on the falling edges.
15	ZCOUT	Digital/Output	Zero Crossing Detection Output
16	ZCIN[1]	Analog/Input	Zero Crossing AC Input.
17	NC	Floating	Must be connected to DVss.
18	DVss	Supply	Digital Ground
19	ATOP1	Power/Output	Power Line Driver Output
20	PAVss	Supply	Power Analog Ground
21	ATOP2	Power/Output	Power Line Driver Output
22	PAV_{CC}	Supply	Power Supply Voltage
23	CL[2]	Analog/Input	Current Limiting Feedback. A resistor between CL and AVss sets the PLI Current Limiting Value
24	ATO	Analog/Output	Small Signal Analog Transmit Output
25	SGND	Supply	Analog Signal Ground
26	XOUT	Analog I/O	Crystal Output- External Clock Input
27	XIN	Analog Input	Crystal Oscillator Input
28	AVdd	Supply	Analog Power supply.
29	Vsense[3]	Analog/Input	Output Voltage Sensing input for the voltage control loop
30	TEST2	Analog/Input	Test Input must be connected SGND
31	RxFO	Analog/Output	Receiving Filter Output
32	RAI	Analog/Input	Receiving Analog Input
33	VDC	Power	5V Voltage Regulator Output
34	NC	floating	Must Be connected to DVss.
35	TEST1	Digital/Input with internal pull-down	Test input. Must Be connected to DVss.
36	REGOK	Digital/Output	Security checksum logic output "1" - Stored data Corrupted "0" - Stored data OK
37	C_MINUS[4]	Analog/Input	Op-amp Inverting Input.
38	C_PLUS[5]	Analog/Input	Op-amp Not Inverting Input.
39	NC	floating	Must Be connected to DVss
40	C_OUT	Analog/Output	Op-amp Output
41	GND	Supply	Substrate Ground (same function as PIN 6)
42	PG	Digital/Output	Power Good logic Output "1" - VDC is above 4.5V "0" - VDC is below 4.25V
43	REG_DATA	Digital/Input with internal pull-down	Mains or Control Register Access Selector "1" - Control Register Access "0" - Mains Access
44	NC	floating	Must be connected to DVss.

<1> If not used this pin must be connected to VDC
<2> Cannot be left floating
<3> Cannot be left floating
<4> If not used this pin must be connected to VDC
<5> If not used this pin must be tied low (SGND or PAVss or DVss)

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
PAV_{CC}	Power Supply Voltage	-0.3 to +14	V
AV_{dd}	Analog Supply Voltage	-0.3 to +5.5	V
DV_{dd}	Digital Supply Voltage	-0.3 to +5.5	V
AV_{ss}/DV_{ss}	Voltage between AV_{ss} and DV_{ss}	-0.3 to +0.3	V
V_I	Digital input Voltage	DV_{ss} - 0.3 to DV_{dd} +0.3	V
V_O	Digital output Voltage	DV_{ss} - 0.3 to DV_{dd} +0.3	V
I_O	Digital Output Current	-2 to +2	mA
V_{sense}, XIN, C_MINUS, C_PLUS, CL	Voltage Range at Vsense, XIN, C_MINUS, C_PLUS, CL Inputs	AV_{ss} - 0.3 to AV_{dd}+0.3	V
RAI, ZCIN	Voltage Range at RAI, ZCIN Inputs	$-AV_{dd}$ - 0.3 to AV_{dd} +0.3	V
ATO, RxFO, C_OUT, XOUT	Voltage range at ATO, RxFO, C_OUT, XOUT Outputs	AV_{ss} - 0.3 to AV_{dd} +0.3	V
ATOP1,2	Voltage range at Powered ATO Output	AV_{ss} - 0.3 to $+PAV_{cc}$ +0.3	V
ATOP	Powered ATO Output Current (*)	400	mArms
T_{amb}	Operating ambient Temperature	-40 to +85	°C
T_{stg}	Storage Temperature	-50 to 150	°C
ATOP1 Pin	Maximum Withstanding Voltage Range Test Condition: CDF-AEC-Q100-002- “Human Body Model” Acceptance Criteria: “Normal Performance”	±1500	V
ATOP2 Pin		±1000	V
Other pins		±2000	V

(*) This current is intended as not repetitive pulse current

Table 4. Thermal Data

Symbol	Parameter	TQFP44 with slug	Unit
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient Steady State(*)	35	°C/W
$R_{th\text{-}j\text{-}amb2}$	Maximum Thermal Resistance Junction-Ambient Steady State(**)	50	°C/W

(*) Mounted on Multilayer PCB with a dissipating surface on the bottom side of the PCB
(**) It's the same condition of the point above, without any heatsinking surface on the board.

Table 5. Electrical Characteristcs

(AVcc = DVcc = +5V, PAVcc =+9 V, PAVss, SGND = DVss = 0V,-40°C ≤ Tamb ≤ 85°C, Fc = 86kHz, other Control Register parameters as default value, unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
AV_{CC}, DV_{CC}	Supply Voltages		4.75	5	5.25	V
PAV_{CC} - DV_{CC}	PAV_{CC} and DV_{CC} Relation during Power-Up Sequence	DV_{CC} < 4.75V	0.1		1.2	V
PAV_{CC} - AV_{CC}	PAV_{CC} and DV_{CC} Relation during Power-Up Sequence	AV_{CC} < 4.75V	0.1		1.2	V
PAV_{cc}	Power Supply Voltage		7.5		12.5	V
	Max allowed slope during Power-Up				100	V/ms
AI_{CC} + DI_{CC}	Input Supply Current	Transmission & Receiving mode		5	7	mA
I PAV_{CC}	Powered Analog Supply Current	TX mode (no load)		30	50	mArms
		RX mode		0.5	1	mA
		Maximum total current			370	mArms
Digital I/O						
V_{IH}	High Logic Level Input Voltage		2			V
V_{IL}	Low Logic Level input Voltage				0.8	V
V_{OH}	High Logic Level Output Voltage	I_{OH}= -2mA	3.5			V
V_{OL}	Low Logic Level Output Voltage	I_{OL}= 2mA			0.4	V
R_{down}	Pull Down Resistor			100		kΩ
R_{up}	Pull up Resistor			100		kΩ
Oscillator						
$XOUT_{SWING}$	XOUT Input Voltage Swing	External Clock (see par. 3.8)	1		3	V
$XOUT_{OFFSET}$	XOUT Input Voltage Offset		1.5		2.5	V
DC	XTAL Clock Duty Cycle	External Clock	40		60	%
Xtal	Crystal Oscillator frequency			16		MHz
$Xtal_{ESR}$	External Oscillator Esr Resistance				40	Ω
$Xtal_{CL}$	External Oscillator Stabilization Capacitance				16	pF
Transmitter						
IATO	Output Transmitting Current on ATO				1	mArms
V_{ATO}	Max Carrier Output AC Voltage	R_{CL} = 1.75kΩ $V_{sense\ (AC)}$ = 0V	1.75	2.3	3.5	V_{PP}
V_{ATODC}	Output DC Voltage on ATO		1.7	2.1	2.5	V
$HD2_{ATO}$	Second Harmonic Distortion on ATO	V_{ATO} = $2V_{PP}$		-55	-42	dB
$HD3_{ATO}$	Third Harmonic Distortion on ATO			-52	-49	dB
IATOP	Output Transmitting Current in programmable current limiting	Vsense connected though a 100pF cap to GND; Rcl=1.85kΩ; R_{LOAD} =1Ω (as in fig. 17)	250	310	370	mArms

Table 5. Electrical Characteristcs (continued)
(AVcc = DVcc = +5V, PAVcc =+9 V, PAVss, SGND = DVss = 0V,-40°C ≤ Tamb ≤ 85°C, Fc = 86kHz, other Control Register parameters as default value, unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{ATOP(AC)}$	Max Carrier Output AC Voltage for each ATOP1 and ATOP2 pins	R_{CL} = 1.75kΩ ; $V_{sense\ (AC)}$ = 0V $PAVcc \geq \frac{VATOP(AC)}{2} + 7.5V$	3.5	4.6	7	V_{pp}
$V_{ATOP(DC)}$	Output DC Voltage on ATOP1 and ATOP2 pins		3.5	4.2	5	V
$HD2_{ATOP}$	Second Harmonic Distortion on each ATOP1 and ATOP2 pins	V_{ATOP} = $4V_{PP}$, PAVCC = 10V No Load		-55	-42	dB
	Differential Second Harmonic Distortion	V_{ATOP} = $4V_{PP}$, PAVCC = 10V R_{LOAD} =50Ω (Differential) Carrier Frequency: 132.5KHz		-65	-53	dB
$HD3_{ATOP}$	Third Harmonic Distortion on each ATOP1 and ATOP2 pins	V_{ATOP} = $4V_{PP}$, PAVCC = 10V No Load.		-56	-49	dB
	Differential Third Harmonic Distortion	V_{ATOP} = $4V_{PP}$, PAVCC = 10V R_{LOAD} =50Ω (Differential) Carrier Frequency: 132.5KHz		-65	-52	dB
VATOP	Accuracy with Voltage Control Loop Active	R_{CL} = 1.75kΩ; $V_{sense\ (AC)}$ = 0V	-1		+1	G_{STEP}
G_{STEP}	ALC Gain Step Control loop gain step		0.6	1	1.4	dB
D_{RNG}	ALC Dynamic Range			30		dB
VCL_{TH}	Voltage control loop reference threshold on V_{sense} pin	Figure 15	160	180	200	mV_{PK}
VCL_{HYST}	Hysteresis on Voltage loop reference threshold	Figure 15		±18		mV
CCL_{TH}	Current control loop reference threshold on C_{sense} pin	Figure 15	1.80	1.90	2.00	V
CCL_{HYST}	Hysteresis on Current loop reference threshold	Figure 15	210	250	290	mV
$V_{SENSE\ (DC)}$	Output DC Voltage on VSENSE			1.865		V
V_{SENSE}	VSENSE Input Impedance			36		KΩ
T_{RxTx}	Carrier Activation Time	Figure 18 - 600 Baud Xtal=16MHz	0.01		1.6	ms
		Figure 18- 1200 Baud Xtal=16MHz	0.01		800	µs
		Figure 18- 2400 Baud Xtal=16MHz	0.01		400	µs
		Figure 18- 4800 Baud Xtal=16MHz	0.01		200	µs
TALC	Carrier Stabilization Time From STEP 16 to zero or From step 16 to step 31,	Figure 18. Xtal =16MHz			3.2	ms
T_{ST}	Tstep	Figure 18 Xtal =16MHz			200	µs
Receiver						
V_{IN}	Input Sensitivity (Normal Mode)			0.5	2	mV_{rms}
	Input Sensitivity (High Sens.)			250		μV_{rms}
V_{IN}	Maximum Input Signal				2	V_{rms}

Table 5. Electrical Characteristcs (continued)
(AVcc = DVcc = +5V, PAVcc =+9 V, PAVss, SGND = DVss = 0V,-40°C ≤ Tamb ≤ 85°C, Fc = 86kHz, other Control Register parameters as default value, unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{IN}	Input Impedance		80	100	140	kΩ
V_{CD}	Carrier Detection Sensitivity (Normal Mode)			0.5	2	mV_{rms}
	Carrier Detection Sensitivity (High Sensitivity Mode)			250		μV_{rms}
V_{BU}	Band in Use Detection Level			77	85	dB/ µVrms
Voltage Regulator						
VDC	Linear Regulator Output Voltage	-25<Tj<125 C 0<$I_{(VDC)}$<100mA	4.9	5.05	5.2	V
		-25<Tj<125 C 0<$I_{(VDC)}$<150mA	4.7		5.2	V
ΔVDC	Line Regulation	7.5V<PAVcc<12.5V $I_{(VDC)}$=10mA		10	50	mV
	Load Regulation	5mA<$I_{(VDC)}$<100mA PAVcc=7.5V		20	75	mV
$I(V_{DC})$	Linear Regulator Current Limitation		150	180	210	mA
UVLO	Input Under Voltage Lock Out Threshold		3.7	3.9	4.1	V
$UVLO_{HYS}$	UVLO Hysteresis			340		mV
PG	Power Good Output Voltage Threshold on VDC pin		4.3	4.5	4.7	V
PG_{HYS}	PG Hysteresis			250		mV
Other Functions						
T_{RSTO}	Reset Time	See Figure 22; Xtal=16MHz	50			ms
T_{WD}	Watch-dog Pulse Width	See Figure 22	3.5			ms
T_{WM}	Watch-dog Pulse Period		T_{WD} + 3.5		1490	ms
T_{WO}	Watch-dog Time Out				1.5	s
T_{OUT}	TX TIME OUT	Control Register Bit 7 and Bit 8 See Figure 21		1 3		s
T_{OFF}	Time Out OFF Time	See Figure 21	125			ms
T_{OFFD}	RxTx 0->1 vs. TOUT Delay				20	µs
T_{CD}	Carrier Detection Time selectable by register	Control Register bit 9 and bit10 Figure 12		500 1 3 5		µs ms ms ms
T_{DCD}	CD_PD Propagation Delay	Figure 12		300	500	µs
M_{CLK}	Master Clock Output Selectable by register	Control Register bit 15 and bit 16 see table 11		fclock fclock/2 fclock/4		MHz
B_{AUD}	Baud rate	Control Register bit 3 and bit 4 see table 11		600 1200 2400 4800		Baud

Table 5. Electrical Characteristcs (continued)
(AVcc = DVcc = +5V, PAVcc =+9 V, PAVss, SGND = DVss = 0V,-40°C ≤ Tamb ≤ 85°C, Fc = 86kHz, other Control Register parameters as default value, unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_B	Baud rate Bit Time (=1/$_{BAUD}$)	Control Register bit 3 and bit 4 see table 11		1667 833 417 208		µs
Zero Crossing Detection						
ZC_{DEL}	Zero Crossing Detection delay (delay between the ZCIN and ZCOUT signals)	Figure 23			1	µs
$ZC_{(LOW)}$	Zero Crossing Detection Low Threshold		-45		-5	mV
$ZC_{(HIGH)}$	Zero Crossing Detection High Threshold		5		+45	mV
$ZC_{(OFFSET)}$	Zero Crossing Offset		-20		+20	mV
Operational Amplifier						
$C_{OUT(Sync)}$	Max Sync Current		15	28	45	mA
$C_{OUT(Source)}$	Max Source Current		-30	-20	-10	mA
$C_{IN(Offset)}$	Input Terminals OFFSET		-38		+38	mV
GBWP	Gain Bandwidth Product		6	7	9	MHz
Serial Interface						
Ts	Setup Time	see figure 6, 7, 8, 9 & 10			5	ns
T_H	Hold Time	see figure 6, 7, 8, 9 & 10			2	ns
T_{CR}	CLR/T vs. REG_DATA or RxTx	see figure 6, 7, 8, 9 & 10			$T_B/4$	
T_{CC}	CLR/T vs. CLR/T	see figure 6, 7, 8, 9 & 10	T_B		$2*T_B$	
T_{DS}	Setup Time	see figure 6, 7, 8, 9 & 10	$T_B/4$		$T_B/2$	
T_{DH}	Hold Time	see figure 6, 7, 8, 9 & 10	$T_B/4$		$T_B/2$	
T_{CRP}			T_H		$T_B/2$	

3 FUNCTIONAL DESCRIPTION

3.1 Carrier Frequencies

ST7538 is a multi frequency device: eight programmable Carrier Frequencies are available (see table 6). Only one Carrier at a time can be used; anyway, it's possible to switch the communication channel during the normal working Mode. Selecting the desired frequency in the Control Register the Transmission and Reception filters are accordingly tuned.

Table 6. ST7538 Channels List

FCarrier	F (KHz)
F0	60
F1	66
F2	72
F3	76
F4	82.05
F5	86
F6	110
F7(1)	132.5

3.2 Baud Rates

ST7538 is a multi Baud rate device: four Baud Rate are available (See table 7).

Table 7. ST7538 mark and space tones frequency distance Vs Baud Rate and Deviation

Baud Rate [Baud]	ΔF (2)(Hz)	Deviation (3)
600	600	1(4)
1200	600 1200	0.5 1
2400(1)	1200(1) 2400	0.5 1
4800	2400 4800	0.5 1

Note: 1. Default value
2. Frequency deviation.
3. Deviation = ΔF / (Baud Rate)
4. Deviation 0.5 Not Allowed

3.3 Mark and Space Frequencies

Mark and Space Communication Frequencies are defined by the following formula:

F ("0") = FCarrier + [ΔF]/2

F ("1") = FCarrier - [ΔF]/2

ΔF(Frequency Deviation) = Deviation*BAUD rate.

Here follows a table listing the correlation between frequency parameters and actual tones frequencies.

Table 8. ST7538 synthesized frequencies

Carrier Frequency (KHz)	Baud Rate	Deviation	Exact Frequency [Hz] (Clock=16MHz)		Carrier Frequency (KHz)	Baud Rate	Deviation	Exact Frequency [Hz] (Clock=16MHz)	
			"1"	"0"				"1"	"0"
60	600	--			82.05	600	--		
		1	59733	60221			1	81706	82357
	1200	0.5	59733	60221		1200	0.5	81706	82357
		1	59408	60547			1	81380	82682
	2400	0.5	59408	60547		2400	0.5	81380	82682
		1	58757	61198			1	80892	83171
	4800	0.5	58757	61198		4800	0.5	80892	83171
		1	57617	62337			1	79590	84473
66	600	--			86	600	--		
		1	65755	66243			1	85775	86263
	1200	0.5	65755	66243		1200	0.5	85775	86263
		1	65430	66569			1	85449	86589
	2400	0.5	65430	66569		2400	0.5	85449	86589
		1	64779	67220			1	84798	87240
	4800	0.5	64779	67220		4800	0.5	84798	87240
		1	63639	68359			1	83659	88379
72	600	--			110	600	--		
		1	71777	72266			1	109701	110352
	1200	0.5	71777	72266		1200	0.5	109701	110352
		1	71452	72591			1	109375	110677
	2400	0.5	71452	72591		2400	0.5	109375	110677
		1	70801	73242			1	108724	111165
	4800	0.5	70801	73242		4800	0.5	108724	111165
		1	69661	74382			1	107585	112467
76	600	--			132.5	600	--		
		1	75684	76335			1	132161	132813
	1200	0.5	75684	76335		1200	0.5	132161	132813
		1	75358	76660			1	131836	133138
	2400	0.5	75358	76660		2400	0.5	131836	133138
		1	74870	77148			1	131348	133626
	4800	0.5	74870	77148		4800	0.5	131348	133626
		1	73568	78451			1	130046	134928

3.4 Host Processor Interface

ST7538 exchanges data with the host processor thorough a serial interface.

The data transfer is managed by REG_DATA and RxTx Lines, while data are exchanged using RxD, TxD and CLR/T lines.

Four are the ST7538 working modes:

- Data Reception
- Data Transmission
- Control Register Read
- Control Register Write

REG_DATA and RxTx lines are level sensitive inputs.

Table 9. Data and Control register access bits configuration

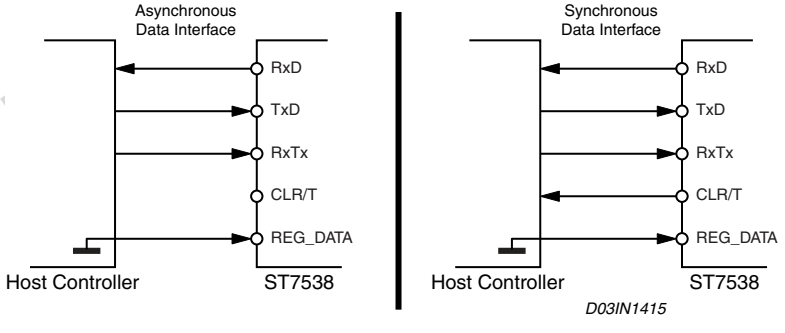
	REG_DATA	RxTx
Data Transmission	0	0
Data Reception	0	1
Control Register Read	1	1
Control Register Write	1	0

- **Mains Access**

  ST7538 features two type of communication interfaces:
  - Asynchronous
  - Synchronous

  The selection can be done through the internal Control Register.

Figure 4. Synchronous and Asynchronous ST7538/Host Controller interfaces



– Asynchronous Mode.

ST7538 allows to interface the Host Controller using a 3 line interface (RXD,TXD & RxTx).
Data are exchange without any auxiliary Clock reference in an Asynchronous mode without adding any protocol bits. The host controller has to recover the clock reference in receiving Mode and control the Bit time in transmission mode. RxD line is forced to a low logic level when no carrier is detected.

– **Synchronous mode.**

ST7538 allows to interface the host Controller using a four lines synchronous interface (RXD,TXD, CLR/T & RxTx). ST7538 is always the master of the communication and provides the clock reference on CLR/T line.
When ST7538 is in receiving mode an internal PLL recovers the clock reference. Data on RxD line are stable on CLR/T rising Edge.

When ST7538 is in transmitting mode the clock reference is internally generated and data are read on TxD line on CLR/T rising Edge.

If RxTx line is set to “1” & REG_DATA=”0” (Data Reception), ST7538 enters in an Idle State and CLR/T line is forced Low. After Tcc time the modem starts providing received data on RxD line.

If RxTx line is set to “0” & REG_DATA=”0” (Data Transmission), ST7538 enters in an Idle State and transmission circuitry is switched on. After Tcc time the modem starts transmitting data present on TXD line (figure 6) .

Figure 5. Receiving and transmitting data/recovered clock timing

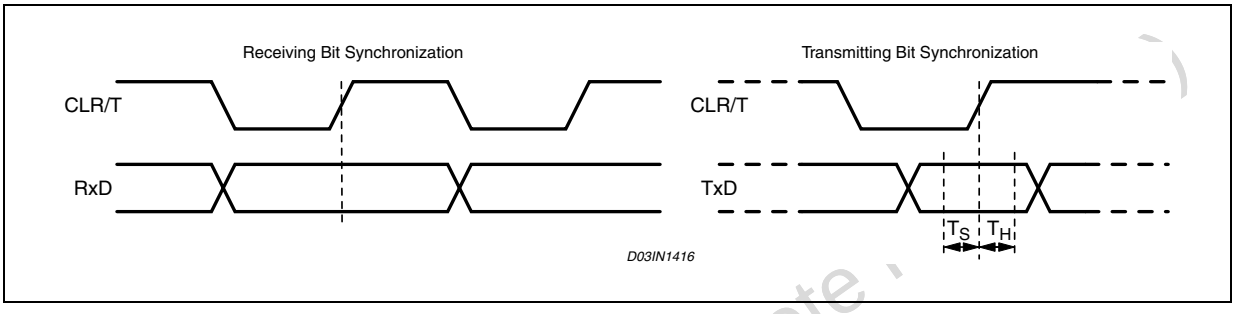
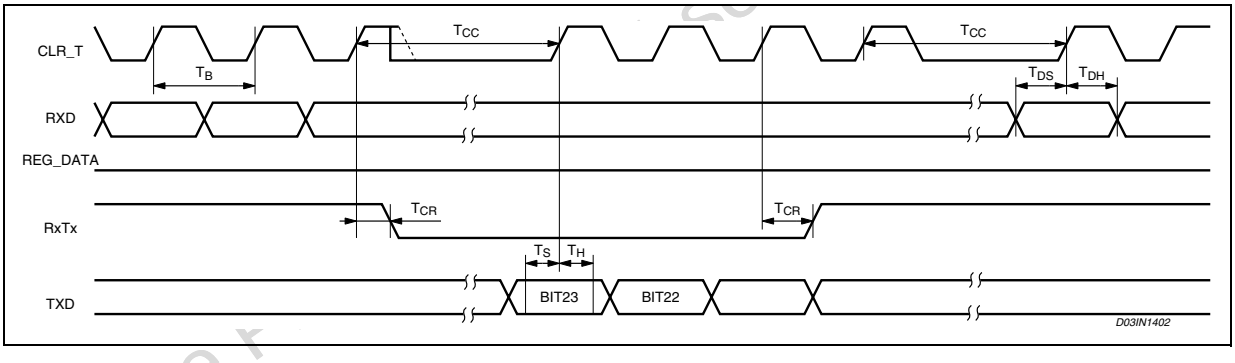


Figure 6. Data Reception -> Data Transmission -> Data reception



3.5 Control Register Access

The communication with ST7538 Control Register is always synchronous. The access is achieved using the same lines of the Mains interface (RxD, TxD and CLR/T) plus REG_DATA Line.

With REG_DATA = 1 and RxTx=0, the data present on TxD are loaded into the Control Register MSB first. The ST7538 samples the TxD line on CLR/T rising edges. The control Register content is updated at the end of the register access section (REG_DATA falling edge). If more than 24 bits are transferred to ST7538 only the latest 24 bits are stored inside the Control Register.

With REG_DATA = 1 and RxTx=1, the content of the Control Register is sent on RxD port. The Data on RxD are stable on CLR/T rising edges MSB First.

Figure 7. Data Reception ➨ Control Register read ➨ Data Reception Timing Diagram

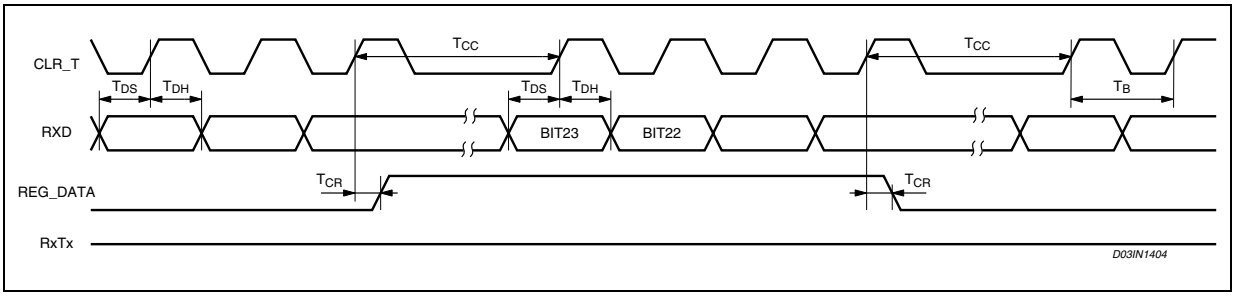


Figure 8. Data Reception ➨ Control Register write ➨ Data Reception Timing Diagram

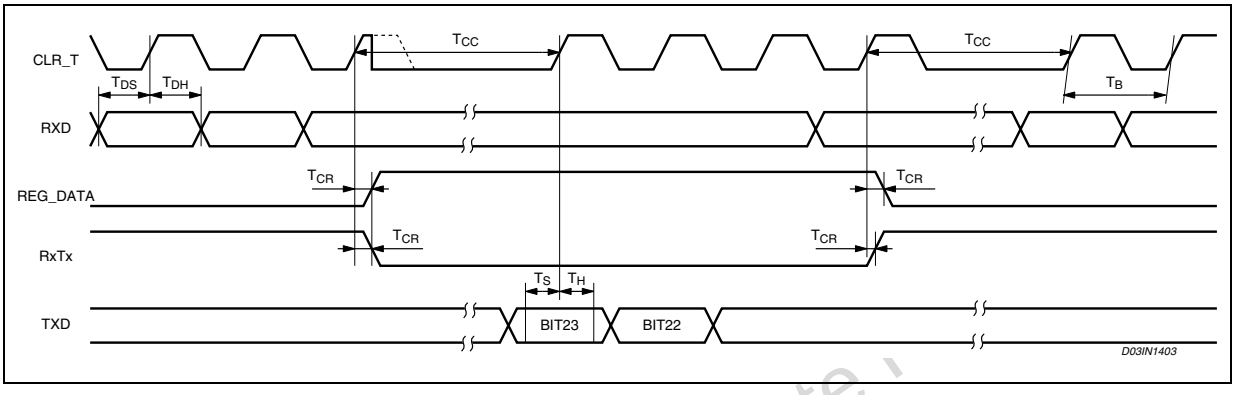


Figure 9. Data Transmission ➨ Control Register read ➨ Data Reception Timing Diagram

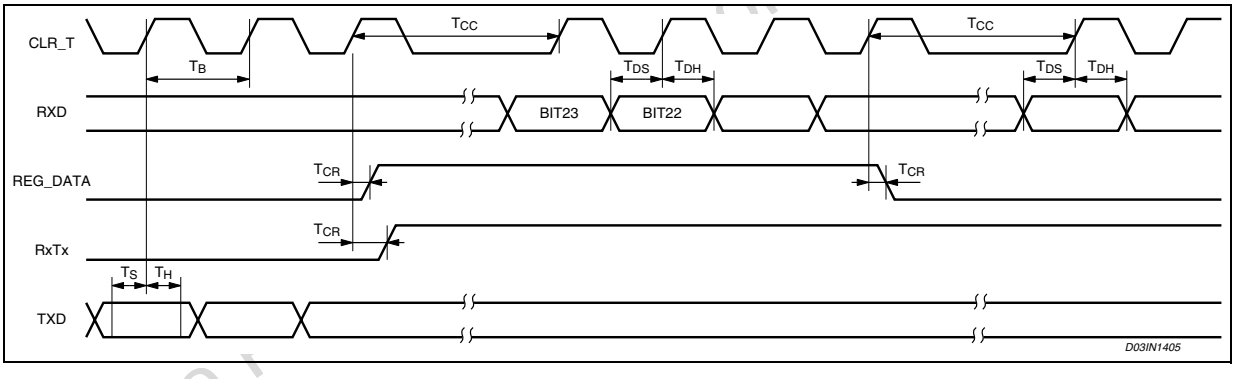
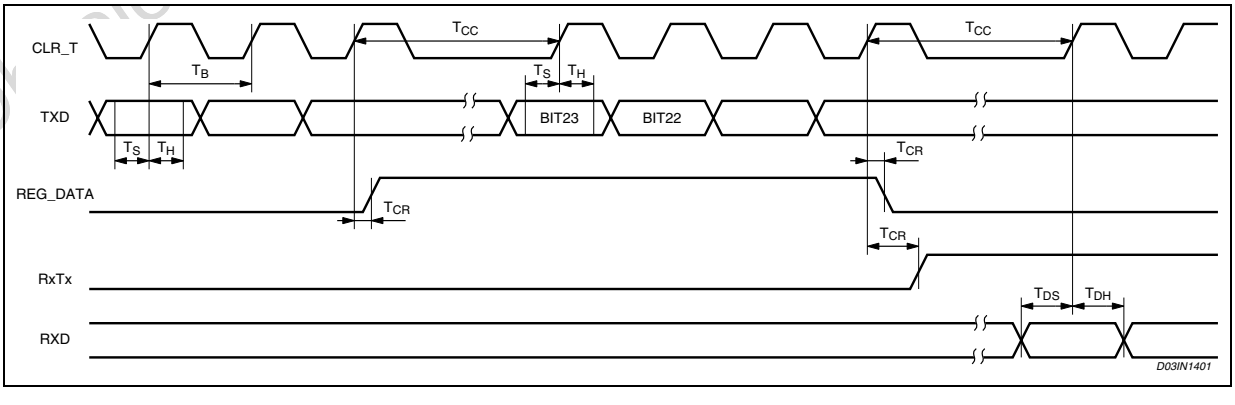


Figure 10. Data Transmission ➨ Control Register Write ➨ Data Reception Timing Diagram



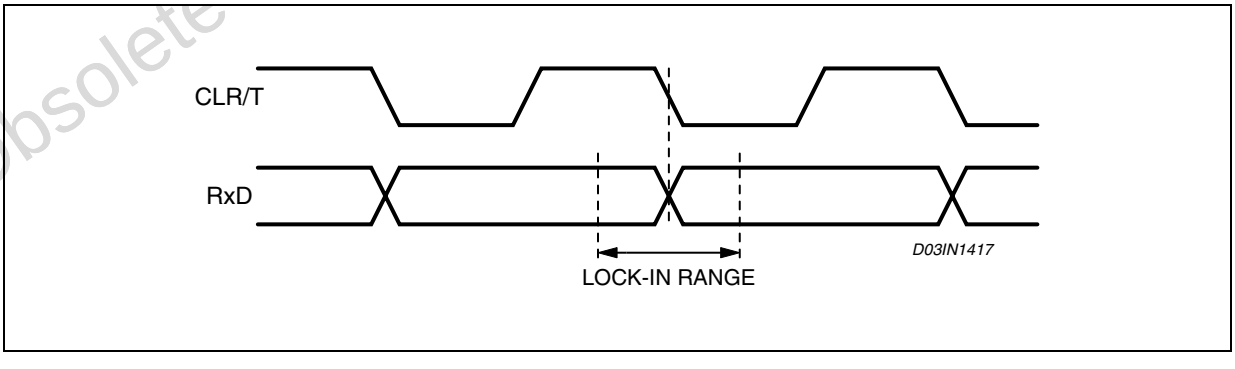
3.6 Receiving Mode

The receive section is active when RxTx Pin ="1" and REG_DATA=0.
The input signal is read on RAI Pin using SGND as ground reference and then pre-filtered by a Band pass Filter (62kHz max. bandwidth at -3dB). The Pre-Filter can be removed setting one bit in the Control Register. The Input Stage features a wide dynamic range to receive Signal with a Very Low Signal to Noise Ratio. The Amplitude of the applied waveform is automatically adapted by an Automatic Gain Control block (AGC) and then filtered by a Narrow Band Band-Pass Filter centered around the Selected Channel Frequency (14kHz max. bandwidth at -3dB). The resulting signal is down-converted by a mixer using a sinewave generated by the FSK Modulator. Finally an Intermediate Frequency Band Pass-Filter (IF Filter) improves the Signal to Noise ration before sending the signal to the FSK demodulator. The FSK demodulator then send the signal to the RX Logic for final digital filtering. Digital filtering Removes Noise spikes far from the BAUD rate frequency and Reduces the Signal Jitter. RxD Line is forced at logic level "0" when neither mark or space frequencies are detected on RAI Pin.
Mark and Space Frequency in Receiving Mode must be distant at least BaudRate/2 to have a correct demodulation.
While ST7538 is in Receiving Mode (RxTx pin ="1"), the transmit circuitry, Power Line Interface included, are turned off. This allows the device to achieve a very low current consumption (5 mA typ). In Receiving mode ATOP2 pin is internally connected to PAVSS.

- **High Sensitivity Mode**
  It is possible to increase ST7538 Receiving Sensitivity setting to "1" the High Sensitivity Bit of Control Register. This Function allows to increase the communication reliability when the ST7538 sensitivity is the limiting factor.

- **Synchronization Recovery System (PLL)**
  ST7538 embeds a Clock Recovery System to feature a Synchronous data exchange with the Host Controller.
  The clock recovery system is realized by means of a second order PLL. Data on the data line (RxD) are stable on CLR/T line rising edge (CLR/T Falling edge synchronized to RxD line transitions ± LOCK-IN Range).
  The PLL Lock-in and Lock-out Range is $\pm\pi/2$. When the PLL is in the unlock condition, CLR/T and RxD lines are forced to a low logic level.
  When PLL is in unlock condition it is sensitive to RxD Rising and Falling Edges. The maximum number of transition required to reach the lock-in condition is 5. When in lock-in condition the PLL is sensitive only to RxD rising Edges to reduce the CLR/T Jitter.
  ST7538 PLL is forced in the un-lock condition, when more than 32 equal symbols are received.
  Due to the fact that the PLL, in lock-in condition, is sensitive only to RxD rising edge, sequences equal or longer than 15 equal symbols can put the PLL into the un-lock condition.

Figure 11. ST7538 PLL lock-in range



■ **Carrier/Preamble Detection**

The Carrier/Preamble Block is a digital Frequency detector Circuit.
It can be used to manage the MAINS access and to detect an incoming signal.
Two are the possible setting:
- Carrier Detection
- Preamble Detection

CARRIER DETECTION: The Carrier/Preamble detection Block notifies to the host controller the presence of a Carrier when it detects on the RAI Input a signal with an harmonic component close to the programmed Carrier Frequency. The CD_PD signal sensitivity is identical to the data reception sensitivity (0.5mVrms Typ. in Normal Sensitivity Mode).
The CD_PD line is forced to a logic level low when a Carrier is detected.
PREAMBLE DETECTION: The Carrier/Preamble detection Block notifies to the host controller the presence of a Carrier modulated at the Programmed Baud Rate for at least 4 Consecutive Symbols ("1010" or "0101" are the symbols sequences detected).
CD_PD line is forced low till a Carrier signal is detected and PLL is in the lock-in range.
To reinforce the effectiveness of the information given by CD_PD Block, a digital filtering is applied on Carrier or Preamble notification signal (See Control Register Paragraph). The Detection Time Bits in the Control Register define the filter performance. Increasing the Detection Time reduced the false notifications caused by noise on main line. The Digital filter adds a delay to CD_PD notification equal to the programmed Detection Time. When the carrier frequency disappears, CD_PD line is held low for a period equal to the detection time and then forced high.

Figure 12. CD_PD Timing during RX

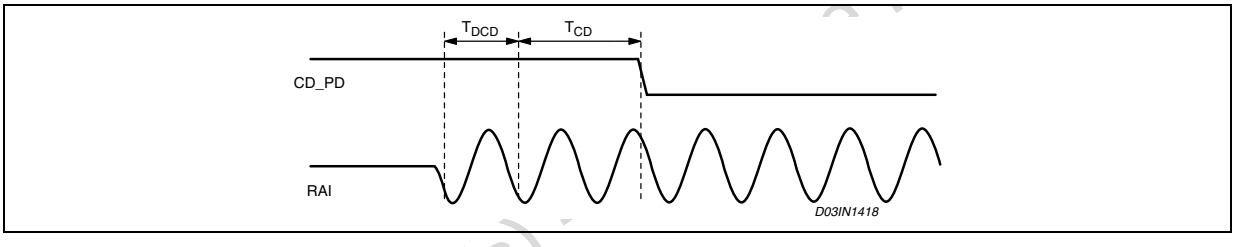
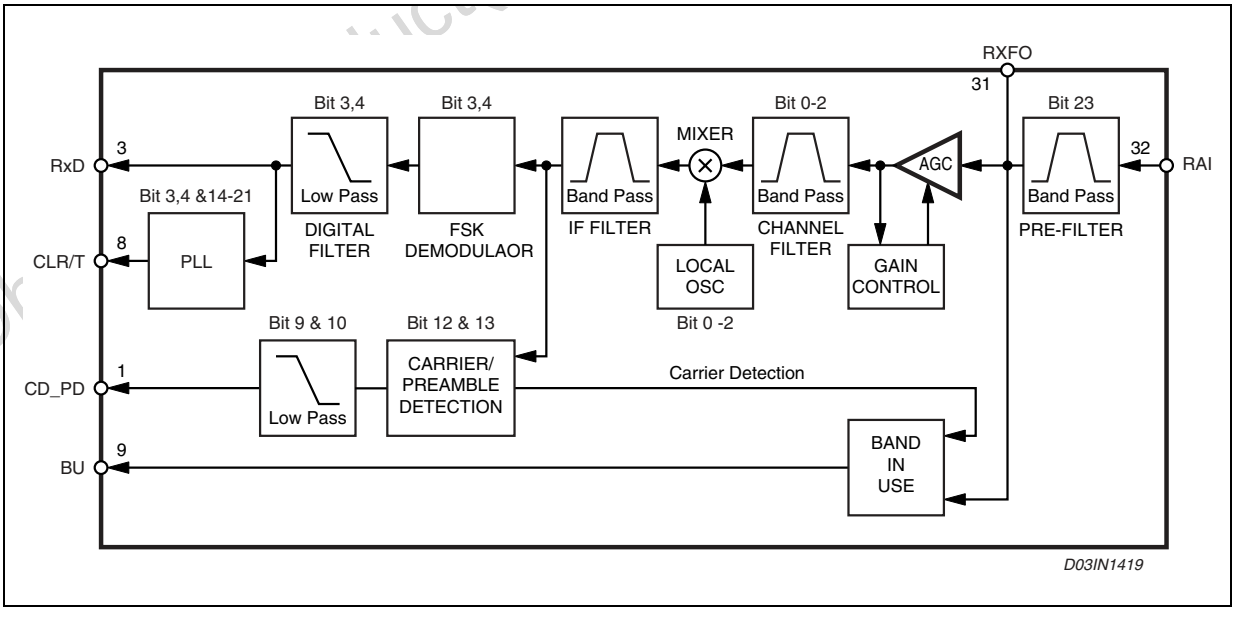


Figure 13. Receiving Path Block Diagram



3.7 Transmission Mode

The transmit mode is set when RxTx Pin ="0" and REG_DATA Pin ="0". In transmitting mode the FSK Modulator and the Power Line Interface are turned ON. The transmit Data (TXD) enter synchronously or asynchronously to the FSK modulator.

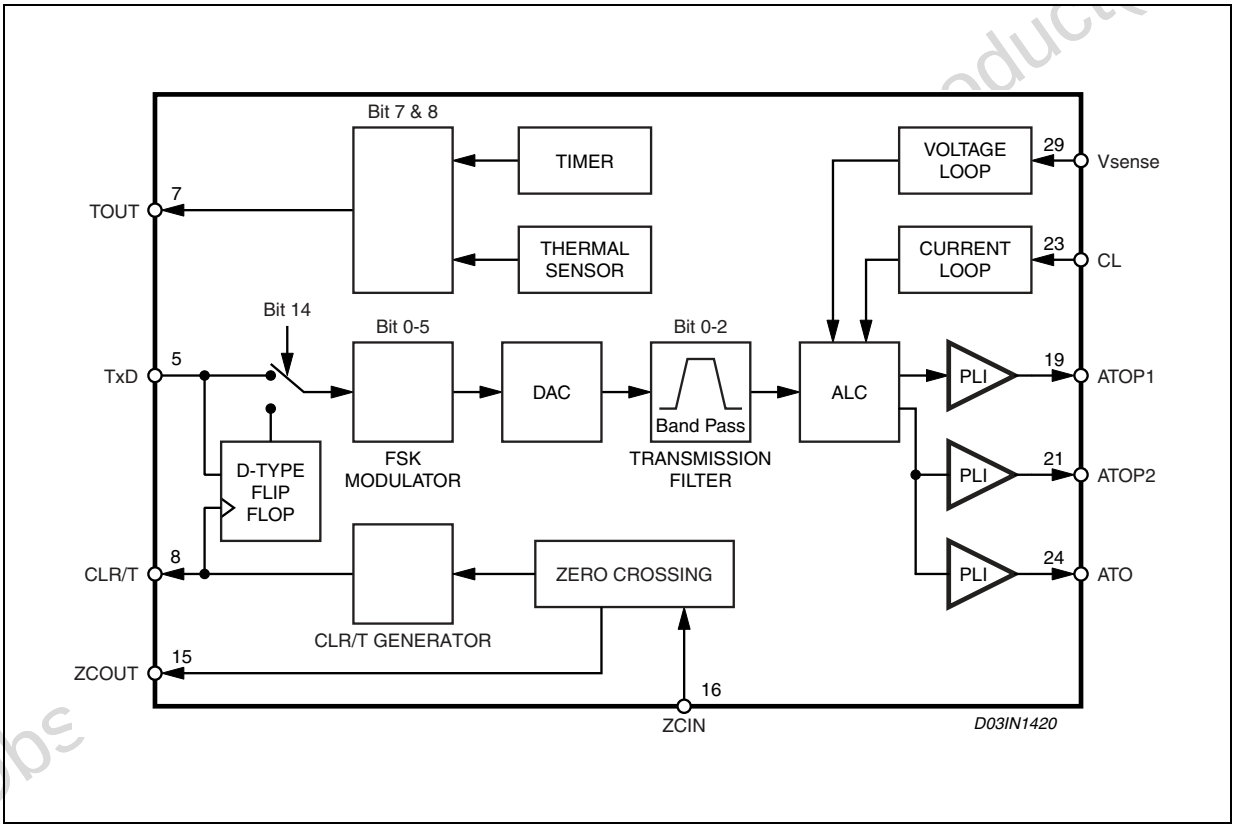
– Host Controller Synchronous Communication Mode: on CLR/T rising edge, TXD Line Value is read and sent to the FSK Modulator. ST7538 Manage the Transmission timing according to the BaudRate Selected

– Host Controller Asynchronous Communication Mode: TXD data enter directly to the FSK Modulator.The Host Controller Manages the Transmission timing

In both conditions no Protocol Bits are added by ST7538.

The FSK frequencies are synthesized in the FSK modulator from a 16 MHz crystal oscillator by direct digital synthesis technique. The frequencies Table in different Configuration is reported in Table 8. The frequencies precision is same as external crystal one's.
In the analog domain, the signal is filtered in order to reduce the output signal spectrum and to reduce the harmonic distortion. The transition between a symbol and the following is done at the end of the on-going half FSK sinewave cycle.

Figure 14. Transmitting Path Block Diagram



■ **Automatic Level Control (ALC)**

The Automatic Level Control Block (ALC) is a variable gain amplifier (with 32 non linear discrete steps) controlled by two analog feed backs acting at the same time. The ALC gain range is 0dB to 30 dB and the gain change is clocked at 5KHz. Each step increases or reduces the voltage of 1dB (Typ).
Two are the control loops acting to define the ALC gain:
- A Voltage Control loop
- A Current Control Loop

The Voltage control loop acts to keep the Peak-to-Peak Voltage constant on Vsense. The gain adjustment is related to the result of a peak detection between the Voltage waveform on Vsense and two internal Voltage references.

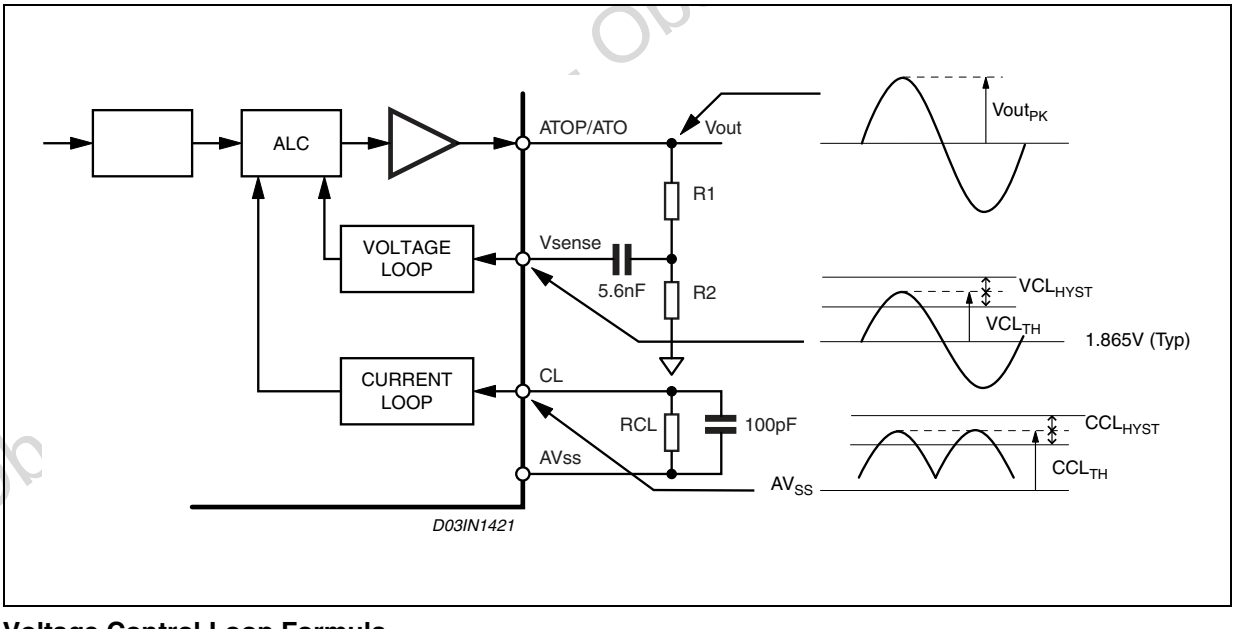
- If Vsense < VCL_{TH} - VCL_{HYST}	The next gain level is increased by 1 step
- If VCL_{TH} - VCL_{HYST} < Vsense < VCL_{TH} + VCL_{HYST}	No Gain Change
- If Vsense > VCL_{TH} + VLC_{HYST}	The next gain level is decreased by 1 step

The Current control loop acts to limit the maximum Peak Output current inside ATOP1 and ATOP2.
The current control loop acts through the voltage control loop decreasing the Output Peak-to-Peak Amplitude to reduce the Current inside the Power Line Interface.
The current sensing is done by mirroring the current in the High side MOS of the Power Amplifier (not dissipating current Sensing). The Output Current Limit (up to 370mArms), is set by means of an external resistor (R_{CL}) connected between CL and PAVss. The resistor converts the current sensed into a voltage signal. The Peak current sensing block works as the Output Voltage sensing Block:

- If V(CL) < CCL_{TH} - CCL_{HYST}	Voltage Control Loop Acting
- If CCL_{TH} - CCL_{HYST} < V(CL) < CCL_{TH} + CCL_{HYST}	No Gain Change
- If V(CL) > CCL_{TH} + CLC_{HYST}	The next gain level is decreased by 1 step

Figure 15 shows the typical connection of Current anVoltage control loops.

Figure 15. Voltage and Current Feedback external interconnection Example



Voltage Control Loop Formula

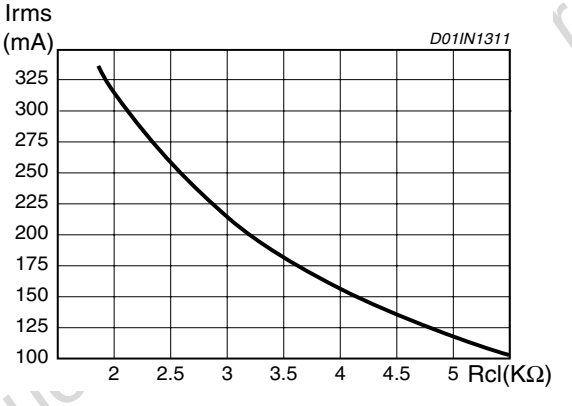
$$Vout_{PK} \cong \frac{R_1 + R_2}{R_2} \cdot (VCL_{TH} \pm VCL_{HYST})$$

Table 10. Vout vs. R1 & R2 resistors value

Vout (Vrms)	Vout (dBμV)	(R1+R2)/R2	R2 (KΩ)	R1 (KΩ)
0.150	103.5	1.1	7.5	1.0
0.250	108.0	1.9	5.1	3.9
0.350	110.9	2.7	3.6	5.6
0.500	114.0	3.7	3.3	8.2
0.625	115.9	4.7	3.3	11.0
0.750	117.5	5.8	2.7	12.0
0.875	118.8	6.6	2.0	11.0
1.000	120.0	7.6	1.6	10.0
1.250	121.9	9.5	1.6	13.0
1.500	123.5	10.8	1.6	15.0

Notes: The rate of R2 takes in account the input resistance on the SENSE pin (36 KΩ).
5.6nF capacitor effect has been neglected.

Figure 16. Typical Output Current vs. Rcl



■ **Integrated Power Line Interface (PLI)**

The Power Line Interface (PLI) is a double CMOS AB Class Power Amplifier with the two outputs (ATOP1 and ATOP2) in opposition of phase.

Two are the possible configuration:

- Single Ended Output (ATOP1).
- Bridge Connection

The Bridge connection guarantee a Differential Output Voltage to the load with twice the swing of each individual Output. This topology virtually eliminates the even harmonics generation.

The PLI requires, to ensure a proper operation, a regulated and well filtered Supply Voltage. PAVcc Voltage must fulfil the following formula to work without clipping phenomena:

$$PAVcc \geq \frac{VATOP(AC)}{2} + 7.5V$$

To allow the driving of an external Power Line Interface, the output of the ALC is available even on ATO pin. ATO output has a current capability much lower than ATOP1 and ATOP2.

Figure 17. PLI Bridge Topology

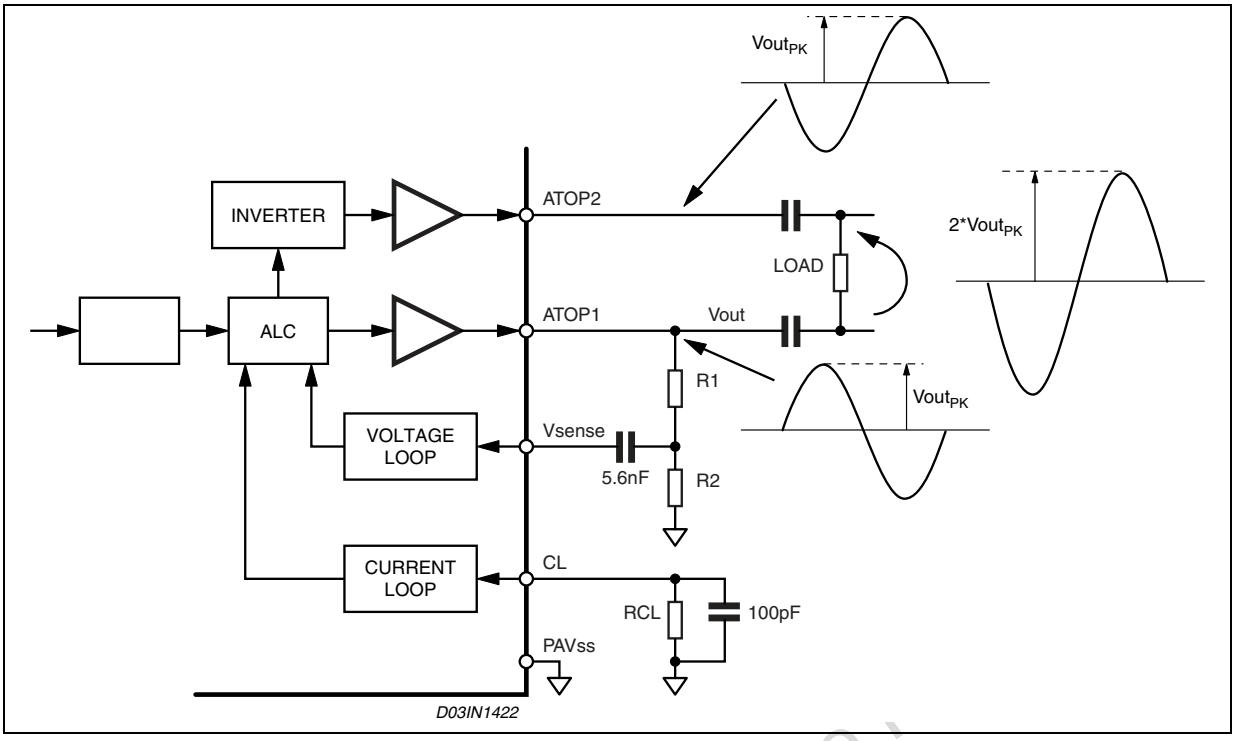
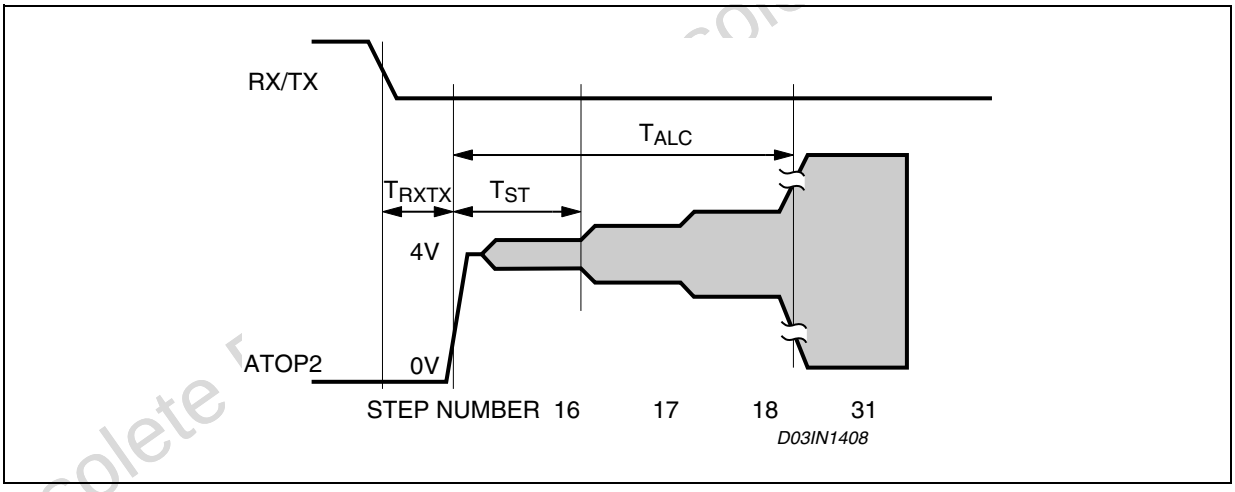


Figure 18. PLI Startup Timing Diagram



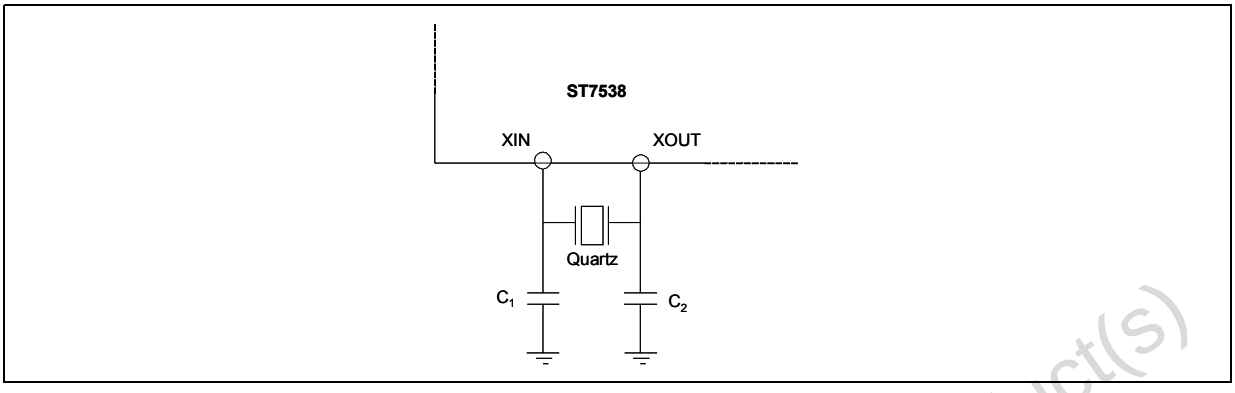
3.8 Crystal Oscillator

ST7538 integrates a sub-threshold driver circuit to realize a 16MHz crystal oscillator.

This circuit is able to drive a maximum load capacitance of 16pF with typical quartz ESR of 40Ω.

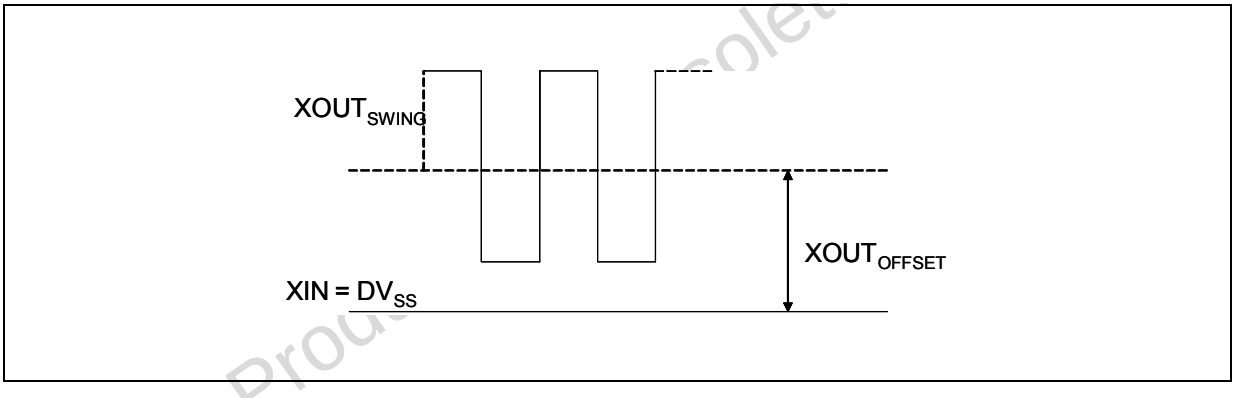
If the internal driver circuit is used, only one external crystal quartz and two external load capacitors (C_1 e C_2) are needed to realize the oscillator function (fig.19).

Figure 19. Typical crystal configuration if ST7538 internal crystal driver circuit is used



If an external oscillator is used, XIN must be connected to DVss, while XOUT must satisfy the specifications given in table 5 (see also fig.20).

Figure 20. XOUT waveforms if an external oscillator is used (see table 8 for parameter values)



3.9 Control Register

The ST7538 is a multi-channel and multifunction transceiver. An internal 24 Bits Control Register allows to manage all the programmable parameters (table 11).
The programmable functions are:

- Channel Frequency
- Baud Rate
- Deviation
- Watchdog
- Transmission Timeout
- Frequency Detection Time

- Zero Crossing Synchronization
- Detection Method
- Mains Interfacing Mode
- Output Clock
- Input Pre-Filter
- Sensitivity Mode

Table 11. Control Register Functions

	Function	Value	Selection			Note	Default
0 to 2	Frequencies		**Bit2**	**Bit1**	**Bit0**		
		60 KHz	0	0	0		132.5 kHz
		66 KHz	0	0	1		
		72 KHz	0	1	0		
		76 KHz	0	1	1		
		82.05 KHz	1	0	0		
		86 KHz	1	0	1		
		110 KHz	1	1	0		
		132.5 KHz	1	1	1		
3 to 4	Baud Rate		**Bit 4**	**Bit 3**			
		600	0	0			2400
		1,200	0	1			
		2,400	1	0			
		4,800	1	1			
5	Deviation		**Bit 5**				
		0.5	0				0.5
		1	1				
6	Watchdog		**Bit 6**				
		Disabled	0				Enabled
		Enabled (1.5 s)	1				
7 to 8	Transmission Time Out		**Bit 8**	**Bit 7**			
		Disabled	0	0			1 sec
		1 s	0	1			
		3 s	1	0			
		Not Used	1	1			
9 to 10	Frequency detection time		**Bit 10**	**Bit 9**			
		500 µs	0	0			1 ms
		1 ms	0	1			
		3 ms	1	0			
		5 ms	1	1			
11	Zero Crossing Synchronization		**Bit 11**				
		Disabled	0				Disabled
		Enabled	1				
			Bit 13	**Bit 12**			

Table 11. Control Register Functions (continued)

	Function	Value	Selection		Note	Default
12 to 13	Detection Method	Carrier detection without conditioning	0	0	Carrier Detection Notification on CD_PD Line CLR/T and RxD signal always Present	Preamble detection without conditioning
		Carrier detection with conditioning	0	1	CLR/T and RxD lines are forced to “0” when Carrier is not detected	
		Preamble detection without conditioning	1	0	Preamble Detection Notification on CD_PD Line CLR/T and RxD signal always Present	
		Preamble detection with conditioning	1	1	Preamble Detection Notification on CD_PD Line CLR/T and RxD lines are forced to “0” when Preamble has not been detected or PLL is in Unlock condition	
14	Mains Interfacing Mode		**Bit 14**			Asynchronous
		Synchronous Asynchronous	0 1			
15 to 16	Output Clock		**Bit 16**	**Bit 15**		4 MHz
		16 MHz 8 MHz 4 MHz Not Used	0 0 1 1	0 1 0 1		
17 to 20	Not Used					1001
21	Reserved				Do not modify the default value	0
22	Sensitivity Mode		**Bit 22**			Normal
		Normal Sensitivity High Sensitivity	0 1			
23	Input Filter		**Bit 23**			Disabled
		Disabled Enabled	0 1			

4 AUXILIARY ANALOG AND DIGITAL FUNCTIONS

4.1 Band In Use

The Band in Use Block has a Carrier Detection like function but with a different Input Sensibility (77dBµV Typ.)
and with a different BandPass filter Selectivity (40dB/Dec).

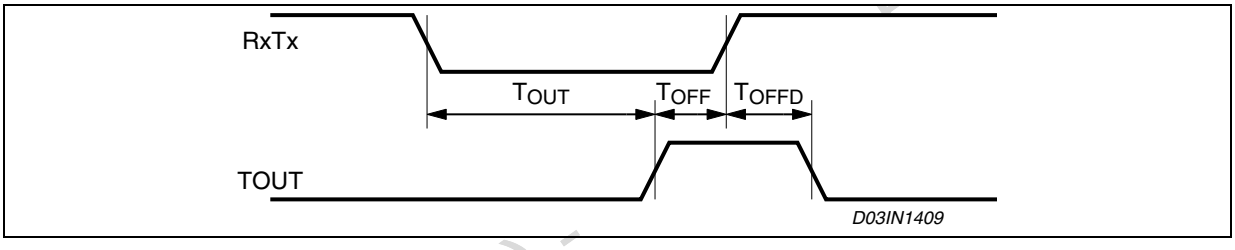
BU line is forced High when a signal in band is detected.
To prevent BU line false transition, BU signal is conditioned to Carrier Detection Internal Signal.

4.2 Time Out

Time Out Function is a protection against a too long data transmission. When Time Out function is enabled after 1 or 3 second of continuos transmission the transceiver is forced in receiving mode. This function allows ST7538 to automatically manage the CENELEC Medium Access specification. When a time-out event occur, TOUT is forced high, and is held high for at least 125 ms. To Unlock the Time Out condition RxTx should be forced High. During the time out period only register access or reception mode are enabled.

During Reset sequence if RxTx line =”0” & REG_DATA line =”0”, TIMEOUT protection is suddendly enabled and ST7538 must be configured in data reception after the reset event before starting a new data transmission.
Time Out time is programmable using Control Register bits 7 and 8 (table 11).

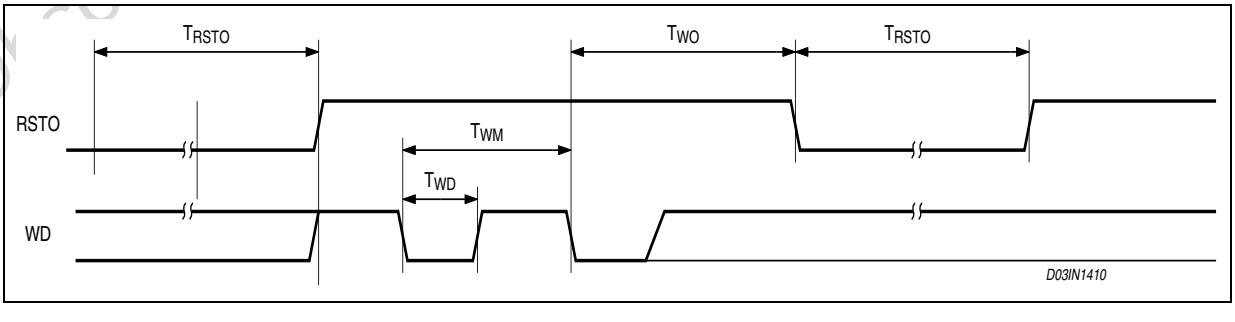
Figure 21. Time-out Timing and Unlock Sequence



4.3 Reset & Watchdog

RSTO Output is a reset generator for the application circuitry. During the ST7538 startup sequence is forced low. RSTO becomes high after a T_{RSTO} delay from the end of oscillator startup sequence.
Inside ST7538 is also embedded a watchdog function. The watchdog function is used to detect the occurrence of a software fault of the Host Controller. The watchdog circuitry generates an internal and external reset (RSTO low for T_{RSTO} time) on expiry of the internal watchdog timer. The watchdog timer reset can be achieved applying a negative pulse on WD pin Fig 22.

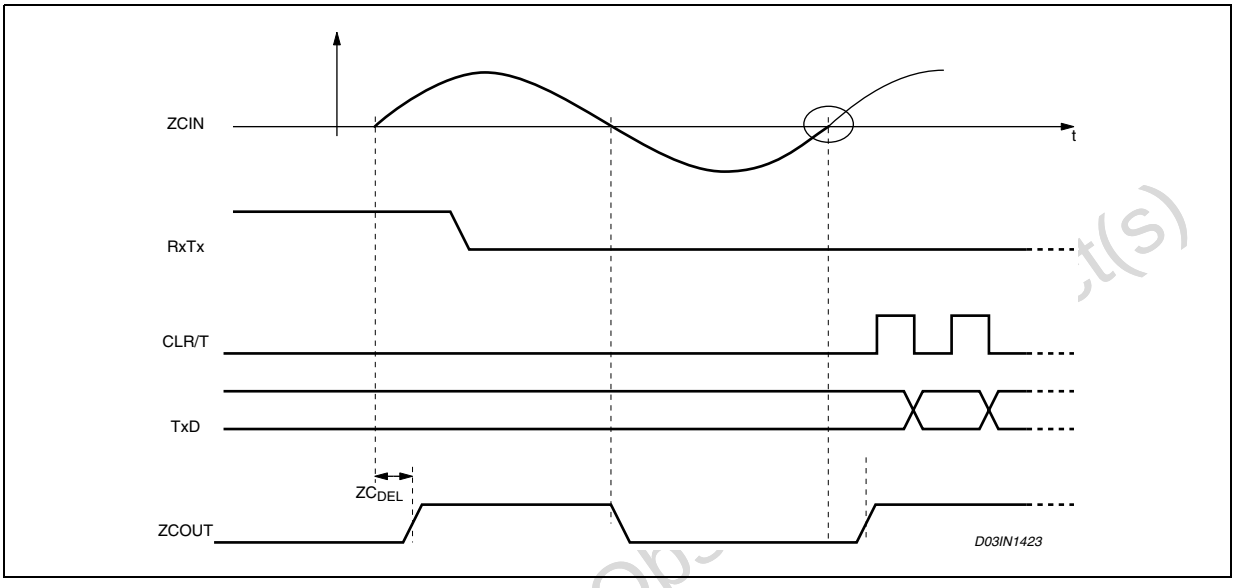
Figure 22. Reset and Watchdog Timing



4.4 Zero Crossing Detection

The Mains Voltage Zero Crossing can be detected, through a proper connection of ZCIN to the Mains. ZCIN comparator has a threshold fixed at SGND. ZCOUT is a TTL Output forced High after a positive zero-crossing transition, and low after a negative one.
Setting the Bit 11 inside the Control Register to “1” the transmission is automatically synchronized to the mains positive zero-crossing transition. This function is achieved turning on the PLI when RX/TX is low and delaying the CLR/T first transition until the first zero-crossing event. The automatic synchronization procedure can work only if the synchronous interface is programmed. If asynchronous interface is in use the Zero Crossing synchronization can be achieved managing the ZCOUT line.

Figure 23. Synchronous Zero-Crossing Transmission



4.5 Output Clock

MCLK is the master clock output. The clock frequency sourced can be programed through the control register to be a ratio of the crystal oscillator frequency (Fosc, Fosc/2 Fosc/4). The transition between one frequency and another is done only at the end of the ongoing cycle.

4.6 Reg OK

REGOK allows to detect an accidental corruption of the Control Register content. If a register content corruption is detected, REGOK goes to "1". REGOK function is disabled during a control register writing session.

4.7 Under Voltage Lock Out

The UVLO function turns off the device if the PAVdd voltage falls under 4V. Hysteresis is 340mV typically.

4.8 Thermal Shutdown

The ST7538 is provided of a thermal protection which turn off the PLI when the junction temperature exceeds 170°C ±10% . Hysteresis is around 30°C.

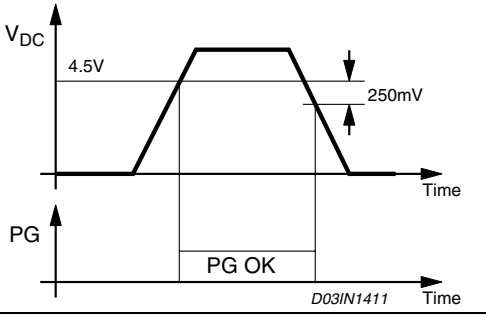
When shutdown threshold is overcome, PLI interface is switched OFF.

Thermal Shutdown event is notified to the HOST controller using TIMEOUT line. When TIMEOUT line is High, ST7538 junction temperature exceed the shutdown threshold (Not Lached).

4.9 5V Voltage Regulator and Power Good Function

ST7538 has an embedded 5V linear regulator externally available to supply the application circuitry. The linear regulator has a very low quiescent current (50µA) and a current capability of 100mA. The regulator is protected against short circuitry events.
When the regulator Voltage is above the power good threshold ($V_{PG)}$, Power Good line is forced high, while is forced low at startup and when VDC falls below V_{PG} - V_{PGHYS} Voltage.

Figure 24. Power Good Function



4.10 Power-Up Procedure

To ensure ST7538 proper power-Up sequence, PAVcc, AVss and DVss Supply has to fulfil the following rules:

1) PAVcc rising slope must not exceed 100V/ms.

2) When DVdd and AVdd are below 5V (externally supplied): 100mV < PAVcc-AVdd , PAVcc-DVdd < 1.2V.

When AVdd and DVdd supply are connected to VDC, with load < 100mA and filtering capacitor on VDC < 100uF, the second rule can be ignored.

Figure 25. Power-UP Sequence

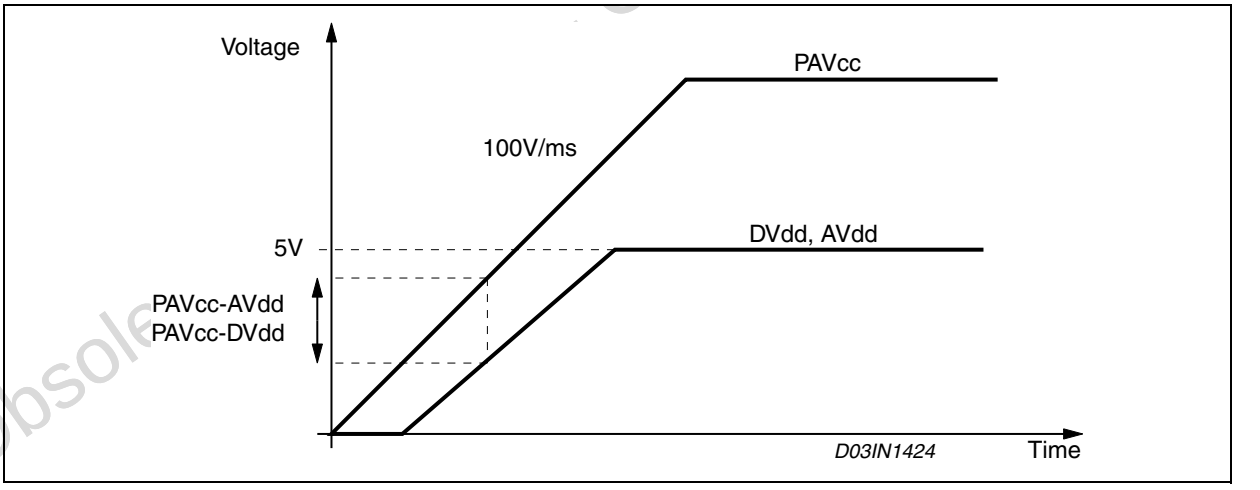
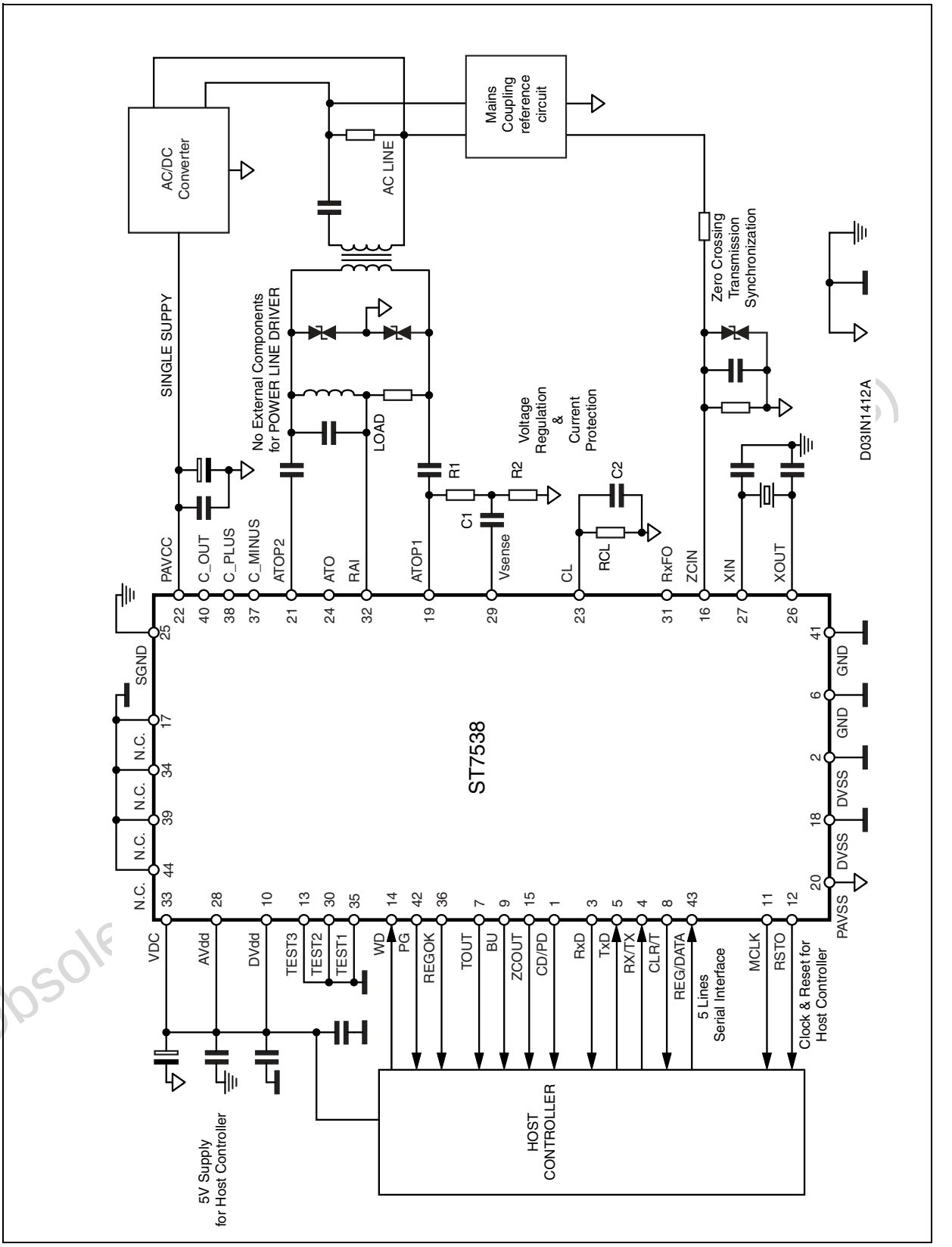


Figure 26. Application Schematic Example with Coupling Tranformer.



5 PACKAGE INFORMATION

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

5.1 Thermal and Soldering Information

Best thermal performance is acheived when slug is soldered to PCB.
It is recomended to have five solder dots (See fig. 28) without resist to connect the Copper slug to the ground layer on the soldering side. Moreover it is recomeded to connect the ground layer on the soldering side to another ground layer on the opposite side with 15 to 20 vias.

It is suggested to not use the PCB surface below the slug area to interconnect any pin except groung pins.

Figure 27. ST7538 Slug Drawing

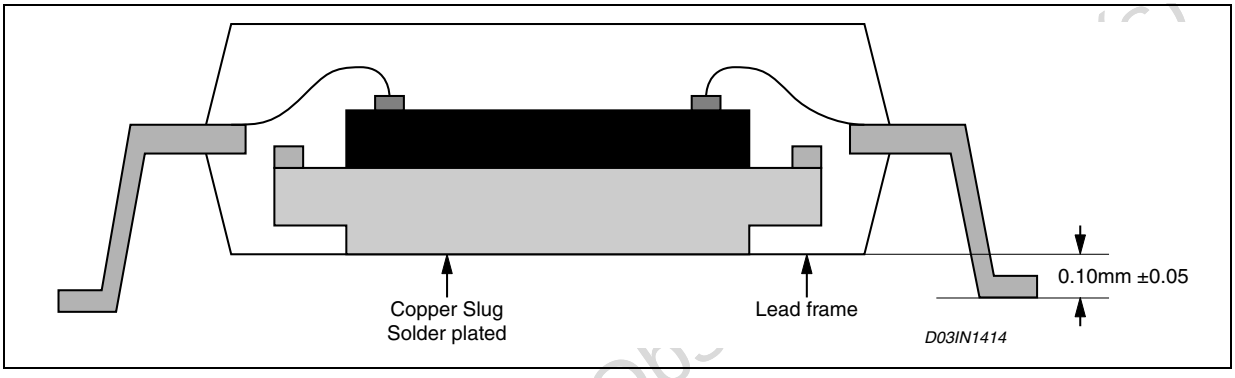
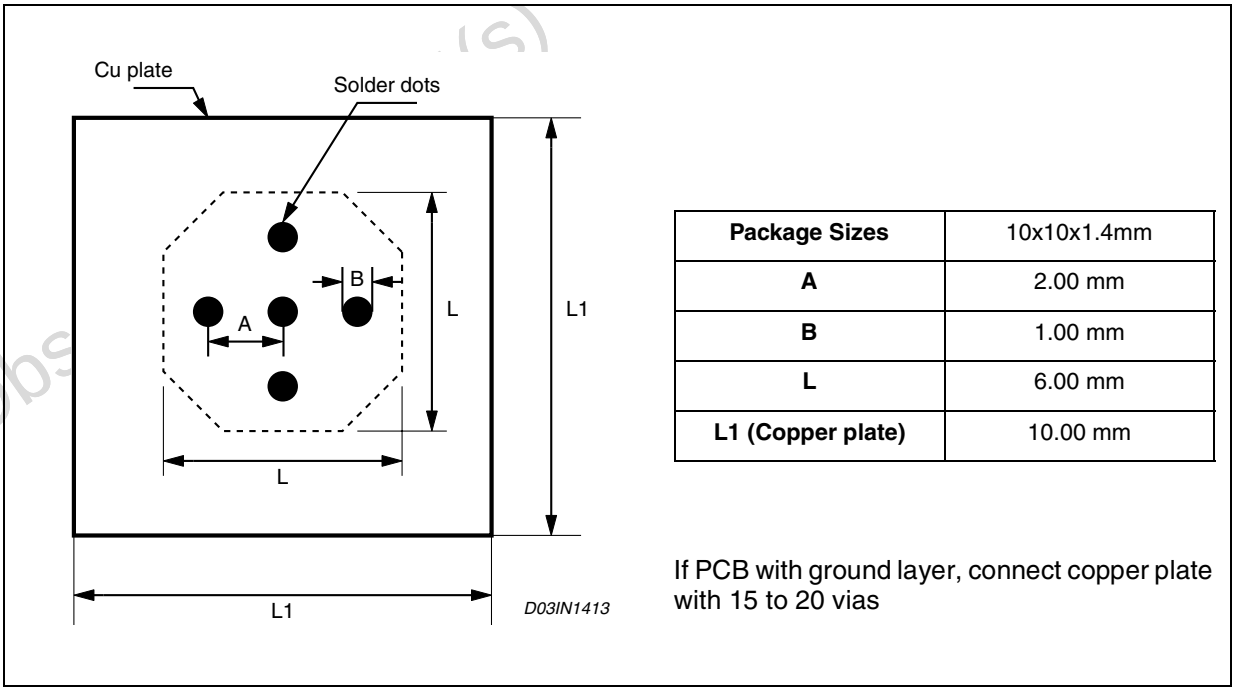


Figure 28. Soldering Information



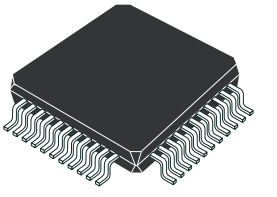
Package Sizes	10x10x1.4mm
A	2.00 mm
B	1.00 mm
L	6.00 mm
L1 (Copper plate)	10.00 mm

If PCB with ground layer, connect copper plate with 15 to 20 vias

Figure 29. TQFP44 (Slug Down) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.37	0.45	0.012	0.014	0.018
c	0.09		0.20	0.003		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
e		0.80			0.031	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
H		5.89			0.232	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
S	6.00			0.236		
S1	6.00			0.236		
K	0° (min.), 3.5° (typ.), 7°(max.)					
ccc			0.10			0.004

OUTLINE AND MECHANICAL DATA



TQFP44 (10x10x1.40mm) with Slug Down

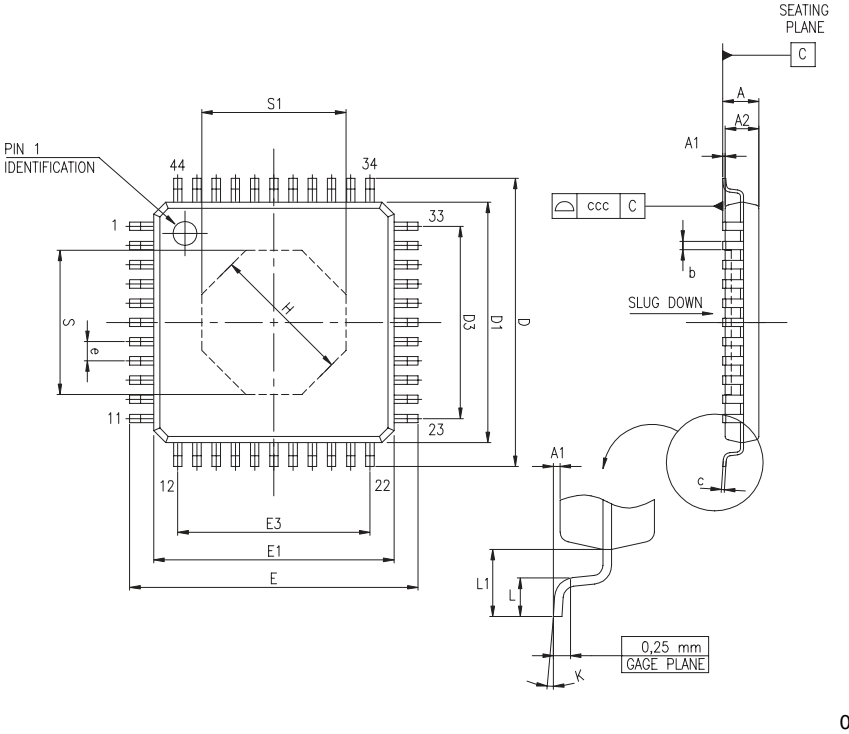


Table 12. Revision History

Date	Revision	Description of Changes
January 2004	4	Migration from ST-Press to EDOCS DMS.
24-Nov-2005	5	Removed “Packet Mode” function. Inserted new Paragraph 3.8. on Crystal Oscillator. Added ECOPACK information.