Rochester Electronics®

Datasheet

IM6654

4096 Bit CMOS UV EPROM

The Harris IM6654 is a fully decoded 4096 bit CMOS electrically programmable ROM (EPROM) fabricated with Harris' advanced CMOS processing technology. In all static states this device exhibits the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and chip select functions simplify system interfacing requirements.

The IM6654 is specifically designed for program development applications where rapid turn-around for program changes is required. The device may be erased by exposing its transparent lid to ultra-violet light, and then reprogrammed.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

HARRIS SEMICONDUCTOR

IM6654

January 1992

4096 Bit CMOS UV EPROM

Features

- Organization ..... 512 x 8
- Low Power ..... 770µW Max Standby
- High Speed
  - Access Time for IM6654-AI 300ns 10V
  - Access Time for IM6654-1I 450ns 5V
- Single Supply Operation 5V
- UV Erasable
- Synchronous Operation for Low Power Dissipation
- Three-State Outputs and Chip Select for Easy System Expansion

Description

The Harris IM6654 is a fully decoded 4096 bit CMOS electrically programmable ROM (EPROM) fabricated with Harris' advanced CMOS processing technology. In all static states this device exhibits the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and chip select functions simplify system interfacing requirements.

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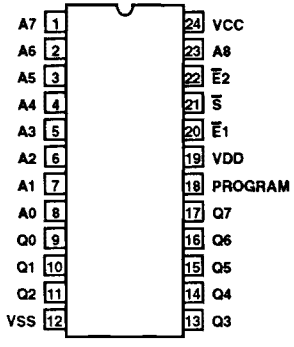
Ordering Information

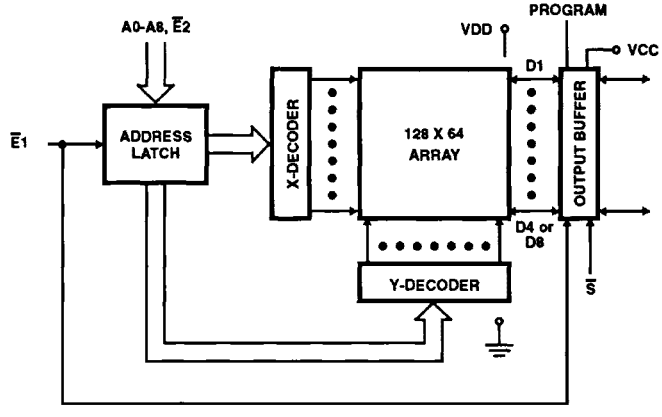
PACKAGE	TEMPERATURE RANGE	5V	10V
Ceramic DIP	-40°C to +85°C	IM6654IJG	IM6654AIJG
		IM6654-1IJG	-
	-55°C to+125°C	IM6654MJG	IM6654AMJG

Pinout

24 LEAD DIP
TOP VIEW



Block Diagram



File Number 3015

Program Mode Operation

Initially, all 4096 bits of the EPROM are in the logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode for all EPROMs, VCC and VDD are tied together to a +5V operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at VDD -2V minimum. Low logic levels must be set at VSS +0.8V maximum. Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ($\overline{S}$) pins are set high. The address is latched by the downward edge on the strobe line ($\overline{E}1$)). During valid DATA IN time, the PROGRAM pin is pulsed from VDD to -40V. This pulse initiates the programming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. PULSE RISE AND FALL TIMES MUST NOT BE FASTER THAN 5μs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences is recommended.

Programming System Characteristics

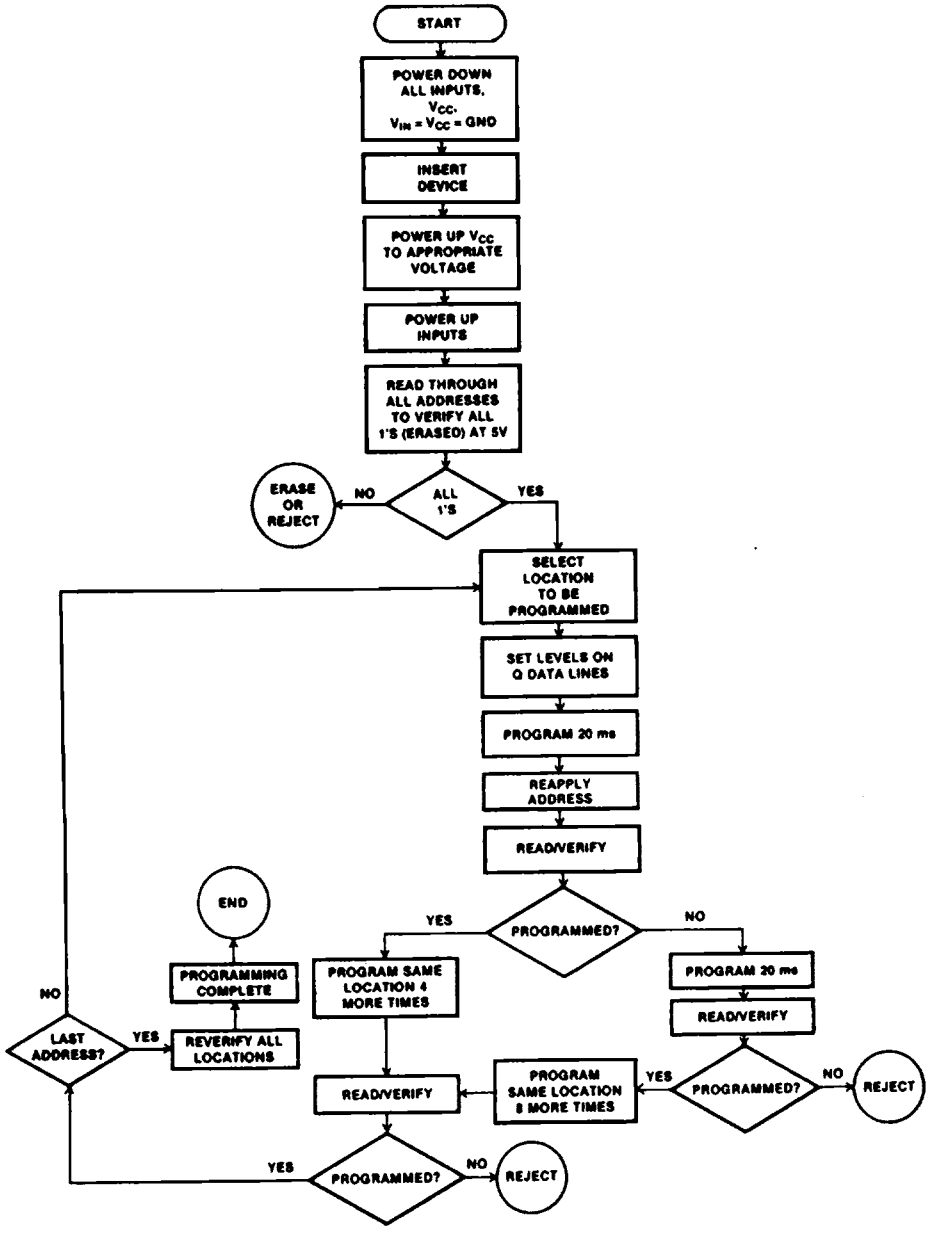
1. During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
2. The programming pin is driven from VDD to -40 volts (±2V) by pulses of 20 milliseconds duration. These pulses should be applied in the sequence shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
3. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins. Both "A" (10V) and non "A" EPROMs are programmed at VCC, VDD of 5V ±5%.
4. Programming is to be done at room temperature.

Erasing Procedure

The IM6654 is erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 10W sec/cm^2. The lamps should be used without short-wave filters, and the IM6654 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before reprogramming.

The erasing effect of UV light is cumulative. Care should be taken to protect EPROMs from exposure to direct sunlight or fluorescent lamps radiating UV light in the 2000Å to 4000Å range.

Programming Flow Chart



DC Characteristics for Programming Operation VCC = VDD = 5V ±5% VSS = 0V, T_A = +25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
IPROG	Program Pin Load Current		-	80	100	mA
VPROG	Programming Pulse Amplitude		-38	-40	-42	V
ICC	VCC Current		-	0.1	5	mA
IDD	VDD Current		-	40	100	mA
VIHA	Address Input High Voltage		VDD-2.0	-	-	V
VILA	Address Input Low Voltage		-	-	0.8	V
VIH	Data Input High Voltage		VDD-2.0	-	-	V
VIL	Data Input Low Voltage		-	-	0.8	V

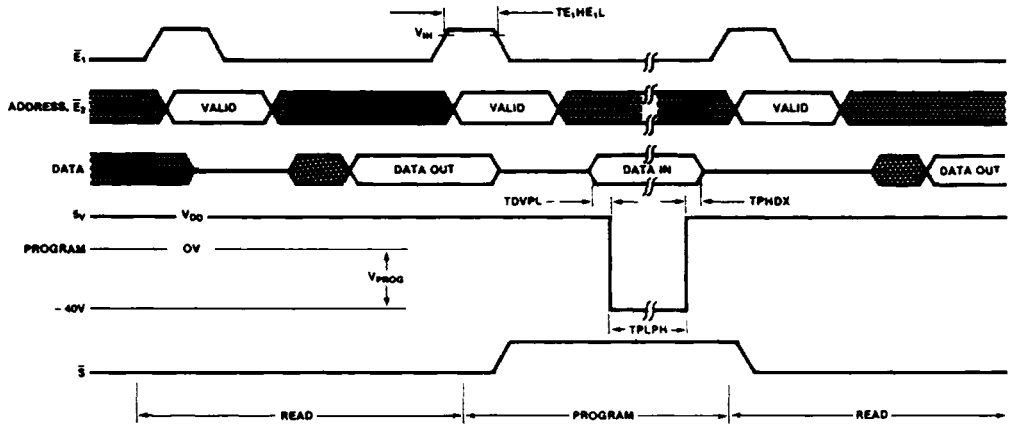
AC Characteristics for Programming Operation VCC = VDD = 5V ±5% VSS = 0V, T_A = +25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TPLPH	Program Pulse Width	trise = tfall = 5µs	18	20	22	ms
	Program Pulse Duty Cycle		-	-	75%	
TDVPL	Data Setup Time		9	-	-	µs
TPHDX	Data Hold Time		9	-	-	µs
TE1HE1L	Strobe Pulse Width		150	-	-	ns
TAVE1L	Address Setup Time		0	-	-	ns
TE1LE1X	Address Hold Time		100	-	-	ns
TE1LQV	Access Time		-	-	1000	ns

Pin Description

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1-8, 23	A0-A7, A8	-	Address Lines
9-11, 13-17	Q0-Q7	-	Data Out Lines
12	VSS	-	Negative Supply
18	Program	-	Programming Pulse Input
19	VDD	-	Chip Positive Supply, Normally Tied to VCC
20	$\overline{E}1$	L	Strobe Line, Latches Both Address Lines and Chip Enable $\overline{E}2$
21	$\overline{S}$	L	Chip Select Line, Must be Low for Valid Data Out
22	$\overline{E}2$	L	Chip Enable Line, Latched by Chip Enable $\overline{E}1$
24	VCC	-	Output Buffer Positive Supply

Read and Program Cycle Timing



Read Mode Operation

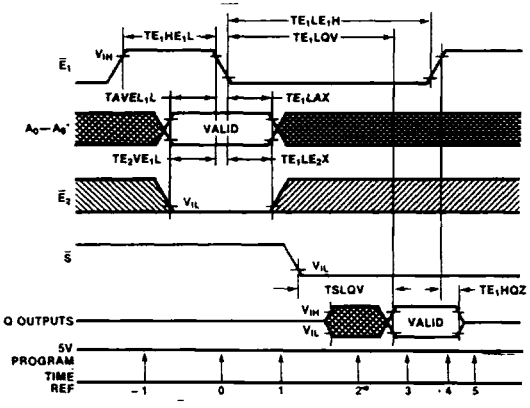
In a typical READ operation address lines and chip enable $\overline{E}2$ are latched by the falling edge of chip enable $\overline{E}1$ (T=0). Valid data appears at the outputs one access time (TELQV) later, provided level-sensitive chip select line $\overline{S}$ is low (T=3). Data remains valid until either $\overline{E}1$ or $\overline{S}$ returns to a high level (T=4). Outputs are then forced to a high-Z state.

Address lines and $\overline{E}2$ must be valid one setup time before (TAVEL), and one hold time after (TELAX), the falling edge of $\overline{E}1$ starting the read cycle. Before becoming valid, Q output lines become active (T=2). The Q output lines return to a high-Z state one output disable time (TE1HQZ) after any rising edge on $\overline{E}1$ or $\overline{S}$.

The program line remains high throughout the READ cycle.

Chip enable line $\overline{E}1$ must remain high one minimum positive pulse width (TEHEL) before the next cycle can begin.

Read Cycle Timing



FUNCTION TABLE

TIME REFERENCE	INPUTS				OUTPUTS	NOTES
	$\overline{E}1$	$\overline{E}2$	$\overline{S}$	A	Q	
-1	H	X	X	X	Z	Device Inactive
0	↘	L	X	V	Z	Cycle Begins; Addresses, $\overline{E}2$ Latched
1	L	X	X	X	Z	Internal Operations Only
2	L	X	L	X	A	Outputs Active Under Control of $\overline{E}1$, $\overline{S}$
3	L	X	L	X	V	Outputs Valid After Access Time
4	↗	X	L	X	V	Read Complete
5	H	X	X	X	Z	Cycle Ends (Same as -1)

Absolute Maximum Ratings (IM6654 I, -1I, M)

Supply Voltages
- VDD - VSS ..... +8.0V
- VCC - VSS ..... +8.0V

Input or Output Voltage..... VSS-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s)..... +300°C

Operating Temperature Range (T_A)
- Industrial ..... -40°C to +85°C
- Military..... -55°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Characteristics VCC = VDD = 5V ±10% VSS = 0V, T_A = Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	IM6654 I, -1I, M		UNITS
			MIN	MAX	
VIH	Logical "1" Input Voltage	$\overline{E}1$, $\overline{S}$	VDD - 2.0	-	V
		Address Pins	2.7	-	V
VIL	Logical "0" Input Voltage	-	-	0.8	V
II	Input Leakage	GND ≤ VIN ≤ VDD	-1.0	1.0	µA
VOH	Logical "1" Output Voltage	IOH = -0.2mA	2.4	-	V
VOL	Logical "0" Output Voltage	IOL = 2.0mA	-	0.45	V
IOLK	Output Leakage	GND ≤ VO ≤ VCC	-1.0	1.0	µA
ISTBY	Standby Supply Current	VIN = VDD	-	100	µA
ICC	Standby Supply Current	VIN = VDD	-	40	µA
IDD	Operating Supply Current (1)	f = 1MHz		6.0	mA
CI	Input Capacitance	Note 1		7.0	pF
CO	Output Capacitance	Note 1		10.0	pF

NOTE: 1. For design reference only, not 100% tested.

AC Electrical Characteristics VCC = VDD = 5V ±10% VSS = 0V, CL = 50pF, T_A = Operating Temperature Range

SYMBOL	PARAMETER	IM6654 -1I		IM6654 I		IM6654 M		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
TE1LQV	Access Time From $\overline{E}1$	-	450	-	550	-	600	ns
TSLQV	Output Enable Time	-	110	-	140	-	150	ns
TE1HQZ	Output Disable Time	-	110	-	140	-	150	ns
TE1HE1L	$\overline{E}1$ Pulse Width (Positive)	130	-	150	-	150	-	ns
TE1LE1H	$\overline{E}1$ Pulse Width (Negative)	450	-	550	-	600	-	ns
TAVE1L	Address Setup Time	0	-	0	-	0	-	ns
TE1LAX	Address Hold Time	80	-	100	-	100	-	ns
TE2VE1L	Chip Enable Setup Time	0	-	0	-	0	-	ns
TE1LE2X	Chip Enable Hold Time	80	-	100	-	100	-	ns

Absolute Maximum Ratings (IM6654AI, AM)

Supply Voltages
- VDD - VSS ..... +11.0V
- VCC - VSS ..... +11.0V

Input or Output Voltage ..... VSS-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Operating Temperature Range (T_A)
- Industrial ..... -40°C to +85°C
- Military ..... -55°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Characteristics

VCC = VDD = 4.5V to 10.5V VSS = 0V, T_A = Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	IM6654 I, AM		UNITS
			MIN	MAX	
VIH	Logical "1" Input Voltage	$\overline{E1}$, $\overline{S}$	VDD - 2.0	-	V
		Address Pins	VDD - 2.0	-	V
VIL	Logical "0" Input Voltage	-	-	0.8	V
II	Input Leakage	GND ≤ VIN ≤ VDD	-1.0	1.0	µA
VOH	Logical "1" Output Voltage	IOUT = 0 (Note 1)	VCC - 0.01	-	V
VOL	Logical "0" Output Voltage	IOUT = 0 (Note 1)	-	VSS+0.01	V
IOLK	Output Leakage	VSS ≤ VO ≤ VCC	-1.0	1.0	µA
ISTBY	Standby Supply Current	VIN = VDD	-	100	µA
ICC	Standby Supply Current	VIN = VDD	-	40	µA
IDD	Operating Supply Current (1)	f = 1MHz	-	12	mA
CI	Input Capacitance	Note 1	-	7.0	pF
CO	Output Capacitance	Note 1	-	10.0	pF

NOTE: 1. For design reference only, not 100% tested.

AC Electrical Characteristics

VCC = VDD = 5V ±10% VSS = 0V, CL = 50pF, T_A = Operating Temperature Range

SYMBOL	PARAMETER	IM6654 AI		IM6654 AM		UNITS
		MIN	MAX	MIN	MAX	
TE1LQV	Access Time From $\overline{E1}$	-	300	-	350	ns
TSLQV	Output Enable Time	-	60	-	70	ns
TE1HQZ	Output Disable Time	-	60	-	70	ns
TE1HE1L	$\overline{E1}$ Pulse Width (Positive)	125	-	125	-	ns
TE1LE1H	$\overline{E1}$ Pulse Width (Negative)	300	-	350	-	ns
TAVE1L	Address Setup Time	0	-	0	-	ns
TE1LAX	Address Hold Time	60	-	60	-	ns
TE2VE1L	Chip Enable Setup Time	0	-	0	-	ns
TE1LE2X	Chip Enable Hold Time	60	-	60	-	ns

Using IM6654 CMOS EPROM to Extend Program Memory