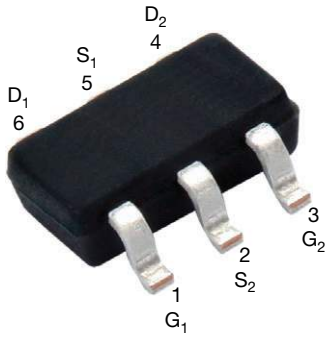
Automotive N- and P-Channel 20 V (D-S) MOSFET

TSOP-6 Dual



Top View

FEATURES

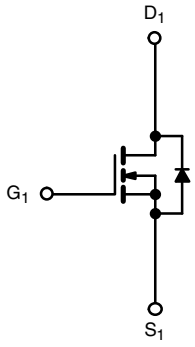
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

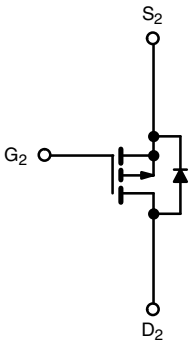
Pb-free

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET



P-Channel MOSFET

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V_{DS} (V)	20	-20
$R_{DS(on)}$ (Ω) at V_{GS} = ± 4.5 V	0.077	0.166
$R_{DS(on)}$ (Ω) at V_{GS} = ± 2.5 V	0.120	0.318
I_D (A)	3.57	-2.5
Configuration	N- and p-pair	

ORDERING INFORMATION	
Package	TSOP-6 Dual
Lead (Pb)-free and halogen-free	SQ3585EV (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage		V_{DS}	20	-20	V
Gate-source voltage		V_{GS}	± 12	± 12	
Continuous drain current	T_C = 25 °C	I_D	3.57	-2.5	A
	T_C = 125 °C		2	-1.45	
Pulsed drain current		I_{DM}	12	-10	
Continuous source current (diode conduction)		I_S	2.1	-2.1	
Maximum power dissipation	T_C = 25 °C	P_D	1.67	1.67	W
	T_C = 125 °C		0.56	0.56	
Unclamped inductive surge UIS		I_{AV}	3.3	3	A
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175		°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
			MAX.	MAX.	
Maximum junction-to-ambient [a]	Steady state	R_{thJA}	150	150	°C/W
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	90	90	

Note

a. Surface mounted on 1" x 1" FR4 board

SPECIFICATIONS (T_J = 25°C, unless otherwise noted)								
PARAMETER	**SYMBOL**	**TEST CONDITIONS**			**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static								
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		N-Ch	0.6	-	1.5	V
		V_{DS} = V_{GS}, I_D = -250 µA		P-Ch	-0.6	-	-1.5	
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V		N-Ch	-	-	± 100	nA
				P-Ch	-	-	± 100	
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 20 V	N-Ch	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = -20 V	P-Ch	-	-	-1	
		V_{GS} = 0 V	V_{DS} = 20 V, T_J = 55 °C	N-Ch	-	-	5	
		V_{GS} = 0 V	V_{DS} = -20 V, T_J = 55 °C	P-Ch	-	-	-5	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 4.5 V	V_{DS} ≥ 5 V	N-Ch	5	-	-	A
		V_{GS} = -4.5 V	V_{DS} ≤ -5 V	P-Ch	-5	-	-	
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V	I_D = 1 A	N-Ch	-	0.049	0.077	Ω
		V_{GS} = -4.5 V	I_D = -1 A	P-Ch	-	0.140	0.166	
		V_{GS} = 2.5 V	I_D = 1 A	N-Ch	-	0.066	0.120	
		V_{GS} = -2.5 V	I_D = -1 A	P-Ch	-	0.265	0.318	
Forward transconductance [a]	g_{fs}	V_{DS} = 5 V, I_D = 1 A		N-Ch	-	10	-	S
		V_{DS} = -5 V, I_D = -1 A		P-Ch	-	3	-	
Diode forward voltage [a]	V_{SD}	I_S = 1.05 A, V_{GS} = 0 V		N-Ch	-	0.80	1.10	V
		I_S = -1.05 A, V_{GS} = 0 V		P-Ch	-	-0.83	-1.10	
Dynamic [b]								
Total gate charge	Q_g	V_{GS} = 4.5 V	V_{DS} = 10 V, I_D = 1 A	N-Ch	-	1.8	2.5	nC
		V_{GS} = -4.5 V	V_{DS} = -10 V, I_D = -1 A	P-Ch	-	2.4	3.5	
Gate-source charge	Q_{gs}	V_{GS} = 4.5 V	V_{DS} = 10 V, I_D = 1 A	N-Ch	-	0.3	-	
		V_{GS} = -4.5 V	V_{DS} = -10 V, I_D = -1 A	P-Ch	-	0.4	-	
Gate-drain charge	Q_{gd}	V_{GS} = 4.5 V	V_{DS} = 10 V, I_D = 1 A	N-Ch	-	0.4	-	
		V_{GS} = -4.5 V	V_{DS} = -10 V, I_D = -1 A	P-Ch	-	0.7	-	
Gate resistance	R_g	f = 1 MHz		N-Ch	3.4	-	9.1	Ω
				P-Ch	3.4	-	9.1	
Turn-on delay time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_g = 1 kΩ P-Channel V_{DD} = -10 V, R_L = 10 Ω I_D ≅ -1 A, V_{GEN} = -10 V, R_g = 1 kΩ		N-Ch	-	9	12	ns
				P-Ch	-	7	11	
Rise time	t_r			N-Ch	-	15	19	
				P-Ch	-	16	22	
Turn-off delay time	$t_{d(off)}$			N-Ch	-	22	28	
				P-Ch	-	29	40	
Fall time	t_f			N-Ch	-	8	12	
				P-Ch	-	14	24	

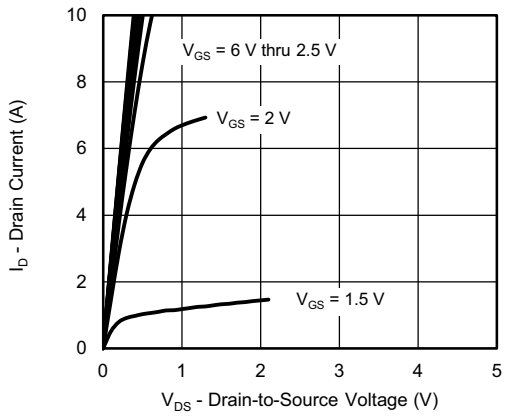
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

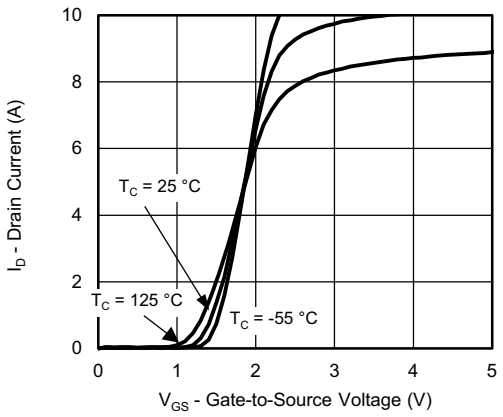
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

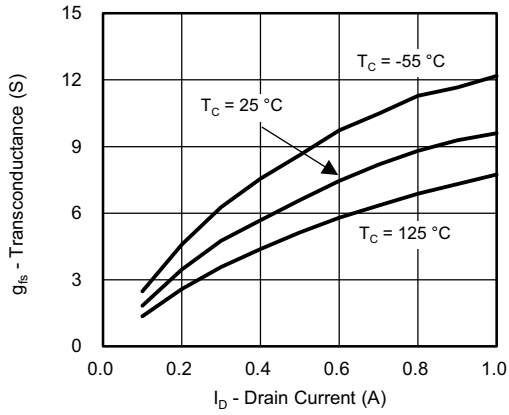
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



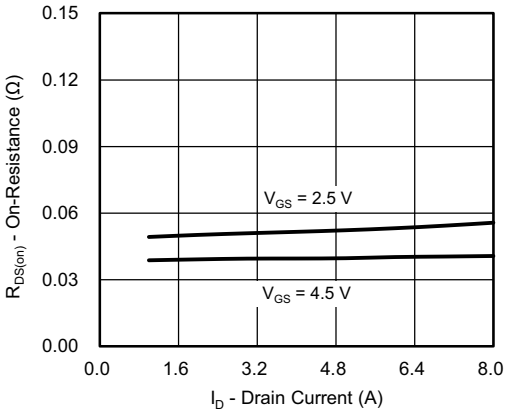
Output Characteristics



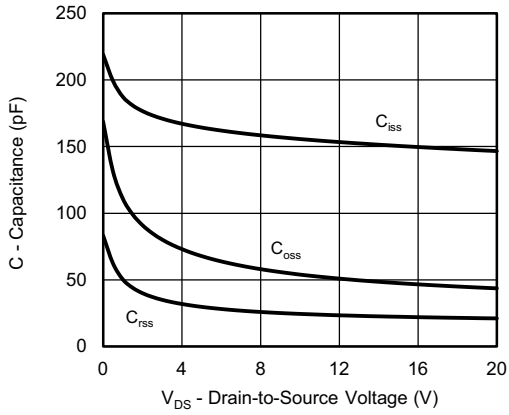
Transfer Characteristics



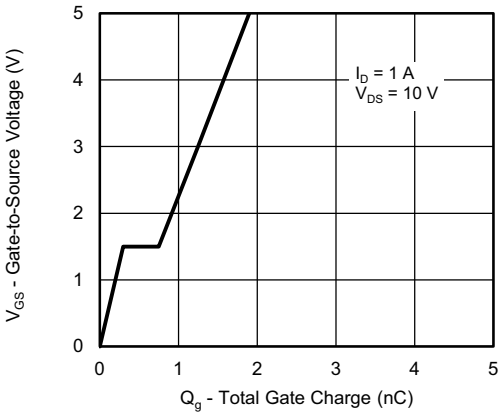
Transconductance



On-Resistance vs. Drain Current

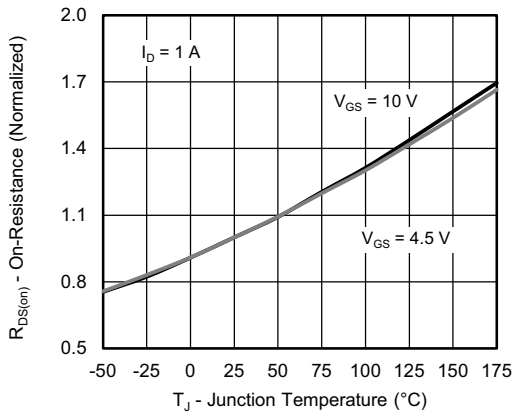


Capacitance

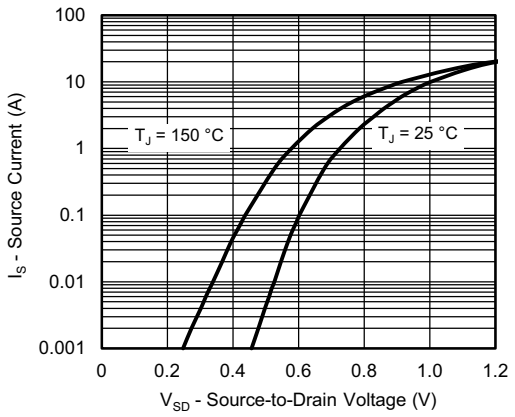


Gate Charge

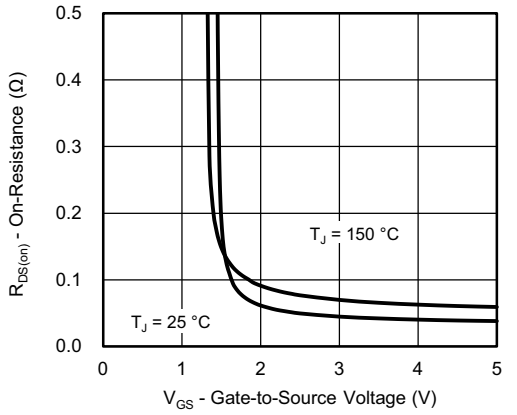
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



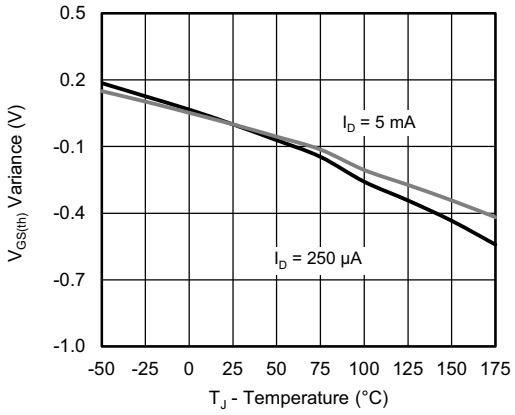
On-Resistance vs. Junction Temperature



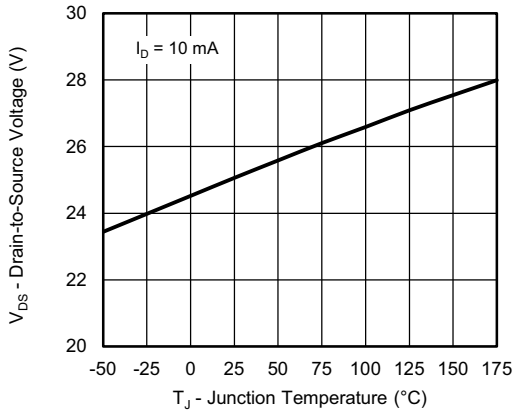
Source-Drain Diode Forward Voltage



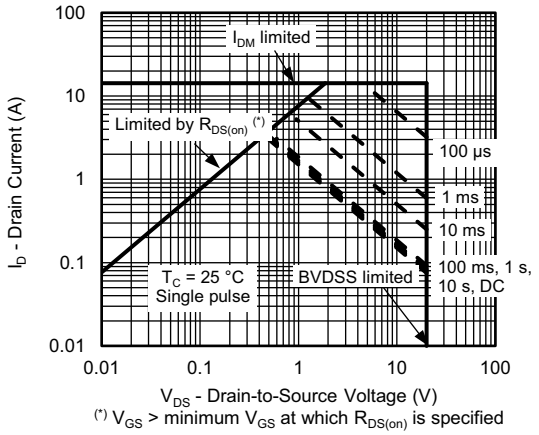
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

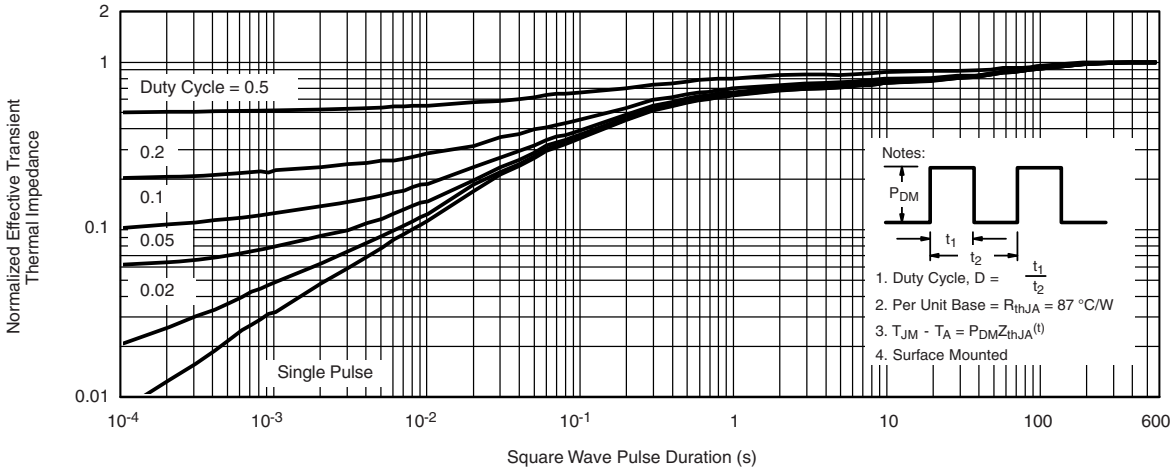


Drain Source Breakdown vs. Junction Temperature

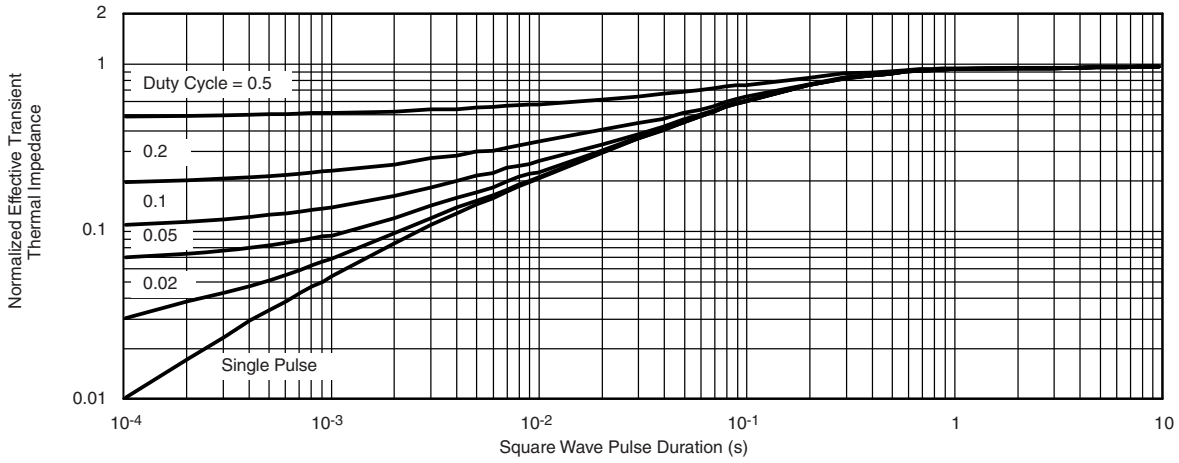


Safe Operating Area

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

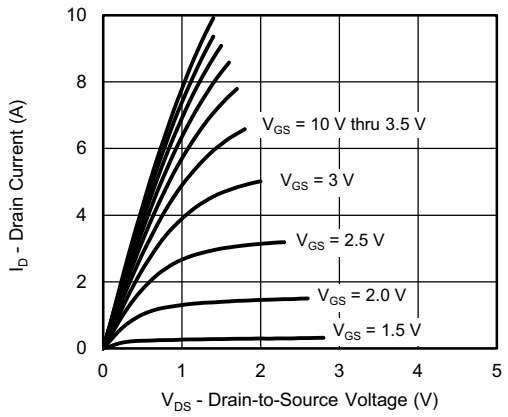


Normalized Thermal Transient Impedance, Junction-to-Ambient

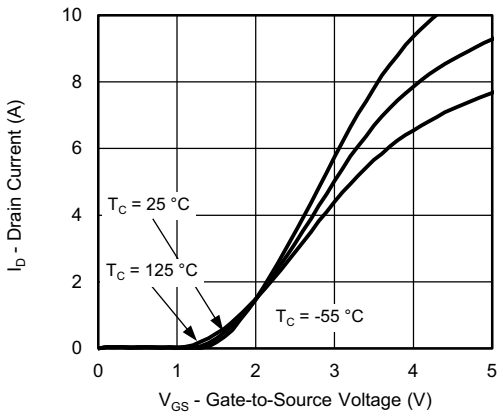


Normalized Thermal Transient Impedance, Junction-to-Foot

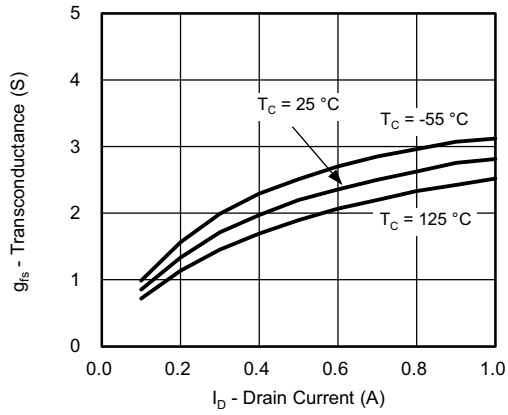
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



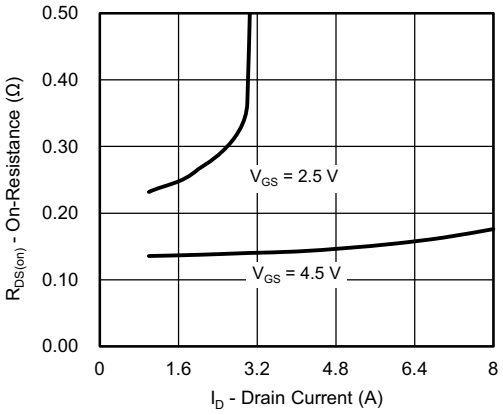
Output Characteristics



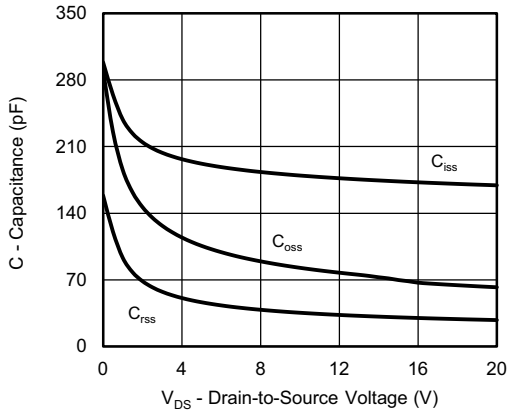
Transfer Characteristics



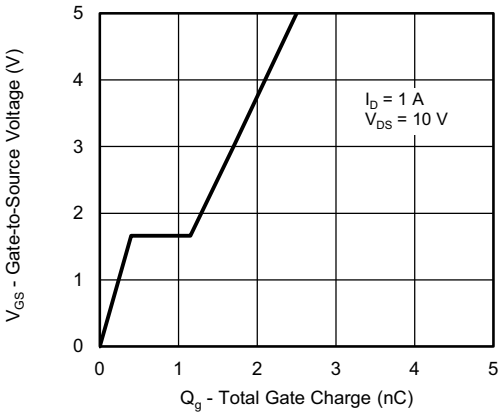
Transconductance



On-Resistance vs. Drain Current

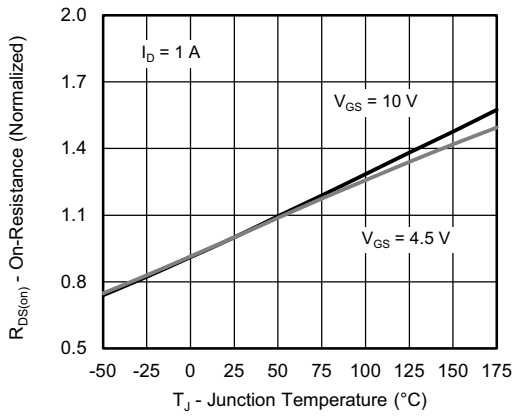


Capacitance

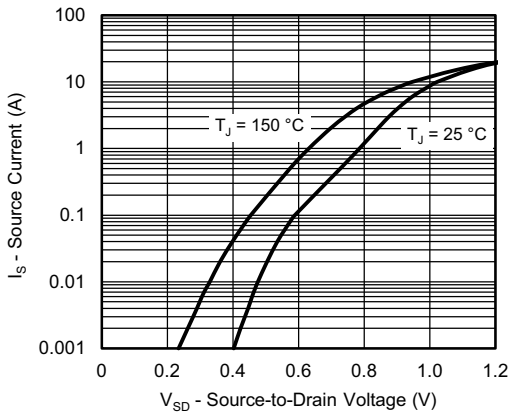


Gate Charge

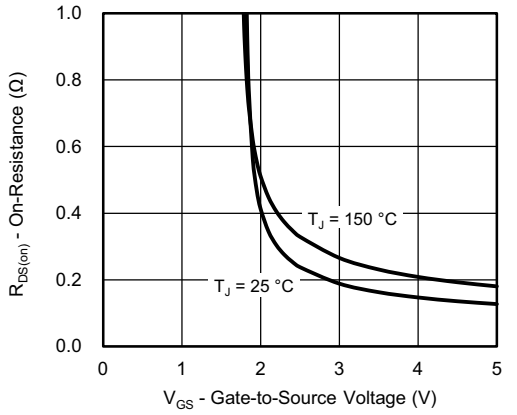
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



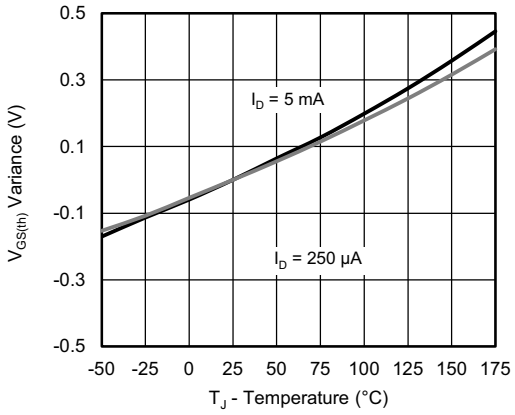
On-Resistance vs. Junction Temperature



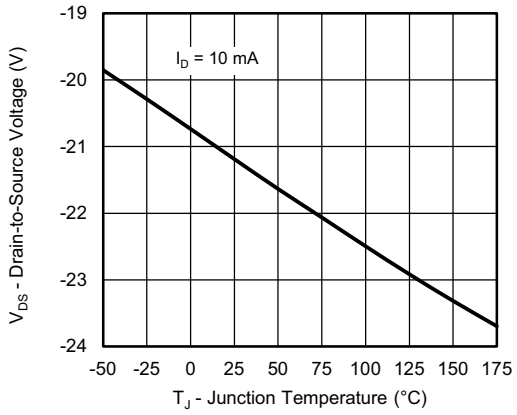
Source-Drain Diode Forward Voltage



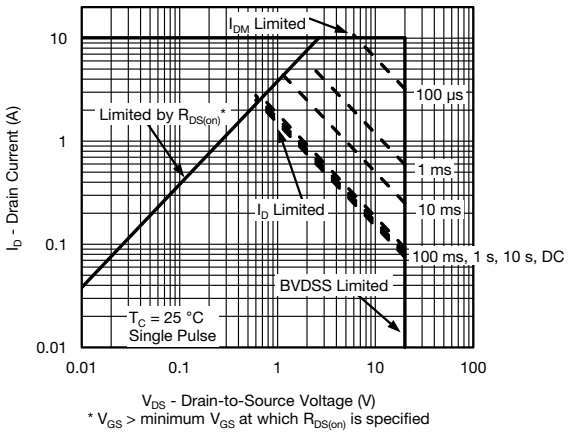
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

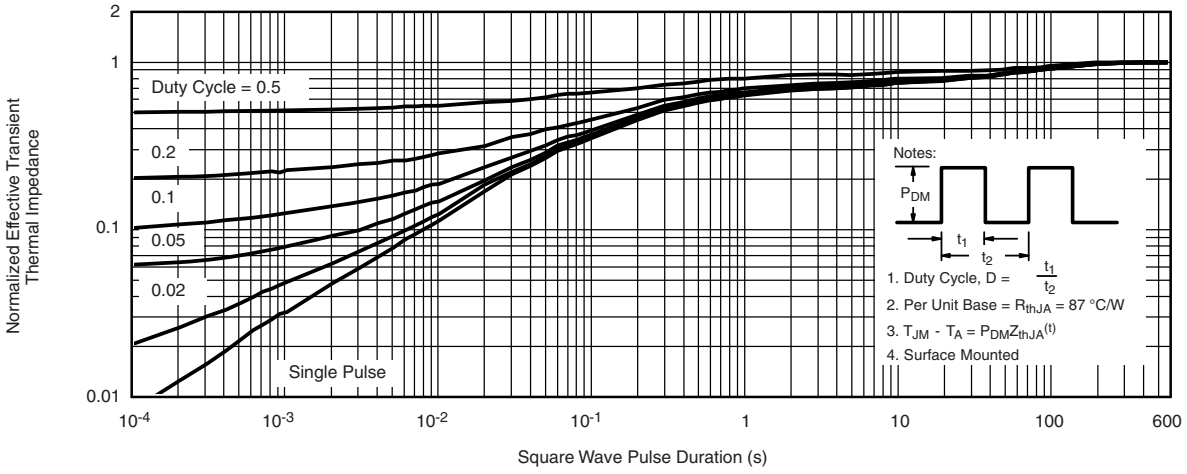


Drain Source Breakdown vs. Junction Temperature

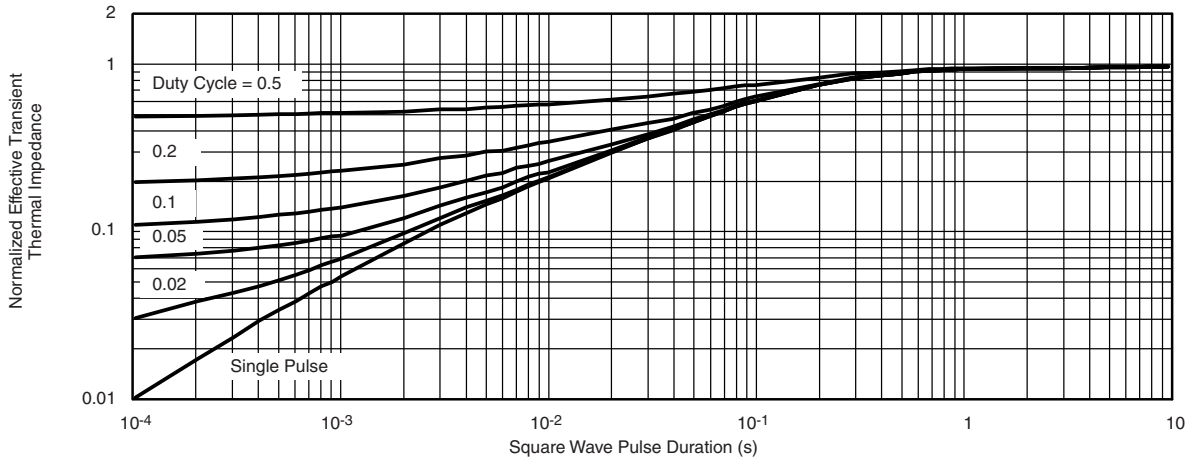


Safe Operating Area

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



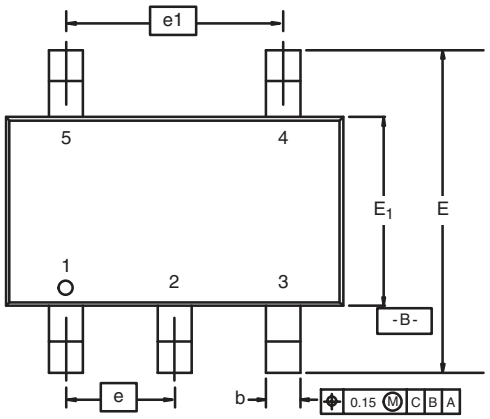
Normalized Thermal Transient Impedance, Junction-to-Ambient



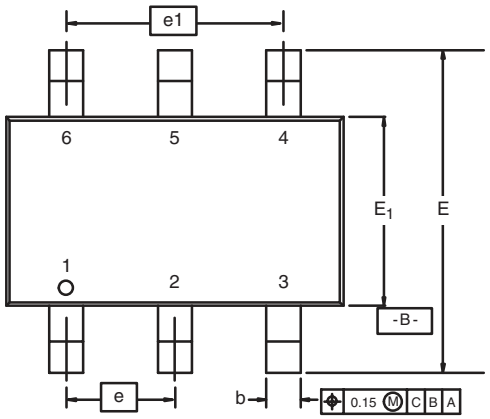
Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75126.

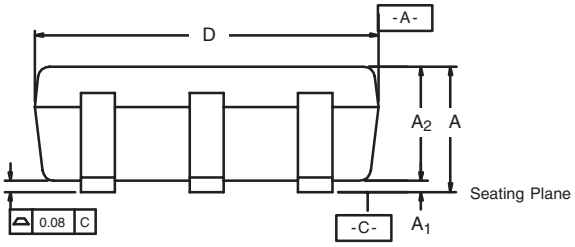
TSOP: 5/6–LEAD
JEDEC Part Number: MO-193C

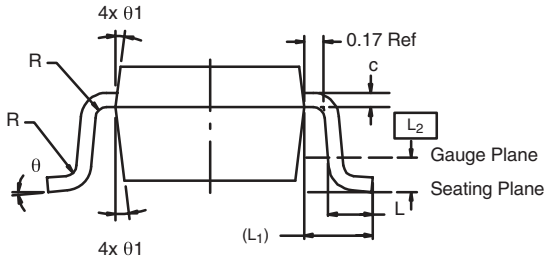


5-LEAD TSOP



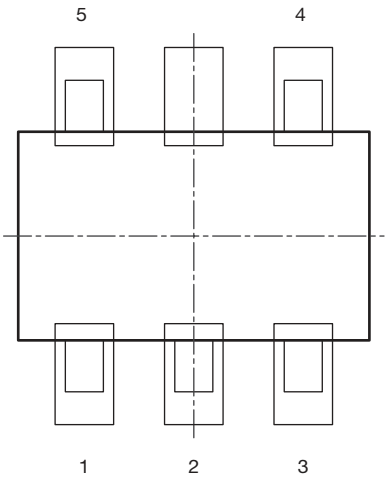
6-LEAD TSOP



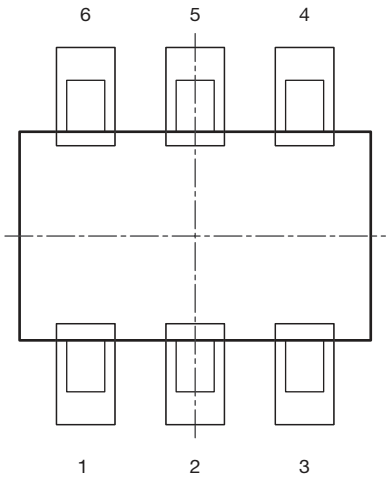


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A_1	0.01	-	0.10	0.0004	-	0.004
A_2	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e_1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

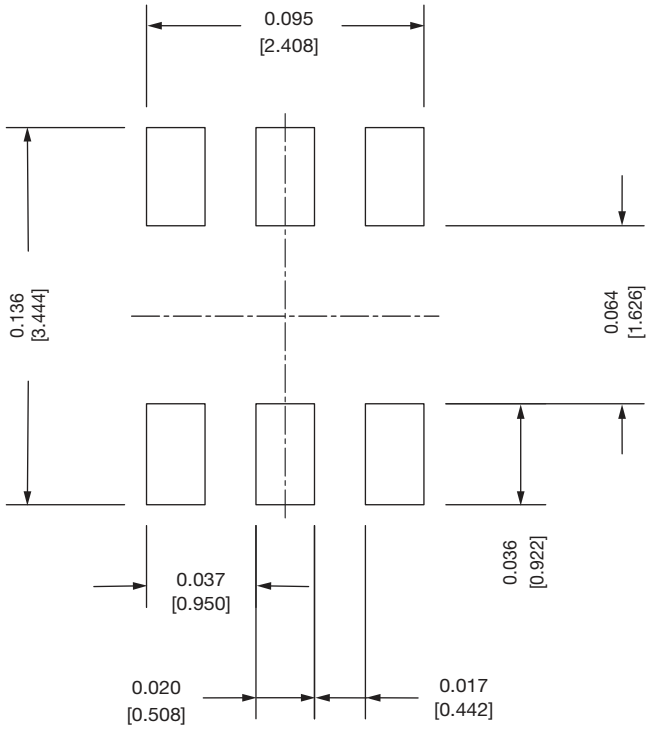
Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L



Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010

Disclaimer

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