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July 1997 Revised July 2002

FST16211 24-Bit Bus Switch

General Description

The Fairchild Switch FST16211 provides 24-bits of highspeed CMOS TTL-compatible bus switching. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 12-bit or 24-bit bus switch. When $\overline{\text{OE}}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{\text{OE}}_2$ is LOW, Port 2A is connected to Port 2B. When $\overline{\text{OE}}_{1/2}$ is HIGH, a high impedance state exists between the A and B Ports.

Features

- \blacksquare 4 Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

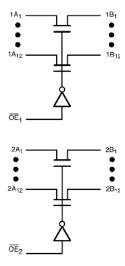
Ordering Code:

Order Number	Package Number	Package Description
FST16211G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
FST16211MEA (Note 2)	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
FST16211MTD (Note 2)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 1: Ordering code "G" indicates Trays.

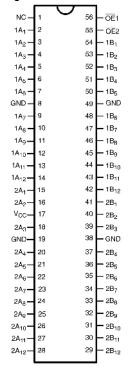
Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram

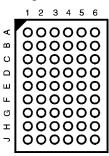


Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Name	Description
\overline{OE}_1 , \overline{OE}_2	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

FBGA Pin Assignments

		1	2	3	4	5	6
Α		1A ₂	1A ₁	NC	OE ₂	1B ₁	1B ₂
В		1A ₄	1A ₃	1A ₇	OE ₁	1B ₃	1B ₄
С		1A ₆	1A ₅	GND	1B ₇	1B ₅	1B ₆
D	1	1A ₁₀	1A ₉	1A ₈	1B ₈	1B ₉	1B ₁₀
Е		1A ₁₂	1A ₁₁	2A ₁	2B ₁	1B ₁₁	1B ₁₂
F		2A ₄	2A ₃	2A ₂	2B ₂	2B ₃	2B ₄
G	i	2A ₆	2A ₅	V _{CC}	GND	2B ₅	2B ₆
Н		2A ₈	2A ₇	2A ₉	2B ₉	2B ₇	2B ₈
J		2A ₁₂	2A ₁₁	2A ₁₀	2B ₁₀	2B ₁₁	2B ₁₂

Truth Table

Inp	uts	Inputs/Outputs			
\overline{OE}_1 \overline{OE}_2		1A, 1B	2A, 2B		
L	L	1A = 1B	2A = 2B		
L	Н	1A = 1B	Z		
Н	L	Z	2A = 2B		
Н	Н	Z	Z		

Absolute Maximum Ratings(Note 3)

Recommended Operating Conditions (Note 6)

 $\begin{array}{lll} \mbox{Power Supply Operating (V_{CC})} & 4.0\mbox{V to } 5.5\mbox{V} \\ \mbox{Input Voltage (V_{IN})} & 0\mbox{V to } 5.5\mbox{V} \\ \mbox{Output Voltage (V_{OUT})} & 0\mbox{V to } 5.5\mbox{V} \\ \end{array}$

Input Rise and Fall Time (t_r, t_f)

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: V_S is the voltage observed/applied at either A or B Ports across the switch.

Note 5: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 6: Unused control inputs must be held HIGH or LOW. They may not float

DC Electrical Characteristics

	Parameter	V _{CC} (V)	T _A = -40 °C to +85 °C				
Symbol			Min	Typ (Note 7)	Max	Units	Conditions
V _{IK}	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18 \text{ mA}$
V _{IH}	HIGH Level Input Voltage	4.0-5.5	2.0			V	
V _{IL}	LOW Level Input Voltage	4.0-5.5			0.8	V	
ı	Input Leakage Current	5.5			±1.0	μА	$0 \le V_{IN} \le 5.5V$
		0			10	μΑ	V _{IN} = 5.5V
OZ	OFF-STATE Leakage Current	5.5			±1.0	μΑ	$0 \le A, B \le V_{CC}$
R _{ON}	Switch On Resistance	4.5		4	7	Ω	$V_{IN} = 0V, I_{IN} = 64 \text{ mA}$
	(Note 8)	4.5		4	7	Ω	$V_{IN} = 0V, I_{IN} = 30 \text{ mA}$
		4.5		8	12	Ω	$V_{IN} = 2.4V, I_{IN} = 15 \text{ mA}$
		4.0		11	20	Ω	$V_{IN} = 2.4V$, $I_{IN} = 15 \text{ mA}$
СС	Quiescent Supply Current	5.5			3	μΑ	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
ı I _{CC}	Increase in I _{CC} per Input	5.5			2.5	mA	One Input at 3.4V
							Other Inputs at V _{CC} or GND

Note 7: Typical values are at $V_{CC} = 5.0V$ and $T_A = +25^{\circ}C$

Note 8: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40$ °C to +85 °C, $C_L = 50$ pF, $R_U = R_D = 500$ Ω				Units	Conditions	Figure
Symbol	rarameter	$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$		Onits	Conditions	Number
		Min	Max	Min	Max			
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus (Note 9)		0.25		0.25	ns	V _I = OPEN	Figures 1, 2
t _{PZH} , t _{PZL}	Output Enable Time	1.5	6.0		6.5	ns	$V_I = 7V$ for t_{PZL} $V_I = OPEN$ for t_{PZH}	Figures
							$V_I = OPEN$ for t_{PZH}	1, 2
t _{PHZ} , t _{PLZ}	Output Disable Time	1.5	7.0		7.2	ns	$V_I = 7V$ for t_{PLZ} $V_I = OPEN$ for t_{PHZ}	Figures
							$V_I = OPEN$ for t_{PHZ}	1, 2

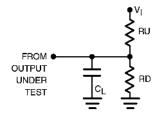
Note 9: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 10)

Symbol	Parameter	Тур	Max	Units	Conditions
C _{IN}	Control Pin Input Capacitance	3		pF	V _{CC} = 5.0V
C _{I/O}	Input/Output Capacitance	6		pF	V_{CC} , $\overline{OE} = 5.0V$

Note 10: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, $t_W = 500 \text{ ns}$

FIGURE 1. AC Test Circuit

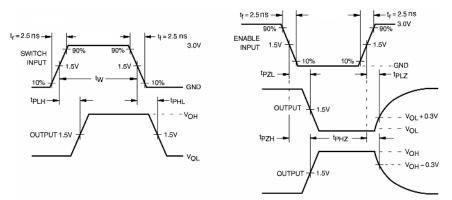
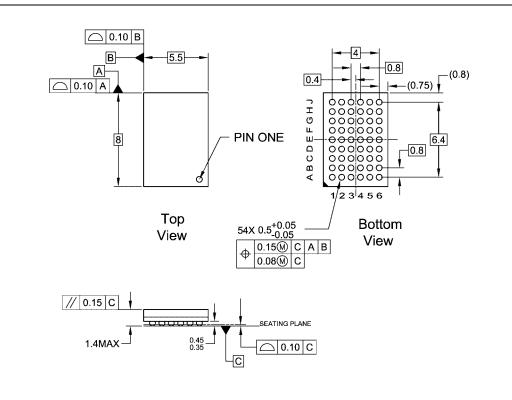


FIGURE 2. AC Waveforms



NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- A. THIS PACKAGE CONFORMS TO JEDEC MU-205

 B. ALL DIMENSIONS IN MILLIMETERS

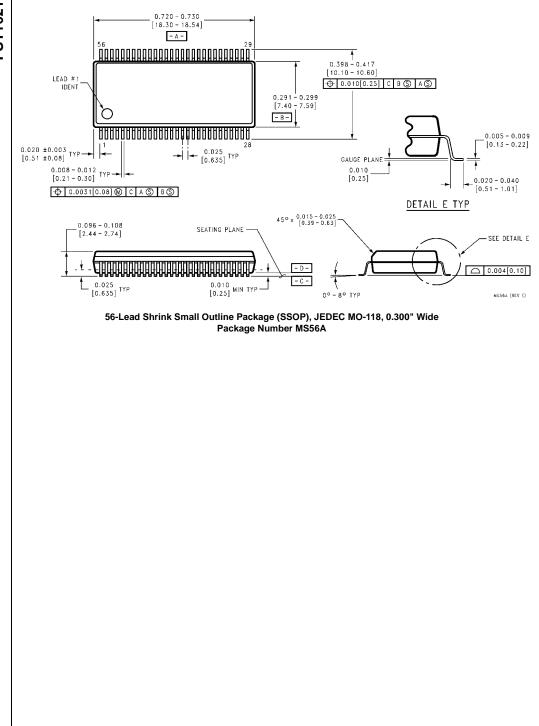
 C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)

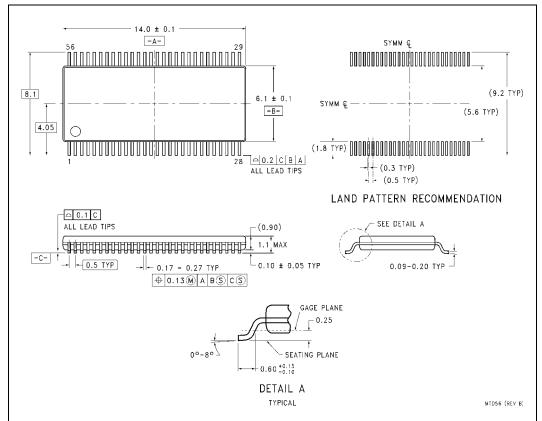
 .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS

 D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide Package Number BGA54A





56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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