February 2006



General Description

FAIRCHILD Semiconductor

This N-Channel UltraFET device has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.

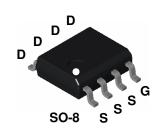
Applications

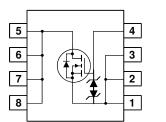




Features

- Max $r_{DS(on)} = 24m\Omega$ at $V_{GS} = 10V$, $I_D = 5.8A$
- Max $r_{DS(on)} = 33m\Omega$ at $V_{GS} = 4.5V$, $I_D = 5.6A$
- ESD protection diode (note 3)
- Low Qgd
- Fast switching speed





MOSFET Maximum Ratings T_{A=25°C} unless otherwise noted

	Parameter			Ratings	Units
Drain-Sour	ce Voltage			50	V
Gate-Source	e Voltage			± 20	V
Drain Curre	ent – Continuous	(Note	1a)	5.8	А
	– Pulsed			40	
Single Puls	e Avalanche Energy			72	mJ
UltraFET D	UltraFET Dissipation for Single Operation (Note 1a)			2.5	W
		(Note 1	lb)	1.2	
		(Note	1c)	1.1	
Operating a	and Storage Junction Te	mperature Rang	je	-55 to 150	°C
I Charac	teristics				
Thermal Re	Resistance, Junction-to-Ambient (Note 1a)		la)	50	°C/W
Thermal Re	esistance, Junction-to-Ar	nbient (Note	1c)	125	
Thermal Re	esistance, Junction-to-Ca	ASE (Note	1)	25	
e Markin	g and Ordering	Informati	on		•
Marking	Device	Package	Reel Size	Tape width	Quantity
	Gate-Source Drain Curree Single Puls UltraFET D Operating a I Charace Thermal Ree Thermal Ree	Drain-Source Voltage Gate-Source Voltage Drain Current – Continuous – Pulsed Single Pulse Avalanche Energy UltraFET Dissipation for Single Ope Operating and Storage Junction Te I Characteristics Thermal Resistance, Junction-to-Ar Thermal Resistance, Junction-to-Ca	Drain-Source Voltage Gate-Source Voltage Drain Current – Continuous - Pulsed Single Pulse Avalanche Energy UltraFET Dissipation for Single Operation (Note 1) (Note 2) Operating and Storage Junction Temperature Range I Characteristics Thermal Resistance, Junction-to-Ambient (Note 2) Unction-to-Ambient (Note 2) Operating Resistance, Junction-to-Case (Note 2)	Drain-Source Voltage Gate-Source Voltage Drain Current – Continuous (Note 1a) – Pulsed Single Pulse Avalanche Energy UltraFET Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c) Operating and Storage Junction Temperature Range I Characteristics Thermal Resistance, Junction-to-Ambient (Note 1a) Thermal Resistance, Junction-to-Ambient (Note 1c)	Drain-Source Voltage50Gate-Source Voltage± 20Drain Current – Continuous(Note 1a)- Pulsed40Single Pulse Avalanche Energy72UltraFET Dissipation for Single Operation (Note 1b) (Note 1c)2.5(Note 1b)1.2(Note 1c)1.1Operating and Storage Junction Temperature Range-55 to 150CharacteristicsThermal Resistance, Junction-to-Ambient (Note 1c)Thermal Resistance, Junction-to-Ambient (Note 1c)125Thermal Resistance, Junction-to-Case (Note 1)25

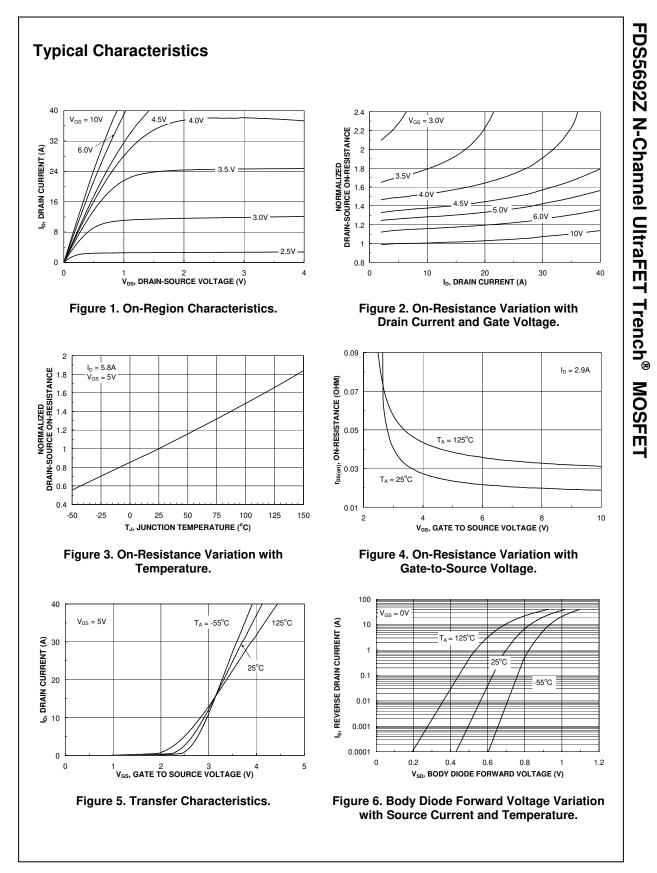
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Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-So	ource Avalanche Ratings			•		•
AS	Drain-Source Avalanche Energy	$V_{DD} = 50 \text{ V}, I_{D} = 12 \text{ A}, L = 1 \text{ mH}$			72	mJ
AS	(Single Pulse) Drain-Source Avalanche Current			12		А
-				12		Λ
	acteristics		50	1		V
BV _{DSS}	Drain–Source Breakdown Voltage Breakdown Voltage Temperature	$V_{GS} = 0 V,$ $I_{D} = 250 \ \mu A$	50			V
ΔT_{J}	Coefficient	$I_D = 250 \ \mu A$, Referenced to $25^{\circ}C$		48		mV/°C
DSS	Zero Gate Voltage Drain Current	$V_{DS} = 40 \text{ V}$ $V_{GS} = 0 \text{ V}$			1	μA
GSS	Gate-Body Leakage	$V_{GS} = \pm 20V, \qquad V_{DS} = 0 V$			± 10	μA
On Char	acteristics (Note 4)	•				
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1	1.6	3	V
$\Delta V_{GS(th)}$	Gate Threshold Voltage	$I_D = 250 \ \mu$ A, Referenced to 25°C		-6		mV/°C
ΔT_{J}	Temperature Coefficient					IIIV/ C
	Static Drain-Source			20	24 33	
DS(on)	On-Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 5.8 \text{ A}, V_{GS} = 10 \text{ V}, I_D = 5.8 \text{ A}, T_J = 125^{\circ}\text{C}$		26 32	33 41	mΩ
Dynamic	Characteristics					1
Dynamic C _{iss}	Input Capacitance	$V_{DS} = 25 V$, $V_{GS} = 0 V$,	1	1025	1	pF
Coss	Output Capacitance	f = 1.0 MHz		150		pF
Crss	Reverse Transfer Capacitance			50		pF
7 _G	Gate Resistance	f = 1.0 MHz		0.79		Ω
	Total Gate Charge, V _{GS} = 10V			18	25	nC
Q _{g(TOT)}	Total Gate Charge, $V_{GS} = 5V$	$V_{DS} = 25V, I_{D} = 5.8A$		10	14	nC
Q _{gs}	Gate-Source Gate Charge			2.8		nC
J _{gd}	Gate-Drain Gate Charge			3.0		nC
Switchin	g Characteristics (Note 4)					
d(on)	Turn-On Delay Time	$V_{\text{DD}} = 25 \text{ V}, \qquad I_{\text{D}} = 5.8 \text{A},$		9	18	ns
	Rise Time	$V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		5	10	ns
d(off)	Turn-Off Delay Time	-		27	43	ns
	Fall Time	-		6	12	ns

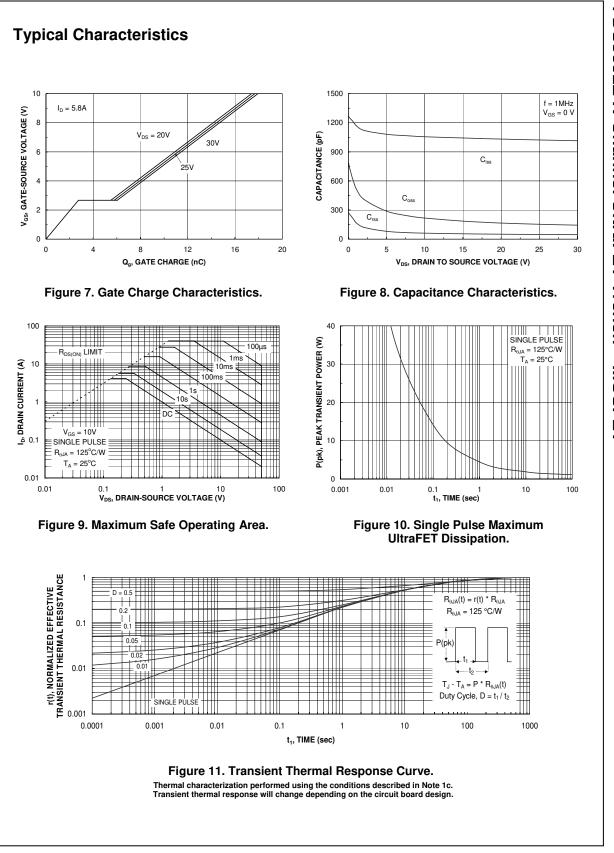
FDS5692Z N-Channel UltraFET Trench[®] MOSFET

VoltageVGS = 0 V,IS = 2.9 A0.751.0VReverse Recovery TimeIF = 6A,dIF/dt = 100A/us24ns	Symbol	Parameter	Test Cor	nditions	Min	Тур	Max	Units
SD Drain–Source Diode Forward Voltage $V_{GS} = 0 V$, $I_S = 5.8 A$ 0.79 1.25 V Reverse Recovery Time rr Reverse Recovery Time Reverse Recovery Charge $I_F = 6A$, $dI_F/dt = 100A/\mu s$ 24 ns Reverse Recovery Charge $I_F = 6A$, $dI_F/dt = 100A/\mu s$ 16 nC And the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{aJC} is guaranteed by design while R_{eCA} is determined by the user's board design. 0.75×100 $I_F = 6A$, $dI_F/dt = 100A/\mu s$ 0.75×100 0.75×100 0.75×100 0.75×100 $I_F = 6A$, $dI_F/dt = 100A/\mu s$ 0.75×100 0.75×100 0.75×100 0.75×100 $I_F = 6A$, 0.75×100 $I_F = 6A$ 0.75×100 $I_F = 6A$ $I_F = 6A$ $I_F = 6A$ $I_F = 6A$ 0.75×100 0.75×100 0.75×100 </th <th>Drain-S</th> <th>ource Diode Characteri</th> <th>stics</th> <th></th> <th>1</th> <th>l</th> <th>L</th> <th>I</th>	Drain-S	ource Diode Characteri	stics		1	l	L	I
Is 2.9 A 0.75 1.0 V Reverse Recovery Time IF 6A, dIF/dt 100 / μ s V rr Reverse Recovery Charge IF 6A, dIF/dt 100 / μ s 24 ns ntes: Rough is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Rough is guaranteed by design while RocA is determined by the user's board design. 0 105°C/W when mounted on a .04 in ² pad of 2 oz copper 0 125°C/W when mounted on a minimum pad. a) 50°C/W when mounted on a 11n ² pad of 2 oz copper b) 105°C/W when mounted on a .04 in ² pad of 2 oz copper c) 125°C/W when mounted on a minimum pad.	SD	Drain–Source Diode Forward		$I_{\rm S} = 5.8 \ A$		0.79	1.25	V
r_r Reverse Recovery Charge $I_F = 6A$, $dI_F/dI = 100A/\mu S$ 16 nC otes: R_{oJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{oJC} is guaranteed by design while R_{oCA} is determined by the user's board design. 000000000000000000000000000000000000		Voltage	$\mathbf{v}_{GS} = 0 \mathbf{v},$	I _S = 2.9 A		0.75	1.0	V
rr Heverse Recovery Charge 16 nC thes: R _{aux} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R _{auc} is guaranteed by design while R _{acA} is determined by the user's board design. Image: Comparison of the provide the drain pins. R _{auc} is guaranteed by design while R _{acA} is determined by the user's board design. Image: Comparison of the provide the drain pins. R _{auc} is guaranteed by design while R _{acA} is determined by the user's board design. Image: Comparison of the provide the drain pins. R _{auc} is guaranteed by design while R _{acA} is determined by the user's board design. Image: Comparison of the provide the drain pins. R _{auc} is guaranteed by design while R _{acA} is determined by the user's board design. Image: Comparison of the provide the drain pins. R _{auc} is guaranteed by design while R _{acA} is determined by the user's board design. Image: Comparison of the provide the drain pins. R _{auc} is guaranteed by design while R _{acA} is determined by the user's board design. Image: Comparison of the pins of the drain pins of the d	r		I⊧ = 6A, dI⊧/dt =	100A/us				
R _{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R _{0JC} is guaranteed by design while R _{0CA} is determined by the user's board design. a) 50°C/W when mounted on a 1in² pad of 2 oz copper b) 105°C/W when mounted on a .04 in² pad of 2 oz copper c) 125°C/W when mounted on a minimum pad.) ^u	Reverse Recovery Charge	1 -) - 1			16		nC
ale 1 : 1 on letter size paper		mounted on a 1in ² pad of 2 oz copper	b) 105°C/W when mounted on a .04	4 in ² ler	c)			ited on a
	Pulse Test:	Pulse Width < 300us. Duty Cycle < 2.0%						
Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0% The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.								



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