

## 1. General description

Planar passivated very sensitive gate Silicon Controlled Rectifier in a SOT54 (TO-92) plastic package.

## 2. Features and benefits

- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Very sensitive gate

## 3. Applications

- Earth leakage circuit breakers or Ground Fault Circuit Interrupters (GFCI)
- Ignition circuits
- Low power latching circuits
- Protection circuits / shut-down circuits: lighting ballasts
- Protection circuits / shut-down circuits: Switched Mode Power Supplies

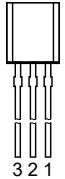


## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RRM}$	repetitive peak reverse voltage		-	-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83\text{ °C}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	0.8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 8.3\text{ ms}$	-	-	10	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	9	A
$T_j$	junction temperature		-	-	125	°C
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	15	33	50	$\mu\text{A}$
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 1\text{ k}\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; <a href="#">Fig. 12</a>	150	-	-	$\text{V}/\mu\text{s}$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 <p>TO-92 (SOT54)</p>	 <p>A  K G sym037</p>
2	G	gate		
3	K	cathode		

## 6. Ordering information

Table 3. Ordering information

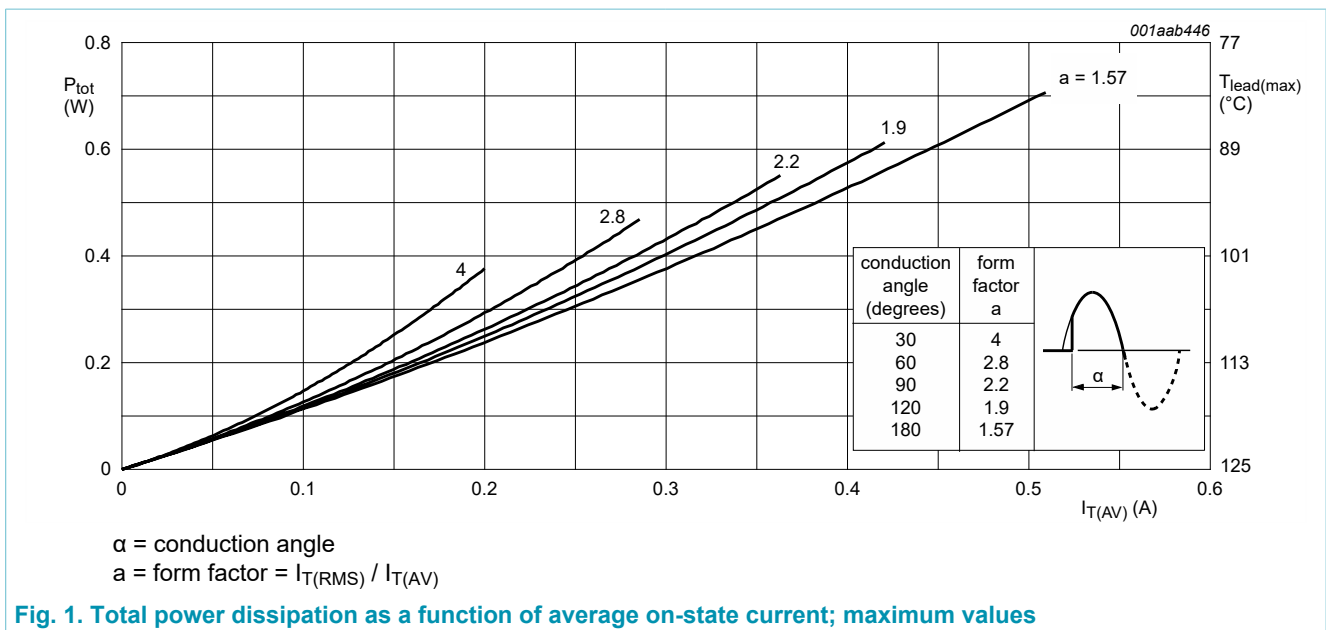
Type number	Package		
	Name	Description	Version
BT169H-L	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	800	V
$V_{RRM}$	repetitive peak reverse voltage		-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$ ; Fig. 1	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$ ; Fig. 2; Fig. 3	-	0.8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 8.3\text{ ms}$	-	10	A
		half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 10\text{ ms}$ ; Fig. 4; Fig. 5	-	9	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	0.41	$\text{A}^2\text{s}$
$dl_T/dt$	rate of rise of on-state current	$I_T = 2\text{ A}$ ; $I_G = 10\text{ mA}$ ; $dl_G/dt = 100\text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current		-	1	A
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
$T_{stg}$	storage temperature		-40	150	$^{\circ}\text{C}$
$T_j$	junction temperature		-	125	$^{\circ}\text{C}$



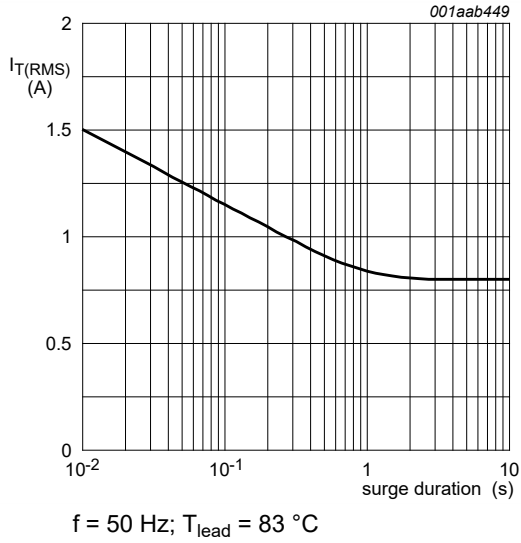


Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents

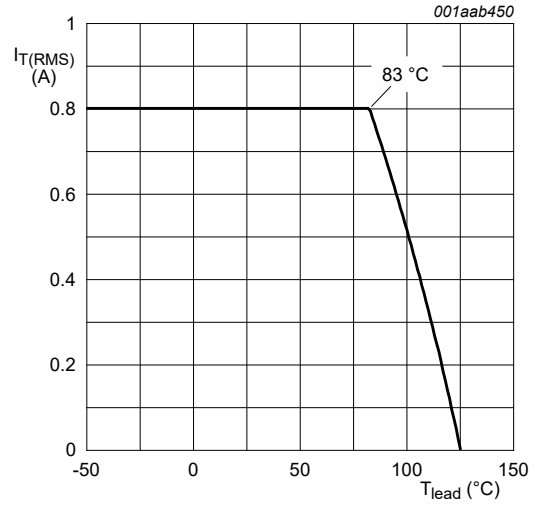


Fig. 3. RMS on-state current as a function of lead temperature; maximum values

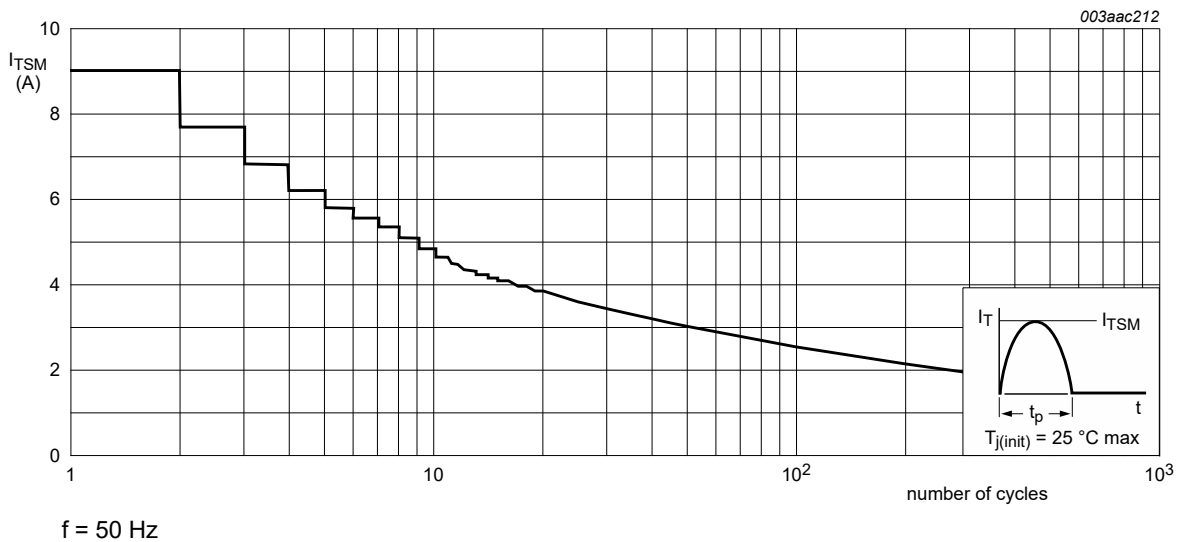
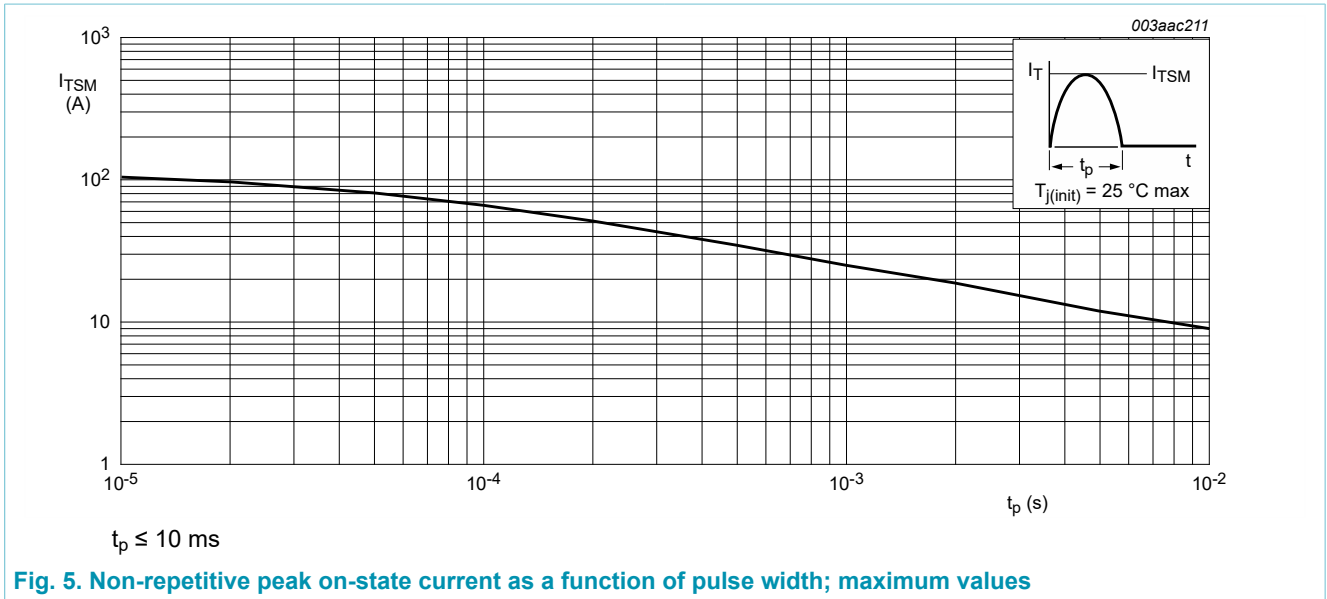


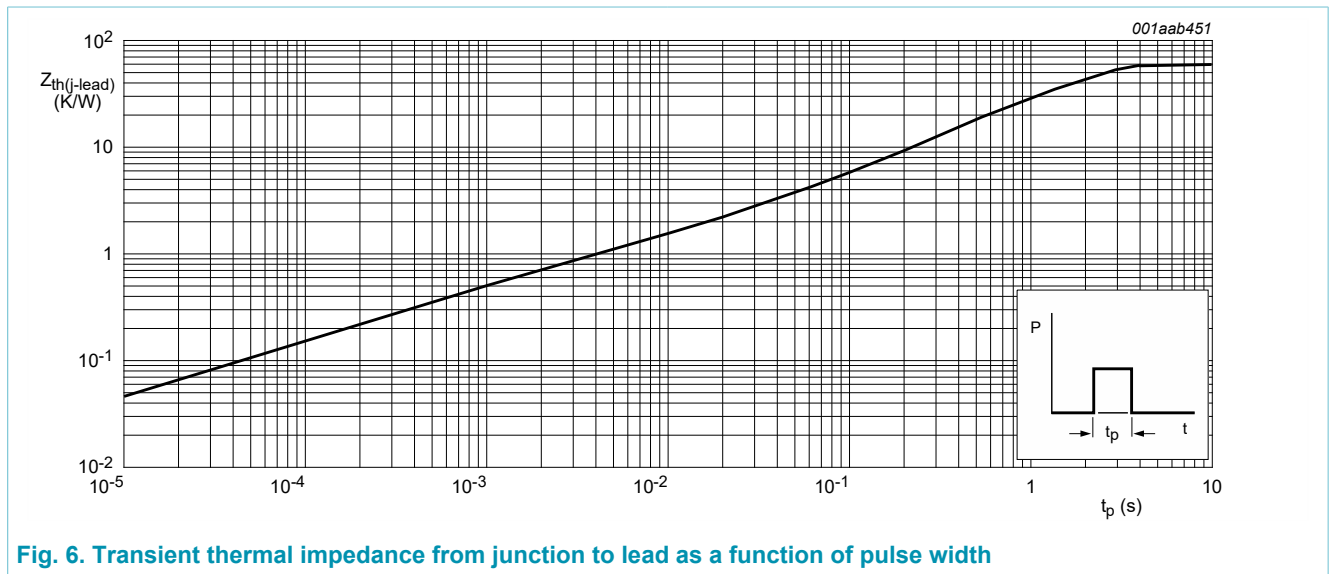
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



## 8. Thermal characteristics

Table 5. Thermal characteristics

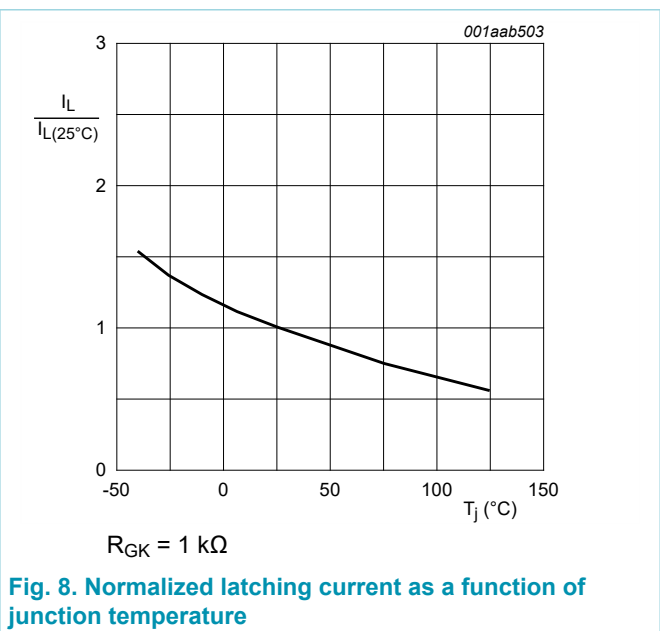
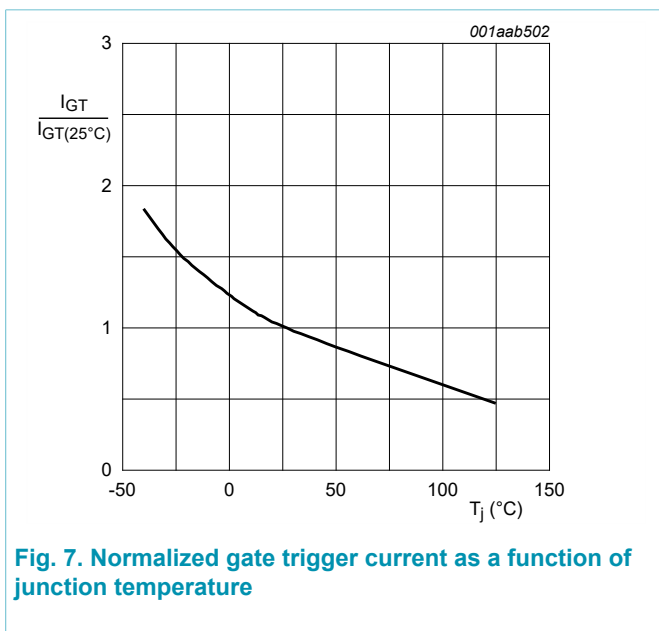
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	<a href="#">Fig. 6</a>	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W



## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	15	33	50	$\mu\text{A}$
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.5\text{ mA}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; $R_{GK(\text{ext})} = 1\text{ k}\Omega$ ; <a href="#">Fig. 8</a>	-	2	6	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; $R_{GK(\text{ext})} = 1\text{ k}\Omega$ ; <a href="#">Fig. 9</a>	-	1.5	3	mA
$V_T$	on-state voltage	$I_T = 1.2\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>	-	1.25	1.7	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	-	0.5	0.8	V
		$V_D = 800\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	0.3	0.5	-	V
$I_D$	off-state current	$V_D = 800\text{ V}$ ; $R_{GK(\text{ext})} = 1\text{ k}\Omega$ ; $T_j = 125\text{ }^\circ\text{C}$	-	0.05	0.1	mA
$I_R$	reverse current	$V_R = 800\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $R_{GK(\text{ext})} = 1\text{ k}\Omega$	-	0.05	0.1	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $R_{GK} = 1\text{ k}\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; <a href="#">Fig. 12</a>	150	-	-	$\text{V}/\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 2\text{ A}$ ; $V_D = 800\text{ V}$ ; $I_G = 10\text{ mA}$ ; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$ ; $T_j = 25\text{ }^\circ\text{C}$	-	2	-	$\mu\text{s}$
$t_q$	commutated turn-off time	$V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $I_{TM} = 1.6\text{ A}$ ; $V_R = 35\text{ V}$ ; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$ ; $dV_D/dt = 2\text{ V}/\mu\text{s}$ ; $R_{GK(\text{ext})} = 1\text{ k}\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ )	-	100	-	$\mu\text{s}$



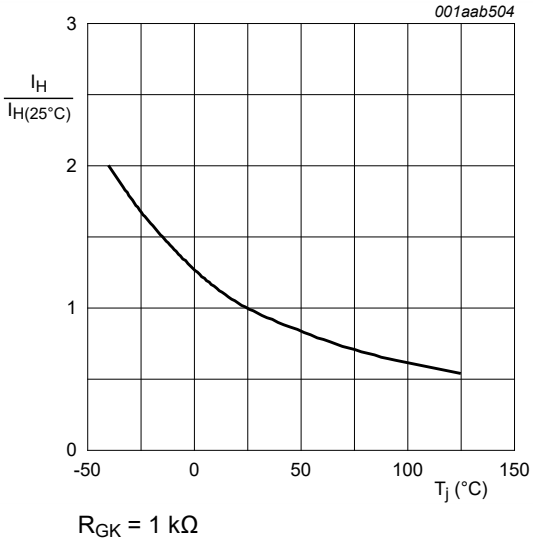


Fig. 9. Normalized holding current as a function of junction temperature

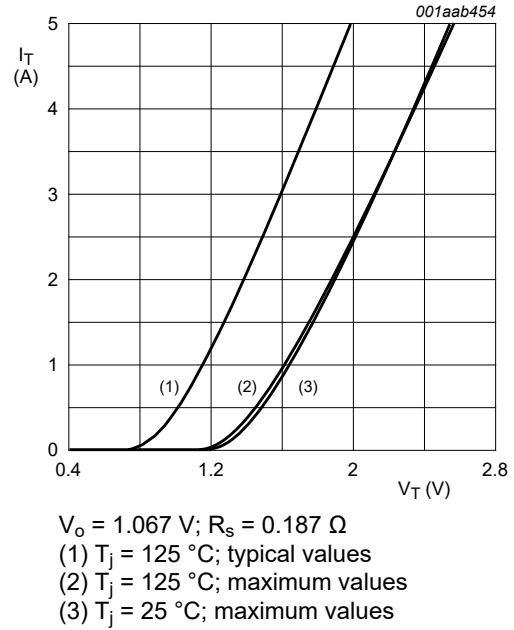


Fig. 10. On-state current as a function of on-state voltage

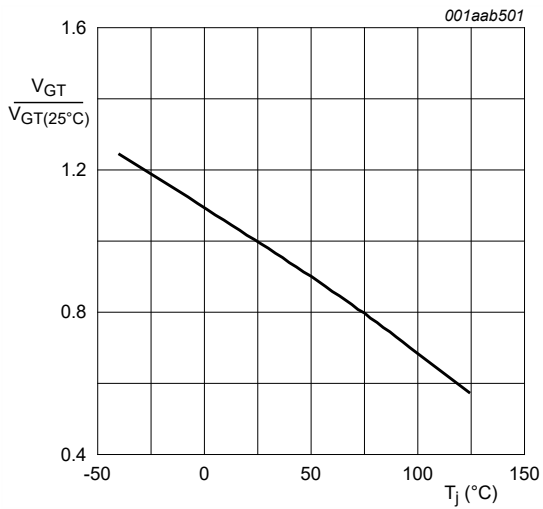


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

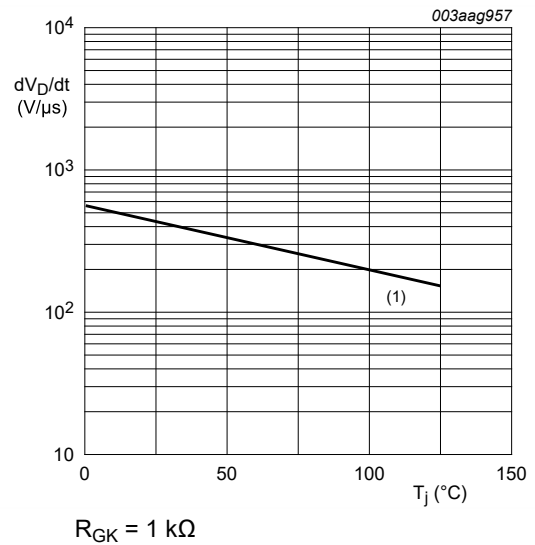


Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values



### 10. Package outline

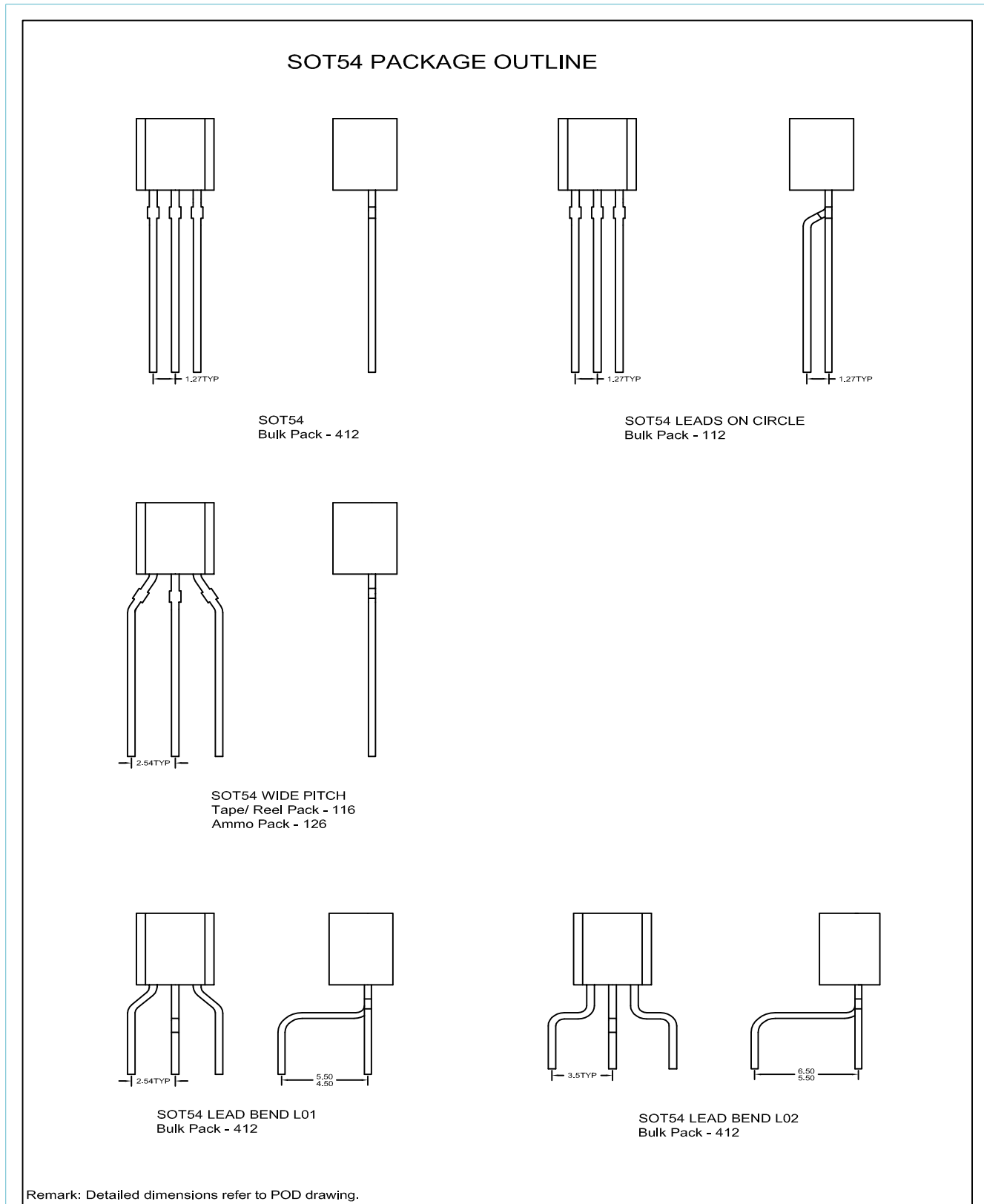


Fig. 13. Package outline TO-92 (SOT54)

# 11. Legal information

## Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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