



60V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D T _C = +25°C
001/	$4.8 \text{m}\Omega$ @ $V_{GS} = 10V$	77.8A
60V	$6.5 \text{m}\Omega$ @ $V_{GS} = 4.5 \text{V}$	68.2A

Features and Benefits

- 100% Unclamped Inductive Switching (UIS) Test in Production -Ensures More Reliable and Robust End Application
- High Conversion Efficiency
- Low R_{DS(ON)}—Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- **ESD Protected Gate**
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen- and Antimony-Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

https://www.diodes.com/quality/product-definitions/

Description and Applications

This new generation N-channel enhancement mode MOSFET is designed to minimize R_{DS(ON)} yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and load switch.

- Synchronous Rectifier
- Power Management Functions
- **DC-DC Converters**

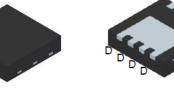
Mechanical Data

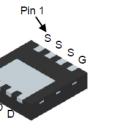
- Case: V-DFN3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Below Diagram
- Terminals: Finish—NiPdAu over Copper Lead-Frame. Solderable per MIL-STD-202, Method 208 @4
- Weight: 0.027 grams (Approximate)

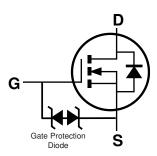
V-DFN3333-8 (Type B)











Top View

Bottom View

Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMT64M8LCG-7	V-DFN3333-8 (Type B)	2,000/Tape & Reel
DMT64M8LCG-13	V-DFN3333-8 (Type B)	3,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/



Marking Information

Site 1:

648

648 = Product Type Marking Code YYWW = Date Code Marking YY = Year (ex: 20 = 2020) WW = Week (01 to 53)

Site 2:

648

648 = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 0 = 2020)

W = Week (ex: a = week 27; z represents week 52 and 53) X = Internal Code (ex: U = Monday)

Date Code Kev

Year	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	9	0	1	2	3	4	5	6	7	8	9	0
Week	Week 1-26				27-52				53			
Code		А	-Z			a	-Z			Z	<u> </u>	
Internal Code	Sur	ı	Mon		Tue	W	ed	Thu		Fri		Sat
Code	Т		U		V	V	٧	Х		Υ		Z



Maximum Ratings (@ $T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V _{DSS}	60	V	
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current, V _{GS} = 10V (Note 6) Steady State	, · ·	I _D	16.1 12.9	Α
Continuous Drain Current, V _{GS} = 10V (Note 7)	I_{D}	77.8 62.2	Α	
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I _{DM}	310	Α	
Maximum Continuous Body Diode Forward Current (Note 7)	Is	77	Α	
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle	I _{SM}	310	Α	
Avalanche Current, L = 0.3mH	I _{AS}	27.2	Α	
Avalanche Energy, L = 0.3mH	Eas	111	mJ	

Thermal Characteristics (@ T_A = +25°C, unless otherwise specified.)

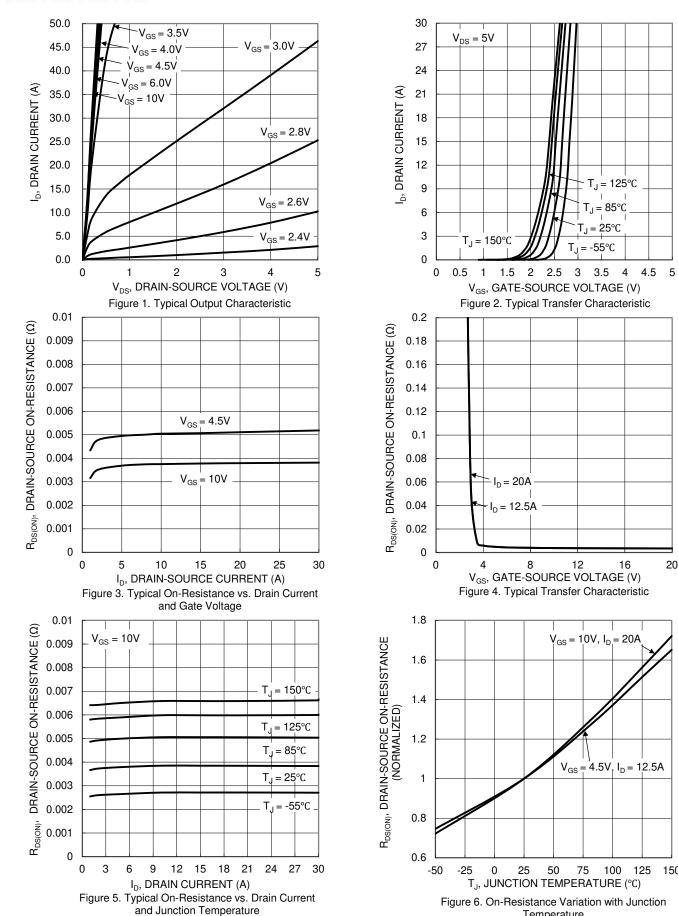
Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^{\circ}C$	P_{D}	0.99	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{ hetaJA}$	126	°C/W
Total Power Dissipation (Note 6)	$T_A = +25^{\circ}C$	P_{D}	2.16	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{ heta JA}$	58	°C/W
Thermal Resistance, Junction to Case (Note 7)		$R_{ heta JC}$	2.5	°C/W
Operating and Storage Temperature Range		$T_{J_1}T_{STG}$	-55 to +150	°C

Electrical Characteristics (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage	BV _{DSS}	60	_	_	٧	$V_{GS} = 0V$, $I_D = 1mA$	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	1	μΑ	$V_{DS} = 48V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±10	μΑ	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	V _{GS(TH)}	1.3	_	2.4	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
Ctatic Duals Course On Resistance		_	3.8	4.8		V _{GS} = 10V, I _D = 20A	
Static Drain-Source On-Resistance	R _{DS(ON)}	_	4.8	6.5	mΩ	V _{GS} = 4.5V, I _D = 12.5A	
Diode Forward Voltage	V_{SD}	_	0.7	1.2	V	V _{GS} = 0V, I _S = 1A	
DYNAMIC CHARACTERISTICS (Note 9)							
Input Capacitance	C _{iss}	_	2664	_		$V_{DS} = 30V, V_{GS} = 0V,$ f = 1MHz	
Output Capacitance	Coss	_	955	_	pF		
Reverse Transfer Capacitance	C _{rss}	_	75	_			
Gate Resistance	Rg	_	0.76	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	26.1	_			
Total Gate Charge (V _{GS} = 10V)	Qg	_	47.5	_	20	2011 204	
Gate-Source Charge	Q _{gs}	_	6.2	_	nC	$V_{DS} = 30V, I_{D} = 20A$	
Gate-Drain Charge	Q_{gd}	_	12.5	_	1		
Turn-On Delay Time	t _{D(ON)}	_	6.4	_			
Turn-On Rise Time	t _R	_	9.1	_	1	$V_{DD} = 30V, V_{GS} = 10V,$	
Turn-Off Delay Time	t _{D(OFF)}	_	29.8	_	ns	$I_D = 20A$, $R_G = 3.3\Omega$	
Turn-Off Fall Time	t _F	_	18.3	_	1		
Reverse Recovery Time	t _{RR}	_	41	_	ns	1 224 11/11 1004/1-	
Reverse Recovery Charge	Q _{RR}	_	53	_	nC	$I_F = 20A$, di/dt = 100A/ μ s	

 Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
Thermal resistance from junction to soldering point (on the exposed drain pad).
Short duration pulse test used to minimize self-heating effect.
Guaranteed by design. Not subject to product testing. Notes:





Temperature



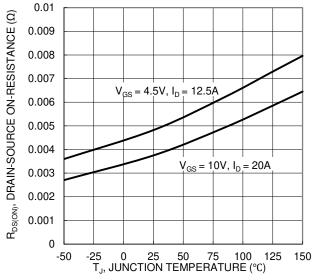


Figure 7. On-Resistance Variation with Junction Temperature

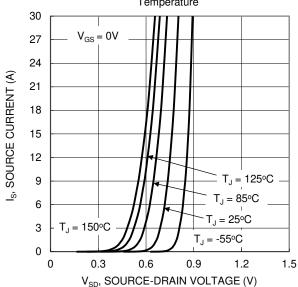


Figure 9. Diode Forward Voltage vs. Current

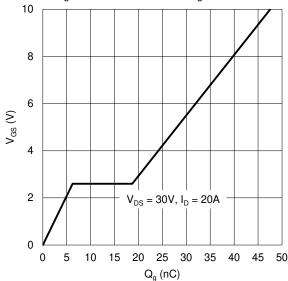


Figure 11. Gate Charge

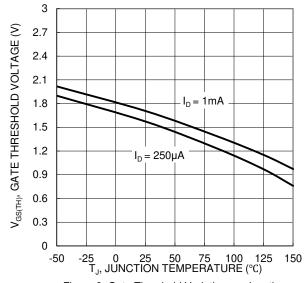


Figure 8. Gate Threshold Variation vs. Junction Temperature

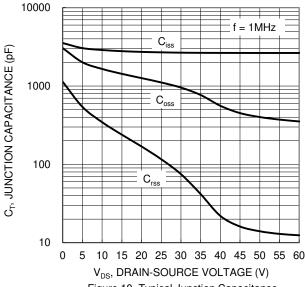


Figure 10. Typical Junction Capacitance

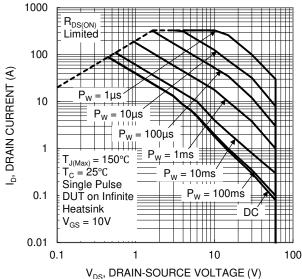


Figure 12. SOA, Safe Operation Area



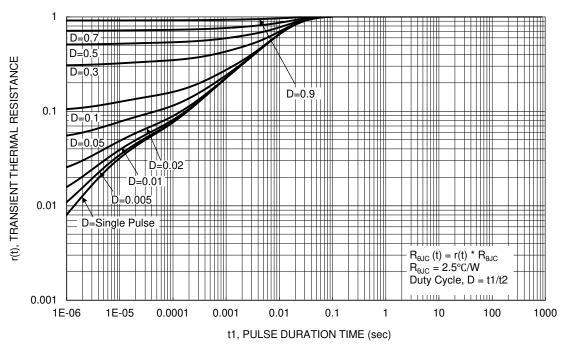
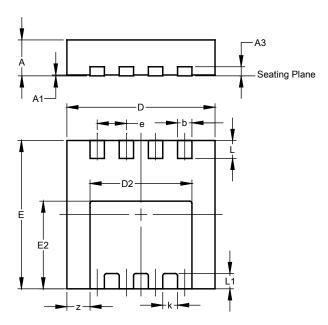


Figure 13. Transient Thermal Resistance



Package Outline Dimensions

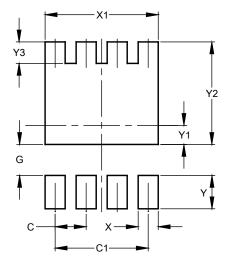
Please see http://www.diodes.com/package-outlines.html for the latest version.



V-DFN3333-8							
(Type B)							
Dim	Min	Max	Тур				
Α	0.75	0.85	0.80				
A 1	0.00	0.05	0.02				
A3			0.203				
q	0.27	0.37	0.32				
D	3.25	3.35	3.30				
D2	2.17	2.37	2.27				
П	3.25	3.35	3.30				
E2	1.85	2.05	1.95				
е			0.65				
k			0.33				
L	0.35	0.45	0.40				
L			0.34				
Z			0.515				
All Dimensions in mm							

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



Dimensions	Value (in mm)			
С	0.650			
C1	1.950			
G	0.650			
Х	0.420			
X1	2.370			
Υ	0.700			
Y1	0.400			
Y2	2.150			
V3	0.450			



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