CG5982AF

2K x 8 Automotive Dual-port Static RAM

Features

- **True dual-ported memory cells that allow simultaneous reads of the same memory location**
- **Automotive temperature operation: –40°C to +115°C**
- **2K x 8 organization**
- **High-speed access: 55 ns**
- **Low operating power: I_{CC} = 120 mA (max.)**
- **Fully asynchronous operation**
- **Automatic power-down**
- **Master CG5982AF easily expands data bus width to 16 or more bits using slave**
- **$\overline{BUSY}$ output flag**
- **$\overline{INT}$ flag for port-to-port communication**

Functional Description

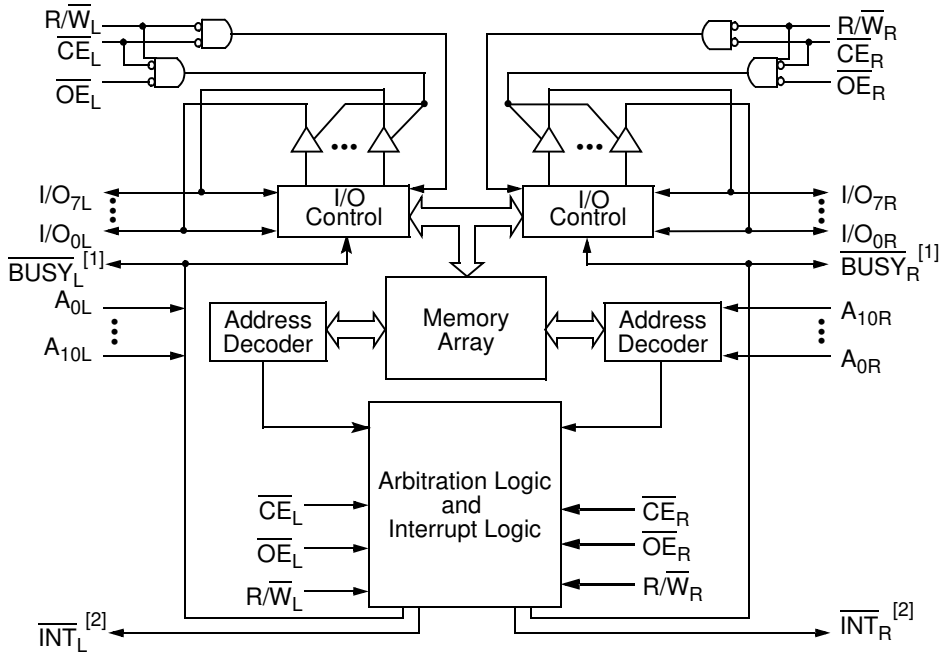
The CG5982AF are high-speed CMOS 2K x 8 dual-port static RAMs. Two ports are provided to permit independent access to any location in memory. The CG5982AF can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CG5982AF SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). BUSY flags are provided on each port. In addition, an interrupt flag ($\overline{INT}$) is provided on each port of the 52-pin PLCC version. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. On the PLCC version, $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CG5982AF is available in a 52-pin PLCC package.

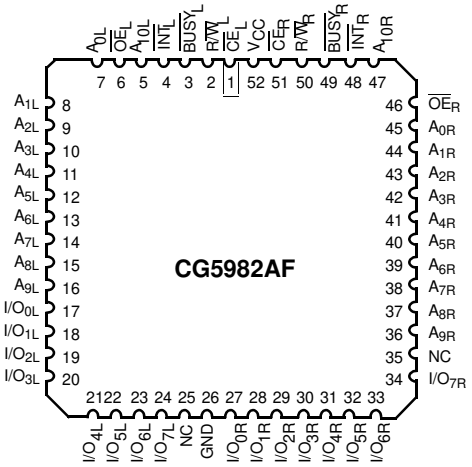
Logic Block Diagram



Notes:
1. CG5982AF (Master): BUSY is open-drain output and requires pull-up resistor.
2. Open drain outputs; pull-up resistor required.

Pin Configurations

PLCC
Top View



Selection Guide

	CG5982AF	Unit
Maximum Access Time	55	ns
Maximum Operating Current	120	mA
Maximum Standby Current	45	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) .....–0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State .....–0.5V to +7.0V

DC Input Voltage .....–3.5V to +7.0V

Output Current into Outputs (LOW).....20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive[3]	–40°C to +115°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions	CG5982AF		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
		I_{OL} = 16.0 mA[5]		0.5	
V_{IH}	Input HIGH Voltage		2.2		V
V_{IL}	Input LOW Voltage			0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–5	+5	μA
I_{OS}	Output Short–Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND		–350	mA

Note:
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. $\overline{BUSY}$ and $\overline{INT}$ pins only.
6. Duration of the short circuit should not exceed 30 seconds.

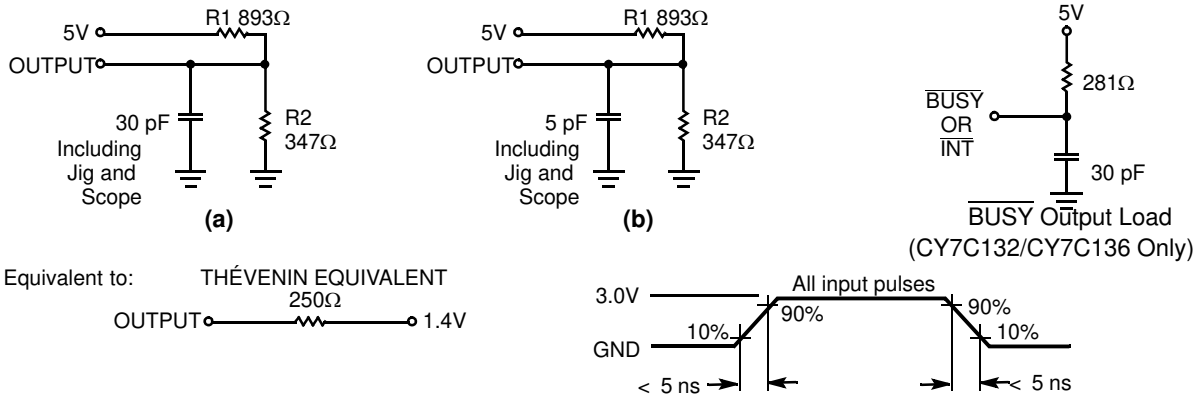
Electrical Characteristics Over the Operating Range[4] (continued)

Parameter	Description	Test Conditions		CG5982AF Min.	CG5982AF Max.	Unit
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[7]	Auto		120	mA
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[7]	Auto		45	mA
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$, Active Port Outputs Open, f = f_{MAX}[7]	Auto		90	mA
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0	Auto		15	mA
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Open, f = f_{MAX}[7]	Auto		85	mA

Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[4, 9]

Parameter	Description	CG5982AF Min.	CG5982AF Max.	Unit
Read Cycle				
t_{RC}	Read Cycle Time	55		ns
t_{AA}	Address to Data Valid[10]		55	ns
t_{OHA}	Data Hold from Address Change	0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[10]		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[10]		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[8, 11]	3		ns

Notes:
7. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{rc}$ and using AC Test Waveforms input levels of GND to 3V.
8. This parameter is guaranteed but not tested.
9. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
10. AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
11. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.

Switching Characteristics Over the Operating Range[4, 9] (continued)

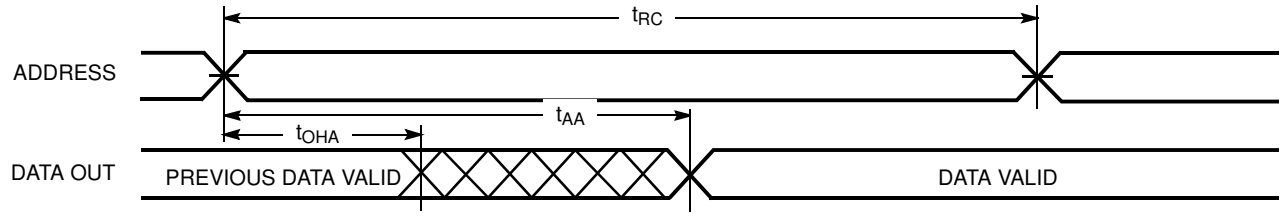
Parameter	Description	CG5982AF		Unit
		Min.	Max.	
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8, 11, 12]		25	ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[8, 11, 12]		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up[8]	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down[8]		35	ns
Write Cycle[13]				
t_{WC}	Write Cycle Time	55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	40		ns
t_{AW}	Address Set-up to Write End	40		ns
t_{HA}	Address Hold from Write End	2		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	30		ns
t_{SD}	Data Set-up to Write End	20		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High-Z [8]		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low-Z [8]	0		ns
Busy/Interrupt Timing				
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[14]		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[14]		30	ns
t_{PS}	Port Set-up for Priority	5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 15	ns
t_{WDD}	Write Pulse to Data Delay		Note 15	ns
Interrupt Timing[15]				
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[14]		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[14]		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[14]		45	ns

Notes:

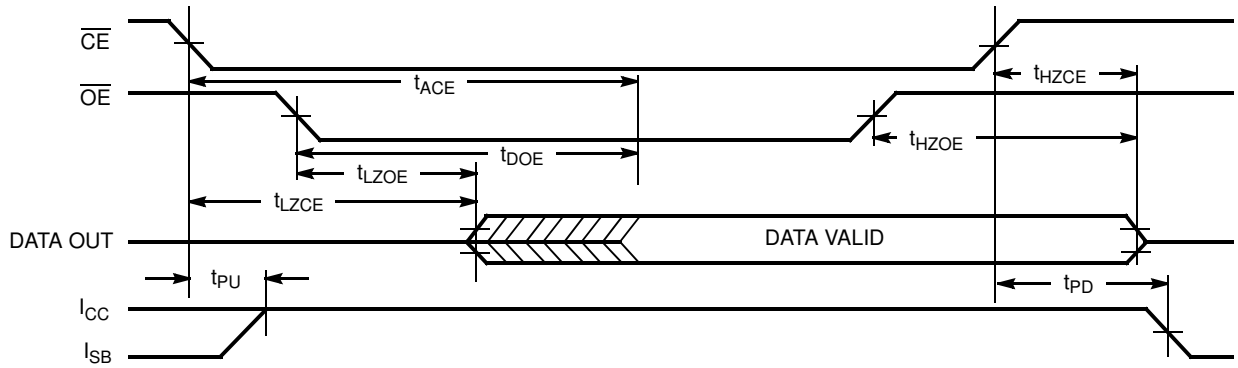
12. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5 pF, as in (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
13. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
15. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    BUSY on Port B goes HIGH.
    Port B's address toggled.
    $\overline{CE}$ for Port B is toggled.
    R/$\overline{W}$ for Port B is toggled during valid read.

Switching Waveforms

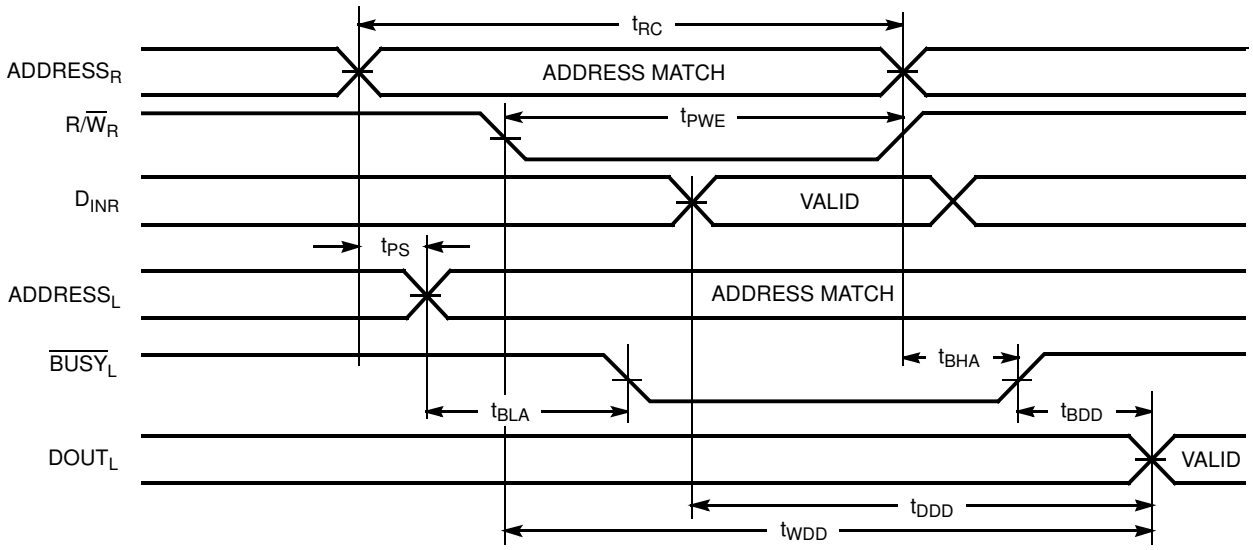
Read Cycle No. 1 (Either Port-Address Access)[16, 17]



Read Cycle No. 2 (Either Port-$\overline{CE}$/$\overline{OE}$)[16, 18]



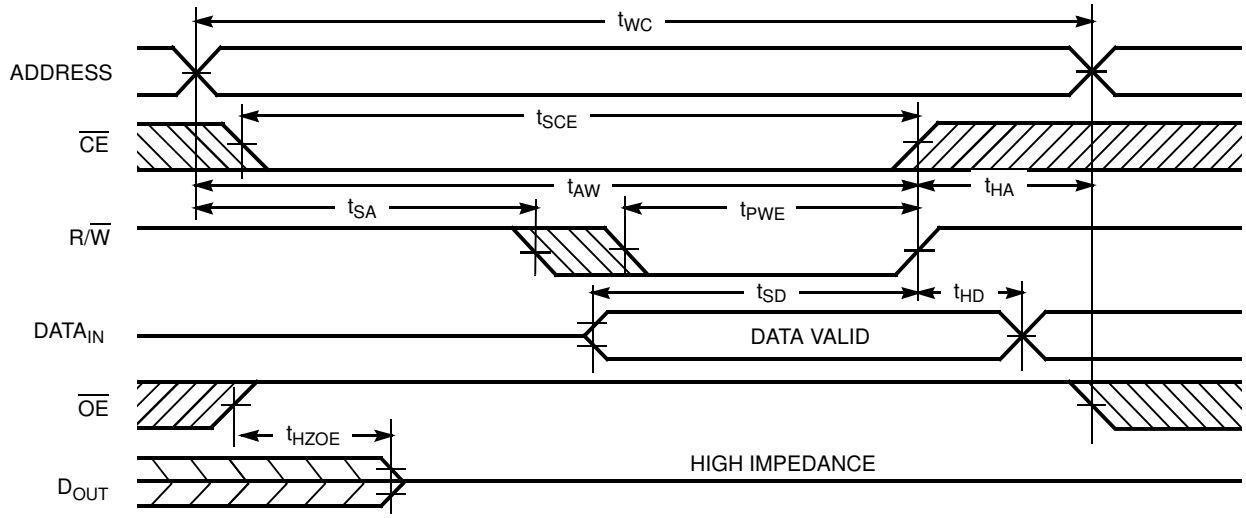
Read Cycle No. 3 (Read with $\overline{BUSY}$ Master)



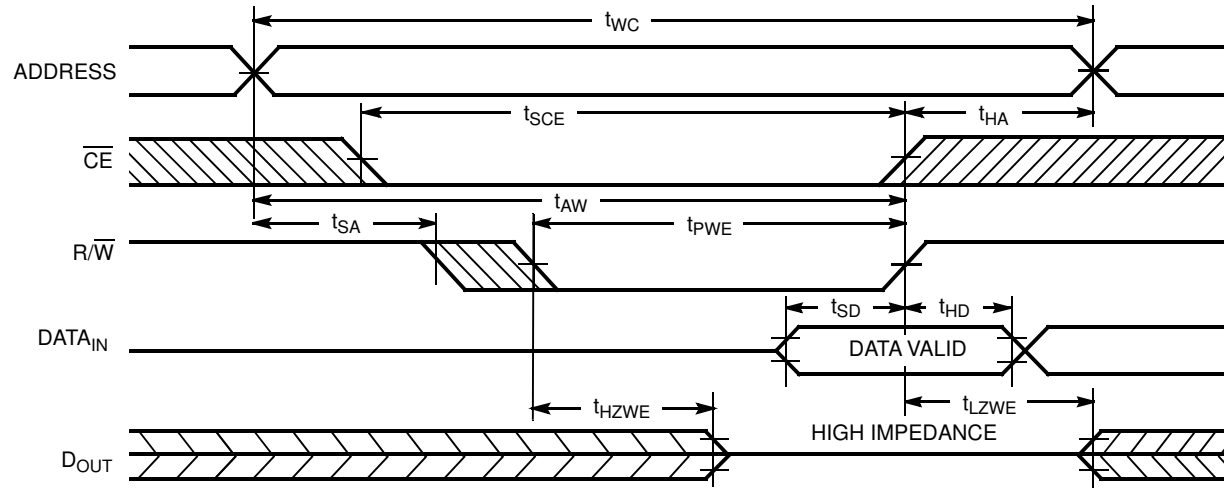
Notes:
16. R/$\overline{W}$ is HIGH for read cycle.
17. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
18. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No.1 ($\overline{OE}$ Three-States Data I/Os—Either Port)[13, 19]



Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os—Either Port)[13, 20]

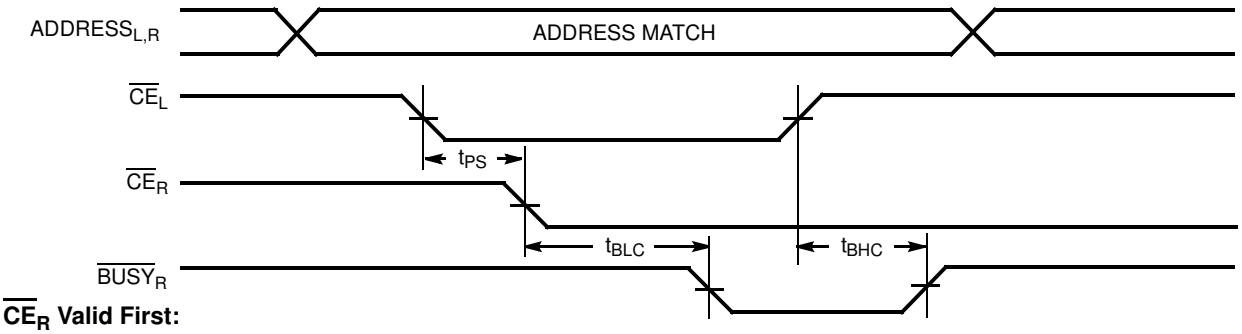


Notes:
19. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
20. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in a high-impedance state.

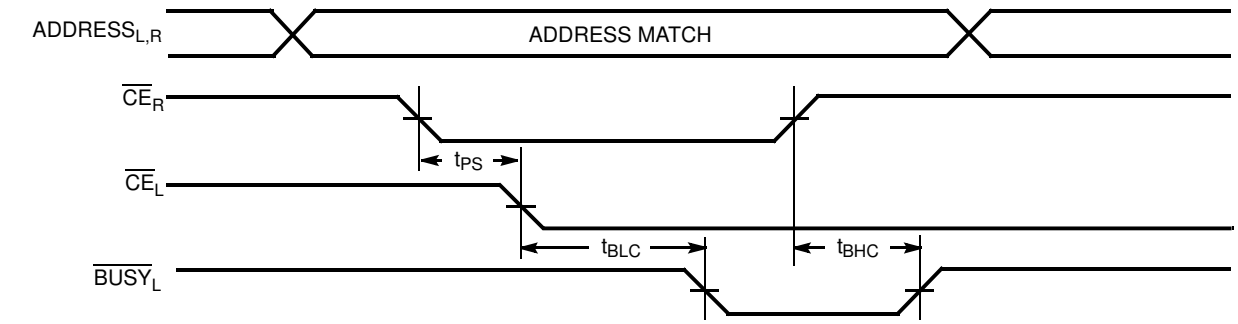
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:

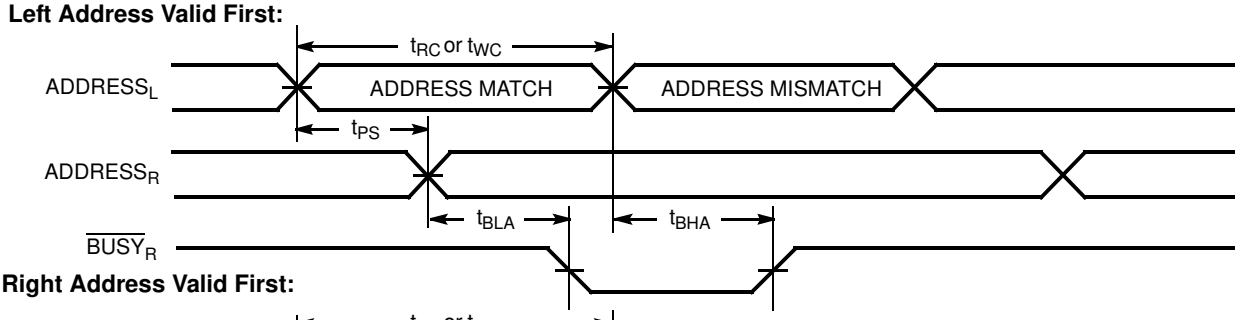


$\overline{CE}_R$ Valid First:

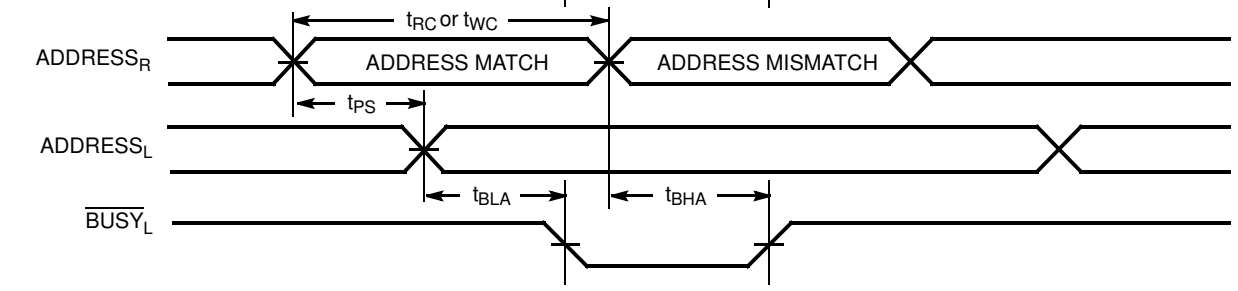


Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:

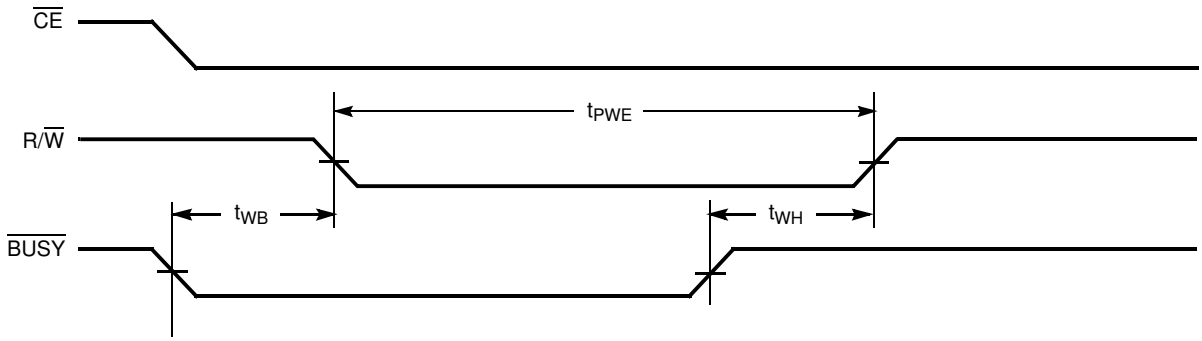


Right Address Valid First:



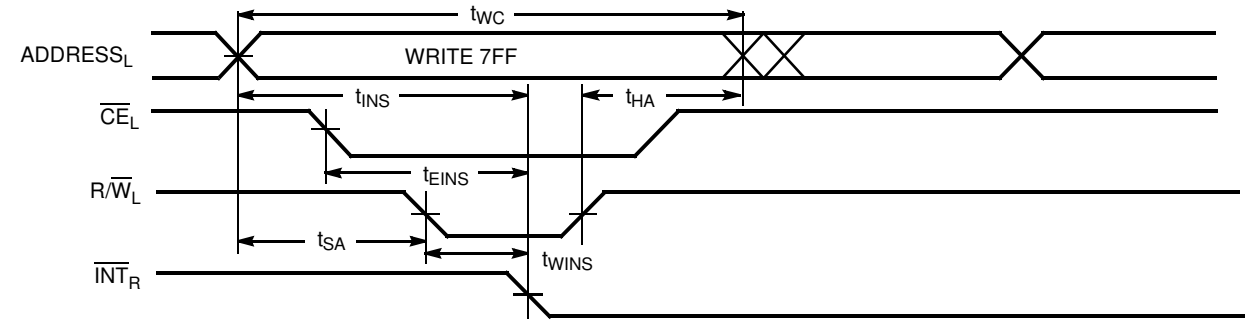
Switching Waveforms (continued)

Busy Timing Diagram No. 3 (Write with $\overline{BUSY}$, Slave)

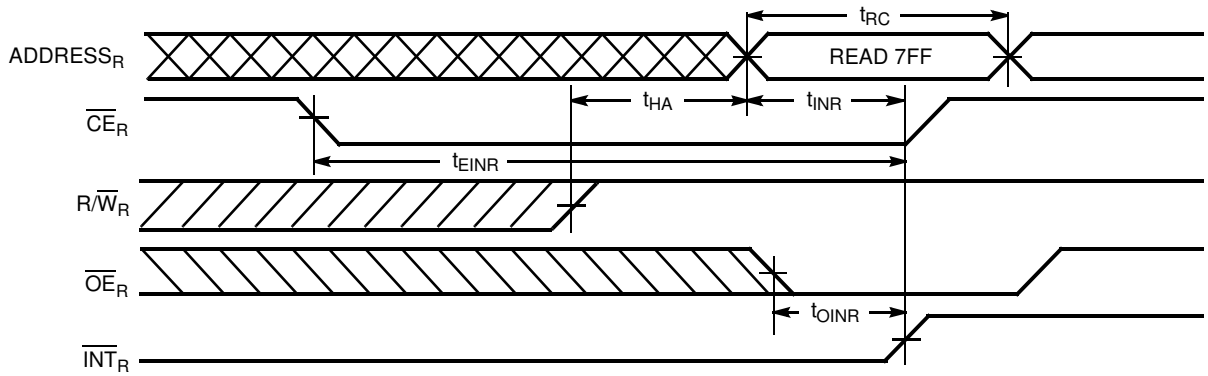


Interrupt Timing Diagrams[16]

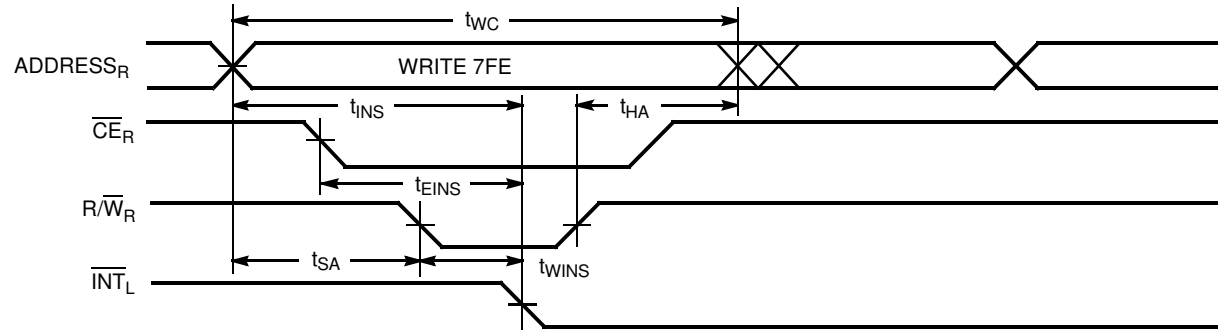
Left Side Sets $\overline{INT}_R$:



Right Side Clears $\overline{INT}_R$:

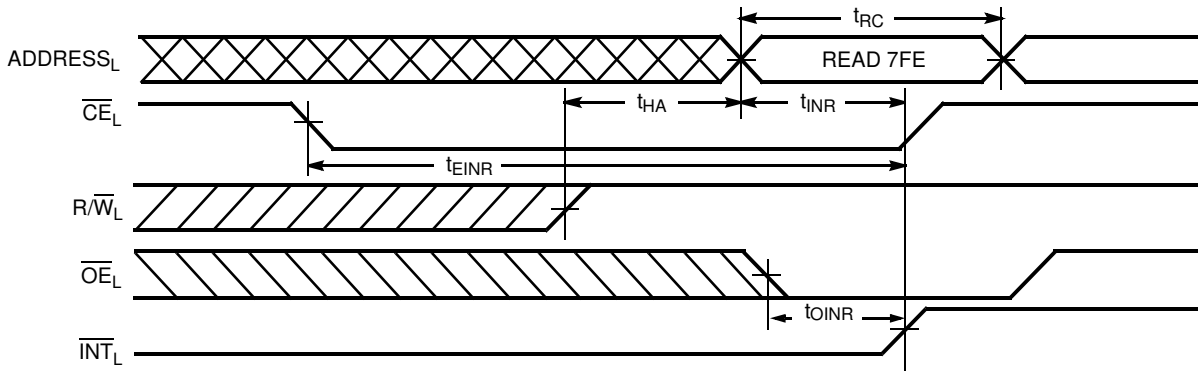


Right Side Sets $\overline{INT}_L$:

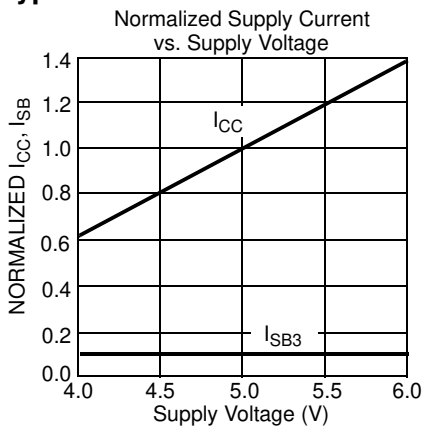


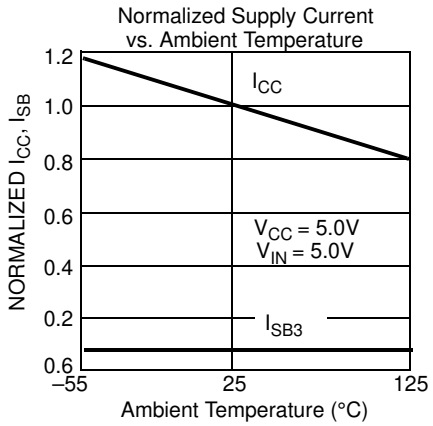
Interrupt Timing Diagrams[16] (continued)

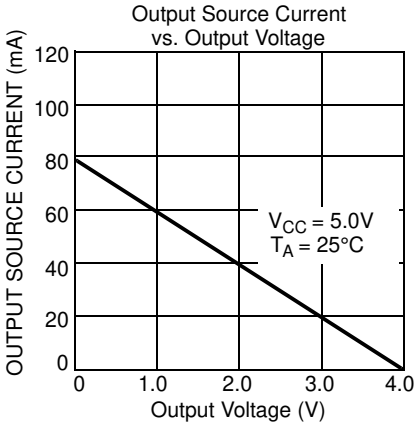
Left Side Clears $\overline{INT}_L$:

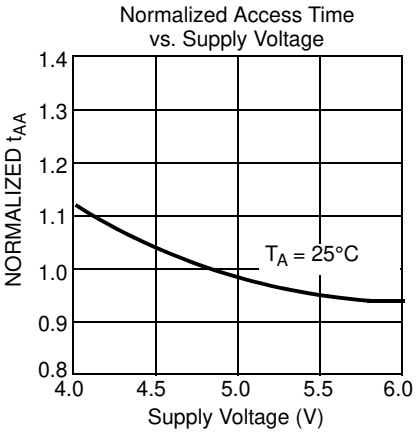


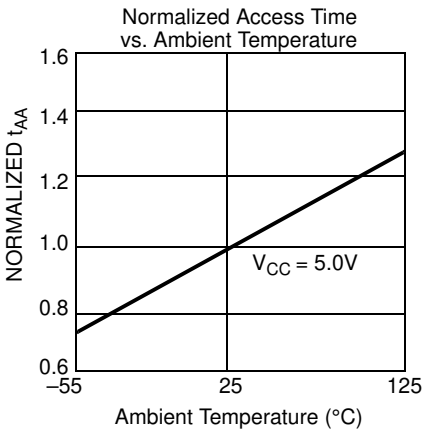
Typical DC and AC Characteristics

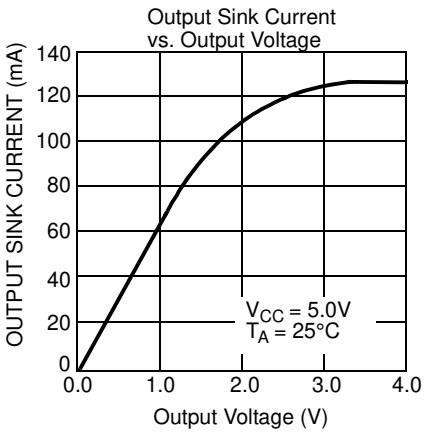


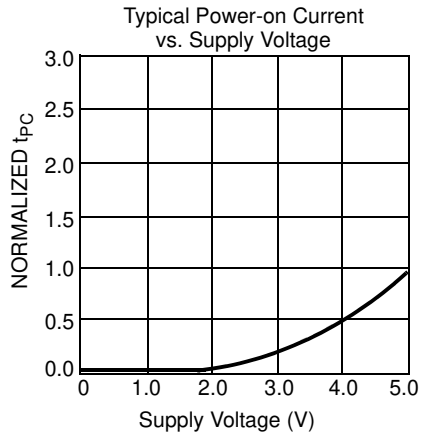


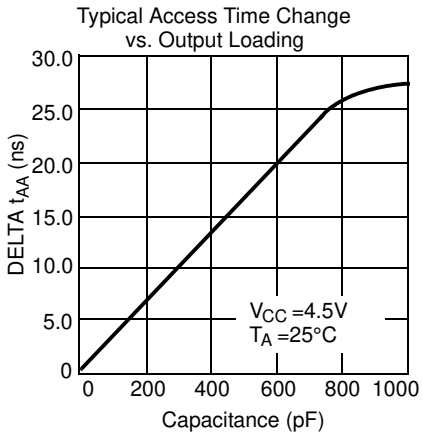


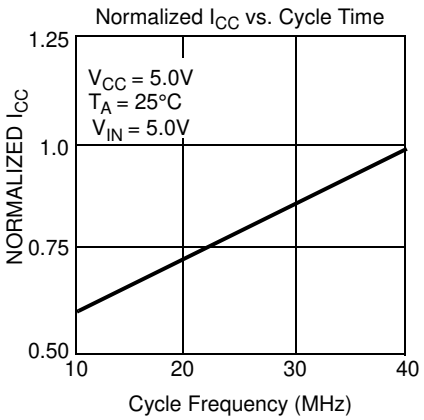










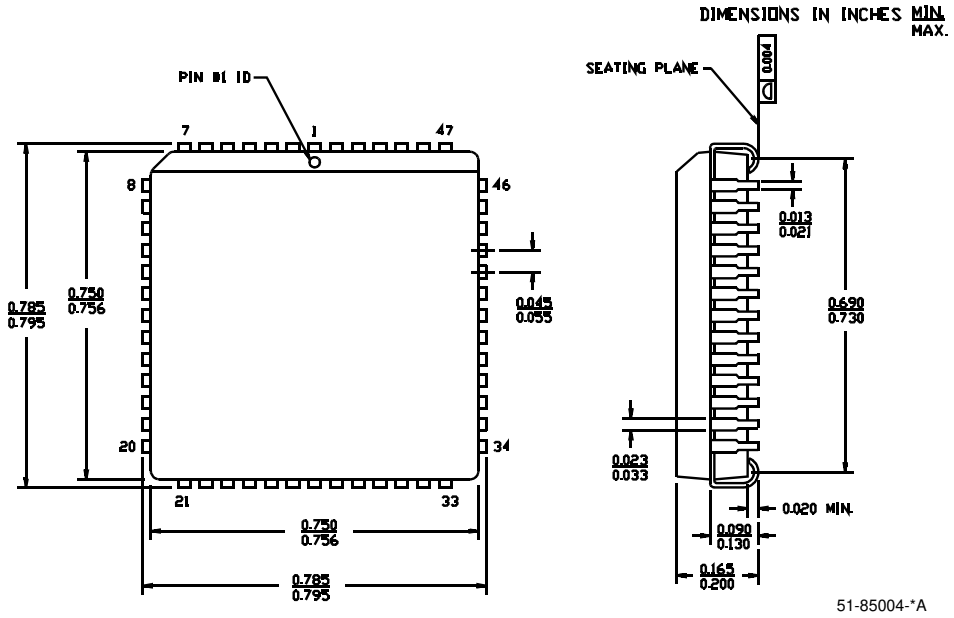


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CG5982AF	J69	52-lead Plastic Leaded Chip Carrier	Automotive

Package Diagrams

52-lead Plastic Leaded Chip Carrier J69



Document History Page

Document Title: CG5982AF 2K x 8 Automotive Dual-port Static RAM Document Number: 38-06067				
REV.	**ECN**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	119657	10/10/02	NIM	Customized data sheet to meet special requirements for CG5982AF; automotive temperature –40°C to +115°C; base part in CY7C136
*A	121488	12/09/02	OOR	Fixed Typo- changed 5 mA to 5 μA (p.2)
*B	393195	SEE ECN	KGH	Included the automotive temperature operation range to the Features section Removed the micron CMOS size and the 52-pin PLCC references from the Features section Added Automotive to the title description
*C	421244	See ECN	ODC	Add to external web.