ADS52J90 10-Bit, 12-Bit, 14-Bit, Multichannel, Low-Power, High-Speed ADC with LVDS, JESD Outputs

1 Features

- 16-Channel ADC Configurable to Convert 8, 16, or 32 Inputs
- 10-, 12-, and 14-Bit Resolution Modes
- Maximum ADC Conversion Rate:
  - 100 MSPS in 10-Bit Mode
  - 80 MSPS in 12-Bit Mode
  - 65 MSPS in 14-Bit Mode
- 16 ADCs Configurable to Convert:
  - 8 Inputs with a Sampling Rate of a 2X ADC Conversion Rate
  - 16 Inputs with a Sampling Rate of a 1X ADC Conversion Rate
  - 32 Inputs with a Sampling Rate of a 0.5X ADC Conversion Rate
- LVDS Outputs with 16X, 14X, 12X, and 10X Serialization
- 5-Gbps JESD Interface:
  - Supported in 16-Input and 32-Input Modes
  - JESD204B Subclass 0, 1, and 2
  - 2, 4, or 8 Channels per JESD Lane
- Optional Digital I-Q Demodulator (1)
- Supplies: 1.2 V, 1.8 V
- 2-V_{PP} Differential Input, 0.8-V Common-Mode
- Differential or Single-Ended Input Clock
- Signal-to-Noise Ratio (SNR):
  - 61 dBFS in 10-Bit Mode
  - 70 dBFS in 12-Bit Mode
  - 73.5 dBFS in 14-Bit Mode
- Power at 100 MSPS: 41 mW/Channel
- Package: NFBGA-198 (9 mm × 15 mm)
- Pb-Free (RoHS Compliant) and Green

2 Applications

- Ultrasound Imaging
- Portable Instrumentation
- SONAR and RADAR
- High-Speed Multichannel Data Acquisition

(1) Not detailed in this document. For details and information, contact factory.

3 Description

The ADS52J90 is a low-power, high-performance, 16-channel, analog-to-digital converter (ADC). The conversion rate of each ADC goes up to a maximum of 100 MSPS in 10-bit mode. The maximum conversion rate reduces when the ADC resolution is set to a higher value.

The device can be configured to accept 8, 16, or 32 inputs. In 32-input mode, each ADC alternately samples and converts two different inputs each at an effective sampling rate that is half of the ADC conversion rate. In 8-bit input mode, two ADCs convert the same input in an interleaved manner, resulting in an effective sampling rate that is twice the ADC conversion rate. The ADC is designed to scale its power with the conversion rate.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS52J90	NFBGA (198)	9.00 mm × 15.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

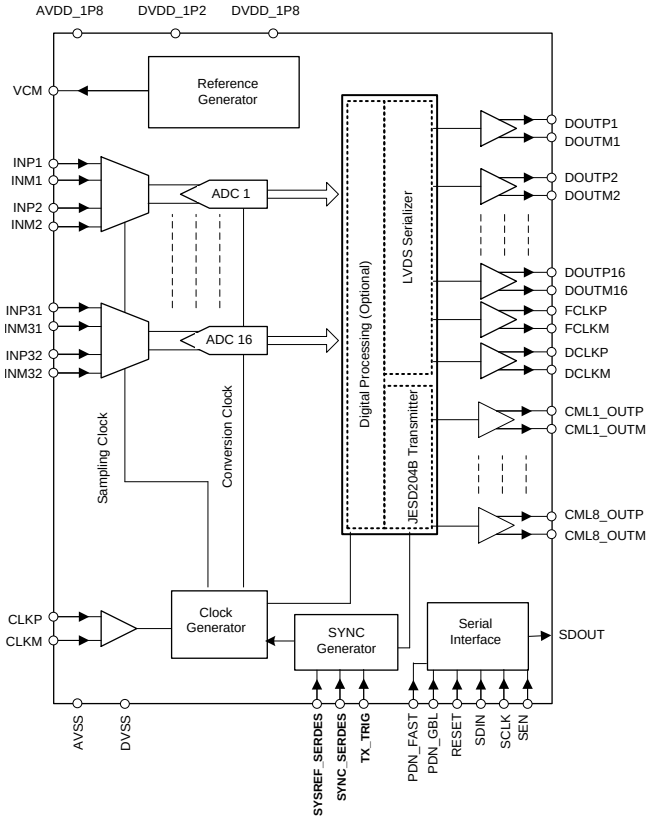


Table of Contents

4 Revision History

Changes from Revision B (August 2015) to Revision C — **Page**

- Changed *HPF_ROUND_ENABLE register bit (register 15, bit 5)* to *HPF_ROUND_EN_CH1-8 and HPF_ROUND_EN_CH9-16 bits* in last paragraph of *Digital HPF* section ... 40
- Changed *Masking of the Various Reset Operations Resulting from SYNC~ or SYSREF* table ... 59
- Added *Interfacing SYNC~ and SYSREF Between the FPGA and ADCs* section ... 65
- Changed *Mapping of Analog Inputs to LVDS Outputs (8-Input Mode, 1X Data Rate)* table ... 84
- Changed *Mapping of Analog Inputs to LVDS Outputs (8-Input Mode, 2X Data Rate)* table ... 85
- Changed description for the value 001 in *Pattern Mode Bit Description* table ... 99
- Changed bit 5 from *HPF_ROUND_EN* to *HPF_ROUND_EN_CH1-8* in Register 15 ... 109
- Changed bit 5 from 0 to *HPF_ROUND_EN_CH9-16* in Register 2Dh ... 123
- Changed description for JESD_RESET1 in Register 70 ... 135
- Changed description of JESD_RESET2 and JESD_RESET3 in Register 74 ... 137

Changes from Revision A (June 2015) to Revision B — **Page**

- Changed document title to include LVDS, JESD outputs ... 1
- Added *JESD Interface Optional Demodulator* and Features bullets ... 1
- Changed *Simplified Schematic* ... 1
- Added JESD interface information to *Description* section ... 4
- Added footnote 1 to *Pin Functions* table ... 6
- Changed description of SPI_DIG_EN pin in *Pin Functions* table ... 8
- Changed title of *Current Consumption with LVDS Interface Enabled* section of *Electrical Characteristics* table ... 12
- Changed *Current Consumption with JESD Interface Enabled* section of *Electrical Characteristics* table ... 12

- Added SPI_DIG_EN to *Digital Inputs* section title of *Digital Characteristics* table 13
- Changed $V_{OC\text{-}CML}$ parameter name in *JESD Interface Timing Requirements* table 15
- Added Figure 47 25
- Added LVDS, JESD discussion to second paragraph of *Overview* section 51
- Added *Community Resources* section 149

Changes from Original (May 2015) to Revision A **Page**

- Released to production 1
- Changed *Circuit to Level-Shift the Common-Mode Voltage From 1.2 V at the Driver Output to 0.7 V at the ADC Input* figure 65
- Changed *AC-Coupling Scheme for SYSREF* figure 66

5 Description (continued)

The ADC outputs are serialized and output through a low-voltage differential signaling (LVDS) interface along with a frame clock and a high-speed bit clock

The device also has an optional JESD204B interface while operating in the 16-input and 32-input modes. This interface runs up to 5 Gbps.

The ADS52J90 is available in a 9-mm × 15-mm, 0.8-mm pitch, NFBGA-198 package and is specified over a temperature range of –40°C to +85°C.

6 Pin Configuration and Functions

ZZE Package
NFBGA-198 (15 mm × 9 mm)
Top View

	1	2	3	4	5	6	7	8	9	10	11
A	INM2	INP2	INP1	AVDD_1P8	SDIN	RESET	DVDD_1P2	DVSS	CML1_OUTP	CML1_OUTM	CML2_OUTP
B	INM3	INP3	INM1	AVSS	SEN	SPI_DIG_EN	SCLK	DVDD_1P2	DOUTP1	DOUTM1	CML2_OUTM
C	INM5	INP5	INP4	AVSS	SDOUT	PDN_FAST	PDN_GBL	DVDD_1P2	DOUTP2	DOUTM2	CML3_OUTP
D	INM6	INP6	INM4	AVSS	NC	TX_TRIG	DVSS	DVDD_1P2	DOUTP3	DOUTM3	CML3_OUTM
E	INM7	INP7	INM8	INP8	NC	AVDD_1P8	DVSS	DVDD_1P8	DOUTP4	DOUTM4	CML4_OUTP
F	INM9	INP9	INM10	INP10	VCM	AVDD_1P8	DVDD_1P2	DVDD_1P8	DOUTP5	DOUTM5	CML4_OUTM
G	INM11	INP11	INM12	INP12	AVDD_1P8	AVDD_1P8	DVDD_1P2	DVDD_1P8	DOUTP6	DOUTM6	DOUTM8
H	INM13	INP13	INM14	INP14	AVSS	AVSS	DVSS	DVSS	DOUTP7	DOUTM7	DOUTP8
J	INM15	INP15	INM16	INP16	AVSS	AVSS	DVSS	DVSS	FCLKP	DVDD_1P8	DCLKP
K	INM17	INP17	INM18	INP18	AVSS	AVSS	DVSS	DVSS	FCLKM	DVSS	DCLKM
L	INM19	INP19	INM20	INP20	AVSS	AVSS	DVSS	DVSS	DOUTP10	DOUTM10	DOUTP9
M	INM21	INP21	INM22	INP22	AVDD_1P8	AVDD_1P8	DVDD_1P2	DVDD_1P8	DOUTP11	DOUTM11	DOUTM9
N	INM23	INP23	INM24	INP24	NC	AVDD_1P8	DVDD_1P2	DVDD_1P8	DOUTP12	DOUTM12	CML8_OUTM
P	INM25	INP25	INM26	INP26	NC	AVDD_1P8	SYNCM_ SERDES	DVDD_1P8	DOUTP13	DOUTM13	CML8_OUTP
R	INM27	INP27	INM28	AVSS	AVSS	DVSS	SYNCP_ SERDES	DVDD_1P2	DOUTP14	DOUTM14	CML7_OUTM
T	INM29	INP29	INP28	AVSS	AVSS	DVDD_1P2	SYSREFM_ SERDES	DVDD_1P2	DOUTP15	DOUTM15	CML7_OUTP
U	INM30	INP30	INM32	AVSS	CLKM	AVSS	SYSREFP_ SERDES	DVDD_1P2	DOUTP16	DOUTM16	CML6_OUTM
V	INM31	INP31	INP32	AVDD_1P8	CLKP	AVSS	DVDD_1P2	DVSS	CML5_OUTP	CML5_OUTM	CML6_OUTP

Pin Functions[1]

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD_1P8	A4, E6, F6, G5, G6, M5, M6, N6, P6, V4	P	1.8-V analog supply voltage
AVSS	B4, C4, D4, H5, H6, J5, J6, K5, K6, L5, L6, R4, R5, T4, T5, U4, U6, V6	G	Analog ground
CLKM	U5	I	Differential clock input pins. A single-ended clock is also supported. See the *Clock Input* section for further details.
CLKP	V5		
CML1_OUTM	A10	O	JESD output lane 1
CML1_OUTP	A9		
CML2_OUTM	B11	O	JESD output lane 2
CML2_OUTP	A11		
CML3_OUTM	D11	O	JESD output lane 3
CML3_OUTP	C11		
CML4_OUTM	F11	O	JESD output lane 4
CML4_OUTP	E11		
CML5_OUTM	V10	O	JESD output lane 5
CML5_OUTP	V9		
CML6_OUTM	U11	O	JESD output lane 6
CML6_OUTP	V11		
CML7_OUTM	R11	O	JESD output lane 7
CML7_OUTP	T11		
CML8_OUTM	N11	O	JESD output lane 8
CML8_OUTP	P11		
DCLKM	K11	O	LVDS bit clock output
DCLKP	J11		
DOUTM1	B10	O	LVDS data lane 1
DOUTP1	B9		
DOUTM2	C10	O	LVDS data lane 2
DOUTP2	C9		
DOUTM3	D10	O	LVDS data lane 3
DOUTP3	D9		
DOUTM4	E10	O	LVDS data lane 4
DOUTP4	E9		
DOUTM5	F10	O	LVDS data lane 5
DOUTP5	F9		
DOUTM6	G10	O	LVDS data lane 6
DOUTP6	G9		
DOUTM7	H10	O	LVDS data lane 7
DOUTP7	H9		
DOUTM8	G11	O	LVDS data lane 8
DOUTP8	H11		
DOUTM9	M11	O	LVDS data lane 9
DOUTP9	L11		
DOUTM10	L10	O	LVDS data lane 10
DOUTP10	L9		
DOUTM11	M10	O	LVDS data lane 11
DOUTP11	M9		
DOUTM12	N10	O	LVDS data lane 12
DOUTP12	N9		

(1) If the JESD interface is not used, then do not connect the CMLx, SYNCx, and SYSREFx pins. If the LVDS interface is not used, then do not connect DOUTx, DCLKx, and FCLKx.

Pin Functions[1] (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DOUTM13	P10	O	LVDS data lane 13
DOUTP13	P9		
DOUTM14	R10	O	LVDS data lane 14
DOUTP14	R9		
DOUTM15	T10	O	LVDS data lane 15
DOUTP15	T9		
DOUTM16	U10	O	LVDS data lane 16
DOUTP16	U9		
DVDD_1P2	A7, B8, C8, D8, F7, G7, M7, N7, R8, T6, T8, U8, V7	P	1.2-V digital supply voltage
DVDD_1P8	E8, F8, G8, J10, M8, N8, P8	P	1.8-V digital supply voltage
DVSS	A8, D7, E7, H7, H8, J7, J8, K7, K8, K10, L7, L8, R6, V8	G	Digital ground
FCLKM	K9	O	LVDS frame clock output
FCLKP	J9		
INM1	B3	I	Differential analog input 1 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP1	A3		
INM2	A1	I	Differential analog input 2 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP2	A2		
INM3	B1	I	Differential analog input 3 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP3	B2		
INM4	D3	I	Differential analog input 4 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP4	C3		
INM5	C1	I	Differential analog input 5 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP5	C2		
INM6	D1	I	Differential analog input 6 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP6	D2		
INM7	E1	I	Differential analog input 7 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP7	E2		
INM8	E3	I	Differential analog input 8 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP8	E4		
INM9	F1	I	Differential analog input 9 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP9	F2		
INM10	F3	I	Differential analog input 10 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP10	F4		
INM11	G1	I	Differential analog input 11 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP11	G2		
INM12	G3	I	Differential analog input 12 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP12	G4		
INM13	H1	I	Differential analog input 13 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP13	H2		
INM14	H3	I	Differential analog input 14 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP14	H4		
INM15	J1	I	Differential analog input 15 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP15	J2		
INM16	J3	I	Differential analog input 16 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP16	J4		
INM17	K1	I	Differential analog input 17 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP17	K2		

Pin Functions[1] (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
INM18	K3	I	Differential analog input 18 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP18	K4		
INM19	L1	I	Differential analog input 19 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP19	L2		
INM20	L3	I	Differential analog input 20 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP20	L4		
INM21	M1	I	Differential analog input 21 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP21	M2		
INM22	M3	I	Differential analog input 22 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP22	M4		
INM23	N1	I	Differential analog input 23 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP23	N2		
INM24	N3	I	Differential analog input 24 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP24	N4		
INM25	P1	I	Differential analog input 25 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP25	P2		
INM26	P3	I	Differential analog input 26 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP26	P4		
INM27	R1	I	Differential analog input 27 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP27	R2		
INM28	R3	I	Differential analog input 28 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP28	T3		
INM29	T1	I	Differential analog input 29 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP29	T2		
INM30	U1	I	Differential analog input 30 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP30	U2		
INM31	V1	I	Differential analog input 31 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP31	V2		
INM32	U3	I	Differential analog input 32 pins; see Table 1 for mapping to external inputs in 8-, 16-, and 32-input modes
INP32	V3		
NC	D5, E5, N5, P5	—	Do not connect; leave floating.
PDN_FAST	C6	I	Fast power-down control pin (active high) with an internal pulldown resistor of 20 kΩ. For active high, a 1.8-V logic level is recommended.
PDN_GBL	C7	I	Global power-down control input (active high) with an internal pulldown resistor of 20 kΩ. For active high, a 1.8-V logic level is recommended.
SPI_DIG_EN	B6	I	Reserved for digital functionality. This pin can be left floating or be connected to the 1.8-V supply. This pin has an internal pullup resistor of 20 kΩ.
RESET	A6	I	Hardware reset pin (active high) with an internal pulldown resistor of 20 kΩ. For active high, a 1.8-V logic level is recommended.
SCLK	B7	I	Serial interface clock input with an internal pulldown resistor of 20 kΩ. For active high, a 1.8-V logic level is recommended.
SDIN	A5	I	Serial interface data input with an internal pulldown resistor of 20 kΩ. For active high, a 1.8-V logic level is recommended.
SDOUT	C5	O	Serial interface data readout. High impedance when readout is disabled. 1.8-V logic level is recommended.
SEN	B5	I	Serial interface enable with an internal pullup resistor of 20 kΩ. 1.8-V logic level is recommended.
TX_TRIG	D6	I	1.8-V logic; a pulse on TX_TRIG must be applied after power-up to ensure that all internal clock dividers are synchronized[2].Has an internal pull-down resistor of 20 kΩ to ground.
SYNCM_SERDES	P7	I	Frame synchronization input as per JESD204B standard
SYNCP_SERDES	R7		

(2) See the *Device Synchronization Using TX_TRIG* section for more details on synchronization using TX_TRIG.

Pin Functions(1) (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SYSREFM_SERDES	T7	I	Frame clock and local multiframe clock (LMFC) synchronization input as per JESD204B, subclass 1 standard
SYSREFP_SERDES	U7		
VCM	F5	O	Common-mode output pin for biasing analog input signals. Connect a 10-µF capacitor to ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	AVDD_1P8	–0.3	2.2	V
	DVDD_1P2	–0.3	1.35	
	DVDD_1P8	–0.3	2.2	
Analog input pins (INM_i, INP_i)		–0.3	Minimum [2.2, (AVDD_1P8 + 0.3)]	V
CLKP, CLKM		–0.3	Minimum [2.2, (AVDD_1P8 + 0.3)]	V
Digital control pins	PDN_GBL, PDN_FAST, RESET, SCLK, SDIN, SEN, TX_TRIG, SPI_DIG_EN, SYNCM_SERDES, SYNCP_SERDES, SYSREFM_SERDES, SYSREFP_SERDES	–0.3	Minimum [2.2, (DVDD_1P8 + 0.3)]	V
Maximum operating junction temperature, T_{JMax}			105	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
TEMPERATURE						
T_A	Ambient		–40		85	°C
SUPPLIES						
$V_{(AVDD\_1P8)}$	1.8-V analog supply voltage		1.7	1.8	1.9	V
$V_{(DVDD\_1P8)}$	1.8-V digital supply voltage		1.7	1.8	1.9	V
$V_{(DVDD\_1P2)}$	1.2-V digital supply voltage		1.15	1.2	1.25	V
ANALOG INPUT						
$V_{(INx)}$	Voltage range at analog input pins		VCM – 0.5		VCM + 0.5	V
$V_{IN(CM)}$	Input common-mode range at analog input pins		0.7	0.8	0.9	V
$V_{IN(FS)}$	Input differential full-scale voltage			2		V_{PP}
F_{IN}	Analog input frequency range[1]		0		70	MHz
ANALOG OUTPUT						
$I_{(VCM)}$	External loading on VCM pin	±50-mV change in VCM			100	µA
CLOCK INPUT						
f_S	System clock frequency	16-input mode, 10-bit ADC resolution	5		100	MSPS
		16-input mode, 12-bit ADC resolution	5		80	
		16-input mode, 14-bit ADC resolution	5		65	
		32-input mode, 10-bit ADC resolution	5		100	
		32-input mode, 12-bit ADC resolution	5		80	
		32-input mode, 14-bit ADC resolution	5		65	
		8-input mode, 10-bit ADC resolution	10		200	
$V_{CLKP} – V_{CLKM}$	Differential clock amplitude	Sine-wave, ac-coupled	0.7			V_{PP}
		LVPECL, ac-coupled		1.6		
		LVDS, ac-coupled	0.35	0.7		
V_{CLKP}	Single-ended clock amplitude	LVCMOS on CLKP with CLKM grounded		1.8		V_{PP}
	Input clock duty cycle		40%	50%	60%	
DIGITAL INPUTS						
V_{IH}	Digital input minimum, high level		0.75 × DVDD_1P8	1.8		V
V_{IL}	Digital input maximum, low level			0	0.25 × DVDD_1P8	V
DIGITAL OUTPUT (LVDS)						
R_{LOAD}	Differential load resistance	Between DOUTP and DOUTM		100		Ω
DIGITAL OUTPUT (CML)						
R_{CML}	Load resistance from each CML output to a common mode			50		Ω

(1) Performance degradation may be seen at high input frequencies.

7.4 Thermal Information

THERMAL METRIC[1]		ADS52J90 ZZE (NFBGA) 198 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	4.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Typical values are across ADC resolution and input modes, unless otherwise specified. Typical values are at 25°C, AVDD_1P8 = DVDD_1P8 = 1.8 V, DVDD_1P2 = 1.2 V. External 100-Ω differential load between LVDS outputs, 4-pF load capacitor from each LVDS output to ground, and 1X data rate mode.
All ADCs are powered up and the input signal is a –1-dBFS tone at 5 MHz applied on one channel at a time.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC						
N_{adc}	ADC resolution	32-channel input, 16-channel input	10		14	Bits
		8-channel input		10		
	Number of ADCs			16		ADCs
CLOCK DOMAINS						
f_C	Conversion rate of each ADC (conversion clock frequency)	10-bit ADC resolution			100	MSPS
		12-bit ADC resolution			80	
		14-bit ADC resolution			65	
f_S	System clock frequency in terms of f_C	16-input mode		f_C		MSPS
		32-input mode		f_C		
		8-input mode		$2 \times f_C$		
f_{SAMP}	Effective sampling rate of each input channel in terms of f_C	16-input mode		f_C		MSPS
		32-input mode		$0.5 \times f_C$		
		8-input mode		$2 \times f_C$		
PERFORMANCE						
G_{MATCH}	Gain matching	Same device, across channels		±0.1		dB
		Same channel, across devices		±0.1		
G_{DRIFT}	Gain drift with temperature over full temperature range			0.1		dB
V_{OFF}	Offset error			–7 to 7		mV
DNL	Differential nonlinearity of the ADC	10-bit resolution		–0.5 to 0.5		LSB
		12-bit resolution		–0.9 to 0.9		
		14-bit resolution		–1 to 2		
INL	Integral nonlinearity of the ADC	10-bit resolution		–0.5 to 0.5		LSB
		12-bit resolution		–1 to 1		
		14-bit resolution		–3 to 3		
SNR	Signal-to-noise ratio: excludes first 9 harmonics as well as spurs at ($f_S / 2 \pm f_{IN}$), ($f_S / 4 \pm f_{IN}$), $f_S / 2$, and $f_S / 4$	10-bit, 16-channel input mode, f_{SAMP} = 100 MSPS		61.3		dBFS
		10-bit, 32-channel input mode, f_{SAMP} = 50 MSPS		61.3		
		10-bit mode, 8-channel input, f_{SAMP} = 200 MSPS	56	60		
		10-bit mode, 8-channel input, f_{SAMP} = 130 MSPS	58.2	61		
		12-bit mode, 16- channel input, f_{SAMP} = 80 MSPS		69.5		
		12-bit mode, 32-channel input, f_{SAMP} = 40 MSPS	65	69.5		
		12-bit mode, 32-channel input, f_{SAMP} = 20 MSPS	67.5	70.2		
		14-bit mode, 16- channel input, f_{SAMP} = 65 MSPS	65.9	72.5		
		14-bit mode, 16- channel input, f_{SAMP} = 50 MSPS	67.9	73.5		
		14-bit mode, 32-channel input, f_{SAMP} = 32.5 MSPS		73		
HD2	Second-order harmonic distortion	All input modes and resolutions		–80		dBc
HD3	Third-order harmonic distortion	All input modes and resolutions		–80		dBc
THD	Total harmonic distortion	All input modes and resolutions		–76		dBc
	Magnitude of spur at ($f_S / 2 \pm f_{IN}$)	16-input mode; 10-,12-,14-bit resolutions		–73		dBc
		8-input mode, 10-bit resolution		–62		
	Magnitude of spur at ($f_S / 4 \pm f_{IN}$)	8-input mode, 10-bit resolution		–65		dBc
	Crosstalk	Input spur on neighboring channel with one channel excited at 5 MHz, –1 dBFS		–80		dBc

Electrical Characteristics (continued)

Typical values are across ADC resolution and input modes, unless otherwise specified. Typical values are at 25°C, AVDD_1P8 = DVDD_1P8 = 1.8 V, DVDD_1P2 = 1.2 V. External 100-Ω differential load between LVDS outputs, 4-pF load capacitor from each LVDS output to ground, and 1X data rate mode.
All ADCs are powered up and the input signal is a –1-dBFS tone at 5 MHz applied on one channel at a time.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PERFORMANCE (continued)						
$PSRR_{100kHz}$	AC power-supply rejection ratio: tone at output relative to tone on supply	100-mV_{PP}, 100-kHz tone on supply		–70		dBc
$PSMR_{100kHz}$	AC power-supply modulation ratio: intermodulation tone at output resulting from tones at supply and input measured relative to input tone	100-mV_{PP}, 100-kHz tone on supply and –1-dBFS, 5-MHz tone on input		–80		dBc
CMRR	AC common-mode rejection ratio: tone at output relative to the common-mode tone applied at the analog input pins	50-mV_{PP} common-mode tone at input pins with a frequency of 5 MHz		–40		dBc
TRANSIENT BEHAVIOR						
$N_{OVERLOAD}$	Input overload recovery	5-MHz overload input, 6-dBFS overload		1		Conversion clock
t_{PDN_GBL}	Recovery time from global power-down mode	PDN_GBL from high to low		1		ms
t_{PDN_FAST}	Recovery time from fast power-down mode (standby mode)	PDN_FAST from high to low		15		Conversion clocks
CURRENT CONSUMPTION WITH LVDS INTERFACE ENABLED						
	Current consumption in global power-down mode (PDN_GBL = 1)	AVDD_1P8 current		3		mA
		DVDD_1P8 current		3		
		DVDD_1P2 current		25		
	Current consumption in standby mode (PDN_FAST = 1) at f_C = 100 MSPS	AVDD_1P8 current		80		mA
		DVDD_1P8 current		35		
		DVDD_1P2 current		70		
	Current consumption in active mode at f_C = 100 MSPS(1)	AVDD_1P8 current		190		mA
		DVDD_1P8 current		100		
		DVDD_1P2 current		110		
P_{CH}	Power dissipation in active mode per input channel at f_C = 100 MSPS	16-channel input mode		41		mW/channel
		32-channel input mode		20.5		
		8-channel input mode		82		
CURRENT CONSUMPTION WITH JESD INTERFACE ENABLED						
I_{JESD}	Supply currents: JESD204B interface enabled, LVDS interface disabled at 12-bit, 80-MSPS, 4 ADCs per lane mode	AVDD_1P8 current(1)		170		mA
		DVDD_1P2 current(1)		260		
		DVDD_1P8 current(1)		40		
P_{JESD_CH}	Power dissipation in active mode per input channel: f_C = 80 MSPS, 12-bit mode, LVDS interface disabled, JESD interface enabled (4 ADCs per lane mode)	16-channel input mode		43.1		mW/channel
		32-channel input mode		21.6		

(1) See the *Power Supply Recommendations* section for guidelines on designing the supplies.

7.6 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. Typical values are at 25°C, AVDD_1P8 = DVDD_1P8 = 1.8 V, DVDD_1P2 = 1.2 V, and external differential load resistance between the LVDS output pair (R_{LOAD} = 100 Ω), unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (PDN_FAST, PDN_GBL, RESET, SCLK, SDIN, SEN, TX_TRIG, SPI_DIG_EN)						
V_{IH}	High-level input voltage		1.35			V
V_{IL}	Low-level input voltage				0.45	V
I_{IH}	High-level input current			150		µA
I_{IL}	Low-level input current			150		µA
C_i	Input capacitance			4		pF
DIGITAL OUTPUTS (SDOUT)						
V_{OH}	High-level output voltage		1.6	1.8		V
V_{OL}	Low-level output voltage			0	0.2	V
z_o	Output impedance			50		Ω
LVDS DIGITAL OUTPUTS (DOUTPI, DOUTMI) (1)						
$\|V_{OD}\|$	Output differential voltage	100-Ω external load connected differentially across $DOUTP_I$ and $DOUTM_I$	320	400	480	mV
V_{OS}	Output offset voltage (common-mode voltage of $DOUTP_I$ and $DOUTM_I$)	100-Ω external load connected differentially across $DOUTP_I$ and $DOUTM_I$	0.9	1.03	1.15	V

(1) All digital specifications are characterized across operating temperature range but are not tested at production.

7.7 Timing Requirements: Signal Chain

Typical values are at 25°C. AVDD_1P8 = DVDD_1P8 = 1.8 V, DVDD_1P2 = 1.2 V, and external differential load resistance between the LVDS output pair (R_{LOAD}= 100 Ω), unless otherwise noted. A capacitive load of 4 pF is on the LVDS outputs.

			MIN	TYP	MAX	UNIT
GENERAL						
t_{AP}	Aperture delay			1.6		ns
δt_{AP}	Aperture delay variation from device to device (at same temperature and supply)			±0.5		ns
t_{APJ}	Aperture jitter with LVPECL clock as input clock			0.5		ps
ADC TIMING						
N_{LAT}	ADC latency	Default after reset		8.5		Conversion clocks
		Low-latency mode		4.5		
LVDS TIMING						
f_F	Frame clock frequency	16-input and 8-input modes		f_C		MHz
		32-input mode		f_C / 2		
D_{FRAME}	Frame clock duty cycle			50%		
N_{SER}	Number of bits serialization of each ADC word		10		16	Bits
f_D	Output rate of serialized data for 1X output data rate mode, 16-, 8-. and 32-input modes			$N_{SER} \times f_C$	1000	Mbps
	Output rate of serialized data for 2X output data rate mode, 16-input and 8-input modes			$2 \times N_{SER} \times f_C$	1000	
f_B	Bit clock frequency			f_D / 2	500	MHz
D_{BIT}	Bit clock duty cycle			50%		
t_D	Data bit duration		1	1000 / f_D		ns
t_{PROP}	Clock propagation delay(1)			6 × t_D+ 5		ns
δt_{PROP}	Clock propagation delay variation from device to device (at same temperature and supply)			±2		ns
t_{ORF}	DOUT, DCLK, FCLK rise and fall time, transition time between –100 mV and +100 mV			0.2		ns
t_{OSU}	Minimum serial data, serial clock setup time(2)			t_D / 2 – 0.4		ns
t_{OH}	Minimum serial data, serial clock hold time(2)			t_D / 2 – 0.4		ns
t_{DV}	Minimum data valid window(3)(2)			t_D – 0.65		ns
TX_TRIG TIMING						
$t_{TX\_TRIG\_DEL}$	Delay between TX_TRIG and TX_TRIGD(4)		0.5		0.4 × t_S(5)	ns
$t_{SU\_TX\_TRIGD}$	Setup time related to latching TX_TRIG relative to the rising edge of the system clock			0.6		ns
$t_{H\_TX\_TRIGD}$	Hold time related to latching TX_TRIG relative to the rising edge of the system clock			0.4		ns

(1) See Figure 64 to Figure 68 for the definition of t_{PROP} in various operating modes.
(2) See Figure 1.
(3) The specification for the minimum data valid window is larger than the sum of the minimum setup and hold times because there can be a skew between the ideal transitions of the serial output data with respect to the transition of the bit clock. This skew can vary across channels and across devices. A mechanism to correct this skew can therefore improve the setup and hold timing margins. For example, the LVDS_DCLK_DELAY_PROG control can be used to shift the relative timing of the bit clock with respect to the data.
(4) TX_TRIGD is the internally delayed version of TX_TRIG that gets latched on the rising edge of the system clock.
(5) t_S is the system clock period in ns.

7.8 Timing Requirements: JESD Interface

Typical values are at T_A = 25°C, AVDD_1P8 = 1.8 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, differential ADC clock, R_{LOAD} = 50 Ω from each CML pin to DVDD_1P2, 12-bit ADC resolution, sample rate, and f_C = 80 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C. The JESD204B interface operates in default mode after setting the JESD_EN bit to 1 (12-bit ADC resolution, 12-bit serialization, 4 ADCs per lane, and scrambling disabled).

		MIN	TYP	MAX	UNIT
TIMING CHARACTERISTICS					
f_{JESD}	Serial output data rate in terms of F (number of octets per frame) and f_C (ADC clock frequency in MHz)		0.01 × F × f_C		Gbps
UI	Unit interval	200	1000 / f_{JESD}	2000	ps
Tj	Total jitter: f_{JESD} = 5 Gbps, PRE_EMP = 7, INC_JESD_VDD = 1		0.27		p-p UI
t_R, t_F	Rise and fall time: 20% to 80%, each pin loaded by C_{LOAD} = 1.2 pF to DVDD_1P2		85		ps
SAMPLING TIMING					
t_{SU_S}	Setup time for SYSREF with respect to the device clock rising edge		3		ns
t_{H_S}	Hold time for SYSREF with respect to the device clock rising edge		2		ns
t_{SU_T}	Setup time for SYNC~ with respect to the device clock rising edge		3		ns
t_{H_T}	Hold time for SYNC~ with respect to the device clock rising edge		2		ns
JESD LATENCY					
$N_{A\_SYNC\sim}$	Latency from SYNC~ assertion (falling) edge to start of CGS phase (K28.5) in subclass 0, 1, and 2		17		Device clock cycles
$N_{D\_SYNC\sim}$	Latency from the first LMFC boundary after SYNC~ deassertion (rising) edge to start of ILA phase (K28.0) in subclass 1		11		Device clock cycles
N_{LAT_JESD}	Latency from the device clock falling edge sampling the analog input of ADC1 to the appearance of the corresponding octets on the JESD outputs		14.5		Device clock cycles
JESD DIGITAL OUTPUTS					
$V_{OH\text{-}CML}$	High-level output voltage of the CML output (CMLx_OUTP, CMLx_OUTM)		DVDD_1P2		V
$V_{OL\text{-}CML}$	Low-level output voltage of the CML output (CMLx_OUTP, CMLx_OUTM)		DVDD_1P2 – 0.4		V
$\lvert V_{OD\text{-}CML} \rvert$	Differential output voltage of CMLx_OUT		0.4		V
$V_{OC\text{-}CML}$	Common-mode output voltage of CMLx_OUTP, CMLx_OUTM		DVDD_1P2 – 0.2		V
z_{OS}	Single-ended output impedance		50 ± 25%		Ω
C_{CML}	Output capacitance inside device from either CML output to ground		1		pF
	Transmitter short-circuit current: transmitter terminals shorted to any voltage between –0.25 V and 1.45 V		±100		mA

7.9 Timing Requirements: Serial Interface(1)(2)

		MIN	TYP	MAX	UNIT
t_{SCLK}	SCLK period	50			ns
t_{SCLK_H}	SCLK high time	20			ns
t_{SCLK_L}	SCLK low time	20			ns
t_{DSU}	Data setup time	5			ns
t_{DHO}	Data hold time	5			ns
t_{SEN_SU}	SEN falling edge to SCLK rising edge	8			ns
t_{SEN_HO}	Time between last SCLK rising edge to SEN rising edge	8			ns
t_{OUT_DV}	SDOUT delay	12	20	28	ns

(1) Characterized in lab over operating temperature range, not tested at production testing.
(2) See Figure 92 and Figure 93.

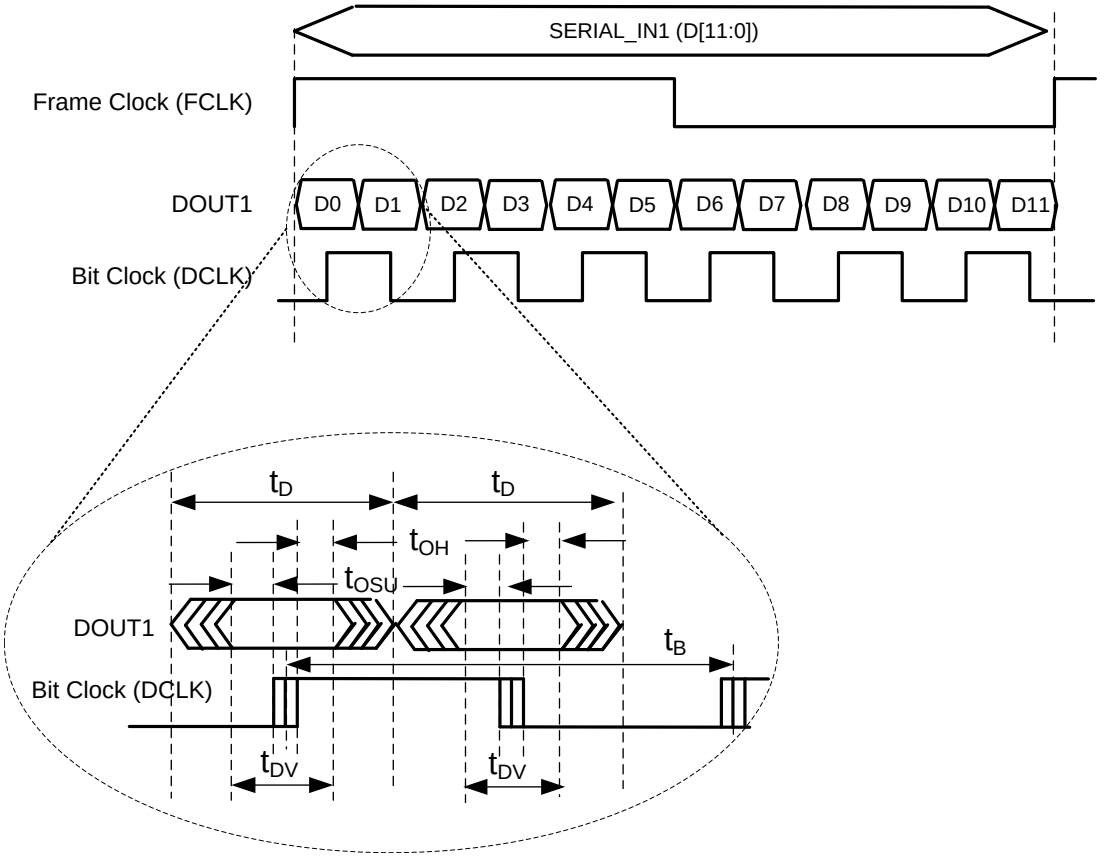
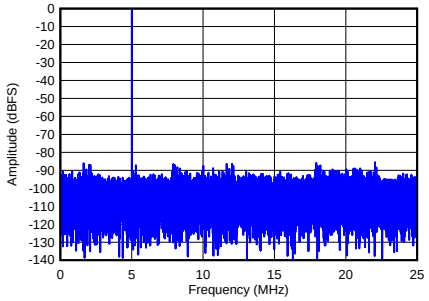


Figure 1. LVDS Output Signals Timing Diagram in 16-Input Mode with 12-Bit Serialization, LSB-First, 1X Data Rate Mode

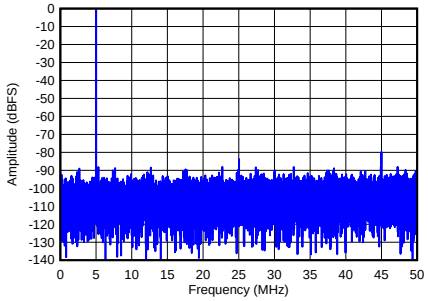
7.10 Typical Characteristics

At 25°C, AVDD_IP8 = DVDD_1P8 = 1.8 V, and DVDD_1P2 = 1.2 V, unless otherwise noted. All LVDS outputs are active with 100-Ω differential terminations and a 4-pF load capacitor from each LVDS output pin to ground. A –1-dBFS input signal at 5 MHz is applied to the input channel under test. SNR is computed by ignoring the power contained in the first nine harmonic bins, the f_S / 2 and f_S / 4 frequency bins as well as the bins corresponding to the intermodulation frequencies between the input and the clock. A LVPECL clock is used as the clock source.



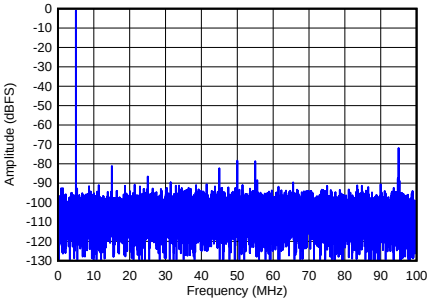
f_{IN} = 5 MHz, f_C = 100 MSPS, SNR = 61.5 dBFS, SFDR = 81.9 dBc, HD2 = –86.5 dBc, HD3 = –93.9 dBc

Figure 2. FFT of 10-Bit, 32-Input Mode



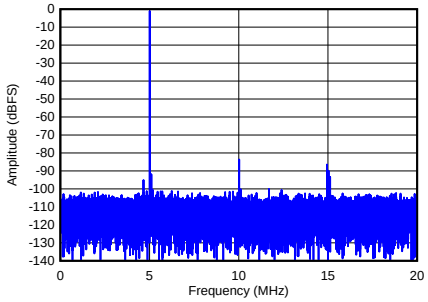
f_{IN} = 5 MHz, f_C = 100 MSPS, SNR = 61.6 dBFS, SFDR = 78.7 dBc, HD2 = –97.6 dBc, HD3 = –92.2 dBc

Figure 3. FFT of 10-Bit, 16-Input Mode



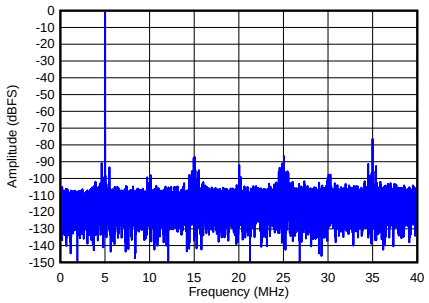
f_{IN} = 5 MHz, f_C = 100 MSPS, SNR = 61.3 dBFS, SFDR = 70.8 dBc, HD2 = –94.2 dBc, HD3 = –80.1 dBc

Figure 4. FFT of 10-Bit, 8-Input Mode



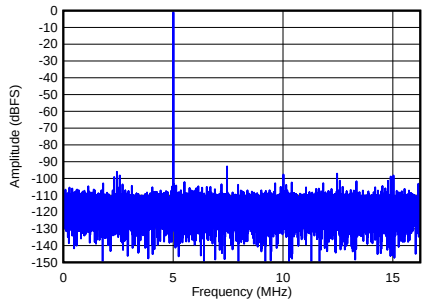
f_{IN} = 5 MHz, f_C = 80 MSPS, SNR = 69.9 dBFS, SFDR = 82.6 dBc, HD2 = –82.6 dBc, HD3 = –88.9 dBc

Figure 5. FFT of 12-Bit, 32-Input Mode



f_{IN} = 5 MHz, f_C = 80 MSPS, SNR = 70.2 dBFS, SFDR = 75.4 dBc, HD2 = –109.8 dBc, HD3 = –86.1 dBc

Figure 6. FFT of 12-Bit, 16-Input Mode

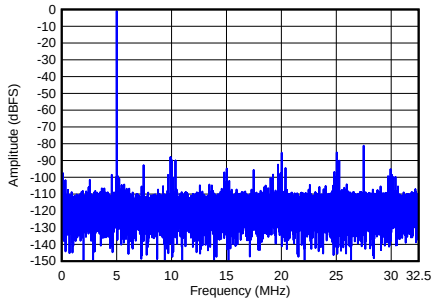


f_{IN} = 5 MHz, f_C = 65 MSPS, SNR = 73.7 dBFS, SFDR = 91.8 dBc, HD2 = –96.6 dBc, HD3 = –97.2 dBc

Figure 7. FFT of 14-Bit, 32-Input Mode

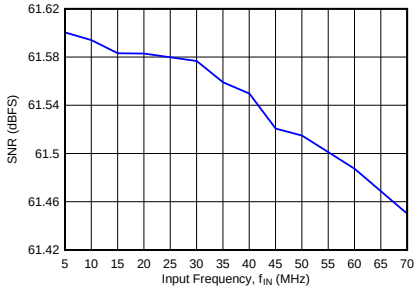
Typical Characteristics (continued)

At 25°C, AVDD_IP8 = DVDD_1P8 = 1.8 V, and DVDD_1P2 = 1.2 V, unless otherwise noted. All LVDS outputs are active with 100-Ω differential terminations and a 4-pF load capacitor from each LVDS output pin to ground. A –1-dBFS input signal at 5 MHz is applied to the input channel under test. SNR is computed by ignoring the power contained in the first nine harmonic bins, the f_S / 2 and f_S / 4 frequency bins as well as the bins corresponding to the intermodulation frequencies between the input and the clock. A LVPECL clock is used as the clock source.



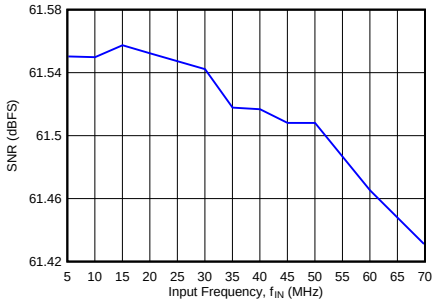
f_{IN} = 5 MHz, f_C = 65 MSPS, SNR = 73.4 dBFS, SFDR = 80.2 dBc, HD2 = –88.7 dBc, HD3 = –93.9 dBc

Figure 8. FFT of 14-Bit, 16-Input Mode



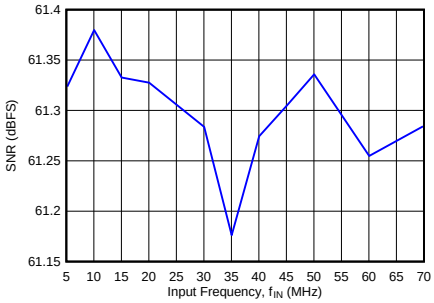
f_{SAMP} = 50 MSPS

Figure 9. Signal-to-Noise Ratio vs f_{IN} in 10-Bit, 32-Input Mode



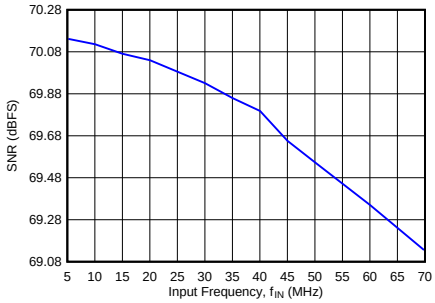
f_{SAMP} = 100 MSPS

Figure 10. Signal-to-Noise Ratio vs f_{IN} in 10-Bit, 16-Input Mode



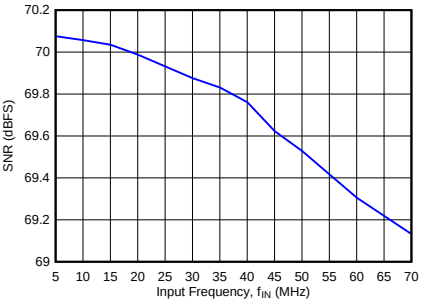
f_{SAMP} = 200 MSPS

Figure 11. Signal-to-Noise Ratio vs f_{IN} in 10-Bit, 8-Input Mode



f_{SAMP} = 40 MSPS

Figure 12. Signal-to-Noise Ratio vs f_{IN} in 12-Bit, 32-Input Mode

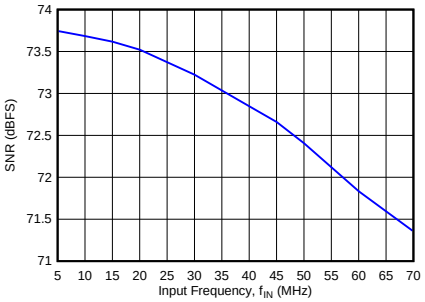


f_{SAMP} = 80 MSPS

Figure 13. Signal-to-Noise Ratio vs f_{IN} in 12-Bit, 16-Input Mode

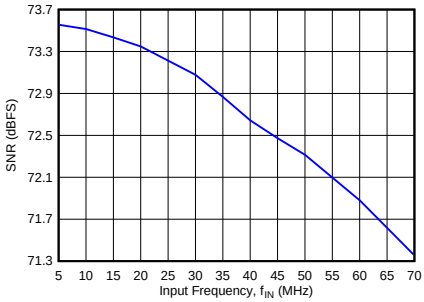
Typical Characteristics (continued)

At 25°C, AVDD_IP8 = DVDD_1P8 = 1.8 V, and DVDD_1P2 = 1.2 V, unless otherwise noted. All LVDS outputs are active with 100-Ω differential terminations and a 4-pF load capacitor from each LVDS output pin to ground. A –1-dBFS input signal at 5 MHz is applied to the input channel under test. SNR is computed by ignoring the power contained in the first nine harmonic bins, the f_S / 2 and f_S / 4 frequency bins as well as the bins corresponding to the intermodulation frequencies between the input and the clock. A LVPECL clock is used as the clock source.



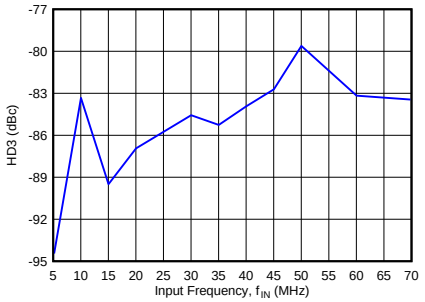
f_{SAMP} = 32.5 MSPS

Figure 14. Signal-to-Noise Ratio vs f_{IN} in 14-Bit, 32-Input Mode



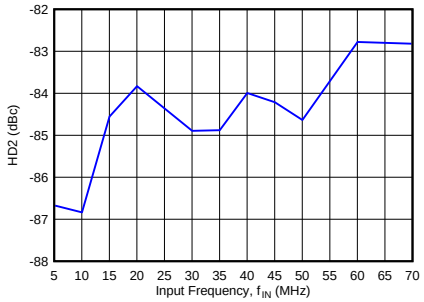
f_{SAMP} = 65 MSPS

Figure 15. Signal-to-Noise Ratio vs f_{IN} in 14-Bit, 16-Input Mode



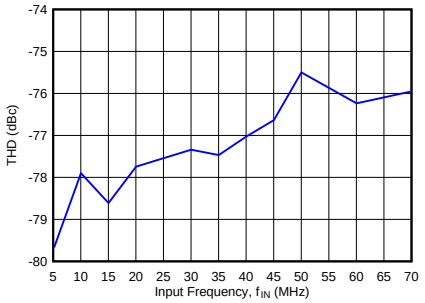
100-MSPS conversion clock

Figure 16. Third-Order Harmonic Distortion vs f_{IN}



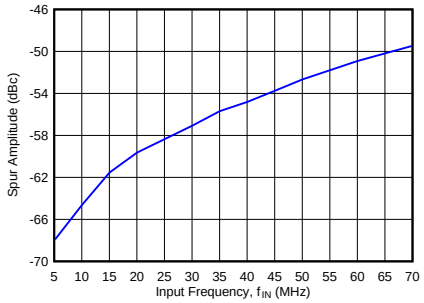
100-MSPS conversion clock

Figure 17. Second-Order Harmonic Distortion vs f_{IN}



100-MSPS conversion clock

Figure 18. Total Harmonic Distortion vs f_{IN}

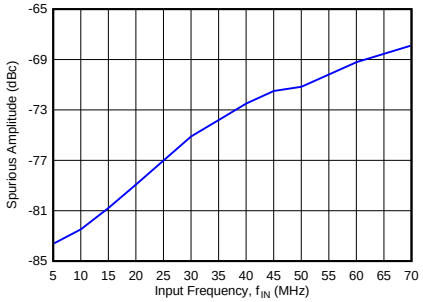


f_{SAMP} = 200 MSPS

Figure 19. Input-Clock Intermodulation Spur at (f_S / 2 ± f_{IN}) vs f_{IN} in 8-Input Mode

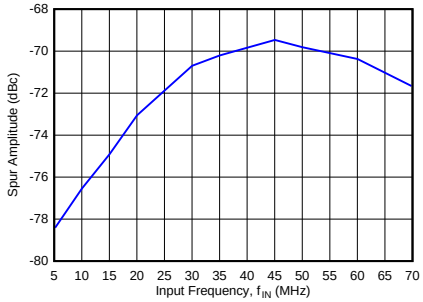
Typical Characteristics (continued)

At 25°C, AVDD_IP8 = DVDD_1P8 = 1.8 V, and DVDD_1P2 = 1.2 V, unless otherwise noted. All LVDS outputs are active with 100-Ω differential terminations and a 4-pF load capacitor from each LVDS output pin to ground. A –1-dBFS input signal at 5 MHz is applied to the input channel under test. SNR is computed by ignoring the power contained in the first nine harmonic bins, the f_S / 2 and f_S / 4 frequency bins as well as the bins corresponding to the intermodulation frequencies between the input and the clock. A LVPECL clock is used as the clock source.



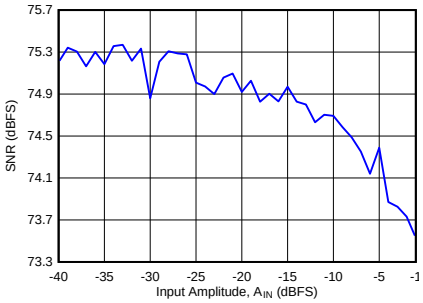
f_{SAMP} = 100 MSPS

Figure 20. Input-Clock Intermodulation Spur at (f_S / 2 ± f_{IN}) vs f_{IN} in 16-Input Mode



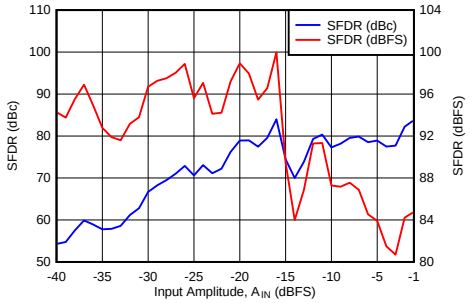
f_{SAMP} = 200 MSPS

Figure 21. Input-Clock Intermodulation Spur at (f_S / 4 ± f_{IN}) vs f_{IN} in 8-Input Mode



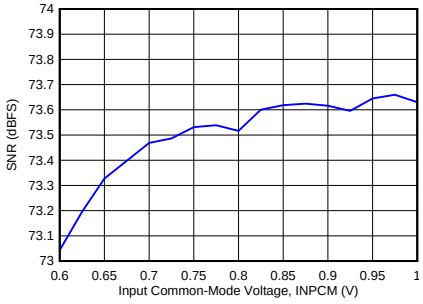
16-input mode, 14-bit resolution, f_{SAMP} = 65 MSPS

Figure 22. Signal-to-Noise Ratio vs A_{IN}



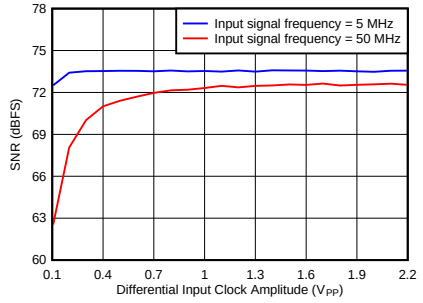
32-input mode, 14-bit resolution, f_{SAMP} = 32.5 MSPS

Figure 23. Spurious-Free Dynamic Range vs A_{IN}



16-input mode, 14-bit resolution, f_{SAMP} = 65 MSPS

Figure 24. Signal-to-Noise Ratio vs Input Common-Mode Voltage (INPCM)

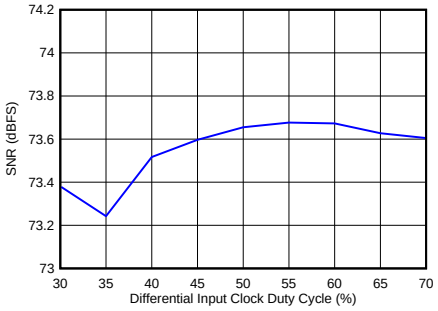


16-input mode, 14-bit resolution, f_{SAMP} = 65 MSPS

Figure 25. Signal-to-Noise Ratio vs Amplitude of Differential Sine-Wave Input Clock

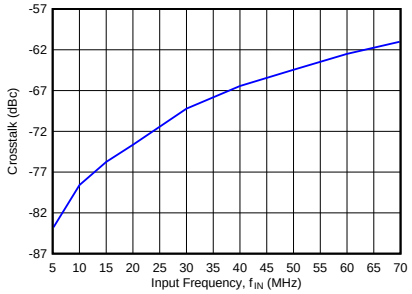
Typical Characteristics (continued)

At 25°C, AVDD_IP8 = DVDD_1P8 = 1.8 V, and DVDD_1P2 = 1.2 V, unless otherwise noted. All LVDS outputs are active with 100-Ω differential terminations and a 4-pF load capacitor from each LVDS output pin to ground. A –1-dBFS input signal at 5 MHz is applied to the input channel under test. SNR is computed by ignoring the power contained in the first nine harmonic bins, the f_S / 2 and f_S / 4 frequency bins as well as the bins corresponding to the intermodulation frequencies between the input and the clock. A LVPECL clock is used as the clock source.



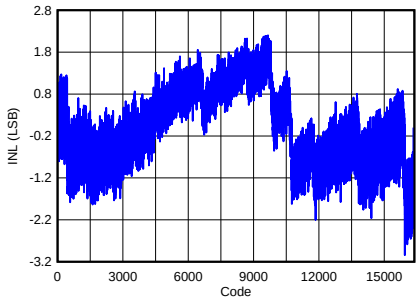
16-input mode, 14-bit resolution, f_{SAMP} = 65 MSPS

Figure 26. Signal-to-Noise Ratio vs Differential Input Clock Duty Cycle



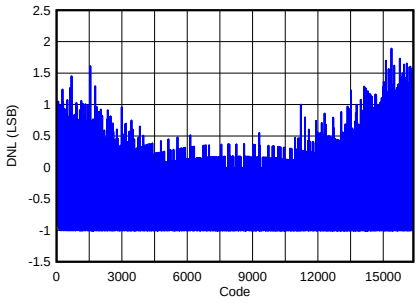
32-input mode, 14-bit resolution, f_{SAMP} = 32.5 MSPS, –1-dBFS tone applied on one channel and spur on neighboring channel measured as crosstalk

Figure 27. Crosstalk vs f_{IN}



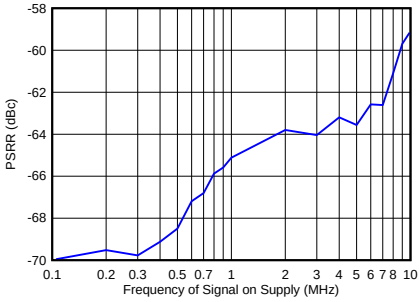
32-input mode, 14-bit resolution, f_{SAMP} = 32.5 MSPS

Figure 28. Integral Nonlinearity



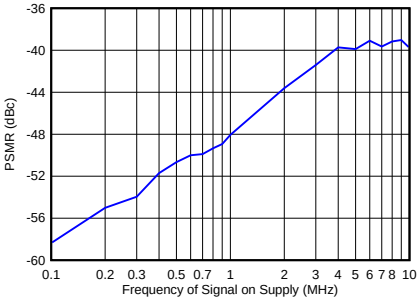
32-input mode, 14-bit resolution, f_{SAMP} = 32.5 MSPS

Figure 29. Differential Nonlinearity



32-input mode, 14-bit resolution, f_{SAMP} = 32.5 MSPS, 100-mV_{PP} tone on supply

Figure 30. Power-Supply Rejection Ratio vs Frequency of Signal on Supply

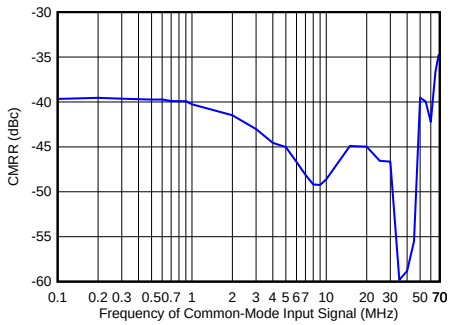


32-input mode; 14-bit resolution; f_{SAMP} = 32.5 MSPS; 100-mV_{PP} tone on supply; 5-MHz, –1-dBFS tone on input; PSMR is intermodulation tone referred to input tone amplitude

Figure 31. Power-Supply Modulation Ratio vs Frequency of Signal on Supply

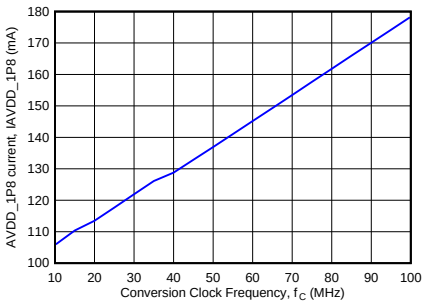
Typical Characteristics (continued)

At 25°C, AVDD_IP8 = DVDD_1P8 = 1.8 V, and DVDD_1P2 = 1.2 V, unless otherwise noted. All LVDS outputs are active with 100-Ω differential terminations and a 4-pF load capacitor from each LVDS output pin to ground. A –1-dBFS input signal at 5 MHz is applied to the input channel under test. SNR is computed by ignoring the power contained in the first nine harmonic bins, the f_S / 2 and f_S / 4 frequency bins as well as the bins corresponding to the intermodulation frequencies between the input and the clock. A LVPECL clock is used as the clock source.



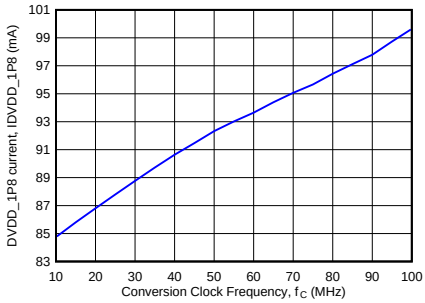
32-input mode, 14-bit resolution, f_{SAMP} = 32.5 MSPS, 50-mV_{PP} common-mode tone applied at the inputs, output tone referred to the input tone

Figure 32. Common-Mode Rejection Ratio vs Frequency of Common-Mode Input Signal



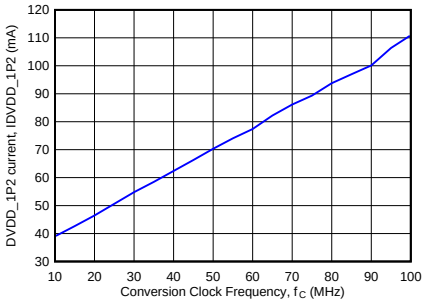
32-input mode, 10-bit resolution

Figure 33. AVDD_1P8 Current vs Conversion Clock Frequency



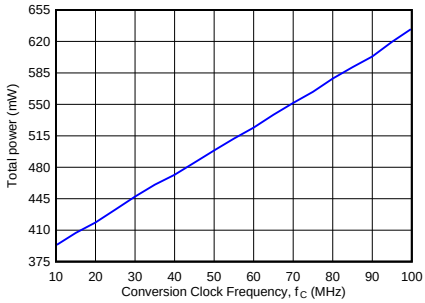
32-input mode, 10-bit resolution

Figure 34. DVDD_1P8 Current vs Conversion Clock Frequency



32-input mode, 10-bit resolution

Figure 35. DVDD_1P2 Current vs Conversion Clock Frequency



32-input mode, 10-bit resolution

Figure 36. Total Power vs Conversion Clock Frequency

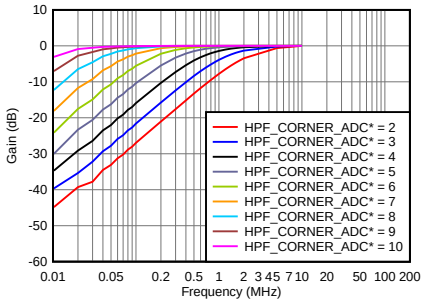
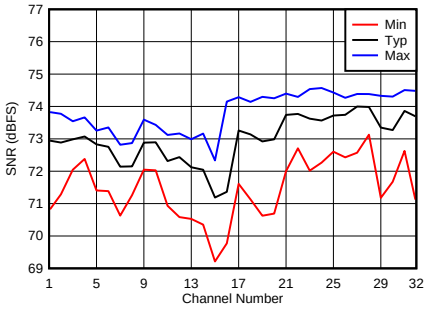


Figure 37. Digital High-Pass Filter Response

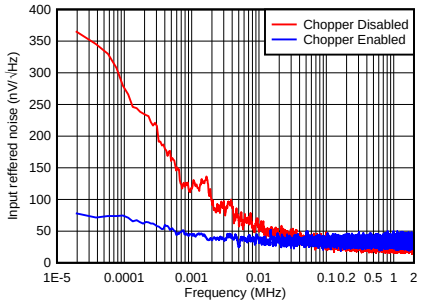
Typical Characteristics (continued)

At 25°C, AVDD_IP8 = DVDD_1P8 = 1.8 V, and DVDD_1P2 = 1.2 V, unless otherwise noted. All LVDS outputs are active with 100-Ω differential terminations and a 4-pF load capacitor from each LVDS output pin to ground. A –1-dBFS input signal at 5 MHz is applied to the input channel under test. SNR is computed by ignoring the power contained in the first nine harmonic bins, the f_S / 2 and f_S / 4 frequency bins as well as the bins corresponding to the intermodulation frequencies between the input and the clock. A LVPECL clock is used as the clock source.



Statistical values taken over 100 devices in 14-bit, 32-input mode at f_{SAMP} = 32.5 MSPS

Figure 38. Signal-to-Noise Ratio Histogram

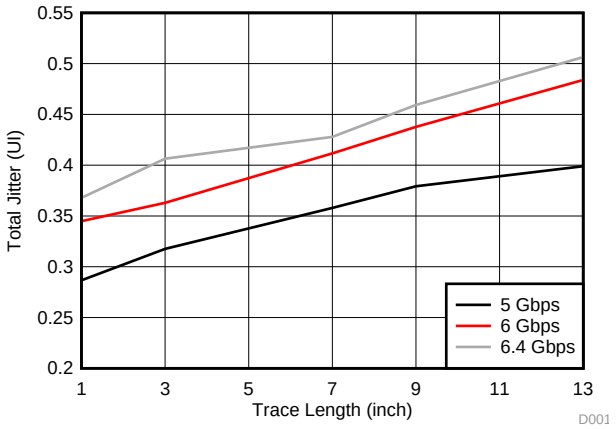


16-input mode, 12-bit resolution

Figure 39. Low-Frequency Noise With and Without Chopper Enabled

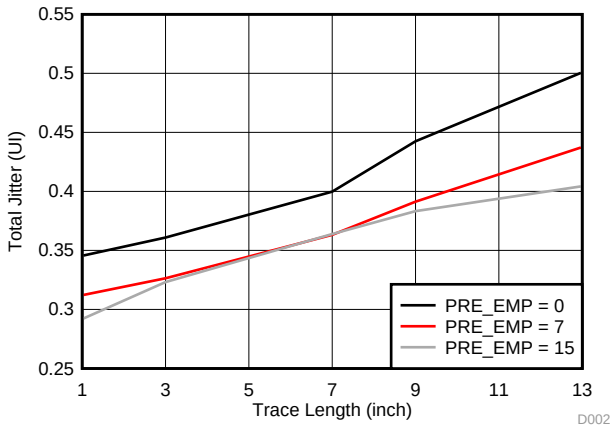
7.11 Typical Characteristics: JESD Interface

Typical values are at T_A = 25°C, AVDD_1P8 = 1.8 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, differential ADC clock, R_{LOAD} = 50 Ω from each CML pin to DVDD_1P2, 12-bit ADC resolution, sample rate, and f_{CLKIN} = 80 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C. The JESD204B interface operates in default mode after setting the JESD_EN bit to 1 (12-bit ADC resolution, 12-bit serialization, 4 ADCs per lane, and scrambling disabled).



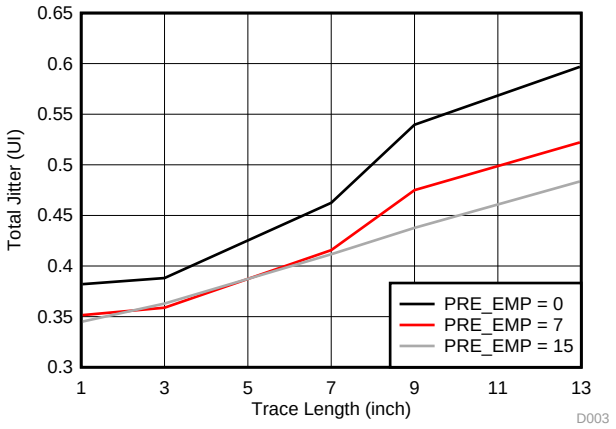
PRE_EMP = 15 , across JESD speeds

Figure 40. Total Jitter vs Trace Length



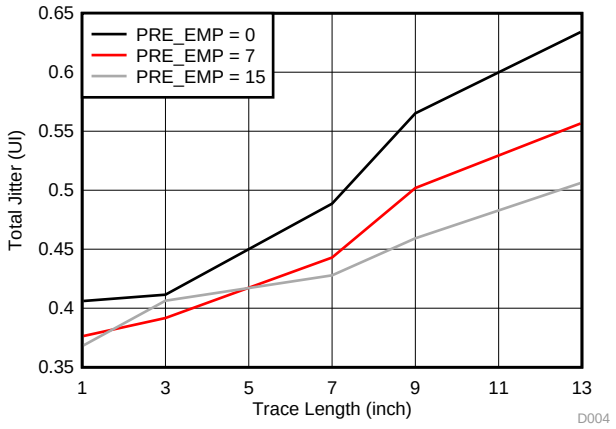
JESD speed = 5 Gbps, across PRE_EMP settings

Figure 41. Total Jitter vs Trace Length



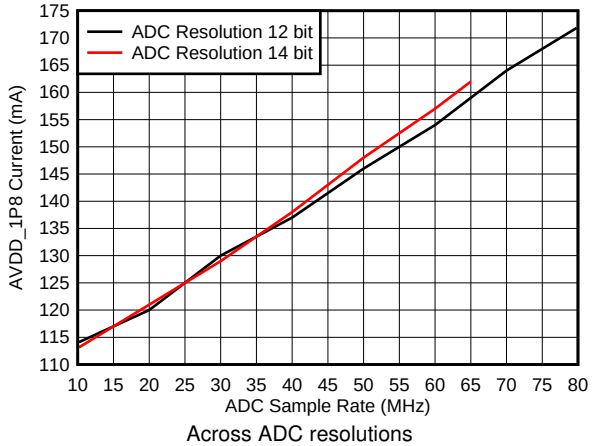
JESD speed = 6 Gbps, across PRE_EMP settings

Figure 42. Total Jitter vs Trace Length



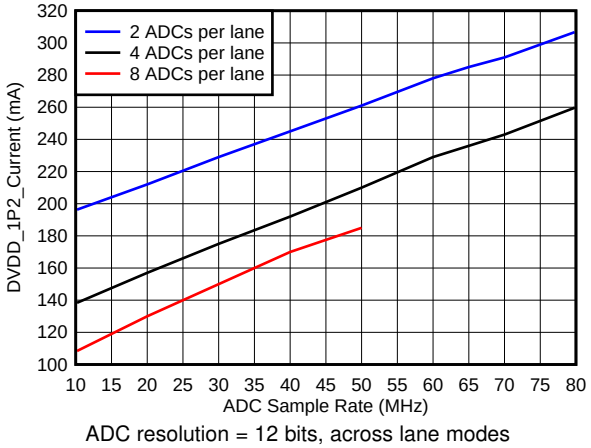
JESD speed = 6.4 Gbps, across PRE_EMP settings

Figure 43. Total Jitter vs Trace Length



Across ADC resolutions

Figure 44. AVDD_1P8 Current vs ADC Sample Rate

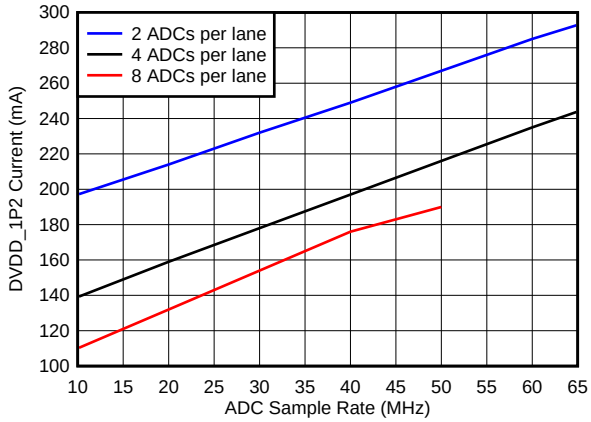


ADC resolution = 12 bits, across lane modes

Figure 45. DVDD_1P2 Current vs ADC Sample Rate

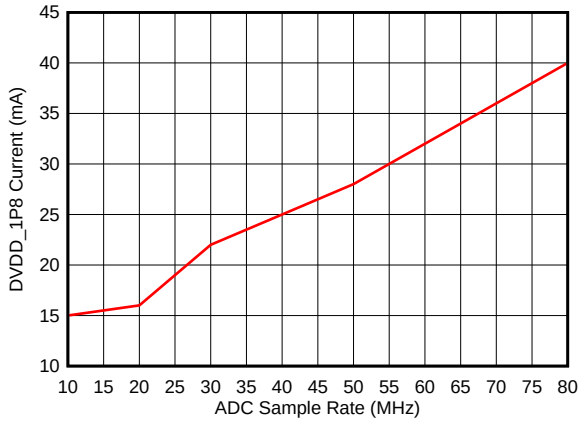
Typical Characteristics: JESD Interface (continued)

Typical values are at T_A = 25°C, AVDD_1P8 = 1.8 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, differential ADC clock, R_{LOAD} = 50 Ω from each CML pin to DVDD_1P2, 12-bit ADC resolution, sample rate, and f_{CLKIN} = 80 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C. The JESD204B interface operates in default mode after setting the JESD_EN bit to 1 (12-bit ADC resolution, 12-bit serialization, 4 ADCs per lane, and scrambling disabled).



ADC resolution = 14 bits, across lane modes

Figure 46. DVDD_1P2 Current vs ADC Sample Rate



ADC resolution = 12, 14 bits; across lane modes

Figure 47. DVDD_1P8 Current vs ADC Sample Rate

7.12 Typical Characteristics: Contour Plots

At 25°C, AVDD_IP8 = DVDD_1P8 = 1.8 V, and DVDD_1P2 = 1.2 V, unless otherwise noted. All LVDS outputs are active with 100-Ω differential terminations and a 4-pF load capacitor from each LVDS output pin to ground. A –1-dBFS input signal at 5 MHz is applied to the input channel under test. SNR is computed by ignoring the power contained in the first nine harmonic bins, the f_S / 2 and f_S / 4 frequency bins as well as the bins corresponding to the intermodulation frequencies between the input and the clock. An LVPECL clock is used as the clock source.

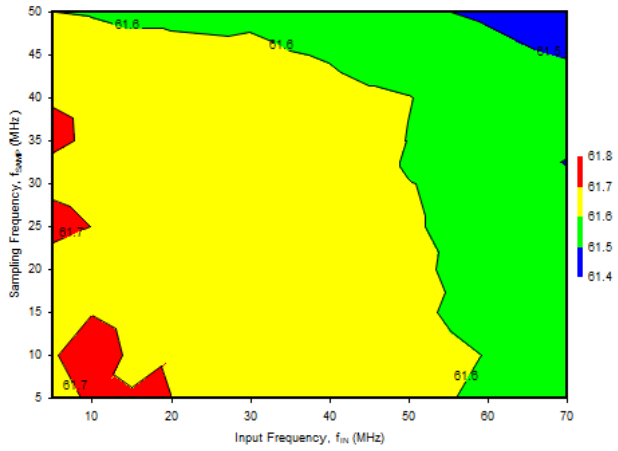


Figure 48. Signal-to-Noise Ratio in 10-Bit, 32-Input Mode

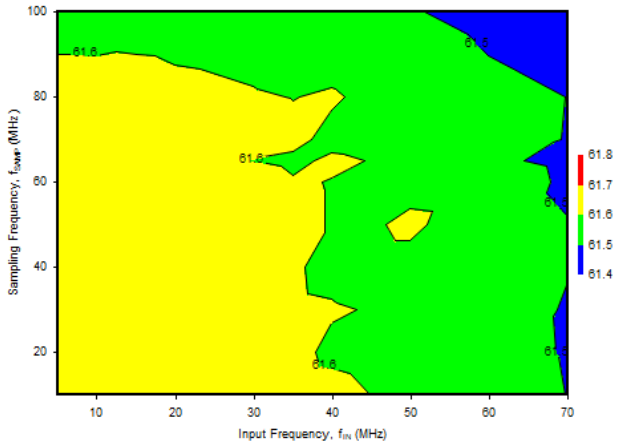


Figure 49. Signal-to-Noise Ratio in 10-Bit, 16-Input Mode

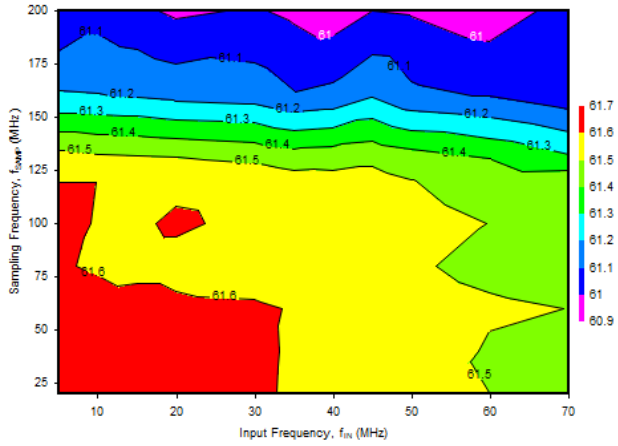


Figure 50. Signal-to-Noise Ratio in 10-Bit, 8-Input Mode

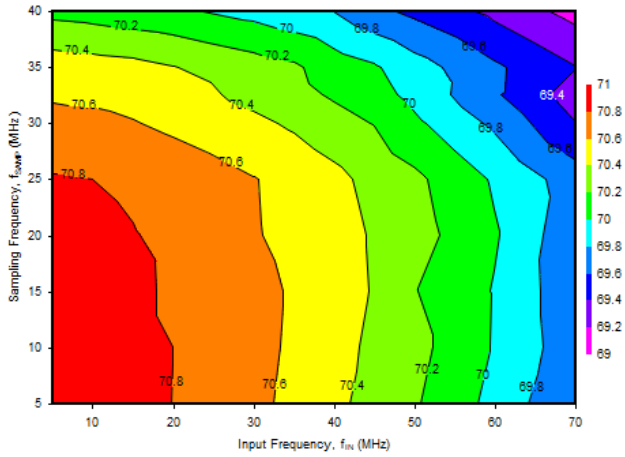


Figure 51. Signal-to-Noise Ratio in 12-Bit, 32-Input Mode

Typical Characteristics: Contour Plots (continued)

At 25°C, AVDD_IP8 = DVDD_1P8 = 1.8 V, and DVDD_1P2 = 1.2 V, unless otherwise noted. All LVDS outputs are active with 100-Ω differential terminations and a 4-pF load capacitor from each LVDS output pin to ground. A –1-dBFS input signal at 5 MHz is applied to the input channel under test. SNR is computed by ignoring the power contained in the first nine harmonic bins, the f_S / 2 and f_S / 4 frequency bins as well as the bins corresponding to the intermodulation frequencies between the input and the clock. An LVPECL clock is used as the clock source.

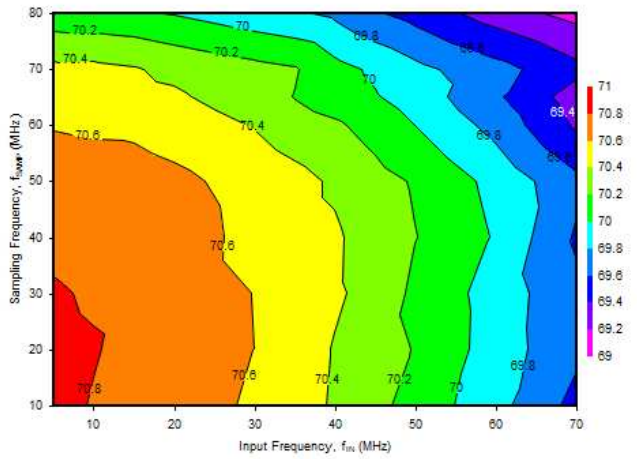


Figure 52. Signal-to-Noise Ratio in 12-Bit, 16-Input Mode

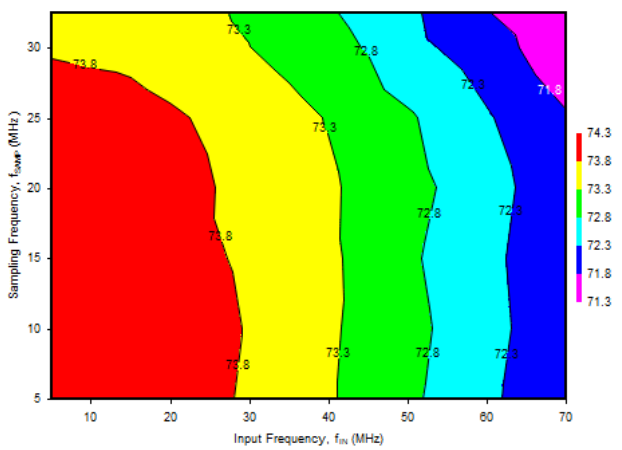


Figure 53. Signal-to-Noise Ratio in 14-Bit, 32-Input Mode

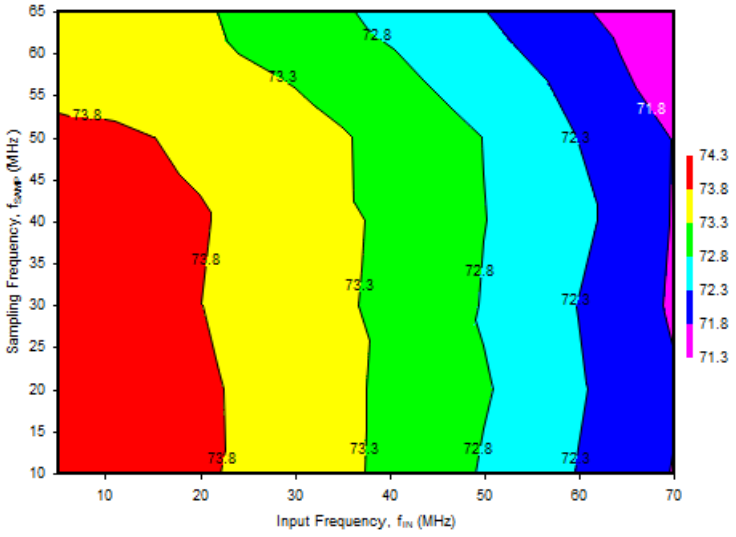


Figure 54. Signal-to-Noise Ratio in 14-Bit, 16-Input Mode

8 Detailed Description

8.1 Overview

A block diagram of the device is shown in Figure 55. Figure 56 illustrates the signal flow for the device while operating with the LVDS output interface. The device consists of 16 ADCs configurable to convert 8-, 16-, or 32-inputs. All ADCs run off the external clocks (provided on the CLKP, CLKM pins). The references needed for the ADCs are internally generated. The reference voltage that can be used to set the common mode voltage of the analog input comes out on the VCM pin. The output data from the 16 ADCs are serialized and output on the LVDS interface. The device also has an optional JESD204B interface. The device is controlled using an SPI interface.

8.2 Functional Block Diagrams

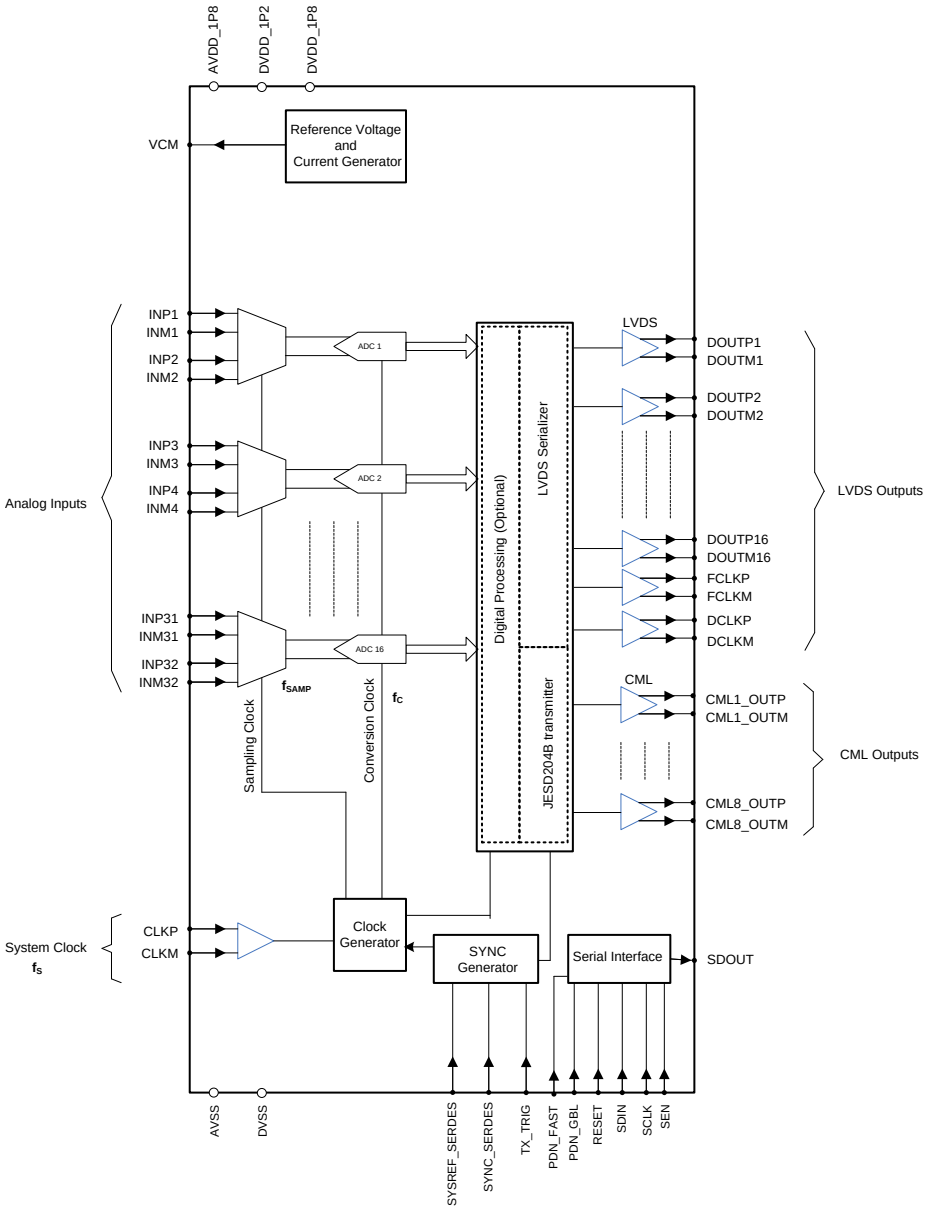


Figure 55. Block Diagram

Functional Block Diagrams (continued)

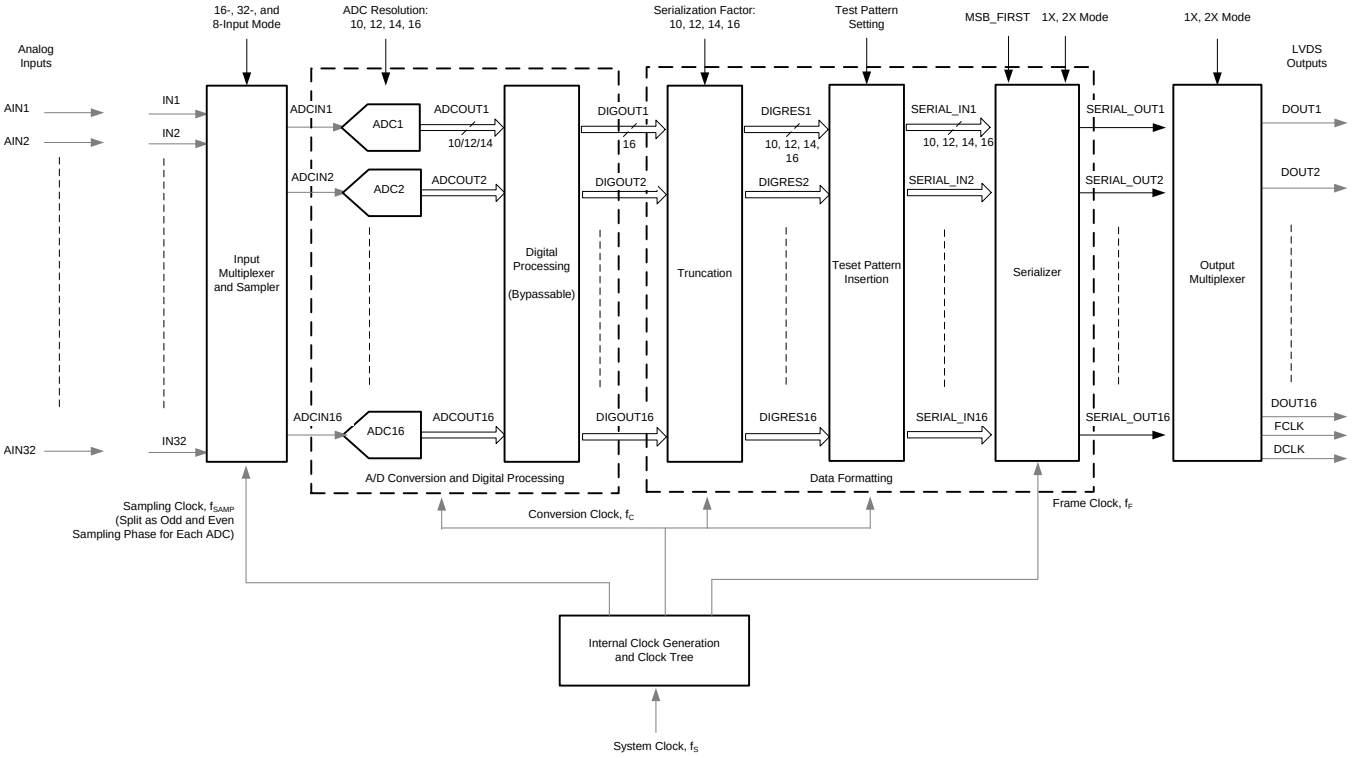


Figure 56. Signal Flow Diagram

8.3 Feature Description

The device has 16 synchronously operating ADCs (ADC1 to ADC16) and can be configured to accept and convert 8, 16, or 32 active differential external analog inputs (AIN1 to AIN32). The converted digital outputs can be made to come out on either 16 pairs of low-voltage differential signaling (LVDS) outputs or compressed into eight pairs. The device operates from a single clock input. This input is referred to as the system clock and its frequency is denoted by f_S. The recommended mode of driving the clock is with a differential low-voltage positive-referenced emitter coupled logic (LVPECL) clock. The system clock can be also driven by a differential sine-wave or LVDS, or can be driven with a single-ended low voltage complementary metal oxide semiconductor (LVCMOS) clock. The various aspects of the signal chain are discussed in the following sections.

Feature Description (continued)

8.3.1 Connection of the External Inputs to the Input Pins

The effective conversion rate per input changes depending on the input mode. The methodology of connecting the external inputs (AINx) to the input pins (INx) is shown in Table 1 for the 16-, 32- and 8-channel input modes. In Table 1, AIN1 refers to the differential input signal (AINP1, AINM1) and IN1 refers to the input pair (INP1, INM1). The voltage that gets sampled and converted by the device is (AINP1-AINM1).

Table 1. Scheme of Driving the Input Pins (16-, 32-, 8-Channel Input Modes)

INPUT PAIR	CONNECTION TO THE EXTERNAL ANALOG INPUT SIGNAL		
	16-CHANNEL INPUT MODE(1)(2)	32-CHANNEL INPUT MODE	8-CHANNEL INPUT MODE(1)
IN1	AIN1	AIN1	AIN1
IN2	—	AIN2	—
IN3	AIN2	AIN3	AIN1
IN4	—	AIN4	—
IN5	AIN3	AIN5	AIN2
IN6	—	AIN6	—
IN7	AIN4	AIN7	AIN2
IN8	—	AIN8	—
IN9	AIN5	AIN9	AIN3
IN10	—	AIN10	—
IN11	AIN6	AIN11	AIN3
IN12	—	AIN12	—
IN13	AIN7	AIN13	AIN4
IN14	—	AIN14	—
IN15	AIN8	AIN15	AIN4
IN16	—	AIN16	—
IN17	AIN9	AIN17	AIN5
IN18	—	AIN18	—
IN19	AIN10	AIN19	AIN5
IN20	—	AIN20	—
IN21	AIN11	AIN21	AIN6
IN22	—	AIN22	—
IN23	AIN12	AIN23	AIN6
IN24	—	AIN24	—
IN25	AIN13	AIN25	AIN7
IN26	—	AIN26	—
IN27	AIN14	AIN27	AIN7
IN28	—	AIN28	—
IN29	AIN15	AIN29	AIN8
IN30	—	AIN30	—
IN31	AIN16	AIN31	AIN8
IN32	—	AIN32	—

(1) — = do not connect.
(2) To switch ADCx to convert the even numbered inputs, use register control IN_16CH_ADCx.

8.3.2 Input Multiplexer and Sampler

The input multiplexer determines the mapping of the input pins (IN1 to IN32) to the inputs that are sampled and converted by the ADCs (ADC1 to ADC16). Each ADC has two sets of sampling circuits (termed odd and even) and alternately converts the inputs presented to them.

The sampling windows for the odd and even sampling circuits of each ADC are derived from the system clock. A pair of ADCs are used in Figure 57, Figure 58, and Figure 59 to illustrate how the odd and even sampling phases are derived for each ADC in each input mode. AIN1 (t_1) refers to the AIN1 input sampled at the t_1 instant. ADC1o refers to the odd sample converted by ADC1 and ADC1e refers to the even sample converted by ADC1. The input sampling and conversion schemes for the 32-, 16-, and 8-input modes are illustrated in Figure 57, Figure 58, and Figure 59, respectively.

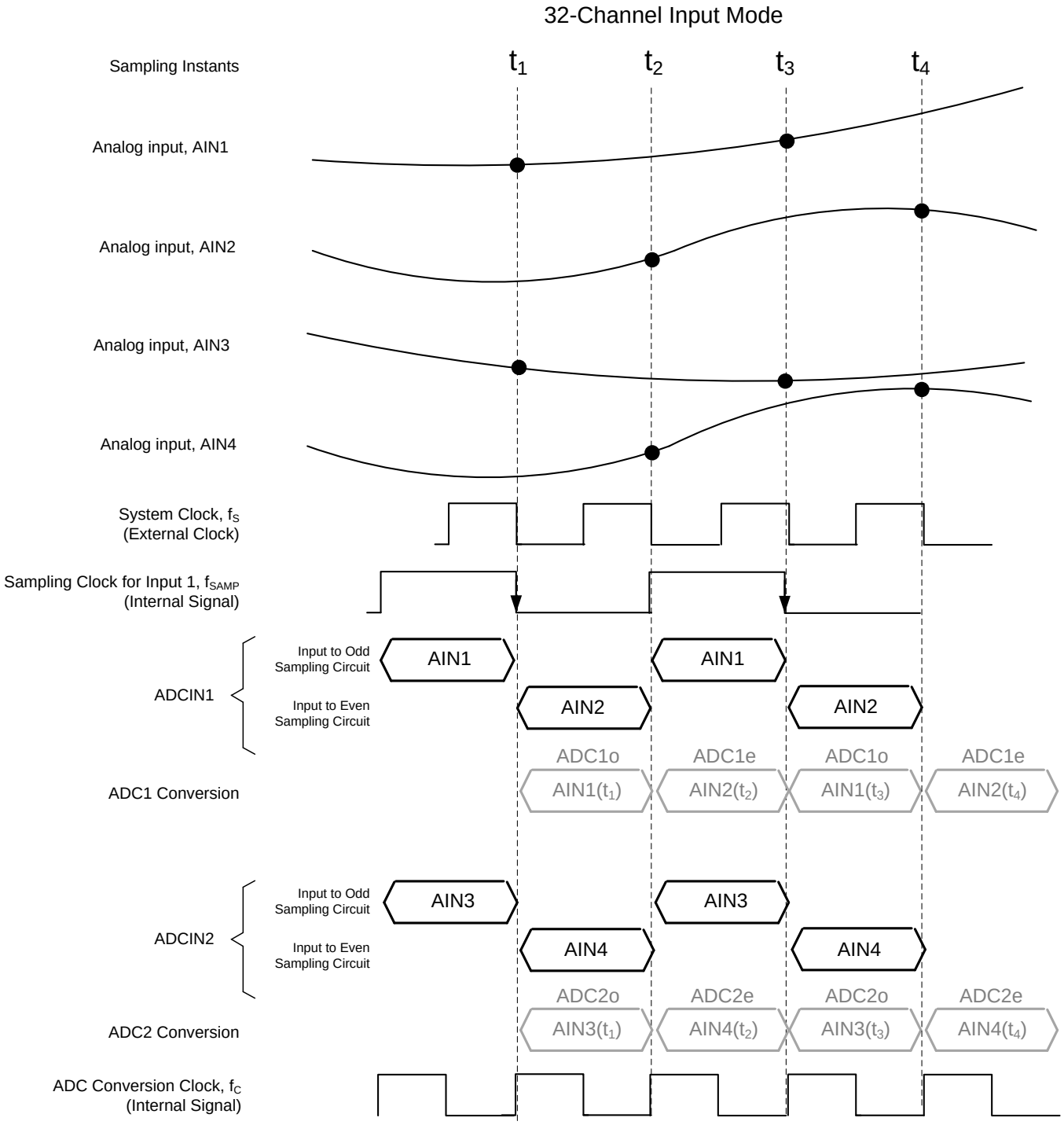


Figure 57. Input Sampling and Conversion Scheme (32-Input Mode)

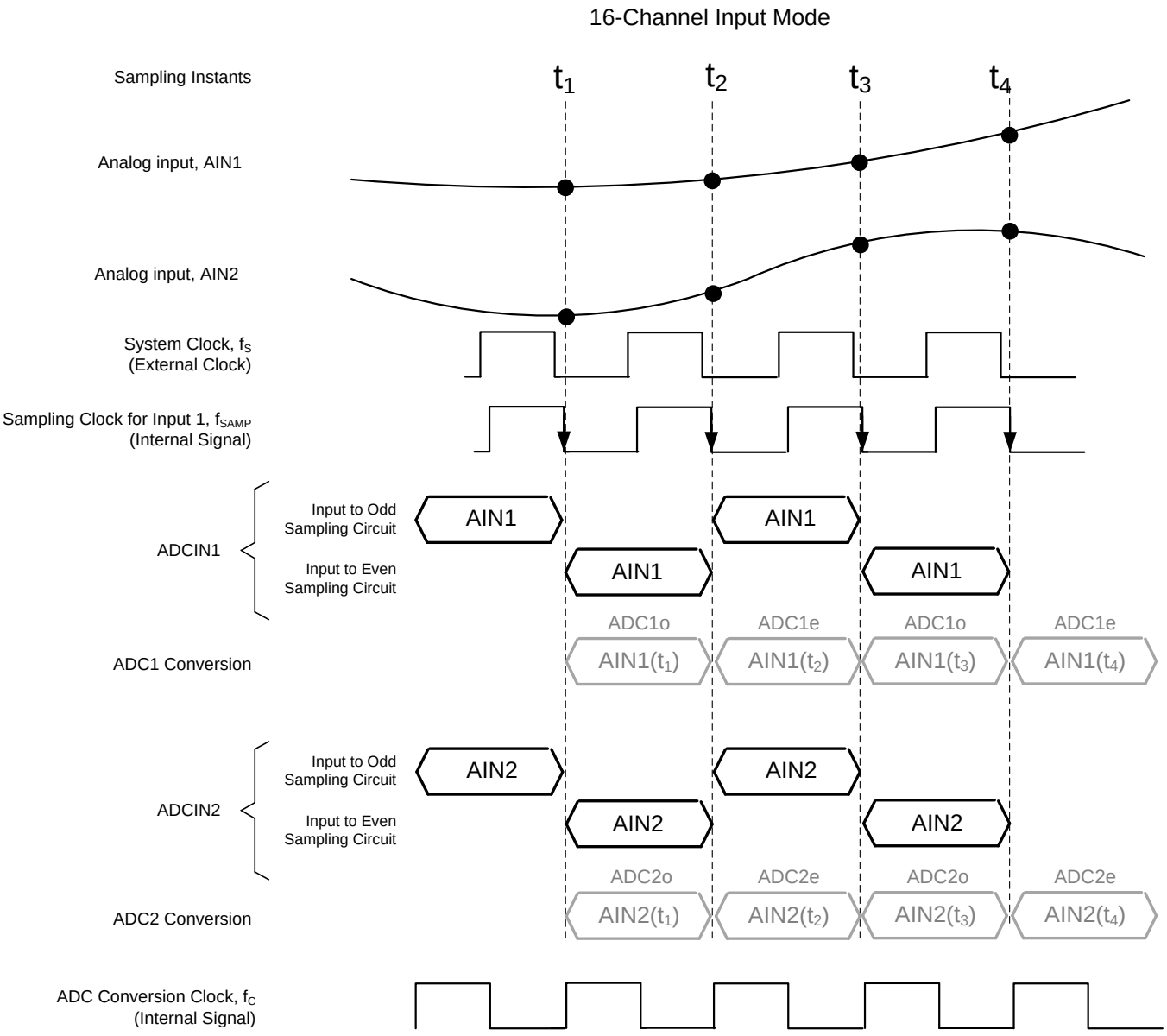


Figure 58. Input Sampling and Conversion Scheme (16-Input Mode)

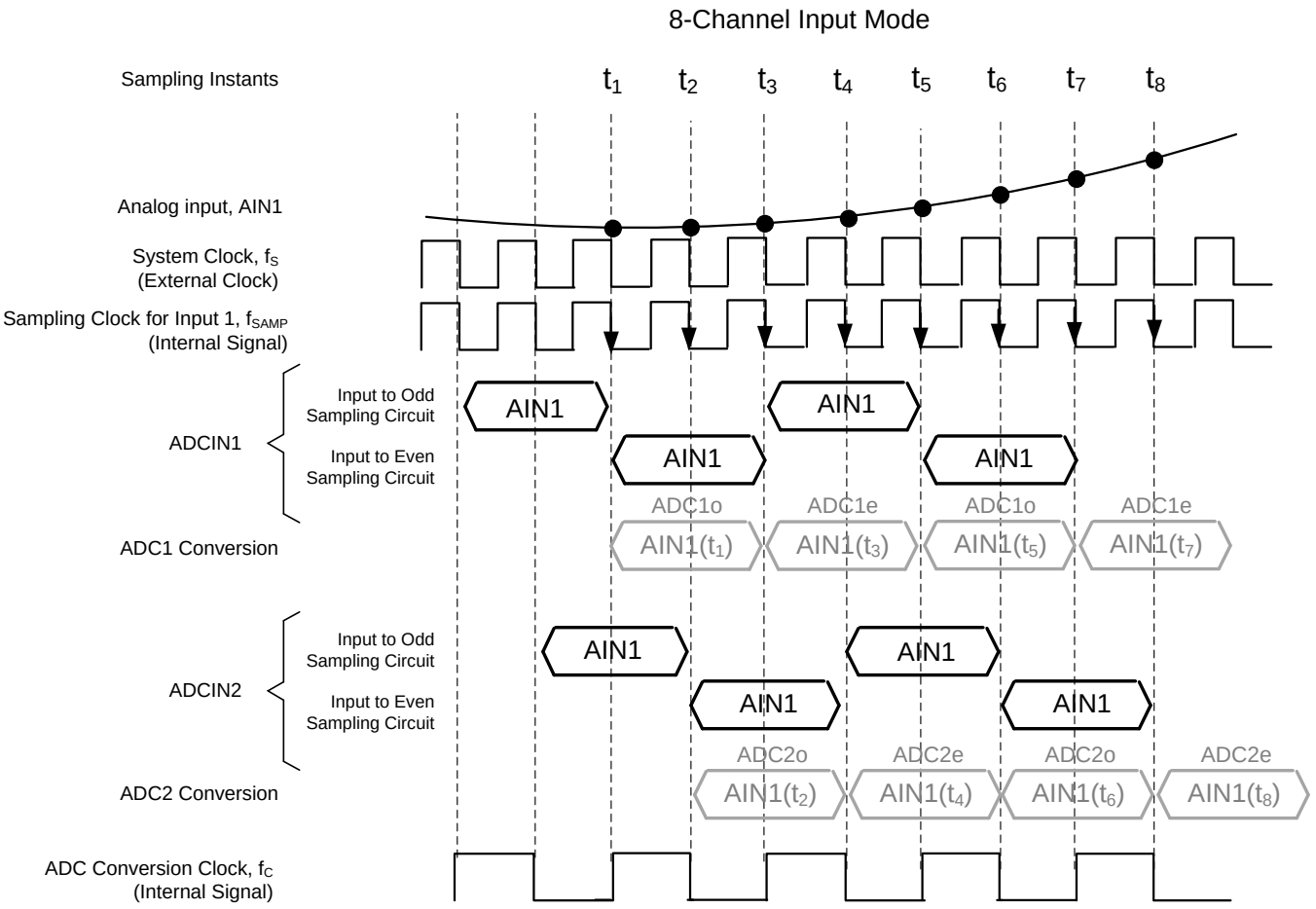


Figure 59. Input Sampling and Conversion Scheme (8-Input Mode)

Mapping the inputs of the odd and even sampling circuits of subsequent-numbered ADCs to subsequent-numbered sets of input pairs repeats in a similar manner.

The sampling rate (f_{SAMP}) can be defined as the rate at which the device converts each analog input presented to it. The relationship between the sampling rate and the system clock frequency is listed in Table 2 for the three input modes.

Table 2. Sampling Rate and Input Clock Frequency

ANALOG INPUT MODE (Number of Input Channels)	SAMPLING RATE (f_{SAMP})
16	f_S
32	0.5 × f_S
8	f_S

In 16-input mode, each ADC converts one input at a sampling rate equal to the system clock. In 32-input mode, one ADC alternately converts two sets of inputs, each at a sampling rate that is half the system clock. In the 8-input mode, two ADCs convert the same input in interleaved manner.

In 16-input mode, a ping-pong operation exists between two sampling circuits of one ADC that are sampling the same input. The mismatch between the two sampling circuit bandwidths can result in an interleaving spur at (f_S / 2 ± f_{IN}), where f_S is the frequency of the system clock and f_{IN} is the frequency of the input signal.

In 8-input mode, additional interleaving across two adjacent ADCs is present in addition to the ping-pong operation between the two sampling circuits of the same ADC. This increased mismatch can result in significant interleaving spurs at (f_S / 2 ± f_{IN}) and (f_S / 4 ± f_{IN}). The offset mismatch between the four sets of sampling circuits can result in a spur at f_S / 4.

For the 32-input mode, the sampling instants of the even-numbered input signals are offset from the sampling instants of the odd-numbered input signals by one system clock period. The magnitude of the interleaving spurs increases when the input frequency is increased because the sampling bandwidth mismatch across the different sampling circuits results in larger phase error mismatches when the input frequency is increased.

8.3.3 Analog-to-Digital Converter (ADC)

The device has 16 synchronous ADCs that provide a digital representation of the input in twos complement format. Each ADC converts at a rate of f_C using a conversion clock that is internally generated from the system clock. Every cycle of a conversion clock corresponds to a new ADC conversion.

The mapping of the ADC conversions to the analog input is described in Table 3. See Figure 57, Figure 58, and Figure 59 for the naming conventions.

Table 3. Mapping of the ADC Conversions to the Analog Inputs and Sampling Instants

ADC SAMPLE	INPUT CONVERTED BY THE ADC		
	16-INPUT MODE	32-INPUT MODE	8-INPUT MODE
ADC1o	AIN1 (t_1)	AIN1 (t_1)	AIN1 (t_1)
ADC2o	AIN2 (t_1)	AIN3 (t_1)	AIN1 (t_2)
ADC1e	AIN1 (t_2)	AIN2 (t_2)	AIN1 (t_3)
ADC2e	AIN2 (t_2)	AIN4 (t_2)	AIN1 (t_4)

The ADC resolution (the number of bits in the signals marked as ADCOUT1 to ADCOUT16) can be programmed as 10, 12, or 14 bits using the ADC_RES bits. The maximum conversion clock of the ADC depends on the ADC resolution setting, as shown in Table 4.

Table 4. Maximum Conversion Rate of the ADC for Different ADC Resolutions

ADC RESOLUTION (Bits)	MAXIMUM CONVERSION CLOCK ($f_{C(max)}$, MSPS)
10	100
12	80
14	65

The relationship between the system clock and sampling clock rates to the ADC conversion clock is shown in Table 5. Note that the maximum conversion rate of the ADC is fixed for the three resolution modes. In Table 5, *sampling rate* refers to the effective rate of sampling each active analog input.

Table 5. System Clock and Sampling Clock Relationship to the ADC Conversion Clock

ANALOG INPUT MODE (Number of Input Channels)	SYSTEM CLOCK RATE (f_S)	SAMPLING RATE (f_{SAMP})(1)	ADC RESOLUTIONS SUPPORTED
16	f_C	f_C	10, 12, 14
32	f_C	$0.5 \times f_C$	10, 12, 14
8	$2 \times f_C$	$2 \times f_C$	10

(1) Sampling rate is also the effective conversion rate of each input channel.

8.3.4 Device Synchronization Using TX_TRIG

The device has multiple PLLs and clock dividers that are used to generate the programmable ADC resolutions and LVDS synchronization factors as well as to synchronize LVDS test patterns.

The TX_TRIG input is used to synchronize clock dividers inside the device. The synchronization achieved using TX_TRIG also enables multiple parallel devices to operate synchronously.

For the 32-input mode, the same ADC alternates between converting two inputs. The TX_TRIG signal provides the mechanism to determine the sampling instants of the odd and even input signals with respect to the system clock, as shown in Figure 60.

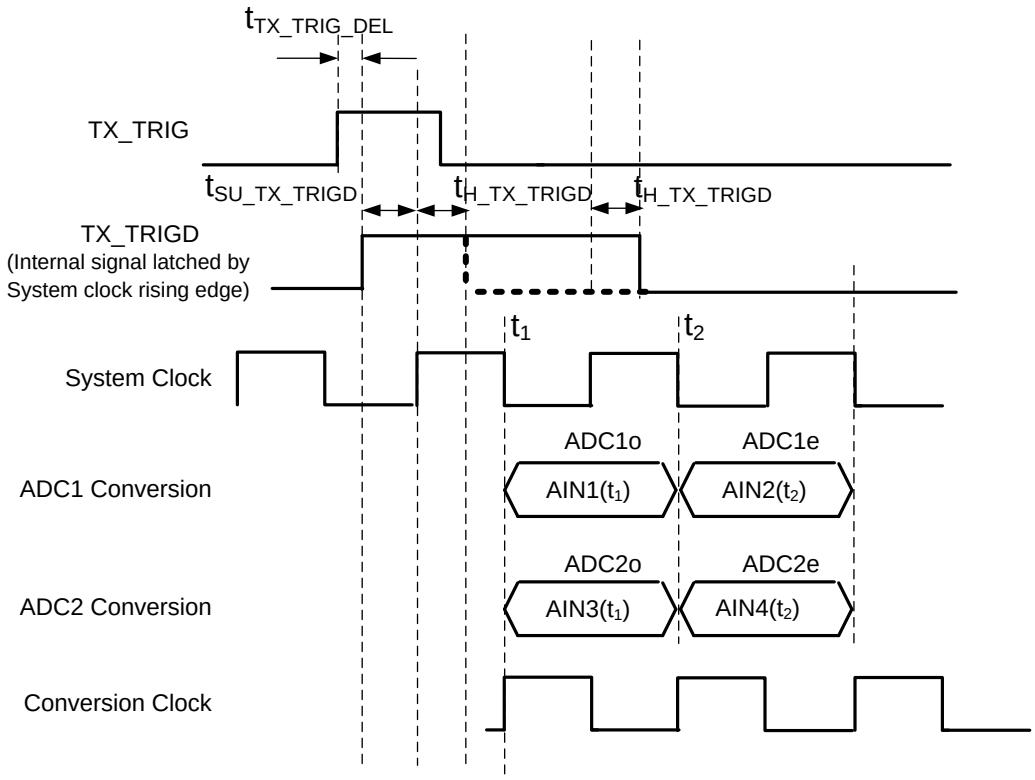


Figure 60. Odd- and Even-Channel Sampling Instant Definition Mechanism in 32-Input Mode with the TX_TRIG Signal

For the 8-input mode, the conversion clock is obtained by dividing the system clock by 2. The phase of the division is again determined by the TX_TRIG signal, as shown in Figure 61.

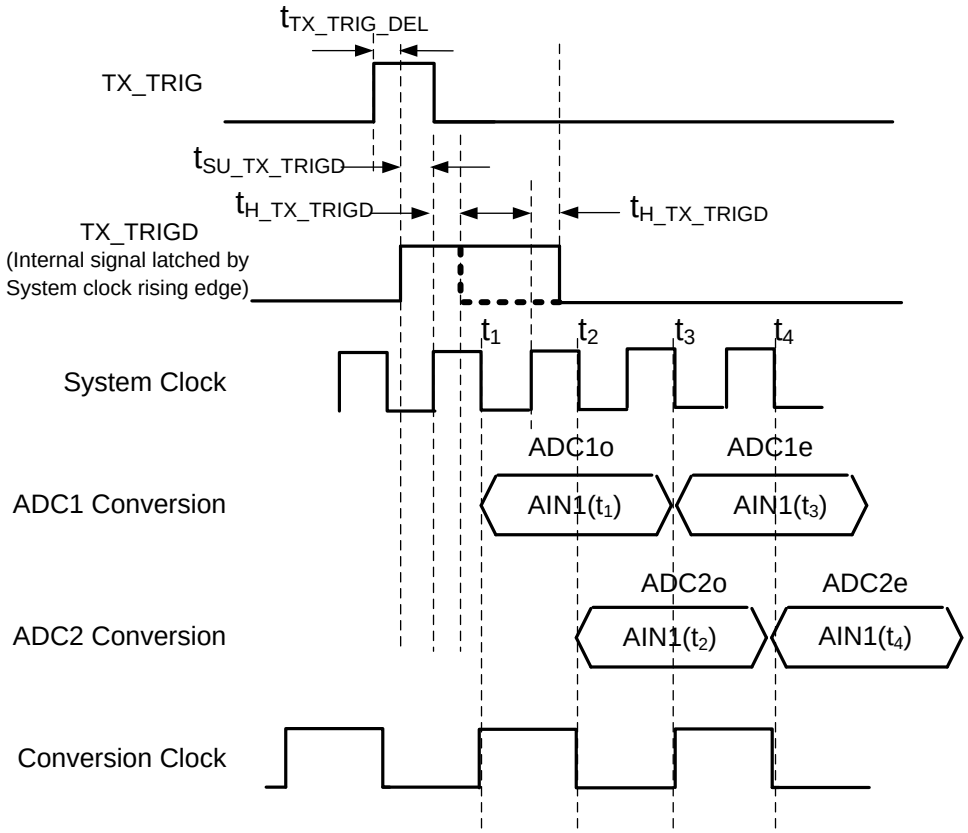


Figure 61. Conversion Clock Deriving Mechanism from Division of the Sampling Clock in 8-Input Mode

Applying a pulse on TX_TRIG is a mandatory part of the power-up and initialization sequence; see the *Power Sequencing and Initialization* section.

In case a TX_TRIG is not applied, the device can possibly behave in an unexpected manner. The identified cases are shown in Table 6.

Table 6. Device Behavior Cases: TX_TRIG is Not Applied

SCENARIO	ISSUE	INPUT MODE WHERE ISSUE OCCURS (8-, 16-, 32-Channel Input Modes)
Multiple devices operating in parallel	Frame clock across devices is not synchronized	8- and 32-channel input modes
	LVDS patterns across devices are not synchronized	8-, 16-, and 32-channel input modes
Serialization factor different from ADC resolution	Framing of data words within a frame clock is not defined	8- and 32-channel input modes

The TX_TRIG pulse resets the phase of the test pattern generator, the odd and even sampling phase selection, and the phase of the frame clock. As a result of this phase reset operation, the ADC data can be corrupted for four to six clocks immediately after applying TX_TRIG. The phase reset from TX_TRIG can be disabled using MASK_TX_TRIG.

8.3.5 Digital Processing

The ADC outputs go to a digital processing block that can be used to enhance ADC performance. Some of the operations done in the digital processing block can enhance the effective signal to noise ratio at its output. For this reason, the number of bits at the DIGOUT1 to DIGOUT16 signals are considered to be 16. However, some of the LSBs of this 16-bit word may be zero. For example, when the digital processing block is bypassed, the number of non-zero bits in DIGOUT is the same as the ADC resolution—the extra LSBs of the 16-bit word are zero.

The digital processing block results in additional latency that can be avoided by using the low latency mode (programmed using the LOW_LATENCY_EN bit) that bypasses the entire digital processing block without introducing extra latency. The various features available in the digital processing block are shown in Figure 62 and are explained in the subsequent sections.

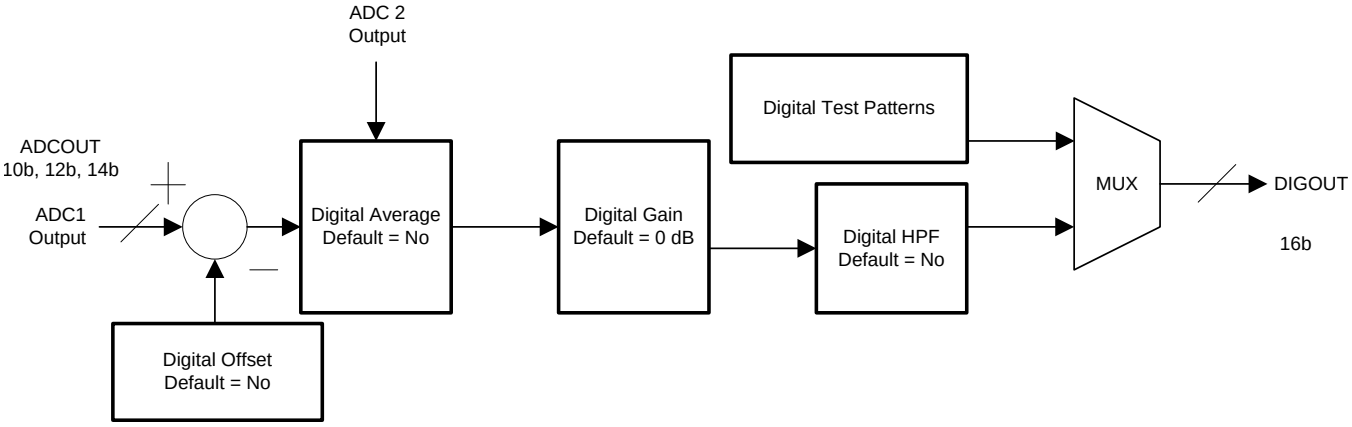


Figure 62. ADC Digital Block Diagram

8.3.5.1 Digital Offset

Digital functionality provides for channel offset correction. Setting the DIG_OFFSET_EN bit to 1 enables the subtraction of the offset value from the ADC output. There are two offset correction modes, as shown in Figure 63.

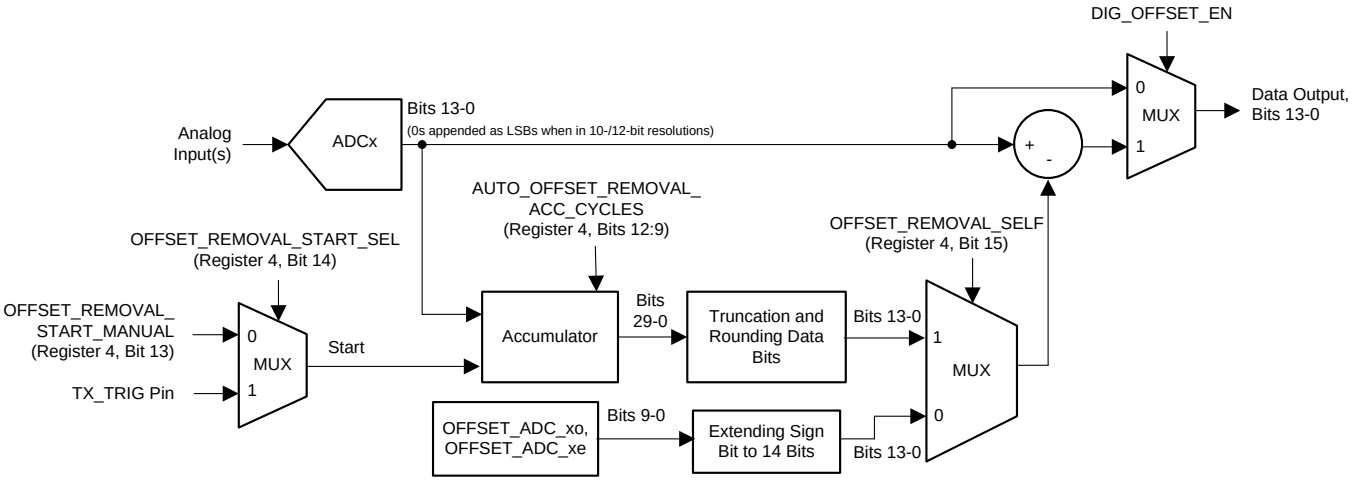


Figure 63. Digital Offset Correction Block Diagram

8.3.5.1.1 Manual Offset Correction

If the channel offset is known or estimated, it can be written into a 10-bit register and can be subtracted from the ADC output. There are 32 sets of manual offset controls. To enable per-channel offset correction in the 32-input mode, the offset values for the odd and even data streams of each of the 16 ADCs can be independently controlled. The registers OFFSET_ADCxo and OFFSET_ADCxe correspond to the offsets subtracted from the odd and even data streams of ADCx. Write the offset values in twos complement format.

8.3.5.1.2 Auto Offset Correction Mode (Offset Correction using a Built-In Offset Calculation Function)

The auto offset calculation module can be used to calculate the channel offset that is then subtracted from the ADC output. To enable the auto offset correction mode, set the OFFSET_REMOVAL_SELF bit and DIG_OFFSET_EN bit to 1.

In auto offset correction mode the dc component of the ADC output (assumed to be the channel offset) is estimated using a digital accumulator. The ADC output sample set used by the accumulator is determined by a start time or first sample and number of samples to be used. A high pulse on the TX_TRIG pin or setting the OFFSET_REMOVAL_START_MANUAL register can be used to determine the first sample to the accumulator. To set the number of samples, the AUTO_OFFSET_REMOVAL_ACC_CYCLES register must be programmed according to Table 7.

If a pulse on the TX_TRIG pin is used to set the first sample, additional flexibility in setting the first sample is provided. A programmable delay between the TX_TRIG pulse and the first sample can be set by writing to the OFFSET_CORR_DELAY_FROM_TX_TRIG register.

The determined offset value can be read out for each channel. Set the channel number in the AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL register and read the offset value for the corresponding channel in the AUTO_OFFSET_REMOVAL_VAL_RD register. Note that the offset estimation is done separately for the odd and even data streams of each of the 16 ADCs and results in 32 sets of offset estimates that can be read out.

Table 7. Auto Offset Removal Accumulator Cycles

AUTO_OFFSET_REMOVAL_ACC_CYCLES (Bits 3-0)	NUMBER OF SAMPLES USED FOR OFFSET VALUE EVALUATION
0	2047
1	127
2	255
3	511
4	1023
5	2045
6	4095
7	8191
8	16383
9	32767
10 to 15	65535

8.3.5.1.3 Digital Averaging

The data from two adjacent ADCs (ADC1 and ADC2, ADC3 and ADC4, and so forth) can be averaged by enabling the AVG_EN bit. A scenario where this feature can be useful is where the same analog input is fed to two channels and their outputs are averaged to achieve approximately a 3-dB improvement in SNR. The mapping of DIGOUT to the ADC data is shown in Table 8.

Table 8. Mapping of the DIGOUT Words to the ADC Outputs when Using Digital Averaging

DIGOUT	RELATIONSHIP TO ADC DATA	LVDS PAIR THE DATA COME OUT ON	
		1X DATA RATE MODE	2X DATA RATE MODE
DIGOUT1	Average of ADC1 and ADC2	DOUT1	DOUT1
DIGOUT2	Average of ADC3 and ADC4	DOUT2	
DIGOUT3	Average of ADC5 and ADC6	DOUT3	DOUT2
DIGOUT4	Average of ADC7 and ADC8	DOUT4	
DIGOUT5	Ignore	—	—
DIGOUT6	Ignore	—	—
DIGOUT7	Ignore	—	—
DIGOUT8	Ignore	—	—
DIGOUT9	Average of ADC9 and ADC10	DOUT9	DOUT9
DIGOUT10	Average of ADC11 and ADC12	DOUT10	
DIGOUT11	Average of ADC13 and ADC14	DOUT11	DOUT10
DIGOUT12	Average of ADC15 and ADC16	DOUT12	
DIGOUT13	Ignore	—	—
DIGOUT14	Ignore	—	—
DIGOUT15	Ignore	—	—
DIGOUT16	Ignore	—	—

8.3.5.1.4 Digital Gain

The digital gain block can be enabled using the DIG_GAIN_EN bit. When enabled, a digital gain programmable from 0 dB to 6 dB in steps of 0.2 dB can be applied. To enable individual digital gain control for each input in 32-input mode, a separate digital gain control is provided for the odd and even sample of each ADC. Therefore, there are 32 gain controls. When using 16-input mode, set the odd and even gain controls of the same ADC to the same value. When using 8-input mode, four sets of gain controls are to be set to the same value (the odd and even gains of adjacent ADCs; for instance, ADC1 and ADC2).

8.3.5.1.5 Digital HPF

A digital high-pass filter (HPF) can be enabled in the path of each ADC word. The enable control is shared between sets of four consecutive-numbered ADCs (ADC1-ADC4, ADC5-ADC8, ADC9-ADC12, and ADC13-ADC16). For example, DIG_HPF_EN_ADC1-4 enables the HPF in the paths of ADCOUT1, ADCOUT2, ADCOUT3, and ADCOUT4. The digital high-pass transfer function is determined by Equation 1:

$$Y(n) = \frac{2^k}{2^k + 1} [x(n) - x(n-1) + y(n-1)] \quad (1)$$

When DIG_HPF_EN_ADC1-4 is set, the value of K in Equation 1 is set by the HPF_CORNER_ADC1-4 bits. The value of K can be programmed from 2 to 10. Table 9 shows the cutoff frequency as a function of K.

Table 9. Digital HPF, –1-dB Corner Frequency versus K and f_S

CORNER FREQUENCY (k) (HPF_CORNER_ADCx Register)	CORNER FREQUENCY (kHz)		
	f_S = 40 MSPS	f_S = 50 MSPS	f_S = 65 MSPS
2	2780	3480	4520
3	1490	1860	2420
4	738	230	1200
5	369	461	600
6	185	230	300
7	111	138	180
8	49	61	80
9	25	30	40
10	12.	15	20

By default the HPF output is truncated to 14 bits. To enable the rounding operation to map the HPF output to the ADC resolution, set the HPF_ROUND_EN_CH1-8 and HPF_ROUND_EN_CH9-16 bits to 1.

8.3.6 Data Formatting

The data formatting block does two functions: truncation and test pattern insertion. The serialization block following the data formatting block performs a parallel-to-serial conversion of the input word. The serialization factor is programmable to 10, 12, 14, or 16. The truncation block truncates the DIGOUT signal to the number of bits specified by the serialization factor. The number of bits in DIGRES1 to DIGRES16 is therefore determined by the serialization factor. Again, some of the bits in DIGRES may always be zero, depending on the combination of ADC resolution, what digital features are enabled or disabled, and the serialization factor that is programmed. To aid the FPGA in capturing and deserializing the serial output, the device includes provisions to replace the ADC data with test patterns. The SERIAL_IN1 to SERIAL_IN16 signals are the same as the DIGRES1 to DIGRES16 signals during normal operation. When a test pattern is programmed, the DIGRES signals are replaced with the appropriate test pattern. The manner in which a given test pattern actually comes out of the LVDS lines can be altered based on the serializer operating mode because the serializer itself has multiple modes (LSB-, MSB-first modes and 1X, 2X data rate modes).

8.3.7 Serializer and LVDS Interface

By default, each serializer takes in one SERIAL_IN word and performs a parallel-to-serial conversion. This mode is referred to as the *1X data rate mode*. In the 1X data rate mode, all 16 LVDS pairs are active and each pair corresponds to the data coming out of one ADC. In the 2X data rate mode (set using the LVDS_RATE_2X bit), the data from a pair of ADCs (two SERIAL_IN words) is packed into the same serial stream. In 2X mode, half the LVDS pairs are idle and can be powered down. The 2X data rate mode causes the LVDS interface to run at twice the rate but results in power saving. See the *Timing Requirements: Signal Chain* table for speed restrictions when using the 1X and 2X data rate modes.

The LVDS interface is a clock-data-frame (CDF) format, and has a frame clock and a high-speed bit clock in addition to the serial data lines.

The frequency of the bit clock with respect to the conversion clock frequency depends on the serialization factor (set using the SER_DATA_RATE bits), as shown in Table 10. Note that the serialized data are meant to be captured on both the rising and falling edges of the bit clock. Thus, the serialized data rate is twice the bit clock frequency.

Table 10. Bit Clock Rate Relationship to the Conversion Clock and System Clock Rates

SERIALIZATION FACTOR	DATA RATE MODE	BIT CLOCK RATE (f_B in Terms of f_C)	BIT CLOCK RATE (f_B in Terms of f_S)		
			16-INPUT MODE	32-INPUT MODE	8-INPUT MODE
10	1X	$5 \times f_C$	$5 \times f_S$	$5 \times f_S$	$2.5 \times f_S$
	2X	$10 \times f_C$	$10 \times f_S$	$10 \times f_S$	$5 \times f_S$
12	1X	$6 \times f_C$	$6 \times f_S$	$6 \times f_S$	$3 \times f_S$
	2X	$12 \times f_C$	$12 \times f_S$	$12 \times f_S$	$6 \times f_S$
14	1X	$7 \times f_C$	$7 \times f_S$	$7 \times f_S$	$3.5 \times f_S$
	2X	$14 \times f_C$	$14 \times f_S$	$14 \times f_S$	$7 \times f_S$
16	1X	$8 \times f_C$	$8 \times f_S$	$8 \times f_S$	$4 \times f_S$
	2X	$16 \times f_C$	$16 \times f_S$	$16 \times f_S$	$8 \times f_S$

The relationship of the frame clock frequency to the conversion clock frequency for the three input modes is as shown in Table 11. The relationship of the frame clock frequency to the system clock (and conversion clock) frequencies is the same between the 1X and 2X data rate modes.

Table 11. Relation of Frame Clock Rate to the Conversion Clock and System Clock Rates

ANALOG INPUT MODE (Number of Channels)	FRAME CLOCK RATE (f_F in Terms of f_C)	FRAME CLOCK RATE (f_F in Terms of f_S)	DATA RATE MODES SUPPORTED
16	f_C	f_S	1X, 2X
32	$0.5 \times f_C$	$0.5 \times f_S$	1X
8	f_C	$0.5 \times f_S$	1X, 2X

The serialization schemes for the various modes are illustrated in Figure 64 to Figure 68. Note that although the signals marked *ADCx Conversion* in Figure 64 to Figure 68 represent a multi-bit digital word, the SERIAL_OUTx signals are actually serialized representations of the correspondingly colored signals. For example, the blue-colored section in the SERIAL_OUT1 signal in Figure 64 contains the serial stream of data that originated from the word corresponding to ADC1o.

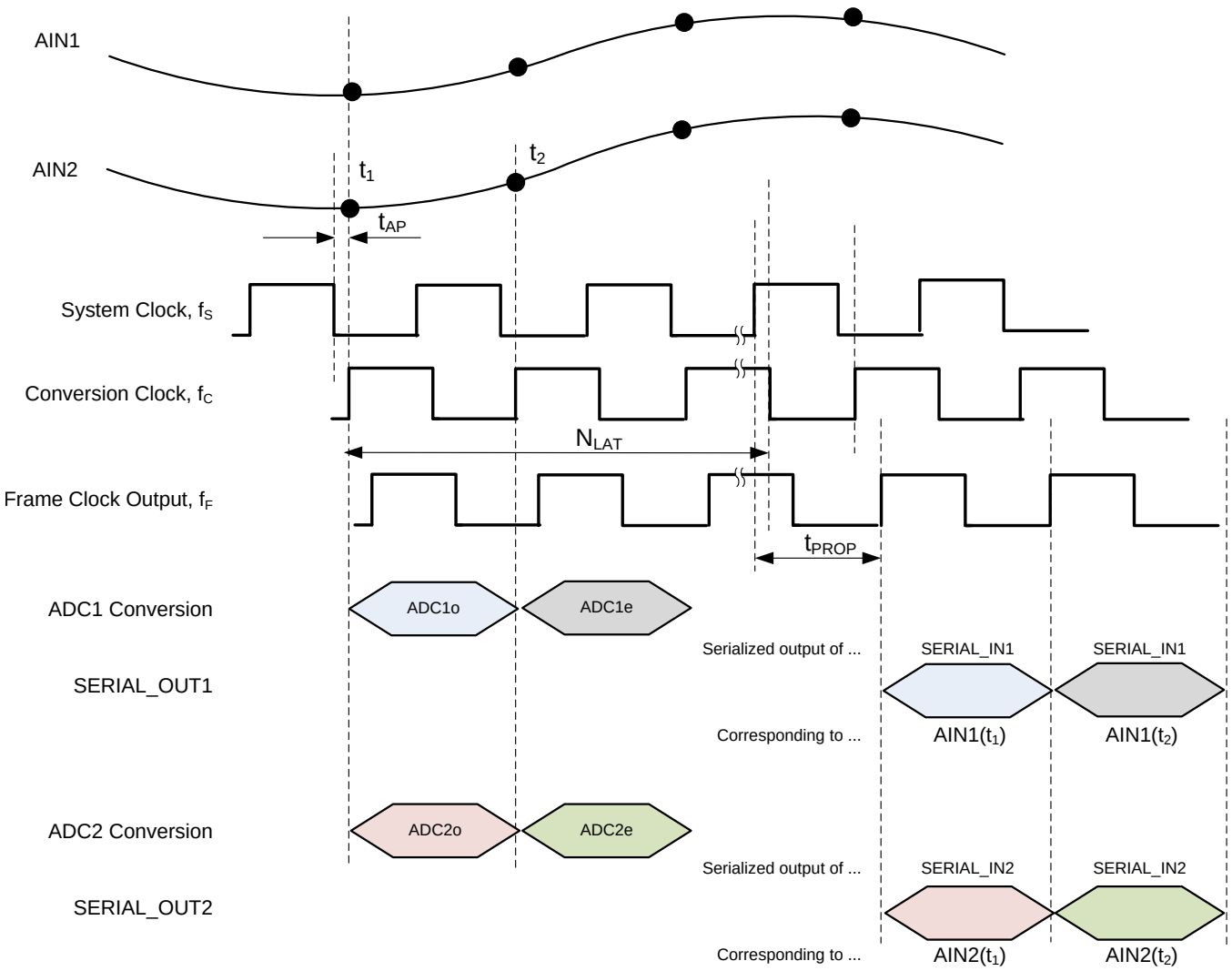


Figure 64. ADC to Output Mapping in 16-Input, 1X Mode in LVDS Interface Mode

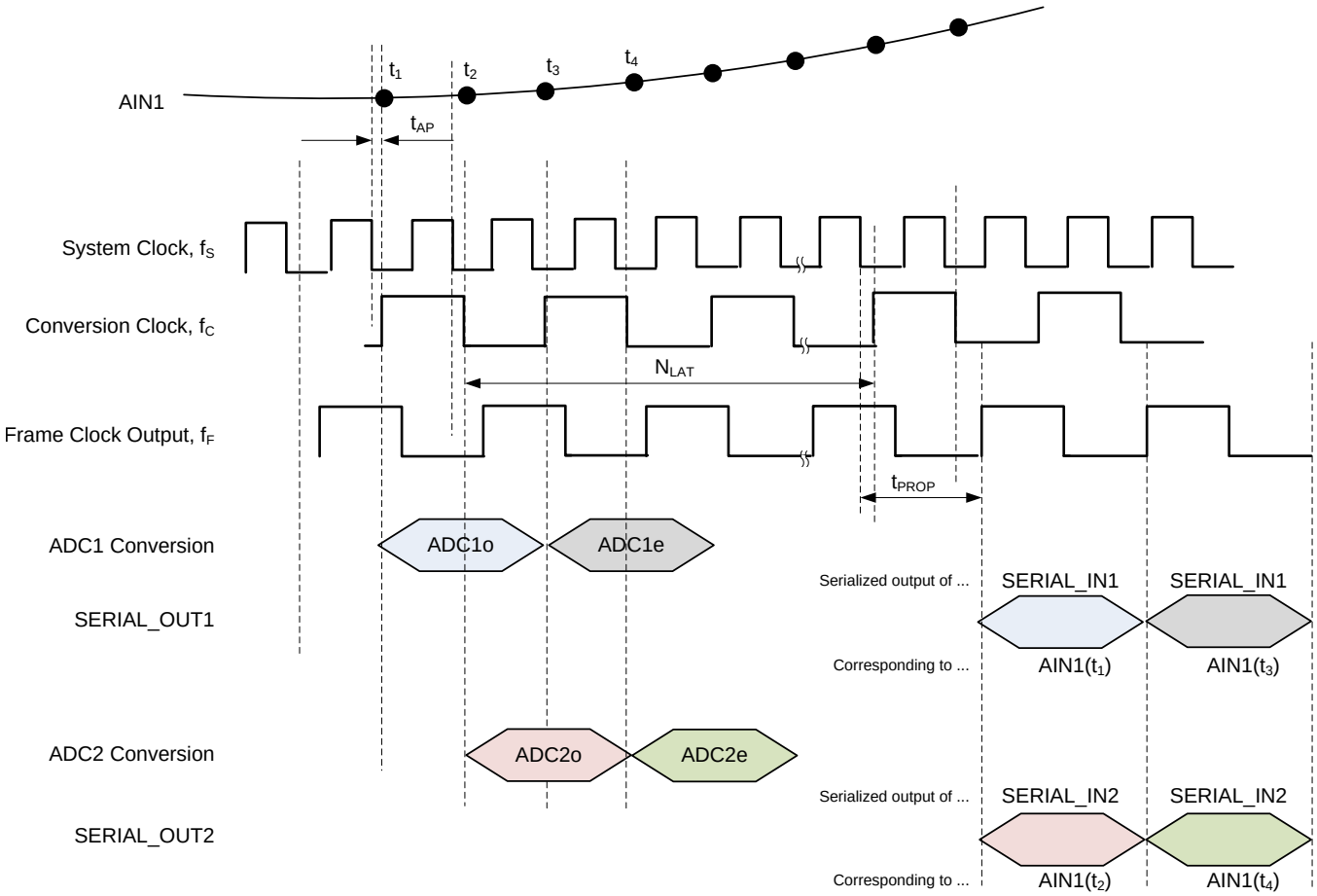


Figure 65. ADC to Output Mapping in 8-Input, 1X Mode in LVDS Interface Mode

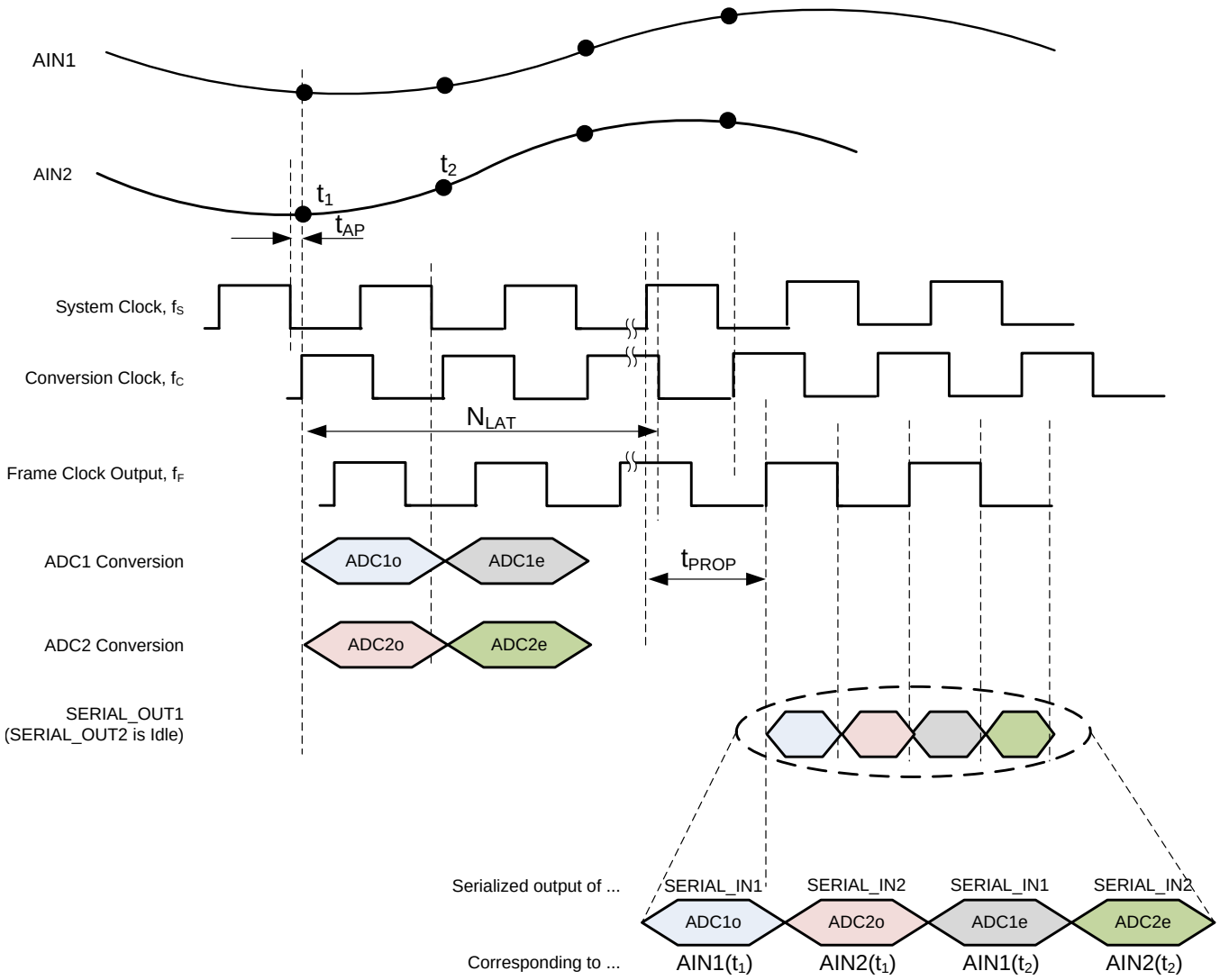


Figure 66. ADC to Output Mapping in 16-Input, 2X Mode in LVDS Interface Mode

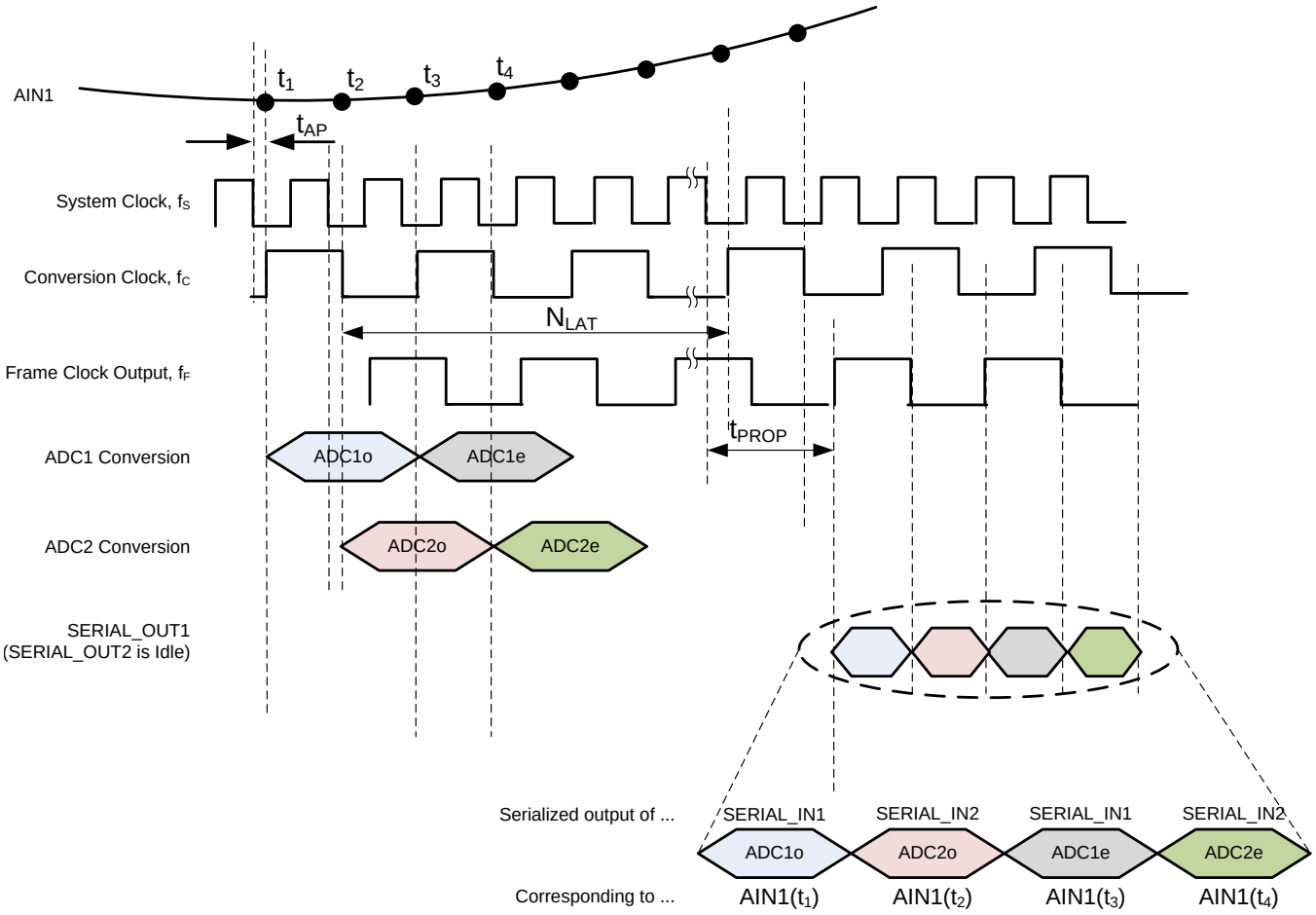


Figure 67. ADC to Output Mapping in 8-Input, 2X Mode in LVDS Interface Mode

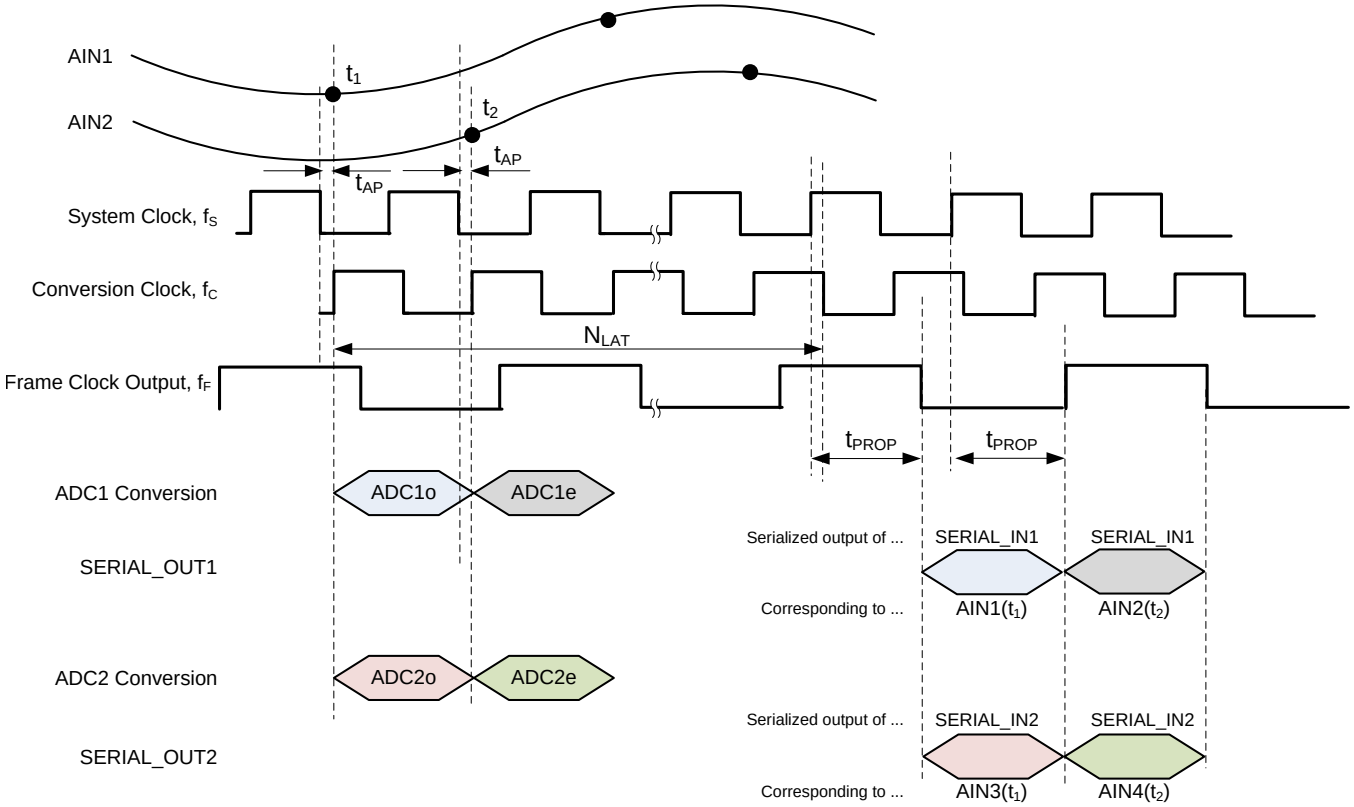


Figure 68. ADC to Output Mapping in 32-Input, 1X Mode in LVDS Interface Mode

The mapping of the subsequent-numbered ADC signals to subsequent-numbered SERIAL_OUT signals follows the same pattern as indicated previously.

The serialized stream in SERIAL_OUT is a serialized representation of SERIAL_IN, which is the input word coming into the serializer. By default, serialization is done LSB-first. By setting the MSB_FIRST bit, serialization can be set to MSB-first.

The alignment of the frame clock, bit clock, and the serialized output data is illustrated in Figure 1 for 16-input mode where the serialization factor is set to 12 bit, serialization is LSB-first, and the data rate is set to 1X mode.

Another case is shown in Figure 69 for 16-input mode. Here, the serialization factor is set to 14 bit, serialization is MSB-first, and the data rate is set to 2X mode.

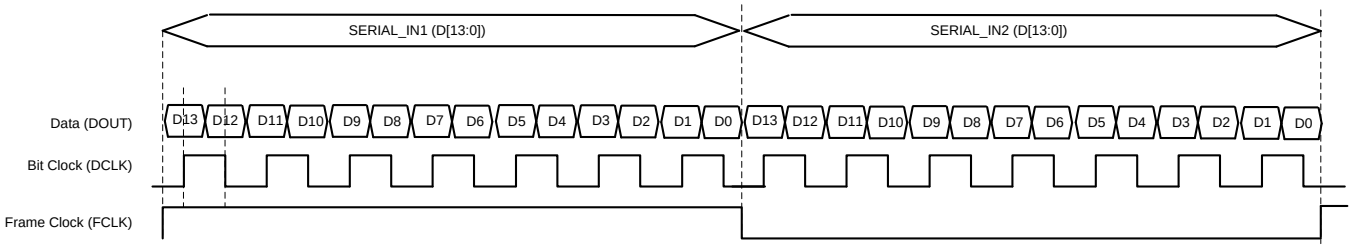


Figure 69. LVDS Output Signals Timing Diagram in 16-Input Mode with 14-Bit Serialization, MSB-First, 2X Data Rate Mode

The serialized signals come out on the DOUT pins as indicated in Table 12. The buffers marked *Idle* can be powered down using the appropriate register bits to save power.

Table 12. Mapping of the Serialized Outputs to the DOUT Pins

LVDS OUTPUT PIN (DOUT)	OUTPUT SIGNAL	
	1X DATA RATE MODE	2X DATA RATE MODE
DOUT1	SERIAL_OUT1	SERIAL_OUT1
DOUT2	SERIAL_OUT2	SERIAL_OUT3
DOUT3	SERIAL_OUT3	SERIAL_OUT5
DOUT4	SERIAL_OUT4	SERIAL_OUT7
DOUT5	SERIAL_OUT5	Idle
DOUT6	SERIAL_OUT6	Idle
DOUT7	SERIAL_OUT7	Idle
DOUT8	SERIAL_OUT8	Idle
DOUT9	SERIAL_OUT9	SERIAL_OUT9
DOUT10	SERIAL_OUT10	SERIAL_OUT11
DOUT11	SERIAL_OUT11	SERIAL_OUT13
DOUT12	SERIAL_OUT12	SERIAL_OUT15
DOUT13	SERIAL_OUT13	Idle
DOUT14	SERIAL_OUT14	Idle
DOUT15	SERIAL_OUT15	Idle
DOUT16	SERIAL_OUT16	Idle

8.3.8 LVDS Buffers

A graphical representation of the 18 LVDS output buffers is shown in Figure 70.

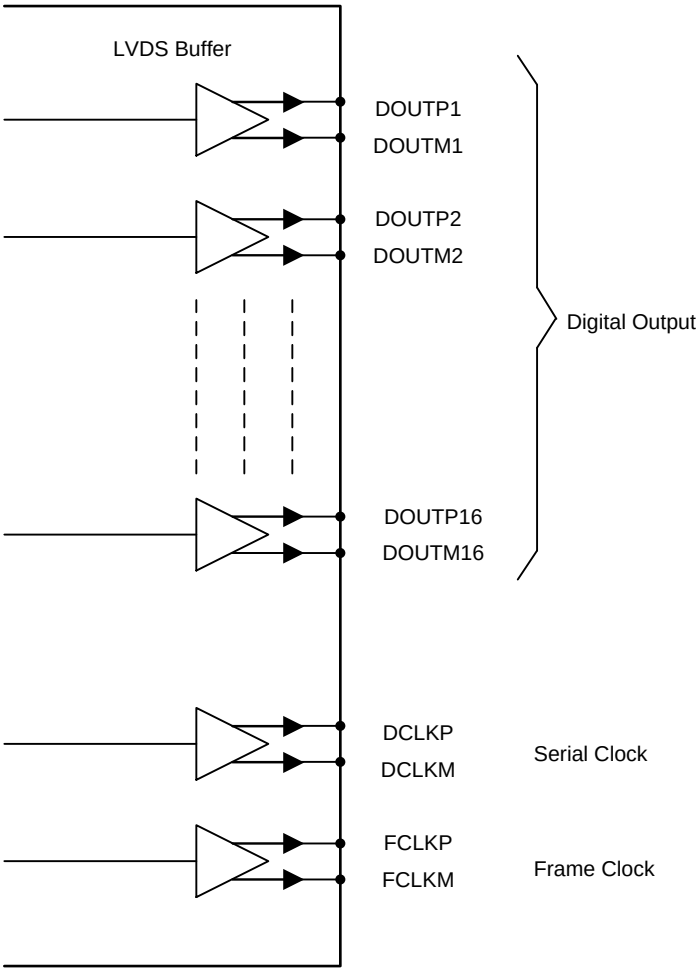
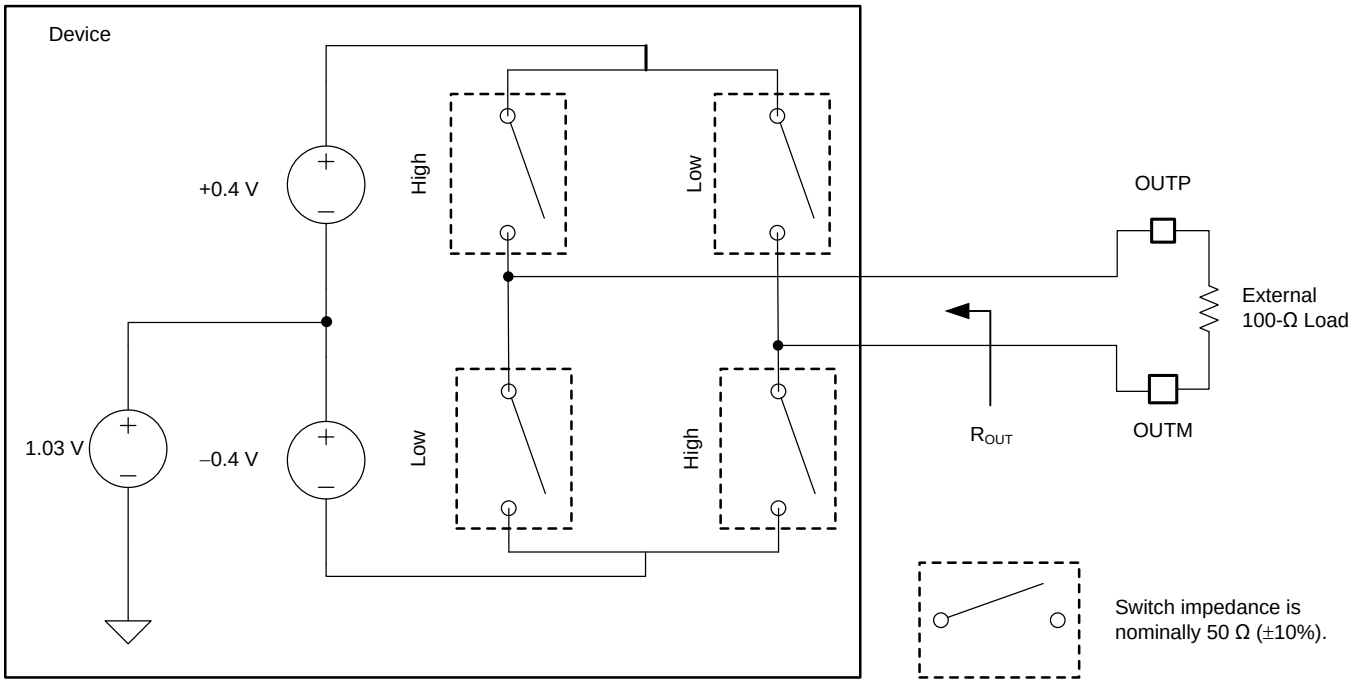


Figure 70. LVDS Output

The equivalent circuit of each LVDS output buffer is shown in Figure 71. The buffer is designed for a differential output impedance of 100 Ω (R_{OUT}). The differential outputs can be terminated at the receiver end by a 100-Ω termination. The buffer output impedance functions like a source-side series termination. By absorbing reflections from the receiver end, the buffer output impedance helps improve signal integrity.



NOTE: When either the high or low switches are closed, differential R_{OUT} = 100 Ω.

Figure 71. LVDS Output Circuit

8.3.9 JESD204B Interface

8.3.9.1 Overview

When operating in 16-input and 32-input modes, the device supports a multi-lane output interface based on the JEDEC standard: JESD204B (serial interface for data converters). This interface runs up to 5 Gbps and provides a compact way of routing the data from multiple ADCs in the device to the FPGA. Subclasses 0, 1, and 2 of the JESD204B interface are supported. The block diagram in Figure 72 illustrates the connections of the JESD interface to the rest of the device. After the test pattern insertion block, the parallel data streams SERIAL_IN1 to SERIAL_IN16 can be routed to either the LVDS interface or to the JESD interface (or both). The ADC data can be sent out using the EN_JESD and DIS_LVDS controls. The LVDS_INx and CML_INx words are the same as the SERIAL_INx words.

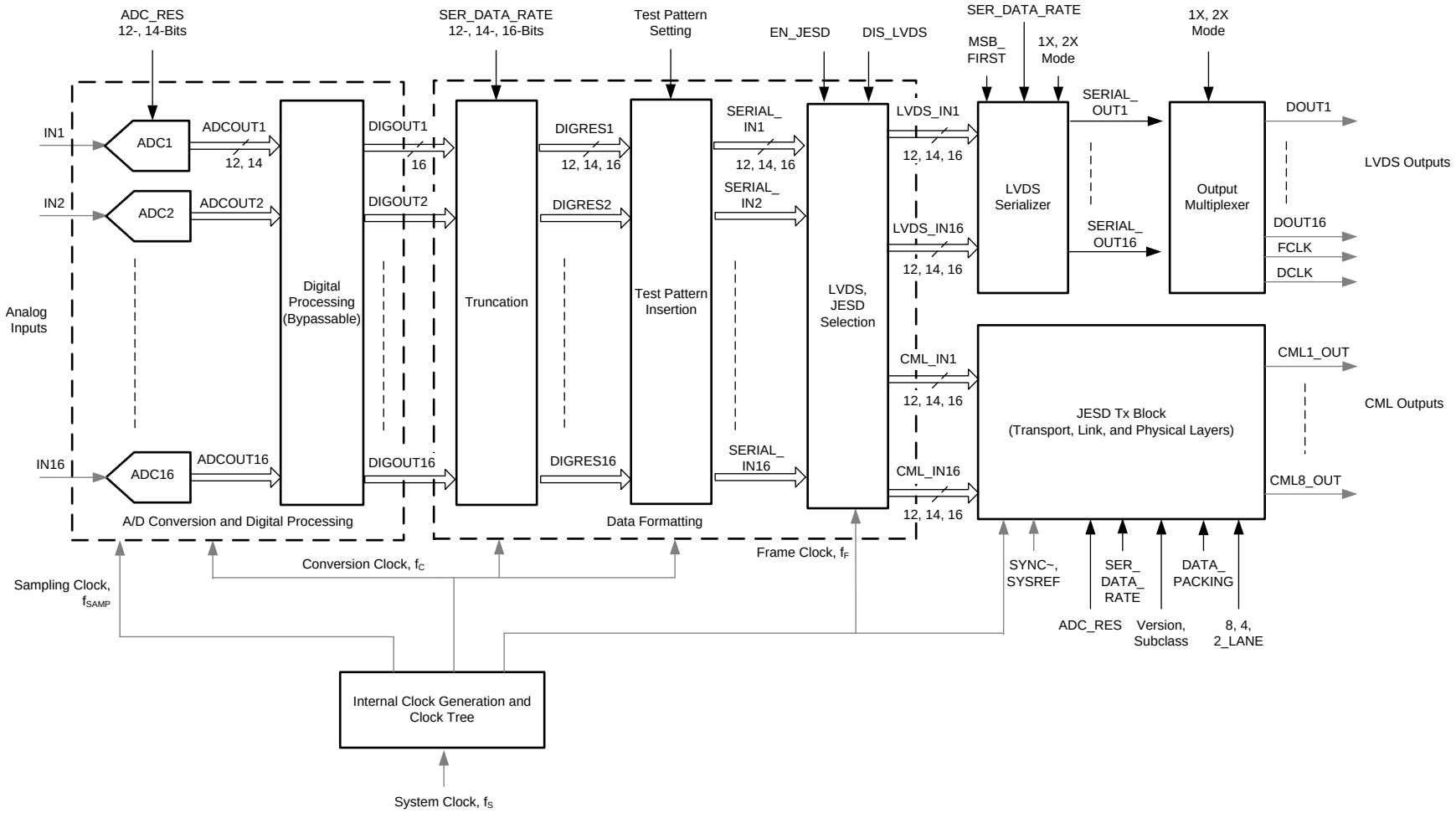


Figure 72. JESD Interface Connection to the Digital Processing Output

The JESD interface can be enabled by setting the EN_JESD bit to 1. When in JESD mode, the LVDS interface can be disabled by setting the DIS_LVDS bit to 1. Both the LVDS and JESD interfaces can be simultaneously kept active by setting the DIS_LVDS bit to 0 and the EN_JESD bit to 1.

Table 13 shows the clock rates corresponding to the various clocks mentioned in the JESD204B document. This mapping is independent of whether the device operates in 8-, 16-, or 32-input mode.

Table 13. Mapping of JESD204B Clock Notation to the Clock Rates

CLOCK NOTATION IN JESD204B DOCUMENT	CORRESPONDING CLOCK RATE
Device clock	f_S
Frame clock	f_C
Conversion clock	f_C
Sample clock	f_C

All mandatory features of the JESD204B interface are supported by the device, and are:

- Breaking up of data from the ADCs into octets.
- Optional scrambling of octets to avoid spectral tones.
- Conversion of (scrambled) octets to 10-bit words using 8b, 10b encoding.
- Parallel-to-serial conversion of octets.
- A code group synchronization (CGS) phase to enable the receiver to synchronize to the frame boundaries.
- An initial lane alignment (ILA) sequence phase to help the receiver align the data from all lanes and also for the receiver to read and verify the link configuration parameters.
- Character replacement at frame and multi-frame boundaries during normal data transmission to enable the receiver to monitor frame alignment.
- Mechanism to achieve deterministic latency across the link using the SYSREF signal in subclass 1 and the SYNC~ signal in subclass 2.

The *Link Configuration* section details only the device-specific implementation aspects of the JESD204B interface. For additional details related to the standard, see the JEDEC standard 204B (July 2011).

8.3.9.2 Link Configuration

The JESD204B link in the device can be configured to operate in different modes using the register controls in Table 14.

Table 14. Register Controls Determining Link Configuration Parameters

REGISTER CONTROL	DESCRIPTION	ALLOWED SETTINGS
NUM_ADC_PER_LANE	Number of ADC words packed into one lane	2, 4, 8
ADC_RES	Number of bits resolution in the ADC word input to the JESD transmitter block	10, 12, 14, 16
SER_DATA_RATE	Serialization factor control	10, 12, 14, 16

In addition to the register controls mentioned in Table 14, the SING_CONV_PER_OCT register bit controls the packaging efficiency of the ADC data into octets.

The link configuration parameters are determined by Table 15.

Table 15. Link Configuration Parameters

LINK CONFIGURATION PARAMETER					LINK CONFIGURATION FIELD	
LINK CONFIGURATION PARAMETER	DESCRIPTION	ALLOWED VALUES (Decimal)	DEFAULT VALUE (In Decimal, Unless Otherwise Specified)(1)	METHOD OF SETTING	CORRESPONDING FIELD IN ILAS	RELATION OF FIELD TO PARAMETER
ADJCNT	Not relevant	0	0	Forced to 0; not used	ADJCNT[3:0]	Binary value
ADJDIR	Not relevant	0	0	Forced to 0; not used	ADJDIR[0]	Binary value
BID	Bank ID	0…15	0	BANK_ID register control	BID[3:0]	Binary value
CF	Number of control words per frame	0	0	Forced to 0	CF[4:0]	Binary value
CS	Number of control bits per sample	0	0	Forced to 0	CS[1:0]	Binary value
DID	Device ID	0…255	0	DEVICE_ID register control	DID[7:0]	Binary value
F	Number of octets per frame	See Table 18	6	Determined by Table 18	F[7:0]	Binary value minus 1
HD	High density format	0	0	Forced to 0; not used	HD[0]	Binary value
JESDV	JESD204 version	0 = JESD204A 1 = JESD204B	1	ENABLE_JESD_VER_CONTROL, JESD_VERSION register control; see Table 16	JESDV[2:0]	Binary value
K	Number of frames per multiframe	See Table 16	3	Determined by Table 29; can be changed using FORCE_K and K_VALUE_TO_FORCE register controls	K[4:0]	Binary value minus 1
L	Number of lanes	2, 4, 8	4	Determined by Table 18	L[4:0]	Binary value minus 1
LID	Lane ID	1 to 8	As given in Table 5	Default (value given in Table 17) can be changed using EN_LANE_ID# and LANE_ID# register controls for each lane number	LID[4:0]	Binary value
M	Number of ADCs	16	16	Forced to 16	M[7:0]	Binary value minus 1
N	ADC resolution	10, 12, 14, 16	12	Determined by ADC_RES register control	N[4:0]	Binary value minus 1
N’	Total number of bits per sample	See Table 18	12	Determined by Table 18	N’[4:0]	Binary value minus 1
PHADJ	Not relevant	0	0	Forced to 0; not used	PHADJ[0]	Binary value
S	Number of samples per ADC per frame	1	1	Forced to 1	S[4:0]	Binary value minus 1
SCR	Scrambler enable or disable	0,1	0	SCR_EN register control	SCR[0]	Binary value
SUBCLASSV	Device subclass version	0 = Subclass 0 1 = Subclass 1 2 = Subclass 2	1	ENABLE_JESD_VER_CONTROL, JESD_SUBCLASS register control; see Table 16	SUBCLASSV[2:0]	Binary value
RES1	Reserved field 1	0	0	Forced to 0	RES1[7:0]	Binary value
RES2	Reserved field 2	0	0	Forced to 0	RES2[7:0]	Binary value
CHKSUM	Checksum	—	Lane 1 – 32h Lane 3 – 34h Lane 5 – 36h Lane 7 – 38h	Default value as calculated by device can be changed using EN_CHECKSUM_LANE# and CHECK_SUM# for each lane number	FCHK[7:0]	Binary value

(1) Corresponding to ADC_RES set to 12 bits, SER_DATA_RATE set to 12 bits, NUM_ADC_PER_LANE set to four ADCs per lane, SING_CONV_PER_OCT mode disabled, and ENABLE_JESD_VER_CONTROL set to 0 (to operate in JESD204B-subclass1).

8.3.9.3 JESD Version and Subclass

The interface can be configured to operate either as a JESD204A version or as a JESD204B version. Furthermore, when operating as a JESD204B version, the subclass can be configured as subclass 0, 1, or 2. The register controls for programming the version and subclass are shown in Table 16.

Table 16. JESD Version and Subclass Control

ENABLE_JESD_VER_CONTROL	JESD_VERSION	JESD_SUBCLASS	JESD VERSION	FIELD VALUE	
				JESD VERSION	SUBCLASS VERSION
0	X[1]	X	JESD204B-subclass1	001	001
1	000	000	JESD204A	000	000
1	001	000	JESD204B-subclass 0	001	000
1	001	001	JESD204B-subclass 1	001	001
1	001	010	JESD204B-subclass 2	001	010

(1) X = don't care.

8.3.9.4 Transport Layer

In the JESD204B transport layer, the incoming stream of ADC samples are mapped to one or more parallel lanes and grouped into a frame of F octets for transmission on each lane. Additional tail bits can be appended to the ADC samples.

8.3.9.4.1 User Data Format

The interface can be configured to operate in 2, 4, or 8 lane modes (L = 2, 4, or 8). Depending on the number of lanes used, the data from the 16 ADCs comes out in the different lanes as shown in Table 17.

Table 17. Lane Mapping to CML Pins[1]

DEFAULT LANE ID	MAPPING TO THE PINS	2 ADCS PER LANE (8-Lane Mode)[2]	4 ADCS PER LANE (4-Lane Mode)[2]	8 ADCS PER LANE (2-Lane Mode)[2]
1	CML1_OUTP-CML1_OUTM	ADC1, ADC2	ADC1…ADC4	ADC1…ADC8
2	CML2_OUTP-CML2_OUTM	ADC3, ADC4	—	—
3	CML3_OUTP-CML3_OUTM	ADC5, ADC6	ADC5…ADC8	—
4	CML4_OUTP-CML4_OUTM	ADC7, ADC8	—	—
5	CML5_OUTP-CML5_OUTM	ADC9, ADC10	ADC9…ADC12	ADC9…ADC16
6	CML6_OUTP-CML6_OUTM	ADC11, ADC12	—	—
7	CML7_OUTP-CML7_OUTM	ADC13, ADC14	ADC13…ADC16	—
8	CML8_OUTP-CML8_OUTM	ADC15, ADC16	—	—

(1) More accurately, ADC1…ADC16 corresponds to CML_IN1…CML_IN16 as illustrated in Figure 72.
(2) Determined by the NUM_ADC_PER_LANE register control.

The unused lanes are automatically powered down.

The device supports several combinations of ADC resolutions and number of lanes. There are no control bits or control words (CF = 0). The device has two modes of data packing: normal packing mode and single converter per octet mode. The packing mode can be chosen using the SING_CONV_PER_OCT register control. The number of ADCs per lane can be programmed to 8, 4, or 2 using the NUM_ADC_PER_LANE register control. The number of ADCs per lane automatically determines the value of L (the number of lanes). The values of N' and F for the different modes are described in Table 18.

Table 18. Different JESD204B Interface Modes of Operation

NUMBER OF ADCS PER LANE, N_{AL} (1)	SER_DATA_RATE, N_{SER} (1)(2) (Bits)	ADC_RES, N_{RES} (1) (Bits)	L (3) (Lanes)	N (3) (Resolution of ADC Word Input to the JESD204B Transmitter)	NORMAL PACKING MODE (1)		SINGLE CONVERTER PER OCTET MODE (1)	
					N' (3) (Total Number of Bits)	F (3) (Octets per Frame)	N' (3) (Total Number of Bits)	F (3) (Octets per Frame)
8	10, 12, 14, 16	10, 12, 14, 16	2	ADC_RES	SER_DATA_RATE (4)	SER_DATA_RATE	16	16 (5)
4	10, 12, 14, 16	10, 12, 14, 16	4	ADC_RES	SER_DATA_RATE (4)	SER_DATA_RATE/2	16	8 (5)
2	10	10	8	ADC_RES	12	3 (6)	16	4 (5)
	12	10, 12		ADC_RES	12	3	16	4 (5)
	14	10, 12, 14		ADC_RES	16	4 (6)	16	4 (5)
	16	10, 12, 14, 16		ADC_RES	16	4	16	4 (5)

(1) Value or mode is set by programming the appropriate registers.
(2) SER_DATA_RATE must be greater than or equal to ADC_RES.
(3) Automatically calculated and set by the device.
(4) When SER_DATA_RATE > ADC_RES, then each ADC word is additionally padded with the (SER_DATA_RATE – ADC_RES) number of zeros on the LSB side to create the'JESD ADC word. Each JESD ADC word is broken up into nibbles. Incomplete nibbles (if any) are stuffed with the starting bits of the subsequent JESD ADC word for maximum data packing.
(5) Each ADC sample is broken into two octets; the incomplete octet is completed using zeros as tail bits.
(6) Each ADC sample is broken into nibbles; incomplete nibbles are completed using zeros as tail bits.

The data packing modes are described in Table 19 to Table 24 for different modes of operation. Lane 1 is used for illustration purposes in these tables.

Table 19. Data Packing in Normal Packing Mode for N_{AL} = 8 and N_{RES} = N_{SER} (1)

OCTET	N_{RES} = 10, N_{SER} = 10		N_{RES} = 12, N_{SER} = 12		N_{RES} = 14, N_{SER} = 14		N_{RES} = 16, N_{SER} = 16	
	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2
1	ADC1[9:6]	ADC1[5:2]	ADC1[11:8]	ADC1[7:4]	ADC1[13:10]	ADC1[9:6]	ADC1[15:12]	ADC1[11:8]
2	ADC1[1:0], ADC2[9:8]	ADC2[7:4]	ADC1[3:0]	ADC2[11:8]	ADC1[5:2]	ADC1[1:0], ADC2[13:12]	ADC1[7:4]	ADC1[3:0]
3	ADC2[3:0]	ADC3[9:6]	ADC2[7:4]	ADC2[3:0]	ADC2[11:8]	ADC2[7:4]	ADC2[15:12]	ADC2[11:8]
4	ADC3[5:2]	ADC3[1:0], ADC4[9:8]	ADC3[11:8]	ADC3[7:4]	ADC2[3:0]	ADC3[13:10]	ADC2[7:4]	ADC2[3:0]
5	ADC4[7:4]	ADC4[3:0]	ADC3[3:0]	ADC4[11:8]	ADC3[9:6]	ADC3[5:2]	ADC3[15:12]	ADC3[11:8]
6	ADC5[9:6]	ADC5[5:2]	ADC4[7:4]	ADC4[3:0]	ADC3[1:0], ADC4[13:12]	ADC4[11:8]	ADC3[7:4]	ADC3[3:0]
7	ADC5[1:0], ADC6[9:8]	ADC6[7:4]	ADC5[11:8]	ADC5[7:4]	ADC4[7:4]	ADC4[3:0]	ADC4[15:12]	ADC4[11:8]
8	ADC6[3:0]	ADC7[9:6]	ADC5[3:0]	ADC6[11:8]	ADC5[13:10]	ADC5[9:6]	ADC4[7:4]	ADC4[3:0]
9	ADC7[5:2]	ADC7[1:0], ADC8[9:8]	ADC6[7:4]	ADC6[3:0]	ADC5[5:2]	ADC5[1:0], ADC6[13:12]	ADC5[15:12]	ADC5[11:8]
10	ADC7[7:4]	ADC8[3:0]	ADC7[11:8]	ADC7[7:4]	ADC6[11:8]	ADC6[7:4]	ADC5[7:4]	ADC5[3:0]
11	—	—	ADC7[3:0]	ADC8[11:8]	ADC6[3:0]	ADC7[13:10]	ADC6[15:12]	ADC6[11:8]
12	—	—	ADC8[7:4]	ADC8[3:0]	ADC7[9:6]	ADC7[5:2]	ADC6[7:4]	ADC6[3:0]
13	—	—	—	—	ADC7[1:0], ADC8[13:12]	ADC8[11:8]	ADC7[15:12]	ADC7[11:8]
14	—	—	—	—	ADC8[7:4]	ADC8[3:0]	ADC7[7:4]	ADC7[3:0]
15	—	—	—	—	—	—	ADC8[15:12]	ADC8[11:8]
16	—	—	—	—	—	—	ADC8[7:4]	ADC8[3:0]

(1) A similar data packing scheme is used for other lanes with the mapping of ADCs per lane as indicated in Table 17.

Table 20. Data Packing in Normal Packing Mode for N_{AL} = 8 and N_{SER} > N_{RES} (1)

OCTET	N_{RES} = 10, N_{SER} = 12		N_{RES} = 12, N_{SER} = 14		N_{RES} = 14, N_{SER} = 16	
	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2
1	ADC1[9:6]	ADC1[5:2]	ADC1[11:8]	ADC1[7:4]	ADC1[13:10]	ADC1[9:6]
2	ADC1[1:0], 00	ADC2[9:6]	ADC1[3:0]	00,ADC2[11:10]	ADC1[5:2]	ADC1[1:0], 00
3	ADC2[5:2]	ADC2[1:0], 00	ADC2[9:6]	ADC2[5:2]	ADC2[13:10]	ADC2[9:6]
4	ADC3[9:6]	ADC3[5:2]	ADC2[1:0],00	ADC3[11:8]	ADC2[5:2]	ADC2[1:0], 00
5	ADC3[1:0], 00	ADC4[9:6]	ADC3[7:4]	ADC3[3:0]	ADC3[13:10]	ADC3[9:6]
6	ADC4[5:2]	ADC4[1:0], 00	00,ADC4[11:10]	ADC4[9:6]	ADC3[5:2]	ADC3[1:0], 00
7	ADC5[9:6]	ADC5[5:2]	ADC4[5:2]	ADC4[1:0],00	ADC4[13:10]	ADC4[9:6]
8	ADC5[1:0], 00	ADC6[9:6]	ADC5[11:8]	ADC5[7:4]	ADC4[5:2]	ADC4[1:0], 00
9	ADC6[5:2]	ADC6[1:0], 00	ADC5[3:0]	00,ADC6[11:10]	ADC5[13:10]	ADC5[9:6]
10	ADC7[9:6]	ADC7[5:2]	ADC6[9:6]	ADC6[5:2]	ADC5[5:2]	ADC5[1:0], 00
11	ADC7[1:0], 00	ADC8[9:6]	ADC6[1:0],00	ADC7[11:8]	ADC6[13:10]	ADC6[9:6]
12	ADC8[5:2]	ADC8[1:0], 00	ADC7[7:4]	ADC7[3:0]	ADC6[5:2]	ADC6[1:0], 00
13	—	—	00,ADC8[11:10]	ADC8[9:6]	ADC7[13:10]	ADC7[9:6]
14	—	—	ADC8[5:2]	ADC8[1:0],00	ADC7[5:2]	ADC7[1:0], 00
15	—	—	—	—	ADC8[13:10]	ADC8[9:6]
16	—	—	—	—	ADC8[5:2]	ADC8[1:0], 00

(1) A similar data packing scheme is used for other lanes with the mapping of ADCs per lane as indicated in Table 17.

Table 21. Data Packing in Normal Packing Mode for N_{AL} = 4 and N_{RES} = N_{SER} (1)

OCTET	N_{RES} = 10, NSER = 10		N_{RES} = 12, N_{SER} = 12		N_{RES} = 14, N_{SER} = 14		N_{RES} = 16, N_{SER} = 16	
	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2
1	ADC1[9:6]	ADC1[5:2]	ADC1[11:8]	ADC1[7:4]	ADC1[13:10]	ADC1[9:6]	ADC1[15:12]	ADC1[11:8]
2	ADC1[1:0], ADC2[9:8]	ADC2[7:4]	ADC1[3:0]	ADC2[11:8]	ADC1[5:2]	ADC1[1:0], ADC2[13:12]	ADC1[7:4]	ADC1[3:0]
3	ADC2[3:0]	ADC3[9:6]	ADC2[7:4]	ADC2[3:0]	ADC2[11:8]	ADC2[7:4]	ADC2[15:12]	ADC2[11:8]
4	ADC3[5:2]	ADC3[1:0], AD4[9:8]	ADC3[11:8]	ADC3[7:4]	ADC2[3:0]	ADC3[13:10]	ADC2[7:4]	ADC2[3:0]
5	ADC4[7:4]	ADC4[3:0]	ADC3[3:0]	ADC4[11:8]	ADC3[9:6]	ADC3[5:2]	ADC3[15:12]	ADC3[11:8]
6	—	—	ADC4[7:4]	ADC4[3:0]	ADC3[1:0], ADC4[13:12]	ADC4[11:8]	ADC3[7:4]	ADC3[3:0]
7	—	—	—	—	ADC4[7:4]	ADC4[3:0]	ADC4[15:12]	ADC4[11:8]
8	—	—	—	—	—	—	ADC4[7:4]	ADC4[3:0]

(1) A similar data packing scheme is used for other lanes with the mapping of ADCs per lane as indicated in Table 17.

Table 22. Data Packing in Normal Packing Mode for N_{AL} = 4 and N_{SER} > N_{RES} (1)

OCTET	N_{RES} = 10, NSER = 12		N_{RES} = 12, N_{SER} = 14		N_{RES} = 14, N_{SER} = 16	
	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2
1	ADC1[9:6]	ADC1[5:2]	ADC1[11:8]	ADC1[7:4]	ADC1[13:10]	ADC1[9:6]
2	ADC1[1:0], 00	ADC2[9:6]	ADC1[3:0]	00,ADC2[11:10]	ADC1[5:2]	ADC1[1:0], 00
3	ADC2[5:2]	ADC2[1:0], 00	ADC2[9:6]	ADC2[5:2]	ADC2[13:10]	ADC2[9:6]
4	ADC3[9:6]	ADC3[5:2]	ADC2[1:0],00	ADC3[11:8]	ADC2[5:2]	ADC2[1:0], 00
5	ADC3[1:0], 00	ADC4[9:6]	ADC3[7:4]	ADC3[3:0]	ADC3[13:10]	ADC3[9:6]
6	ADC4[5:2]	ADC4[1:0], 00	00,ADC4[11:10]	ADC4[9:6]	ADC3[5:2]	ADC3[1:0], 00
7	—	—	ADC4[5:2]	ADC4[1:0],00	ADC4[13:10]	ADC4[9:6]
8	—	—	—	—	ADC4[5:2]	ADC4[1:0], 00

(1) A similar data packing scheme is used for other lanes with the mapping of ADCs per lane as indicated in Table 17.

Table 23. Data Packing in Normal Packing Mode for N_{AL} = 2(1)

OCTET	N_{RES} = 10, NSER = 10 or 12		N_{RES} = 12, N_{SER} = 12		N_{RES} = 14, N_{SER} = 14 or 16		N_{RES} = 16, N_{SER} = 16	
	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2
1	ADC1[9:6]	ADC1[5:2]	ADC1[11:8]	ADC1[7:4]	ADC1[13:10]	ADC1[9:6]	ADC1[15:12]	ADC1[11:8]
2	ADC1[1:0], 00	ADC2[9:6]	ADC1[3:0]	ADC2[11:8]	ADC1[5:2]	ADC1[1:0], 00	ADC1[7:4]	ADC1[3:0]
3	ADC2[5:2]	ADC3[1:0], 00	ADC2[7:4]	ADC2[3:0]	ADC2[13:10]	ADC2[9:6]	ADC2[15:12]	ADC2[11:8]
4	—	—	—	—	ADC2[5:2]	ADC2[1:0], 00	ADC2[7:4]	ADC2[3:0]

(1) A similar data packing scheme is used for other lanes with the mapping of ADCs per lane as indicated in Table 17.

Table 24. Data Packing in Single Converter per Octet Packing Mode for N_{AL} = 8 (Independent of N_{SER})(1)(2)

OCTET	N_{RES} = 10		N_{RES} = 12		N_{RES} = 14		N_{RES} = 16, N_{SER} = 16	
	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2	NIBBLE 1	NIBBLE 2
1	ADC1[9:6]	ADC1[5:2]	ADC1[11:8]	ADC1[7:4]	ADC1[13:10]	ADC1[9:6]	ADC1[15:12]	ADC1[11:8]
2	ADC1[1:0], 00	0000	ADC1[3:0]	0000	ADC1[5:2]	ADC1[1:0], 00	ADC1[7:4]	ADC1[3:0]
3	ADC2[9:6]	ADC2[5:2]	ADC2[11:8]	ADC2[7:4]	ADC2[13:10]	ADC2[9:6]	ADC2[15:12]	ADC2[11:8]
4	ADC2[1:0], 00	0000	ADC2[3:0]	0000	ADC2[5:2]	ADC2[1:0], 00	ADC2[7:4]	ADC2[3:0]
5	ADC3[9:6]	ADC3[5:2]	ADC3[11:8]	ADC3[7:4]	ADC3[13:10]	ADC3[9:6]	ADC3[15:12]	ADC3[11:8]
6	ADC3[1:0], 00	0000	ADC3[3:0]	0000	ADC3[5:2]	ADC3[1:0], 00	ADC3[7:4]	ADC3[3:0]
7	ADC4[9:6]	ADC4[5:2]	ADC4[11:8]	ADC4[7:4]	ADC4[13:10]	ADC4[9:6]	ADC4[15:12]	ADC4[11:8]
8	ADC4[1:0], 00	0000	ADC4[3:0]	0000	ADC4[5:2]	ADC4[1:0], 00	ADC4[7:4]	ADC4[3:0]
9	ADC5[9:6]	ADC5[5:2]	ADC5[11:8]	ADC5[7:4]	ADC5[13:10]	ADC5[9:6]	ADC5[15:12]	ADC5[11:8]
10	ADC5[1:0], 00	0000	ADC5[3:0]	0000	ADC5[5:2]	ADC5[1:0], 00	ADC5[7:4]	ADC5[3:0]
11	ADC6[9:6]	ADC6[5:2]	ADC6[11:8]	ADC6[7:4]	ADC6[13:10]	ADC6[9:6]	ADC6[15:12]	ADC6[11:8]
12	ADC6[1:0], 00	0000	ADC6[3:0]	0000	ADC6[5:2]	ADC6[1:0], 00	ADC6[7:4]	ADC6[3:0]
13	ADC7[9:6]	ADC7[5:2]	ADC7[11:8]	ADC7[7:4]	ADC7[13:10]	ADC7[9:6]	ADC7[15:12]	ADC7[11:8]
14	ADC7[1:0], 00	0000	ADC7[3:0]	0000	ADC7[5:2]	ADC7[1:0], 00	ADC7[7:4]	ADC7[3:0]
15	ADC8[9:6]	ADC8[5:2]	ADC8[11:8]	ADC8[7:4]	ADC8[13:10]	ADC8[9:6]	ADC8[15:12]	ADC8[11:8]
16	ADC8[1:0], 00	0000	ADC8[3:0]	0000	ADC8[5:2]	ADC8[1:0], 00	ADC8[7:4]	ADC8[3:0]

(1) For N_{AL} = 4, use the first eight octets. For N_{AL} = 2, use the first four octets.
(2) A similar data packing scheme is used for other lanes with the mapping of ADCs per lane as indicated in Table 17.

Tail bits (in modes where applicable) are set to 0. There is no option for a pseudo-random generator for generating the tail bits. When a converter is powered down, the corresponding sample is replaced by a dummy sample that corresponds to all zeros. There is no option for a pseudo-random generator for generating the dummy samples. The value *S* (number of samples per ADC per frame minus 1) is always 0 and HD mode is not supported.

8.3.9.4.2 Transport Layer Test Patterns

All test patterns described in the *LVDS Test Pattern Mode* section can be set, even with the JESD204B interface. These test patterns serve as transport layer test modes for the JESD interface. These test patterns can replace the normal ADC data going into the JESD204B link layer.

8.3.9.5 Scrambler

An optional scrambler is implemented in the device using the polynomial as defined in the JESD204B standard. The scrambler can be enabled using the SCR_EN register control. The scrambler is bypassed during the code group synchronization and transmission of the initial lane alignment sequence. There is no alternate scrambler to keep processing the user data during these states.

8.3.9.6 Data Link Layer

The data link layer of the JESD204B block handles various functions (such as the 8b, 10b encoding of the input octets, code group synchronization (CGS), transmission of an initial lane alignment (ILA) sequence, frame alignment character replacement, and transmission of link layer test patterns). As specified by the standard, the device uses 8b, 10b coding to encode the data before being transmitted. The frame contents are processed from MSB to LSB.

8.3.9.6.1 Code Group Synchronization (CGS)

In the CGS state, the device transmits a set of /K28.5/ characters that are used by the receiver to recover the clock and data from the serial stream using a clock and data recovery (CDR) circuit, and also to align to the symbol boundaries. The device enters the CGS state when it receives an active (low going) SYNC pulse that is at least four device clocks wide. In addition, when the device is in the CGS state as defined by the JESD204B standard, the device can also be made to transmit a stream of /K28.5/ symbols by programming the TX_SYNC_REQ register control.

8.3.9.6.2 Initial Lane Alignment (ILA)

By default, the CGS phase is followed by the transmission of an ILA sequence. The ILA transmission can be disabled using the LINK_CONFIG_DIS register control. Transitioning from a CGS state to an ILA sequence state occurs on the local multiframe clock (LMFC) boundary. By default, the transition occurs at the first LMFC boundary after SYNC~ is deasserted. However, the transition point can be delayed to the second, third, or fourth LMFC edge by programming the RELEASE_ILA register control to 1, 2, or 3, respectively. This mode can be used to provide sufficient time to the receiver to achieve synchronization.

8.3.9.6.3 Lane and Frame Alignment Monitoring

The lane and frame alignment monitoring and character replacement are as per the JESD204B standard. The insertion of frame and lane alignment characters can be enabled by setting the LANE_ALIGN and FRAME_ALIGN register controls. These controls, in conjunction with the SCR_EN control, determine the mechanism of the lane and frame alignment character replacement, as shown in Table 25.

Table 25. Character Replacement for Lane and Frame Alignment

SCR_EN	FRAME_ALIGN	LANE_ALIGN	EFFECT ON LINK DATA
0	0	0	ADC data are sent without any character replacement.
0	0	1	If the last octet of the multiframe is the same as the last octet of the previous multiframe, then the last octet is replaced with /K28.3/.
0	1	0	If the last octet of the frame is the same as the last octet of the previous frame, then the last octet is replaced with /K28.7/. If an alignment character has already been sent in the previous frame, then no characters are replaced.
0	1	1	Frame and lane alignment character replacements are enabled.
1	0	0	ADC data are scrambled and sent without any character replacement.
1	0	1	If the last scrambled octet of the multiframe is D28.3, then that octet is replaced with /K28.3/.
1	1	0	If the last scrambled octet of the frame is D28.7, then that octet is replaced with /K28.7/.
1	1	1	Frame and lane alignment character replacements are enabled with scrambling.

8.3.9.6.4 Link Layer Test Modes

The JESD link can be tested by transmitting predetermined 8b, 10b characters in all frames and on all lanes. Test modes can be enabled with the LINK_LAYER_TESTMODES register control. These test patterns are never scrambled. A pseudo-random pattern of 120 bits corresponds to the random pattern (RPAT). An additional PRBS pattern can be output by setting the transport layer test mode to a constant pattern and enabling the scrambler. A scrambled jitter pattern (JSPAT) is not supported.

8.3.9.7 Deterministic Latency

Deterministic latency is achieved in the subclass 1 and subclass 2 of the JESD204B standard through a local multiframe clock (LMFC) that is synchronized between the transmitter and receiver. The phase of the LMFC is dictated by the sampled SYSREF input in subclass 1 and by the SYNC~ rising edge in subclass 2.

8.3.9.7.1 Synchronization Using SYNC~ and SYSREF

In order to achieve deterministic latency across the entire link, the device supports system-level link synchronization using the SYNC~ (in subclass 2) and SYSREF (in subclass 1) signals, as mentioned in the JESD204B standards document. The mapping of these signals to the pin voltages is shown in Table 26.

Table 26. Mapping of the JESD204B Signals to Device Pins

SIGNAL NOTATION IN JESD204B DOCUMENT	RELATION TO DEVICE PINS
Device clock	ADC_CLKP – ADC_CLKM
SYNC~	SYNCP_SERDES – SYNCM_SERDES
SYSREF(1)	SYSREFP_SERDES – SYSREFM_SERDES

(1) Must be inactive (low) except when operating in JESD204B subclass 1.

JESD subclasses 1 and 2 use an internal clock called the local multiframe clock (LMFC) to achieve deterministic latency in the link. The phase of the LMFC clock is set based on the device clock rising edge that the SYSREF (in subclass 1) or SYNC~(in subclass 2) signals are sampled on. The device clock is the highest speed input clock for the device and there is no provision for a higher speed adjustment clock to achieve phase adjustments finer than what is achievable using the device clock. By default, the LMFC count is reset to 0 during a SYNC~ or SYSREF event. This reset count can be forced to a different value by using the FORCE_LMFC_COUNT and LMFC_COUNTER_INIT_VALUE register controls. The LMFC does not exist in JESD subclass 0.

SYSREF can be a periodic, one-shot, or gapped periodic active-high signal that is sampled on the rising edge of the device clock. There is no option to sample the SYSREF signal on the falling edge of the device clock. If SYSREF is a periodic or gapped periodic signal, then its periodicity must be a multiple of the LMFC period in order to avoid unwanted sudden shifts in the phase of the LMFC. Note that a continuous periodic SYSREF can cause spurious degradation in the ADC performance because of energy coupling into the device at a rate that is a sub-harmonic of the device clock rate.

In addition to resetting the phase of the LMFC, SYSREF (or SYNC~) also resets some of the other internal clock dividers not related to the JESD block and affects the reset of the phase of the test pattern generator (see the *LVDS Test Pattern Mode* section). SYSREF (or SYNC~) also affects the reset of the frame clock phases and the odd or even sampling selection in 32-channel mode.

The default mode is to reset all internal dividers as well as the phase of the LMFC during every SYSREF (or SYNC~) event based on the JESD subclass.

The reset operations based on SYNC~ and SYSREF for the different subclasses occurs as shown in Table 27.

Table 27. Reset Operations from SYNC~ or SYSREF in the Various JESD204B Subclasses

SUBCLASS	EVENT CONTROLLING THE RESET	What gets reset	
		JESD BLOCK (Phase of the LMFC Clock)	REST OF DEVICE
JESD204B-subclass 0	SYNC~ rising edge	Not applicable	Yes
JESD204B-subclass 1	SYSREF(1)	Yes	Yes
JESD204B-subclass 2	SYNC~ rising edge	Yes	Yes
JESD204A	SYNC~ rising edge	Not applicable	Yes

(1) To avoid unexpected reset behavior, SYSREF must be active only when operating in JESD204B subclass 1.

Table 28 lists the register controls to selectively mask the reset operations of the various blocks.

Table 28. Masking of the Various Reset Operations Resulting from SYNC~ or SYSREF

REGISTER BIT	MASKS RESET OPERATION IN		
	JESD BLOCK (Phase of the LMFC Clock)	CLOCK DIVIDERS	OTHER SYNCHRONIZATION(1)
JESD_RESET1	No	Yes	Yes
JESD_RESET2	Yes	Yes	No

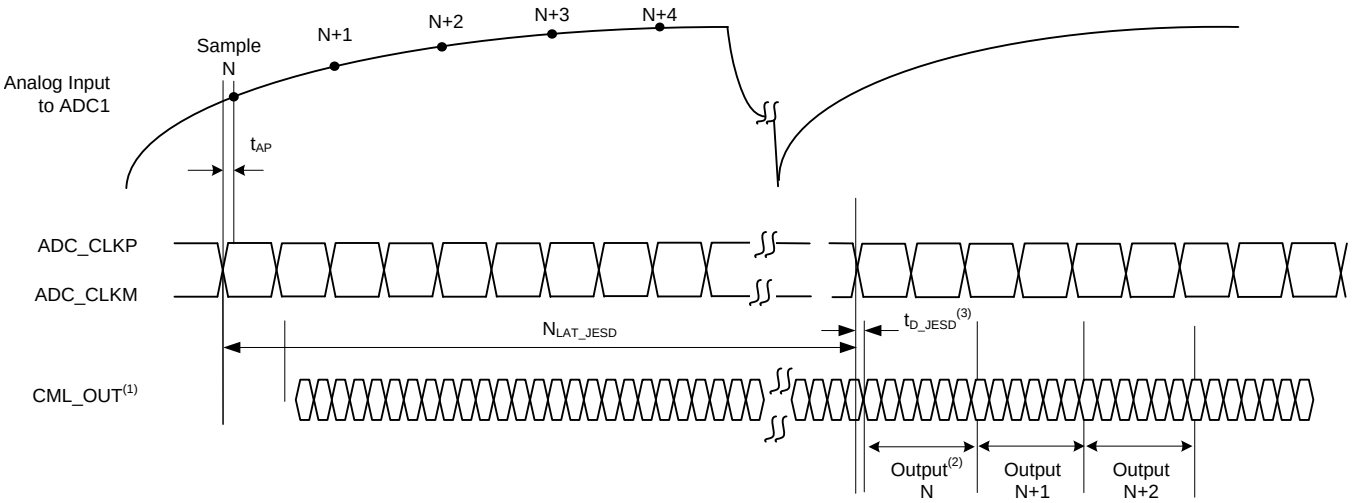
(1) Demodulators and test pattern generation.

The JESD_RESET1 and JESD_RESET2 bits mask the reset operations as indicated in Table 28 for all subsequent SYNC~ and SYSREF events after the bits are set. The JESD_RESET3 register bit is functionally similar to JESD_RESET2 (in terms of masking the reset function to the blocks). However, when JESD_RESET3 is set, this bit allows the first SYNC~ or SYSREF event to reset all clock dividers, takes affect, and masks the reset of the LMFC clock divider only after the first SYNC~ or SYSREF event occurs. The JESD_RESET1, JESD_RESET2, and JESD_RESET3 bits can be used appropriately to avoid unwanted reset operations resulting from SYNC~ and SYSREF events.

When SYSREF resets the rest of the device, the ADC data can be corrupted for four to six clocks. If SYSREF is periodic, then periodic corruption of ADC data can result. Thus, when using a periodic or a gapped periodic SYSREF, one JESD_RESET (JESD_RESET1, JESD_RESET2, or JESD_RESET3) must be set to 1.

8.3.9.7.2 Latency

Figure 73 to Figure 76 illustrate the relevant latencies for the JESD interface with the default mode of operation (four ADCs per lane mode, N_{ADC} = 12, N_{SER} = 12, and K = 3) used for illustration purposes.

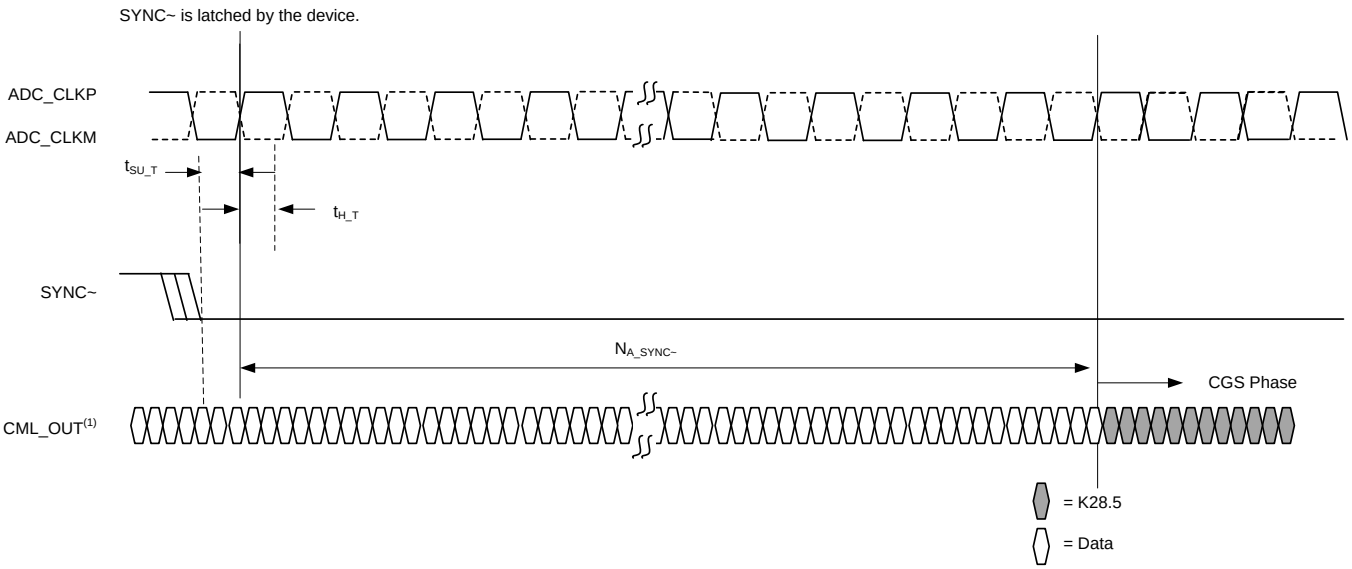


(1) CML_OUT is shown broken in terms of octets.

(2) The ADC word corresponding to ADC1 is contained in the first two octets of output *N*.

(3) t_{D_JESD} is a small additional variable delay which is a fraction of the device clock period.

Figure 73. ADC Latency in JESD Mode



(1) CML_OUT is broken in terms of octets.

Figure 74. Latency from SYNC~ Assertion to Start of CGS Phase

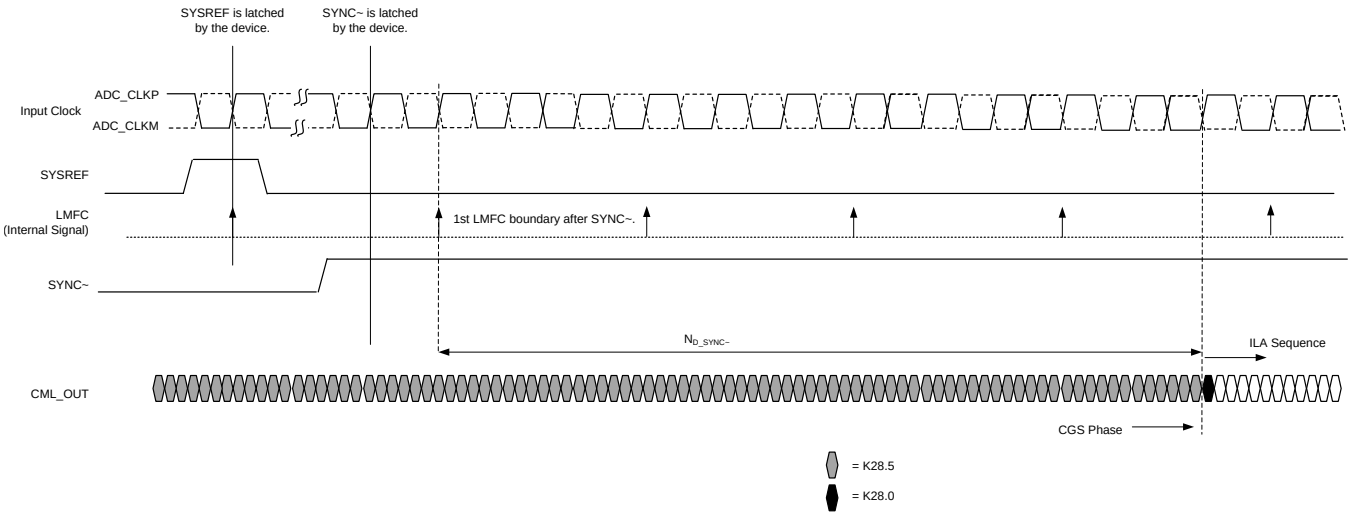


Figure 75. Latency from SYNC~ Deassertion to Start of ILA Phase in Subclass 1

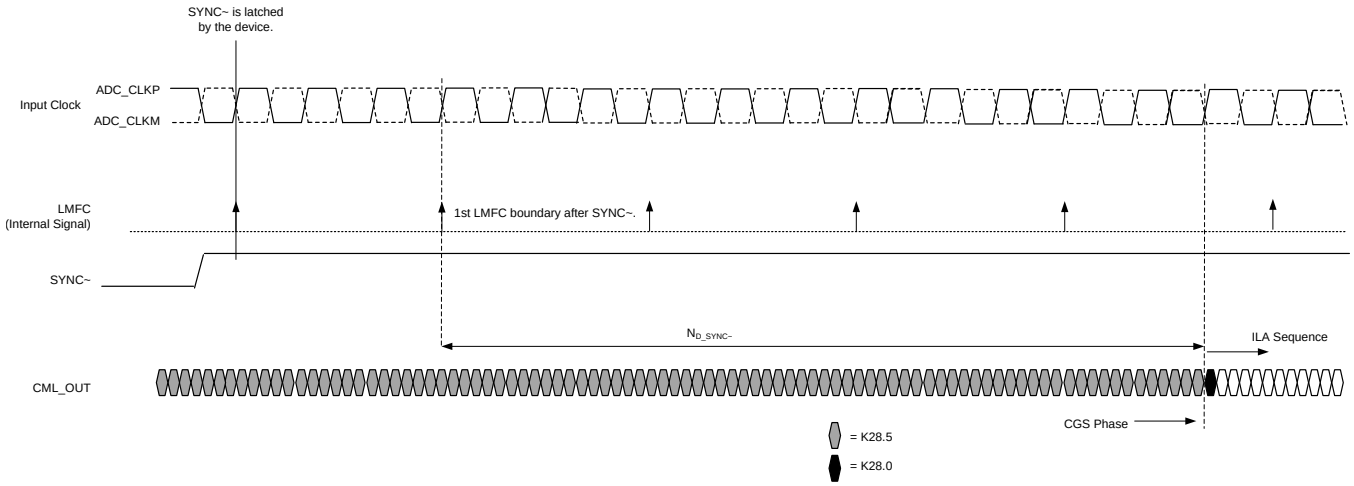


Figure 76. Latency from SYNC~ Deassertion to Start of ILA Phase in Subclass 2

8.3.9.7.3 Multiframe Size

The size of the multiframe (as well as the periodicity of the LMFC clock) is denoted as K. Multiframe size is calculated as shown in Equation 2:

Ceil (17 / Number of Octets per Frame) ≤ Multiframe Size (In Terms of Number of Frames) (2)

Table 29 lists the multiframe size for different modes of operation.

Table 29. Multiframe Size in Different Modes(1)

ADC RESOLUTION (Bits)	2 ADCS PER LANE(2)			4 ADCS PER LANE(2)			8 ADCS PER LANE(2)		
	FRAME SIZE (Octets)	MULTIFRAME SIZE		FRAME SIZE (Octets)	MULTIFRAME SIZE		FRAME SIZE (Octets)	MULTIFRAME SIZE	
		FRAMES	OCTETS		FRAMES	OCTETS		FRAMES	OCTETS
12	3	6	18	6	3	18	12	2	24
14	4	5	20	7	3	21	14	2	28
16	4	5	20	8	3	24	16	2	32

(1) The decimal equivalent of K[4:0] in the link configuration parameter is equal to the multiframe size (in frames) minus 1.
(2) Determined by the register control NUM_ADC_PER_LANE.

8.3.9.8 JESD Physical Layer

The JESD transmitter uses a PLL that runs off an internal low-dropout (LDO) regulator that provides noise rejection on the external 1.2-V supply. At higher speeds (beyond 4 Gbps), the LDO voltage drops because of increased switching currents. To improve the jitter at higher speeds, restore the LDO voltage with the INC_JESD_VDD register control.

8.3.9.8.1 CML Buffer

The device JESD204B transmitter uses differential CML output drivers with a typical current drive of 16 mA. The output driver includes an internal 50-Ω termination to the DVDD_1P2 supply. Additionally, external 50-Ω termination resistors connected to DVDD_1P2 must be placed close to the receiver pins. DC compliance to the standard is not ensured and ac coupling can be used to avoid the common-mode mismatch between the transmitter and receiver, as shown in Figure 77.

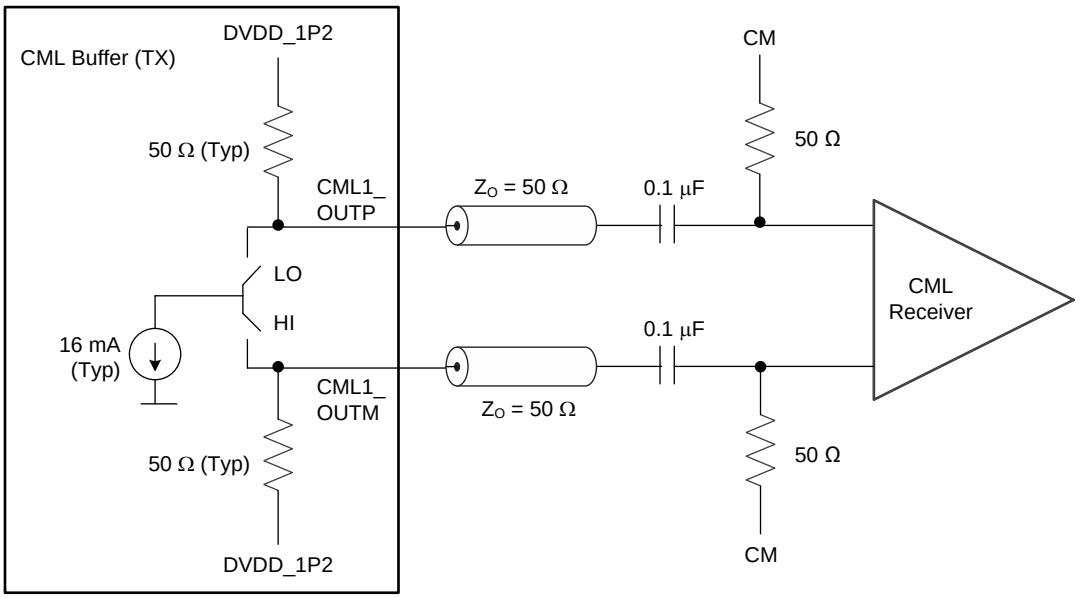


Figure 77. CML Output Connections

The CML buffer also has a pre-emphasis control for improving the timing margins. Pre-emphasis is achieved by increasing the CML buffer current if the current transmitter bit is different from the previous one. The current of the CML buffer for a transitioning bit can be increased from the CML buffer current setting to one of 16 settings in steps of 0.25 mA using the PRE_EMP register control. Pre-emphasis is recommended to be used at higher speeds in order to improve the timing margins.

8.3.9.8.2 Jitter Considerations

Figure 78 shows the data eye measurement of the device JESD204B transmitter against the JESD204B transmitter eye mask at 3.125 Gbps.

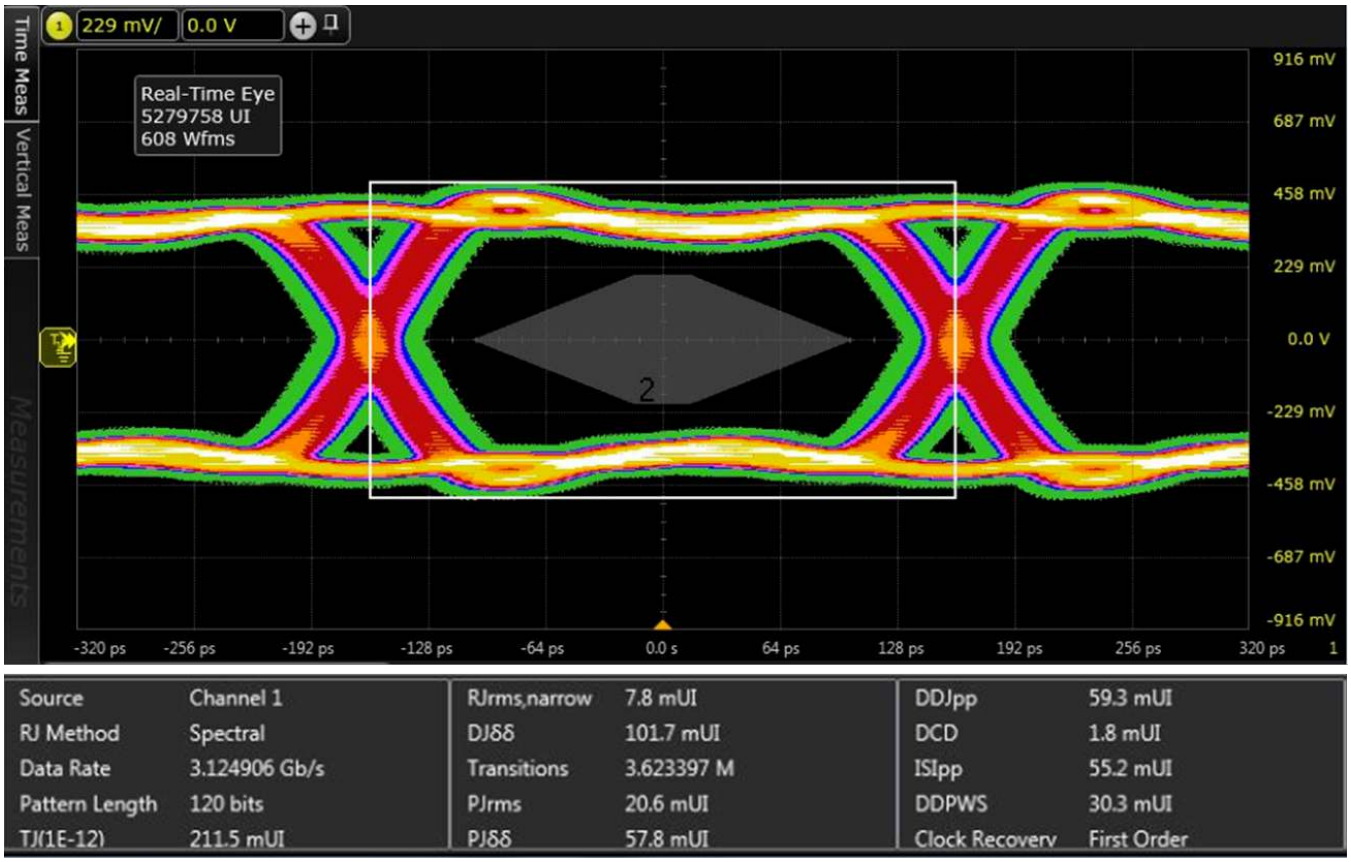


Figure 78. Eye Diagram at the CML Output at a Data Rate of 3.125 Gbps

Figure 79 shows the data eye measurement of the device JESD204B transmitter against the JESD204B transmitter eye mask at 5 Gbps. This measurement is taken with PRE_EMP set to 7.

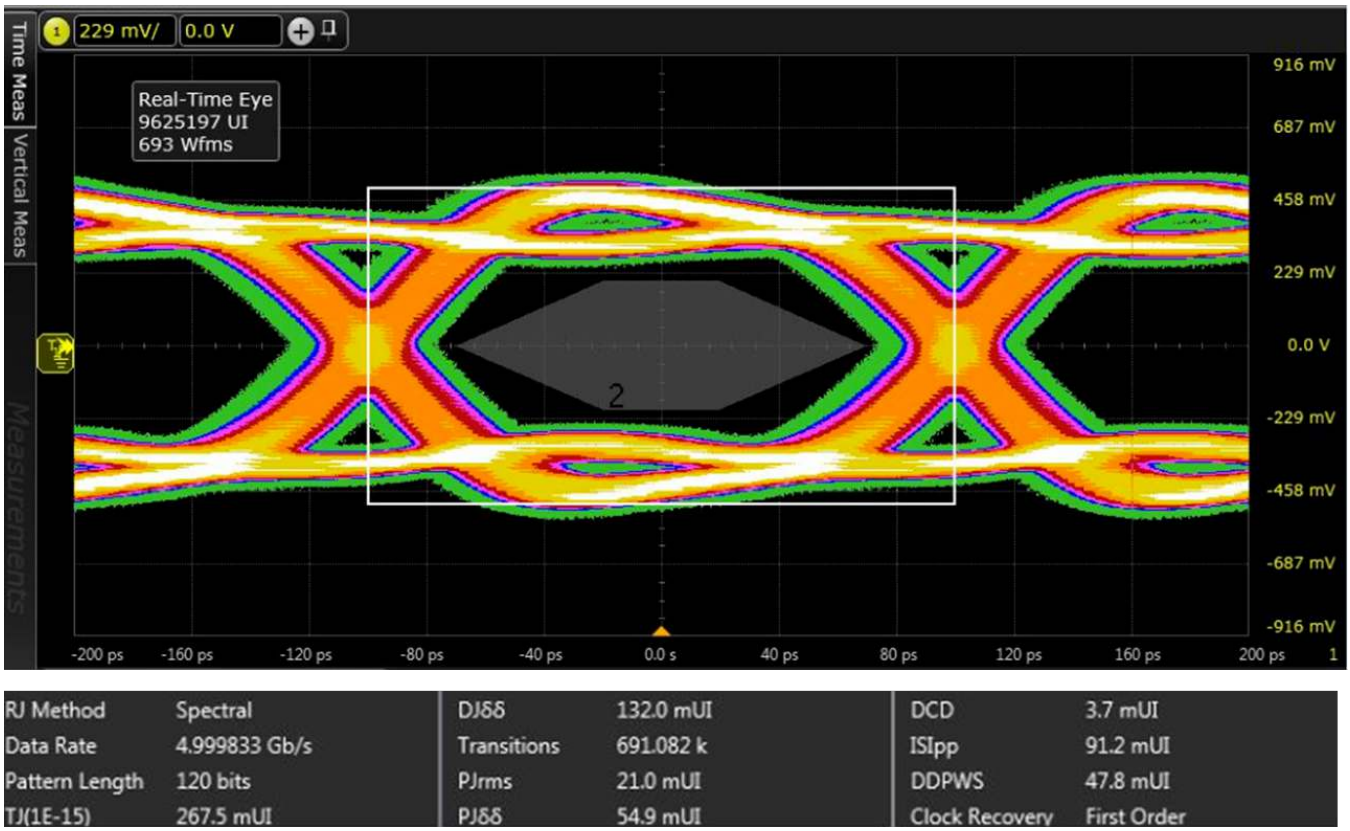


Figure 79. Eye Diagram at the CML Output at a Data Rate of 5 Gbps

The total jitter as a fraction of the UI changes with interface speed, pre-emphasis setting, and the length of the trace from the transmitter pins to the external termination resistor. The total jitter at the transmitter pins can exceed the transmitter eye mask specification for speeds beyond 5 Gbps. However, the interface can be made to work (and meet the eye mask specification at the receiver inputs) at speeds higher than 5 Gbps for short trace lengths. Figure 40 illustrates the total jitter as a function of the trace length (between the transmitter pins and the termination resistor) for 5-Gbps, 6-Gbps, and 6.4-Gbps speeds. Figure 41 to Figure 43 illustrate the total jitter as a function of the trace length for different pre-emphasis settings at 5 Gbps, 6 Gbps, and 6.4 Gbps, respectively.

8.3.10 Interfacing SYNC~ and SYSREF Between the FPGA and ADCs

The SYNC~ and SYSREF signals must be connected to the FPGA and the multiple ADCs in the system. When driving SYNC~ and SYSREF using differential signals, additional interface circuits may be required to decouple the common-mode levels between the FPGA and the ADC. Figure 80 shows an overview of such a scheme for driving the SYNC~ signal from the FPGA to multiple ADCs.

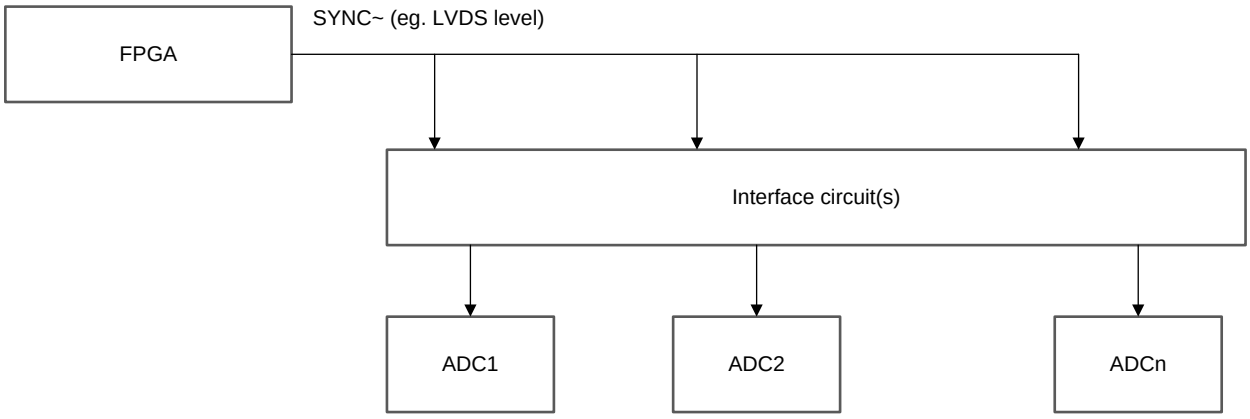


Figure 80. Connection of SYNC~ From the FPGA to the ADCs

The ADC has internal 5-kΩ resistors from the SYNCP and SYNCM pins to an internal reference voltage of 0.7 V. When driven by a differential driver, an interface circuit may be required to match the common-mode voltages between the driver and the ADC. An example circuit is shown in Figure 81 to level-shift from a 1.2-V common-mode voltage at the driver output to the 0.7 V at the ADC input. The 100 Ω at the driver output depicts the differential termination and could be realized inside the FPGA.

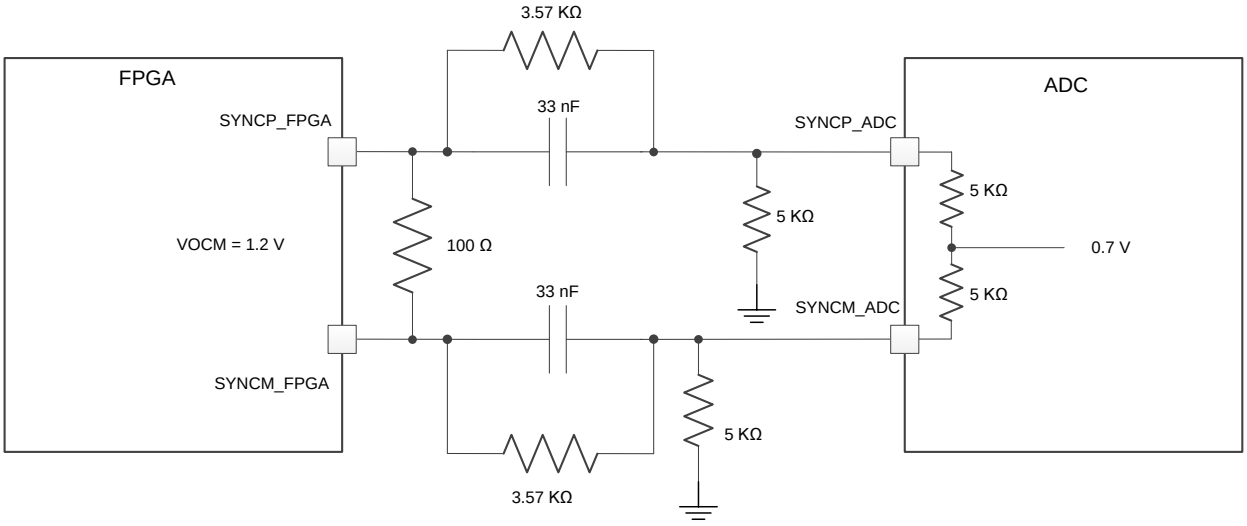


Figure 81. Circuit to Level-Shift the Common-Mode Voltage From 1.2 V at the Driver Output to 0.7 V at the ADC Input

For a different driver output common-mode than the one shown in Figure 81, the interface circuit must be modified.

A similar circuit as shown in Figure 81 can also be used to interface the SYSREF signals to the ADC. As shown in Figure 82, the SYSREF signal can also be driven using an ac-coupling scheme. The external components are chosen for a case where the SYSREF source drives only one ADC. The values of these components must be changed if the signal is interfaced to multiple ADCs (contact the factory for details).

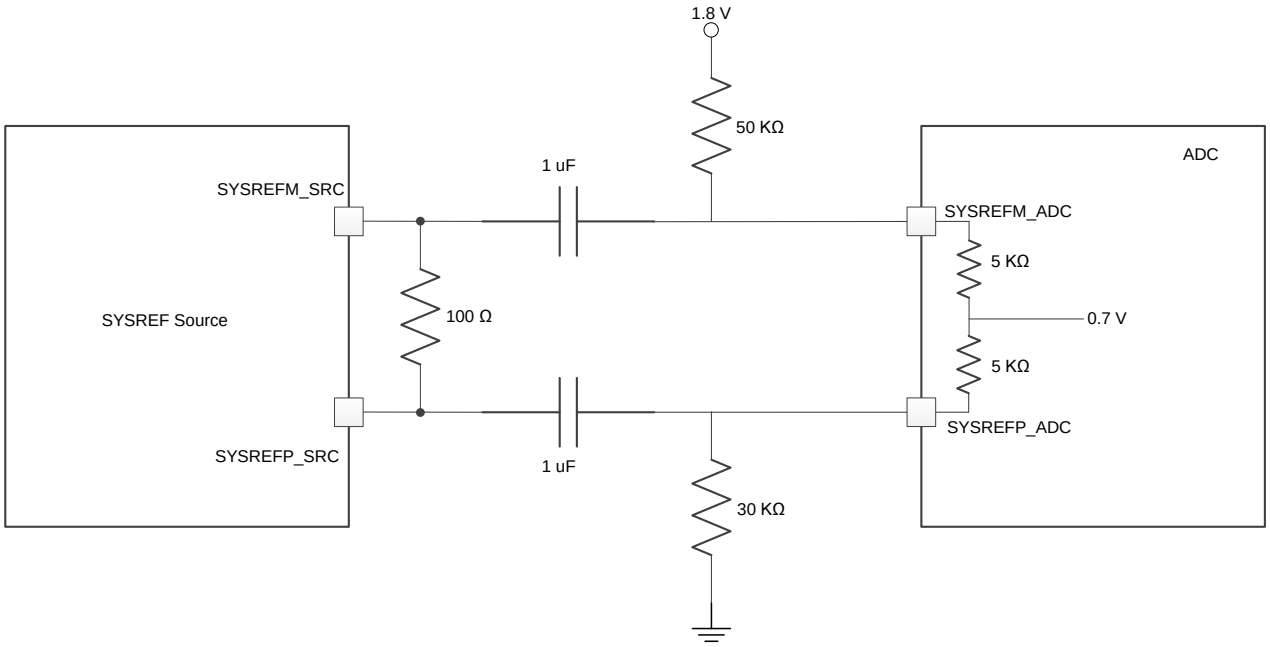


Figure 82. AC-Coupling Scheme for SYSREF (do not use for SYNC~)

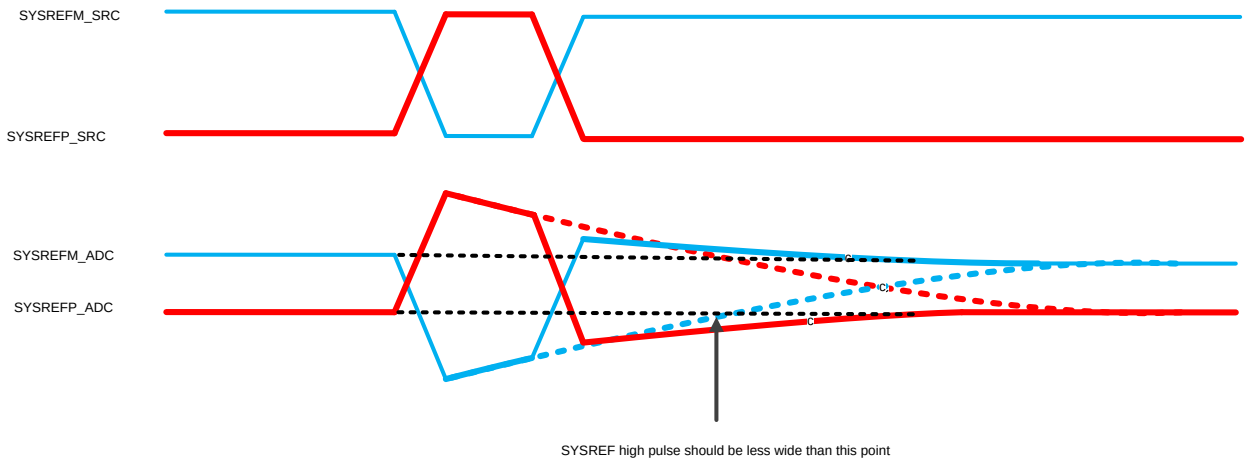


Figure 83. Transient of SYSREF With AC-Coupling

The 50-kΩ and 30-kΩ external resistors along with the two 5-kΩ resistors internal to the ADC form a voltage divider circuit to generate a negative differential offset at the ADC SYSREF input when SYSREF is low. A high-going pulse on the SYSREF_SRC signal passes through the ac-coupling capacitor. The ac-coupling capacitor and the resistors form a high-pass filter and cause the SYSREF_ADC signal to droop towards their quiescent values over time (denoted by the dotted lines in Figure 83). However, if the high width of SYSREF is much lower than the time constant of the filter, the circuit is able to pass the pulse properly.

The SYNC~ and SYSREF signals also can be driven using single-ended LVCMOS levels, which can be done by driving the P side with the LVCMOS level and connecting the M side to ground as shown in Figure 84. When driven in this manner, the internal 5-kΩ resistor (connecting the P and M pins to the 0.7-V node) is disconnected from the pins.

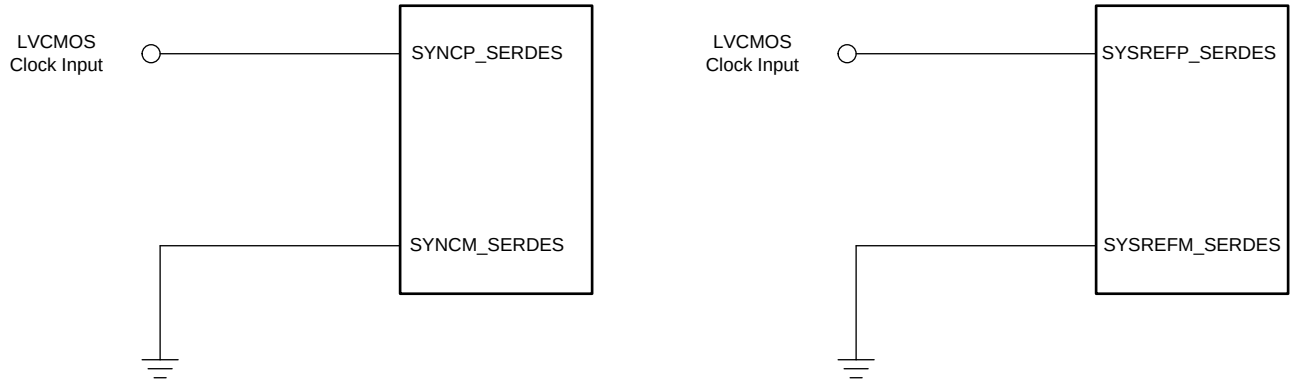


Figure 84. Single-Ended Driving Circuit for SYNC~ and SYSREF

8.3.11 Clock Input

The input clock to the device (referred to as the system clock) goes to an input buffer that automatically configures itself either to accept a single-ended clock or a differential clock. The equivalent load on the clock pins in the case of a differential clock input is shown in Figure 85. For the case of a single-ended clock input, the 5-kΩ resistor is disconnected from the input.

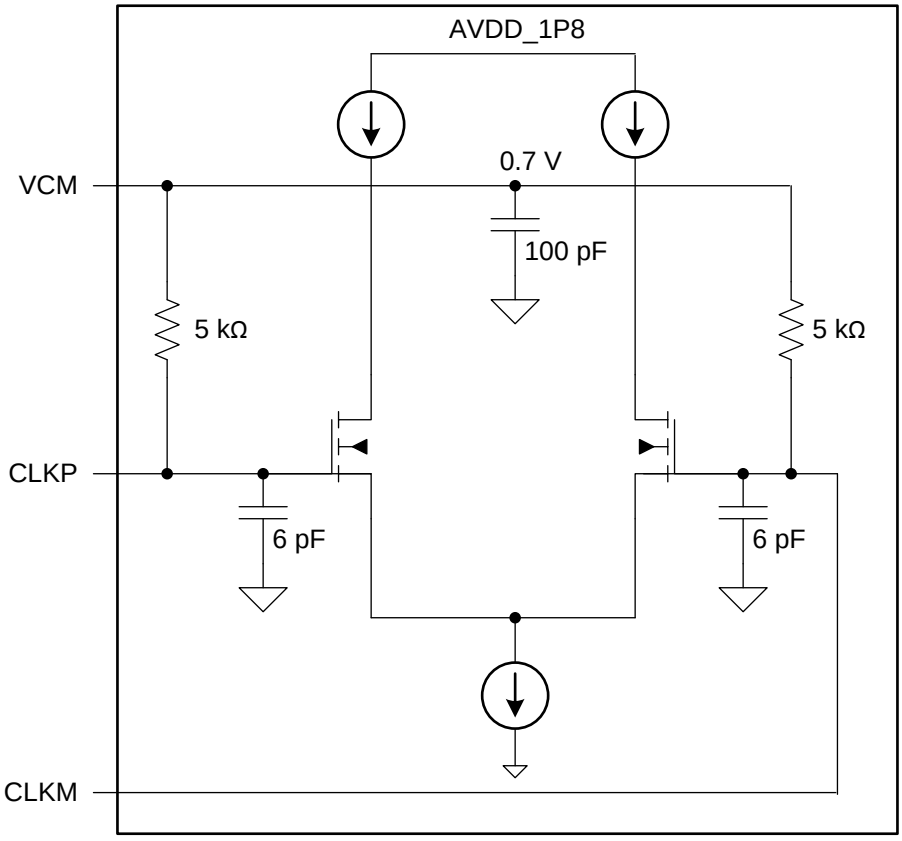


Figure 85. Internal Clock Buffer for Differential Clock Mode

If the preferred clocking scheme for the device is single-ended, connect the CLKM pin to ground (in other words, short CLKM directly to AVSS, as shown in Figure 86). In this case, the auto-detect feature shuts down the internal differential clock buffer and the device automatically goes into a single-ended clock input. Connect the single-ended clock source directly (without decoupling) to the CLKP pin. When using a single-ended clock input, TI recommends using low-jitter, square signals (LVCMOS levels, 1.8-V amplitude) to drive the ADC (refer to technical brief, *Clocking High-Speed Data Converters,* SLYT075 for further details).

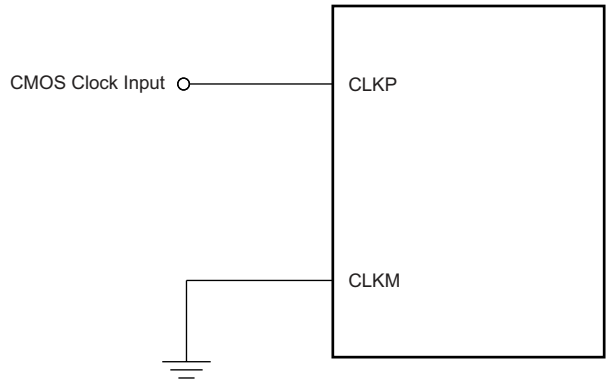


Figure 86. Single-Ended Clock Driving Circuit

For differential clocks (such as differential sine-wave, LVPECL, LVDS, and so forth), enable the clock amplifier with the connection scheme shown in Figure 87. This same scheme applies when the clock is single-ended but the clock amplitude is either small or its edges are not sharp. In this case, connect the input clock signal with a capacitor to CLKP (as in Figure 87) and connect CLKM to ground through a capacitor (that is, ac-coupled to AVSS).

If a transformer is used with the secondary coil floating (for instance, to convert from single-ended to differential), the outputs of the transformer can be connected directly to the clock inputs without requiring the 10-nF series capacitors.

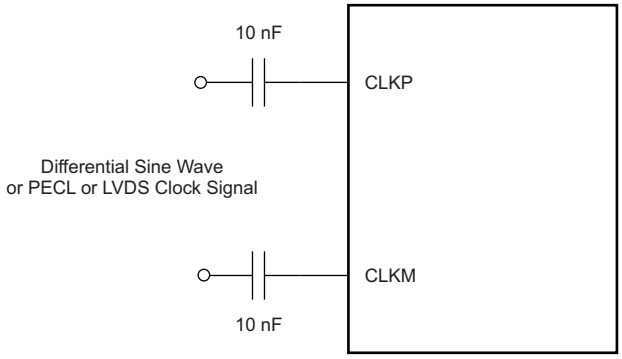


Figure 87. Differential Clock Driving Circuit

To ensure that the aperture delay and jitter are the same for all channels, the device uses a clock tree network to generate individual sampling clocks for each channel. For all channels, the clock is closley matched from the source point to the sampling circuit of each of the eight internal devices.

The jitter cleaners CDCM7005, CDCE72010, or LMK048X series are suitable to generate the system clock and enable high performance. Figure 88 shows a clock distribution network.

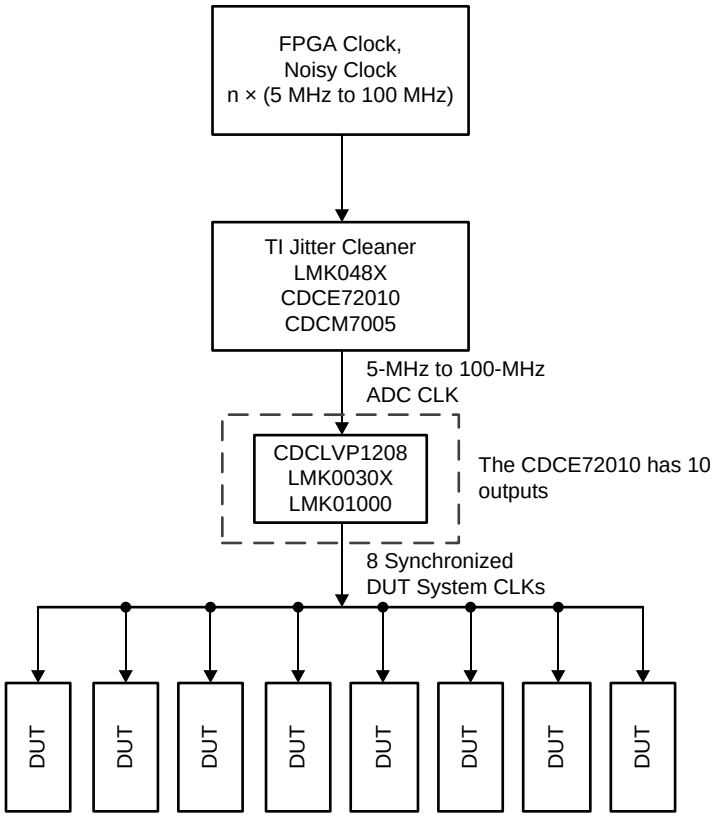


Figure 88. System Clock Distribution Network

8.3.12 Analog Input and Driving Circuit

8.3.12.1 Signal Input

The analog input to the device can be either ac- or dc-coupled. In ac-coupling, the input common-mode required for device functionality can be forced with the common-mode voltage, generated internally by the device (that comes at the VCM pin) through a resistor, as shown in Figure 89. The resistor and capacitor values used for coupling determines the high-pass filter corner of the input circuit; thus, these values are chosen with the frequency of interest in mind.

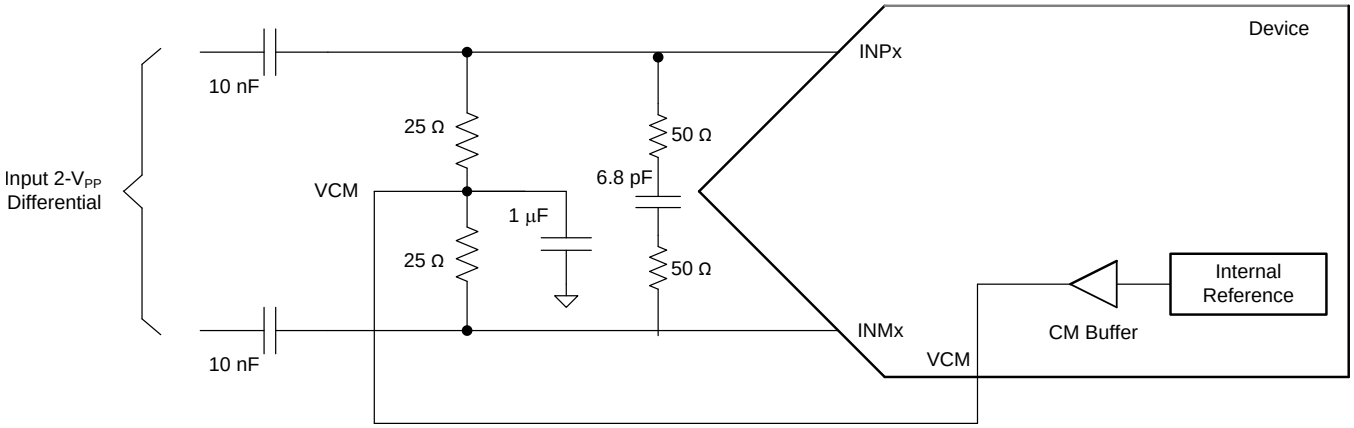


Figure 89. AC Coupling

When dc-coupling the analog input, the output common-mode voltage of the driver can be set using the VCM output pin as a reference, as shown in Figure 90.

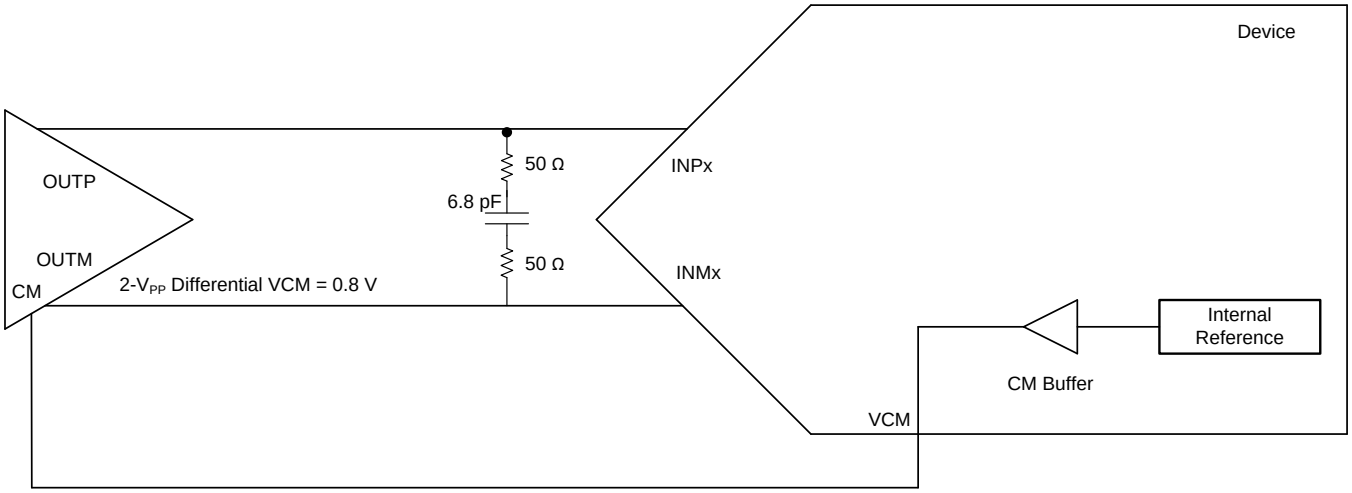


Figure 90. DC Coupling

Each input interfaces to two sets of identical sampling circuits. The electrical model of the load that each of the sampling networks present is illustrated in Figure 91. For the sake of simplification, the MOS switches can be considered as ideal switches.

As illustrated in Figure 57, Figure 58, and Figure 59, the scheme of connecting each input sampling circuit to the input pins differs across the three input modes. The time-dependent loading of the input pins therefore is different across the three input modes, and can be determined by referring to Figure 57, Figure 58, Figure 59, and Figure 91.

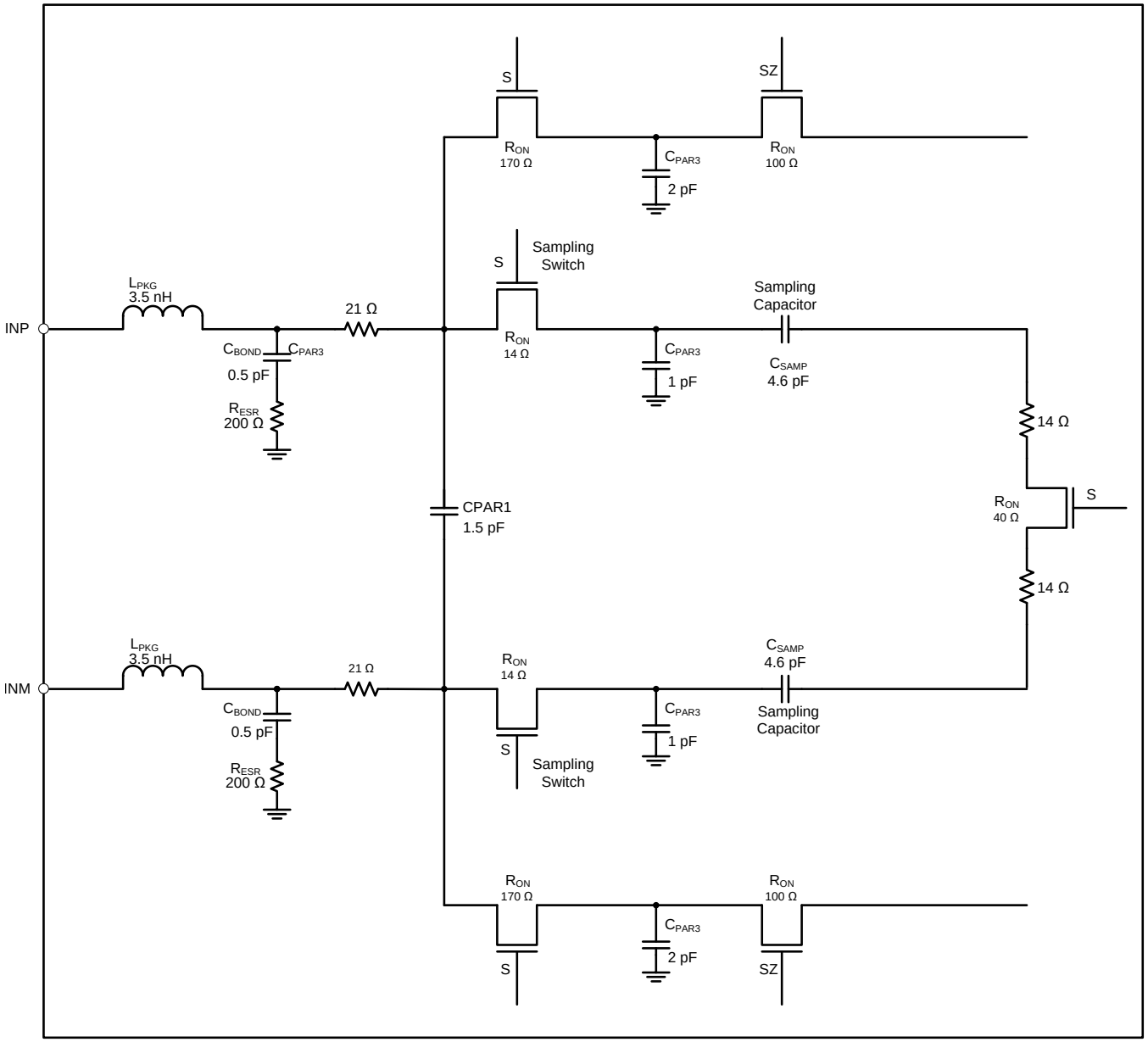


Figure 91. Analog Input Sampling Network

8.4 Device Functional Modes

8.4.1 Input Modes

The device supports three input modes: a 16-input, a 32-input, and an 8-input mode using the SEL_CH[2:0] register controls. See Table 49 for a listing of register bits that select the 8-, 16-, and 32-input modes. Using the same set of 16 ADCs, the three modes can be used to convert 16, 32, or 8 input channels, respectively. The performance of the ADC itself depends on the conversion clock frequency, which has a different relationship to the system clock and sampling rates in each of the three modes. Although the ADCs are common to all three modes, the manner in which the ADCs are used determines unique performance characteristics in each mode. For example, the 8-input mode can have significant interleaving spurs. Additionally, in the 8-input mode, the conversion phases of two adjacent ADCs are offset by one system clock period. The switching operation in one ADC can affect the performance of the adjacent ADC especially at higher input frequencies. For this reason, only 10-bit ADC resolution is supported in the 8-input mode. The restrictions when operating in the different input modes are listed in Table 30.

Table 30. Modes Supported in 8-, 16-, and 32-Input Modes

ANALOG INPUT MODE	ADC RESOLUTIONS SUPPORTED (Bits)	LVDS DATA RATE MODES SUPPORTED
16	10, 12, 14	1X, 2X
32	10, 12, 14	1X
8	10	1X, 2X

8.4.2 ADC Resolution Modes

The ADC resolution can be programmed between 10, 12,and 14 with the ADC_RES register control. The maximum conversion rate of each ADC is determined by the programmed ADC resolution. The restrictions when operating with the different ADC resolutions are listed in Table 31.

Table 31. Modes Supported in the 10-, 12-, and 14-Bit ADC Resolution Modes

ADC RESOLUTION (Bits)	ANALOG INPUT MODES SUPPORTED	MAXIMUM CONVERSION CLOCK (f_C, MHz)
10	16, 8, 32	100
12	16, 32	80
14	16, 32	65

8.4.3 LVDS and JESD Interface Modes

By default, the LVDS interface is enabled. To disable the LVDS interface, set DIS_LVDS to 1.

To enable the JESD204B interface, set EN_JESD to 1. The JESD204B interface is supported only in 16-input and 32-input modes.

8.4.4 LVDS Serialization and Output Data Rate Modes

The serialization factor of the LVDS interface can be set to 10, 12, 14, or 16 using the SER_DATA_RATE register. Additionally, the density of output data payload can be set to 1X or 2X mode by using the LVDS_RATE_2X register bits. The maximum data rate (in bits per sec) of the LVDS interface is limited. Depending on the input mode, serialization factor, and output data rate mode, the LVDS interface speed restriction may impose additional constraints on the maximum sampling rate achievable.

8.4.5 Power Modes

The ADS52J90 can be configured via SPI or pin settings to a global power-down mode and via pin settings to a fast power-down (standby mode). During these two modes (global and standby power-down), different internal functions stay powered up, resulting in different power consumption and wake-up times.

In standby mode, all LVDS data lanes are powered down. The bit clock and frame clock lanes remain enabled to save time to sync again on the receiver side. However, in global power-down mode all lanes are powered down and thus this mode requires more time to wake-up because the bit clock and frame clock lanes must sync again with the receiver device.

The device consists of the following key blocks:

- Band-gap circuit,
- Serial interface,
- Reference voltage and current generator,
- ADC analog block that performs a sampling and conversion,
- ADC digital block that includes all the digital post processing blocks (such as the offset, gain, digital HPF, and so forth),
- LVDS data serializer and buffer that converts the ADC parallel data to a serial stream,
- LVDS frame and clock serializer and buffer, and
- PLL (phase-locked loop) that generates a high-frequency clock for both the ADC and serializer.

Of all these blocks, only the band-gap and serial interface block are not powered down using the power-down pins or bits. Table 32 lists which blocks in the ADC are powered down using different pins and bits.

Table 32. Power-Down Modes Description for the ADC

NAME	TYPE (Pin or Register)	ADC ANALOG	ADC DIGITAL	LVDS DATA SERIALIZER, BUFFER	LVDS FRAME AND CLOCK SERIALIZER, BUFFER	REFERENCE + ADC CLOCK BUFFER	PLL	CHANNEL
PDN_GBL	Pin	Yes(1)	Yes	Yes	Yes	Yes	Yes	All(2)
GLOBAL_PDN	Register	Yes	Yes	Yes	Yes	Yes	Yes	All
PDN_FAST	Pin	Yes	Yes	Yes	No	No	No	All
DIS_LVDS	Register	No	No	Yes	Yes	No	No	All
PDN_ANA_ADCx	Register	Yes	No	No	No	No	No	Individual
PDN_DIG_ADCx	Register	No	Yes	No	No	No	No	Individual
PDN_LVDSx	Register	No	No	Yes	No	No	No	Individual

(1) Yes = powered down. No = active.
(2) All = all channels are powered down. Individual = only a single channel is powered down, depending upon the corresponding bit.

8.4.6 LVDS Test Pattern Mode

The ADC data coming out of the LVDS outputs can be replaced by different kinds of test patterns. Note that the test patterns replace the data streaming out of the ADCs (more specifically, the DIGRES1 signal). Therefore, in 16-, 8-, and 32-channel input modes, the pattern that occurs on a per-channel basis can be different for some test patterns. The different test patterns are described in Table 33.

Table 33. Description of LVDS Test Patterns

TEST PATTERN MODE	PROGRAMMING THE MODE		TEST PATTERNS REPLACE(1)
	THE SAME PATTERN MUST BE COMMON TO ALL DATA LINES	THE PATTERN IS SELECTIVELY REQUIRED ON ONE OR MORE DATA LINE	
All 0s	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	Zeros in all bits (00000000000000) of DIGRESx
All 1s	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	Ones in all bits (11111111111111) of DIGRESx
Deskew	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	DIGRESx word is replaced by alternate 0s and 1s (01010101010101)
Sync	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	DIGRESx word is replaced by half 1s and half 0s (11111110000000)
Custom	Set the mode using PAT_MODES[2:0]. Set the desired custom pattern using the CUSTOM_PATTERN register control.	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	The word written in the CUSTOM_PATTERN control (taken from the MSB side) replaces DIGRESx. (For instance, CUSTOM_PATTERN = 1100101101011100 and DIGRESx = 11001011010111 when the serialization factor is 14.)
Ramp	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	The ADCOUTx word (not the DIGRESx word) is replaced by a word that increments by 1 LSB every conversion clock starting at negative full-scale, increments until positive full-scale, and wraps back to negative full-scale.
Toggle	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	The DIGRESx word alternates between two words that are all 1s and all 0s. At each setting of the toggle pattern, the start word can either be all 0s or all 1s. (Alternate between 11111111111111 and 00000000000000.)
PRBS	Set SEL_PRBS_PAT_GBL = 1. Select either custom or ramp pattern with PAT_MODES[2:0]. Enable PRBS mode using PRBS_EN. Select the desired PRBS mode using PRBS_MODE. Reset the PRBS generator with PRBS_SYNC.	Set PAT_SELECT_IND = 1. Select either custom or ramp pattern with PAT_LVDSx[2:0]. Enable PRBS mode on DOUTx with the PAT_PRBS_LVDSx control. Select the desired PRBS mode using PRBS_MODE. Reset the PRBS generator with PRBS_SYNC.	A 16-bit pattern is generated by a 23-bit (or 9-bit) PRBS pattern generator (taken from the MSB side) and replaces the DIGRESx word.

(1) Shown for a serialization factor of 14.

All patterns listed in Table 33 (except the PRBS pattern) can also be forced on the frame clock output line by using PAT_MODES_FCLK[2:0]. To force a PRBS pattern on the frame clock, use the SEL_PRBS_PAT_FCLK, PRBS_EN, and PAT_MODES_FCLK register controls.

The ramp, toggle, and pseudo-random sequence (PRBS) test patterns can be reset or synchronized by providing a synchronization pulse on the TX_TRIG pin or by setting and resetting a specific register bit.

These test patterns also function as transport layer test patterns for the JESD204B interface.

8.5 Programming

8.5.1 Serial Peripheral Interface (SPI) Operation

This section discusses the read and write operations of the SPI interface.

8.5.1.1 Serial Register Write Description

Several different modes can be programmed with the serial peripheral interface (SPI). This interface is formed by the SEN (serial interface enable), SCLK (serial interface clock), SDIN (serial interface data), and RESET pins. The SCLK, SDIN, and RESET pins have a 20-kΩ pulldown resistor to ground. SEN has a 20-kΩ pullup resistor to supply. Serially shifting bits into the device is enabled when SEN is low. SDIN serial data are latched at every SCLK rising edge when SEN is active (low). SDIN serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse (an internal counter counts the number of 24 clock groups after the SEN falling edge). Data is divided into two main portions: the register address (8 bits) and data (16 bits). Figure 92 shows the timing diagram for serial interface write operation.

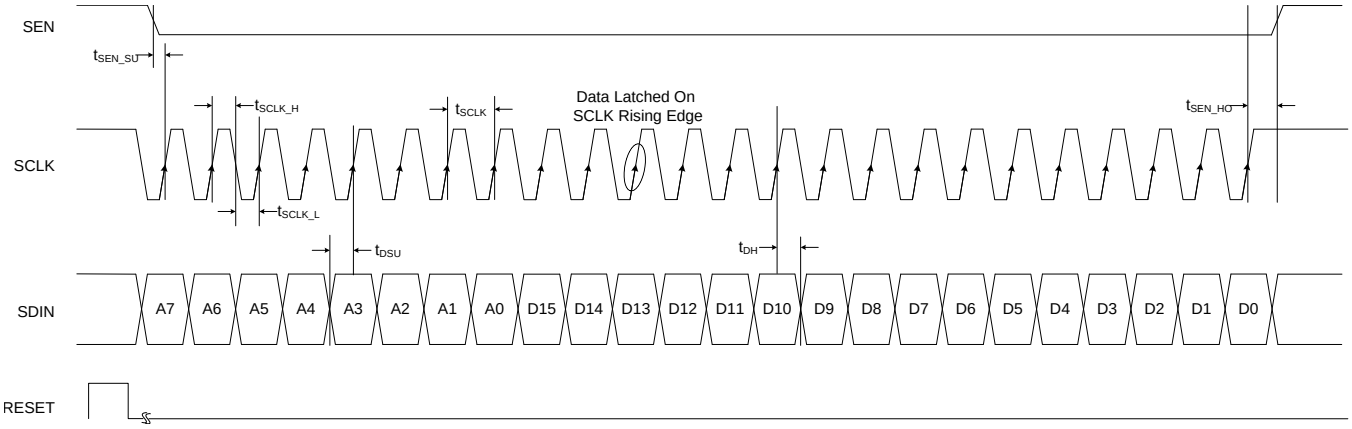


Figure 92. Serial Interface Timing

Programming (continued)

8.5.1.2 Register Readout

The device includes an option where the contents of the internal registers can be read back. This readback can be useful as a diagnostic test to verify the serial interface communication between the external controller and AFE. First, the REG_READ_EN bit must be set to 1. Then, initiate a serial interface cycle specifying the address of the register (A[7:0]) whose content must be read. The data bits are *don't care*. The device outputs the contents (D[15:0]) of the selected register on the SDOUT pin. For lower-speed SCLKs, SDOUT can be latched on the SCLK rising edge. For higher-speed SCLKs, latching SDOUT at the next SCLK falling edge is preferable. The read operation timing diagram is shown in Figure 93. In readout mode, the REG_READ_EN bit can be accessed with SDIN, SCLK, and SEN. To enable serial register writes, set the REG_READ_EN bit back to 0.

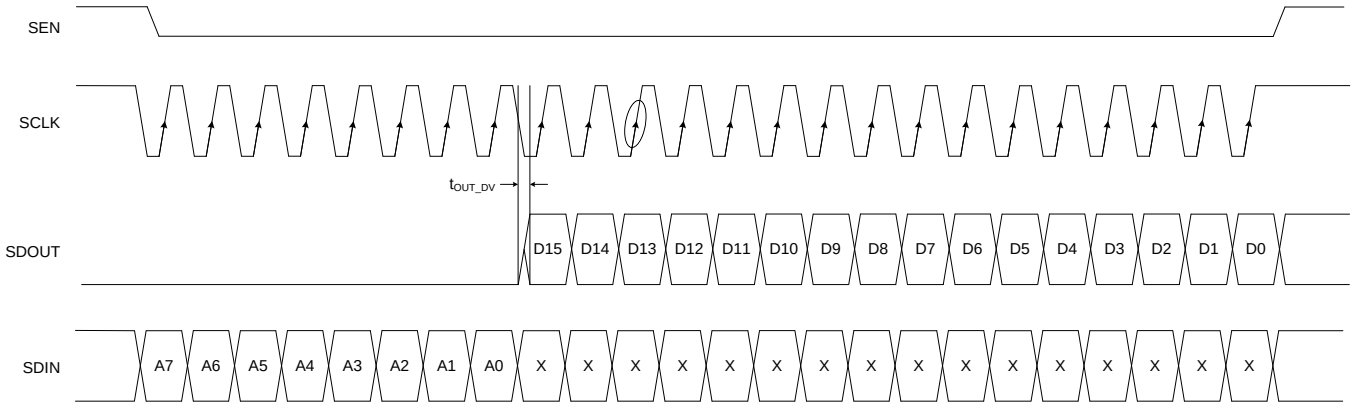


Figure 93. Serial Interface Register, Read Operation

The device SDOUT buffer is 3-stated and is only enabled when the REG_READ_EN bit is enabled. SDOUT pins from multiple devices can therefore be tied together without any pullup resistors. The SN74AUP1T04 level shifter can be used to convert 1.8-V logic to 2.5-V or 3.3-V logic, if necessary.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ADS52J90 supports multiple levels of channel integration (8, 16, and 32) with high sampling rates achievable for each channel. The ADS52J90 also has options to synchronize the clocking and LVDS interface of multiple devices. These features, combined with the excellent ADC performance and low power, make the ADS52J90 an excellent choice for applications involving high channel counts. Such applications include ultrasound imaging systems, sonar imaging equipment, and radar.

9.2 Typical Application

An illustration of a system with a channel count of 64 is shown in Figure 94. In Figure 94, the output interface is selected as the LVDS interface. Four ADS52J90 devices, each operating in 16-input mode, are connected to a single FPGA that aggregates the data from all ADCs for further data processing and storage.

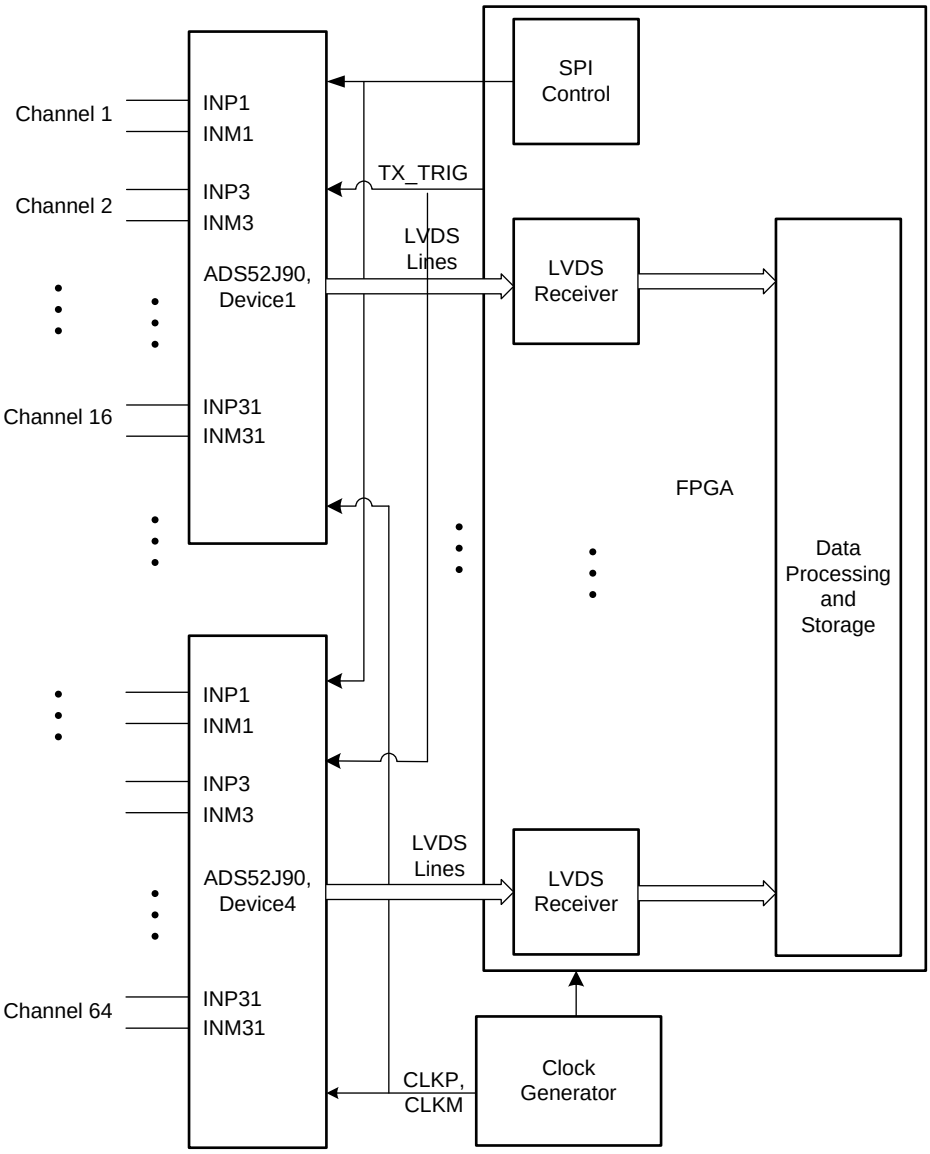


Figure 94. Application Schematic: 64-Channel Medical Ultrasound Receiver Using the ADS52J90

Typical Application (continued)

9.2.1 Design Requirements

Typical requirements of a medical ultrasound receiver system are listed in Table 34.

Table 34. Requirements of a Typical Medical Ultrasound Receiver

DESIGN PARAMETER	EXAMPLE VALUES
Signal center frequency	5 MHz-15 MHz
Signal bandwidth	2 MHz
Maximum input signal amplitude	100 mV_{PP}
Transducer noise level	1 nV/$\sqrt{Hz}$
Total harmonic distortion	40 dBc

The ultrasound system typically has an LNA and a time-dependent gain block at the front-end before the ADC. In an ultrasound receiver, the signal level keeps reducing as a function of time and the role of the front-end blocks is to gain up the signal level without adding too much additional noise. The gain of the front-end can be adjusted so that the input signal to the ADC always remains within its full-scale range.

A sampling rate of approximately 40 MHz to 50 MHz is usually sufficient for such an application. Thus the ADS52J90 can be operated in 16-input mode. Furthermore, the resolution can be set to 14 bits to maximize the SNR of the device. A higher sampling rate ADC results in a lower noise density in the signal band of interest. For example, an ADC with a 2-V_{PP} input operating at 50 MSPS with an SNR of 73 dBFS has a noise level of approximately 35 nV/$\sqrt{Hz}$ referred to the input of the ADC. If the front-end has a gain of 40 dB, the ADC noise referred to the input of the front-end is then 0.35 nV/$\sqrt{Hz}$, which in this case is lower than the transducer noise level.

9.2.2 Detailed Design Procedure

The design considerations when designing with the 16-, 32-, and 8-input modes are described in the following sections.

9.2.2.1 Designing with the 16-Input Mode

Mapping of the analog inputs to the LVDS outputs is shown in Table 35 for a case corresponding to a 16-input mode and a 1X data rate.

Table 35. Mapping of Analog Inputs to LVDS Outputs (16-Input Mode, 1X Data Rate)

ANALOG INPUT SIGNAL	CONNECTION TO ANALOG INPUT PINS	SAMPLING INSTANT	ADC WORD	SERIAL_OUT (Over Two Frames)	LVDS OUTPUTS ON DOUT PINS
AIN1	IN1	t_1	ADCOUT1o	Frame 1: ADCOUT1o Frame 2: ADCOUT1e	DOUT1
		t_2	ADCOUT1e		
AIN2	IN3	t_1	ADCOUT2o	Frame 1: ADCOUT2o Frame 2: ADCOUT2e	DOUT2
		t_2	ADCOUT2e		
AIN3	IN5	t_1	ADCOUT3o	Frame 1: ADCOUT3o Frame 2: ADCOUT3e	DOUT3
		t_2	ADCOUT3e		
AIN4	IN7	t_1	ADCOUT4o	Frame 1: ADCOUT4o Frame 2: ADCOUT4e	DOUT4
		t_2	ADCOUT4e		
AIN5	IN9	t_1	ADCOUT5o	Frame 1: ADCOUT5o Frame 2: ADCOUT5e	DOUT5
		t_2	ADCOUT5e		
AIN6	IN11	t_1	ADCOUT6o	Frame 1: ADCOUT6o Frame 2: ADCOUT6e	DOUT6
		t_2	ADCOUT6e		
AIN7	IN13	t_1	ADCOUT7o	Frame 1: ADCOUT7o Frame 2: ADCOUT7e	DOUT7
		t_2	ADCOUT7e		
AIN8	IN15	t_1	ADCOUT8o	Frame 1: ADCOUT8o Frame 2: ADCOUT8e	DOUT8
		t_2	ADCOUT8e		
AIN9	IN17	t_1	ADCOUT9o	Frame 1: ADCOUT9o Frame 2: ADCOUT9e	DOUT9
		t_2	ADCOUT9e		
AIN10	IN19	t_1	ADCOUT10o	Frame 1: ADCOUT10o Frame 2: ADCOUT10e	DOUT10
		t_2	ADCOUT10e		
AIN11	IN21	t_1	ADCOUT11o	Frame 1: ADCOUT11o Frame 2: ADCOUT11e	DOUT11
		t_2	ADCOUT11e		
AIN12	IN23	t_1	ADCOUT12o	Frame 1: ADCOUT12o Frame 2: ADCOUT12e	DOUT12
		t_2	ADCOUT12e		
AIN13	IN25	t_1	ADCOUT13o	Frame 1: ADCOUT13o Frame 2: ADCOUT13e	DOUT13
		t_2	ADCOUT13e		
AIN14	IN27	t_1	ADCOUT14o	Frame 1: ADCOUT14o Frame 2: ADCOUT14e	DOUT14
		t_2	ADCOUT14e		
AIN15	IN29	t_1	ADCOUT15o	Frame 1: ADCOUT15o Frame 2: ADCOUT15e	DOUT15
		t_2	ADCOUT15e		
AIN16	IN31	t_1	ADCOUT16o	Frame 1: ADCOUT16o Frame 2: ADCOUT16e	DOUT16
		t_2	ADCOUT16e		

Mapping of the analog inputs to the LVDS outputs is shown in Table 36 for a case corresponding to a 16-input mode and a 2X data rate.

Table 36. Mapping of Analog Inputs to LVDS Outputs (16-Input Mode, 2X Data Rate)

ANALOG INPUT SIGNAL	CONNECTION TO ANALOG INPUT PINS	SAMPLING INSTANT	ADC WORD	SERIAL_OUT (Over Two Frames)	LVDS OUTPUTS ON DOUT PINS
AIN1	IN1	t_1	ADCOUT1o	Frame 1: ADCOUT1o, ADCOUT2o Frame 2: ADCOUT1e, ADCOUT2e	DOUT1
		t_2	ADCOUT1e		
AIN2	IN3	t_1	ADCOUT2o		
		t_2	ADCOUT2e		
AIN3	IN5	t_1	ADCOUT3o	Frame 1: ADCOUT3o, ADCOUT4o Frame 2: ADCOUT3e, ADCOUT4e	DOUT2
		t_2	ADCOUT3e		
AIN4	IN7	t_1	ADCOUT4o		
		t_2	ADCOUT4e		
AIN5	IN9	t_1	ADCOUT5o	Frame 1: ADCOUT5o, ADCOUT6o Frame 2: ADCOUT5e, ADCOUT6e	DOUT3
		t_2	ADCOUT5e		
AIN6	IN11	t_1	ADCOUT6o		
		t_2	ADCOUT6e		
AIN7	IN13	t_1	ADCOUT7o	Frame 1: ADCOUT7o, ADCOUT8o Frame 2: ADCOUT7e, ADCOUT8e	DOUT4
		t_2	ADCOUT7e		
AIN8	IN15	t_1	ADCOUT8o		
		t_2	ADCOUT8e		
AIN9	IN17	t_1	ADCOUT9o	Frame 1: ADCOUT9o, ADCOUT10o Frame 2: ADCOUT9e, ADCOUT10e	DOUT9
		t_2	ADCOUT9e		
AIN10	IN19	t_1	ADCOUT10o		
		t_2	ADCOUT10e		
AIN11	IN21	t_1	ADCOUT11o	Frame 1: ADCOUT11o, ADCOUT12o Frame 2: ADCOUT11e, ADCOUT12e	DOUT10
		t_2	ADCOUT11e		
AIN12	IN23	t_1	ADCOUT12o		
		t_2	ADCOUT12e		
AIN13	IN25	t_1	ADCOUT13o	Frame 1: ADCOUT13o, ADCOUT14 Frame 2: ADCOUT13e, ADCOUT14e	DOUT11
		t_2	ADCOUT13e		
AIN14	IN27	t_1	ADCOUT14o		
		t_2	ADCOUT14e		
AIN15	IN29	t_1	ADCOUT15o	Frame 1: ADCOUT15o, ADCOUT16o Frame 2: ADCOUT15e, ADCOUT16e	DOUT12
		t_2	ADCOUT15e		
AIN16	IN31	t_1	ADCOUT16o		
		t_2	ADCOUT16e		

Table 35 and Table 36 illustrate that the ADCs convert the odd numbered input when operating in the 16-input mode. Each ADC can be set to convert the following even numbered input using the register control IN_CH_ADCx. The performance of the ADC may slightly degrade when IN_CH_ADCx is set to 1.

In 16-input mode, there is a one-to-one mapping between the inputs and the ADCs. The register map relative to the ADCs can therefore be mapped to the 16 channels, as shown in Table 37.

Table 37. Reinterpretation of the Register Map in 16-Input Mode

REGISTER MAP NOTATION	MAPPING TO CHANNELS IN 16-INPUT MODE	EXAMPLE
GAIN_ADCxo, GAIN_ADCxe	GAIN_CHANNELx	GAIN_CHANNEL1 = GAIN_ADC1o (same for GAIN_ADC1e) (Set odd and even gains of the same ADC to the same setting)
OFFSET_ADCxo, OFFSET_ADCxe	OFFSET_CHANNELx	OFFSET_CHANNEL1 = OFFSET_ADC1o (same for OFFSET_ADC1e (Set odd and even offsets of the same ADC to the same setting)
PDN_DIG_ADCx	PDN_DIG_CHANNELx	PDN_DIG_CHANNEL1 = PDN_DIG_ADC1
PDN_ANA_ADCx	PDN_ANA_CHANNELx	PDN_ANA_CHANNEL1 = PDN_ANA_ADC1
DIG_HPF_EN_ADCx	Mapped to 4 channels	DIG_HPF_EN_CHANNEL1-4 = DIG_HPF_EN_ADC1-4 Common setting for 4 ADCs maps to common setting for 4 channels
HPF_CORNER_ADCx	Mapped to 4 channels	HPF_CORNER_CHANNEL1-4 = HPF_CORNER_ADC1-4 Common setting for 4 ADCs maps to common setting for 4 channels

9.2.2.2 Designing with the 32-Input Mode

Mapping of the analog inputs to the LVDS outputs is shown in Table 38 for a case corresponding to a 32-input mode and a 1X data rate.

Table 38. Mapping of Analog Inputs to LVDS Outputs (32-Input Mode, 1X Data Rate)

ANALOG INPUT SIGNAL	CONNECTION TO ANALOG INPUT PINS	SAMPLING INSTANT	ADC WORD	SERIAL_OUT (Over One Frame)	LVDS OUTPUTS ON DOUT PINS
AIN1	IN1	t_1	ADCOUT1o	ADCOUT1o, ADCOUT1e	DOUT1
AIN2	IN2	t_2	ADCOUT1e		
AIN3	IN3	t_1	ADCOUT2o	ADCOUT2o, ADCOUT2e	DOUT2
AIN4	IN4	t_2	ADCOUT2e		
AIN5	IN5	t_1	ADCOUT3o	ADCOUT3o, ADCOUT3e	DOUT3
AIN6	IN6	t_2	ADCOUT3e		
AIN7	IN7	t_1	ADCOUT4o	ADCOUT4o, ADCOUT4e	DOUT4
AIN8	IN8	t_2	ADCOUT4e		
AIN9	IN9	t_1	ADCOUT5o	ADCOUT5o, ADCOUT5e	DOUT5
AIN10	IN10	t_2	ADCOUT5e		
AIN11	IN11	t_1	ADCOUT6o	ADCOUT6o, ADCOUT6e	DOUT6
AIN12	IN12	t_2	ADCOUT6e		
AIN13	IN13	t_1	ADCOUT7o	ADCOUT7o, ADCOUT7e	DOUT7
AIN14	IN14	t_2	ADCOUT7e		
AIN15	IN15	t_1	ADCOUT8o	ADCOUT8o, ADCOUT8e	DOUT8
AIN16	IN16	t_2	ADCOUT8e		
AIN17	IN17	t_1	ADCOUT9o	ADCOUT9o, ADCOUT9e	DOUT9
AIN18	IN18	t_2	ADCOUT9e		
AIN19	IN19	t_1	ADCOUT10o	ADCOUT10o, ADCOUT10e	DOUT10
AIN20	IN20	t_2	ADCOUT10e		
AIN21	IN21	t_1	ADCOUT11o	ADCOUT11o, ADCOUT11e	DOUT11
AIN22	IN22	t_2	ADCOUT11e		
AIN23	IN23	t_1	ADCOUT12o	ADCOUT12o, ADCOUT12e	DOUT12
AIN24	IN24	t_2	ADCOUT12e		
AIN25	IN25	t_1	ADCOUT13o	ADCOUT13o, ADCOUT13e	DOUT13
AIN26	IN26	t_2	ADCOUT13e		

Table 38. Mapping of Analog Inputs to LVDS Outputs (32-Input Mode, 1X Data Rate) (continued)

ANALOG INPUT SIGNAL	CONNECTION TO ANALOG INPUT PINS	SAMPLING INSTANT	ADC WORD	SERIAL_OUT (Over One Frame)	LVDS OUTPUTS ON DOUT PINS
AIN27	IN27	t_1	ADCOUT14o	ADCOUT14o, ADCOUT14e	DOUT14
AIN28	IN28	t_2	ADCOUT14e		
AIN29	IN29	t_1	ADCOUT15o	ADCOUT15o, ADCOUT15e	DOUT15
AIN30	IN30	t_2	ADCOUT15e		
AIN31	IN31	t_1	ADCOUT16o	ADCOUT16o, ADCOUT16e	DOUT16
AIN32	IN32	t_2	ADCOUT16e		

Note that 2X data rate mode is not supported in 32-input mode. In 32-input mode, only one ADC is used to convert two inputs.

The odd numbered inputs correspond to the odd sample from the ADC, and the even numbered inputs correspond to the even sample from the ADC. The register map relative to the ADCs can therefore be mapped to the 32 channels, as shown in Table 39.

Table 39. Reinterpretation of Register Map in 32-Input Mode

REGISTER MAP NOTATION	MAPPING TO CHANNELS IN 16-INPUT MODE	EXAMPLE
GAIN_ADCxo	GAIN_CHANNEL (odd)	GAIN_CHANNEL1 = GAIN_ADC1o
GAIN_ADCxe	GAIN_CHANNEL (even)	GAIN_CHANNEL2 = GAIN_ADC1e
OFFSET_ADCXo	OFFSET_CHANNEL (odd)	OFFSET_CHANNEL1 = OFFSET_ADC1o
OFFSET_ADCxe	OFFSET_CHANNEL (even)	OFFSET_CHANNEL2 = OFFSET_ADC1e
PDN_DIG_ADCx	PDN_DIG_CHANNEL (odd and even)	PDN_DIG_CHANNEL1 = PDN_DIG_CHANNEL2 = PDN_DIG_ADC1
PDN_ANA_ADCx	PDN_ANA_CHANNEL (odd and even)	PDN_ANA_CHANNEL1 = PDN_ANA_CHANNEL2 = PDN_ANA_ADC1
DIG_HPF_EN_ADCx	Mapped to 8 channels	DIG_HPF_EN_CHANNEL1-8 = DIG_HPF_EN_ADC1-4 Common setting for 4 ADCs mapped to common setting for 8 channels
HPF_CORNER_ADCx	Mapped to 8 channels	HPF_CORNER_CHANNEL1-8 = HPF_CORNER_ADC1-4 Common setting for 4 ADCs mapped to common setting for 8 channels

9.2.2.3 Designing with the 8-Input Mode

Mapping of the analog inputs to the LVDS outputs is shown in Table 40 for a case corresponding to an 8-input mode and a 1X data rate.

Table 40. Mapping of Analog Inputs to LVDS Outputs (8-Input Mode, 1X Data Rate)

ANALOG INPUT SIGNAL	CONNECTION TO ANALOG INPUT PINS	SAMPLING INSTANT	ADC WORD	SERIAL_OUT (Over Two Frames)	LVDS OUTPUTS ON DOUT PINS
AIN1	IN1, IN3 (shorted externally)	t_1	ADCOUT1o	Frame 1: ADCOUT1o Frame 2: ADCOUT1e	DOUT1
		t_2	ADCOUT2o		
		t_3	ADCOUT1e	Frame 1: ADCOUT2o Frame 2: ADCOUT2e	DOUT2
		t_4	ADCOUT2e		
AIN2	IN5, IN7 (shorted externally)	t_1	ADCOUT3o	Frame 1: ADCOUT3o Frame 2: ADCOUT3e	DOUT3
		t_2	ADCOUT4o		
		t_3	ADCOUT3e	Frame 1: ADCOUT4o Frame 2: ADCOUT4e	DOUT4
		t_4	ADCOUT4e		
AIN3	IN9, IN11 (shorted externally)	t_1	ADCOUT5o	Frame 1: ADCOUT5o Frame 2: ADCOUT5e	DOUT5
		t_2	ADCOUT6o		
		t_3	ADCOUT5e	Frame 1: ADCOUT6o Frame 2: ADCOUT6e	DOUT6
		t_4	ADCOUT6e		
AIN4	IN13, IN15 (shorted externally)	t_1	ADCOUT7o	Frame 1: ADCOUT7o Frame 2: ADCOUT7e	DOUT7
		t_2	ADCOUT8o		
		t_3	ADCOUT7e	Frame 1: ADCOUT8o Frame 2: ADCOUT8e	DOUT8
		t_4	ADCOUT8e		
AIN5	IN17, IN19 (shorted externally)	t_1	ADCOUT9o	Frame 1: ADCOUT9o Frame 2: ADCOUT9e	DOUT9
		t_2	ADCOUT10o		
		t_3	ADCOUT9e	Frame 1: ADCOUT10o Frame 2: ADCOUT10e	DOUT10
		t_4	ADCOUT10e		
AIN6	IN21, IN23 (shorted externally)	t_1	ADCOUT11o	Frame 1: ADCOUT11o Frame 2: ADCOUT11e	DOUT11
		t_2	ADCOUT12o		
		t_3	ADCOUT11e	Frame 1: ADCOUT12o Frame 2: ADCOUT12e	DOUT12
		t_4	ADCOUT12e		
AIN7	IN25, IN27 (shorted externally)	t_1	ADCOUT13o	Frame 1: ADCOUT13o Frame 2: ADCOUT13e	DOUT13
		t_2	ADCOUT14o		
		t_3	ADCOUT13e	Frame 1: ADCOUT14o Frame 2: ADCOUT14e	DOUT14
		t_4	ADCOUT14e		
AIN8	IN29, IN31 (shorted externally)	t_1	ADCOUT15o	Frame 1: ADCOUT15o Frame 2: ADCOUT15e	DOUT15
		t_2	ADCOUT16o		
		t_3	ADCOUT15e	Frame 1: ADCOUT16o Frame 2: ADCOUT16e	DOUT16
		t_4	ADCOUT16e		

Mapping of the analog inputs to the LVDS outputs is shown in Table 41 for a case corresponding to an 8-input mode and a 2X data rate.

Table 41. Mapping of Analog Inputs to LVDS Outputs (8-Input Mode, 2X Data Rate)

ANALOG INPUT SIGNAL	CONNECTION TO ANALOG INPUT PINS	SAMPLING INSTANT	ADC WORD	SERIAL_OUT (Over Two Frames)	LVDS OUTPUTS ON DOUT PINS
AIN1	IN1, IN3 (shorted externally)	t_1	ADCOUT1o	Frame 1: ADCOUT1o, ADCOUT2o	DOUT1
		t_2	ADCOUT2o		
		t_3	ADCOUT1e	Frame 2: ADCOUT1e, ADCOUT2e	
		t_4	ADCOUT2e		
AIN2	IN5, IN7 (shorted externally)	t_1	ADCOUT3o	Frame 1: ADCOUT3o, ADCOUT4o	DOUT2
		t_2	ADCOUT4o		
		t_3	ADCOUT3e	Frame 2: ADCOUT3e, ADCOUT4e	
		t_4	ADCOUT4e		
AIN3	IN9, IN11 (shorted externally)	t_1	ADCOUT5o	Frame 1: ADCOUT5o, ADCOUT6o	DOUT3
		t_2	ADCOUT6o		
		t_3	ADCOUT5e	Frame 2: ADCOUT5e, ADCOUT6e	
		t_4	ADCOUT6e		
AIN4	IN13, IN15 (shorted externally)	t_1	ADCOUT7o	Frame 1: ADCOUT7o, ADCOUT8o	DOUT4
		t_2	ADCOUT8o		
		t_3	ADCOUT7e	Frame 2: ADCOUT7e, ADCOUT8e	
		t_4	ADCOUT8e		
AIN5	IN17, IN19 (shorted externally)	t_1	ADCOUT9o	Frame 1: ADCOUT9o, ADCOUT10o	DOUT9
		t_2	ADCOUT10o		
		t_3	ADCOUT9e	Frame 2: ADCOUT9e, ADCOUT10e	
		t_4	ADCOUT10e		
AIN6	IN21, IN23 (shorted externally)	t_1	ADCOUT11o	Frame 1: ADCOUT11o, ADCOUT12o	DOUT10
		t_2	ADCOUT12o		
		t_3	ADCOUT11e	Frame 2: ADCOUT11e, ADCOUT12e	
		t_4	ADCOUT12e		
AIN7	IN25, IN27 (shorted externally)	t_1	ADCOUT13o	Frame 1: ADCOUT13o, ADCOUT14	DOUT11
		t_2	ADCOUT14o		
		t_3	ADCOUT13e	Frame 2: ADCOUT13e, ADCOUT14e	
		t_4	ADCOUT14e		
AIN8	IN29, IN31 (shorted externally)	t_1	ADCOUT15o	Frame 1: ADCOUT15o, ADCOUT16o	DOUT12
		t_2	ADCOUT16o		
		t_3	ADCOUT15e	Frame 2: ADCOUT15e, ADCOUT16e	
		t_4	ADCOUT16e		

In 8-input mode, two neighboring ADCs are used to convert a single input. The register map relative to the ADCs can be mapped to the eight channels, as shown in Table 42.

Table 42. Reinterpretation of Register Map in 8-input Mode

REGISTER MAP NOTATION	MAPPING TO CHANNELS IN 16-INPUT MODE	EXAMPLE
GAIN_ADCxo, GAIN_ADCxe of two adjacent channels	GAIN_CHANNELx	GAIN_CHANNEL1 = GAIN_ADC1o (same for GAIN_ADC1e, GAIN_ADC2o, and GAIN_ADC2e) Set odd and even gains of two adjacent ADCs to the same setting.
OFFSET_ADCxo, OFFSET_ADCxe	OFFSET_CHANNELx	OFFSET_CHANNEL1 = OFFSET_ADC1o (same for OFFSET_ADC1e, OFFSET_ADC2o, and OFFSET_ADC2e) Set odd and even offsets of two adjacent ADCs to the same setting.
PDN_DIG_ADCx of two adjacent channels	PDN_DIG_CHANNELx	PDN_DIG_CHANNEL1 = PDN_DIG_ADC1 (same for PDN_DIG_ADC2) Set the power-down for two adjacent ADCs to the same setting.
PDN_ANA_ADCx of two adjacent channels	PDN_ANA_CHANNELx	PDN_ANA_CHANNEL1 = PDN_ANA_ADC1 (same for PDN_ANA_ADC2) Set the power-down for two adjacent ADCs to the same setting.
DIG_HPF_EN_ADCx	Mapped to 2 channels	DIG_HPF_EN_CHANNEL1-2 = DIG_HPF_EN_ADC1-4 Common setting for 4 ADCs mapped to the common setting for 2 channels.
HPF_CORNER_ADCx	Mapped to 2 channels	HPF_CORNER_CHANNEL1-2 = HPF_CORNER_ADC1-4 Common setting for 4 ADCs mapped to the common setting for 2 channels.

9.2.3 Application Curves

This section outlines the trends described in the *Typical Characteristics* section from an application perspective.

Figure 2 illustrates the FFT with a 5-MHz input signal for 32-input mode with the ADC resolution set to 10 bits. The system clock provided is 100 MSPS and the input is sampled at an effective rate of 50 MSPS, which is the maximum sampling rate for this mode of operation.

Figure 3 illustrates the FFT with a 5-MHz input signal for 16-input mode with the ADC resolution set to 10 bits. The system clock provided is 100 MSPS and the input is sampled at an effective rate of 100 MSPS, which is the maximum sampling rate for this mode of operation.

Figure 4 illustrates the FFT with a 5-MHz input signal for 8-input mode with the ADC resolution set to 10 bits. The system clock provided is 200 MSPS and the input is sampled at an effective rate of 200 MSPS, which is the maximum sampling rate for this mode of operation. The increase in sampling rate is achieved through two ADCs converting the same input in an interleaved manner. The interleaving spurs are visible in the FFT. The predominant spur is at the frequencies of (f_S / 2 ± f_{IN}), which appear at 95 MHz. Additional spurs are at the frequencies of (f_S / 4 ± f_{IN}), which appear at 45 MHz and 55 MHz. The magnitude of the spurs is expected to rise when the input frequency is increased. Also, the spur level is sensitive to the matching of the manner in which the two sets of input pins are driven. A spur at f_S/4 is also seen. This arises from the offset mismatch between the four sets of sampling circuits used to sample the same input.

Figure 5 illustrates the FFT with a 5-MHz input signal for 32-input mode with the ADC resolution set to 12 bits. The system clock provided is 80 MSPS and the input is sampled at an effective rate of 40 MSPS, which is the maximum sampling rate for this mode of operation.

Figure 6 illustrates the FFT with a 5-MHz input signal for 16-input mode with the ADC resolution set to 12 bits. The system clock provided is 80 MSPS and the input is sampled at an effective rate of 80 MSPS, which is the maximum sampling rate for this mode of operation.

Figure 7 illustrates the FFT with a 5-MHz input signal for 32-input mode with the ADC resolution set to 14 bits. The system clock provided is 65 MSPS and the input is sampled at an effective rate of 32.5 MSPS, which is the maximum sampling rate for this mode of operation.

Figure 8 illustrates the FFT with a 5-MHz input signal for 16-input mode with the ADC resolution set to 14 bits. The system clock provided is 65 MSPS and the input is sampled at an effective rate of 65 MSPS, which is the maximum sampling rate for this mode of operation. In addition to the harmonics, the spur at the frequency (f_S / 2 ± f_{IN}) also occurs at 27.5 MHz. This spur is caused by the interleaved sampling of the input signal by two physically different sampling circuits of the same ADC.

Figure 9 illustrates the signal-to-noise ratio (SNR) versus the frequency of the input signal for 32-input mode with the ADC resolution set to 10 bits. SNR is expressed in the dBFS scale where the RMS noise at the ADC output is referred to the full-scale differential voltage of 2 V. The system clock provided is 100 MSPS and the input is sampled at an effective rate of 50 MSPS. SNR is computed by integrating the noise in all FFT bins after excluding the first nine harmonics. SNR is dominated by the quantization noise of the 10-bit conversion.

Figure 10 illustrates SNR versus the frequency of the input signal for 16-input mode with the ADC resolution set to 10 bits. The system clock provided is 100 MSPS and the input is sampled at an effective rate of 100 MSPS. SNR is computed by integrating the noise in all FFT bins after excluding the first nine harmonics and any interleaving spurs. SNR is dominated by the quantization noise of the 10-bit conversion.

Figure 11 illustrates SNR versus the frequency of the input signal for 8-input mode with the ADC resolution set to 10 bits. The system clock provided is 200 MSPS and the input is sampled at an effective rate of 200 MSPS. SNR is computed by integrating the noise in all FFT bins after excluding the first nine harmonics and any interleaving spurs at (f_S / 2 ± f_{IN}) and (f_S / 4 ± f_{IN}) as well as additional spurs at f_S / 2 and f_S / 4. SNR is dominated by the quantization noise of the 10-bit conversion.

Figure 12 illustrates SNR versus the frequency of the input signal for 32-input mode with the ADC resolution set to 12 bits. The system clock provided is 80 MSPS and the input is sampled at an effective rate of 40 MSPS.

Figure 13 illustrates SNR versus the frequency of the input signal for 16-input mode with the ADC resolution set to 12 bits. The system clock provided is 80 MSPS and the input is sampled at an effective rate of 80 MSPS.

Figure 14 illustrates SNR versus the frequency of the input signal for 32-input mode with the ADC resolution set to 14 bits. The system clock provided is 65 MSPS and the input is sampled at an effective rate of 32.5 MSPS. SNR at high input frequencies degrades because of clock jitter.

Figure 15 illustrates SNR versus the frequency of the input signal for 16-input mode with the ADC resolution set to 14 bits. The system clock provided is 65 MSPS and the input is sampled at an effective rate of 65 MSPS.

Figure 16 illustrates the amplitude of the third-order harmonic distortion (HD3) of the input signal versus the frequency of the input signal. The unit of dBc indicates that the HD3 amplitude is referred to the amplitude of the input signal, which is set to –1 dBFS. Figure 16 is taken for 32-input mode with the ADC resolution set to 10 bits. The system clock provided is 100 MSPS and the input is sampled at an effective rate of 50 MSPS. The device follows a similar trend across the other input modes and resolutions.

Figure 17 illustrates the amplitude of the second-order harmonic distortion (HD2) of the input signal versus the frequency of the input signal. The unit of dBc indicates that the HD2 amplitude is referred to the amplitude of the input signal, which is set to –1 dBFS. Figure 17 is taken for 32-input mode with the ADC resolution set to 10 bits. The system clock provided is 100 MSPS and the input is sampled at an effective rate of 50 MSPS. The device follows a similar trend across the other input modes and resolutions.

Figure 18 illustrates the total harmonic distortion (THD) versus the frequency of the input signal. The THD parameter includes the RMS amplitude of the first nine harmonics of the fundamental signal. The unit of dBc indicates that THD is referred to the amplitude of the input signal, which is set to –1 dBFS. Figure 18 is taken for 32-input mode with the ADC resolution set to 10 bits. The system clock provided is 100 MSPS and the input is sampled at an effective rate of 50 MSPS. The device follows a similar trend across the other input modes and resolutions.

Figure 19 illustrates the interleaving spur at (f_S / 2 ± f_{IN}) versus the frequency of the input signal. Figure 19 is taken for 8-input mode with the ADC resolution set to 10 bits. The system clock is set to 200 MSPS and the input is sampled at an effective rate of 200 MSPS. The interleaving spur at (f_S / 2 ± f_{IN}) is referred to the fundamental amplitude, which is at a level of –1 dBFS. The (f_S / 2 ± f_{IN}) spur comes about because of the interleaved conversion of the same input by two ADCs. As illustrated in Figure 19, the interleaving spur gets much worse at higher input frequencies. This degradation results from the fact that when the input frequency is increased, any mismatch in the sampling bandwidths and sampling instants of the two interleaved ADCs leads to a larger phase error between the interleaved conversions.

Figure 20 illustrates the interleaving spur at (f_S / 2 ± f_{IN}) versus the frequency of the input signal. Figure 20 is taken for 16-input mode with the ADC resolution set to 10 bits. The system clock is set to 100 MSPS and the input is sampled at an effective rate of 100 MSPS. The (f_S / 2 ± f_{IN}) spur comes about because of the interleaved sampling of the input by the two sampling circuits of one ADC. Although not as bad as the (f_S / 2 ± f_{IN}) spur for 8-input mode, the interleaving spur could still be the dominant factor governing the SFDR at high input frequencies.

Figure 21 illustrates the interleaving spur at (f_S / 4 ± f_{IN}) versus the frequency of the input signal. Figure 21 is taken for 8-input mode with the ADC resolution set to 10 bits. The system clock is set to 200 MSPS and the input is sampled at an effective rate of 200 MSPS. In 8-input mode, there are a total of four sampling circuits (two in each ADC) that sample the same input in sequence. The (f_S / 4 ± f_{IN}) spur comes about from mismatches between these four sampling circuits.

Figure 22 illustrates SNR in dBFS as a function of the input amplitude, also expressed in dBFS. SNR excludes the first nine harmonics and the interleaving spurs. Figure 22 is taken for the 16-input mode with the ADC resolution set to 14 bits. The system clock is set to 65 MSPS and the input is sampled at an effective rate of 65 MSPS. The points in the left extreme of the curve provide an estimate of the idle channel SNR (SNR in the absence of an input signal).

Figure 23 illustrates the spurious-free dynamic range (SFDR) as a function of the input amplitude. Figure 23 is taken for 32-input mode with the ADC resolution set to 14 bits. In 32-input mode, there is no interleaved operation of any sort and SFDR is a true measure of ADC conversion performance. As mentioned previously, SFDR may be dominated by interleaving spurs (and significantly lower than 32-input mode) when operated in 16-input or 8-input modes. SFDR is plotted in both dBc and dBFS: the former referring the amplitude of the worst-spur to the fundamental amplitude and the latter to the full-scale voltage.

Figure 24 illustrates SNR as a function of the input common-mode voltage (average of INP and INM). Figure 24 is taken for 16-input mode with the ADC resolution set to 14 bits. The device is meant to be operated at an input common-mode that is tightly controlled around the ideal value of 0.8 V. The driving circuit can generate its output common-mode using the 0.8-V reference voltage provided at the VCM pin.

Figure 25 illustrates SNR as a function of the input clock amplitude (expressed in differential V_{PP}) when driven with a differential sine-wave clock input. At small input amplitudes, the sine-wave clock has a low dV/dt slope at the zero crossings. This low slope can cause increased jitter in the clocking and can lead to a reduction in the SNR within the device. The effect is more pronounced when the input frequency is set to a higher value (as is evidenced by the difference in behavior between the 5-MHz and 50-MHz inputs). The recommended manner to drive the device is with an LVPECL clock.

Figure 26 illustrates SNR as a function of the duty cycle of a differential clock input. Ideally, the device is driven with a 50% clock; see the *Electrical Characteristics* table for the acceptable variation around 50% duty cycle.

Figure 27 illustrates the channel-to-channel crosstalk as a function of the analog input frequency. An analog input of a –1-dBFS amplitude is applied on one channel and the crosstalk spur (at the input frequency) is measured on all channels. The worst of the crosstalk numbers (usually on the physically closest channel) is plotted.

Figure 28 illustrates the integral nonlinearity (INL) versus ADC code. The device is operated in 32-input mode at 14-bit resolution with an effective sampling rate of 32.5 MSPS. Figure 28 provides an accurate INL estimate of the ADC inside the device because there is no interleaving of any kind in the 32-input mode operation.

Figure 29 illustrates the differential nonlinearity (DNL) versus ADC code. The device is operated in 32-input mode at 14-bit resolution with an effective sampling rate of 32.5 MSPS. The saturation of the DNL on the lower side to –1 indicates missing codes at the 14-bit level.

Figure 30 illustrates the power-supply rejection ratio (PSRR) as a function of the tone frequency applied on the supply. A tone is applied on the supplies and the tone at the same frequency is measured at the device output. The unit of dBc refers to the relation of the amplitude of the output tone to the amplitude of the supply tone that is set to 100 mV_{PP} for this measurement.

Figure 31 illustrates the power-supply modulation ratio (PSMR) as a function of the tone frequency applied on the supply. A –1-dBFS input at 5 MHz is applied on the analog input. Simultaneously, a 100-mV_{PP} tone is applied on the supply. The tone caused by the intermodulation between the supply tone and the input tone is measured at the device output. PSMR refers to the intermodulation tone referred to in terms of dBc to the amplitude of the input tone.

Figure 32 illustrates the common-mode rejection ratio (CMRR) as a function of the tone frequency applied as a common-mode signal on the input pins. A 50-mV_{PP} common-mode signal is applied to INP and INM around the ideal common-mode voltage of 0.8 V. The amplitude of the tone at the same frequency is measured at the device output. CMRR refers to the amplitude of this output tone referred to in terms of dBc to the amplitude of the common-mode input tone.

Figure 33 illustrates the current of the AVDD_1P8 supply as a function of f_C, the conversion clock frequency. The relation of the sampling rate to the conversion clock frequency is different between the 16-, 32-, and 8- input modes and therefore the curve can be appropriately interpreted for each mode. The curve extends to a conversion clock frequency of up to 100 MSPS, which is the maximum value for the 10-bit ADC resolution. For the 12- and 14-bit ADC resolutions, sections of the same curve up to 80 MSPS and 65 MSPS (respectively) are applicable.

Figure 34 illustrates the current of the DVDD_1P8 supply as a function of the conversion clock frequency. All 16 LVDS buffers are on during this measurement.

Figure 35 illustrates the current of the DVDD_1P2 supply as a function of the conversion clock frequency.

Figure 36 illustrates the total power consumption as a function of the conversion clock frequency. The power per input channel can be calculated by dividing this total power by 8, 16, or 32 for the 8-, 16-, or 32-input modes.

Figure 37 illustrates the digital high-pass filter response for different settings of the HPF corner frequency.

Figure 38 illustrates the typical minimum and maximum SNR values taken across 100 devices operating in the 14-bit, 32-input mode at f_C = 65 MSPS (corresponding to f_{SAMP} = 32.5 MSPS). A trend can be observed across channels and originates from the physical placement and routing of common signals (such as reference voltage and power) to the channels. Depending on the way the channel data are combined, an averaging effect can result when the system-level SNR is computed.

Figure 39 illustrates a plot of the low-frequency noise from the device with and without the chopper enabled. When the chopper is enabled (using the CHOPPER_EN register control), the low-frequency noise generated inside the device is shifted to approximately f_S / 2. Chopper mode is useful when the signal frequency of interest is close to dc.

Figure 48 illustrates a contour plot of SNR as a function of both the input frequency and sampling frequency for 32-input mode operating with a 10-bit ADC resolution.

Figure 49 illustrates a contour plot of SNR as a function of both the input frequency and sampling frequency for 16-input mode operating with a 10-bit ADC resolution.

Figure 50 illustrates a contour plot of SNR as a function of both the input frequency and sampling frequency for 8-input mode operating with a 10-bit ADC resolution.

Figure 51 illustrates a contour plot of SNR as a function of both the input frequency and sampling frequency for 32-input mode operating with a 12-bit ADC resolution.

Figure 52 illustrates a contour plot of SNR as a function of both the input frequency and sampling frequency for 16-input mode operating with a 12-bit ADC resolution.

Figure 53 illustrates a contour plot of SNR as a function of both the input frequency and sampling frequency for 32-input mode operating with a 14-bit ADC resolution.

Figure 54 illustrates a contour plot of SNR as a function of both the input frequency and sampling frequency for 16-input mode operating with a 14-bit ADC resolution.

9.3 Do's and Don'ts

Driving the inputs (analog or digital) beyond the power-supply rails. For device reliability, an input must not go more than 300 mV below the ground pins or 300 mV above the supply pins. Exceeding these limits, even on a transient basis, can cause faulty or erratic operation and can impair device reliability.

Driving the device signal input with an excessively high level signal. The device offers consistent and fast overload recovery for an overload of upto 6 dBFS. For very large overload signals (> 6 dB of the linear input signal range), TI recommends back-to-back Schottky clamping diodes at the input to limit the amplitude of the input signal.

Using a clock source with excessive jitter, an excessively long input clock signal trace, or having other signals coupled to the ADC clock signal trace. These situations cause the sampling instant vary, causing an excessive output noise and a reduction in SNR performance. For a system with multiple devices, the clock tree scheme must be used to apply an ADC clock. Excessive clock delay mismatch between devices can also lead to latency mismatch and functional failure at the system level.

LVDS routing length mismatch. The routing length of all LVDS lines routing to the FPGA must be matched to avoid any timing-related issues. For systems with multiple devices, the LVDS serialized data clock (DCLKP, DCLKM) and the frame clock (FCLKP, FCLKM) of each individual device must be used to deserialize the corresponding LDVS serialized data (DOUTP, DOUTM).

Failure to provide adequate heat removal. Use the appropriate thermal parameter listed in the *Thermal Information* table and an ambient, board, or case temperature in order to calculate device junction temperature. A suitable heat removal technique must be used to keep the device junction temperature below the maximum limit of 105°C.

10 Power Supply Recommendations

The device requires three supplies in order to operate properly. These supplies are AVDD_1P8, DVDD_1P8, and DVDD_1P2. All supplies must be driven with low-noise sources to be able to achieve the best performance from the device. When determining the drive current needed to drive each of the supplies of the device, a margin of 50-100% over the typical current might be needed to account for the current consumption across different modes of operation.

10.1 Power Sequencing and Initialization

Figure 95 shows the suggested power-up sequencing and reset timing for the device. Note that the DVDD_1P2 supply must rise before the AVDD_1P8 supply. If the AVDD_1P8 supply rises before the DVDD_1P2 supply, the AVDD_1P8 supply current is several times higher than the normal operating current until the time the DVDD_1P2 supply reaches the 1.2-V level.

The device requires register described in Table 43 to be written as part of the initialization.

Table 43. Initialization Register Details

INITIALIZATION REGISTER ADDRESS	16-BIT DATA WORD TO BE WRITTEN
0Ah	3000h

The initialization sequence is described below:

1. Power-up the supplies as indicated,
2. Apply a hardware reset pulse,
3. Write the initialization register listed in Table 43 through the SPI interface,
4. Write other device settings through the SPI interface, and
5. After a wait time, the device is ready for high accuracy operation.

The power sequence and initialization is shown in Figure 95.

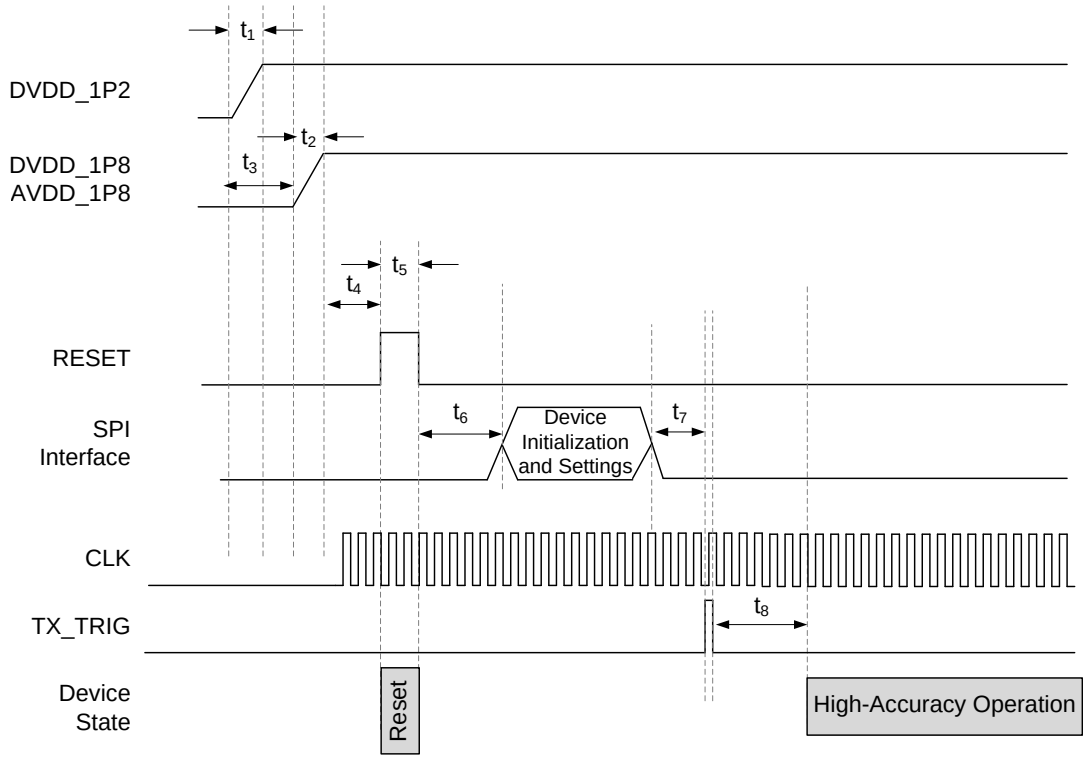


Figure 95. Power Sequencing and Initialization

The timing parameters corresponding to Figure 95 are shown in Table 44.

Table 44. Timing for Power Sequencing and Initialization

		MIN	MAX	UNIT
t_1	Ramp-up time of DVDD_1P2	10 µ	50 m	s
t_2	Ramp up time of AVDD_1P8 and DVDD_1P8	10 µ	50 m	s
t_3	Time between DVDD_1P2 and AVDD_1P8 start of ramp up	t_1		
t_4	Time between supplies stabilizing and application of a hardware reset	10		ms
t_5	Width of hardware reset	100		ns
t_6	Time between hardware reset and SPI write for device initialization and programming of device settings	100		ns
t_7	Time between programming of device settings and synchronization using TX_TRIG	100		ns
t_8	Time between TX_TRIG pulse and device ready for high-accuracy operation	10		ADC clocks

11 Layout

11.1 Power Supply, Grounding, and Bypassing

In a mixed-signal system design, the power-supply and grounding design plays a significant role. The device distinguishes between two different grounds: AVSS (analog ground) and DVSS (digital ground). In most cases, laying out the PCB to use a single ground plane is adequate. However, in high-frequency or high-performance systems, care must be taken so that this ground plane is properly partitioned between various sections within the system to minimize interactions between analog and digital circuitry. Alternatively, the digital supply set consisting of the DVDD_1P8, DVDD_1P2, and DVSS pins can be placed on separate power and ground planes. For this configuration, tie the AVSS and DVSS grounds together at the power connector in a star layout. In addition, optical or digital isolators (such as the ISO7240) can completely separate the analog portion from the digital portion. Consequently, such isolators prevent digital noise from contaminating the analog portion. Table 45 lists the related circuit blocks for each power supply.

Table 45. Supply versus Circuit Blocks

POWER SUPPLY	GROUND	CIRCUIT BLOCKS
AVDD_1P8	AVSS	ADC analog, reference voltage and current generator, band-gap circuit, and ADC clock buffer
DVDD_1P8	DVSS	LVDS serializer and buffer, and PLL
DVDD_1P2	DVSS	ADC digital and serial interface

Reference all bypassing and power supplies for the device to their corresponding ground planes. Bypass all supply pins with 0.1-μF ceramic chip capacitors (size 0603 or smaller). In order to minimize the lead and trace inductance, the capacitors must be located as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition, larger bipolar decoupling capacitors (2.2 μF to 10 μF, effective at lower frequencies) can also be used on the main supply pins. These components can be placed on the PCB in close proximity (< 0.5 inch or 12.7 mm) to the device itself.

Bypass the VCM pin with at least a 1-μF capacitor; higher value capacitors can be used for better low-frequency noise suppression. For best results, choose low-inductance ceramic chip capacitors (size 0402, > 1 μF) placed as close as possible to the device pin.

11.2 Layout Guidelines

High-speed, mixed-signal devices are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffer and drivers. For the device, care must be taken to ensure that the interaction between the analog and digital supplies within the device is kept to a minimal amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each of the supply and ground connections. Smaller effective inductances of the supply and ground pins result in better noise suppression. For this reason, multiple pins are used to connect each supply and ground sets. Low inductance properties must be maintained throughout the design of the PCB layout by use of proper planes and layer thickness.

To avoid noise coupling through supply pins, TI recommends keeping sensitive input pins (such as the INM and INP pins) away from the supply planes. For example, do not route the traces or vias connected to these pins across the supply planes. That is, avoid the power planes under the INM and INP pins.

Some layout guidelines associated with the layout of the high speed interfaces are listed below:

- The length of the positive and negative traces of a differential pair must be matched to within 2 mils of each other.
- Each differential pair length must be matched within 10 mils of other differential pairs.
- When the ADC is used on the same printed circuit board (PCB) with a digital intensive component (such as an FPGA or ASIC), separate digital and analog ground planes must be used. Do not overlap these separate ground planes to minimize undesired coupling.
- Connect decoupling capacitors directly to ground and place these capacitors close to the ADC power pins and the power-supply pins to filter high-frequency current transients directly to the ground plane.
- Ground and power planes must be wide enough to keep the impedance very low. In a multilayer PCB, one layer must be dedicated to each ground and power plane.

Layout Guidelines (continued)

- All high-speed traces must be routed straight with minimum bends. Where a bend is necessary, avoid making very sharp right-angle bends in the trace.
- In order to maintain proper LVDS timing, all LVDS traces must follow a controlled impedance design. In addition, all LVDS trace lengths must be equal and symmetrical; TI recommends keeping trace length variations less than 150 mil (0.150 inch or 3.81 mm).
- When routing CML lines, the traces must be designed for a controlled impedance of 50 Ω. The routing of different lines must be matched as much as possible to minimize the inter-lane skew. However, trace length matching is less critical for the JESD interface as compared to the LVDS interface.

Additional details on the NFBGA PCB layout techniques can be found in the Texas Instruments application report, *MicroStar BGA Packaging Reference Guide* (SSYZ015), available from www.ti.com.

11.3 Layout Example

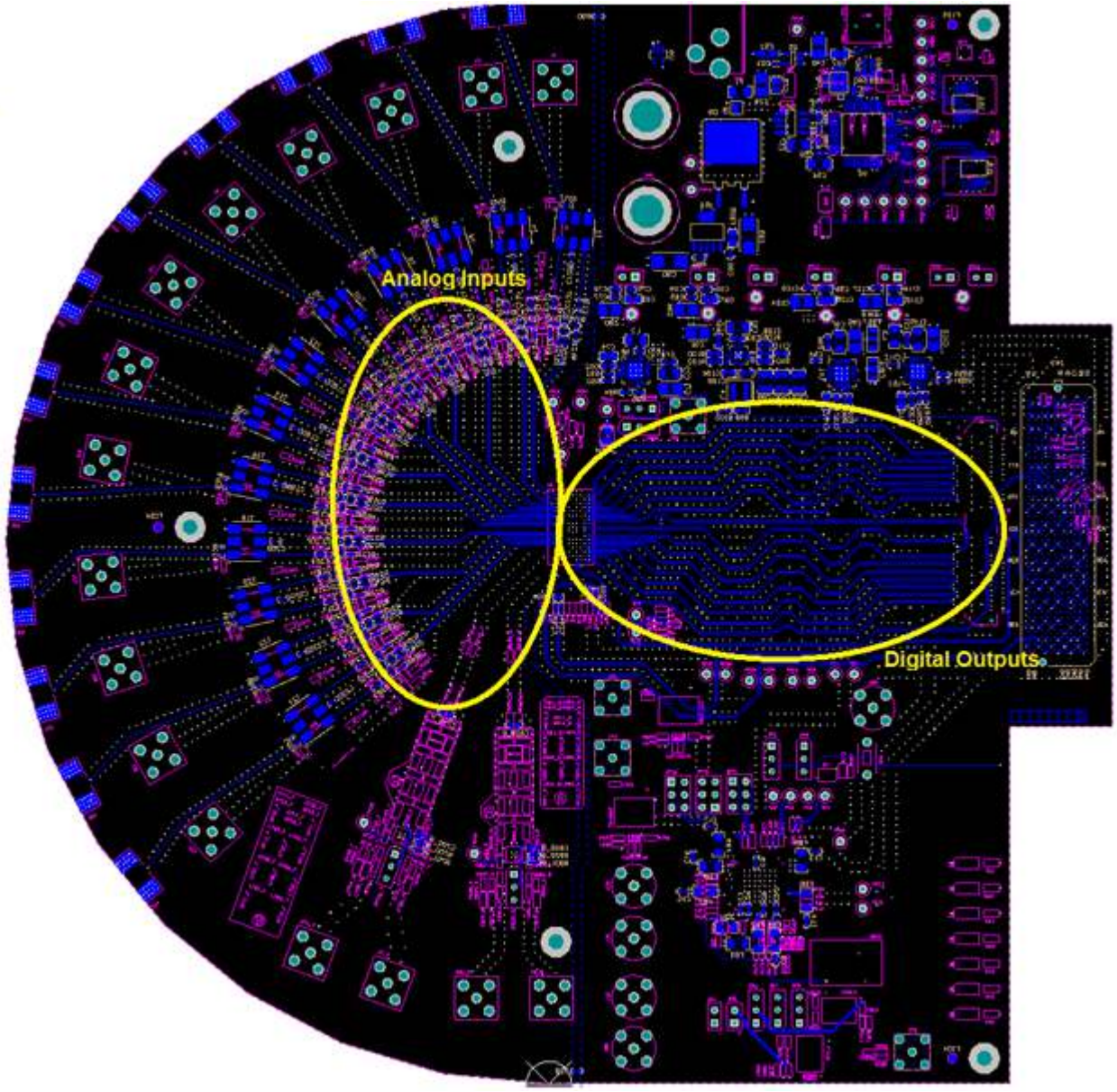


Figure 96. Example Layout

12 Register Map

12.1 ADC Registers

The register map of the device is shown in Table 46.

Table 46. ADC Register Map

REGISTER ADDRESS	REGISTER DATA(1)															
(Hex)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	REG_READ_EN	RESET
1	0	LVDS_RATE_2X	0	0	0	0	0	0	SEL_CH[2]	EN_JESD	DIS_LVDS	SEL_CH[1]	0	SEL_CH[0]	0	GLOBAL_PDN
2	PAT_MODES_FCLK			LOW_LATENCY_EN	AVG_EN	SEL_PRBS_PAT_FCLK	PAT_MODES			SEL_PRBS_PAT_GBL	OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0]					
3	SER_DATA_RATE			DIG_GAIN_EN	0	OFFSET_CORR_DELAY_FROM_TX_TRIG[7:6]		DIG_OFFSET_EN	0	0	JESD_WR_SEL	0	0	0	0	0
4	OFFSET_REMOVAL_SELF	OFFSET_REMOVAL_START_SEL	OFFSET_REMOVAL_START_MANUAL	AUTO_OFFSET_REMOVAL_ACC_CYCLES				PAT_SEL_IND	PRBS_SYNC	PRBS_MODE	PRBS_EN	MSB_FIRST	0	0	ADC_RES	
5	CUSTOM_PATTERN															
7	AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL					0	0	0	0	0	0	0	0	0	0	CHOPPER_EN
8	0	0	AUTO_OFFSET_REMOVAL_VAL_RD													
A	0	0	INIT2	INIT1	0	0	0	0	0	0	0	0	0	0	0	0
B	0	0	0	0	EN_DITHER	0	0	0	0	0	0	0	0	0	0	0
D	GAIN_ADC1o					0	OFFSET_ADC1o									
E	GAIN_ADC1e					0	OFFSET_ADC1e									
F	GAIN_ADC2o					0	OFFSET_ADC2o									
10	GAIN_ADC2e					0	OFFSET_ADC2e									
11	GAIN_ADC3o					0	OFFSET_ADC3o									
12	GAIN_ADC3e					0	OFFSET_ADC3e									
13	GAIN_ADC4o					0	OFFSET_ADC4o									
14	GAIN_ADC4e					0	OFFSET_ADC4e									
15	PAT_PRBS_LVDS1	PAT_PRBS_LVDS2	PAT_PRBS_LVDS3	PAT_PRBS_LVDS4	PAT_LVDS1			PAT_LVDS2			HPF_ROUND_EN_CH1-8	HPF_CORNER_ADC1-4				DIG_HPF_EN_ADC1-4
17	0	0	0	0	IN_16CH_ADC1	IN_16CH_ADC2	IN_16CH_ADC3	IN_16CH_ADC4	PAT_LVDS3			PAT_LVDS4			0	0
18	PDN_DIG_ADC4	PDN_DIG_ADC3	PDN_DIG_ADC2	PDN_DIG_ADC1	PDN_LVDS4	PDN_LVDS3	PDN_LVDS2	PDN_LVDS1	PDN_ANA_ADC4	PDN_ANA_ADC3	PDN_ANA_ADC2	PDN_ANA_ADC1	INVERT_LVDS4	INVERT_LVDS3	INVERT_LVDS2	INVERT_LVDS1

(1) Default value of all registers is 0.

ADC Registers (continued)

Table 46. ADC Register Map (continued)

REGISTER ADDRESS	REGISTER DATA[1]															
(Hex)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
19	GAIN_ADC5o					0	OFFSET_ADC5o									
1A	GAIN_ADC5e					0	OFFSET_ADC5e									
1B	GAIN_ADC6o					0	OFFSET_ADC6o									
1C	GAIN_ADC6e					0	OFFSET_ADC6e									
1D	GAIN_ADC7o					0	OFFSET_ADC7o									
1E	GAIN_ADC7e					0	OFFSET_ADC7e									
1F	GAIN_ADC8o					0	OFFSET_ADC8o									
20	GAIN_ADC8e					0	OFFSET_ADC8e									
21	PAT_PRBS_LVDS5	PAT_PRBS_LVDS6	PAT_PRBS_LVDS7	PAT_PRBS_LVDS8	PAT_LVDS5			PAT_LVDS6			0	HPF_CORNER_ADC5-8				DIG_HPF_EN_ADC5-8
23	0	0	0	0	IN_16CH_ADC5	IN_16CH_ADC6	IN_16CH_ADC7	IN_16CH_ADC8	PAT_LVDS7			PAT_LVDS8			0	0
24	PDN_DIG_ADC8	PDN_DIG_ADC7	PDN_DIG_ADC6	PDN_DIG_ADC5	PDN_LVDS8	PDN_LVDS7	PDN_LVDS6	PDN_LVDS5	PDN_ANA_ADC8	PDN_ANA_ADC7	PDN_ANA_ADC6	PDN_ANA_ADC5	INVERT_LVDS8	INVERT_LVDS7	INVERT_LVDS6	INVERT_LVDS5
25	GAIN_ADC9o					0	OFFSET_ADC9o									
26	GAIN_ADC9e					0	OFFSET_ADC9e									
27	GAIN_ADC10o					0	OFFSET_ADC10o									
28	GAIN_ADC10e					0	OFFSET_ADC10e									
29	GAIN_ADC11o					0	OFFSET_ADC11o									
2A	GAIN_ADC11e					0	OFFSET_ADC11e									
2B	GAIN_ADC12o					0	OFFSET_ADC12o									
2C	GAIN_ADC12e					0	OFFSET_ADC12e									
2D	PAT_PRBS_LVDS9	PAT_PRBS_LVDS10	PAT_PRBS_LVDS11	PAT_PRBS_LVDS12	PAT_LVDS9			PAT_LVDS10			HPF_ROUND_EN_CH9-16	HPF_CORNER_ADC9-12				DIG_HPF_EN_ADC9-12
2F	0	0	0	0	IN_16CH_ADC9	IN_16CH_ADC10	IN_16CH_ADC11	IN_16CH_ADC12	PAT_LVDS11			PAT_LVDS12			0	0
30	PDN_DIG_ADC12	PDN_DIG_ADC11	PDN_DIG_ADC10	PDN_DIG_ADC9	PDN_LVDS12	PDN_LVDS11	PDN_LVDS10	PDN_LVDS9	PDN_ANA_ADC12	PDN_ANA_ADC11	PDN_ANA_ADC10	PDN_ANA_ADC9	INVERT_LVDS12	INVERT_LVDS11	INVERT_LVDS10	INVERT_LVDS9

ADC Registers (continued)

Table 46. ADC Register Map (continued)

REGISTER ADDRESS	REGISTER DATA[1]															
(Hex)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31	GAIN_ADC13o					0	OFFSET_ADC13o									
32	GAIN_ADC13e					0	OFFSET_ADC13e									
33	GAIN_ADC14o					0	OFFSET_ADC14o									
34	GAIN_ADC14e					0	OFFSET_ADC14e									
35	GAIN_ADC15o					0	OFFSET_ADC15o									
36	GAIN_ADC15e					0	OFFSET_ADC15e									
37	GAIN_ADC16o					0	OFFSET_ADC16o									
38	GAIN_ADC16e					0	OFFSET_ADC16e									
39	PAT_PRBS_LVDS13	PAT_PRBS_LVDS14	PAT_PRBS_LVDS15	PAT_PRBS_LVDS16	PAT_LVDS13			PAT_LVDS14			0	HPF_CORNER_ADC13-16				DIG_HPF_EN_ADC13-16
3B	0	0	0	0	IN_16CH_ADC13	IN_16CH_ADC14	IN_16CH_ADC15	IN_16CH_ADC16	PAT_LVDS15			PAT_LVDS16			0	0
3C	PDN_DIG_ADC16	PDN_DIG_ADC15	PDN_DIG_ADC14	PDN_DIG_ADC13	PDN_LVDS16	PDN_LVDS15	PDN_LVDS14	PDN_LVDS13	PDN_ANA_ADC16	PDN_ANA_ADC15	PDN_ANA_ADC14	PDN_ANA_ADC13	INVERT_LVDS16	INVERT_LVDS15	INVERT_LVDS14	INVERT_LVDS13
43	0	0	0	0	0	0	0	0	0	0	0	LVDS_DCLK_DELAY_PROG				

12.1.1 Description of Registers

12.1.1.1 Register 0h (address = 0h)

Figure 97. Register 0h

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	REG_READ_EN	RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 47. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
15-2	0	W	0h	Must write 0
1	REG_READ_EN	W	0h	Register readout enabled. 0 = Disabled 1 = Enabled; see the *Serial Peripheral Interface (SPI) Operation* section for further details.
0	RESET	W	0h	0 = Disabled 1 = Enabled (this setting returns the device to a reset state; this bit is self-clearing bit)

12.1.1.2 Register 1h (address = 1h)

Figure 98. Register 1h

15	14	13	12	11	10	9	8
0	LVDS_RATE_2X	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEL_CH[2]	EN_JESD	DIS_LVDS	SEL_CH[1]	0	SEL_CH[0]	0	GLOBAL_PDN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 48. Register 1h Field Descriptions

Bit	Field	Type	Reset	Description
15	0	R/W	0h	Must write 0
14	LVDS_RATE_2X	R/W	0h	0 = 1X rate; normal operation (default) 1 = 2X rate. This setting combines the data of two LVDS pairs into a single LVDS pair. This feature can be used when the ADC clock rate is low.
13-8	0	R/W	0h	Must write 0
7	SEL_CH[2]	R/W	0h	Input mode selection bit 3. Table 49 lists bit settings for the three input modes.
6	EN_JESD	R/W	0h	0 = JESD interface disabled 1 = JESD interface enabled; see Table 49
5	DIS_LVDS	R/W	0h	0 = LVDS interface is enabled (default) 1 = LVDS interface is disabled
4	SEL_CH[1]	R/W	0h	Input mode selection bit 2. Table 49 lists bit settings for the three input modes.
3	0	R/W	0h	Must write 0
2	SEL_CH[0]	R/W	0h	Input mode selection bit 1. Table 49 lists bit settings for the three input modes.
1	0	R/W	0h	Must write 0
0	GLOBAL_PDN	R/W	0h	0 = The device operates in normal mode (default) 1 = ADC enters complete power-down mode

Table 49. 8-, 16-, and 32-Input Mode Selection

INPUT MODE	SEL_CH[2]	SEL_CH[1]	SEL_CH[0]
8-channel input	1	1	1
16-channel input	0	1	1
32-channel input	0	0	0

Table 50. Output Interface Supported in 8-, 16-, and 32-Input Mode

INPUT MODE	OUTPUT INTERFACE SUPPORTED?	
	LVDS	JESD204B
8-channel input	Yes	No
16-channel input	Yes	Yes
32-channel input	Yes	Yes

12.1.1.3 Register 2h (address = 2h)

Figure 99. Register 2h

15	14	13	12	11	10	9	8
PAT_MODES_FCLK[2:0]			LOW_LATENCY_EN	AVG_EN	SEL_PRBS_PAT_FCLK	PAT_MODES[2:0]	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
PAT_MODES[2:0]	SEL_PRBS_PAT_GBL	OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0]					
R/W-0h	R/W-0h	R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 51. Register 2h Field Descriptions

Bit	Field	Type	Reset	Description
15-13	PAT_MODES_FCLK[2:0]	R/W	0h	These bits enable different test patterns on the frame clock line; see Table 52 for bit descriptions and the *LVDS Test Pattern Mode* section for further details.
12	LOW_LATENCY_EN	R/W	0h	0 = Default latency with digital features supported 1 = Low-latency with digital features bypassed
11	AVG_EN	R/W	0h	0 = No digital averaging 1 = Enables digital averaging of two channels to improve signal-to-noise ratio (SNR)
10	SEL_PRBS_PAT_FCLK	R/W	0h	0 = Normal operation 1 = Enables the PRBS pattern to be generated on FCLK; see the *LVDS Test Pattern Mode* section for further details.
9-7	PAT_MODES[2:0]	R/W	0h	These bits enable different test patterns on the LVDS data lines; see Table 52 for bit descriptions and the *LVDS Test Pattern Mode* section for further details.
6	SEL_PRBS_PAT_GBL	R/W	0h	0 = Normal operation 1 = Enables the PRBS pattern to be generated on all the LVDS data lines; see the *LVDS Test Pattern Mode* section for further details.
5-0	OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0]	R/W	0h	This is a part of an 8-bit control that initiates offset correction after the TX_TRIG input pulse (each step is equivalent to one sample delay); the remaining two MSB bits are the OFFSET_CORR_DELAY_FROM_TX_TRIG[7:6] bits (bits 10-9) in register 3.

Table 52. Pattern Mode Bit Description(1)

PAT_MODES[2:0] or PAT_MODES_FCLK[2:0] or PAT_LVDSx[2:0]	DESCRIPTION
000	Normal operation
001	Sync (half frame 1, half frame 0)
010	Deskew
011	Custom(2)
100	All 1s
101	Toggle mode
110	All 0s
111	Ramp(2)

(1) For detailed description, see Table 33.
(2) Either the custom or ramp pattern setting is required for PRBS pattern selection.

12.1.1.4 Register 3h (address = 3h)

Figure 100. Register 3h

15	14	13	12	11	10	9	8
SER_DATA_RATE			DIG_GAIN_EN	0	OFFSET_CORR_DELAY_FROM_TX_TRIG[7:6]		DIG_OFFSET_EN
R/W-0h			R/W-0h	R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
0	0	JESD_WR_SEL	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 53. Register 3h Field Descriptions

Bit	Field	Type	Reset	Description
15-13	SER_DATA_RATE	R/W	0h	These bits control the LVDS serialization rate. 000 = 12X 001 = 14X 100 = 16X 011 = 10X 101, 110, 111, 010 = Unused
12	DIG_GAIN_EN	R/W	0h	0 = Digital gain disabled 1 = Digital gain enabled
11	0	R/W	0h	Must write 0
10-9	OFFSET_CORR_DELAY_FROM_TX_TRIG[7:6]	R/W	0h	This is a part of an 8-bit control that initiates offset correction after the TX_TRIG input pulse (each step is equivalent to one sample delay); the remaining six LSB bits are the OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0] bits (bits 5-0) in register 2.
8	DIG_OFFSET_EN	R/W	0h	0 = Digital offset subtraction disabled 1 = Digital offset subtraction enabled
7-6	0	R/W	0h	Must write 0
5	JESD_WR_SEL	R/W	0h	0 = Setting when writing to all registers except for registers with addresses in the decimal range of 115-119 and 134-138 1 = Setting when writing to registers with addresses in the decimal range of 115-119 and 134-138
4-0	0	R/W	0h	Must write 0

12.1.1.5 Register 4h (address = 4h)

Figure 101. Register 4h

15	14	13	12	11	10	9	8
OFFSET_ REMOVAL_ SELF	OFFSET_ REMOVAL_ START_ SEL	OFFEST_ REMOVAL_ START_ MANUAL	AUTO_OFFSET_REMOVAL_ACC_CYCLES[3:0]				PAT_ SELECT_ IND
R/W-0h	R/W-0h	R/W-0h	R/W-0h				R/W-0h
7	6	5	4	3	2	1	0
PRBS_ SYNC	PRBS_ MODE	PRBS_EN	MSB_FIRST	0	0	ADC_RES	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 54. Register 4h Field Descriptions

Bit	Field	Type	Reset	Description
15	OFFSET_REMOVAL_SELF	R/W	0h	Auto offset removal mode is enabled when this bit is set to 1
14	OFFSET_REMOVAL_START_SEL	R/W	0h	0 = Auto offset correction initiated when the OFFSET_REMOVAL_START_ MANUAL bit is set to 1. 1 = Auto offset correction initiated with a pulse on TX_TRIG pin.
13	OFFSET_REMOVAL_START_ MANUAL	R/W	0h	This bit initiates offset correction when OFFSET_REMOVAL_START_SEL is set to 0.
12-9	AUTO_OFFSET_REMOVAL_ACC_ CYCLES	R/W	0h	These bits define the number of samples required to generate an offset in auto offset correction mode
8	PAT_SELECT_IND	R/W	0h	0 = All LVDS output data lines have the same pattern, as determined by the PAT_MODES[2:0] bits 1 = Different test patterns can be sent on different LVDS data lines; see the *LVDS Test Pattern Mode* section for further details
7	PRBS_SYNC	R/W	0h	0 = Normal operation 1 = PRBS generator is in a reset state
6	PRBS_MODE	R/W	0h	0 = 23-bit PRBS generator 1 = 9-bit PRBS generator
5	PRBS_EN	R/W	0h	0 = PRBS sequence generation block disabled 1 = PRBS sequence generation block enabled; see the *LVDS Test Pattern Mode* section for further details
4	MSB_FIRST	R/W	0h	0 = The LSB is transmitted first on serialized output data 1 = The MSB is transmitted first on serialized output data
3-2	0	R/W	0h	Must write 0
1-0	ADC_RES	R/W	0h	These bits control the ADC resolution. 00 = 12-bit resolution 01 = 14-bit resolution 11 = 10-bit resolution 10 = Unused

12.1.1.6 Register 5h (address = 5h)

Figure 102. Register 5h

15	14	13	12	11	10	9	8
CUSTOM_PATTERN							
R/W-0h							
7	6	5	4	3	2	1	0
CUSTOM_PATTERN							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 55. Register 5h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CUSTOM_PATTERN	R/W	0h	If the pattern mode is programmed to a custom pattern mode, then the custom pattern value can be provided by programming these bits; see the *LVDS Test Pattern Mode* section for further details.

12.1.1.7 Register 7h (address = 7h)

Figure 103. Register 7h

15	14	13	12	11	10	9	8
AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL					0	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	CHOPPER_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 56. Register 7h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL	R/W	0h	Write the channel number to read the offset value in auto offset correction mode for a corresponding channel number (read the offset value in AUTO_OFFSET_REMOVAL_VAL_RD.(1)
10-1	0	R/W	0h	Must write 0
0	CHOPPER_EN	R/W	0h	The chopper can be used to move low-frequency, 1 / f noise to f_S / 2 frequency. 0 = Chopper disabled 1 = Chopper enabled

(1) In 32-channel input mode, the value written in this register corresponds to the channel number (minus 1). When operating in 8- and 16-input modes, the value can be mapped to the odd or even data streams of the 16 ADCs. For example, a value of 0 corresponds to the odd data stream of ADC1. Likewise, a value of 1 corresponds to the even data stream of ADC1, and so on respectively.

12.1.1.8 Register 8h (address = 8h)

Figure 104. Register 8h

15	14	13	12	11	10	9	8
0	0	AUTO_OFFSET_REMOVAL_VAL_RD[13:0]					
R/W-0h	R/W-0h	R/W-0h					
7	6	5	4	3	2	1	0
AUTO_OFFSET_REMOVAL_VAL_RD[13:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 57. Register 8h Field Descriptions

Bit	Field	Type	Reset	Description
15-14	0	R/W	0h	Must write 0
13-0	AUTO_OFFSET_REMOVAL_VAL_RD	R/W	0h	Read the offset value applied in auto offset correction mode for a specific channel number as defined in AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL

12.1.1.9 Register Ah (address = Ah)

Figure 105. Register Ah

15	14	13	12	11	10	9	8
0	0	INIT2	INIT1	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 58. Register Ah Field Descriptions

Bit	Field	Type	Reset	Description
15-14	0	R/W	0h	Must write 0
13	INIT2	R/W	0h	Write 1 as part of the initialization after power-up (1)
12	INIT1	R/W	0h	Write 1 as part of the initialization after power-up (1)
11-0	0	R/W	0h	Must write 0

(1) See Table 43.

12.1.1.10 Register Bh (address = Bh)

Figure 106. Register Bh

15	14	13	12	11	10	9	8
0	0	0	0	EN_DITHER	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 59. Register Bh Field Descriptions

Bit	Field	Type	Reset	Description
15-12	0	R/W	0h	Must write 0
11	EN_DITHER	R/W	0h	Dither can be used to reduce the power in higher-order harmonics. 0 = Dither disabled 1 = Dither enabled Note: Enabling the dither converts higher-order harmonics power into noise. Thus, enabling this mode reduce the power in higher-order harmonics but degrades SNR.
10-0	0	R/W	0h	Must write 0

12.1.1.11 Register Dh (address = Dh)

Figure 107. Register Dh

15	14	13	12	11	10	9	8
GAIN_ADC1o					0	OFFSET_ADC1o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC1o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 60. Register Dh Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC1o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC1 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC1o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC1 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.12 Register Eh (address = Eh)

Figure 108. Register Eh

15	14	13	12	11	10	9	8
GAIN_ADC1e					0	OFFSET_ADC1e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC1e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 61. Register Eh Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC1e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC1 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC1e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC1 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.13 Register Fh (address = Fh)

Figure 109. Register Fh

15	14	13	12	11	10	9	8
GAIN_ADC2o					0	OFFSET_ADC2o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC2o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 62. Register Fh Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC2o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC2 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC2o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC2 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.14 Register 10h (address = 10h)

Figure 110. Register 10h

15	14	13	12	11	10	9	8
GAIN_ADC2e					0	OFFSET_ADC2e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC2e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 63. Register 10h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC2e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC2 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC2e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC2 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.15 Register 11h (address = 11h)

Figure 111. Register 11h

15	14	13	12	11	10	9	8
GAIN_ADC3o					0	OFFSET_ADC3o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC3o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 64. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC3o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC3 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC3o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC3 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.16 Register 12h (address = 12h)

Figure 112. Register 12h

15	14	13	12	11	10	9	8
GAIN_ADC3e					0	OFFSET_ADC3e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC3e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 65. Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC3e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC3 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC3e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC3 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.17 Register 13h (address = 13h)

Figure 113. Register 13h

15	14	13	12	11	10	9	8
GAIN_ADC4o					0	OFFSET_ADC4o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC4o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 66. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC4o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC4 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC4o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC4 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.18 Register 14h (address = 14h)

Figure 114. Register 14h

15	14	13	12	11	10	9	8
GAIN_ADC4e					0	OFFSET_ADC4e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC4e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 67. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC4e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC4 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC4e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC4 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.19 Register 15h (address = 15h)

Figure 115. Register 15h

15	14	13	12	11	10	9	8
PAT_PRBS_LVDS1	PAT_PRBS_LVDS2	PAT_PRBS_LVDS3	PAT_PRBS_LVDS4	PAT_LVDS1			PAT_LVDS2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS2		HPF_ROUND_EN_CH1-8	HPF_CORNER_ADC1-4				DIG_HPF_EN_ADC1-4
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 68. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS1	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 1 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
14	PAT_PRBS_LVDS2	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 2 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
13	PAT_PRBS_LVDS3	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 3 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
12	PAT_PRBS_LVDS4	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 4 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
11-9	PAT_LVDS1	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 1 can be programmed with these bits; see Table 33 for bit descriptions.
8-6	PAT_LVDS2	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 2 can be programmed with these bits; see Table 33 for bit descriptions.
5	HPF_ROUND_EN_CH1-8	R/W	0h	0 = Rounding in the ADC HPF is disabled for channel 1 to 8. HPF output is truncated to be mapped to the ADC resolution bits. 1 = HPF output of channel 1 to 8 is mapped to the ADC resolution bits by the round-off operation.
4-1	HPF_CORNER_ADC1-4	R/W	0h	When the DIG_HPF_EN_ADC1-4 bit is set to 1, the digital HPF characteristic for the corresponding ADCs can be programmed by setting the value of k with these bits. The value of k can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_ADC1-4	R/W	0h	0 = Digital HPF disabled for ADCs 1 to 4 (default) 1 = Enables digital HPF for ADCs 1 to 4

12.1.1.20 Register 17h (address = 17h)

Figure 116. Register 17h

15	14	13	12	11	10	9	8
0	0	0	0	IN_16CH_ ADC1	IN_16CH_ ADC2	IN_16CH_ ADC3	IN_16CH_ ADC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS3			PAT_LVDS4			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 69. Register 17h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	0	R/W	0h	Must write 0
11	IN_16CH_ADC1	R/W	0h	Selects the input pair sampled by ADC1 in 16-input mode. 0 = ADC1 samples the signal on INP1, INM1 1 = ADC1 samples the signal on INP2, INM2
10	IN_16CH_ADC2	R/W	0h	Selects the input pair sampled by ADC2 in 16-input mode. 0 = ADC2 samples the signal on INP3, INM3 1 = ADC2 samples the signal on INP4, INM4
9	IN_16CH_ADC3	R/W	0h	Selects the input pair sampled by ADC3 in 16-input mode. 0 = ADC3 samples the signal on INP5, INM5 1 = ADC3 samples the signal on INP6, INM6
8	IN_16CH_ADC4	R/W	0h	Selects the input pair sampled by ADC4 in 16-input mode. 0 = ADC4 samples the signal on INP7, INM7 1 = ADC4 samples the signal on INP8, INM8
7-5	PAT_LVDS3	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 3 can be programmed with these bits; see Table 33 for bit descriptions.
4-2	PAT_LVDS4	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 4 can be programmed with these bits; see Table 33 for bit descriptions.
1-0	0	R/W	0h	Must write 0

12.1.1.21 Register 18h (address = 18h)

Figure 117. Register 18h

15	14	13	12	11	10	9	8
PDN_DIG_ ADC4	PDN_DIG_ ADC3	PDN_DIG_ ADC2	PDN_DIG_ ADC1	PDN_LVDS4	PDN_LVDS3	PDN_LVDS2	PDN_LVDS1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_ANA_ ADC4	PDN_ANA_ ADC3	PDN_ANA_ ADC2	PDN_ANA_ ADC1	INVERT_ LVDS4	INVERT_ LVDS3	INVERT_ LVDS2	INVERT_ LVDS1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 70. Register 18h Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_ADC4	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC4
14	PDN_DIG_ADC3	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC3
13	PDN_DIG_ADC2	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC2
12	PDN_DIG_ADC1	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC1
11	PDN_LVDS4	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 4
10	PDN_LVDS3	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 3
9	PDN_LVDS2	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 2
8	PDN_LVDS1	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 1
7	PDN_ANA_ADC4	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC4
6	PDN_ANA_ADC3	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC3
5	PDN_ANA_ADC2	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC2
4	PDN_ANA_ADC1	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC1
3	INVERT_LVDS4	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 4. Has no effect on Test patterns.
2	INVERT_LVDS3	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 3. Has no effect on Test patterns.
1	INVERT_LVDS2	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 2. Has no effect on Test patterns.
0	INVERT_LVDS1	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 1. Has no effect on Test patterns.

12.1.1.22 Register 19h (address = 19h)

Figure 118. Register 19h

15	14	13	12	11	10	9	8
GAIN_ADC5o					0	OFFSET_ADC5o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC5o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 71. Register 19h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC5o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC5 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC5o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC5 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.23 Register 1Ah (address = 1Ah)

Figure 119. Register 1Ah

15	14	13	12	11	10	9	8
GAIN_ADC5e					0	OFFSET_ADC5e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC5e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 72. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC5e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC5 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC5e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC5 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.24 Register 1Bh (address = 1Bh)

Figure 120. Register 1Bh

15	14	13	12	11	10	9	8
GAIN_ADC6o					0	OFFSET_ADC6o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC6o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 73. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC6o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC6 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC6o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC6 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.25 Register 1Ch (address = 1Ch)

Figure 121. Register 1Ch

15	14	13	12	11	10	9	8
GAIN_ADC6e					0	OFFSET_ADC6e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC6e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 74. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC6e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC6 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC6e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC6 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.26 Register 1Dh (address = 1Dh)

Figure 122. Register 1Dh

15	14	13	12	11	10	9	8
GAIN_ADC7o					0	OFFSET_ADC7o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC7o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 75. Register 1Dh Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC7o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC7 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC7o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC7 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.27 Register 1Eh (address = 1Eh)

Figure 123. Register 1Eh

15	14	13	12	11	10	9	8
GAIN_ADC7e					0	OFFSET_ADC7e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC7e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 76. Register 1Eh Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC7e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC7 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC7e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC7 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.28 Register 1Fh (address = 1Fh)

Figure 124. Register 1Fh

15	14	13	12	11	10	9	8
GAIN_ADC8o					0	OFFSET_ADC8o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC8o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 77. Register 1Fh Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC8o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC8 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC8o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC8 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.29 Register 20h (address = 20h)

Figure 125. Register 20h

15	14	13	12	11	10	9	8
GAIN_ADC8e					0	OFFSET_ADC8e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC8e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 78. Register 20h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC8e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC8 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC8e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC8 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.30 Register 21h (offset = 21h)

Figure 126. Register 21h

15	14	13	12	11	10	9	8
PAT_PRBS_LVDS5	PAT_PRBS_LVDS6	PAT_PRBS_LVDS7	PAT_PRBS_LVDS8	PAT_LVDS5			PAT_LVDS6
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS6		0	HPF_CORNER_ADC5-8				DIG_HPF_EN_ADC5-8
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 79. Register 21h Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS5	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 5 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
14	PAT_PRBS_LVDS6	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 6 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
13	PAT_PRBS_LVDS7	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 7 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
12	PAT_PRBS_LVDS8	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 8 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
11-9	PAT_LVDS5	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 5 can be programmed with these bits; see Table 33 for bit descriptions.
8-6	PAT_LVDS6	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 6 can be programmed with these bits; see Table 33 for bit descriptions.
5	0	R/W	0h	Must write 0
4-1	HPF_CORNER_ADC5-8	R/W	0h	When the DIG_HPF_EN_ADC5-8 bit is set to 1, the digital HPF characteristic for the corresponding ADCs can be programmed by setting the value of k with these bits. The value of k can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_ADC5-8	R/W	0h	0 = Digital HPF disabled for ADCs 5 to 8 (default) 1 = Enables digital HPF for ADCs 5 to 8

12.1.1.31 Register 23h (register = 23h)

Figure 127. Register 23h

15	14	13	12	11	10	9	8
0	0	0	0	IN_16CH_ ADC5	IN_16CH_ ADC6	IN_16CH_ ADC7	IN_16CH_ ADC8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS7			PAT_LVDS8			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 80. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	0	R/W	0h	Must write 0
11	IN_16CH_ADC5	R/W	0h	Selects the input pair sampled by ADC5 in 16-input mode. 0 = ADC5 samples the signal on INP9, INM9 1 = ADC5 samples the signal on INP10, INM10
10	IN_16CH_ADC6	R/W	0h	Selects the input pair sampled by ADC6 in 16-input mode. 0 = ADC6 samples the signal on INP11, INM11 1 = ADC6 samples the signal on INP12, INM12
9	IN_16CH_ADC7	R/W	0h	Selects the input pair sampled by ADC7 in 16-input mode. 0 = ADC7 samples the signal on INP13, INM13 1 = ADC7 samples the signal on INP14, INM14
8	IN_16CH_ADC8	R/W	0h	Selects the input pair sampled by ADC8 in 16-input mode. 0 = ADC8 samples the signal on INP15, INM15 1 = ADC8 samples the signal on INP16, INM16
7-5	PAT_LVDS7	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 7 can be programmed with these bits; see Table 33 for bit descriptions.
4-2	PAT_LVDS8	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 8 can be programmed with these bits; see Table 33 for bit descriptions.
1-0	0	R/W	0h	Must write 0

12.1.1.32 Register 24h (address = 24h)

Figure 128. Register 24h

15	14	13	12	11	10	9	8
PDN_DIG_ADC8	PDN_DIG_ADC7	PDN_DIG_ADC6	PDN_DIG_ADC5	PDN_LVDS8	PDN_LVDS7	PDN_LVDS6	PDN_LVDS5
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_ANA_ADC8	PDN_ANA_ADC7	PDN_ANA_ADC6	PDN_ANA_ADC5	INVERT_LVDS8	INVERT_LVDS7	INVERT_LVDS6	INVERT_LVDS5
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 81. Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_ADC8	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC8
14	PDN_DIG_ADC7	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC7
13	PDN_DIG_ADC6	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC6
12	PDN_DIG_ADC5	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC5
11	PDN_LVDS8	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 8
10	PDN_LVDS7	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 7
9	PDN_LVDS6	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 6
8	PDN_LVDS5	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 5
7	PDN_ANA_ADC8	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC8
6	PDN_ANA_ADC7	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC7
5	PDN_ANA_ADC6	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC6
4	PDN_ANA_ADC5	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC5
3	INVERT_LVDS8	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 8. Has no effect on Test patterns.
2	INVERT_LVDS7	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 7. Has no effect on Test patterns.
1	INVERT_LVDS6	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 6. Has no effect on Test patterns.
0	INVERT_LVDS5	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 5. Has no effect on Test patterns.

12.1.1.33 Register 25h (address = 25h)

Figure 129. Register 25h

15	14	13	12	11	10	9	8
GAIN_ADC9o					0	OFFSET_ADC9o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC9o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 82. Register 25h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC9o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC9 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC9o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC9 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.34 Register 26h (address = 26h)

Figure 130. Register 26h

15	14	13	12	11	10	9	8
GAIN_ADC9e					0	OFFSET_ADC9e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC9e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 83. Register 26h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC9e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC9 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC9e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC9 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.35 Register 27h (address = 27h)

Figure 131. Register 27h

15	14	13	12	11	10	9	8
GAIN_ADC10o					0	OFFSET_ADC10o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC10o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 84. Register 27h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC10o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC10 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC10o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC10 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.36 Register 28h (address = 28h)

Figure 132. Register 28h

15	14	13	12	11	10	9	8
GAIN_ADC10e					0	OFFSET_ADC10e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC10e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 85. Register 28h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC10e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC10 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC10e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC10 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.37 Register 29h (address = 29h)

Figure 133. Register 29h

15	14	13	12	11	10	9	8
GAIN_ADC11o					0	OFFSET_ADC11o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC11o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 86. Register 29h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC11o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC11 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC11o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC11 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.38 Register 2Ah (address = 2Ah)

Figure 134. Register 2Ah

15	14	13	12	11	10	9	8
GAIN_ADC11e					0	OFFSET_ADC11e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC11e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 87. Register 2Ah Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC11e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC11 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC11e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC11 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.39 Register 2Bh (address = 2Bh)

Figure 135. Register 2Bh

15	14	13	12	11	10	9	8
GAIN_ADC12o					0	OFFSET_ADC12o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC12o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 88. Register 2Bh Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC12o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC12 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC12o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC12 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.40 Register 2Ch (address = 2Ch)

Figure 136. Register 2Ch

15	14	13	12	11	10	9	8
GAIN_ADC12e					0	OFFSET_ADC12e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC12e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 89. Register 2Ch Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC12e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC12 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC12e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC12 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.41 Register 2Dh (address = 2Dh)

Figure 137. Register 2Dh

15	14	13	12	11	10	9	8
PAT_PRBS_LVDS9	PAT_PRBS_LVDS10	PAT_PRBS_LVDS11	PAT_PRBS_LVDS12	PAT_LVDS9			PAT_LVDS10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS10		HPF_ROUND_EN_CH9-16	HPF_CORNER_ADC9-12				DIG_HPF_EN_ADC9-12
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 90. Register 2Dh Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS9	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 9 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
14	PAT_PRBS_LVDS10	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 10 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
13	PAT_PRBS_LVDS11	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 11 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
12	PAT_PRBS_LVDS12	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 12 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
11-9	PAT_LVDS9	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 9 can be programmed with these bits; seeTable 33 for bit descriptions.
8-6	PAT_LVDS10	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 10 can be programmed with these bits; seeTable 33 for bit descriptions.
5	HPF_ROUND_EN_CH9-16	R/W	0h	0 = Rounding in the ADC HPF is disabled for channels 9-16. The HPF output is truncated to be mapped to the ADC resolution bits. 1 = HPF output of channels 9-16 is mapped to the ADC resolution bits by the round-off operation.
4-1	HPF_CORNER_ADC9-12	R/W	0h	When the DIG_HPF_EN_CH9-12 bit is set to 1, the digital HPF characteristic for the corresponding ADCs can be programmed by setting the value of k with these bits. The value of k can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_ADC9-12	R/W	0h	0 = Digital HPF disabled for ADCs 9 to 12 (default) 1 = Enables digital HPF for ADCs 9 to 12

12.1.1.42 Register 2Fh (address = 2Fh)

Figure 138. Register 2Fh

15	14	13	12	11	10	9	8
0	0	0	0	IN_16CH_ ADC9	IN_16CH_ ADC10	IN_16CH_ ADC11	IN_16CH_ ADC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS11			PAT_LVDS12			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write;-n = value after reset

Table 91. Register 2Fh Field Descriptions

Bit	Field	Type	Reset	Description
15-12	0	R/W	0h	Must write 0
11	IN_16CH_ADC9	R/W	0h	Selects the input pair sampled by ADC9 in 16-input mode. 0 = ADC9 samples the signal on INP17, INM17 1 = ADC9 samples the signal on INP18, INM18
10	IN_16CH_ADC10	R/W	0h	Selects the input pair sampled by ADC10 in 16-input mode. 0 = ADC10 samples the signal on INP19, INM19 1 = ADC10 samples the signal on INP20, INM20
9	IN_16CH_ADC11	R/W	0h	Selects the input pair sampled by ADC11 in 16-input mode. 0 = ADC11 samples the signal on INP21, INM21 1 = ADC11 samples the signal on INP22, INM22
8	IN_16CH_ADC12	R/W	0h	Selects the input pair sampled by ADC12 in 16-input mode. 0 = ADC12 samples the signal on INP23, INM23 1 = ADC12 samples the signal on INP24, INM24
7-5	PAT_LVDS11[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 11 can be programmed with these bits; seeTable 33 for bit descriptions.
4-2	PAT_LVDS12[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 12 can be programmed with these bits; seeTable 33 for bit descriptions.
1-0	0	R/W	0h	Must write 0

12.1.1.43 Register 30h (address = 30h)

Figure 139. Register 30h

15	14	13	12	11	10	9	8
PDN_DIG_ ADC12	PDN_DIG_ ADC11	PDN_DIG_ ADC10	PDN_DIG_ ADC9	PDN_ LVDS12	PDN_ LVDS11	PDN_ LVDS10	PDN_ LVDS9
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_ANA_ ADC12	PDN_ANA_ ADC11	PDN_ANA_ ADC10	PDN_ANA_ ADC9	INVERT_ LVDS12	INVERT_ LVDS11	INVERT_ LVDS10	INVERT_ LVDS9
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; = value after reset

Table 92. Register 30h Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_ADC12	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC12
14	PDN_DIG_ADC11	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC11
13	PDN_DIG_ADC10	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC10
12	PDN_DIG_ADC9	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC9
11	PDN_LVDS12	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 12
10	PDN_LVDS11	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 11
9	PDN_LVDS10	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 10
8	PDN_LVDS9	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 9
7	PDN_ANA_ADC12	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC12
6	PDN_ANA_ADC11	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC11
5	PDN_ANA_ADC10	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC10
4	PDN_ANA_ADC9	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC9
3	INVERT_LVDS12	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 12. Has no effect on Test patterns.
2	INVERT_LVDS11	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 11. Has no effect on Test patterns.
1	INVERT_LVDS10	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 10. Has no effect on Test patterns.
0	INVERT_LVDS9	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 9. Has no effect on Test patterns.

12.1.1.44 Register 31h (address = 31h)

Figure 140. Register 31h

15	14	13	12	11	10	9	8
GAIN_ADC13o					0	OFFSET_ADC13o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC13o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 93. Register 31h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC13o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC13 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC13o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC13 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.45 Register 32h (address = 32h)

Figure 141. Register 32h

15	14	13	12	11	10	9	8
GAIN_ADC13e					0	OFFSET_ADC13e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC13e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 94. Register 32h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC13e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC13 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC13e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC13 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.46 Register 33h (address = 33h)

Figure 142. Register 33h

15	14	13	12	11	10	9	8
GAIN_ADC14o					0	OFFSET_ADC14o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC14o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 95. Register 33h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC14o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC14 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC14o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC14 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.47 Register 34h (address = 34h)

Figure 143. Register 34h

15	14	13	12	11	10	9	8
GAIN_ADC14e					0	OFFSET_ADC14e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC14e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 96. Register 34h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC14e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC14 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC14e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC14 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.48 Register 35h (address = 35h)

Figure 144. Register 35h

15	14	13	12	11	10	9	8
GAIN_ADC15o					0	OFFSET_ADC15o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC15o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 97. Register 35h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC15o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC15 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC15o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC15 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.49 Register 36h (address = 36h)

Figure 145. Register 36h

15	14	13	12	11	10	9	8
GAIN_ADC15e					0	OFFSET_ADC15e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC15e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 98. Register 36h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC15e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC15 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC15e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC15 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.50 Register 37h (address = 37h)

Figure 146. Register 37h

15	14	13	12	11	10	9	8
GAIN_ADC16o					0	OFFSET_ADC16o	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC16o							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 99. Register 37h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC16o	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the odd sample of ADC16 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC16o	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the odd sample of ADC16 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.51 Register 38h (address = 38h)

Figure 147. Register 38h

15	14	13	12	11	10	9	8
GAIN_ADC16e					0	OFFSET_ADC16e	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_ADC16e							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 100. Register 38h Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_ADC16e	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, the digital gain value for the even sample of ADC16 can be obtained with this register. For a value of N (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_ADC16e	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, the offset value to be subtracted from the even sample of ADC16 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB.

12.1.1.52 Register 39h (address = 39h)

Figure 148. Register 39h

15	14	13	12	11	10	9	8
PAT_PRBS_LVDS13	PAT_PRBS_LVDS14	PAT_PRBS_LVDS15	PAT_PRBS_LVDS16	PAT_LVDS13			PAT_LVDS14
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS14		0	HPF_CORNER_ADC13-16				DIG_HPF_EN_ADC13-16
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 101. Register 39h Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS13	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 13 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
14	PAT_PRBS_LVDS14	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 14 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
13	PAT_PRBS_LVDS15	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 15 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
12	PAT_PRBS_LVDS16	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the PRBS pattern on LVDS output 16 can be enabled with this bit; see the *LVDS Test Pattern Mode* section for further details.
11-9	PAT_LVDS13[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 13 can be programmed with these bits; see Table 33 for bit descriptions.
8-6	PAT_LVDS14[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 14 can be programmed with these bits; see Table 33 for bit descriptions.
5	0	R/W	0h	Must write 0
4-1	HPF_CORNER_ADC13-16	R/W	0h	When the DIG_HPF_EN_CH13-16 bit is set to 1, the digital HPF characteristic for the corresponding ADCs can be programmed by setting the value of k with these bits. The value of k can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_ADC13-16	R/W	0h	0 = Digital HPF disabled for ADCs 13 to 16 (default) 1 = Enables digital HPF for ADCs 13 to 16

12.1.1.53 Register 3Bh (address = 3Bh)

Figure 149. Register 3Bh

15	14	13	12	11	10	9	8
0	0	0	0	IN_16CH_ ADC13	IN_16CH_ ADC14	IN_16CH_ ADC15	IN_16CH_ ADC16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS15			PAT_LVDS16			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 102. Register 3Bh Field Descriptions

Bit	Field	Type	Reset	Description
15-12	0	R/W	0h	Must write 0
11	IN_16CH_ADC13	R/W	0h	Selects the input pair sampled by ADC13 in 16-input mode. 0 = ADC13 samples the signal on INP25, INM25 1 = ADC13 samples the signal on INP26, INM26
10	IN_16CH_ADC14	R/W	0h	Selects the input pair sampled by ADC14 in 16-input mode. 0 = ADC14 samples the signal on INP27, INM27 1 = ADC14 samples the signal on INP28, INM28
9	IN_16CH_ADC15	R/W	0h	Selects the input pair sampled by ADC15 in 16-input mode. 0 = ADC15 samples the signal on INP29, INM29 1 = ADC15 samples the signal on INP30, INM30
8	IN_16CH_ADC16	R/W	0h	Selects the input pair sampled by ADC16 in 16-input mode. 0 = ADC16 samples the signal on INP31, INM31 1 = ADC16 samples the signal on INP32, INM32
7-5	PAT_LVDS15[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 15 can be programmed with these bits; see Table 33 for bit descriptions.
4-2	PAT_LVDS16[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, the pattern on LVDS output 16 can be programmed with these bits; see Table 33 for bit descriptions.
1-0	0	R/W	0h	Must write 0

12.1.1.54 Register 3Ch (address = 3Ch)

Figure 150. Register 3Ch

15	14	13	12	11	10	9	8
PDN_DIG_ ADC16	PDN_DIG_ ADC15	PDN_DIG_ ADC14	PDN_DIG_	PDN_LVDS16	PDN_LVDS15	PDN_LVDS14	PDN_LVDS13
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_ANA_ ADC16	PDN_ANA_ ADC15	PDN_ANA_ ADC14	PDN_ANA_ ADC13	INVERT_ LVDS16	INVERT_ LVDS15	INVERT_ LVDS14	INVERT_ LVDS13
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 103. Register 3Ch Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_ADC16	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC16
14	PDN_DIG_ADC15	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC15
13	PDN_DIG_ADC14	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC14
12	PDN_DIG_ADC13	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for ADC13
11	PDN_LVDS16	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 16
10	PDN_LVDS15	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 15
9	PDN_LVDS14	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 14
8	PDN_LVDS13	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 13
7	PDN_ANA_ADC16	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC16
6	PDN_ANA_ADC15	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC15
5	PDN_ANA_ADC14	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC14
4	PDN_ANA_ADC13	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for ADC13
3	INVERT_LVDS16	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 16. Has no effect on Test patterns.
2	INVERT_LVDS15	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 15. Has no effect on Test patterns.
1	INVERT_LVDS14	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 14. Has no effect on Test patterns.
0	INVERT_LVDS13	R/W	0h	0 = Normal operation (default) 1 = Inverts ADC data sent on LVDS output line 13. Has no effect on Test patterns.

12.1.1.55 Register 43h (address = 43h)

Figure 151. Register 43h

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	LVDS_DCLK_DELAY_PROG				0
R/W-0h	R/W-0h	R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 104. Register 43h Field Descriptions

Bit	Field	Type	Reset	Description
15-5	0	R/W	0h	Must write 0
4-1	LVDS_DCLK_DELAY_PROG	R/W	0h	The LVDS DCLK output delay is programmable with 110-ps steps. Delay values are in twos complement format. Increasing the positive delay increases setup time and reduces hold time, and vice-versa for the negative delay. 0000 = No delay 0001 = 110 ps 0010 = 220 ps … 1110 = –220 ps 1111 = –110ps …
0	0	R/W	0h	Must write 0

12.2 JESD Serial Interface Registers

This section discusses the JESD registers. A register map is available in Table 105.

Table 105. JESD Register Map

REGISTER ADDRESS		REGISTER DATA[1]															
DECIMAL	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
70	46	0	0	0	0	0	0	0	0	0	0	0	0	0	MASK_TX_TRIG	JESD_RESET1	0
73	49	IDLE_MODE	0	0	LANE_ALIGN	FRAME_ALIGN	LINK_CONFIG_DIS	0	0	0	0	0	0	0	FORCE_K	0	0
74	4A	LINK_LAYER_TESTMODES			TX_SYNC_REQ	RELEASE_ILA		0	JESD_RESET2	JESD_RESET3	0	0	0	0	0	0	0
75	4B	0	0	0	0	0	0	0	SING_CONV_PER_OCT	NUM_ADC_PER_LANE			0	0	0	0	0
77	4D	0	0	0	0	0	0	0	0	PRE_EMP				0	0	0	0
80	50	0	0	0	0	0	0	0	0	0	0	0	0	0	0	INC_JESD_VDD	0
81	51	DEVICE_ID								0	0	0	BANK_ID				
82	52	0	0	0	0	0	0	0	0	SCR_EN	0	0	0	0	0	0	0
83	53	0	0	0	0	0	0	0	0	0	0	0	K_VALUE_TO_FORCE				
85	55	JESD_SUBCLASS			0	0	0	0	0	JESD_VER			0	0	0	0	0
115[2]	73	EN_LANE_ID1	EN_LANE_ID2	EN_LANE_ID3	EN_LANE_ID4	EN_CHECKSUM_LANE1	EN_CHECKSUM_LANE2	EN_CHECKSUM_LANE3	EN_CHECKSUM_LANE4	0	0	0	ENABLE_JESD_VER_CONTROL	0	0	0	0
116[2]	74	CHECK_SUM1								CHECK_SUM2							
117[2]	75	CHECK_SUM3								CHECK_SUM4							
118[2]	76	0	0	0	LANE_ID1					0	0	0	LANE_ID2				
119[2]	77	0	0	0	LANE_ID3					0	0	0	LANE_ID4				
120	78	FORCE_LMFC_COUNT	LMFC_COUNTER_INIT_VALUE					0	0	0	0	0	0	0	0	0	0
134[2]	86	EN_LANE_ID5	EN_LANE_ID6	EN_LANE_ID7	EN_LANE_ID8	EN_CHECKSUM_LANE5	EN_CHECKSUM_LANE6	EN_CHECKSUM_LANE7	EN_CHECKSUM_LANE8	0	0	0	0	0	0	0	0
135[2]	87	CHECK_SUM5								CHECK_SUM6							
136[2]	88	CHECK_SUM7								CHECK_SUM8							
137[2]	89	0	0	0	LANE_ID5					0	0	0	LANE_ID6				
138[2]	8A	0	0	0	LANE_ID7					0	0	0	LANE_ID8				

(1) Default value of all registers is 0.
(2) These registers must only be written to after setting the JESD_WR_SEL register bit (register 3, bit 5) to 1. To write any other registers, set the JESD_WR_SEL bit to 0.

12.2.1 Description of JESD Serial Interface Registers

12.2.1.1 Register 70 (address = 46h)

Figure 152. Register 70

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	MASK_TX_TRIG	JESD_RESET1	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 106. Register 70 Field Descriptions

Bit	Field	Type	Reset	Description
15-3	0	R/W	0h	Must write 0
2	MASK_TX_TRIG	R/W	0h	0 = TX_TRIG affects internal clock-phase resets 1 = TX_TRIG does not affect internal clock-phase resets
1	JESD_RESET1	R/W	0h	0 = SYNC~ and SYSREF events reset non-JESD blocks (such as the clock dividers, demodulator, and test pattern generator) 1 = SYNC~ and SYSREF events do not reset non-JESD blocks (such as the clock dividers, demodulator, and test pattern generator)
0	0	R/W	0h	Must write 0

12.2.1.2 Register 73 (address = 49h)

Figure 153. Register 73

15	14	13	12	11	10	9	8
IDLE_MODE	0	0	LANE_ALIGN	FRAME_ALIGN	LINK_CONFIG_DIS	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	FORCE_K	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 107. Register 73 Field Descriptions

Bit	Field	Type	Reset	Description
15	IDLE_MODE	R/W	0h	0 = Idle mode disabled (normal operation) 1 = Device sends a continuous pattern (BC50h) on all lanes
14-13	0	R/W	0h	Must write 0
12	LANE_ALIGN	R/W	0h	0 = Character replacement disabled. Data are sent without inserting a lane alignment control character. 1 = If the last octet of the multiframe is the same as the last octet of the previous multiframe, then the last octet is replaced with a /K28.3/ character that can be used by the receiver for lane alignment monitoring and correction; see the JESD204B document., section 5.3.3.4 for details.
11	FRAME_ALIGN	R/W	0h	0 = Character replacement is disabled. Data are sent without inserting a frame alignment control character. 1 = If the last octet of the frame is the same as the last octet of the previous frame, then the octet is replaced with /K28.7/. Character replacement is not performed if a control character was already sent in the previous frame; see the JESD204B document., section 5.3.3.4 for details.
10	LINK_CONFIG_DIS	R/W	0h	0 = ILA transmission enabled. The initial lane alignment data are sent, as per section 5.3.3.5 and 8.3 of the JESD204B document. 1 = ILA transmission disabled. The device starts sending payload data immediately after the code group synchronization.
9-3	0	R/W	0h	Must write 0
2	FORCE_K	R/W	0h	0 = Value of K (number of frames per multiframe) minus 1 is automatically calculated and set 1 = Value of K (number of frames per multiframe) minus 1 is set by the K_VALUE_TO_FORCE register setting
1-0	0	R/W	0h	Must write 0

12.2.1.3 Register 74 (address = 4Ah)

Figure 154. Register 74

15	14	13	12	11	10	9	8
LINK_LAYER_TESTMODES			TX_SYNC_REQ	RELEASE_ILA		0	JESD_RESET2
R/W-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
JESD_RESET3	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 108. Register 74 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	LINK_LAYER_TESTMODES	R/W	0h	000 = Normal operation 001 = D21.5 (1010101010) is transmitted on all lanes 010 = /K28.5/ is transmitted on all lanes 011 = ILA sequence is continuously transmitted on all lanes 100 = Pseudo-random pattern of 120 bits is transmitted on all lanes All other combinations are invalid.
12	TX_SYNC_REQ	R/W	0h	0 = Sync reinitialization request disabled (normal operation) 1 = A stream of /K28.5/ symbols are transmitted, requesting link reinitialization. After transmission, the /K28.5/ characters enter into a link initialization state; see section 5.3.3.7 of the JESD204B document for further details.
11-10	RELEASE_ILA	R/W	0h	000 = Default value The value of this register determines the LMFC edge that the transmitter enters in the ILA phase from the code group synchronization. This setting is useful for adjusting the deterministic latency value; see the *Data Link Layer* section.
9	0	R/W	0h	Must write 0
8	JESD_RESET2	R/W	0h	0 = SYNC~ and SYSREF events reset the phase of JESD and non-JESD blocks (demodulator, test pattern generator, and clock dividers) 1 = SYNC~ and SYSREF events do not reset the phase of JESD block and clock dividers but do reset the phase of the demodulator and test pattern generator
7	JESD_RESET3	R/W	0h	0 = SYNC~ and SYSREF events reset the phase of JESD and non-JESD blocks (demodulator, test pattern generator, and clock dividers) 1 = Immediately after setting this bit to 1, the first SYNC~ and SYSREF event resets the phase of the JESD and non-JESD blocks. Subsequent SYNC~ and SYSREF events do not reset the phase of the JESD block and clock dividers but do reset the phase of the demodulator and test pattern generator.
6-0	0	R/W	0h	Must write 0

12.2.1.4 Register 75 (address = 4Bh)

Figure 155. Register 75

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	SING_CONV_PER_OCT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
NUM_ADC_PER_LANE			0	0	0	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 109. Register 75 Field Descriptions

Bit	Field	Type	Reset	Description
15-9	0	R/W	0h	Must write 0
8	SING_CONV_PER_OCT	R/W	0h	0 = Data are packed efficiently and transmitted over the link 1 = Each ADC data are packed in two octets [that is, each ADC data are transmitted as 16 bits (12-, 14-, and 16-bit mode) by the appropriate zero padding]; see the *User Data Format* section for further details.
7-5	NUM_ADC_PER_LANE	R/W	0h	000 = Four ADCs per lane mode: data from four ADCs are packed into a lane. Four lanes are active and four lanes are powered down. 001 = Eight ADCs per lane mode: data from eight ADCs are packed into a lane. Two lanes are active and six lanes are powered down. 100 = Two ADCs per lane mode: data from two ADCs are packed into a lane. All eight lanes are active. All other settings are invalid.
4-0	0	R/W	0h	Must write 0

12.2.1.5 Register 77 (address = 4Dh)

Figure 156. Register 77

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PRE_EMP				0	0	0	0
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 110. Register 77 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	0	R/W	0h	Must write 0
7-4	PRE_EMP	R/W	0h	The extra current during pre-emphasis is equal to the decimal equivalent of the programmed value multiplied by 0.25 mA. A value corresponding to 0 refers to no pre-emphasis.
3-0	0	R/W	0h	Must write 0

12.2.1.6 Register 80 (address = 50h)

Figure 157. Register 80

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	INC_JESD_VDD	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 111. Register 80 Field Descriptions

Bit	Field	Type	Reset	Description
15-2	0	R/W	0h	Must write 0
1	INC_JESD_VDD	R/W	0h	0 = Default value for the internal LDO driving the JESD PLL 1 = Increased value for the internal LDO driving the JESD PLL
0	0	R/W	0h	Must write 0

12.2.1.7 Register 81 (address = 51h)

Figure 158. Register 81

15	14	13	12	11	10	9	8
DEVICE_ID							
R/W-0h							
7	6	5	4	3	2	1	0
0	0	0	BANK_ID				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 112. Register 81 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	DEVICE_ID	R/W	0h	These bits force the device ID value.
7-5	0	R/W	0h	Must write 0
4-0	BANK_ID	R/W	0h	These bits force the bank ID value.

12.2.1.8 Register 82 (address = 52h)

Figure 159. Register 82

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SCR_EN	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 113. Register 82 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	0	R/W	0h	Must write 0
7	SCR_EN	R/W	0h	0 = Scrambler disabled 1 = Scrambler enabled; see the *Scrambler* section for further details
6-0	0	R/W	0h	Must write 0

12.2.1.9 Register 83 (address = 53h)

Figure 160. Register 83

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	K_VALUE_TO_FORCE				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 114. Register 83 Field Descriptions

Bit	Field	Type	Reset	Description
15-5	0	R/W	0h	Must write 0
4-0	K_VALUE_TO_FORCE	R/W	0h	Specifies the value of K (number of frames per multiframe) minus 1 to be forced when the FORCE_K bit is set to 1.

12.2.1.10 Register 85 (address = 55h)

Figure 161. Register 85

15	14	13	12	11	10	9	8
JESD_SUBCLASS			0	0	0	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
JESD_VER			0	0	0	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 115. Register 85 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	JESD_SUBCLASS	R/W	0h	000 = Subclass 0 001 = Subclass 1 010 = subclass 2 See the JESD Version and Subclass section for further details.
12-8	0	R/W	0h	Must write 0
7-5	JESD_VER	R/W	0h	000 = JESD204A 001 = JESD204B See the JESD Version and Subclass section for further details.
4-0	0	R/W	0h	Must write 0

12.2.1.11 Register 115 (address = 73h)

Figure 162. Register 115

15	14	13	12	11	10	9	8
EN_LANE_ID1	EN_LANE_ID2	EN_LANE_ID3	EN_LANE_ID4	EN_CHECKSUM_LANE1	EN_CHECKSUM_LANE2	EN_CHECKSUM_LANE3	EN_CHECKSUM_LANE4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	ENABLE_JESD_VER_CONTROL	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 116. Register 115 Field Descriptions

Bit	Field	Type	Reset	Description
15	EN_LANE_ID1	R/W	0h	0 = Lane 1 default ID (00001) is set 1 = Lane 1 default ID (00001) can be forced with register 118, bits 12-8
14	EN_LANE_ID2	R/W	0h	0 = Lane 2 default ID (00010) is set 1 = Lane 2 default ID (00010) can be forced with register 118, bits 4-0
13	EN_LANE_ID3	R/W	0h	0 = Lane 3 default ID (00011) is set 1 = Lane 3 default ID (00011) can be forced with register 119, bits 12-8
12	EN_LANE_ID4	R/W	0h	0 = Lane 4 default ID (00100) is set 1 = Lane 4 default ID (00100) can be forced with register 119, bits 4-0
11	EN_CHECKSUM_LANE1	R/W	0h	0 = The default checksum value is calculated by the device 1 = Checksum value (FCHK field in Table 15) is forced from register 116, bits 15-8
10	EN_CHECKSUM_LANE2	R/W	0h	0 = The default checksum value is calculated by the device 1 = Checksum value (FCHK field in Table 15) is forced from register 116, bits 7-0
9	EN_CHECKSUM_LANE3	R/W	0h	0 = The default checksum value is calculated by the device 1 = Checksum value (FCHK field in Table 15) is forced from register 117, bits 15-8
8	EN_CHECKSUM_LANE4	R/W	0h	0 = The default checksum value is calculated by the device 1 = Checksum value (FCHK field in Table 15) is forced from register 117, bits 7-0
7-5	0	R/W	0h	Must write 0
4	ENABLE_JESD_VER_CONTROL	R/W	0h	0 = The device is in JESD204B, subclass 1 mode 1 = JESD version and subclass can be changed; see the Table 15 section for further details.
3-0	0	R/W	0h	Must write 0

12.2.1.12 Register 116 (address = 74h)

Figure 163. Register 116

15	14	13	12	11	10	9	8
CHECK_SUM1							
R/W-0h							
7	6	5	4	3	2	1	0
CHECK_SUM2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 117. Register 116 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	CHECK_SUM1	R/W	0h	These bits determine the lane 1 checksum value; see register 135.
7-0	CHECK_SUM2	R/W	0h	These bits determine the lane 2 checksum value; see register 135.

12.2.1.13 Register 117 (address = 75h)

Figure 164. Register 117

15	14	13	12	11	10	9	8
CHECK_SUM3							
R/W-0h							
7	6	5	4	3	2	1	0
CHECK_SUM4							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 118. Register 117 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	CHECK_SUM3	R/W	0h	These bits determine the lane 3 checksum value; see register 136.
7-0	CHECK_SUM4	R/W	0h	These bits determine the lane 4 checksum value; see register 136.

12.2.1.14 Register 118 (address = 76h)

Figure 165. Register 118

15	14	13	12	11	10	9	8
0	0	0	LANE_ID1				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
0	0	0	LANE_ID2				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 119. Register 118 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	0	R/W	0h	Must write 0
12-8	LANE_ID1	R/W	0h	These bits determine the lane 1 ID value; see register 137.
7-5	0	R/W	0h	Must write 0
4-0	LANE_ID2	R/W	0h	These bits determine the lane 2 ID value; see register 137.

12.2.1.15 Register 119 (address = 77h)

Figure 166. Register 119

15	14	13	12	11	10	9	8
0	0	0	LANE_ID3				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
0	0	0	LANE_ID4				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 120. Register 119 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	0	R/W	0h	Must write 0
12-8	LANE_ID3	R/W	0h	These bits determine the lane 3 ID value; see register 138.
7-5	0	R/W	0h	Must write 0
4-0	LANE_ID4	R/W	0h	These bits determine the lane 4 ID value; see register 138.

12.2.1.16 Register 120 (address = 78h)

Figure 167. Register 120

15	14	13	12	11	10	9	8
FORCE_LMFC_COUNT	LMFC_COUNTER_INIT_VALUE					0	0
R/W-0h	R/W-0h					R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 121. Register 120 Field Descriptions

Bit	Field	Type	Reset	Description
15	FORCE_LMFC_COUNT	R/W	0h	0 = Default value 1 = The LMFC counter value is forced, as per register 120, bits 14-10.
14-10	LMFC_COUNTER_INIT_VALUE	R/W	0h	These bits specify the initial value of the LMFC counter. This option is useful when the multiframe size must be different than the default value; see the *Synchronization Using SYNC~ and SYSREF* section.
9-0	0	R/W	0h	Must write 0

12.2.1.17 Register 134 (address = 86h)

Figure 168. Register 134

15	14	13	12	11	10	9	8
EN_LANE_ID5	EN_LANE_ID6	EN_LANE_ID7	EN_LANE_ID8	EN_CHECKSUM_LANE5	EN_CHECKSUM_LANE6	EN_CHECKSUM_LANE7	EN_CHECKSUM_LANE8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

(1) This register is valid when JESD_WR_SEL (register 3, bit 5) is 1.

Table 122. Register 134 Field Descriptions

Bit	Field	Type	Reset	Description
15	EN_LANE_ID5	R/W	0h	0 = Lane 5 default ID (00101) is set 1 = Lane 5 default ID (00101) can be forced with register 137, bits 12-8
14	EN_LANE_ID6	R/W	0h	0 = Lane 6 default ID (00110) is set 1 = Lane 6 default ID (00110) can be forced with register 137, bits 4-0
13	EN_LANE_ID7	R/W	0h	0 = Lane 7 default ID (00111) is set 1 = Lane 7 default ID (00111) can be forced with register 138, bits 12-8
12	EN_LANE_ID8	R/W	0h	0 = Lane 8 default ID (01000) is set 1 = Lane 8 default ID (01000) can be forced with register 138, bits 4-0
11	EN_CHECKSUM_LANE5	R/W	0h	0 = Default checksum value calculated by device 1 = Checksum value (FCHK field in Table 15) from register 135, bits 15-8
10	EN_CHECKSUM_LANE6	R/W	0h	0 = The default checksum value is calculated by the device 1 = Checksum value (FCHK field in Table 15) from register 135, bits 7-0
9	EN_CHECKSUM_LANE7	R/W	0h	0 = The default checksum value is calculated by the device 1 = Checksum value (FCHK field in Table 15) from register 135, bits 15-8
8	EN_CHECKSUM_LANE8	R/W	0h	0 = The default checksum value is calculated by the device 1 = Checksum value (FCHK field in Table 15) from register 135, bits 7-0
7-0	0	R/W	0h	Must write 0

12.2.1.18 Register 135 (address = 87h)

Figure 169. Register 135

15	14	13	12	11	10	9	8
CHECK_SUM5							
R/W-0h							
7	6	5	4	3	2	1	0
CHECK_SUM6							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 123. Register 135 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	CHECK_SUM5	R/W	0h	These bits determine the lane 5 checksum value.
7-0	CHECK_SUM6	R/W	0h	These bits determine the lane 6 checksum value.

12.2.1.19 Register 136 (address = 88h)

Figure 170. Register 136

15	14	13	12	11	10	9	8
CHECK_SUM7							
R/W-0h							
7	6	5	4	3	2	1	0
CHECK_SUM8							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 124. Register 136 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	CHECK_SUM7	R/W	0h	These bits determine the lane 7 checksum value.
7-0	CHECK_SUM8	R/W	0h	These bits determine the lane 8 checksum value.

12.2.1.20 Register 137 (address = 89h)

Figure 171. Register 137

15	14	13	12	11	10	9	8
0	0	0	LANE_ID5				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
0	0	0	LANE_ID6				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 125. Register 137 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	0	R/W	0h	Must write 0
12-8	LANE_ID5	R/W	0h	These bits determine the lane 5 ID value.
7-5	0	R/W	0h	Must write 0
4-0	LANE_ID6	R/W	0h	These bits determine the lane 6 ID value.

12.2.1.21 Register 138 (address = 8Ah)

Figure 172. Register 138

15	14	13	12	11	10	9	8
0	0	0	LANE_ID7				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
0	0	0	LANE_ID8				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 126. Register 138 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	0	R/W	0h	Must write 0
12-8	LANE_ID7	R/W	0h	These bits determine the lane 7 ID value.
7-5	0	R/W	0h	Must write 0
4-0	LANE_ID8	R/W	0h	These bits determine the lane 8 ID value.

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

CDCE72010 Data Sheet, SCAS858

CDCM7005 Data Sheet, SCAS793

LMK048X Data Sheet, SNAS605

SN74AUP1T04 Data Sheet, SCES800

Clocking High-Speed Data Converters, SLYT075

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

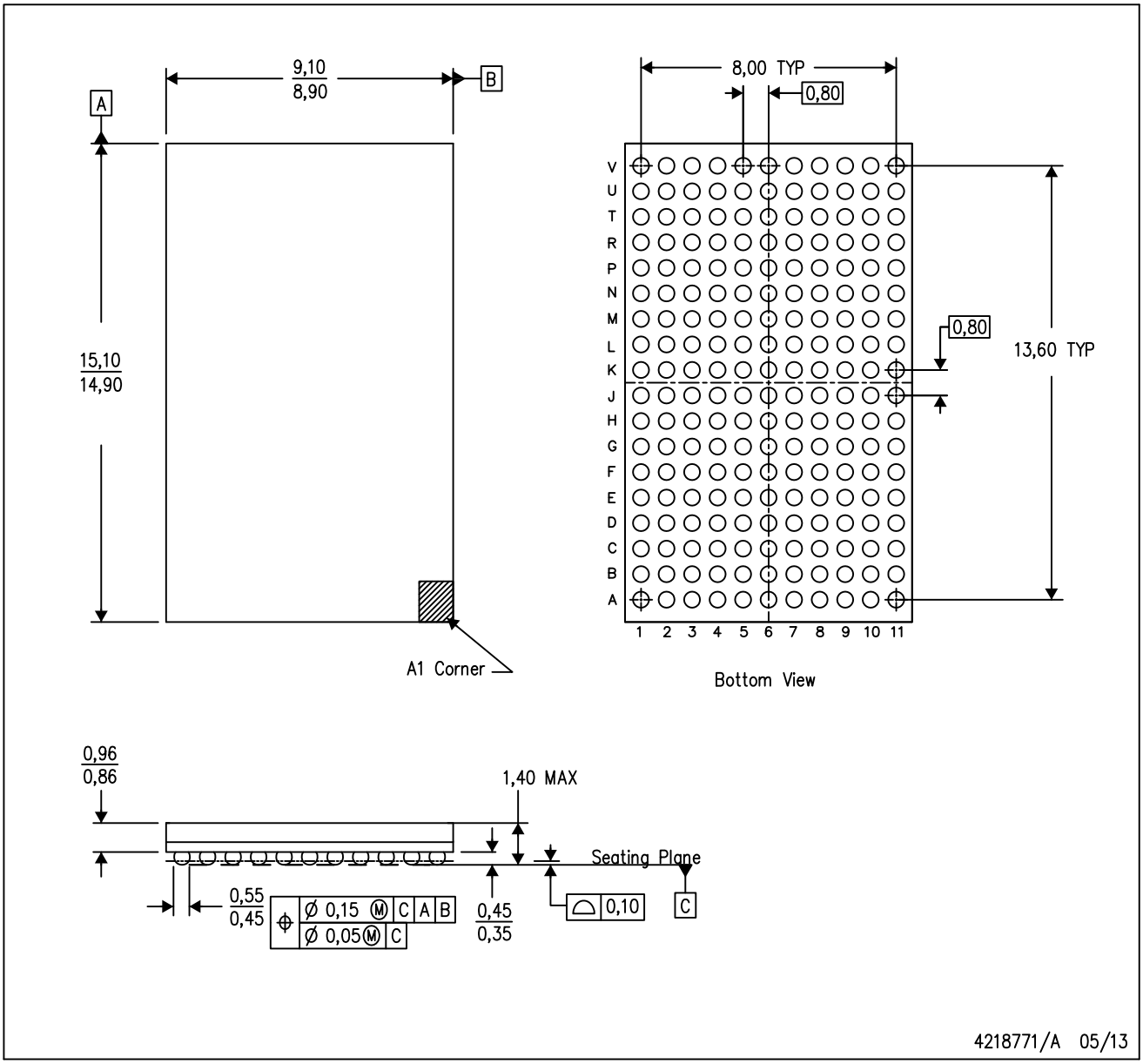
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

MECHANICAL DATA

ZZE (R–PBGA–N198) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS52J90ZZE	ACTIVE	NFBGA	ZZE	198	160	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS52J90	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

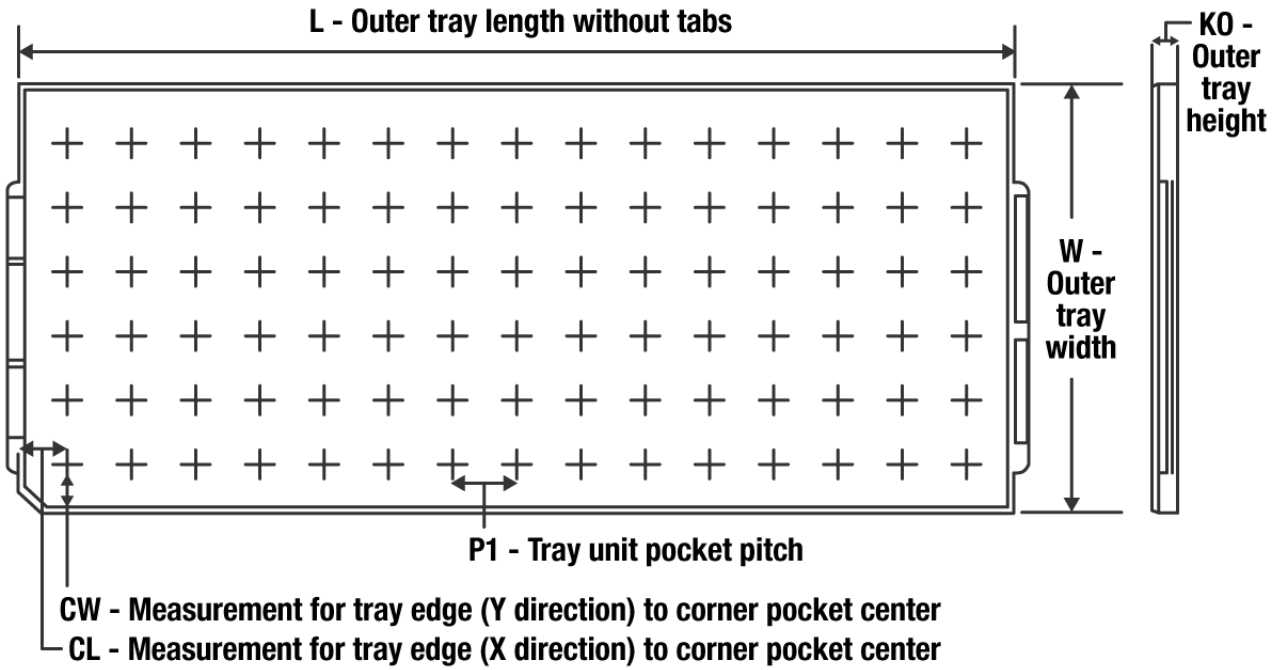
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS52J90ZZE	ZZE	NFBGA	198	160	10 x 16	150	315	135.9	7620	19.2	13.5	10.35

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