MIC68401

4A Sequencing LDO with Tracking and Ramp Control™

General Description

The MIC68401 is a high peak current LDO regulator designed specifically for powering applications such as FPGA core voltages that require high startup current with lower nominal operating current. Capable of sourcing 4A of current for start-up, the MIC68401 provides high power from a small QFN package. The MIC68401 can also implement a variety of power-up and power-down protocols such as sequencing, tracking, and ratiometric tracking.

The MIC68401 operates from a wide input range of 1.65V to 5.5V, which includes all of the main supply voltages commonly available today. It is designed to drive digital circuits requiring low voltage at high currents (i.e., PLDs, DSPs, microcontrollers, etc.). The MIC68401 incorporates a delay pin (DELAY) for control of power-on-reset (POR) output at turn-on. In addition, there is a ramp control (RC) for either tracking applications or output voltage slew rate control at turn-on. These features are important in applications where the load is highly capacitive and inrush currents can cause supply voltages to fail and microprocessors or other complex logic chips to hang up.

Multiple MIC68401s can be "daisy chained" in two modes. In tracking mode the output voltage of the master drives the RC pin of a slave so that the slave tracks the main regulator during turn-on and turn-off. In sequencing mode the POR of the master drives the enable (EN) of the slave so that it turns on after the master. This behavior is critical for power-up control in multi-output power supplies. The MIC68401 is fully protected offering both thermal, current limit protection, and reverse current protection.

The MIC68401 has an adjustable output voltage. The junction temperature range of part is rated from –40°C to +125°C. The MIC68401 is offered in the small 16-pin 4mm × 4mm QFN package.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

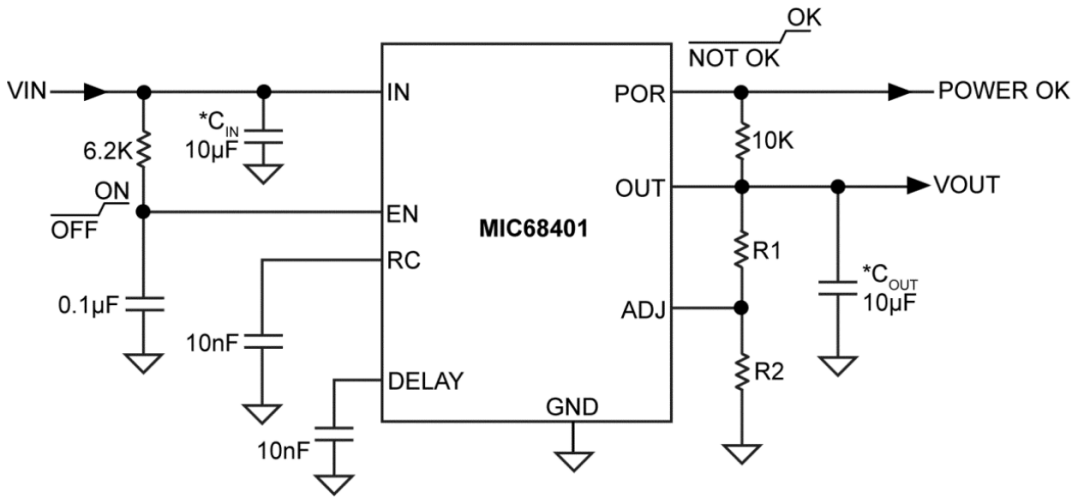
Features

- Stable with 10µF ceramic capacitor
- Input voltage range: 1.65V to 5.5V
- Low 0.5V reference voltage
- ±2.0% output tolerance over temperature
- 4A output current
- Timing-controlled sequencing on/off
- Programmable Ramp Control™ for inrush current limiting and slew rate control of the output voltage during turn-on
- Power-on-reset (POR) supervisor with programmable delay time
- Single master can control multiple slave regulators with tracking output voltages
- Small 4mm × 4mm QFN package
- Maximum dropout (V_{IN} – V_{OUT}) of 500mV over temperature at 3A output current
- Fixed and adjustable output voltages
- Excellent line and load regulation specifications
- Logic-controlled shutdown
- Thermal shutdown and current-limit protection

Applications

- FPGA/PLD power supply
- Networking/telecom equipment
- Microprocessor core voltage
- High-efficiency linear post regulator
- Sequenced or tracked power supply

Typical Application

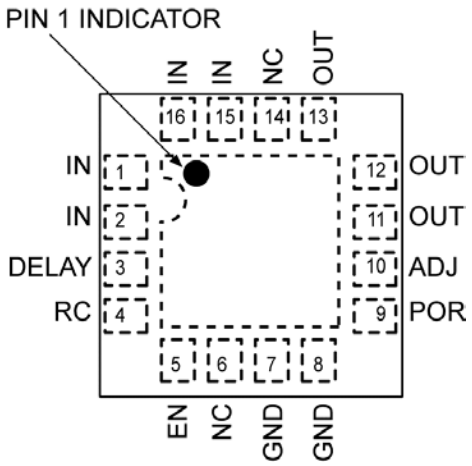


*MINIMUM CAPACITANCE. FOR GUIDANCE ON THE VALUE OF C_{IN} AND C_{OUT}, PLEASE REFER TO THE APPLICATIONS INFORMATION SECTION

Ordering Information

Part Number	Output Current	Output Voltage	Junction Temperature Range	Package
MIC68401YML	4.0A	Adjustable	–40°C to +125°C	16-Pin 4mm × 4mm QFN

Pin Configuration



16-Pin 4mm × 4mm QFN

Pin Description

Pin Number	Pin Name	Pin Function
1, 2, 15, 16	IN	Input: Input voltage supply pin. Connect a X7R type ceramic capacitor to ground to bypass the input supply. Use a minimum 10µF capacitance.
3	DELAY	Delay: A capacitor to ground sets the time of the internal delay timer. This timer delays the power-on reset (POR) output at turn-on.
4	RC	Ramp Control: May be voltage driven for tracking applications or a capacitor to ground will set the turn on slew rate of output voltage during start-up.
5	EN	Enable (Input): CMOS compatible input. Logic high = enable, logic low = shutdown.
6, 14	NC	Not internally connected.
7, 8, Tab	GND	Ground.
9	POR	Power-on-Reset: Open-drain output. When active, this output goes low impedance low, indicating that the output is out of regulation. High (open) means V_{OUT} is regulating within 10%. POR assertion can be delayed by using a single capacitor from the DELAY pin, to ground.
10 (ADJ)	ADJ	Feedback Input: Connect to resistor voltage divider from the OUT pin.
11, 12, 13	OUT	Output Voltage: Output of voltage regulator. Place capacitor to ground to bypass the output voltage. Minimum load current is 100µA. Nominal bypass capacitor is 10µF per amp of output current.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) 6V
Enable Input Voltage (V_{EN}) ..... –0.3V to V_{IN} + 0.3V
POR (V_{POR}) ..... –0.3V to 6V
RC ..... V_{IN} + 0.3V
Power Dissipation ..... Internally Limited[3]
Junction Temperature ..... –40°C ≤ T_J ≤ +125°C
Storage Temperature (T_S) ..... –65°C ≤ T_J ≤ +150°C
ESD Rating[4] 2kV

Operating Ratings[2]

Supply voltage (V_{IN}) ..... 1.65V to 5.5V
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}
POR (V_{POR}) ..... 0V to + 5.5V
Ramp Control (V_{RC}) ..... 0V to 5.5V
Junction Temperature Range ..... –40°C ≤ T_J ≤ +125°C
Package Thermal Resistance
4mm × 4mm QFN-16 (θ_{JA}) ..... 30°C/W

Electrical Characteristics[5]

T_A = 25°C with V_{IN} = V_{OUT} + 1V; V_{EN} = V_{IN}; I_{OUT} = 10mA; **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Voltage Accuracy	10mA < I_{OUT} < $I_{L(MAX)}$, V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V	**–2**		**+2**	%
Feedback Voltage	Adjustable version only	**0.49**	0.50	**0.51**	V
Feedback Current	Adjustable version only		20		nA
Output Voltage Line Regulation	V_{IN} = V_{OUT} + 1V to 5.0V		0.06	**0.5**	%
Output Voltage Load Regulation	I_L = 10mA to 3A		0.5	**1**	%
V_{IN} – V_O; Dropout Voltage	I_L = 1.5A I_L = 3.0A I_L = 4.0A		 300 360	**400** **500** **800**	mV
Ground Pin (GND) Current	I_L = 10mA I_L = 1.5A I_L = 3.0A I_L = 4.0A		1.2 20 55 90	 **130**	mA
Ground Pin (GND) Current in Shutdown	V_{EN} = <0.2V; V_{OUT} = 0V		0.01	**10**	µA
Current Limit	V_{OUT} = 0V; V_{IN} = 3.0V	**4.0**	6.0		A
Start-Up Time	V_{EN} = V_{IN}; C_{RC} = Open		35	**150**	µs
Enable Input					
Enable Input Threshold	Regulator enable Regulator shutdown	**1**		 **0.2**	V
Enable Hysteresis		**20**	120	**200**	mV
Enable Input Current	V_{IL} ≤ 0.2V (Regulator shutdown) V_{IH} ≥ 1V (Regulator enable)		0.02 3		µA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
5. Specification for packaged product only.

Electrical Characteristics[5] (Continued)

T_A = 25°C with V_{IN} = V_{OUT} + 1V; V_{EN} = V_{IN}; I_{OUT} = 10mA; **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted.

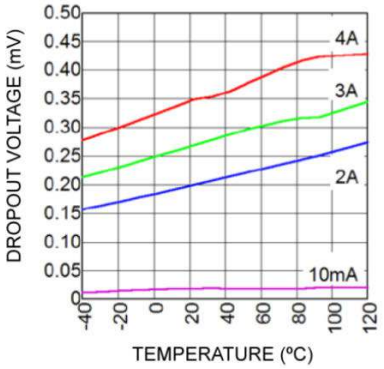
Parameter	Conditions	Min.	Typ.	Max.	Units
POR Output					
$I_{POR(LEAK)}$	POR pin inactive (open drain, high) V_{POR} = 5.5V			**1** **2**	µA
$V_{POR(LO)}$	POR pin active, output logic-low voltage I_{POR} = 1mA		60	**90**	mV
POR Threshold	V_{OUT} ramping up. % of V_{OUT} below nominal	**7.5**	10	**12.5**	%
POR Threshold Hysteresis	VOUT ramping down. Amount that the POR threshold shifts from the ramp up threshold, when it is ramping down.		2.5	**3**	%
DELAY Pin Current	V_{DELAY} = 0.75V	**0.7**	1	**1.3**	µA
DELAY Threshold Voltage[6]	V_{POR} = High	**1.185**	1.235	**1.285**	V
Ramp Control					
I_{RC}	Ramp Control Current (VRC = 0.75V)	**0.7**	1	**1.3**	µA
$I_{DISCHARGE}$[7]	V_{OUT} = 0.5V_{NOM}, V_{RAMP} = 0V	25	45	70	mA
Tracking Accuracy[8]	Measure (V_{OUT} – V_{RC} × (V_{TARGET} / 500mV))	–10	15	50	mV

Notes:

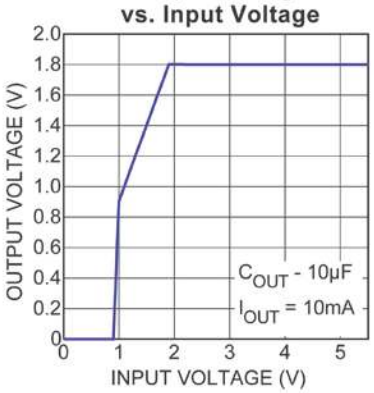
6. Timer high voltage along with DELAY pin current (1µA, nominal) determines the delay per µF of capacitance. Typical delay is 1.235sec/µF.
7. The discharge current ($I_{DISCHARGE}$), is the current drawn from the output to ground to actively discharge the output capacitor during the shutdown process.
8. V_{TARGET} is the desired output voltage.

Typical Characteristics

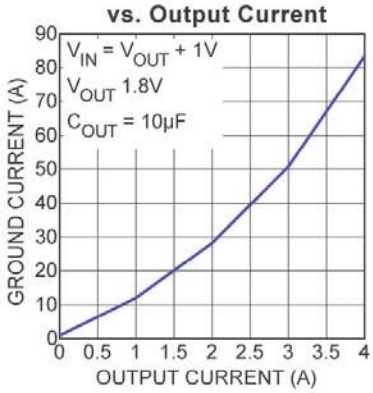
Dropout Voltage vs. Temperature



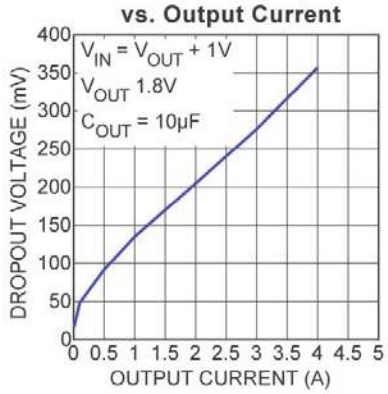
Output Voltage vs. Input Voltage



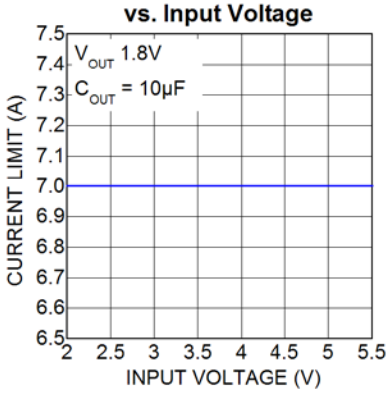
Ground Current vs. Output Current



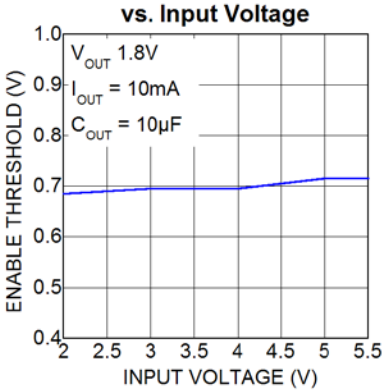
Dropout Voltage vs. Output Current



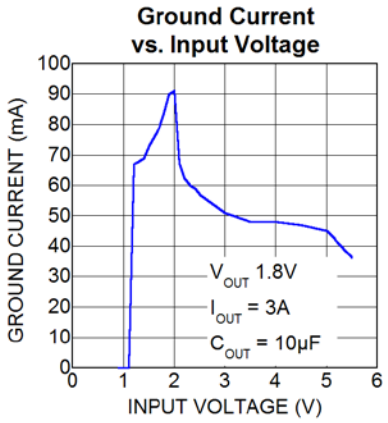
Current Limit vs. Input Voltage



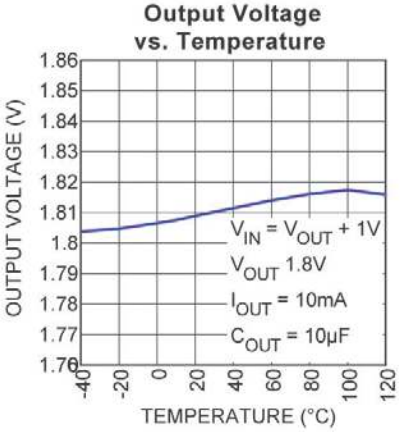
Enable Threshold vs. Input Voltage



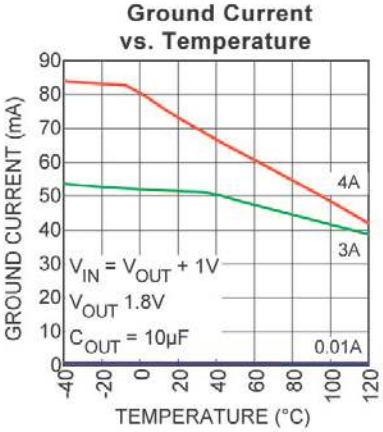
Ground Current vs. Input Voltage



Output Voltage vs. Temperature

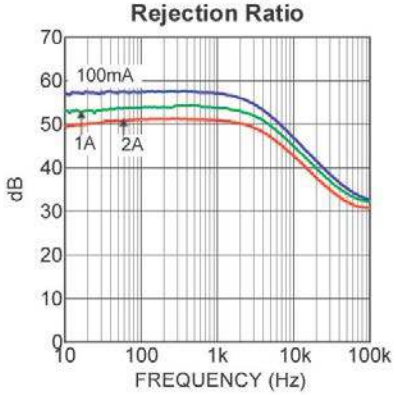


Ground Current vs. Temperature

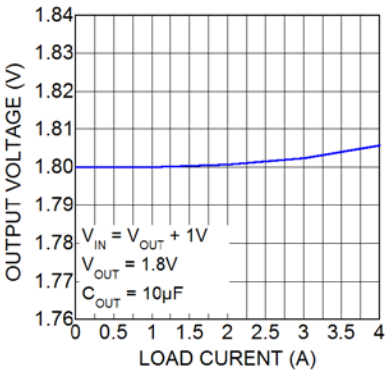


Typical Characteristics (Continued)

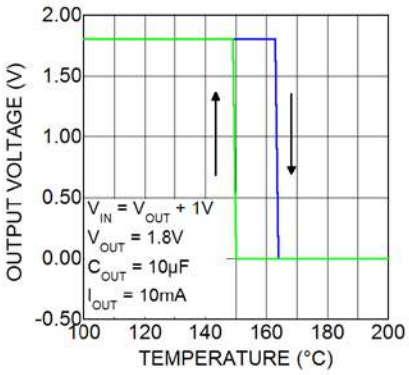
Power Supply Rejection Ratio



Load Regulation

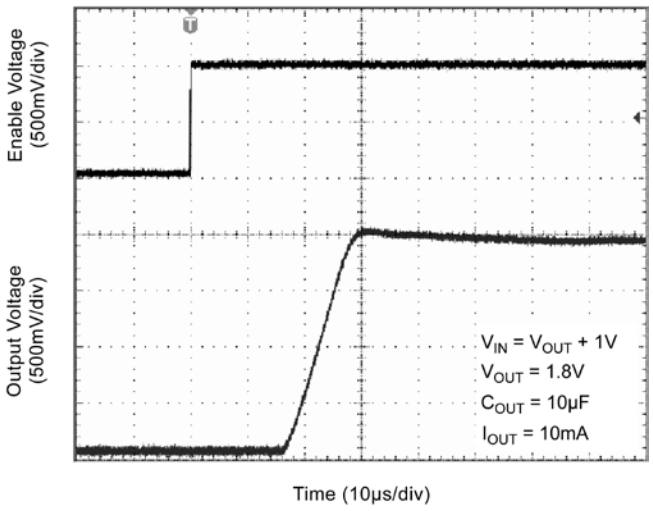


Thermal Shutdown

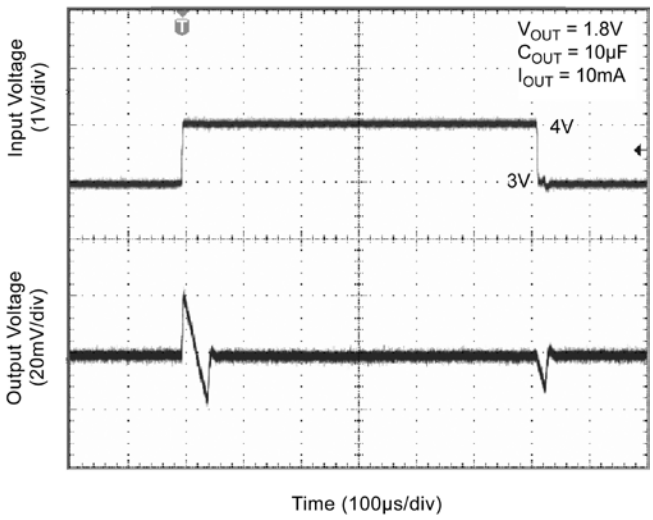


Functional Characteristics

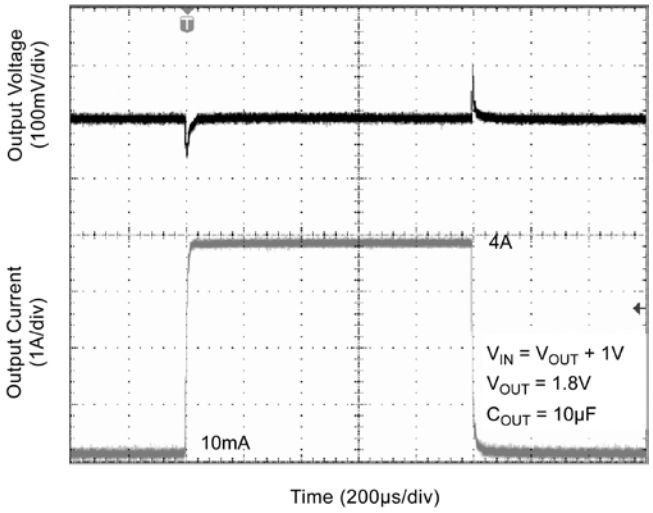
Enable Turn-On



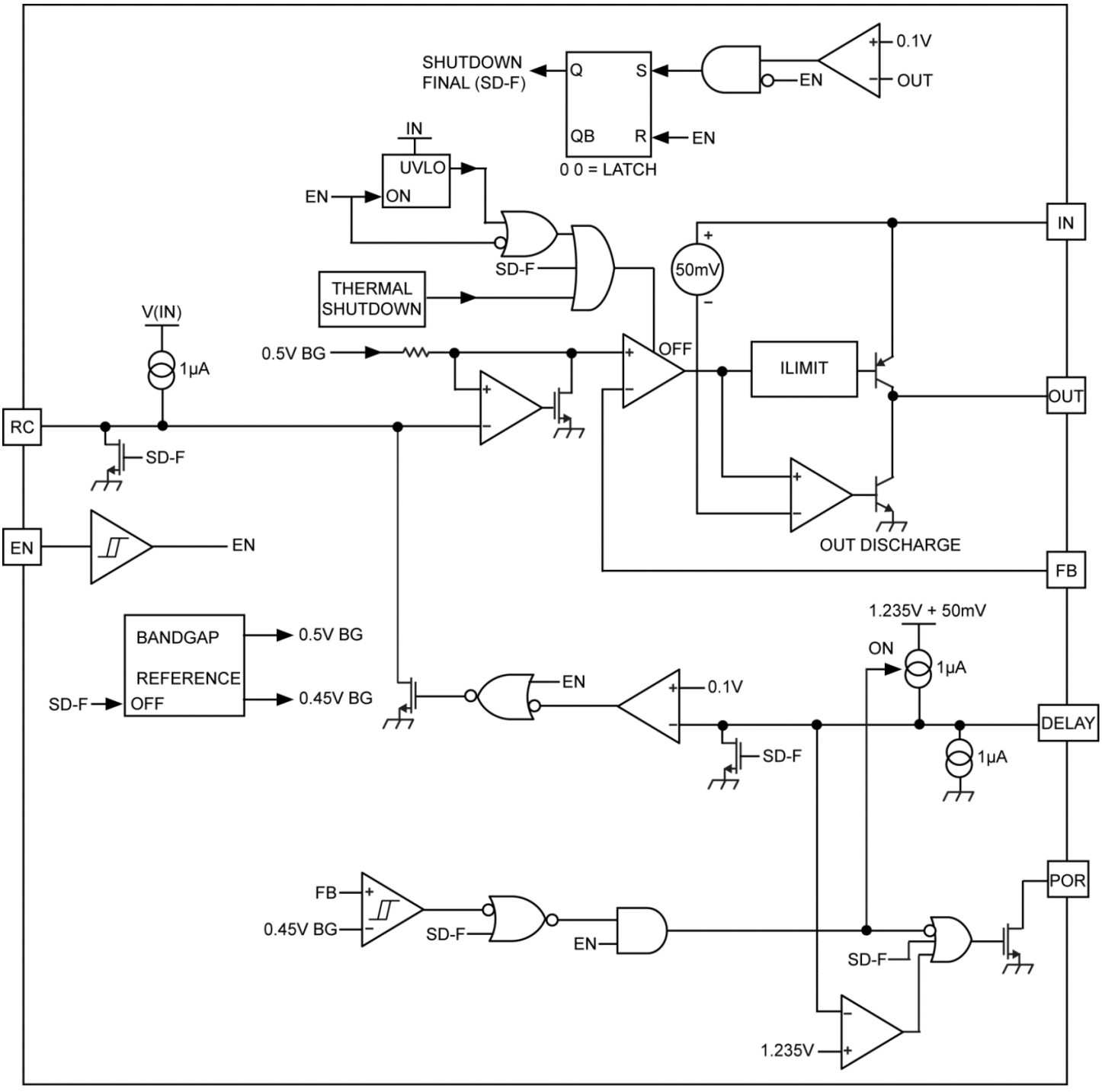
Line Transient



Load Transient



Functional Diagram



Application Information

Enable Input

The MIC68401 features a TTL/CMOS-compatible positive logic enable input for on/off control of the device. When the EN input is greater than 1V, it enables the regulator. When the EN input is less than 0.2V it will disable the regulator. In shutdown the regulator consumes very little current (only a few microamperes of leakage).

Input Capacitor

An input capacitor of 10µF or greater is recommended. The capacitor should be a ceramic X7R type, placed within 1 inch of the device. Larger values will help to improve ripple rejection by bypassing the regulator input, further improving the integrity of the output voltage. If the output capacitor is > 100µF, then the input capacitor should be 1/10 the value of the output capacitor in order to maintain stability during soft-start.

Output Capacitor

The MIC68401 requires an output capacitor for stable operation. As a µCap LDO, the MIC68401 can operate with ceramic output capacitors of 10µF or greater with ESR's ranging from a 3mΩ to 300mΩ. A general guideline for calculating the output capacitance is that it should be greater than 10 µF per amp of output current. At high frequencies, capacitor values greater than 10µF improves the transient response while reducing the noise on the output. X7R dielectric-type ceramic capacitors are recommended because of their superior temperature performance. The specific undershoot/overshoot performance will depend on both the values and ESR/ESL of the capacitors.

Adjustable Regulator Design

The MIC68401 output voltage can be programmed from 0.5V to 5.5V using a resistor divider from output to the ADJ pin. Typical sense input currents are less than 30nA which causes less than 0.3% error with R1 and R2 each less than or equal to 100kΩ. For large value resistors (>50KΩ) R1 should be bypassed by a small capacitor (C_{FF} = 0.1µF bypass capacitor) to avoid instability due to phase lag at the ADJ input.

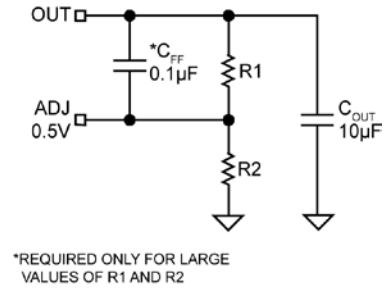


Figure 1. Adjustable Regulator with Resistors

The output resistor divider values are calculated by Equation 1:

$$V_{OUT} = 0.5V\left(\frac{R1}{R2}+1\right) \quad \text{Eq. 1}$$

Power-on-Reset (POR)

The power-on reset output pin (POR) is an open-drain N-Channel device that requires a pull-up resistor to a voltage source. POR is usually connected to the output voltage (OUT pin). Once the voltage on the internal timer (DELAY pin) reaches 1.235V, the POR pin is asserted high. The delay period of the timer begins when the output voltage is within 10% of its nominal voltage; i.e., when the ADJ voltage level exceeds 0.45V. The POR pin is pulled low when enable (EN) is pulled low or if the output goes out of regulation by more than 10% due to loading conditions.

Delay (DELAY)

The MIC68401 is equipped with an internal timer that delays the assertion of the POR output. The delay is set by an external capacitor connected from the DELAY pin to ground. At turn-on, the delay time begins when the EN pin is high AND the output voltage is within 10% of its regulation value. Once the DELAY pin reaches 1.235V, the POR pin asserts high.

The turn on delay (TDLY) is calculated by Equation 2:

$$T_{DELAY} = (1.235V)\left(\frac{C_{DELAY}}{1\mu A}\right) \quad \text{Eq. 2}$$

Scale Factor is:

1.235 seconds/microfarad,

1.235 milliseconds/nanofarad, or

1.235 microseconds/picofarad.

T_{POR} is the time period from the rising of EN to the assertion (low-to-high transition) of the POR output, and is calculated by Equation 3:

$$T_{POR} = T_{DELAY} + T_{RC} \quad \text{Eq. 3}$$

Where: $T_{RC} = (0.45V)\left(\frac{C_{RC}}{1\mu A}\right)$

At turn off, the DELAY capacitor is discharged via a 1µA current sink when the EN pin is driven low.

Ramp Control

When the RC pin voltage is less than 0.5V, the output voltage is controlled by the voltage on the RC pin. When the RC pin voltage is greater than 0.5V, the output voltage is held in regulation by the FB pin. The RC capacitor is charged by an internal 1µA current source when the EN pin goes high and discharged by an N-channel when the EN pin is low and the output voltage is discharged below 0.1V. The size of the capacitor on the RC pin will control the slew rate of the output voltage during startup. The startup slew rate at the FB pin may be calculated from Equation 4:

$$T_{RC} = 0.5V\left(\frac{C_{RC}}{1\mu A}\right) \quad \text{Eq. 4}$$

Ramp Down – Turn Off Slew Rate

When the EN pin goes low, the output will begin to turn off within 5µs. The time that it takes for the output voltage to fully discharge to 0V is dependent upon the value of the output capacitor and the load current. In the absence of a load, the internal discharge current ($I_{DISCHARGE}$) will assure that the output voltage is discharged to 0V. The RC pin and the DELAY pin are quickly discharged through an internal N-channel pull down device when the EN pin goes low and the output voltage is discharged below 0.1V.

Sequencing Configurations

Sequencing allows a master device to control the start and stop timing of a single or multiple Slave MIC68401 devices. In a typical sequencing application, the master device POR output drives the slave EN inputs. The sequence begins with the master EN driven high. The master output ramps up and triggers the master DELAY. When the master output reaches 90% of its final value, the master POR is released which enables the Slave device(s).

Ratiometric Tracking

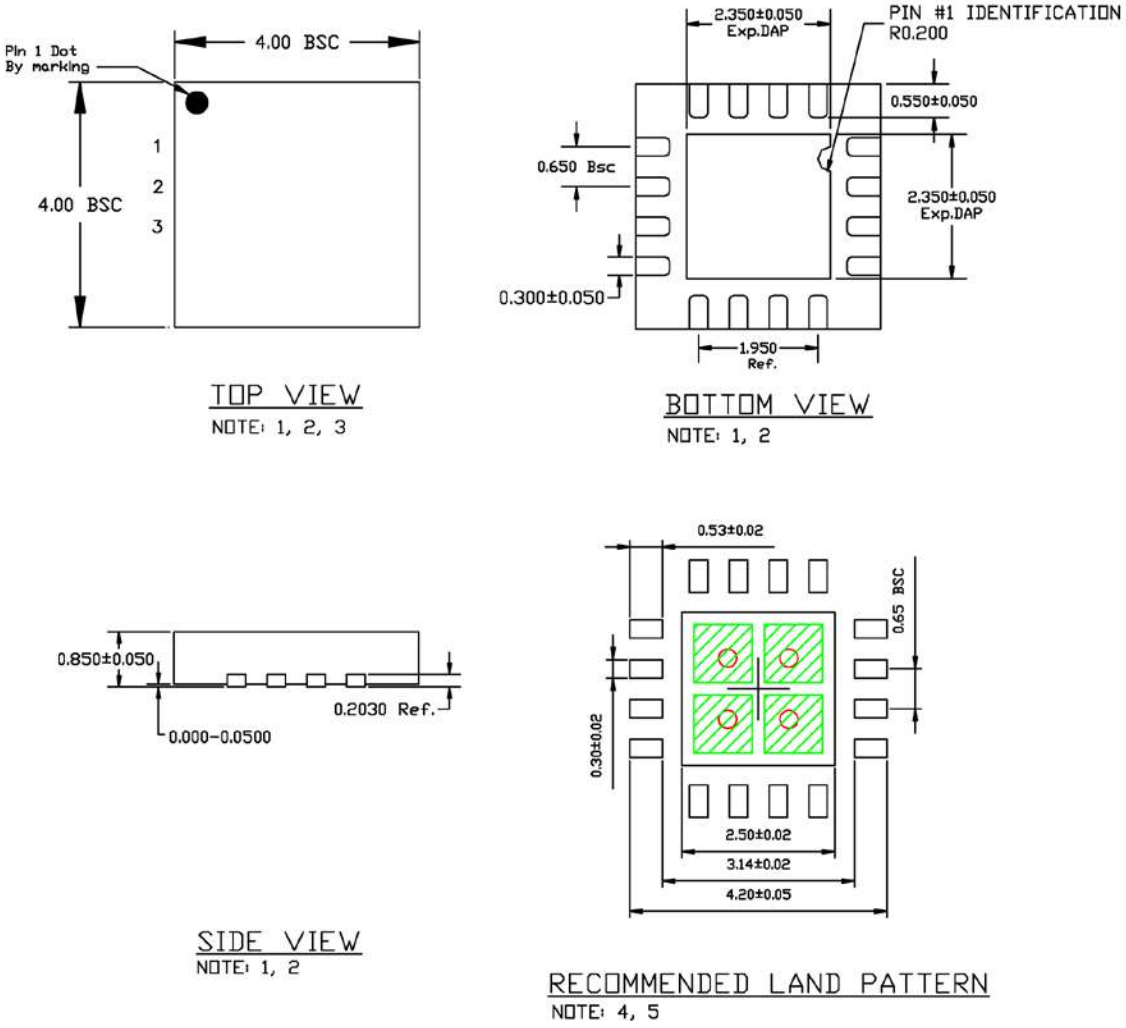
Ratiometric tracking allows independent ramping rates for multiple MIC68401 regulators, such that their final output voltages ramp up, and regulation occurs at the same time. This is accomplished by adding a resistor divider between the master output pin and the slave RC pin. The divider should be scaled such that the slave RC pin reaches or exceeds 0.5V when the master reaches its target output voltage.

Ratiometric tracking can also be accomplished by simply connecting the RC pins of the master and slave(s) together. When the RC pins are connected, the current from each of the MIC68401's RC pin current sources adds together. In order to maintain the desired slew rate, the RC capacitor size needs to be increased by the total number of RC pins that are connected together. For example: One master and two slaves will require three times the RC cap size as compared to a single device.

Final Note on Tracking

The MIC68401 does not fully shutdown until the output voltage is discharged below 100mV. If the RC is driven from an external source in a tracking configuration, and the external source does not go to zero on shutdown, it may prevent complete shutdown of the MIC68401. This will not cause damage to the device, but a higher quiescent will be drawn from the source. A potential cause for concern in battery operated portable equipment. When the RC pin is driven in tracking mode, pulling EN low will cause the output to turn-off. The MIC68401 cannot enter tracking mode unless EN is pulled high.

Package Information[9] and Recommended Landing Pattern



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. GREEN RECTANGLES (SHADED AREA) REPRESENT STENCIL OPENING ON EXPOSED AREA. SIZE IS 0.95X0.95MM, 1.15MM PITCH SPACING
5. RED CIRCLES REPRESENT THERMAL VIAS & SHOULD BE CONNECTED TO GND FOR MAX PERFORMANCE. 0.30 – 0.35 MM RECOMMENDED DIAMETER, 1.0MM PITCH SPACING

16-Pin 4mm × 4mm QFN (ML)

Note:

9. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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