TPS6132x 1.5-A to 4.1-A Multiple LED Camera Flash Driver With I²C Compatible Interface

1 Features

- Four Operational Modes
  - DC-Light and Flashlight
  - Voltage Regulated Converter: 3.8 V to 5.7 V
  - Standby: 2 μA (Typical)
- Storage Capacitor Friendly Solution
- Automatic V_F and ESR Calibration
- Power-Save Mode for Improved Efficiency at Low Output Power, Up to 95% Efficiency
- Output Voltage Remains Regulated When Input Voltage Exceeds Nominal Output Voltage
- I²C Compatible Interface up to 3.4 Mbps
- Dual Wire Camera Module Interface
- Zero Latency Tx-Masking Input
- LED Temperature Monitoring
- Privacy Indicator LED Output
- Integrated LED Safety Timer
- GPIO/Flash Ready Output
- Total Solution Size of Less Than 25 mm² (< 1-mm height)
- Available in a 20-Pin NanoFree™ (DSBGA)

2 Applications

- Single, Dual, or Triple White LED Flashlight Supply for Cell Phones and Smart-Phones
- LED Based Xenon Killer Flashlight

3 Description

The TPS6132x device is based on a high-frequency synchronous boost topology with constant current sinks to drive up to three white LEDs in parallel (445-mA, 890-mA, 445-mA maximum flash current). The extended high-current mode (HC_SEL) allows up to 1025-mA, 2050-mA, and 1025-mA flash current out of the storage capacitor.

The high-capacity storage capacitor on the output of the boost regulator provides the high-peak flash LED current, thereby reducing the peak current demand from the battery to a minimum.

The 2-MHz switching frequency allows the use of small and low profile 2.2-μH inductors. To optimize overall efficiency, the device operates with a 400-mV LED feedback voltage.

The TPS6132x device not only operates as a regulated current source, but also as a standard voltage boost regulator. The device keeps the output voltage regulated even when the input voltage exceeds the nominal output voltage. The device enters power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

To simplify DC-light and flashlight synchronization with the camera module, the device offers a dedicated control interface (STRB0 and STRB1 pins) for zero latency LED turnon time.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6132x	DSBGA (20)	2.20 mm × 1.96 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

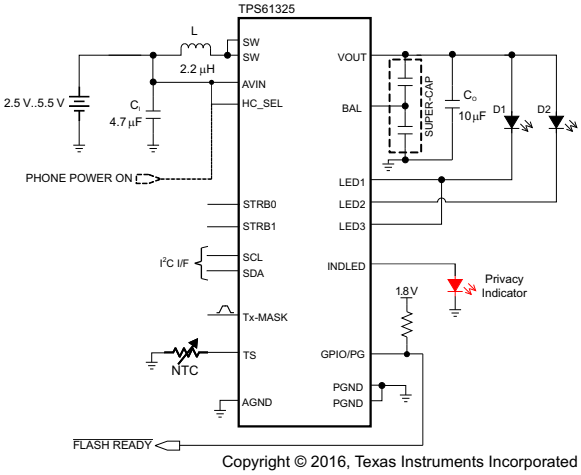


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2010) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed *Ordering Information Table* to *Device Comparison Table*; see POA at the end of the datasheet ... 1

Changes from Original (February 2010) to Revision A **Page**

- Added TPS61326 device as Product Preview ... 3
- Changed I_{STBY} specification, max value from 5 µA to 12 µA ... 5
- Changed V_{DO} specification, max. value from 200 mV to 250 mV for Test Condition I_{OUT} = –15.8 mA, T_J = 25°C, device not switching. ... 6

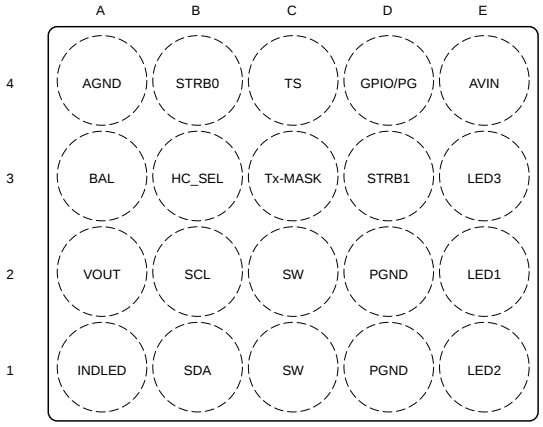
5 Device Comparison Table

PACKAGE MARKING	DEVICE SPECIFIC FEATURES(1)
TPS61325	Dual-Wire Camera Module Interface (STRB0 and STRB1) LED Temperature Monitoring Input (TS) Device I_2C Address = 0x33
TPS61326(2)	Dual-Wire Camera Module Interface (STRB0 and STRB1) LED Temperature Monitoring Input (TS) Device I_2C Address = 0x32

(1) For more details, see *Feature Description*.
(2) Device status is Product Preview. Contact TI for more details.

6 Pin Configuration and Functions

YFF Package
20-Pin DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	A4	—	Analog ground.
AVIN	E4	I	The input voltage pin of the device. Connect directly to the input bypass capacitor.
BAL	A3	O	Balancing output for dual cells super-capacitor. In steady-state operation, this output compensates for leakage current mismatch between the cells.
GPIO/PG	D4	I/O	This pin can be configured as a general purpose input and output pin (GPIO), an open-drain, or a push-pull output to signal when the converters output voltage is within the regulation limits (PG). The pin is configured as an open-drain power-good output by default.
HC_SEL	B3	I	Extended high-current mode selection input. This pin must not be left floating and must be terminated. HC_SEL = LOW: LED direct drive mode. The power stage is active and the maximum LED currents are defined as 445 mA, 890 mA, 445 mA. HC_SEL = HIGH: Energy storage mode. In flash mode, the power stage is either active with reduced current capability or disabled. The maximum LED current is defined as 1025 mA, 2050 mA, 1025 mA.
INDLED	A1	O	This pin provides a constant current source to drive low V_F LEDs. Connect to LED anode.
LED1	E2	I	LED return input. This feedback pin regulates the LED current through the internal sense resistor by regulating the voltage across it. The regulation operates with typically 400-mV (HC_SEL = L) or 400-mV (HC_SEL = H) dropout voltage. Connect to the cathode of the LEDs.
LED2	E1	I	
LED3	E3	I	
PGND	D1, D2	—	Power ground. Connect to AGND underneath IC.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
STRB0	B4	I	LEDx enable logic input. This pin can be used to enable and disable the high-power LEDs connected to the device. STRB0 = LOW: LEDx current regulators are turned off. STRB0 = HIGH: LED2, LED2 and LED3 current regulators are active. The LED current level (DC-light or flashlight current) is defined according to the STRB1 logic level.
STRB1	D3	I	LED current level selection input. Pulling this input high disables the DC-light watchdog timer. STRB1 = LOW: Flashlight mode is enabled. STRB1 = HIGH: DC-light mode is enabled.
SCL	B2	I	Serial interface clock line. This pin must not be left floating and must be terminated.
SDA	B1	I/O	Serial interface address and data line. This pin must not be left floating and must be terminated.
SW	C1, C2	I/O	Inductor connection. Drain of the internal power MOSFET. Connect to the switched side of the inductor. SW is high impedance during shutdown.
TS	C4	I/O	NTC resistor connection. This pin can be used to monitor the LED temperature. Connect a 220-kΩ NTC resistor from the TS input to ground. In case this functionality is not desired, the TS input must be tied to AVIN or left floating.
Tx-MASK	C3	I	RF PA synchronization control input.
VOUT	A2	O	This is the output voltage pin of the converter.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	AVIN, VOUT, SW, LED1, LED2, LED3, SCL, SDA, STRB0, STRB1, GPIO/PG, HC_SEL, Tx-MASK, TS, and BAL pins	–0.3	7	V
Current	GPIO/PG pin		±25	mA
Power dissipation		Internally limited		
Operating ambient temperature(3), T_A		–40	85	°C
Maximum operating junction temperature, $T_{J(MAX)}$			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage		2.5	3.6	5.5	V
V_{OUT}	Output voltage	Current regulation mode	V_{IN}		5.5	V
		Voltage regulation mode	3.825		5.7	
L	Inductor		1.3	2.2	2.9	µH
C_{IN}	Input capacitor		10			µF
C_{OUT}	Output capacitor (effective value)		3	10		µF

7.4 Thermal Information

THERMAL METRIC(1)		TPS61325 YFF (DSBGA) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Unless otherwise noted the specification applies for V_{IN} = 3.6 V over an operating junction temp. –40°C ≤ T_J ≤ 125°C; Circuit in *Parameter Measurement Information* (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.5		5.5	V
I_Q	Operating quiescent current into AVIN	I_{OUT} = 0 mA, device not switching, –40°C ≤ T_J ≤ 85°C		590	700	µA
		$I_{OUT(DC)}$ = 0 mA, PWM operation V_{OUT} = 4.95 V, voltage regulation mode		11.3		mA
I_{SD}	Shutdown current	HC_SEL = 0, –40°C ≤ T_J ≤ 85°C		1	5	µA
I_{STBY}	Standby current	HC_SEL = 1, storage capacitor balanced –40°C ≤ T_J ≤ 85°C		2	12	µA
	Precharge current	0 V ≤ V_{OUT} ≤ 3.3 V, device in precharge mode, –40°C ≤ T_J ≤ 85°C	80	180	220	mA
	Precharge termination threshold	V_{OUT} rising, –40°C ≤ T_J ≤ 85°C		3.35	3.6	V
	Precharge hysteresis (referred to V_{OUT})		40	75		mV
V_{UVLO}	Undervoltage lockout threshold (analog circuitry)	V_{IN} falling		2.3	2.4	V
OUTPUT						
V_{OUT}	Output voltage range	Current regulation mode	VIN		5.5	V
		Voltage regulation mode	3.825		5.7	
	Internal feedback voltage accuracy	2.5 V ≤ V_{IN} ≤ 4.8 V, –20°C ≤ T_J ≤ 125°C Boost mode, PWM voltage regulation	–2%		2%	
	Power-save mode ripple voltage	I_{OUT} = 10 mA		0.015 V_{OUT}		V_{P-P}
OVP	Output overvoltage protection	V_{OUT} rising, 0000 ≤ OV ≤ 0100	4.5	4.65	4.8	V
		V_{OUT} rising, 0101 ≤ OV ≤ 1111	5.8	6	6.2	
	Output overvoltage protection hysteresis	V_{OUT} falling, 0101 ≤ OV ≤ 1111		0.15		V

Electrical Characteristics (continued)

Unless otherwise noted the specification applies for V_{IN} = 3.6 V over an operating junction temp. –40°C ≤ T_J ≤ 125°C; Circuit in *Parameter Measurement Information* (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Switch MOSFET on-resistance		V_{OUT} = V_{GS} = 3.6 V		90		mΩ
	Rectifier MOSFET on-resistance		V_{OUT} = V_{GS} = 3.6 V		135		mΩ
$I_{lkg(SW)}$	Leakage into SW		V_{OUT} = 0 V, SW = 3.6 V, –40°C ≤ T_J ≤ 85°C		0.3	4	µA
I_{lim}	Rectifier valley current limit (open-loop)		V_{OUT} = 4.95 V, HC_SEL = 0, –20°C ≤ T_J ≤ 85°C, PWM operation, ILIM bit = 0	775	1150	1600	mA
			V_{OUT} = 4.95 V, HC_SEL = 0, –20°C ≤ T_J ≤ 85°C, PWM operation, ILIM bit = 1	1050	1600	2225	
			V_{OUT} = 4.95 V, HC_SEL = 1, Tx-MASK = 0, –20°C ≤ T_J ≤ 85°C, PWM operation, ILIM bit = 0	–85	30	150	
			V_{OUT} = 4.95 V, HC_SEL = 1, Tx-MASK = 0, –20°C ≤ T_J ≤ 85°C, PWM operation, ILIM bit = 1	175	250	300	
OSCILLATOR							
f_{OSC}	Oscillator frequency				1.92		MHz
f_{ACC}	Oscillator frequency			–10%		7%	
THERMAL SHUTDOWN, HOT DIE DETECTOR							
	Thermal shutdown			140	160		°C
	Thermal shutdown hysteresis				20		°C
	Hot die detector accuracy			–8		8	°C
LED CURRENT REGULATOR							
	LED1 and LED3 current accuracy	HC_SEL = 0	0.4 V ≤ $V_{LED1/3}$ ≤ 2 V, 0 mA < $I_{LED1/3}$ ≤ 111 mA, T_J = 85°C	–10%		10%	
			0.4 V ≤ V_{LED2} ≤ 2 V, $I_{LED1/3}$ > 111 mA, T_J = 85°C	–7.5%		7.5%	
	LED2 current accuracy		0.4 V ≤ V_{LED2} ≤ 2 V, 0 mA < I_{LED2} ≤ 250 mA, T_J = 85°C	–10%		10%	
			0.4 V ≤ V_{LED2} ≤ 2 V, I_{LED2} > 250 mA, T_J = 85°C	–7.5%		7.5%	
	LED1 and LED3 current accuracy	HC_SEL = 1	0.4 V ≤ $V_{LED1/3}$ ≤ 2 V, 0 mA < $I_{LED1/3}$ ≤ 1027 mA, T_J = 85°C	–10%		10%	
	LED2 current accuracy		0.4 V ≤ V_{LED2} ≤ 2 V, 0 mA < I_{LED2} ≤ 2052 mA, T_J = 85°C	–10%		10%	
	LED1 and LED3 current matching	HC_SEL = 0	$V_{LED1/3}$ = 1 V, $I_{LED1/3}$ = 444 mA, T_J = 85°C	–7.5%		7.5%	
	LEDx current temperature coefficient				0.05		%/°C
	INDLED current accuracy		1.5 V ≤ (V_{IN} – V_{INDLED}) ≤ 2.5 V, 0000 ≤ INDC ≤ 0111, T_J = 25°C	–20%		20%	
	INDLED current temperature coefficient				0.04		%/°C
V_{DO}	LEDx sense voltage		I_{LEDx} = full-scale current, HC_SEL = 0		400		mV
	LEDx sense voltage		$I_{LED1/3}$ = full-scale current, HC_SEL = 1		400	450	
	VOUT dropout voltage		I_{OUT} = –15.8 mA, T_J = 25°C, device not switching			250	
	LEDx input leakage current		V_{LEDx} = V_{OUT} = 5 V, –40°C ≤ T_J ≤ 85°C		0.1	4	µA
	INDLED input leakage current		V_{INDLED} = 0 V, –40°C ≤ T_J ≤ 85°C		0.1	1	µA
STORAGE CAPACITOR ACTIVE CELL BALANCING							
	Active cell balancing circuitry quiescent current into VOUT		HC_SEL = 1, storage capacitor balanced –40°C ≤ T_J ≤ 85°C		1.7	3	µA
	Active cell balancing accuracy		(V_{OUT} – V_{BAL}) vs BAL voltage difference, Storage capacitor balanced HC_SEL = 1, V_{OUT} = 5.7 V	–100		100	mV
	BAL output drive capability		V_{OUT} = 4.95 V, Sink and source current	±10	±15		mA
	Active discharge resistor		HC_SEL = 0, device in shutdown mode VOUT to BAL and BAL to GND		0.85	1.5	kΩ
LED TEMPERATURE MONITORING							
$I_{O(TS)}$	Temperature sense current source		Thermistor bias current		23.8		µA
	TS resistance (warning temperature)		LEDWARN bit = 1, T_J ≥ 25°C	39	44.5	50	kΩ
	TS resistance (hot temperature)		LEDHOT bit = 1, T_J ≥ 25°C	12.5	14.5	16.5	kΩ

Electrical Characteristics (continued)

Unless otherwise noted the specification applies for V_{IN} = 3.6 V over an operating junction temp. –40°C ≤ T_J ≤ 125°C; Circuit in *Parameter Measurement Information* (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA, SCL, GPIO/PG, Tx-MASK, STRB0, STRB1, HC_SEL						
$V_{(IH)}$	High-level input voltage		1.2			V
$V_{(IL)}$	Low-level input voltage				0.4	V
$V_{(OL)}$	Low-level output voltage (SDA)	I_{OL} = 8 mA			0.3	V
	Low-level output voltage (GPIO)	DIR = 1, I_{OL} = 5 mA			0.3	
$V_{(OH)}$	High-level output voltage (GPIO)	DIR = 1, GPIOTYPE = 0, I_{OH} = 8 mA	V_{IN} - 0.4			V
$I_{(LKG)}$	Logic input leakage current	Input connected to VIN or GND, –40°C ≤ T_J ≤ 85°C		0.01	0.1	µA
R_{PD}	STRB0, STRB1 pull-down resistance	STRB0, STRB1 ≤ 0.4 V		350		kΩ
	Tx-MASK pull-down resistance	Tx-MASK ≤ 0.4 V		350		
	HC_SEL pull-down resistance	HC_SEL ≤ 0.4 V		350		
$C_{(IN)}$	SDA input capacitance	SDA = VIN or GND		9		pF
	SCL input capacitance	SCL = VIN or GND		4		
	GPIO/PG input capacitance	DIR = 0, GPIO/PG = VIN or GND		9		
	STRB0 input capacitance	STRB0 = VIN or GND		3		
	STRB1 input capacitance	STRB1 = VIN or GND		3		
	HC_SEL input capacitance	HC_SEL = VIN or GND		3.5		
	Tx-MASK input capacitance	Tx-MASK = VIN or GND		4		
TIMING						
	Start-up time	From shutdown into DC-light mode, HC_SEL = 0, I_{LED} = 111 mA		1.5		ms
	LED current settling time(1) triggered by a rising edge on STRB0	MODE_CTRL = 10, HC_SEL = 0, I_{LED2} = from 0 mA to 890 mA		400		µs
		MODE_CTRL = 10, HC_SEL = 1, I_{LED2} = from 0 mA to 2050 mA		16		
	LED current settling time(1) triggered by Tx-MASK	MODE_CTRL = 10, HC_SEL = 0 I_{LED2} = from 890 mA to 390 mA		15		µs

(1) Setting time to ±15% of the target value.

7.6 Timing Requirements

PARAMETER(1)		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	Standard mode		100	kHz
		Fast mode		400	kHz
		High-speed mode (write operation), C_B - 100-pF maximum		3.4	MHz
		High-speed mode (read operation), C_B - 100-pF maximum		3.4	MHz
		High-speed mode (write operation), C_B - 400-pF maximum		1.7	MHz
		High-speed mode (read operation), C_B - 400-pF maximum		1.7	MHz
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7		µs
		Fast mode	1.3		
t_{HD}, t_{STA}	Hold time (repeated) START condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7		µs
		Fast mode	1.3		µs
		High-speed mode, C_B - 100-pF maximum	160		ns
		High-speed mode, C_B - 400-pF maximum	320		ns

(1) Specified by design. Not tested in production.

Timing Requirements (continued)

PARAMETER[1]		TEST CONDITIONS	MIN	MAX	UNIT
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode, C_B - 100-pF maximum	60		ns
		High-speed mode, C_B - 400-pF maximum	120		ns
t_{SU}, t_{STA}	Setup time for a repeated START condition	Standard mode	4.7		µs
		Fast mode	600		ns
		High-speed mode	160		ns
t_{SU}, t_{DAT}	Data setup time	Standard mode	250		ns
		Fast mode	100		
		High-speed mode	10		
t_{HD}, t_{DAT}	Data hold time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		High-speed mode, C_B - 100-pF maximum	0	70	ns
		High-speed mode, C_B - 400-pF maximum	0	150	ns
t_{RCL}	Rise time of SCL signal	Standard mode	20 + (0.1 × C_B)	1000	ns
		Fast mode	20 + (0.1 × C_B)	300	
		High-speed mode, C_B - 100-pF maximum	10	40	
		High-speed mode, C_B - 400-pF maximum	20	80	
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT	Standard mode	20 + (0.1 × C_B)	1000	ns
		Fast mode	20 + (0.1 × C_B)	300	
		High-speed mode, C_B - 100-pF maximum	10	80	
		High-speed mode, C_B - 400-pF maximum	20	160	
t_{FCL}	Fall time of SCL signal	Standard mode	20 + (0.1 × C_B)	300	ns
		Fast mode	20 + (0.1 × C_B)	300	
		High-speed mode, C_B - 100-pF maximum	10	40	
		High-speed mode, C_B - 400-pF maximum	20	80	
t_{RDA}	Rise time of SDA signal	Standard mode	20 + (0.1 × C_B)	1000	ns
		Fast mode	20 + (0.1 × C_B)	300	
		High-speed mode, C_B - 100-pF maximum	10	80	
		High-speed mode, C_B - 400-pF maximum	20	160	
t_{FDA}	Fall time of SDA signal	Standard mode	20 + (0.1 × C_B)	300	ns
		Fast mode	20 + (0.1 × C_B)	300	
		High-speed mode, C_B - 100-pF maximum	10	80	
		High-speed mode, C_B - 400-pF maximum	20	160	
t_{SU}, t_{STO}	Setup time for STOP condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
C_B	Capacitive load for SDA and SCL			400	pF

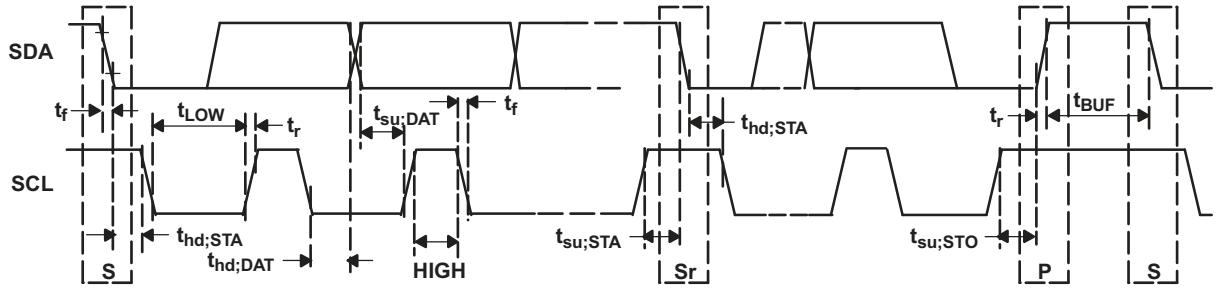
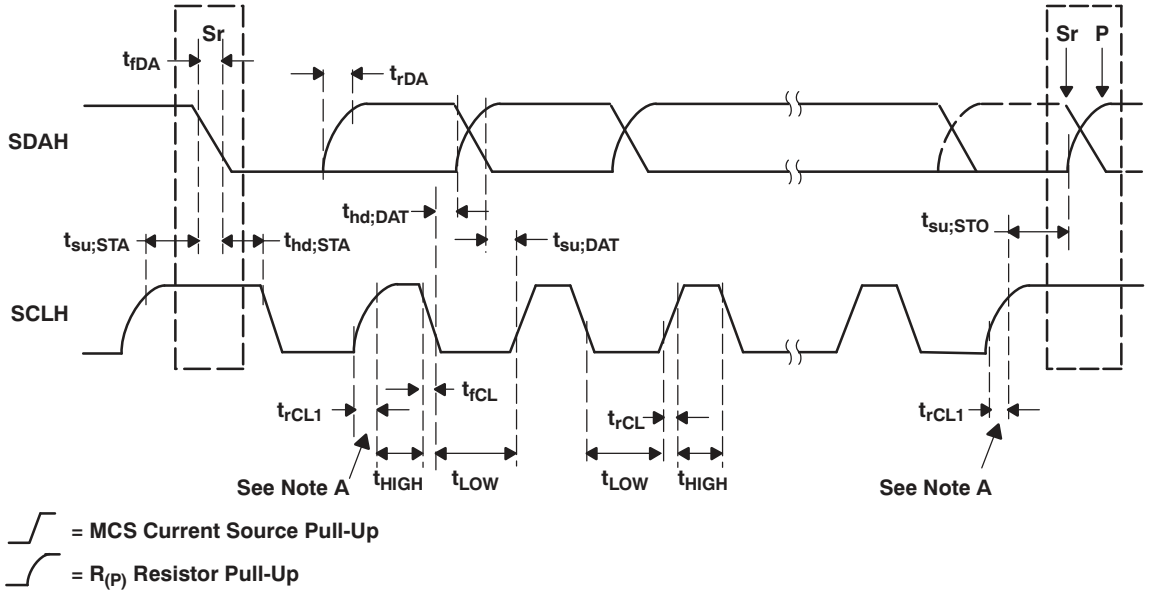


Figure 1. Serial Interface Timing for F/S-Mode



Note A: First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 2. Serial Interface Timing for H/S-Mode

7.7 Typical Characteristics

Table 1. Table of Graphs

GRAPH NAME		FIGURE NO.
LED Power Efficiency	vs Input Voltage	Figure 3, Figure 4
DC Input Current	vs Input Voltage	Figure 5
LED Current	vs LED Pin Headroom Voltage	Figure 6, Figure 7, Figure 8
LED Current	vs LED Current Digital Code	Figure 9, Figure 10, Figure 11, Figure 12
INDLED Current	vs LED Pin Headroom Voltage	Figure 13
Voltage Mode Efficiency	vs Output Current	Figure 14, Figure 15
DC Output Voltage	vs Output Current	Figure 16
	vs Input Voltage	Figure 17
Maximum Output Current	vs Input Voltage	Figure 18
DC Precharge Current	vs Differential Input-Output Voltage	Figure 19, Figure 20
Valley Current Limit		Figure 21, Figure 22
Balancing Current	vs Balance Pin Voltage	Figure 23
Supply Current	vs Input Voltage	Figure 24

Typical Characteristics (continued)

Table 1. Table of Graphs (continued)

GRAPH NAME		FIGURE NO.
Standby Current	vs Ambient Temperature	Figure 25
Temperature Detection Threshold		Figure 26, Figure 27

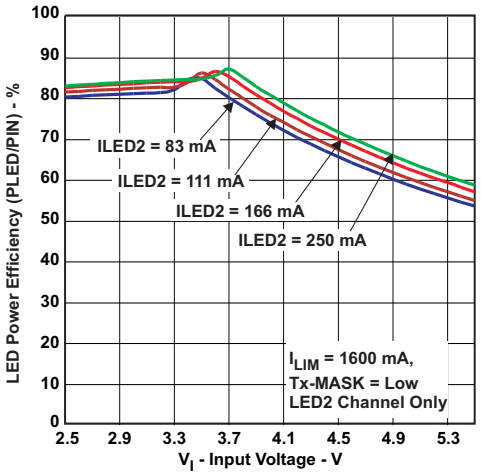


Figure 3. LED Power Efficiency vs Input Voltage

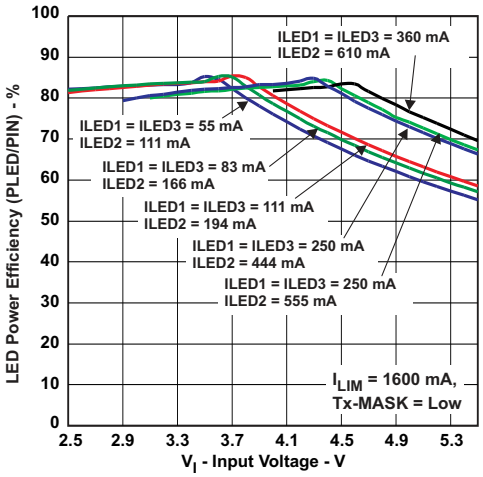


Figure 4. LED Power Efficiency vs Input Voltage

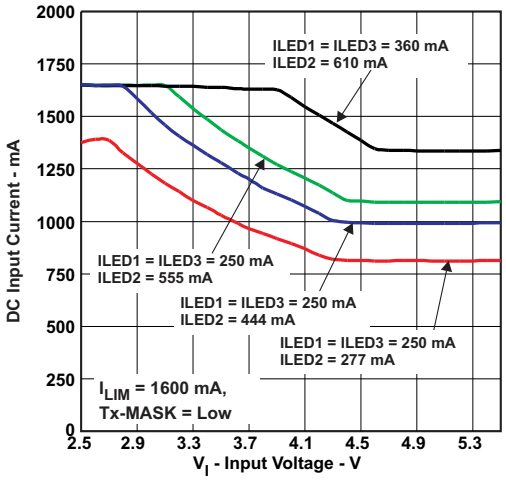


Figure 5. DC Input Current vs Input Voltage

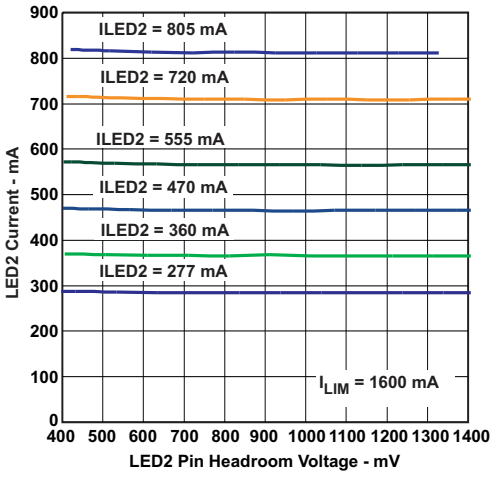


Figure 6. LED2 Current vs LED2 Pin Headroom Voltage (HC_SEL = 0)

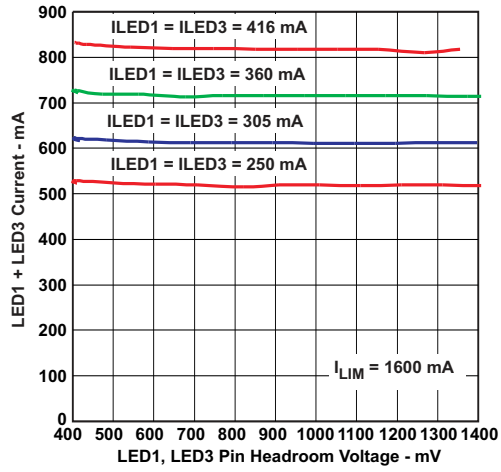


Figure 7. LED1 and LED3 Current vs LED1 and LED3 Pin Headroom Voltage (HC_SEL = 0)

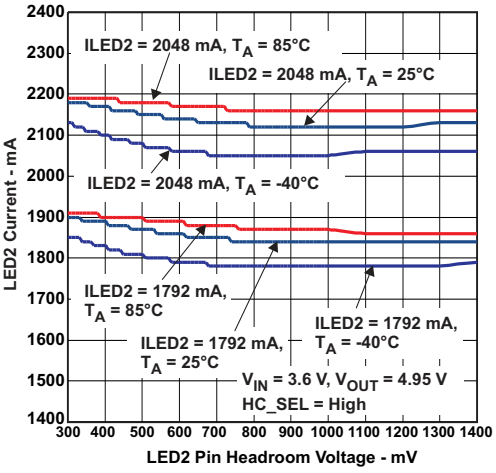


Figure 8. LED2 Current vs LED2 Pin Headroom Voltage (HC_SEL = 1)

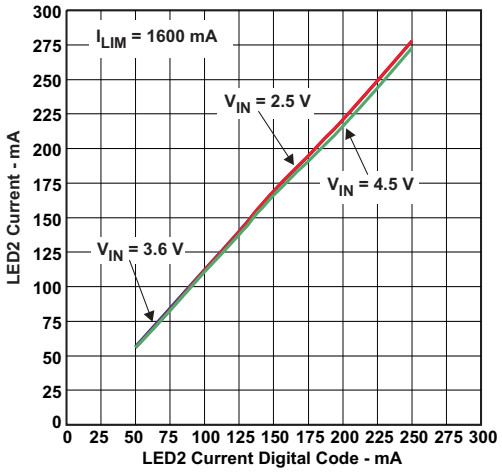


Figure 9. LED2 Current vs LED2 Current Digital Code (HC_SEL = 0)

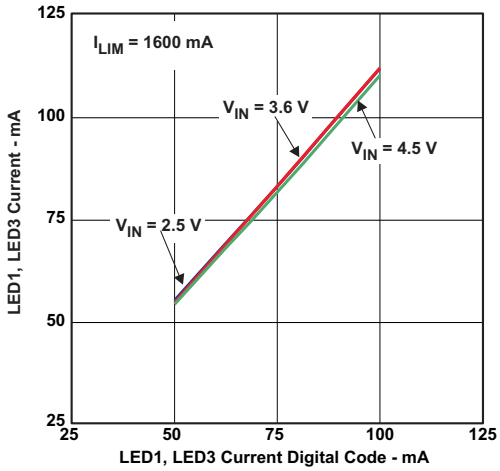


Figure 10. LED1 and LED3 Current vs LED1 and LED3 Current Digital Code (HC_SEL = 0)

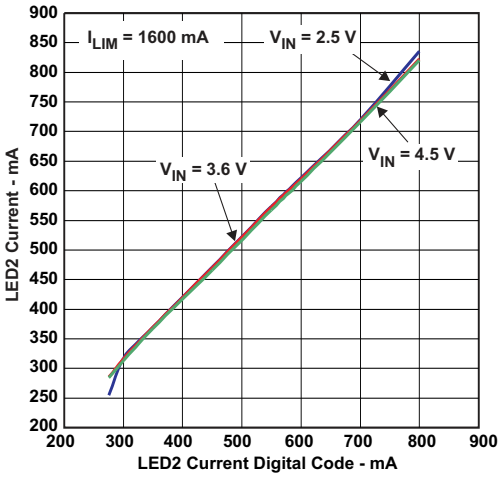


Figure 11. LED2 Current vs LED2 Current Digital Code (HC_SEL = 0)

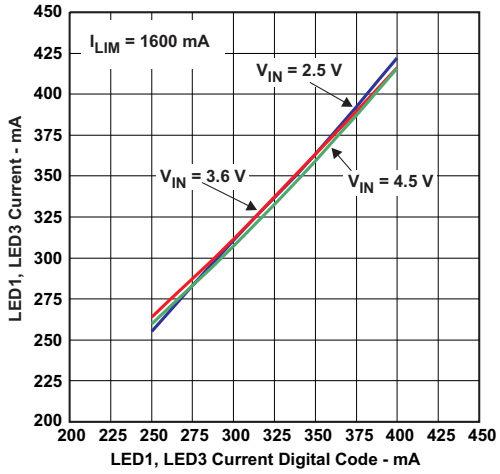


Figure 12. LED1 and LED3 Current vs LED1 and LED3 Current Digital Code (HC_SEL = 0)

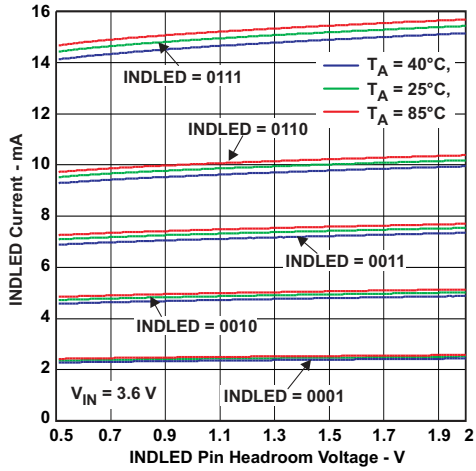


Figure 13. INDLED Current vs INDLED Pin Headroom Voltage

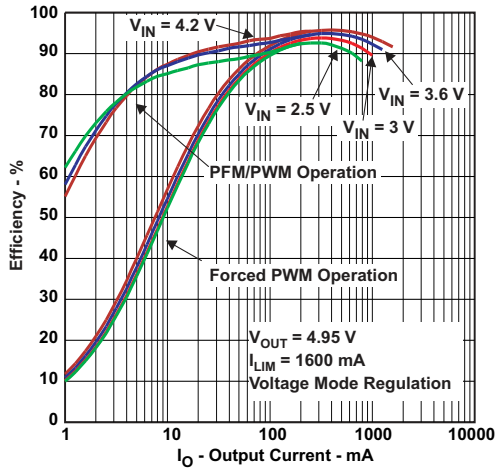


Figure 14. Efficiency vs Output Current

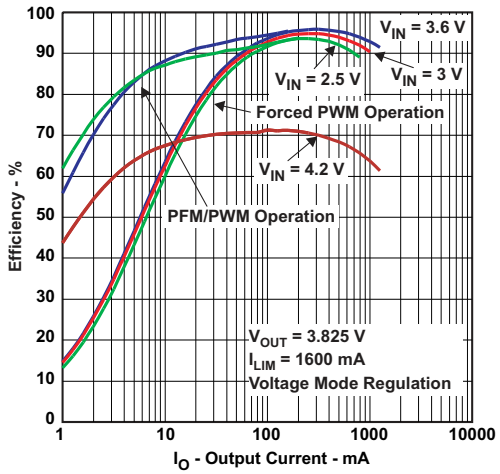


Figure 15. Efficiency vs Output Current

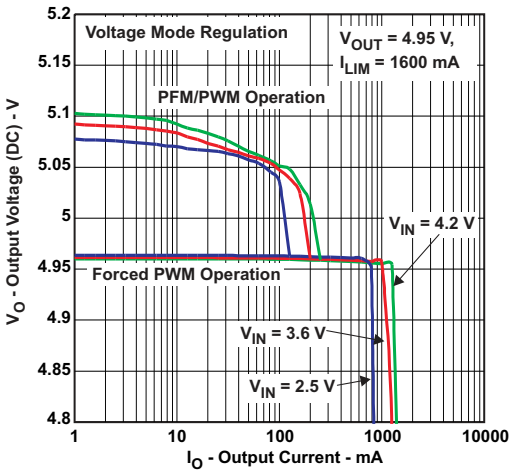


Figure 16. DC Output Voltage vs Load Current

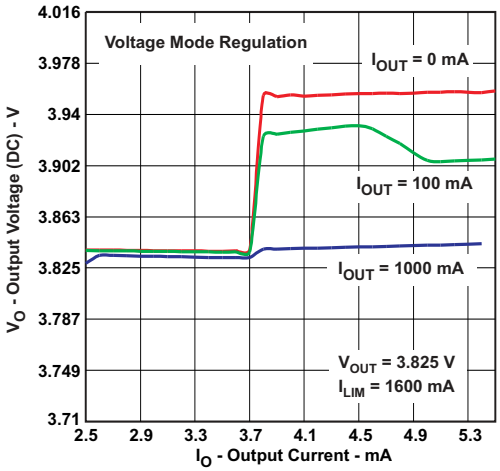


Figure 17. DC Output Voltage vs Input Voltage

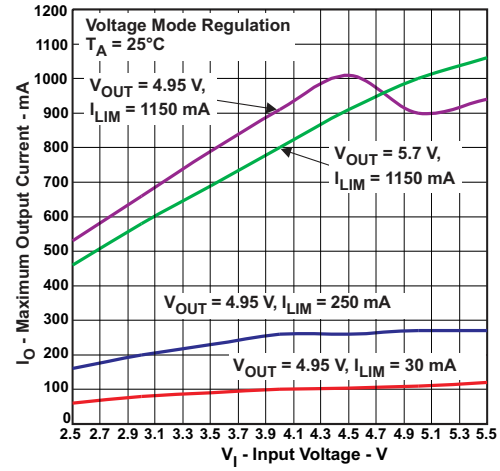


Figure 18. Maximum Output Current vs Input Voltage

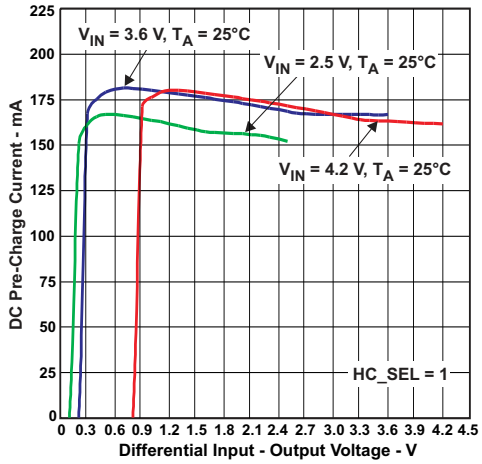


Figure 19. DC Precharge Current vs Differential Input-Output Voltage (HC_SEL = 1)

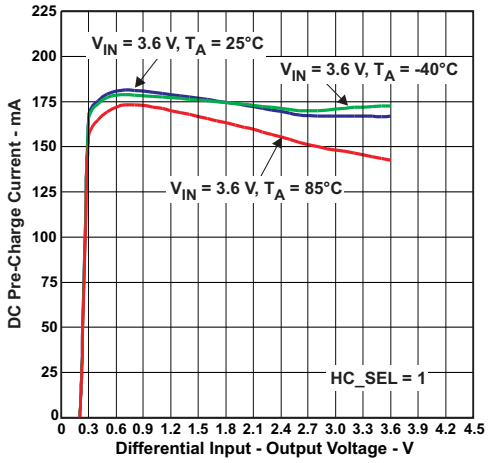


Figure 20. DC Precharge Current vs Differential Input-Output Voltage (HC_SEL = 1)

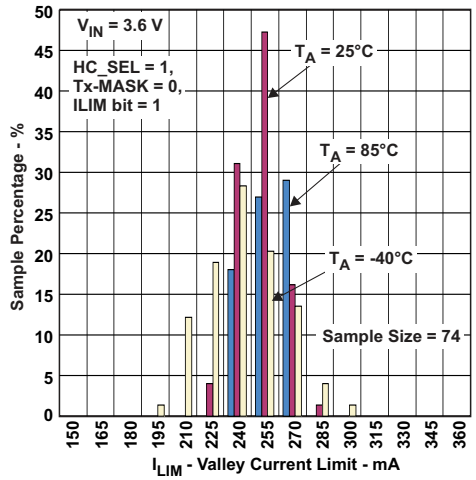


Figure 21. Valley Current Limit (HC_SEL = 1)

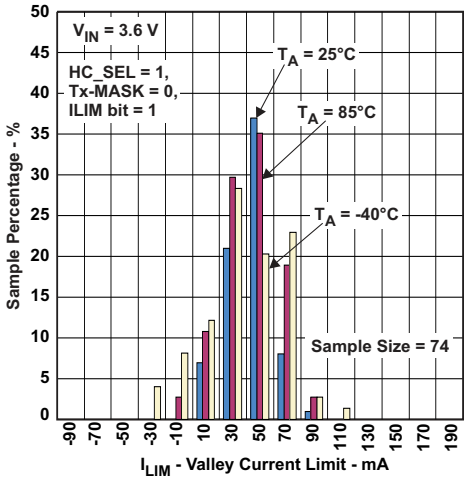


Figure 22. Valley Current Limit (HC_SEL = 1)

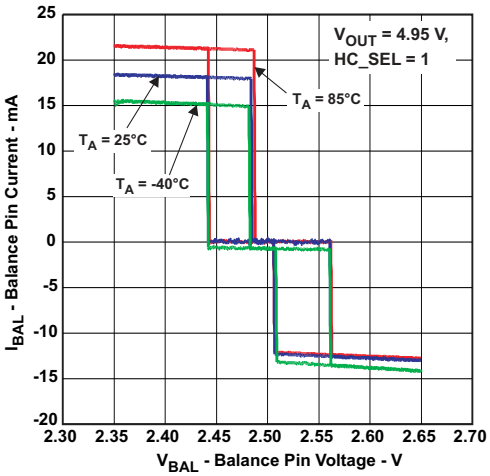


Figure 23. Balancing Current vs Balance Pin Voltage

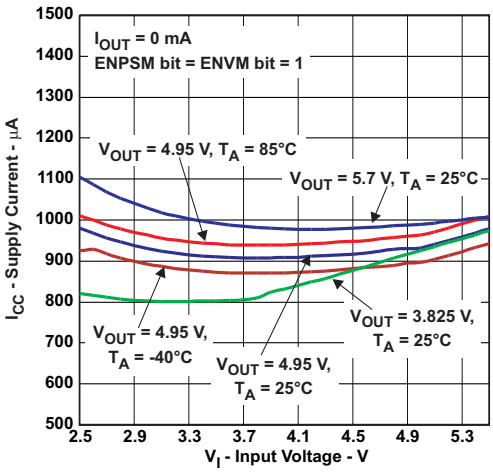


Figure 24. Supply Current vs Input Voltage

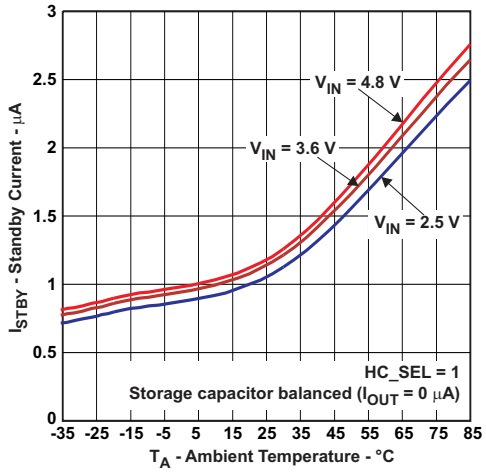


Figure 25. Standby Current vs Ambient Temperature (HC_SEL = 1)

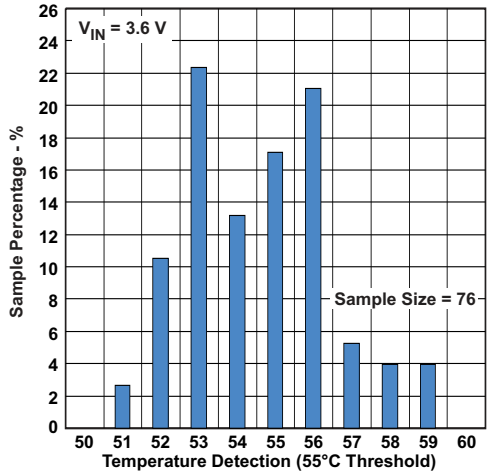


Figure 26. Temperature Detection Threshold

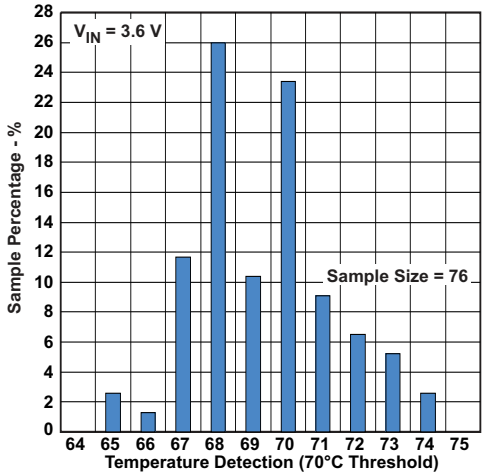


Figure 27. Temperature Detection Threshold

8 Parameter Measurement Information

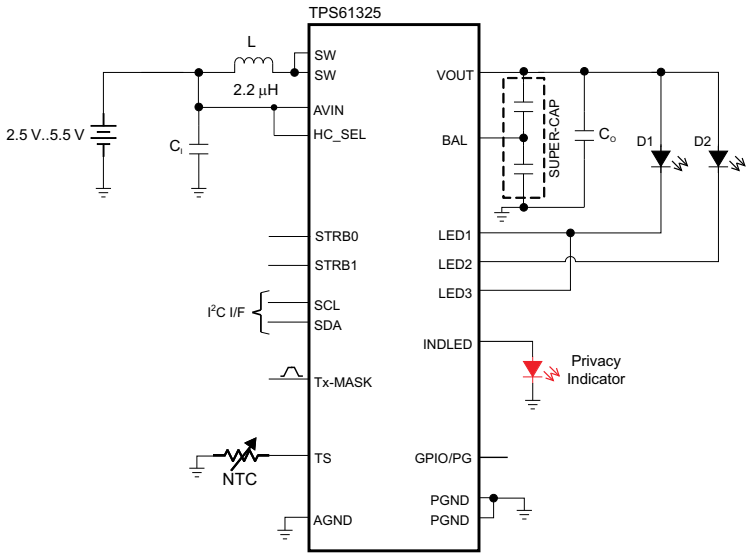


Figure 28. TPS61325 Typical Circuit

List of Components:
L = 2.2 µH, Wuerth Elektronik WE-TPC Series
C_I, C_O = 10 µF, 6.3 V X5R 0603 – TDK C1605X5R0J106MT
Storage Capacitor = TDK EDLC262020-500 mF
NTC = 220 kΩ, muRata NCP18WM224J03RB

9 Detailed Description

9.1 Overview

The TPS6132x family employs a 2-MHz fixed ON-time, PWM current-mode converter to generate the output voltage required to drive up to three high power LEDs in parallel. The device integrates a power stage based on an NMOS switch and a synchronous PMOS rectifier. The device also implements a set of linear low-side current regulators to control the LED current when the battery voltage is higher than the diode forward voltage.

A special circuit is applied to disconnect the load from the battery during shutdown of the converter. In conventional synchronous rectifier circuits, the back-gate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the back-gate diode of the high-side PMOS and disconnects it from the source when the regulator is in shutdown (HC_SEL = L).

The TPS6132x device cannot only operate as a regulated current source but also as a standard voltage boost regulator featuring power-save mode for improved efficiency at light load. Voltage mode operation can be enabled and disabled by software control.

The TPS6132x device also supports storage capacitor on its output (energy storage mode). In this operating mode (HC_SEL = H), the inductive power stage is used to charge-up the super-capacitor to a user selectable value. Once the charge-up is complete, the LEDs can be fired up to 1025 mA (LED1 and LED3) and 2050 mA (LED2) without causing a battery overload.

In general, a boost converter only regulates output voltages which are higher than the input voltage. This device operates differently. For example, in the voltage mode operation the device is capable to regulate 4.2 V at the output from a battery voltage pulsing as high 5.5 V. To control these applications properly, a down conversion mode is implemented.

If the input voltage reaches or exceeds the output voltage, the converter changes to a down conversion mode. In this mode, the control circuit changes the behavior of the rectifying PMOS. It sets the voltage drop across the PMOS as high as required to regulate the output voltage. This means the power losses in the converter increase. This must be taken into account for thermal consideration.

In direct drive mode (HC_SEL = L), the power stage is capable of supplying a maximum total current of roughly 1300 mA to 1500 mA. The TPS6132x provides three constant current inputs capable of sinking up to 445 mA (LED1 and LED3) and 890 mA (LED2) in flashlight mode.

The TPS6132x integrates an I^2C compatible interface allowing transfers up to 3.4 Mbps. This communication interface can be used to set the operating mode (shutdown, constant output current mode vs constant output voltage mode), to control the brightness of the external LED (DC-light and flashlight modes), to adjust the output voltage (from 3.825 V to 5.7 V in 125-mV steps) or to program the safety timer for instance. See *Register Maps* for more details.

In the TPS6132x device, the DC-light and flash can be controlled either by the I^2C interface or by the means of hardware control signals (STRB0 and STRB1). The maximum duration of the flashlight pulse can be limited by means of an internal user programmable safety timer (STIM). To avoid the LEDs to be kept accidentally on in DC-light mode by software control, the device implements a 13-s watchdog timer. The DC-light watchdog timer can be disabled by pulling the STRB1 signal high.

9.2 Functional Block Diagram

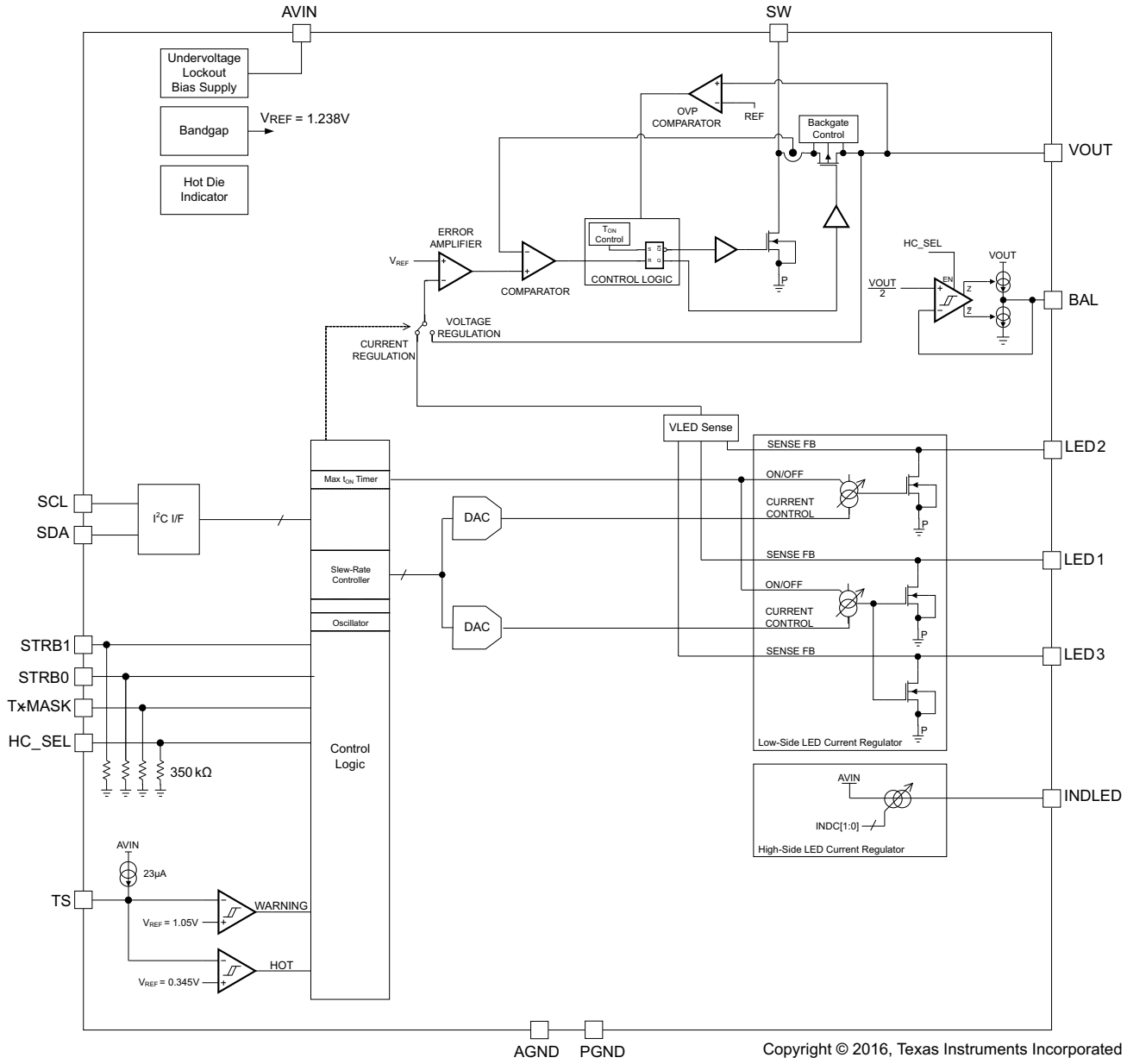


Figure 29. TPS6132x Block Diagram

Functional Block Diagram (continued)

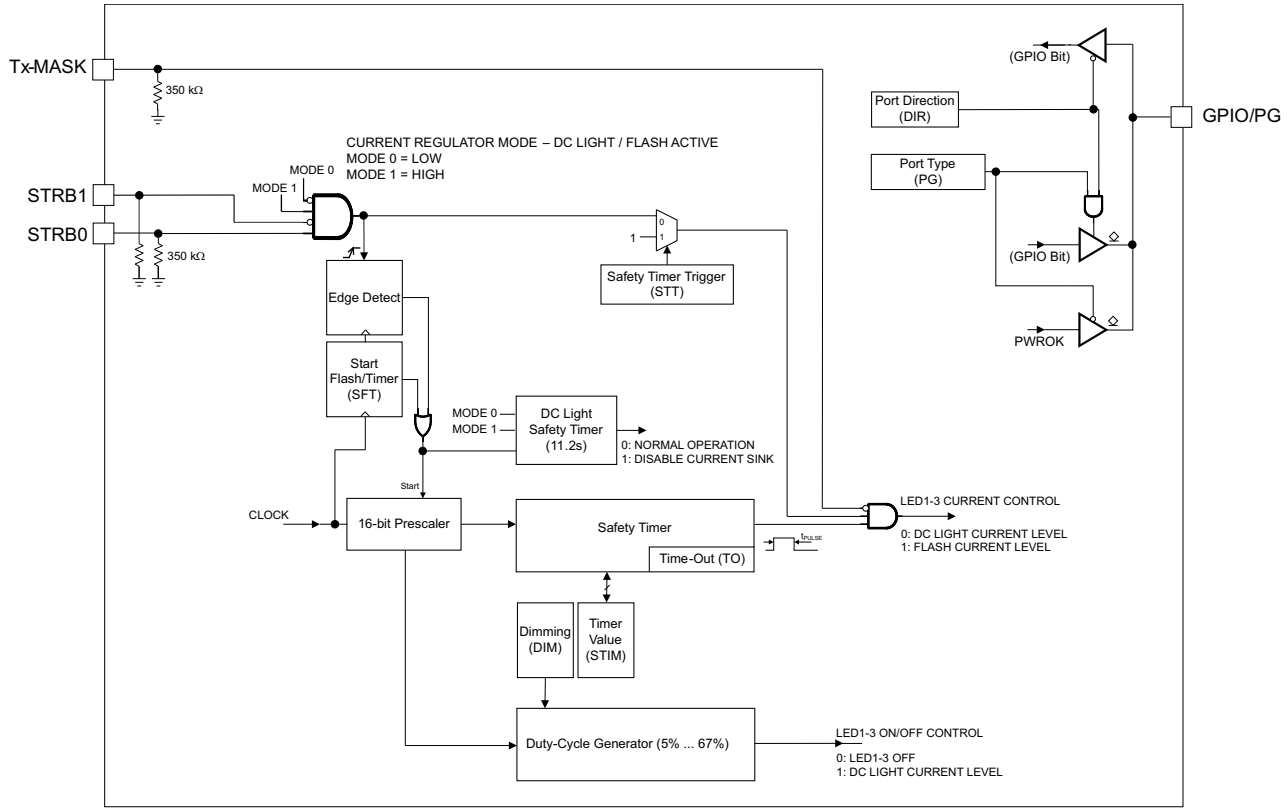


Figure 30. Timer Block Diagram

9.3 Feature Description

9.3.1 LED High-current Regulators, Unused Inputs

The TPS6132x device uses LED forward voltage sensing circuitry on LEDx pins to optimize the power stage boost ratio for maximum efficiency. TI recommends against leaving any of the LEDx pins unused if the operation is selected through ENDLED[3:1] bits due to the nature of the sensing circuitry. Leaving these pins unconnected, whilst the respective ENLEDx bits have been set, forces the control loop into high gain and eventually trip the output over-voltage protection.

The LEDx inputs may be connected together to drive one or two LEDs at higher currents. Connecting the current sink inputs in parallel does not affect the internal operation of the TPS6132x. TI recommends disabling the LED inputs that are not used for best operation (see *REGISTER5 (address = 0x05)*).

To achieve smooth LED current waveforms, the TPS6132x device actively controls the LED current ramp-up and ramp-down sequences.

Table 2. LED Current Ramp-Up and Ramp-Down Control vs Operating Mode

	DIRECT DRIVE MODE (HC_SEL = 0)	HIGH-CURRENT MODE (HC_SEL = 1)
LED CURRENT RAMP-UP	I_{STEP} = 27.5 mA	I_{STEP} = 62 mA
	t_{RISE} = 12 µs	t_{RISE} = 0.5 µs
	Slew-rate ≈ 2.3 mA/µs	Slew-rate ≈ 124 mA/µs

Feature Description (continued)

Table 2. LED Current Ramp-Up and Ramp-Down Control vs Operating Mode (continued)

	DIRECT DRIVE MODE (HC_SEL = 0)	HIGH-CURRENT MODE (HC_SEL = 1)
LED CURRENT RAMP-DOWN	I_{STEP} = 27.5 mA	I_{STEP} = 62 mA
	t_{FALL} = 0.5 µs	t_{FALL} = 0.5 µs
	Slew-rate ≈ 55 mA/µs	Slew-rate ≈ 124 mA/µs

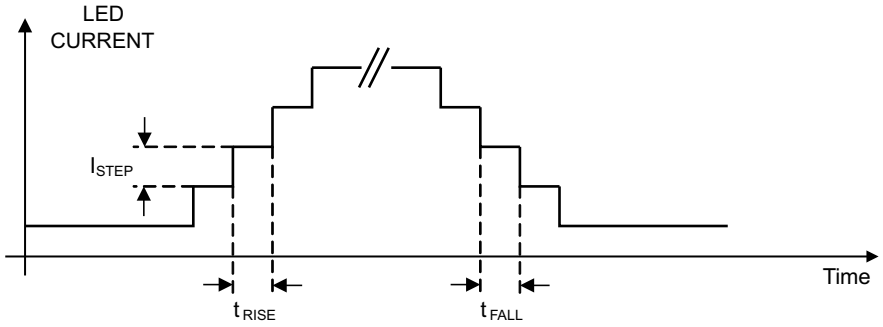


Figure 31. LED Current Slew-Rate Control

In high-current mode (HC_SEL = 1), the LED current settings are defined as a fixed ratio (×2.25) versus the direct drive mode values (HC_SEL = L).

9.3.2 Safety Timer Accuracy

The LED strobe timer uses the internal oscillator as a reference clock. The timer execution speed (see *REGISTER3 (address = 0x03)*) scales according to the reference clock accuracy.

Table 3. Safety Timer Accuracy

OSCILLATOR FREQUENCY	SAFETY TIMER DURATION
Minimum	Maximum = Typical × (1 + f_{ACC}) (1)
Typical	Typical (2)
Maximum	Minimum = Typical × (1 - f_{ACC}) (1)

(1) See *REGISTER3 (address = 0x03)*
(2) See *Electrical Characteristics*

9.3.3 Current Limit Operation

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off-time through sensing of the voltage drop across the synchronous rectifier. The detection threshold is user selectable through the ILIM bit. The ILIM bit can only be set while still in shutdown before the device begins operation..

Figure 32 illustrates the inductor and rectifier current waveforms during current limit operation. The output current (I_{OUT}) is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off-time is lengthened to allow the current to decrease to this threshold before the next on-time begins, so called frequency fold-back mechanism.

Both the output voltage and the switching frequency are reduced as the power stage of the device operates in a constant current mode. Equation 1 shows the maximum continuous output current ($I_{OUT(CL)}$) before entering current limit operation.

$$I_{OUT(CL)} = (1 - D) \times \left(I_{VALLEY} + \frac{1}{2} \Delta I_L\right) \text{ with } \Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \text{ and } D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

The TPS6132x device also provides a negative current limit (approximately 300 mA) to prevent an excessive reverse inductor current when the power stage sinks current from the output (storage capacitor) in the forced continuous conduction mode.

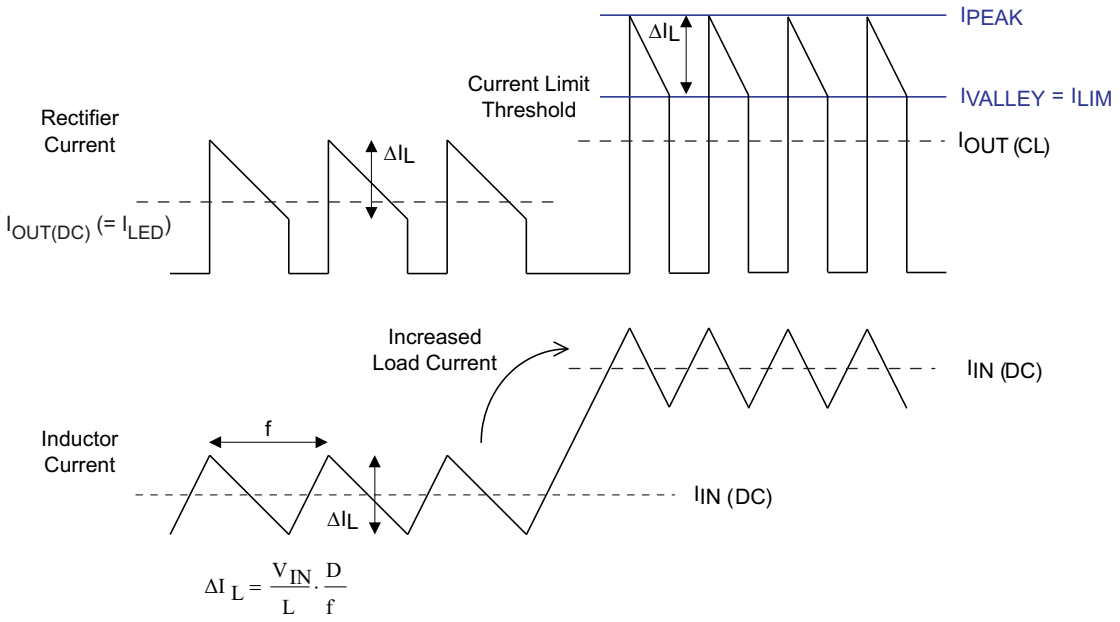


Figure 32. Inductor and Rectifier Currents in Current Limit Operation

NOTE

To minimize the requirements on the energy storage capacitor present at the output of the driver (HC_SEL = 1), the TPS6132x device can contribute to a larger extent in supporting directly the high-current LED flash strobe. In fact, the device can dynamically adjust it's current limit setting according to the Tx-MASK input.

Table 4. Inductor Current Limit Operation vs HC_SEL and Tx-MASK Inputs

VALLEY CURRENT LIMIT SETTING	ILIM BIT	HC_SEL INPUT	Tx-MASK INPUT
1150 mA	Low	Low	Low
1600 mA	High	Low	Low
30 mA	Low	High	Low
250 mA	High	High	Low
1150 mA	Low	Low	High
1600 mA	High	Low	High
—(1)	Low	High	High
—(1)	High	High	High

(1) The DC-DC power stage is disabled, zero current is being drained from the input source.

9.3.4 Start-Up Sequence

To avoid high inrush current during start-up, the internal start-up cycle begins with a precharge phase. During precharge, the rectifying switch is turned on until the output capacitor is either charged to a value close to the input voltage or approximately 3.3 V, whichever occurs first. The rectifying switch is current limited during this phase. The current limit increases with decreasing input to output voltage difference. This circuit also limits the output current under short-circuit conditions at the output. Figure 33 shows the typical precharge current vs input minus the output voltage for a specific input voltage.

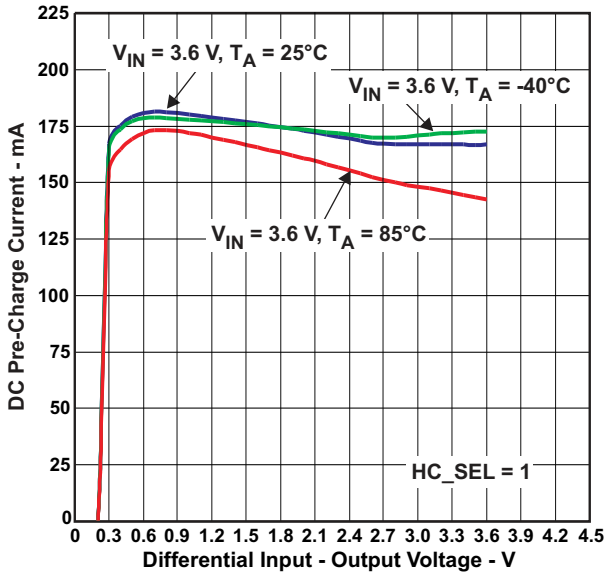


Figure 33. Typical DC Precharge and Short-Circuit Current

In direct drive mode (HC_SEL = L, TPS6132x), after having precharged the output capacitor, the device begins switching and increases its current limit in three steps to the target determined by the ILIM setting, typically to 30 mA, 250 mA, or full current limit. The current limit transition from the first to the second step occurs after a millisecond of operation. Full current limit operation is set once the output voltage reaches its regulation limits. In this mode, the active balancing circuit is disabled.

In high-current mode (HC_SEL = H), the precharge voltage of the storage capacitor is dependent on the input voltage and operating mode (voltage regulation versus current regulation mode). In case the device is set for exclusive current regulation operation (MODE_CTRL = 01 or 10 and ENVM = 0), the output capacitor precharge voltage is close to the input voltage. Under all other operating conditions, the precharge voltage is either close to the input voltage or approximately 3.3 V, whichever is lower. Furthermore, precharge operation can be suspended and resumed through the Tx-MASK input (see *REGISTER4 (address = 0x04)* and *REGISTER3 (address = 0x03)*).

The device begins switching after the storage capacitor pre-charging is complete. During down-mode operation, the inductor valley current is actively limited either to 30 mA or 250 mA (see *REGISTER4 (address = 0x04)*). As the device enters boost mode operation, the current limit transitions to full capacity (see *REGISTER4 (address = 0x04)* and *REGISTER3 (address = 0x03)*). As a consequence, the output voltage ramps-up linearly and the start-up time required to reach the programmed output voltage (see *REGISTER6 (address = 0x06)*) depends primarily on the super-capacitor value and load current. In this mode, the active balancing circuit is enabled.

9.3.5 Power Good (Flash Ready)

The TPS6132x integrates a power-good circuitry that is activated when the device is operating in voltage regulation mode (MODE_CTRL = 11 or ENVM = 1). In shutdown mode (MODE_CTRL = 00) the GPIO/PG pin state is defined in Table 5.

Table 5. GPGIO/PG Pin State

GPIOTYPE	GPIO/PG SHUTDOWN STATE
0	Reset or pulled to ground
1	Open-drain

Depending on the GPIO/PG output stage type selection, push-pull or open-drain, the polarity of the power-good output signal (PG) can be inverted or noninverted. The power-good software bit and hardware signal polarity is defined in Table 6.

Table 6. PG Bit and Polarity

GPIOTYPE	PG BIT	GPIO/PG OUTPUT PORT	COMMENTS
0: push-pull output	0	0	Output is active high signal polarity
	1	1	
1: open-drain output	0	Open-drain	Output is active low signal polarity
	1	Low	

The power good signal is valid when the output voltage is within –1.5% and 2.5% of its nominal value. Conversely, it is asserted low when the voltage mode operation gets suspended (MODE_CTRL ≠ 11 and ENVM = 0).

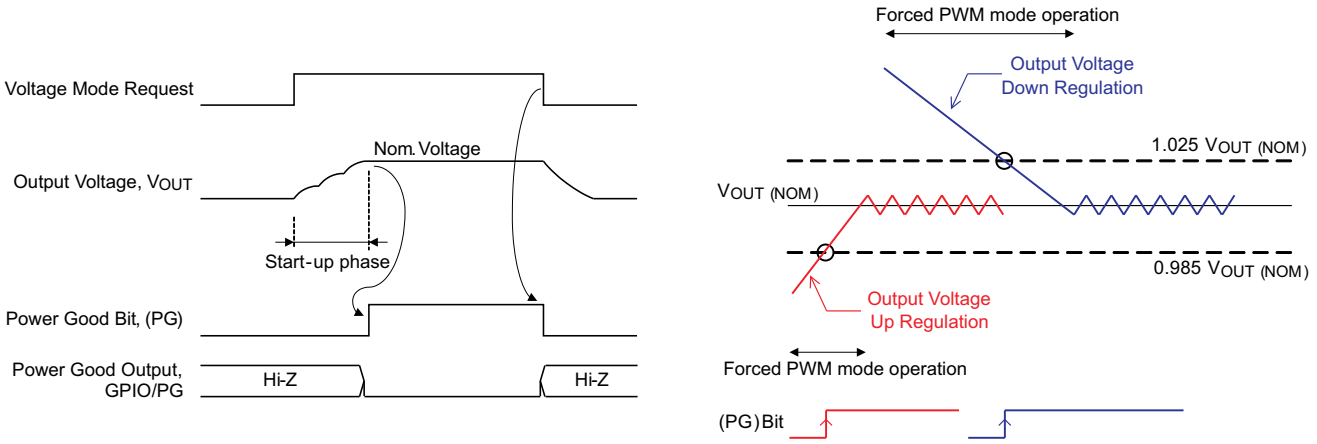


Figure 34. Power Good Operation (DIR = 1, GPIOTYPE = 1)

The TPS6132x device uses a control architecture that allows *recycling* excessive energy that might be stored in the output capacitor. By reversing the operation of the boost power stage, the converter is able to transfer energy from its output back into the input source. In this case, the power-good signal is deasserted while the output voltage is decreasing towards its target value: the closest fit voltage the converter can support. See *Down Mode In Voltage Regulation Mode* for additional information.

9.3.6 LED Temperature Monitoring

The TPS6132x devices monitor the LED temperature by measuring the voltage between the TS and AGND pins. An internal current source provides the bias (approximately 24 μA) for a negative-temperature coefficient resistor (NTC), and the TS pin voltage is compared to internal thresholds (1.05 V and 0.345 V) to protect the LEDs against overheating.

The temperature monitoring related blocks are always active in DC-light or flashlight modes. In voltage mode operation (MODE_CTRL = 11), the device only activates the TS input when the ENTS bit is set to high. In shutdown mode, the LED temperature supervision is disabled and the quiescent current of the device is dramatically reduced.

The LEDWARN and LEDHOT bits reflect the LED temperature. The LEDWARN bit is set when the voltage seen at the TS pin is lower than 1.05 V. This threshold corresponds to an LED warning temperature value, the device operation is still permitted.

While regulating LED current (DC-light or flashlight modes), the LEDHOT bit is latched when the voltage seen at the TS pin is lower than 0.345 V. This threshold corresponds to an excessive LED temperature value, the device operation is immediately suspended (MODE_CTRL bits are reset and HOTDIE bits are set).

9.3.7 Hot Die Detector

The hot die detector monitors the junction temperature but does not shutdown the device. It provides an early warning to the camera engine to avoid excessive power dissipation thus preventing thermal shutdown during the next high-power flash strobe.

The hot die detector (HOTDIE bits) reflects the instantaneous junction temperature and is always enabled, except when the device is in shutdown mode (MODE_CTRL = 00).

9.3.8 Undervoltage Lockout

The undervoltage lockout circuit (UVLO) protects the device from mis-operation at low input voltages by preventing the converter from turning on the switch-MOSFET or rectifier-MOSFET for battery voltages below 2.3 V. The I^2C compatible interface is fully functional down to 2.1-V input voltage.

9.3.9 Storage Capacitor Active Cell Balancing

A fully charged super-capacitor typically has a leakage current under 1 μA. The TPS6132x device integrates an active balancing feature to cut the total leakage current from the super-capacitor and balance circuit to less than 1.7 μA (typical).

The device integrates a window comparator to monitor the tap point of the multi-cell super-capacitor. The balancing output (BAL) is substantially half the actual output voltage (V_{OUT}). If the internal leakage current in one capacitor is larger than in the other, the voltage at their junction tends to change in such a way that the voltage on the capacitor with the larger (or largest) leakage current is reduced.

When this happens, current flows from BAL in an appropriate direction to reduce the magnitude of voltage changes. After a long period of steady-state conditions the current from BAL is approximately equal to the difference between the leakage currents of the capacitor pair being balanced by the circuit. The output resistance of the balancing circuit, approximately 250 Ω, determines how quickly an imbalance is corrected.

9.3.10 RED Light Privacy Indicator

The TPS6132x device provides a high-side linear constant current source to drive low VF LEDs. The LED current is directly regulated off the battery and can be controlled through the INDC bits. Operation is understood best by referring to the Figure 35 and Figure 36.

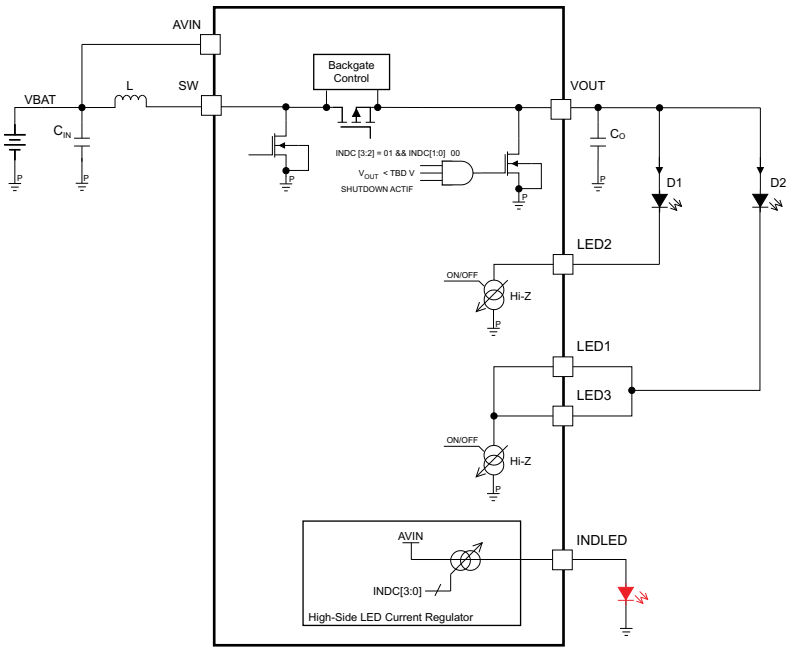


Figure 35. RED Light Indicator, Configuration 1

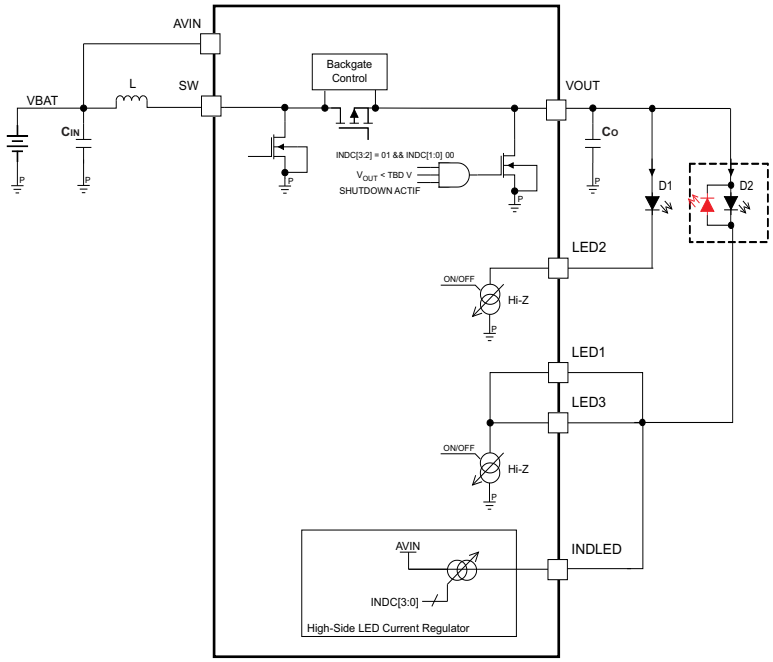


Figure 36. RED Light Indicator, Configuration 2

The device can provide a path to allow for reverse biasing of white LEDs (see Figure 36). To do so, the output of the converter (VOUT) is pulled to ground thus allowing a reverse current to flow. This mode of operation is only possible when the converter's power stage is in shutdown (MODE_CTRL = 00, ENVM = 0 and HC_SEL = 0).

9.3.11 White LED Privacy Indicator

The TPS6132x device features white LED drive capability at low light intensity. To generate a reduced LED average current, the device employs a 30-kHz fixed frequency PWM modulation scheme. The PWM timer uses the internal oscillator as reference clock, therefore the PWM modulating frequency shows the same accuracy as the internal reference clock. See Figure 30 for more information on device operation.

The DC-light current is modulated with a duty cycle defined by the INDC bits. The low light dimming mode can only be activated in the software controlled DC-light only mode (MODE_CTRL = 01, ENVM = 1) and applies to the LEDs selected through ENLED bits. In this mode, the DC-light safety timeout feature is disabled.

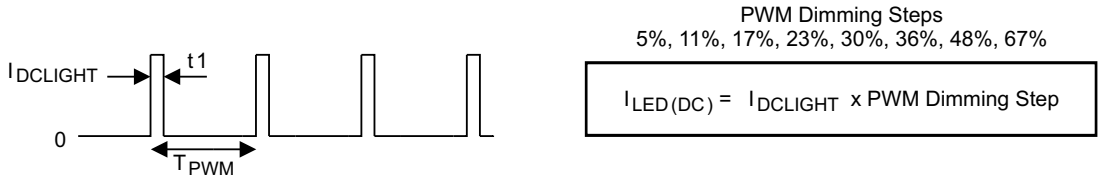


Figure 37. PWM Dimming Principle

9.3.12 Storage Capacitor, Precharge Voltage Calibration

High-power LEDs tend to exhibit a wide forward voltage distribution. The TPS6132x device integrates a self-calibration procedure that can be used to determine the optimum super-capacitor precharge voltage based on the actual worst case LED forward voltage and ESR of the storage capacitor. This calibration procedure is meant to start at a minimum output voltage and can be initiated by setting the SELFCAL bit, preferably with MODE_CTRL = 00, ENVM = 0.

The calibration procedure monitors the sense voltage across the low-side current regulators, according to ENLED bits setting, and registers the LED featuring the largest forward voltage. The TPS6132x device automatically sweeps through its output voltage range and performs a short duration flash strobe for each step (see *REGISTER2 (address = 0x02)* and *REGISTER1 (address = 0x01)*).

In direct drive mode (HC_SEL = L), the energy is being directly transferred from the battery to the LEDs. In high-current mode (HC_SEL = H), the energy is supplied exclusively by the output reservoir capacitor and the inductive power stage is turned off for the flash strobe period of time.

The sequence is stopped once each of the the low-side current regulators has enough headroom voltage, typically 400 mV. The resulting output voltage is written to register OV and the SELFCAL bit is set. The SELFCAL bit is only reset at the start of a calibration cycle. When SELFCAL is asserted, the output voltage register (OV) returns the result of the last calibration sequence.

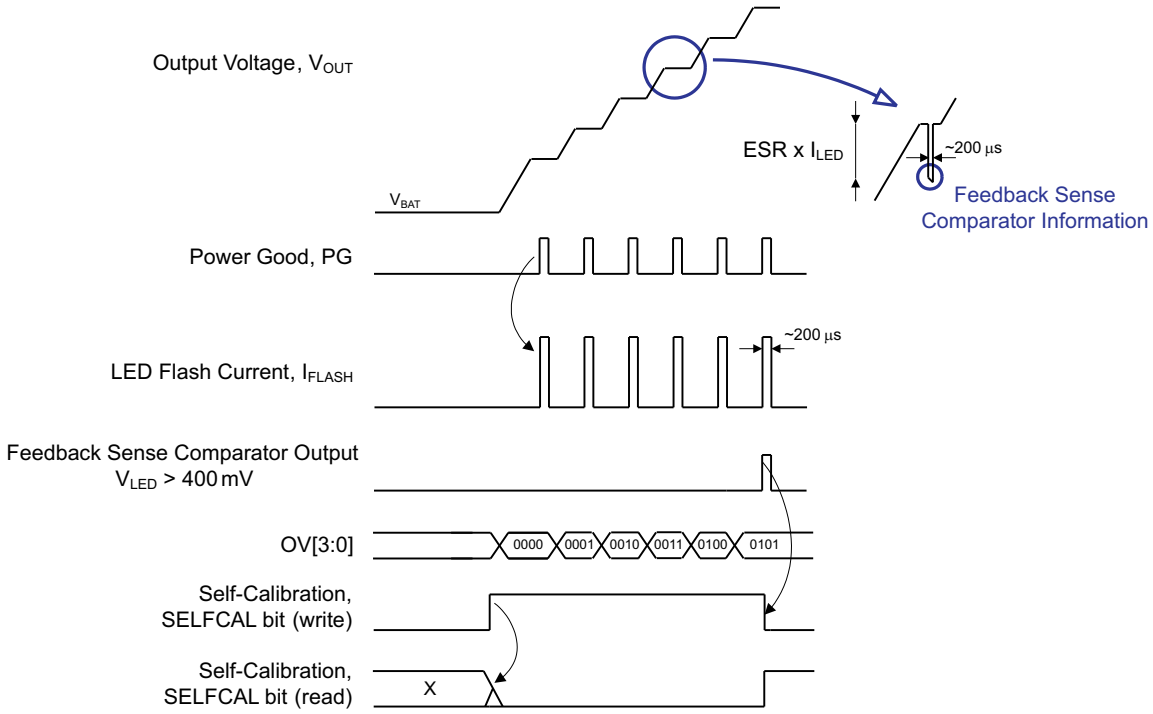


Figure 38. LED Forward Voltage Self-Calibration Principle

9.3.13 Storage Capacitor, Adaptive Precharge Voltage

In high-power LED camera flash applications, the storage capacitor is supposed to be charged to an optimum voltage level to:

- Maintain sufficient headroom voltage across the LED current regulators for the entire strobe time.
- Minimize the power dissipation in the device.

High-power LEDs tend to exhibit large dynamic forward voltage variation relating to own self-heating effects. In addition, the energy storage capacitor, an electrochemical double-layer capacitor or super-capacitor, also shows a relatively large effective capacitance and ESR spread. The main factors contributing to these variations are: flash strobe duration, temperature, and ageing effects.

In practice, it normally becomes very challenging to compensate for all these variations and a worst-case design would presumably be too pessimistic. As a consequence, designers would have to give-up on the benefits coming along with the *Storage Capacitor, Precharge Voltage Calibration* approach.

The TPS6132x device offers the possibility of controlling the storage capacitor precharge voltage in a closed-loop manner. The principle is to dynamically adjust the initial pre-voltage to the minimum value, as required for the particular components characteristic and operating conditions.

The reference criteria used to evaluate proper operation is the headroom voltage across the LED current regulators. In case of a critical headroom voltage (V_{LEDx}) at the end of a flash strobe, cycle *n*, the precharge voltage must be increased before to the next capture sequence, cycle *n* + 1.

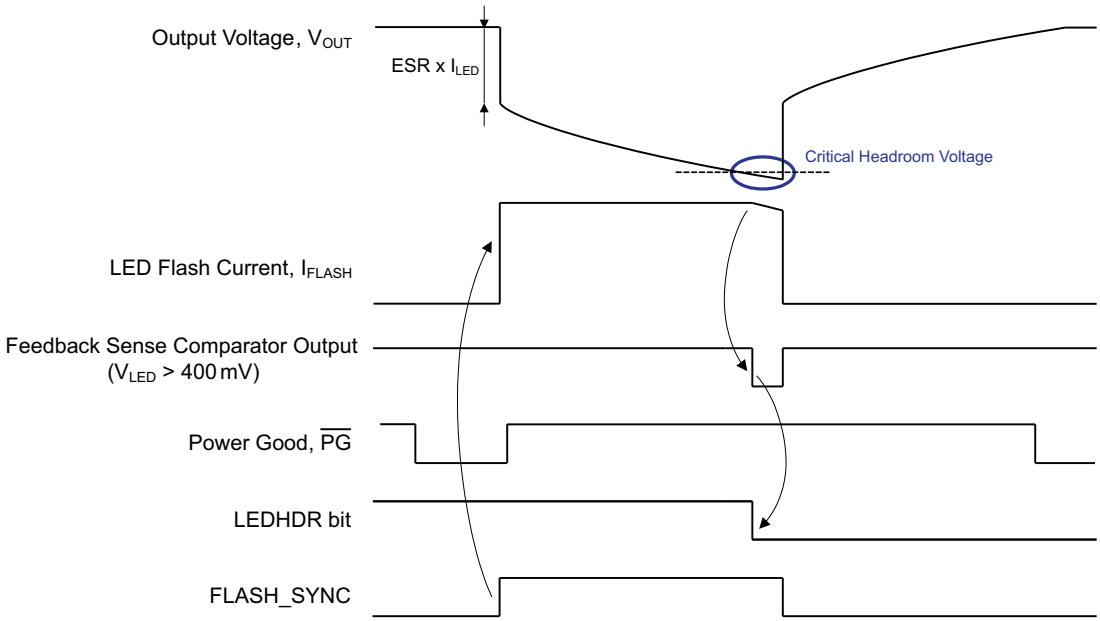


Figure 39. Storage Capacitor, Simple Adaptive Precharge Voltage

9.3.14 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors [1]. The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and transmits data on the bus under control of the master device.

The TPS6132x device works as a *slave* and supports the following data transfer *modes*, as defined in the I^2C-Bus Specification [1]: standard mode (100 kbps) and fast mode (400 kbps), and high-speed mode (3.4 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.1 V.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as HS-mode. The TPS6132x device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is defined as '011 0011' (TPS61325) and '011 0010' (TPS61326).

9.3.14.1 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 40. All I^2C-compatible devices must recognize a start condition.

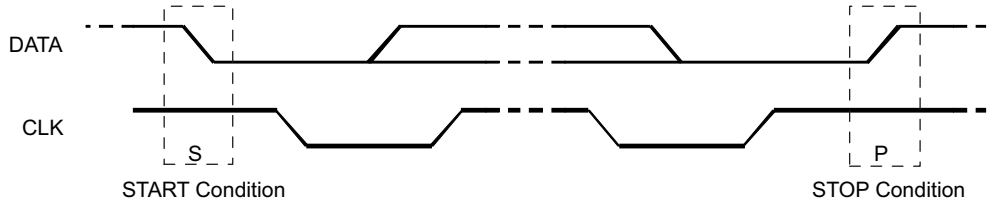


Figure 40. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/W) on the SDA line. The master ensures that data is valid during all transmissions. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 41). All devices receive the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 42) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave is established.

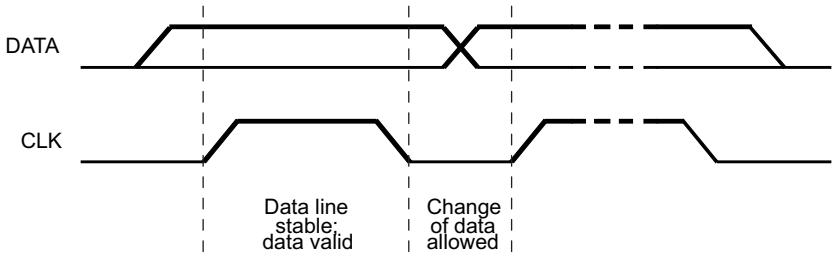


Figure 41. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver must acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8 data bits and a 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 40). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

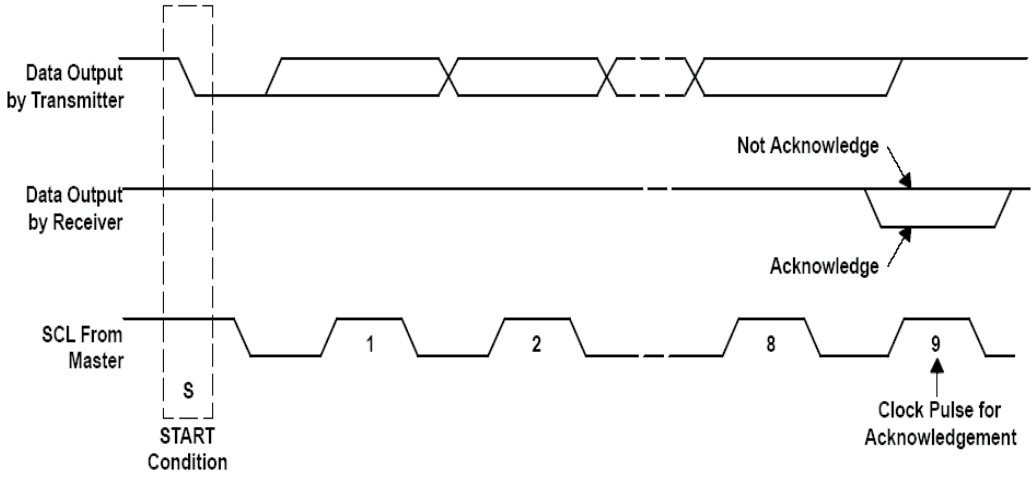


Figure 42. Acknowledge on the I²C Bus

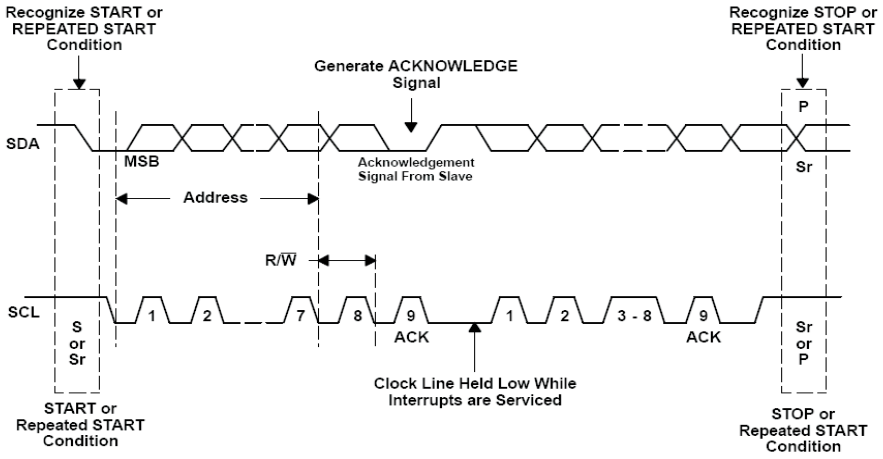


Figure 43. Bus Protocol

9.3.14.2 HS-Mode Protocol

The master generates a start condition followed by a valid serial byte containing HS master code 00001xxx. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a *repeated start condition*, a repeated start condition has the same timing as the start condition. After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in HS-mode.

9.4 Device Functional Modes

9.4.1 Down Mode In Voltage Regulation Mode

In general, a boost converter only regulates output voltages which are higher than the input voltage. The featured devices come with the ability to regulate 4.2 V at the output with an input voltage as high as 5.5 V. To control these applications properly, a down conversion mode is implemented.

In voltage regulation mode, if the input voltage reaches or exceeds the output voltage, the converter changes to the down-conversion mode. In this mode, the control circuit changes the behavior of the rectifying PMOS. It sets the voltage drop across the PMOS as high as necessary to regulate the output voltage. This means the power losses in the converter increase. This must be taken into account for thermal consideration. The down conversion mode is automatically turned off as soon as the input voltage falls about 200 mV below the output voltage.

For proper operation in down conversion mode the output voltage must not be programmed higher than approximately 5.3 V. Take care not to violate the absolute maximum ratings at the SW pins.

The TPS6132x device uses a control architecture that allows *recycling* excessive energy that might be stored in the output capacitor. By reversing the operation of the boost power stage, the converter is capable of transferring energy from its output back into the input source.

In high-current mode (HC_SEL = 1), this feature becomes useful to dynamically adjust the output voltage (V_{OUT}) depending on the operating conditions. For example, 4.95 V constant output voltage to support audio applications or variable storage capacitor precharge voltage, see Figure 76.

This reverse operating mode can only perform within an output voltage range higher than the input supply. For example, if the storage capacitor is initially precharged to 4.95 V, the input voltage is around 4.1 V and the target output voltage is set to 3.825 V, the converter is only able to lower the output node down to the input level.

9.4.2 Power-Save Mode Operation, Efficiency

The TPS6132x device integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage.

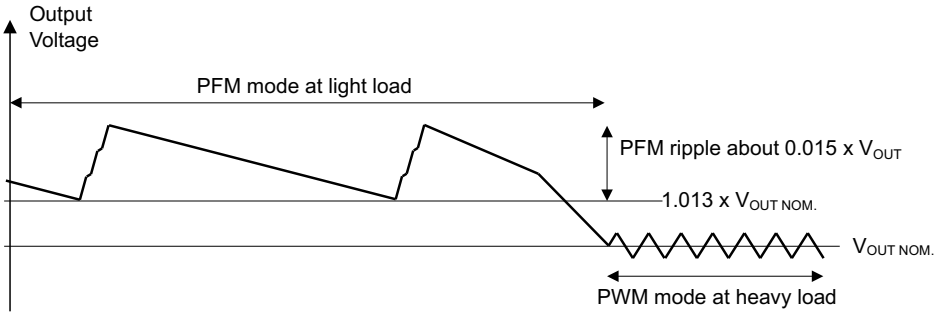


Figure 44. Operation in PFM Mode and Transfer to PWM Mode

The power save mode can be enabled and disabled through the ENPSM bit. In down conversion mode, power save mode is always active and the device cannot be forced into fixed frequency operation at light loads.

The LED sense voltage has a direct effect on the converter's efficiency. Because the voltage across the low-side current regulator does not contribute to the output power, LED brightness, reducing the sense voltage increases the efficiency of the device.

Device Functional Modes (continued)

In direct drive mode (HC_SEL = L), the energy is being directly transferred from the battery to the LEDs. The integrated current control loop automatically selects the minimum boosting ratio to maintain regulation based on the LED forward voltage and current requirements. The low-side current regulators drop the voltage difference between the input voltage and the LEDs forward voltage ($V_{F(LED)} < V_{IN}$). When running in boost mode ($V_{F(LED)} > V_{IN}$), the voltage present at the LEDx pins of the low-side current regulators is typically 400 mV, leading to high power conversion efficiency. Depending on the input voltage and the LEDs forward voltage characteristic, the converter shows efficiency in the range of about 75% to 90%.

In high-current mode (HC_SEL = H), the device is only supplying a limited amount of energy directly from the battery, for example, DC-light, contribution to flash current, or voltage regulation mode. During a flash strobe, the bulk of the energy supplied to the LEDs is provided by the reservoir capacitor. The low-side current regulators typically operate with 400-mV headroom voltage. This means the power losses in the device increase and thermal considerations become more important.

9.4.3 Mode Of Operation: DC-Light and Flashlight

Operation is understood best by referring to Figure 30. The device set to one of four different operating modes depending on the state of the MODE_CTRL bits.

- MODE_CTRL = 00: The device is in shutdown mode.
- MODE_CTRL = 01: The STRB0 and STRB1 inputs are disabled. The device is regulating the LED current in DC-light mode (DCLC bits) regardless of the STRB0 and STRB1 inputs and the START_FLASH/TIMER (SFT) bit. To avoid device shutdown by DC-light safety timeout, MODE_CTRL must be refreshed within less than 13 s (STRB1 = 0). The DC-light watchdog timer can be disabled by pulling the STRB1 signal high.
- MODE_CTRL = 10: The STRB0 and STRB1 inputs are enabled and the flashlight pulse can either be triggered by these synchronization signals or by a software command (START_FLASH/TIMER (SFT) bit, STRB0 = 1). The LEDs' operation is enabled or disabled according to the STRB0 and STRB1 inputs, the flashlight safety timer is activated and the DC-light safety timer is disabled.
- MODE_CTRL = 11: The device is regulating a constant output voltage according to OV bits' settings. The low-side LEDx current regulators are disabled and the LEDs are disconnected from the output. In this operating mode, the safety timer is disabled.

9.4.4 Flash Strobe Is Level Sensitive (STT = 0): LED Strobe Follows STRB0 and STRB1 Inputs

In this mode, the high-power LEDs are driven at the flashlight current level and the safety timer (STIM) is running. The maximum duration of the flashlight pulse is defined in the STIM register.

The safety timer is triggered on rising edge and stopped either by a negative logic on the synchronization source (STRB0 = STRB1 = 0) or by a timeout event (TO bit).

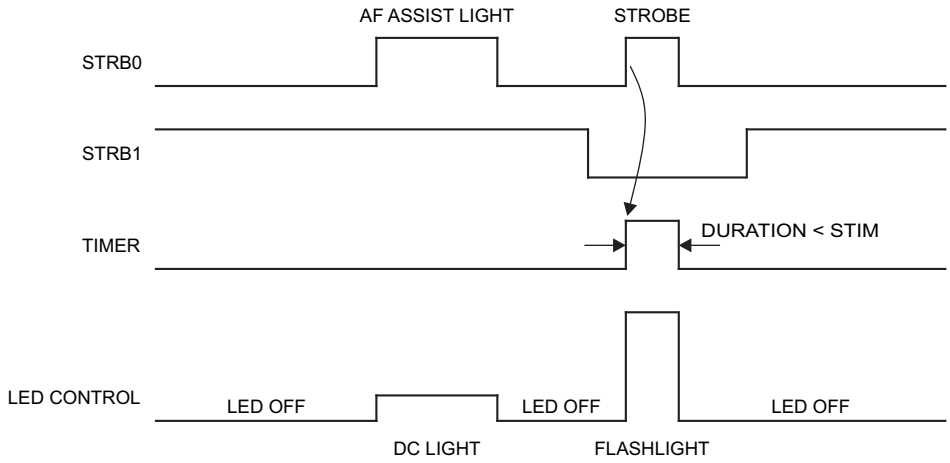


Figure 45. Hardware Synchronized DC-Light and Flashlight Strobe

Device Functional Modes (continued)

9.4.5 Flash Strobe Is Leading Edge Sensitive (STT = 1): One-Shot LED Strobe

In this mode, the high-power LEDs are driven at the flashlight current level and the safety timer (STIM) is running. The duration of the flashlight pulse is defined in the STIM register.

The flashlight strobe is started either by a rising edge on the synchronization source (STRB0 = 1 and STRB1 = 0) or by a positive transition on the START-FLASH/TIMER (SFT) bit (STRB0 = 1 and STRB1 = 0). Once running, the timer ignores all kind of triggering signals and only stops after a timeout (TO). START-FLASH/TIMER (SFT) bit is being reset by the timeout (TO) signal.

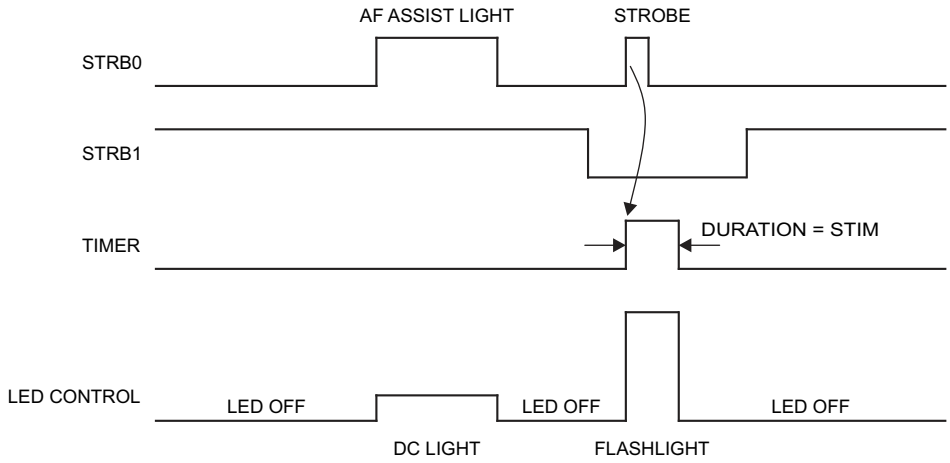


Figure 46. Edge Sensitive Timer (Single Trigger Event)

9.4.6 LED Failure Modes and Overvoltage Protection

If a high-power LED fails as a short circuit, the low-side current regulator limits the maximum output current and the HIGH-POWER LED FAILURE (HPLF) flag is set.

If a high-power LED fails as an open circuit, the control loop initially attempts to regulate off of its low-side current regulator feedback signal. This drives V_{OUT} higher. As the open circuited LED never accepts its programmed current, V_{OUT} must be voltage-limited by means of a secondary control loop.

The TPS6132x device limits V_{OUT} according to the overvoltage protection settings (see Figure 47). In this failure mode, V_{OUT} is either limited to 4.65 V (typical) or 6.0 V (typical) and the HIGH-POWER LED FAILURE (HPLF) flag is set.

Table 7. OVP Threshold

OVP THRESHOLD	OPERATING CONDITIONS
4.65 V (typical)	HC_SEL = L and 0000 ≤ OV ≤ 0100
6 V (typical)	HC_SEL = H or 0101 ≤ OV ≤ 1111

See *LED High-current Regulators, Unused Inputs* for more information.

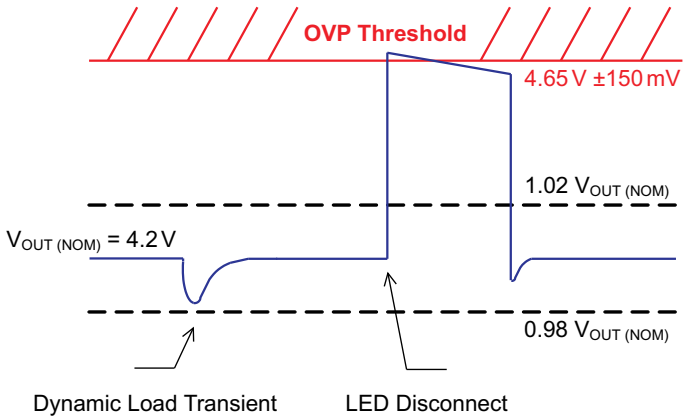


Figure 47. Overvoltage Protection Operation, 4.65 V (Typical)

9.4.7 Hardware Voltage Mode Selection

The TPS6132x device integrates a software control bit (ENVM) that can be used to force the converter to run in voltage mode regulation. Table 8 gives an overview of the different modes of operation.

Table 8. Operating Mode Description

INTERNAL REGISTER SETTINGS MODE_CTRL	ENVM	OPERATING MODES
00	0	The converter is in shutdown mode and the load is disconnected from the battery.
01	0	LEDs are turned on for DC-light operation (for example, a movie light). The converter is operating in the current regulation mode (CM). The output voltage is controlled by the forward voltage characteristic of the LED. The energy is being directly transferred from the battery to the output.
10	0	The converter is operating in the current regulation mode (CM). The output voltage is controlled by the forward voltage characteristic of the LED. LEDs are ready for flashlight operation supported directly from the battery.
		In high-current mode (HC_SEL = H), the energy is supplied by the output reservoir capacitor and the inductive power stage is turned off for the flash strobe period of time.
11	0	LEDs are turned off and the converter is operating in the voltage regulation mode (VM). The output voltage is set through the register OV.
00	1	LEDs are turned off and the converter is operating in the voltage regulation mode (VM). The output voltage is set through the register OV.
01	1	The converter is operating in the voltage regulation mode (VM) and the output voltage is set through the register OV. The LED currents are regulated by the low-side current sinks. The LEDs are turned on for DC-light operation and the energy is being directly transferred from the battery to the output.
10	1	The converter is operating in the voltage regulation mode (VM) and the output voltage is set through the register OV. The LED currents are regulated by the low-side current sinks. The LEDs are ready for flashlight operation.
		In direct drive mode (HC_SEL = L), the energy is being directly transferred from the battery to the output.
		In high-current mode (HC_SEL = H), the energy is largely supplied by the output reservoir capacitor. However, the inductive power stage is active, and contributing to the flash power.
11	1	LEDs are turned off and the converter is operating in the voltage regulation mode (VM). The output voltage is set through the register OV.

9.4.8 Flashlight Blanking (Tx-MASK)

In direct drive mode (HC_SEL = 0), the Tx-MASK input signal can be used to disable the flashlight operation, for example, during a RF PA transmission pulse. This blanking function turns the LED from flashlight to DC-light thereby reducing almost instantaneously the peak current loading from the battery. The Tx-MASK function has no influence on the safety timer duration.

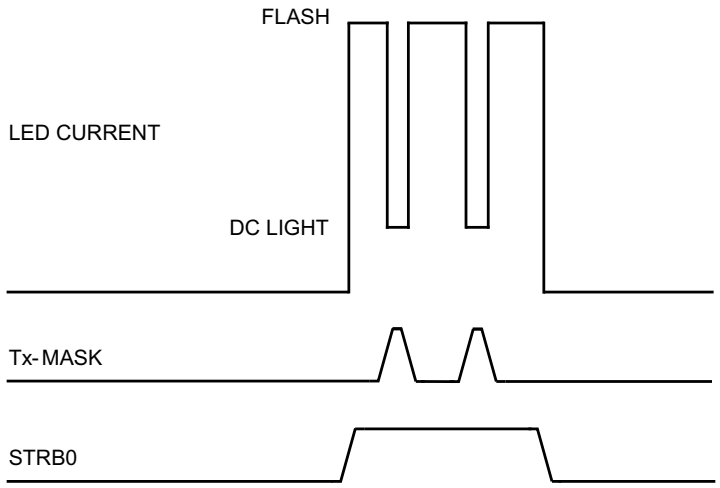


Figure 48. Synchronized Flashlight With Blanking Periods (STRB1 = 0)

In high-current mode (HC_SEL = 1), the Tx-MASK input pin is also used to dynamically adjust the device's current limit setting, controlling the maximum current drawn from the input source. See *Current Limit Operation* for additional information.

9.4.9 Shutdown

Pulling the MODE_CTRL bits low forces the device into shutdown, but only if ENVM = 0.

In direct-drive mode (HC_SEL = L) the regulator stops switching, the high-side PMOS disconnects the load from the input, and the LEDx pins are high impedance thus eliminating any DC conduction path. The TPS6132x device actively discharges the output capacitor when it turns off.

The integrated discharge resistor has a typical resistance of 2 kΩ, equally split between VOUT to BAL and BAL to GND outputs. The required time to discharge the output capacitor at VOUT depends on load current and the effective output capacitance. The active balancing circuit is disabled and the device consumes only a shutdown current of 1 μA (typical).

In high-current mode (HC_SEL = H), the device maintains its output biased at the input voltage level. The synchronous rectifier is current limited, for example, precharge current, in this mode, allowing external load, for example, an audio amplifier, to be powered with a restricted supply. The active balancing circuit is enabled and the device consumes only a standby current of 5 μA (typical).

9.4.10 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 160°C (typical), the device goes into thermal shutdown. In this mode, the power stage and the low-side current regulators are turned off, the HOTDIE bits are set and can only be reset by a readout.

In the voltage mode operation (MODE_CTRL = 11 or ENVM = 1), the device continues operation when the junction temperature falls below 140°C (typical) again. In the current regulation mode, DC-light or flashlight modes, the device operation is suspended.

9.5 Programming

9.5.1 TPS6132x I²C Update Sequence

The TPS6132x requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receiving each byte, the TPS6132x device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the TPS6132x. The TPS6132x performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

Figure 49. Write Data Transfer Format in F/S-Mode

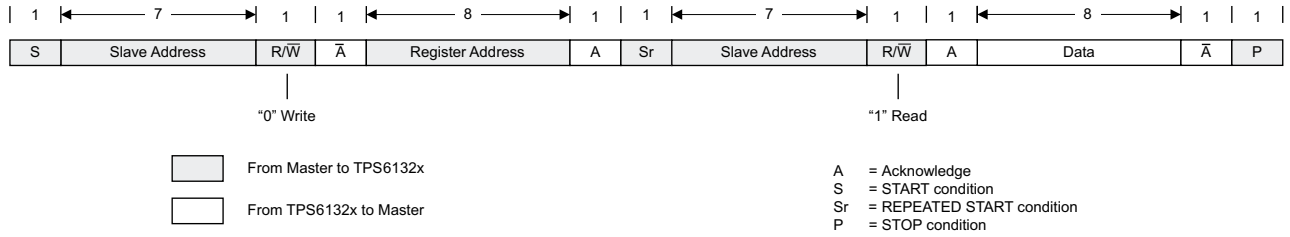


Figure 50. Read Data Transfer Format in F/S-Mode

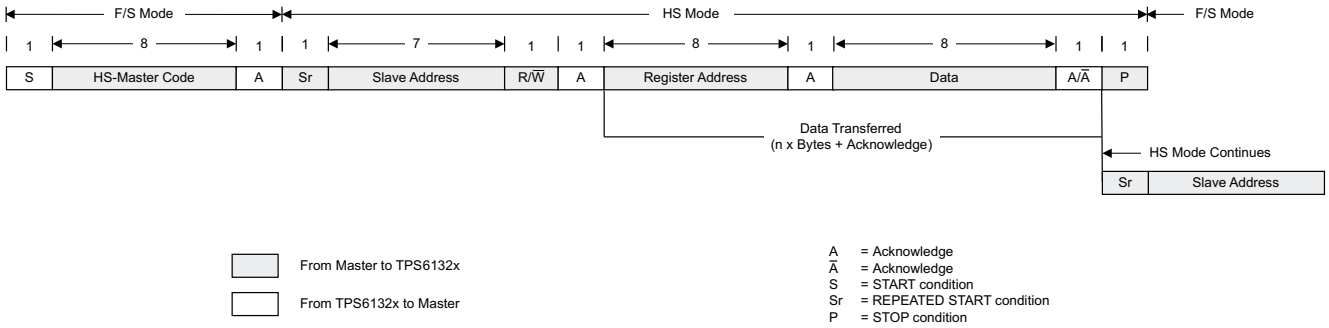


Figure 51. Data Transfer Format in H/S-Mode

9.6 Register Maps

9.6.1 Slave Address Byte

Figure 52. Slave Address Byte Description

MSB							LSB
X	X	X	X	X	X	A1	A0

The slave address byte is the first byte received following the START condition from the master device.

9.6.2 Register Address Byte

Figure 53. Register Address Byte Description

MSB							LSB
0	0	0	0	00	D2	D1	D0

Following the successful acknowledgement of the slave address, the bus master sends a byte to the TPS6132x, which contains the address of the register to be accessed.

9.6.3 REGISTER0 (address = 0x00)

Figure 54. REGISTER0 Fields

7	6	5	4	3	2	1	0
RESET	FREE	DCLC13			DCLC2		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. REGISTER0 Field Descriptions

Bit	Field	Type	Reset	Description
D7	RESET	R/W	0	Register reset 0: Normal operation 1: Default values are set to all internal registers
D5–D3	DCLC13	R/W	001	DC-light current control (LED1 and LED3) 000: 0 mA(1)(2) 001: 28.0 mA 010: 55.75 mA 011: 83.25 mA 100: 111.0 mA 101: 138.75 mA 110: 166.5 mA 111: 194.25 mA
D2–D0	DCLC2	R/W	010	DC-light current control (LED2) 000: 0 mA(1)(2) 001: 28.0 mA 010: 55.75 mA 011: 83.25 mA 100: 111.0 mA 101: 138.75 mA 110: 166.5 mA, 249.75 mA current level can be activated simultaneously with Tx-MASK = 1 111: 194.25 mA, 360.75 mA current level can be activated simultaneously with Tx-MASK = 1

(1) LEDs are off, V_{OUT} set according to OV.
(2) When DCLC2 and DCLC13 are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV.

9.6.4 REGISTER1 (address = 0x01)

Figure 55. REGISTER1 Fields

7	6	5	4	3	2	1	0
MODE_CTRL		FC2					
R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. REGISTER1 Field Descriptions

Bit	Field	Type	Reset	Description
D7–D6	MODE_CTRL	R/W	00	Mode control 00: Device in shutdown mode 01: Device operates in DC-light mode 10: Device operates in flashlight mode 11: Device operates as constant voltage source To avoid device shutdown by DC-light safety timeout, MODE_CTRL bits must be refreshed within less than 13 s. Writing to REGISTER1[7:6] automatically updates REGISTER2[7:6].
D5–D0	FC2	R/W	010000	Flash current control (LED2) HC_SEL = 0 / HC_SEL = 1 000000: 0 mA(1)(2) / 000000: 0 mA(1)(2) 000001: 28.0 mA / 000001: 64 mA 000010: 55.75 mA / 000010: 130 mA 000011: 83.25 mA / 000011: 196 mA 000100: 111.0 mA / 000100: 260 mA 000101: 138.75 mA / 000101: 324 mA 000110: 166.5 mA / 000110: 388 mA 000111: 194.25 mA / 000111: 452 mA 001000: 222.0 mA / 001000: 516 mA 001001: 249.75 mA / 001001: 580 mA 001010: 277.5 mA / 001010: 644 mA 001011: 305.25 mA / 001011: 708 mA 001100: 333.0 mA / 001100: 772 mA 001101: 360.75 mA / 001101: 836 mA 001110: 388.5 mA / 001110: 900 mA 001111: 416.25 mA / 001111: 964 mA 010000: 444.0 mA / 010000: 1028 mA 010001: 471.75 mA / 010001: 1092 mA 010010: 499.5 mA / 010010: 1156 mA 010011: 527.25 mA / 010011: 1220 mA 010100: 555.0 mA / 010100: 1284 mA 010101: 582.75 mA / 010101: 1348 mA 010110: 610.5 mA / 010110: 1412 mA 010111: 638.25 mA / 010111: 1476 mA 011000: 666.0 mA / 011000: 1540 mA 011001: 693.75 mA / 011001: 1604 mA 011010: 721.5 mA / 011010: 1668 mA 011011: 749.25 mA / 011011: 1732 mA 011100: 777.0 mA / 011100: 1796 mA 011101: 804.75 mA / 011101: 1860 mA 011110: 832.5 mA / 011110: 1924 mA 011111: 860.25 mA / 011111: 1988 mA ≥100000: 888.0 mA / ≥100000: 2052 mA

(1) LEDs are off, V_{OUT} set according to OV.
(2) When FC13 and FC2 are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV.

9.6.5 REGISTER2 (address = 0x02)

Figure 56. REGISTER2 Fields

7	6	5	4	3	2	1	0
MODE_CTRL		ENVM	FC13				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. REGISTER2 Field Descriptions

Bit	Field	Type	Reset	Description
D7–D6	MODE_CTRL	R/W	00	Mode control 00: Device in shutdown mode 01: Device operates in DC-light mode 10: Device operates in flashlight mode 11: Device operates as constant voltage source To avoid device shutdown by DC-light safety timeout, MODE_CTRL bits must be refreshed within less than 13 s. Writing to REGISTER2[6:5] automatically updates REGISTER1[6:5].
D5	ENVM	R/W	0	Enable voltage mode 0: Normal operation 1: Forces the device into a constant voltage source In read mode, the ENVM bit returns zero.
D4–D0	FC13	R/W	0100	Flash current control (LED1 and LED3) HC_SEL = 0 / HC_SEL = 1 00000: 0 mA(1)(2) / 00000: 0 mA(1)(2) 00001: 27.75 mA / 00001: 64.5 mA 00010: 55.5 mA / 00010: 127.0 mA 00011: 83.25 mA / 00011: 192.0 mA 00100: 111.0 mA / 00100: 256.0 mA 00101: 138.75 mA / 00101: 320.25 mA 00110: 166.5 mA / 00110: 384.5 mA 00111: 194.25 mA / 00111: 448.75 mA 01000: 222.0 mA / 01000: 513.0 mA 01001: 249.75 mA / 01001: 577.25 mA 01010: 277.5 mA / 01010: 641.5 mA 01011: 305.25 mA / 01011: 705.75 mA 01100: 333.0 mA / 01100: 770.0 mA 01101: 360.75 mA / 01101: 834.25 mA 01110: 388.5 mA / 01110: 898.5 mA 01111: 416.25 mA / 01111: 962.75 mA ≥10000: 444.0 mA / ≥10000: 1027.0 mA

(1) LEDs are off, V_{OUT} set according to OV.
(2) When FC13 and FC2 are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV.

9.6.6 REGISTER3 (address = 0x03)

Figure 57. REGISTER3 Fields

7	6	5	4	3	2	1	0
STIM			HPLF	SELSTIM TO	STT	SFT	Tx-MASK
R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. REGISTER3 Field Descriptions

Bit	Field	Type	Reset	Description
D7–D5	STIM	R/W	110	Safety timer STIM: RANGE 0, RANGE 1 000: 68.2 ms, 5.3 ms 001: 102.2 ms, 10.7 ms 010: 136.3 ms, 16.0 ms 011: 170.4 ms, 21.3 ms 100: 204.5 ms, 26.6 ms 101: 340.8 ms, 32.0 ms 110: 579.3 ms, 37.3 ms 111: 852 ms, 71.5 ms
D4	HPFL	R	0	High-power LED failure flag 0: Proper LED operation 1: LED failed (open or shorted) High-power LED failure flag is reset after readout
D3	SELSTIM	W	0	Safety timer selection range (write only) 0: Safety timer range 0 1: Safety timer range 1
	TO	R		Time-out flag (read only) 0: No time-out event occurred 1: Time-out event occurred. Time-out flag is reset at re-start of the safety timer.
D2	STT	R/W	0	Safety timer trigger 0: LED safety timer is level sensitive 1: LED safety timer is rising edge sensitive This bit is only valid for MODE_CTRL = 10.
D1	SFT	R/W	0	Start/Flash timer In write mode, this bit initiates a flash strobe sequence. Notice that this bit is only active when STRB0 input is high. 0: No change in the high-power LED current 1: High-power LED current ramps to the flash current level In read mode, this bit indicates the high-power LED status 0: High-power LEDs are idle 1: Ongoing high-power LED flash strobe
D0	Tx-MASK	R/W	1	Flash blanking control bit In write mode, this bit enables/disables the flash blanking/LED current reduction function. 0: Flash blanking disabled 1: LED current is reduced to DC-light level when Tx-MASK input is high In read mode, this flag indicates whether or not the flashlight masking input is activated. Tx-MASK flag is reset after readout of the flag. 0: No flash blanking event occurred 1: Tx-MASK input triggered

9.6.7 REGISTER4 (address = 0x04)

Figure 58. REGISTER4 Fields

7	6	5	4	3	2	1	0
PG	HOTDIE		ILIM	INDC			
R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. REGISTER4 Field Descriptions

Bit	Field	Type	Reset	Description
D7	PG	R/W	0	Power good In write mode, this bit selects the functionality of the GPIO/PG output. 0: PG signal is routed to the GPIO port. 1: GPIO PORT VALUE bit is routed to the GPIO port. In read mode, this bit indicates the output voltage conditions. 0: The converter is not operating within the voltage regulation limits. 1: The output voltage is within its nominal value.
D6–D5	HOTDIE	R	00	Instantaneous die temperature 00: T_J < 55°C 01: 55°C < T_J < 70°C 10: T_J > 70°C 11: Thermal shutdown tripped. Indicator flag is reset after readout.
D4	ILIM	R/W	0	Inductor valley current limit The ILIM bit can only be set before the device enters operation (initial shutdown state). Valley current limit: ILIM bit, HC_SEL input, Tx-MASK input 1150 mA: Low, Low, Low 1600 mA: High, Low, Low 30 mA: Low, High, Low 250 mA: High, High, Low 1150 mA: Low, Low, High 1600 mA: High, Low, High —(1): Low, High, High —(1): High, High, High
D3–D0	INDC	R/W	0000	Indicator light control INDC: Privacy indicator INDLED channel 0000: Privacy indicator OFF 0001: INDLED current 2.6 mA(2) 0010: INDLED current 5.2 mA(2) 0011: INDLED current 7.9 mA(2) 0100: Privacy indicator OFF 0101: INDLED current 5.2 mA(2) 0110: INDLED current 10.4 mA(2) 0111: INDLED current 15.8 mA (2) INDC: Privacy indicator LEDx channels(3) 1000: 5% PWM dimming ratio 1001: 11% PWM dimming ratio 1010: 17% PWM dimming ratio 1011: 23% PWM dimming ratio 1100: 30% PWM dimming ratio 1101: 36% PWM dimming ratio 1110: 48% PWM dimming ratio 1111: 67% PWM dimming ratio

(1) The DC-DC power stage is disabled, zero current is being drained from the input source.
(2) For HC_SEL = L, the output node (VOUT) is internally pulled to ground.
(3) This mode of operation can only be activated for MODE_CTRL = 01, ENVM = 1, and STRB1 = 0.

9.6.8 REGISTER5 (address = 0x05)

Figure 59. REGISTER5 Fields

7	6	5	4	3	2	1	0
SELFCAL	ENPSM	DIR (W) STSTRB1 (R)	GPIO	GPIOTYPE	ENLED3	ENLED2	ENLED1
R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. REGISTER5 Field Descriptions

Bit	Field	Type	Reset	Description
D7	SELFCAL	W	0	High-current LED forward voltage self-calibration start In write mode, this bit enables/disables the output voltage vs LED forward voltage/current self-calibration procedure. 0: Self-calibration disabled 1: Self-calibration enabled In read mode, this bit returns the status of the self-calibration procedure. 0: Self-calibration ongoing 1: Self-calibration done Notice that this bit is only being reset at the (re-)start of a calibration cycle.
D6	ENPSM	R/W	1	Enable or disable power-save mode 0: Power-save mode disabled 1: Power-save mode enabled
D5	STSTRB1	R	1	STRB1 input status (read only) This bit indicates the logic state on the STRB1 state.
D5	DIR	W	1	GPIO direction 0: GPIO configured as input 1: GPIO configured as output
D4	GPIO	R/W	0	GPIO port value This bit contains the GPIO port value.
D3	GPIOTYPE	R/W	1	GPIO port type 0: GPIO is configured as push-pull output 1: GPIO is configured as open-drain output
D2	ENLED3	R/W	0	Enable or Disable High-Current LED3 0: LED3 input is disabled 1: LED3 input is enabled
D1	ENLED2	R/W	1	Enable or disable high-current LED2 0: LED2 input is disabled 1: LED2 input is enabled
D0	ENLED1	R/W	0	Enable or disable high-current LED1 0: LED1 input is disabled 1: LED1 input is enabled

9.6.9 REGISTER6 (address = 0x06)

Figure 60. REGISTER6 Fields

7	6	5	4	3	2	1	0
ENTS	LEDHOT	LEDWARN	LEDHDR	OV			
R/W-0	R/W-0	R-0	R-0	R/W-1	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. REGISTER6 Field Descriptions

Bit	Field	Type	Reset	Description
D7	ENTS	R/W	0	Enable or disable LED temperature monitoring 0: LED temperature monitoring disabled 1: LED temperature monitoring enabled
D6	LEDHOT	R/W	0	LED excessive temperature flag This bit can be reset by writing a logic level zero. 0: TS input voltage > 0.345 V 1: TS input voltage < 0.345 V
D5	LEDWARN	R	0	LED temperature warning flag (read only) This flag is reset after readout. 0: TS input voltage > 1.05 V 1: TS input voltage < 1.05 V
D4	LEDHDR	R	0	LED high-current regulator headroom voltage monitoring This bit returns the headroom voltage status of the LED high-current regulators. This value is being updated at the end of a flash strobe, before to the LED current ramp-down phase. 0: Low headroom voltage 1: Sufficient headroom voltage
D3–D0	OV	R/W	1001	Output voltage selection In read mode, these bits return the result of the high-current LED forward voltage self-calibration procedure. In write mode, these bits are used to set the target output voltage (see *Down Mode In Voltage Regulation Mode*). In applications requiring dynamic voltage control, take care to set the new target code after voltage mode operation is enabled (MODE_CTRL = 11 or ENVM bit = 1). OV: Target output voltage 0000: 3.825 V 0001: 3.950 V 0010: 4.075 V 0011: 4.200 V 0100: 4.325 V 0101: 4.450 V 0110: 4.575 V 0111: 4.700 V 1000: 4.825 V 1001: 4.950 V 1010: 5.075 V 1011: 5.200 V 1100: 5.325 V 1101: 5.450 V 1110: 5.575 V 1111: 5.700 V

9.6.10 REGISTER7 (address = 0x07)

Figure 61. REGISTER7 Fields

7	6	5	4	3	2	1	0
					REVID		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R-1	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. REGISTER7 Field Descriptions

Bit	Field	Type	Reset	Description
D2–D0	REVID	R	110	Silicon Revision ID

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6132x drives up to three white LEDs in parallel. The extended high-current mode (HC_SEL) allows up to 1025-mA and 2050-mA, and 1025-mA flash current out of the storage capacitor. The high-capacity storage capacitor on the output of the boost regulator provides the high-peak flash LED current, thereby reducing the peak current demand from the battery to a minimum.

In the TPS6132x device, the DC-light and flash can be controlled either by the I^2C interface or by the means of hardware control signals (STRB0 and STRB1). The maximum duration of the flashlight pulse can be limited by means of an internal user programmable safety timer (STIM). The DC-light watchdog timer can be disabled by pulling high the STRB1 signal.

10.2 Typical Applications

10.2.1 4100-mA Two White High-Power LED Flashlight With Storage Capacitor

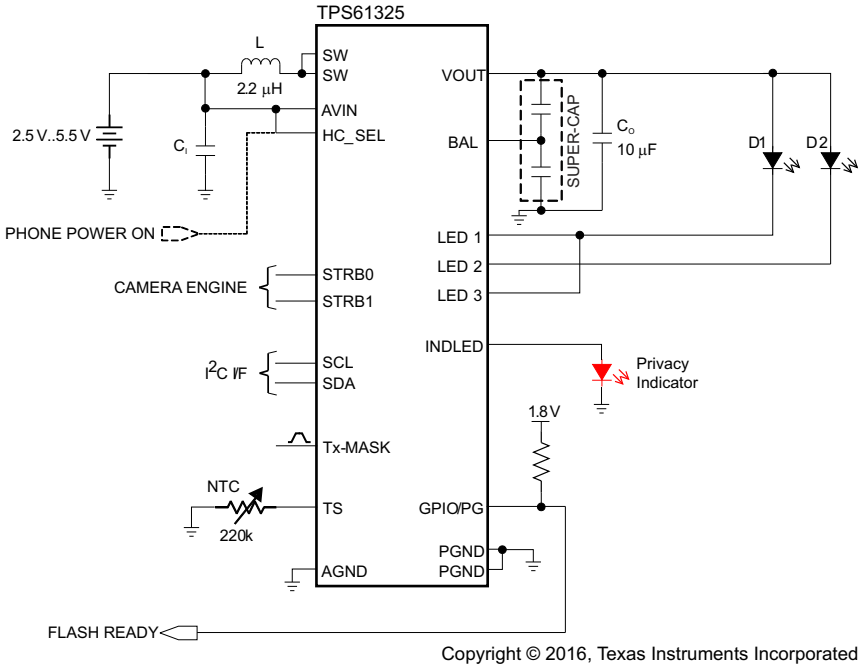


Figure 62. 4100-mA Two High-Power White LED Flashlight With Storage Capacitor Schematic

10.2.1.1 Design Requirements

In this application, the TPS61325 is required to drive a 4100-mA, two high-power white LED, flashlight with an input voltage range of 2.5 V to 5.5 V. This is a high-power LED application, so a storage capacitor is required to maintain sufficient headroom voltage across the LED current regulators for the entire strobe time and also minimize the power dissipation in the device.

Typical Applications (continued)

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Inductor Selection

A boost converter requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. The TPS6132x device integrates a current limit protection circuitry. The valley current of the PMOS rectifier is sensed to limit the maximum current flowing through the synchronous rectifier and the inductor. The valley peak current limit (250 mA, 1150 mA, 1600 mA) is user selectable through the I^2C interface.

To optimize solution size the TPS6132x device is designed to operate with inductance values from 1.3 µH to 2.9 µH. TI recommends 2.2-µH inductance be used in typical high current white LED applications.

The highest peak current through the inductor and the power switch depends on the output load, the input and output voltages. Estimation of the maximum average inductor current and the maximum inductor peak current can be done using Equation 2 and Equation 3:

$$I_L \approx I_{OUT} \times \frac{V_{OUT}}{\eta \times V_{IN}} \quad (2)$$

$$I_{L(PEAK)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1-D) \times \eta} \quad \text{with } D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (3)$$

where

- f = switching frequency (2 MHz)
- L = inductance value (2.2 µH)
- η = estimated efficiency (85%)

The losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

Table 17. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS	ILIM SETTINGS
FDK	MIPST2520	2.5 mm x 2 mm x 0.8 mm (maximum) height	250 mA (typical)
	MIP2520	2.5 mm x 2 mm x 1 mm (maximum) height	
	MIPSA2520	2.5 mm x 2 mm x 1.2 mm (maximum) height	
MURATA	LQM2HP-G0	2.5 mm x 2 mm x 1 mm (maximum) height	
	LQM2HP-GC	2.5 mm x 2 mm x 1 mm (maximum) height	
TDK	VLF3014AT	2.6 mm x 2.8 mm x 1.4 mm (maximum) height	1150 mA (typical)
COILCRAFT	LPS3015	3 mm x 3 mm x 1.5 mm (maximum) height	
MURATA	LQH2HPN	2.5 mm x 2 mm x 1.2 mm (maximum) height	
TOKO	FDSE0312	3 mm x 3 mm x 1.2 mm (maximum) height	1600 mA (typical)
MURATA	LQM32PN	3.2 mm x 2.5 mm x 1.2 mm (maximum) height	

10.2.1.2.2 Input Capacitor

TI recommends low ESR ceramic capacitors for good input voltage filtering. TI recommends a 10-µF input capacitor to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. The input capacitor must be placed as close as possible to the input pin of the converter.

10.2.1.2.3 Output Capacitor

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance required for the defined ripple, supposing that the ESR is zero, by using Equation 4:

$$C_{MIN} \approx \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}}$$

where

- f is the switching frequency
- ΔV is the maximum allowed ripple (4)

With a chosen ripple voltage of 10 mV, a minimum capacitance of 10 µF is required. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 5:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (5)$$

The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. Additional ripple is caused by load transients. This means that the output capacitor must completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change.

For the standard current white LED application (HC_SEL = 0, TPS6132x), a minimum of 3-µF effective output capacitance is usually required when operating with 2.2-µH (typical) inductors. For solution size reasons, this is usually one or more X5R or X7R ceramic capacitors.

Depending on the material, size, and therefore margin to the rated voltage of the used output capacitor, degradation on the effective capacitance can be observed. This loss of capacitance is related to the DC bias voltage applied. TI recommends checking that the selected capacitors are showing enough effective capacitance under real operating conditions.

To support high-current camera flash application (HC_SEL = 1), the converter is designed to work with a low voltage super-capacitor on the output to take advantage of the benefits they offer. A low-voltage super-capacitor in the 0.1-F to 1.5-F range, and with ESR larger than 40 mΩ, is suitable in the TPS6132x application circuit. For this device the output capacitor must be connected between the VOUT pin and a good ground connection.

10.2.1.2.4 NTC Selection

The TPS6132x requires a negative thermistor (NTC) for sensing the LED temperature. Once the temperature monitoring feature is activated, a regulated bias current, approximately 24 µA, is driven out of the TS port and produce a voltage across the thermistor.

If the temperature of the NTC-thermistor rises due to the heat dissipated by the LED, the voltage on the TS input pin decreases. When this voltage goes below the *warning threshold*, the LEDWARN bit in REGISTER6 is set. This flag is cleared by reading the register.

If the voltage on the TS input decreases further and falls below *hot threshold*, the LEDHOT bit in REGISTER6 is set and the device automatically goes into shutdown mode to avoid damaging the LED. This status is latched until the LEDHOT flag gets cleared by software.

The selection of the NTC-thermistor value strongly depends on the power dissipated by the LED and all components surrounding the temperature sensor and on the cooling capabilities of each specific application. With a 220-kΩ (at 25°C) thermistor, the valid temperature window is set from 60°C to 90°C. The temperature window can be enlarged by adding external resistors to the TS pin application circuit. To ensure proper triggering of the LEDWARN and LEDHOT flags in noisy environments, the TS signal may require additional filtering capacitance.

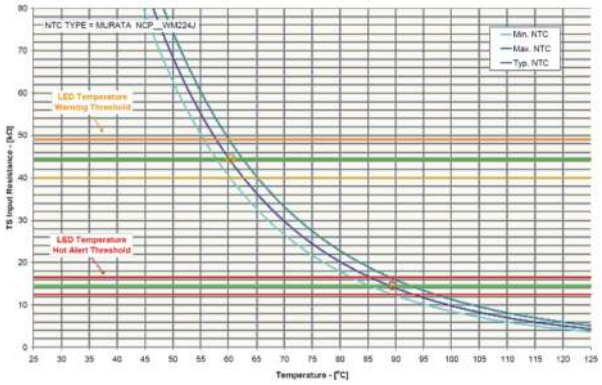


Figure 63. Temperature Monitoring Characteristic

Table 18. List of Negative Thermistor (NTC)

MANUFACTURER	PART NUMBER	VALUE
MURATA	NCP18WM224J03RB	220 kΩ

10.2.1.2.5 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node (SW)
- Inductor current (I_L)
- Output ripple voltage ($V_{OUT(AC)}$)

These are the basic signals that must be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations the regulation loop may be unstable. This is often a result of improper board layout or inductor and capacitor combinations.

The load transient response must be tested as a next step in the evaluation of the regulation loop. V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop usually has more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis must be done over the input voltage range, output current range, and temperature range.

10.2.1.3 Application Curves

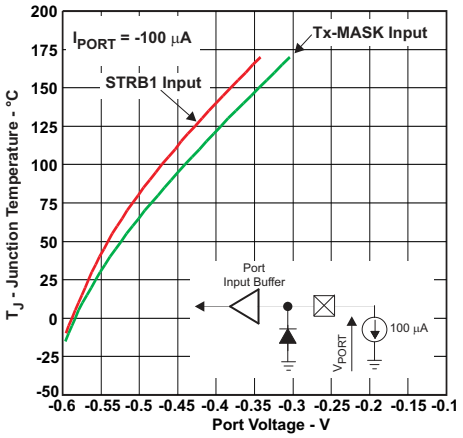


Figure 64. Junction Temperature vs Port Voltage

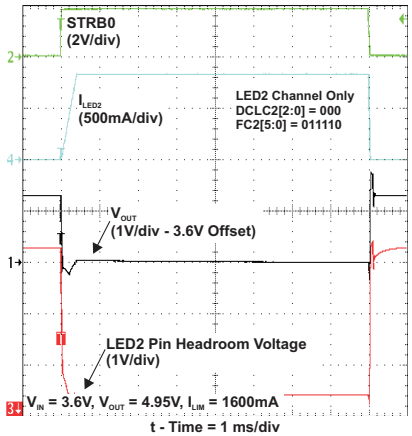


Figure 65. Flash Sequence (HC_SEL = 0)

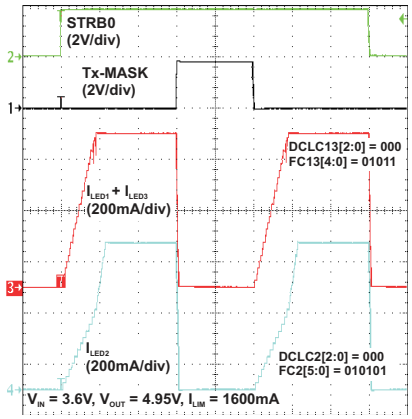


Figure 66. Tx-Masking Operation (HC_SEL = 0)

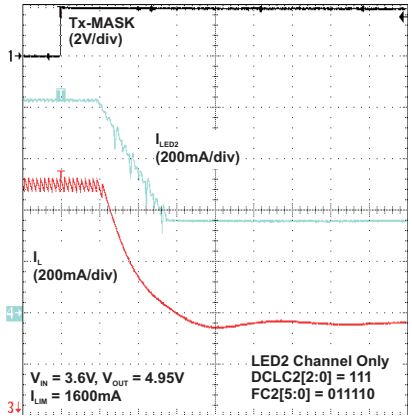


Figure 67. Tx-Masking Operation (HC_SEL = 0)

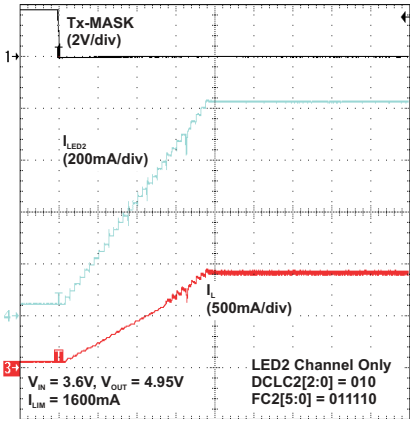


Figure 68. Tx-Masking Operation (HC_SEL = 0)

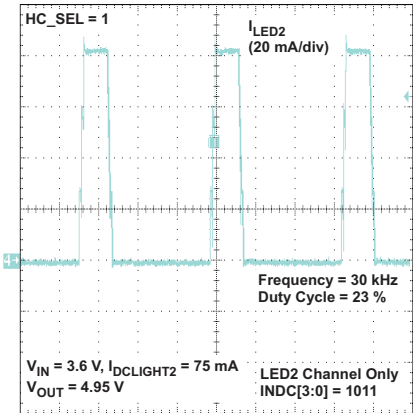


Figure 69. Low-LIGHT Dimming Mode Operation

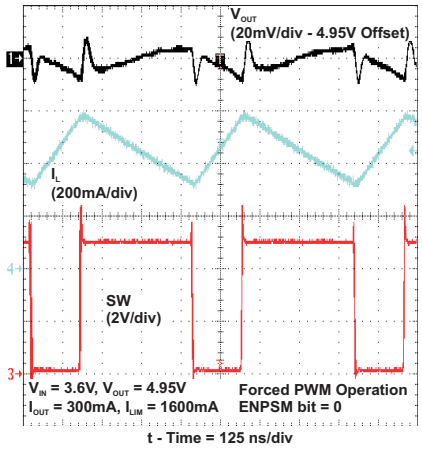


Figure 70. PWM Operation

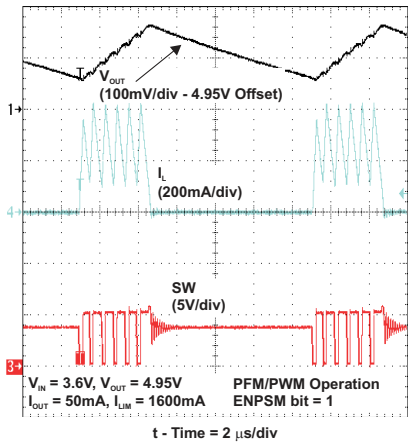


Figure 71. PFM Operation

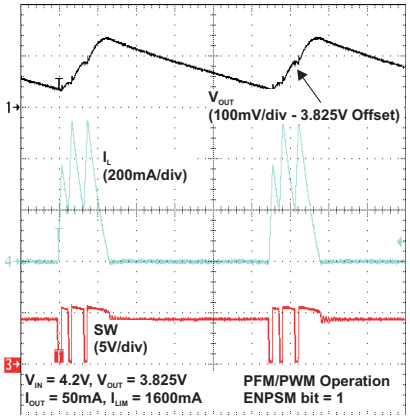


Figure 72. Down-Mode Operation (Voltage Mode)

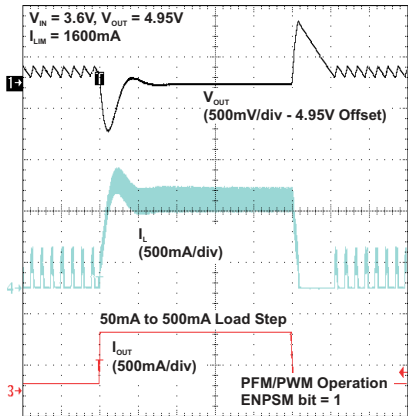


Figure 73. Voltage Mode Load Transient Response

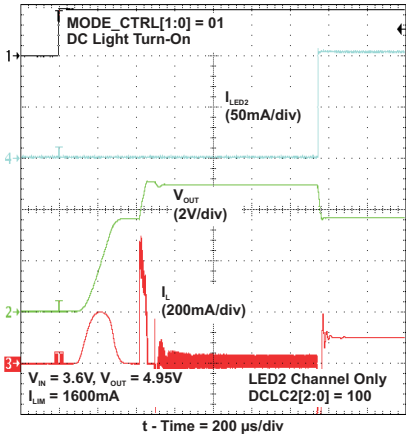


Figure 74. Start-Up Into DC-Light Operation

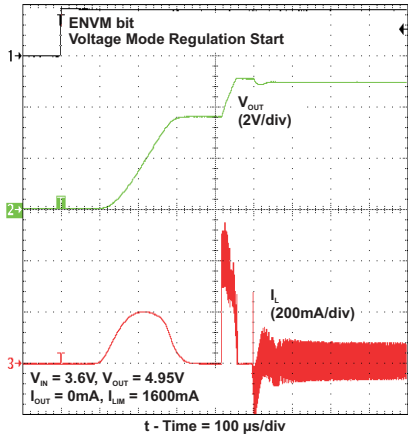


Figure 75. Start-Up Into Voltage Mode Operation

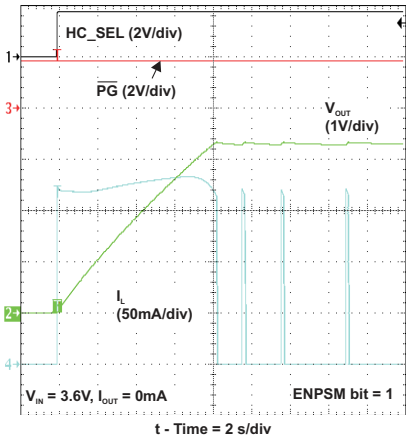


Figure 76. Storage Capacitor Precharge (HC_SEL = 1)

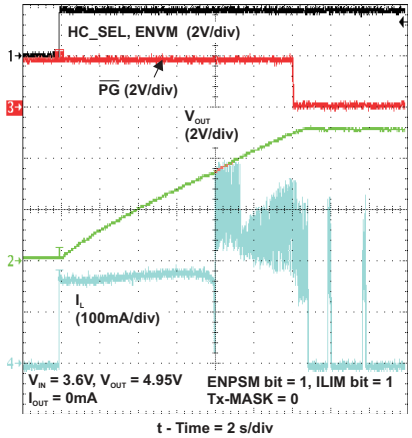


Figure 77. Storage Capacitor Charge-Up (HC_SEL = 1)

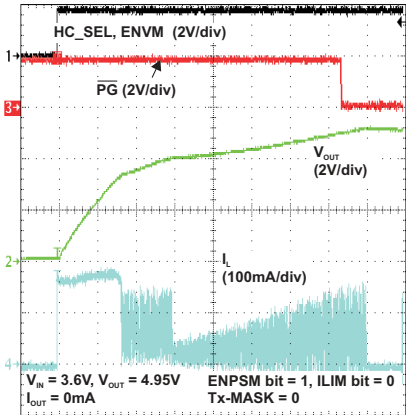


Figure 78. Storage Capacitor Charge-Up (HC_SEL = 1)

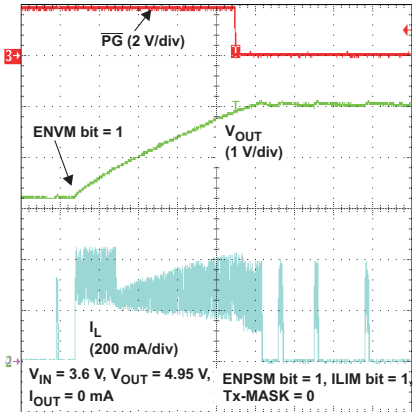


Figure 79. Storage Capacitor Charge-Up (HC_SEL = 1)

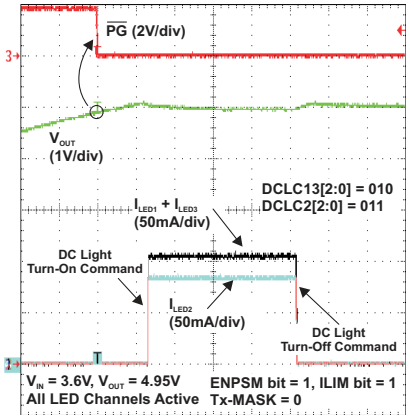


Figure 80. DC-Light Operation (HC_SEL = 1)

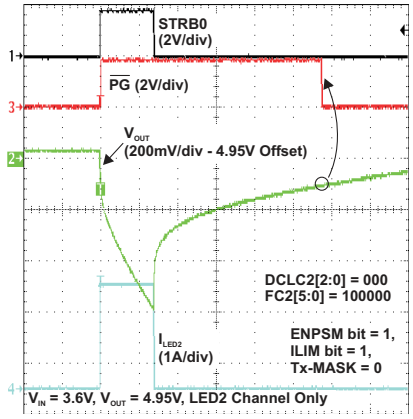


Figure 81. Flash Sequence (HC_SEL = 1)

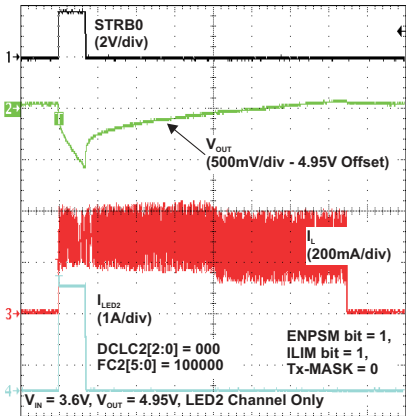


Figure 82. Flash Sequence (HC_SEL = 1)

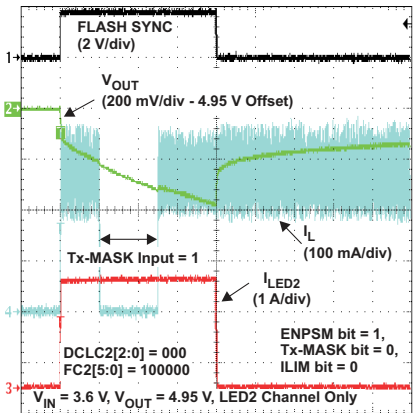


Figure 83. Flash Sequence (HC_SEL = 1)

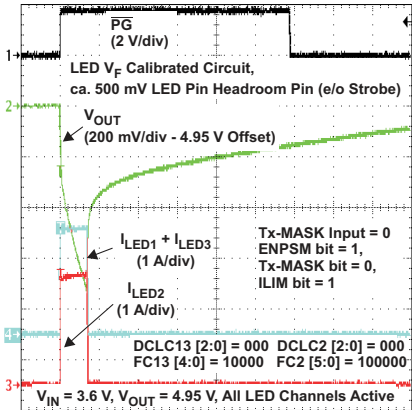


Figure 84. Flash Sequence (HC_SEL = 1)

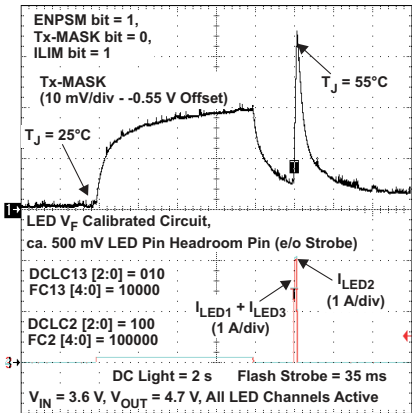


Figure 85. Junction Temperature Monitoring (HC_SEL = 1)

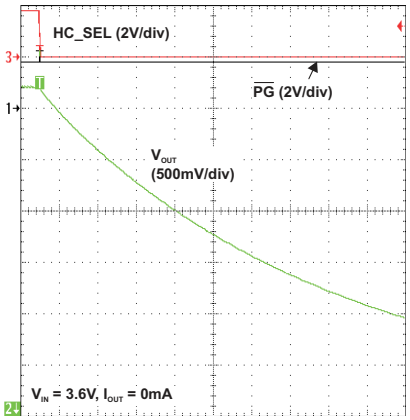


Figure 86. Shutdown (HC_SEL = 1)

10.2.2 Other Application Circuit Examples

Figure 87 and Figure 88 show application circuit examples using the TPS61325 device. Customers must fully validate and test these circuits before implementing a design based on these examples.

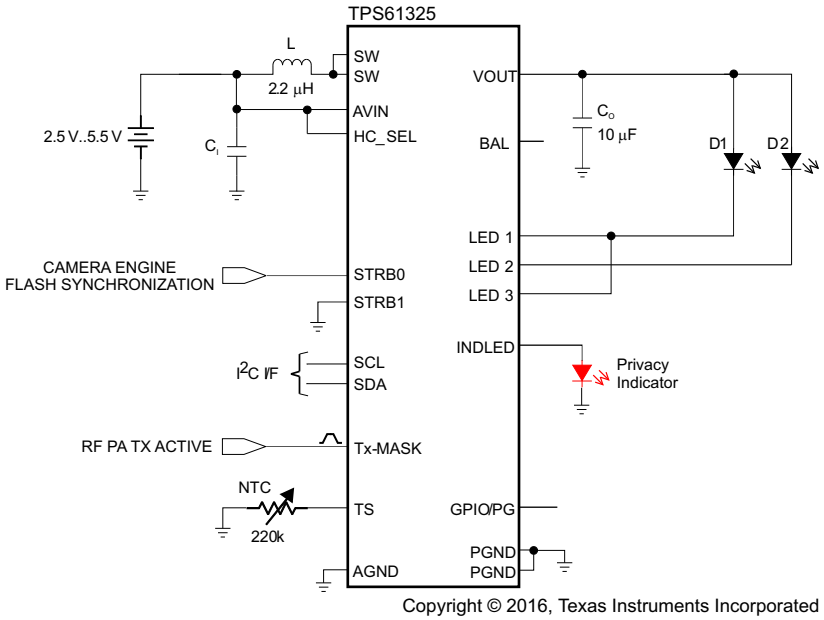


Figure 87. 2x 600-mA High Power White LED Solution With Privacy Indicator Schematic

In this application, TPS61325 is used to drive two 600-mA white LEDs. A storage capacitor is not necessary because the LED current can be supplied by the TPS61325 directly. The privacy indicator is turned on.

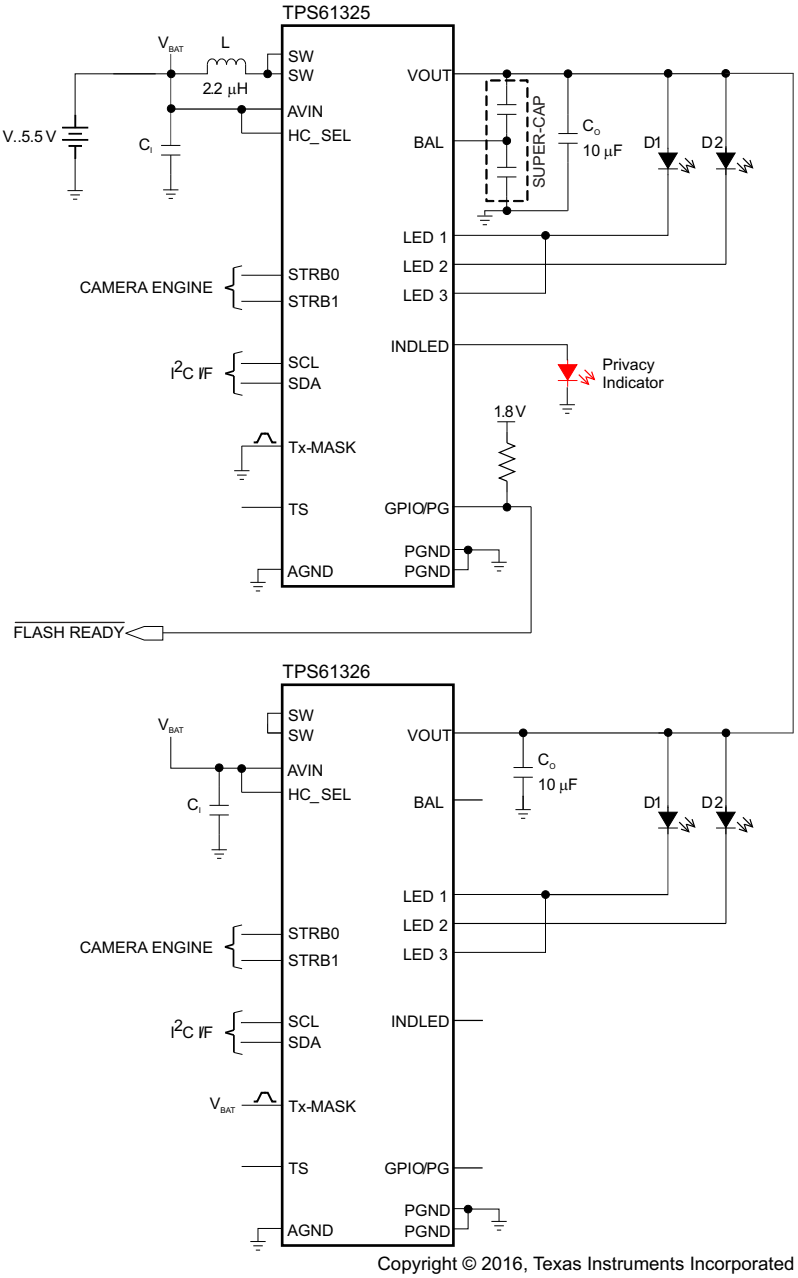


Figure 88. 8200-mA Four High-Power White LED Flashlight With Storage Capacitor Schematic

In this application, it is required to drive a 8200-mA, four high-power white LED, flashlight. Because it is beyond the driving capability of the TPS61325, two devices are connected in parallel to drive the LED flashlight. One works as a master with a storage capacitor, and the other works as a slave.

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. TI recommends an electrolytic or tantalum capacitor with a value of 47 µF in this circumstance.

12 Layout

12.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks.

The input capacitor, output capacitor, and the inductor must be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

TI recommends using short traces to lay out the control ground, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power-ground current and control-ground current.

12.2 Layout Example

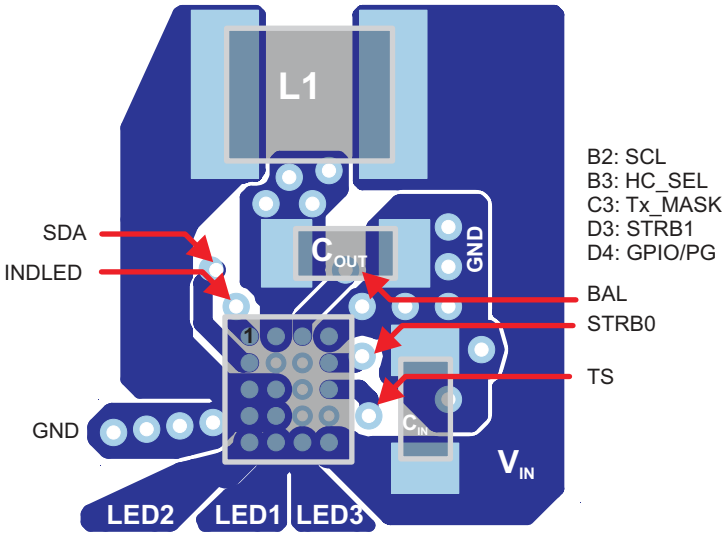


Figure 89. Suggested Layout (Top)

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, pay special attention to thermal dissipation issues in board design. The maximum junction temperature (T_J) of the TPS6132x is 150°C.

The maximum power dissipation is especially critical when the device operates in the linear down mode at high LED current. For single pulse power thermal analysis, for example, flashlight strobe, the allowable power dissipation for the device is given by Figure 90. These values are derived using the reference design.

Thermal Considerations (continued)

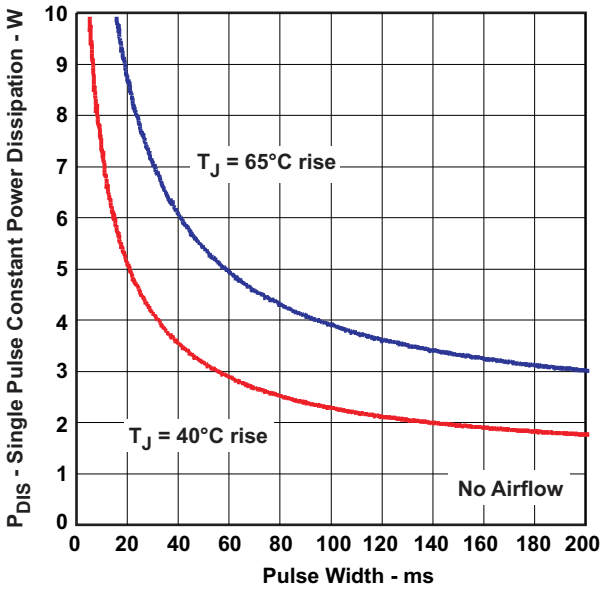


Figure 90. Single Pulse Power Capability

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

UM10204, I^2C-Bus Specification and User Manual; (Rev. 6, April 2014),
http://www.nxp.com/documents/user_manual/UM10204.pdf

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61325YFFR	ACTIVE	DSBGA	YFF	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61325	Samples
TPS61325YFFT	ACTIVE	DSBGA	YFF	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61325	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

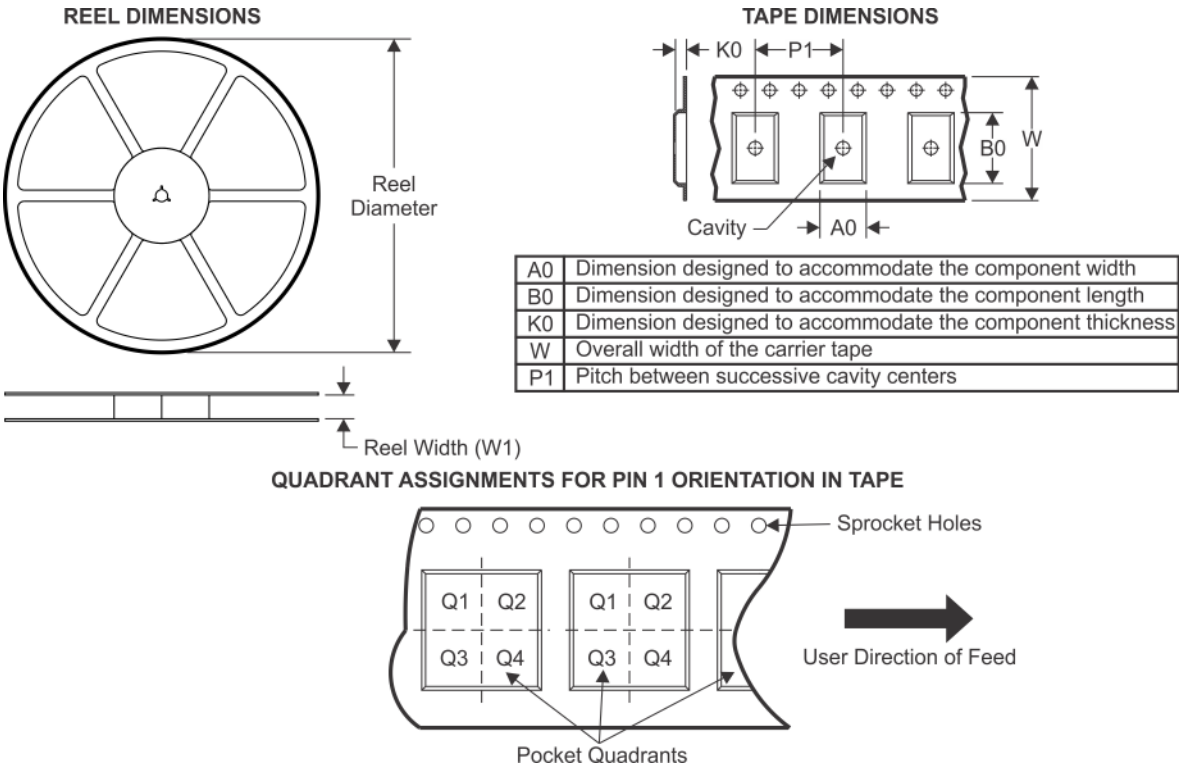
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

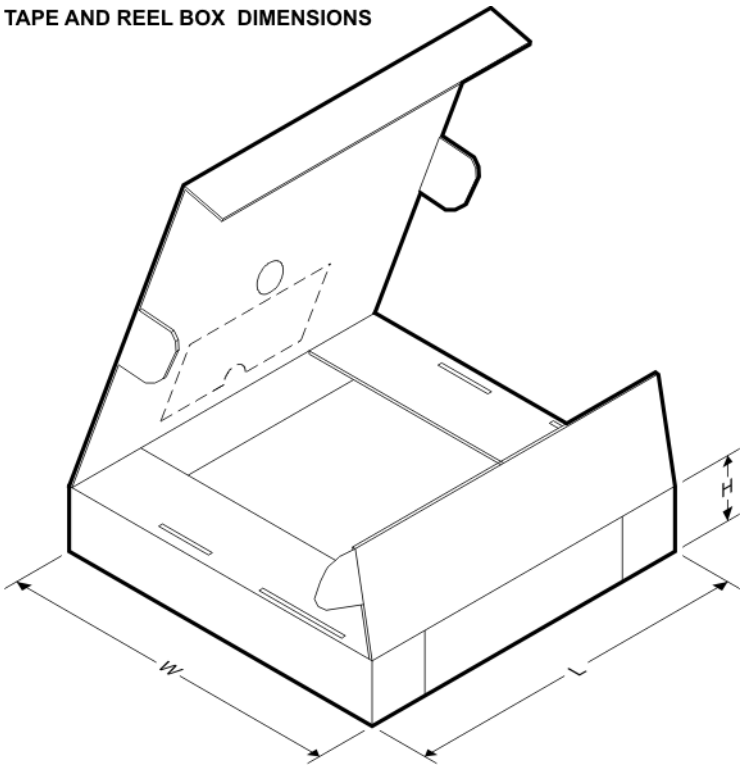


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61325YFFR	DSBGA	YFF	20	3000	180.0	8.4	2.2	2.35	0.8	4.0	8.0	Q1
TPS61325YFFT	DSBGA	YFF	20	250	180.0	8.4	2.2	2.35	0.8	4.0	8.0	Q1

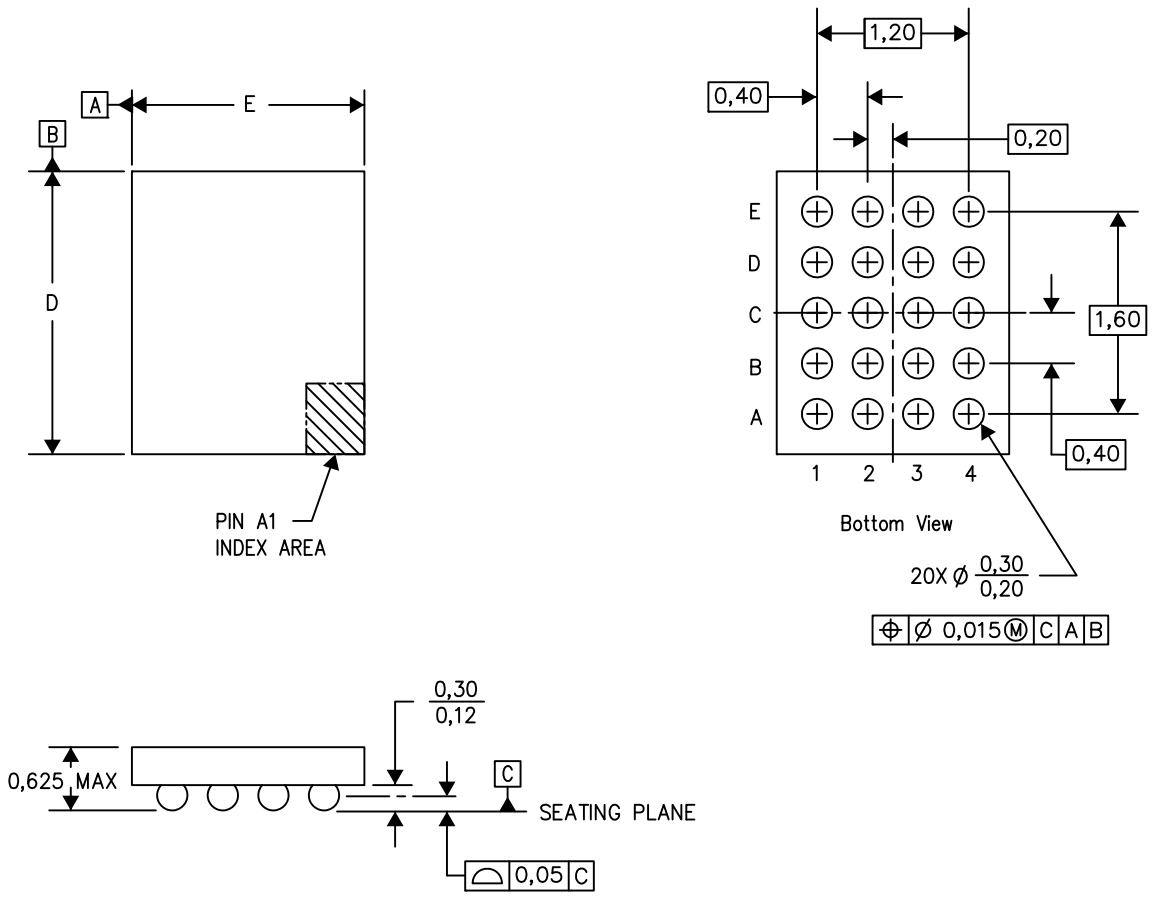
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61325YFFR	DSBGA	YFF	20	3000	182.0	182.0	20.0
TPS61325YFFT	DSBGA	YFF	20	250	182.0	182.0	20.0

YFF (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



D: Max = 2.2 mm, Min = 2.14 mm

E: Max = 1.958 mm, Min =1.898 mm

4207625–9/AO 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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