Description

The 8V19N478 is a fully integrated FemtoClock NG jitter attenuator and clock synthesizer designed as a high-performance clock solution for conditioning and frequency/phase management of 10/40/100/400 Gigabit-Ethernet line cards. The device is optimized to deliver excellent phase noise performance as required to drive physical layer devices, and provides the clean clock frequencies of 625MHz, 500MHz, 312.5MHz, 250MHz, 156.25MHz, and 125MHz.

A two-stage PLL architecture supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator, and uses an external VCXO for best possible phase noise characteristics. The second stage PLL locks on the VCXO-PLL output signal, and synthesizes the target frequency. This PLL has a VCO circuit at 2500MHz.

The 8V19N478 generates the output clock signals from the VCO by frequency division. Four independent frequency dividers are available; three support integer-divider ratios, and one integer as well as fractional-divider ratios. Delay circuits can be used for achieving alignment and controlled phase delay between clock signals. The two redundant inputs are monitored for activity. Four selectable clock switching modes are provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers, and phase adjustment capabilities are added for flexibility.

The device is configured through an I^2C interface and reports lock and signal loss status in internal registers and via a lock detect (LOCK) output. Internal status bit changes can also be reported via the nINT output. The device is ideal for driving converter circuits in wireless infrastructure, radar/imaging, and instrumentation/medical applications. The device is a member of the high-performance clock family from IDT.

Typical Applications

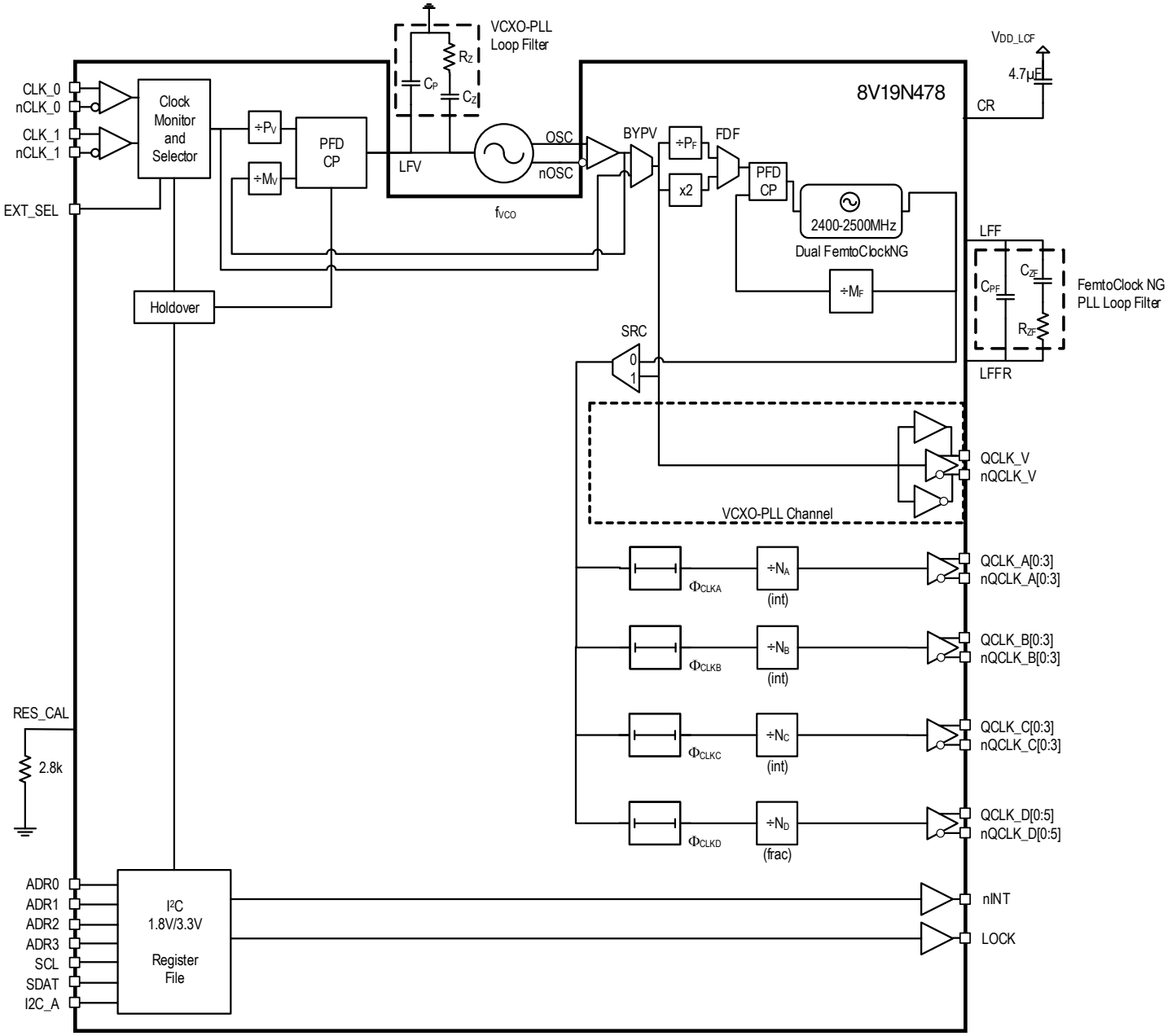
- Sub 70fs – low phase noise clock generation
- 10/40/100 Gigabit-Ethernet line cards
- Wireless Infrastructure
- Reference clock for ADC and DAC circuits
- Radar and Imaging
- Instrumentation and Medical

Features

- High-performance clock RF-PLL:
  - Optimized for low phase noise: -157.7dBc/Hz (1MHz offset; 156.25MHz clock), design target
  - Integrated phase noise, RMS (12kHz–20MHz): 73fs (typical), design target
- Dual-PLL architecture:
  - 1st-PLL stage with external VCXO for clock jitter attenuation
  - 2nd-PLL stage with internal FemtoClock NG PLL at 2500MHz
- Four output banks with a total of 18 outputs, organized in:
  - Three clock banks with one integer frequency divider and four differential outputs
  - One clock bank with one fractional divider and six differential outputs
  - One VCXO-PLL output bank with one selectable LVDS and two LVCMOS outputs
- Four output banks contain a phase delay circuit with steps of the VCO clock period (400ps)
- Supported clock output frequencies include:
  - From the integer dividers: 2500MHz, 1250MHz, 625MHz, 500MHz, 312.5MHz, 250MHz, 156.25MHz, and 125MHz
  - From the fractional divider: 80–300MHz
- Low-power LVPECL and LVDS outputs support configurable signal amplitude, DC and AC coupling, and LVPECL, LVDS, and line termination techniques
- Redundant input clock architecture:
  - Two inputs
  - Individual input signal monitor
  - Digital holdover
  - Manual and automatic clock selection
  - Hitless switching
- Status monitoring and fault reporting:
  - Input signal status
  - Hold-over and reference loss status
  - Lock status with one status pin
  - Mask-able status interrupt pin
- Voltage supply:
  - Device core supply voltage: 3.3V
  - Output supply voltage: 3.3V, 2.5V, or 1.8V
  - I/O voltage: 1.8V or 3.3V (selectable), and 3.3V tolerant inputs when set to 1.8V
- Package: 11 × 11 × 1 mm ball pitch 100-FPBGA
- Temperature range: -40°C to +85°C

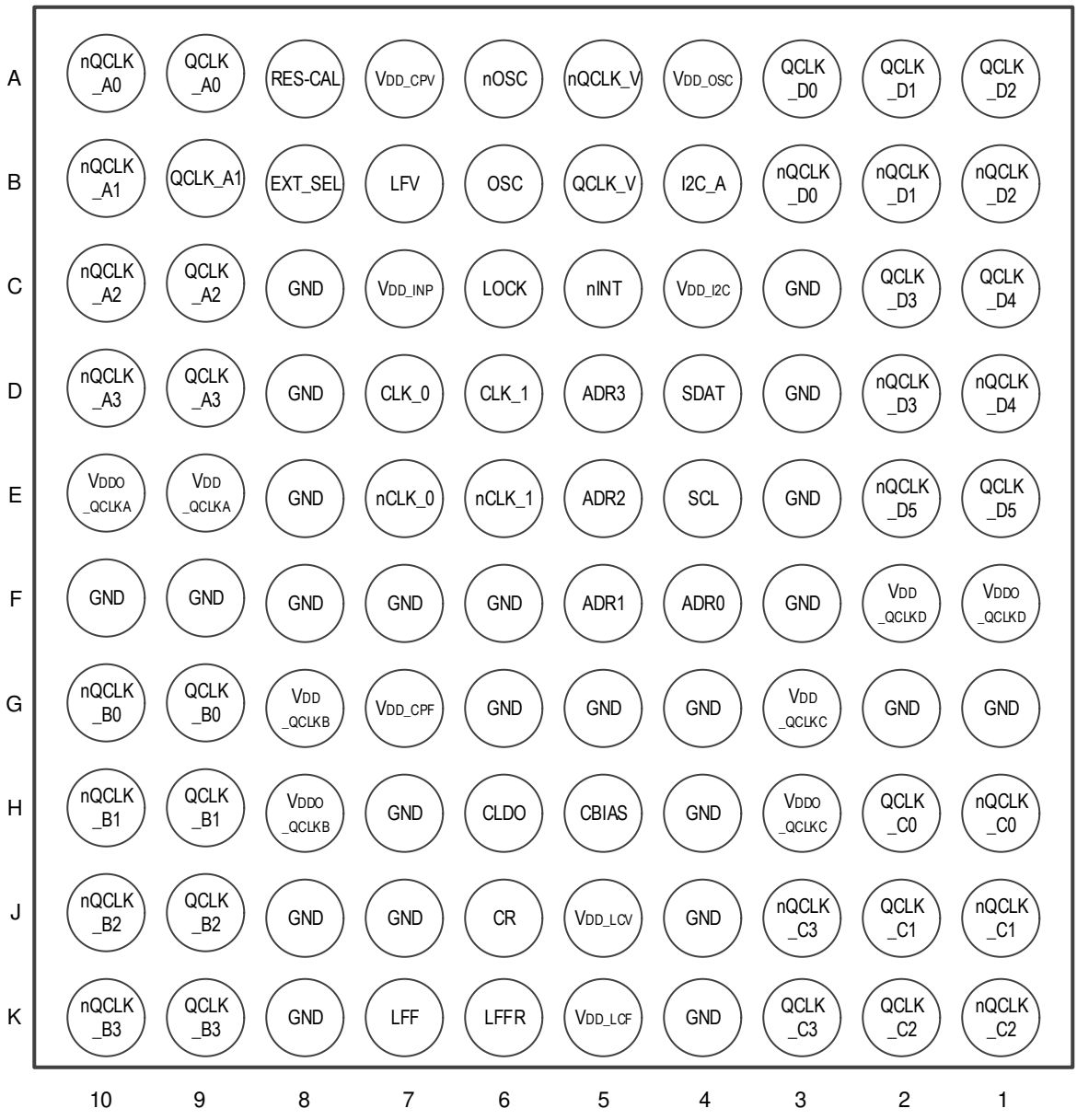
Contents

Block Diagram



Pin Assignments

Figure 1. Pin Assignments for 11 × 11 × 1 mm, 100-FPBGA Package (Bottom View)



Pin Descriptions

Table 1. Pin Descriptions [a]

Ball	Name	Type[b]	Description
A10	nQCLK_A0	Output	Differential clock output A0 (Channel A). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKA} supply voltage.
A9	QCLK_A0	Output	
A8	RES_CAL	Analog	Connect a 2.8kΩ (1%) resistor to GND for output current calibration.
A7	V_{DD_CPV}	Power	Positive supply voltage (3.3V) for internal VCXO_PLL circuits.
A6	nOSC	Input (PD/ PU)	VCXO non-inverting and inverting differential clock input. Compatible with LVPECL, LVDS and LVCMOS signals.
A5	nQCLK_V	Output	Differential VCXO-PLL clock outputs. Selectable LVPECL, LVDS (2x LVCMOS 1.8V) style.
A4	V_{DD_OSC}	Power	Positive supply voltage (3.3V) for the VCXO input.
A3	QCLK_D0	Output	Differential clock output D0 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
A2	QCLK_D1	Output	Differential clock output D1 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
A1	QCLK_D2	Output	Differential clock output D2 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
B10	nQCLK_A1	Output	Differential clock output A1 (Channel A). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKA} supply voltage.
B9	QCLK_A1	Output	
B8	EXT_SEL	Input (PD)	Clock reference select. 1.8V interface levels with hysteresis and 3.3V tolerance.
B7	LFV	Output	VCXO-PLL charge-pump output. Connect to the loop filter for the external VCXO.
B6	OSC	Input (PD)	VCXO non-inverting and inverting differential clock input. Compatible with LVPECL, LVDS and LVCMOS signals.
B5	QCLK_V	Output	Differential VCXO-PLL clock outputs. Selectable LVPECL, LVDS/(2x LVCMOS 1.8V) style.
B4	I2C_A	Input (PD/ PU)	Serial Interface I^2C addresses. Three-level signals (see Table 15).
B3	nQCLK_D0	Output	Differential clock output D0 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
B2	nQCLK_D1	Output	Differential clock output D1 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
B1	nQCLK_D2	Output	Differential clock output D2 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
C10	nQCLK_A2	Output	Differential clock output A2 (Channel A). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKA} supply voltage.
C9	QCLK_A2	Output	
C8	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
C7	V_{DD_INP}	Power	Positive supply voltage (3.3V) for the differential inputs (CLK[1:0]).
C6	LOCK	Output	PLL lock detect status output for both PLLs. Selectable 1.8V/3.3V LVCMOS/LVTTL interface levels.
C5	nINT	Output	Status output pin for signaling internal changed conditions. Selectable 1.8V/3.3V LVCMOS/LVTTL interface levels.

Table 1. Pin Descriptions (Cont.)[a]

Ball	Name	Type[b]	Description
C4	V_{DD_I2C}	Power	Positive supply voltage (3.3V) for I2C_A.
C3	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
C2	QCLK_D3	Output	Differential clock output D3 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
C1	QCLK_D4	Output	Differential clock output D4 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
D10	nQCLK_A3	Output	Differential clock output A3 (Channel A). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKA} supply voltage.
D9	QCLK_A3	Output	
D8	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
D7	CLK_0	Input (PD)	Device clock 0 inverting and non-inverting differential clock input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
D6	CLK_1	Input (PD)	Device clock 1 inverting and non-inverting differential clock input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
D5	ADR3	Input (PU/PD)	Device mode selection (see Table 12).
D4	SDAT	I/O (PU)	I^2C data input/output. 1.8V interface levels with hysteresis and 3.3V tolerance
D3	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
D2	nQCLK_D3	Output	Differential clock output D3 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
D1	nQCLK_D4	Output	Differential clock output D4 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
E10	V_{DDO_QCLKA}	Power	Output power supply voltage (3.3V, 2.5V or 1.8V) for the QCLK_A[3:0] outputs.
E9	V_{DD_QCLKA}	Power	Positive supply voltage (3.3V) for Channel A.
E8	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
E7	nCLK_0	Input (PD/ PU)	Device clock 0 inverting and non-inverting differential clock input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
E6	nCLK_1	Input (PD/ PU)	Device clock 1 inverting and non-inverting differential clock input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
E5	ADR2	Input (PD/ PU)	Control input for output Bank D. 3-level signal (see Table 12 and Table 14).
E4	SCL	Input (PU)	I^2C clock input. 1.8V interface levels with hysteresis and 3.3V tolerance.
E3	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
E2	nQCLK_D5	Output	Differential clock output D5 (Channel D). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKD} supply voltage.
E1	QCLK_D5	Output	
F10	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
F9	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
F8	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).

Table 1. Pin Descriptions (Cont.)[a]

Ball	Name	Type[b]	Description
F7	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
F6	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
F5	ADR1	Input (PD/ PU)	Control input for output Bank B. 3-level signal (see Table 12 and Table 14).
F4	ADR0	Input (PD/ PU)	Control input for output Bank A and Bank C. Three-level signal (see Table 12 and Table 14).
F3	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
F2	V_{DD_QCLKD}	Power	Positive supply voltage (3.3V) for Channel D.
F1	V_{DDO_QCLKD}	Power	Output power supply voltage (3.3V, 2.5V or 1.8V) for the QCLK_D[5:0] outputs.
G10	nQCLK_B0	Output	Differential clock output B0 (Channel B). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKB} supply voltage.
G9	QCLK_B0	Output	
G8	V_{DD_QCLKB}	Power	Positive supply voltage (3.3V) for Channel B.
G7	V_{DD_CPF}	Power	Positive supply voltage (3.3V) for internal FemtoClock NG circuits.
G6	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
G5	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
G4	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
G3	V_{DD_QCLKC}	Power	Positive supply voltage (3.3V) for Channel C.
G2	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
G1	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
H10	nQCLK_B1	Output	Differential clock output B1 (Channel B). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKB} supply voltage.
H9	QCLK_B1	Output	
H8	V_{DDO_QCLKB}	Power	Output power supply voltage (3.3V, 2.5V or 1.8V) for the QCLK_B[3:0] outputs.
H7	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
H6	CLDO	Analog	Analog internal LDO bypass for VCO. Connect a 10µF capacitor to GND.
H5	CBIAS	Analog	Internal bias circuit for VCO. Connect a 4.7µF capacitor to GND.
H4	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
H3	V_{DDO_QCLKC}	Power	Output power supply voltage (3.3V, 2.5V or 1.8V) for the QCLK_C[3:0] outputs.
H2	QCLK_C0	Output	Differential clock output C0 (Channel C). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKC} supply voltage.
H1	nQCLK_C0	Output	
J10	nQCLK_B2	Output	Differential clock output B2 (Channel B). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKB} supply voltage.
J9	QCLK_B2	Output	
J8	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
J7	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
J6	CR	Analog	Internal VCO regulator bypass capacitor. Use a 4.7µF capacitor between the CR and the V_{DD_LCF} terminals.
J5	V_{DD_LCV}	Power	Positive supply voltage (3.3V) for the VCXO-PLL.
J4	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).

Table 1. Pin Descriptions (Cont.)[a]

Ball	Name	Type[b]	Description
J3	nQCLK_C3	Output	Differential clock output C3 (Channel C). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKC} supply voltage.
J2	QCLK_C1	Output	Differential clock output C1 (Channel C). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKC} supply voltage.
J1	nQCLK_C1	Output	
K10	nQCLK_B3	Output	Differential clock output B3 (Channel B). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKB} supply voltage.
K9	QCLK_B3	Output	
K8	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
K7	LFF	Output	Loop filter/charge-pump output for the FemtoClock NG PLL. Connect to the external loop filter.
K6	LFFR	Analog	Ground return path pin for the VCO loop filter.
K5	V_{DD_LCF}	Power	Positive supply voltage (3.3V) for the internal oscillator of the FemtoClock NG PLL. For essential information on power supply filtering, see Power Supply Filtering.
K4	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
K3	nQCLK_C3	Output	Differential clock output C3 (Channel C). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKC} supply voltage.
K2	QCLK_C2	Output	Differential clock output C2 (Channel C). Configurable LVPECL, LVDS style and amplitude. Output levels are determined by the V_{DDO_QCLKC} supply voltage.
K1	nQCLK_C2	Output	

[a] For essential information on power supply filtering, see Power Supply Filtering.

[b] Pull-up (PU) and pull-down (PD) internal input resistors are indicated in parentheses. For typical values, see *Input Characteristics,* Table 41.

Principles of Operation

Overview

The device generates low-phase noise, synchronized clock output signals locked to an input reference frequency. The device contains two PLLs with configurable frequency dividers. The first PLL (VCXO-PLL, suffix V) uses an external VCXO as the oscillator and provides jitter attenuation. The external loop filter is used to set the VCXO-PLL bandwidth frequency in conjunction with internal parameters. The second, low-phase noise PLL (FemtoClock NG, suffix F) multiplies the VCXO-PLL frequency to the VCO frequency of 2500MHz. The FemtoClock NG PLL is completely internal and provides a central reference timing reference point for all output signals. From this point, fully synchronous dividers generate the output frequencies.

The device has four output channels A – D, four channels with one integer output divider A – C and one channel with a fractional output divider (D). The clock outputs are configurable with support for LVPECL and LVDS formats, and a variable output amplitude. In channels A – D, the clock phase can be adjusted in phase. Individual outputs, channels, and unused circuit blocks support powered-down states for operation at reduced power consumption. The register map, accessible through a selectable I^2C interface with read-back capability controls the main device settings and delivers device status information. For redundancy purpose, there are two selectable reference frequency inputs and a configurable switch logic with manual, auto-selection, and holdover support.

Phase-Locked Loop Operation

Frequency Generation

The 8V19N478 supports four operation modes: Dual-PLL and VCXO-PLL with jitter attenuation, frequency synthesis, and the buffer/divider mode. Frequencies higher than the input frequency can be generated by the device by utilizing one or both PLLs. Using the PLL(s) require(s) the user to set the frequency dividers to match input, VCXO and VCO frequency and to achieve frequency and phase lock on the used PLLs. The frequency of the external VCXO is chosen by the user. The internal VCO frequency range is 2400–2500MHz. Available frequency dividers for each of the four modes are displayed in Table 2. Example divider configurations are shown in Table 3 and Table 4.

Dual-PLL Jitter Attenuation Mode: Input clock jitter is attenuated by the VCXO-PLL (1st stage PLL). The 2nd stage PLL (FemtoClock NG) is locked to the 1st stage PLL and synthesizes a frequency in the range of 2400–2500MHz. Output dividers scale the frequency down to the target frequency. Dividers P_V, M_V, P_F, M_F, N_x, and (optionally) N_D require a user configuration. This is the main operation mode of the device with the highest flexibility in frequency generation. Best phase noise is achieved with internal frequency doubler turned on.

VCXO-PLL Jitter Attenuation Mode: Input clock jitter is attenuated by the VCXO-PLL (1st stage PLL). The VCXO-output signal is divided by the output dividers to the target frequency. Dividers P_V, M_V, and N_x require a user configuration. The VCXO sets the highest frequency the device can achieve. The output phase noise is equivalent to the phase noise of the VCXO scaled by the output divider.

Frequency Synthesis Mode: The 1st stage PLL is bypassed. The 2nd stage PLL (FemtoClock NG) is directly locked to the input source and synthesizes a frequency in the range of 2400–2500MHz. output dividers scale the frequency down to the target frequency. Dividers P_V, P_F, M_F, N_x, and (optionally) N_D require a user configuration. This mode is recommend for applications with a low-jitter input source.

Divider/Buffer Mode: Both PLLs are bypassed. Output dividers scale the input frequency to the target frequency. Dividers P_V and N_x require a user configuration. In this mode, the PLL frequency specifications do not apply.

Table 2. PLL Divider Values

Divider	Range	Operation			
		Jitter Attenuation		Frequency Synthesis	Divider/Buffer
		Dual-PLL (BYPV = 0, SRC = 0)	VCXO-PLL (BYPV = 0, SRC = 1)	VCXO-PLL bypassed (BYPV = 1, SRC = 0)	Both PLLs bypassed (BYPV = 1, SRC = 1)
VCXO-PLL Pre-Divider P_V[a]	÷1…÷32767: (15 bit)	Input clock frequency $f_{CLK} = \frac{f_{VCXO}}{M_V} \times P_V$		No external VCXO required	
VCXO-PLL Feedback Divider M_V	÷1…÷32767: (15 bit)				
FemtoClock NG Pre-Divider P_F	÷1…÷63: (6 bit)	VCXO frequency: $f_{VCXO} = f_{VCO} \times \frac{P_F}{M_F}$ f_{VCO}: Note[b] P_F: Note[c]	—	Input clock frequency: $f_{CLK} = f_{VCO} \times \frac{P_F}{M_F}$ f_{VCO}: Note[b] P_F: Note[c]	Output frequency $f_{OUT} = \frac{f_{CLK}}{N_X \times P_V}$
FemtoClock NG Feedback Dividers M_F	÷8 …÷511: (9 bit)				
Output Divider N*x* (*x* = [A:C])	÷1…÷160: (Integer)[d]	Output frequency $f_{OUT} = \frac{f_{VCO}}{N_X}$	Output frequency $f_{OUT} = \frac{f_{VCXO}}{N_X}$	Output frequency $f_{OUT} = \frac{f_{VCO}}{N_X}$	
Output Divider ND	Fractional Divider[e]: N_{INT}: 4…2^4 – 1: (Integer part) N_{FRAC}: 1…2^{24} – 1: (Fractional part)	Output frequency $f_{OUT} = \frac{f_{VCO}}{N_E}$ $N_E = 2 \times \left(N_{INT} + \frac{N_{FRAC}}{2^{24}}\right)$	—		

[a] P_V divider settings are in the *PV0 register* (for CLK_0), and in the *PV1 register* (for CLK_1). The PV divider is automatically loaded from PV0 or PV1 according to the input selection (Clock Selection Settings, Table 11).

[b] f_{VCO} = 2400–2500MHz.

[c] Set P_F to 0.5 in the equation if the frequency doubler is engaged (FDF = 1).

[d] For a list of supported integer output dividers N*x* (Table 8).

[e] Greatest N*D* fractional divider is 2 × (14 + [2^{24} – 1] / 2^{24}) ≈ 29.99999988.

VCXO-PLL

The prescaler P_V and the VCXO-PLLs feedback divider M_V require configuration to match the input frequency to the VCXO-frequency. With the M_V and P_V divider value range of 15 bit, the device support is very flexible and supports a wide range of input and VCXO-frequencies.

In addition, the range of available inputs and feedback dividers allow to adjust the phase detector frequency independent of the used input and VCXO frequencies (Table 3 and Table 4). The VCXO-PLL charge-pump current is controllable via internal registers, and can be set in 50µA steps, from 50µA to 1.6mA. The VCXO-PLL can be bypassed (BYPV): when in bypass, the FemtoClock NG PLL locks to the pre-divided input frequency.

Table 3. Example Configurations for f_{VCXO} = 125MHz

Input Frequency (MHz)	VCXO-PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
19.44	486	3125	0.04
25	1	5	20
	4	20	5
	16	80	1.25
	64	320	0.390625
125	1	1	125
	5	5	25
	25	25	5
	125	125	1
156.25	5	4	31.25
	50	40	3.125
	500	400	0.3125

Table 4. Example Configurations for f_{VCXO} = 156.25MHz

Input Frequency (MHz)	VCXO- PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
19.44	1944	15625	0.01
20	400	3125	0.05
25	4	25	6.25
	40	250	0.625
	400	2500	0.0625
125	4	5	31.25
	40	50	3.125
	400	500	0.3125
156.25	1	1	156.25
	10	10	15.625
	100	100	1.5625

Table 5. VCXO-PLL Bypass Settings

BYPV	Operation
0	VCXO-PLL operation.
1	VCXO-PLL bypassed and disabled. The reference clock for the FemtoClock NG PLL is the selected input clock. The input clock selection must be set to manual by the user. Clock switching and holdover are not defined. The device synthesizes an output frequency, but will not attenuate input jitter. An external VCXO component and loop filter is not required.

FemtoClock NG PLL

The FemtoClock NG PLL is the second stage PLL, and locks to the output signal of the VCXO-PLL (BYPV = 0). It requires configuration from the frequency doubler FDF, or the pre-divider PF and the feedback divider MF to match the VCXO-PLL frequency to the VCO frequency of 2500MHz. Best phase noise is typically achieved by engaging the internal frequency doubler (FDF = 1, ×2). If engaged, the signal from the first PLL stage is doubled in frequency, increasing the phase detector frequency of the FemtoClock NG PLL. When the frequency doubler is enabled, the frequency pre-divider PF is disabled. If the frequency doubler is not used (FDF = 0), the PF pre-divider has to be configured. Typically, the PF is set to ÷1 to keep the phase detector frequency as high as possible. Set the PF to other divider values to achieve specific frequency ratios between the first and second PLL stage. This PLL is internally configured to high-bandwidth.

Table 6. Frequency Doubler

FDF	Operation
0	Frequency doubler off. The PF divides the clock signal from the VCXO-PLL or input (in bypass).
1	Frequency doubler on (×2). A signal from the VCXO-PLL or input (in bypass) is doubled in frequency. The PF divider has no effect.

Table 7. Example PLL Configurations

VCXO-Frequency (MHz)	FemtoClock NG Divider Settings for VCO = 2500MHz		
	FDF	PF	MF
25	×2	–	50
125	×2	–	10
	–	1	20
156.25	×2	–	8
	–	1	16

Channel Frequency Divider

The device supports four independent output channels A–D. The channels A–C have one configurable integer frequency divider N*x* (*x* = A – C), that divides the VCO frequency to the desired output frequency with very low phase noise. The integer divider values can be selected from the range of ÷1 to ÷160 (Table 8). Channel D supports fractional divider ratios (Table 9).

Table 8. Integer Frequency Divider Settings

Channel Divider N*x*[a]	Output Clock Frequency (MHz) for VCO = 2500MHz
÷1	2500
÷2	1250
÷3	833.333
÷4	625
÷5	500
÷8	312.5
÷10	250
÷16	156.25
÷20	125
÷30	83.333
÷32	78.125
÷40	62.5
÷50	50
÷60	41.667
÷64	39.0625
÷80	31.25
÷100	25
÷120	20.833
÷128	19.53125
÷160	15.625

[a] *x* = A – D.

Table 9. Typical Fractional Frequency Divider Settings

Channel Divider N*D* [a]	Output Clock Frequency (MHz) for VCO = 2500MHz
15.51	161.1328125
18.75	133.333

[a] Greatest N*D* fractional divider is $2 \times (14 + [2^{24} - 1] / 2^{24}) \approx 29.99999988$.

Table 10. PLL Feedback Path Settings

SRC	Operation
0	The output divider input signal is the FemtoClock NG PLL.
1	The output divider input signal is the VCXO-PLL output signal. FemtoClock NG PLL is bypassed.

Redundant Inputs

The two inputs are compatible with LVDS and LVPECL signal formats, and also support single-ended LVCMOS signals. For applicable input interface circuits, see Applications Information.

Definitions

- Primary clock – The CLK_n input selected by the selection logic.
- Secondary clock – The CLK_n input not selected by the selection logic.
- PLL reference clock – The CLK_n input selected as the PLL reference signal by the selection logic. In automatic switching mode, the selection can be overwritten by a state machine.

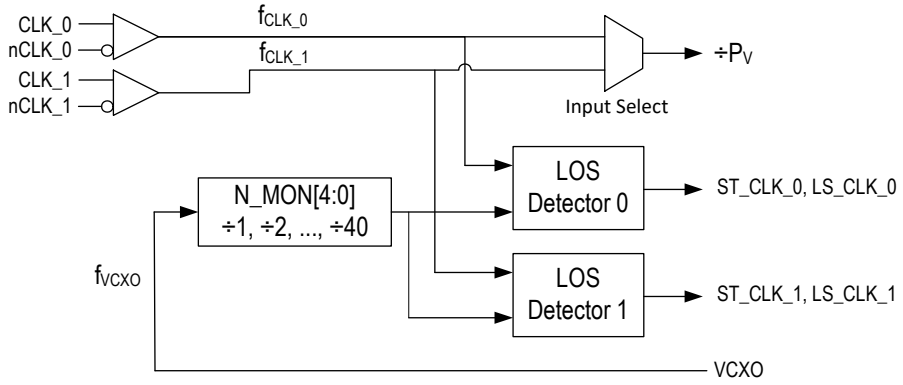
Monitoring

Loss of Input Signal (LOS)

In operation, a clock input is declared invalid (LOS) with the corresponding ST_CLK_*n* and LS_CLK_*n* indicator bits set after a specified number of consecutive clock edges. If differential input signals are applied, the input will also detect an LOS condition in case of a zero differential input voltage.

The device supports LOS detect circuits, one for each input. The signal detect circuits compare the signals at the CLK_0 and CLK_1 inputs to the internal frequency-divided signals from the VCXO-PLL (Figure 2). The loss-of-signal fault condition is declared upon three or more missing clock input edges. LOS requires configuration of the N_MON[4:0] frequency divider setting to individually match the input frequencies CLK_*n* to the VCXO frequency: $f_{VCXO} \div N\_MON[4:0] = f_{CLK\_n}$. For instance, if one of the input frequencies is 25MHz and a 125MHz VCXO is used, set N_MON[4:0] = ÷5. For configuration details see Table 11. Then, LOS is declared after three consecutive missing clock edges. LOS is signaled through the ST_CLK_*n* (momentary) and LS_CLK_*n* (sticky, resettable) status bits. and can be reported as an interrupt signal on the nINT output. The LOS circuit requires the jitter attenuation mode of the device (BYPV = 0). LOS does not detect frequency errors.

Figure 2. LOS Detect Circuit



Input Re-Validation

A clock input is declared valid and the corresponding LOS bit is reset after the clock input signal returned for user-configurable number of consecutive input periods. This re-validation of the selected input clock is controlled by the CNTV setting (verification pulse counter).

Clock Selection

The device supports five input selection modes: manual with and without holdover, short-term holdover, and two automatic switch modes.

Table 11. Clock Selection Settings

Mode			Name	Description	Flags				Application
nHO_EN	nMA1	nMA0			ST_CLKn	nST_HOLD	ST_SEL	ST_REF	
0	X	X	Manual Holdover Control (default)	Input selection follows user-configuration of the EXT_SEL pin or INT_SEL register bit as set by nEXT_INT with holdover. Input selection is *never* changed by the internal state machine.					
				LOS on the primary reference clock: Active reference stays selected, and the PLLs may stall. The device will not go into holdover.	LOS status	1	Selected input	0[a]	Startup and external selection control with holdover
				Manual change of the reference clock: The device will *go into holdover*, and the hold-off down-counter (CNTH) starts. The device initiates a clock switch *after* expiration of the hold-off counter. Duration of holdover is set by CNTH × CNTR / f_{VCXO}. Holdover is terminated even if the secondary clock input is bad (LOS), (Manual Holdover Control (nHO_EN = 0).		0[b]	Selected input[c]	LOS status of *selected* input	
1	0	0	Manual Control	Input selection follows user-configuration of the EXT_SEL pin or INT_SEL register bit as set by nEXT_INT. Input selection is *never* changed by the internal state machine.					
				LOS on the primary reference clock: Active reference stays selected and the PLLs may stall. Device will not go into holdover.	LOS status	1	Selected input	0	External selection control
				Manual change of the reference clock: The device will not go into holdover and will attempt to lock to the newly selected reference.		1	Selected input	Actual LOS status of selected input	
1	0	1	Automatic	Input selection follows LOS status. A failing input clock will cause an LOS event for that clock input. If the selected clock has an LOS event, the device will immediately initiate a clock fail-over switch.					
				LOS on the primary reference clock: The device will switch to the secondary clock without holdover. Input selection is determined by a state machine and may differ from the user's clock selection. No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch, and will not enter the holdover state. The PLL is not locked. Re-validation of all input clocks will result in the PLL to attempt to lock on that input clock (Revertive Switching).	LOS status	1	Selected input determined by state machine	Actual LOS status of selected input determined by state machine	Multiple inputs with qualified clock signals
				Manual change of the reference clock: The device will switch to the newly selected clock without holdover. If the newly selected clock is not valid, the PLL may stall.		1	Selected input	Actual LOS status of selected input	

Table 11. Clock Selection Settings (Cont.)

Mode			Name	Description	Flags				Application
nHO_EN	nMA1	nMA0			ST_CLKn	nST_HOLD	ST_SEL	ST_REF	
1	1	0	Short-term Holdover	Input selection follows user-configuration of EXT_SEL pin or INT_SEL register bit as set by nEXT_INT. Selection is never changed by the internal state machine (see Holdover).					
				LOS on the primary reference clock: A failing reference clock will cause an LOS event. If the selected reference fails, the device will enter holdover *immediately*. Re-validation of the selected input clock is controlled by the CNTV setting. A successful re-validation will result in the PLL to re-lock on that input clock.	LOS status	0 For holdover duration	Selected input	LOS status for duration of LOS until revalidation	Use if a single reference is occasionally interrupted
1	1	1	Automatic with Holdover	Input selection follows LOS status. A failing input clock will cause an LOS event for that clock input. If the *selected* clock has an LOS event, the device will go into holdover and switches input clocks after the hold-off counter expires.					
				LOS on the primary reference clock, or Manual change of the reference clock: The device will go into holdover and the hold-off down-counter (CNTH) starts. The device initiates a clock fail-over switch to a valid secondary clock input *after* expiration of the hold-off counter. Duration of holdover is set by CNTH × CNTR/ f_{VCXO}. The holdover is terminated prior hold-off count-down if the primary clock revalidates or is terminated by a manual change of the reference clock. See Automatic with Holdover (nHO_EN = 1, nM/A[1:0] = 11), and Revertive Switching. No valid clock scenario: The device remains in holdover if the secondary input clock is invalid.	LOS status	0 For holdover duration	Selected input determined by state machine	Actual LOS status of selected input	Multiple inputs

[a] For the duration of an invalid input signal (LOS).

[b] For the duration of holdover.

[c] Delayed by holdover period.

Holdover

In holdover state, the output frequency and phase is derived from an internal, digital value based on previous frequency and phase information. Holdover characteristics are defined in Table 48.

Manual Holdover Control (nHO_EN = 0)

This is the default switching mode of the device. The switch control is manual: The EXT_SEL pin or the INT_SEL bit as set by nEXT_INT determines the selected reference clock input. If the selection is changed by the user, the device will enter holdover until the CNTH[7:0] counter expires. Then, the new reference is selected (input switch). Application for this mode is startup and external selection control.

- ST_REF – Status of selected reference clock
- ST_CLK_n – Both will reflect the status of the corresponding input
- ST_SEL – The new selection
- nST_HOLD = 0 for the duration of holdover

Automatic with Holdover (nHO_EN = 1, nM/A[1:0] = 11)

If an LOS event is detected on the active reference clock:

1. Holdover begins immediately
2. Corresponding ST_REF and LS_REF go low immediately
3. Hold-off countdown begins immediately

During this time, both input clocks continue to be monitored and their respective ST_CLK, LS_CLK flags are active. LOS events will be indicated on ST_CLK, LS_CLK when they occur.

If the active reference clock resumes and is validated during the hold-off countdown:

1. Its ST_CLK status flag will return high and the LS_CLK is available to be cleared by an I^2C write of 1 to that register bit
2. No transitions will occur of the active REF clock; ST_SEL does not change
3. Revertive bit has no effect during this time (whether 0 or 1)

When the hold-off countdown reaches zero:

If the active reference has resumed and has been validated during the countdown, it will maintain being the active reference clock:

1. ST_SEL does not change
2. ST_REF returns to 1
3. LS_REF can be cleared by an I^2C write of 1 to that register
4. Holdover turns off and the VCXO-PLL attempts to lock to the active reference clock

If the active reference has not resumed, but the other clock input CLK_*n* is validated, then:

1. ST_SEL1:0 changes to the new active reference
2. ST_REF returns to 1
3. LS_REF can be cleared by an I^2C write of 1 to that register
4. Holdover turns off

If there is no validated CLK:

1. ST_SEL does not change
2. ST_REF remains low
3. LS_REF cannot be cleared by an I^2C write of 1 to that register
4. Holdover remains active

Revertive capability returns if REVS = 1.

Hold-off Counter

A configurable down-counter applicable to the *Automatic with Holdover* and *Manual with Holdover* selection modes. The purpose of this counter is a deferred, user-configurable input switch. The counter expires when a zero-transition occurs; this triggers a new reference clock selection. The counter is clocked by the frequency-divided VCXO-PLL signal. The CNTR setting determines the hold-off counter frequency divider and the CNTH setting the start value of the hold-off counter. For instance, set CNTR to a value of ÷131072 to achieve 953.67Hz (or a period of 1.048ms at f_{VCXO} = 125MHz): the 8-bit CNTH counter is clocked by 953.67Hz and the user-configurable hold-off period range is:
0ms (CNTR = 0x00) to 267ms (CNTR = 0xFF). After the counter expires, it reloads automatically from the CNTH I^2C register. After the LOS status bit (LS_CLK_*n*) for the corresponding input CLK_*n* has been cleared by the user, the input is enabled for generating a new LOS event.

The CNTR counter is only clocked if the device is configured in the clock selection modes, *Automatic with Holdover* and the selected reference clock experiences an *LOS* event, or in the *Manual with Holdover* mode with manual switching. Otherwise, the counter is automatically disabled (not clocked).

Revertive Switching

Revertive switching is only applicable to the two automatic switch modes shown in Table 11. Revertive switching enabled: Re-validation of any non-selected input clock(s) will cause a new input selection according to the user-preset input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the currently selected reference clock. Revertive switching disabled: Re-validation of a non-selected input clock has no impact on the clock selection. The default setting is revertive switching disabled.

VCXO-PLL Lock Detect (LOLV)

The VCXO-PLL lock detect circuit uses the signal phase difference at the phase detector as Loss-of-lock criteria. Loss-of-lock is reported if the actual phase difference is larger than a configurable phase detector window set by the LOCK_TH[14:0] configuration bits. A Loss-of-lock state is reported through the nST_LOLV and nLS_LOLV status bits (Table 21). The VCXO-PLL lock detect function requires to set FVCV = 0.

Table 12. ADR3 Selection Table

ADR3	Device Mode
Low	Default modes: Outputs – disabled Inputs – unused
Middle	Default frequency profile with 25MHz input
High	Default frequency profile with 20MHz input

Table 13. Input Path Pin Configuration Table

Inputs	SEL_BITS_MASTER (REG20, D0)	X	0	0	1
	ADR3	L	M	H	X
	REFin	X	REF = 25MHZ	REF = 20MHZ	X
Resulting Path Configuration	PV Divide	REG16[7:0], 17[6:0]	160	160	REG16[7:0], 17[6:0]
	REF into PD	REF/ PV	156.25kHz	125kHz	REF/ PV
	MV Divide	REG18[7:0], 19[6:0]	1000	1250	REG18[7:0], 19[6:0]
	FB into PD	FB/ MV	156.25kHz	125kHz	FB/ MV
	lock_th	REG21[7:0], 22[6:0]	128	128	REG21[7:0], 22[6:0]
	PF	REG25[5:0]	X	X	REG25[5:0]
	PF Doubler	REG25[7]	on	on	REG25[7]
	REF into PD	0	312.5MHz	312.5MHz	0
	MF	REG26[7:0], 27[0]	8	8	REG26[7:0], 27[0]
	FB into PD	0	312.5MHz	312.5MHz	0
	BYPV	REG23[0]	off	off	REG23[0]
	SRC	REG24[0]	on	on	REG24[0]
	Polarity	REG28[7]	positive	positive	REG28[7]
	FVCV	REG28[6]	off	off	REG28[6]
	CPV	REG28[4:0]	750µA	750µA	REG28[4:0]
	CPF	REG30[4:0]	5.8mA	5.8mA	REG30[4:0]
	N_MON	REG32[7:3]	8	8	REG32[7:3]
	LOS Monitoring Frequency	0	19.5MHz	19.5MHz	0
	MODE_BLOCK	REG32[2]	on	on	REG32[2]
	nHO_EN	REG32[1]	off	off	REG32[1]
	nEXT_INT	REG32[0]	external	external	REG32[0]
	nMA[1:0]	REG33[3:2]	manual	manual	REG33[3:2]
	CNTV	REG35[1:0]	2	2	REG35[1:0]

Table 14. Output Frequency Pin Configuration Table

Output Bank A and C	ADR0	Output Type	Divide Ratio	FOUT (MHz)	Swing Level
Total outputs per bank: 4, with 1 integer divider	Low	LVPECL	20	125	750mV
	Middle	LVDS	16	156.25	500mV
	High	LVPECL	16	156.25	750mV
Output Bank B	ADR1	Output Type	Divide Ratio	FOUT (MHz)	Swing Level
Total of 4 outputs with 1 integer divider	Low	LVPECL	20	125	750mV
	Middle	LVDS	16	156.25	500mV
	High	LVPECL	16	156.25	750mV
Output Bank D	ADR2	Output Type	Divide Ratio	FOUT (MHz)	Swing Level
Total of 6 outputs with 1 fractional divider	Low	LVPECL	20	125	750mV
	Middle	LVDS	16	156.25	500mV
	High	LVPECL	16	156.25	750mV

Table 15. I^2C Address Selection Table

I2C_A	Output Type	I2C_A[1]	I2C_A[0]
Low	Address 1	0	0
Middle	Address 2	0	1
High	Address 3	1	1

The 8V19N478 can be configured via pin or I2C. ADR3/2/1/0 provides a specific set of configuration options for input and output paths. In addition, the initialization sequence of the device is controlled by the ADR3 pin and the synchronization of the outputs by transition from Low to Middle or High.

Table 16. Initialization Sequence Control

Initialization	In Pin Mode, Triggered by:
init_clk	(Pin I2C_A3 = M or H) + IBM die powered up
pb_cal	(Pin I2C_A3 = M or H) + IBM die powered up
relock	Completion of init_clk sequence (above)
OE	Completion of init_clk sequence (above)

The pin configuration is overridden by I2C programming of the register map. The I2C_A pin set the Address as shown in following table.

Table 17. I2C Address

		1	I2C_A1	I2C_A0	R	W	I2C_A	
D8, D9	1101	1	0	0	1	0	L	Address 1
DA, DB	1101	1	0	1	1	0	M	Address 2
DE, DF	1101	1	1	1	1	0	H	Address 3

The default values of the register map are Read back by the I^2C in the Pin-Strap configuration mode.

FemtoClock NG Loss-of-lock (LOLF)

FemtoClock NG-PLL loss-of-lock is signaled through the nST_LOLF (momentary), and nLS_LOLF (sticky, resettable) status bits, and can reported as hardware signal on the LOCK_V output as well as an interrupt signal on the nINT output.

Differential Outputs

Table 18. Output Features

Output	Style	Amplitude[a]	Disable	Power Down	Termination
QCLK_*y*	LVPECL	350 – 850mV 4 steps	Yes	Yes	50Ω to V_{TT}[b]
	LVDS				100Ω differential
					—
QCLK_V	LVPECL	350 – 850mV 4 steps	Yes	Yes	50Ω to V_{TT}
	LVDS				100Ω differential
	LVCMOS[c]	1.8V	Yes	Yes	—

[a] Amplitudes are measured single-ended.

[b] For V_{TT} (Termination voltage) values (see Table 50).

[c] LVCMOS style: nQCLK_V and QCLK_V are complementary.

Table 19. Individual Clock Output Settings

PD[a]	Output Power	STYLE	Termination	Enable	State	A[1:0]	Amplitude (mV)[b]
1	Off	X	100Ω differential or no termination	X	Off	X	X
0	On	0	100Ω differential (LVDS)	0	Disable[c]	XX	X
				1	Enable	00	350
						01	500
						10	700
						11	850
		1	50Ω to V_{TT}[d] (LVPECL)	0	Disable	XX	X
				1	Enable	00	350
						01	500
						10	700
						11	850

[a] Power-down modes are available for the individual channels A – D and the outputs QCLK_y (A0 – D3).

[b] Output amplitudes of 700mV and 850mV require a 3.3V output supply (V_{DDO_V}). 350mV and 500mV output amplitudes support V_{DDO_V} = 2.5V and 1.8V.

[c] Differential output is disabled in static low/high state.

[d] For V_{TT} (Termination voltage) values, see Table 50.

Output Phase-Delay

Output phase delay is supported in each channel. The selected VCO frequency sets the delay unit to $1/f_{VCO}$.

Table 20. Delay Circuit Settings

Delay Circuit	Unit	Steps	Range
Clock Phase Φ_{CLK_x}	$\frac{1}{f_{VCO}}$ f_{VCO} = 2500MHz: 400ps	256	0–102ns

Status Conditions and Interrupts

The 8V19N478 has an interrupt output to signal changes in status conditions. Settings for status conditions may be accessed in the *Status registers*. The device has several conditions that can indicate faults and status changes in the operation of the device. These are shown in Table 21 and can be monitored directly in the status registers. Status bits (named: ST_*condition*) are read-only and reflect the momentary device status at the time of read-access. Several status bits are also copied into latched bit positions (named: LS_*condition*). The latched version is controlled by the corresponding fault and status conditions and remains set ("sticky") until reset by the user by writing "1" to the status register bit. The reset of the status condition has only an effect if the corresponding fault condition is removed, otherwise, the status bit will set again. Setting a status bit on several latched registers can be programmed to generate an interrupt signal (nINT) via settings in the Interrupt Enable bits (named: IE_*condition*). A setting of "0" in any of these bits will mask the corresponding latched status bits from affecting the interrupt status pin. Setting all IE bits to 0 has the effect of disabling interrupts from the device.

Table 21. Status Bit Functions

Status Bit		Function			
			Status if Bit is:		
Momentary	Latched	Description	1	0	Interrupt Enable Bit
ST_CLK_0	LS_CLK_0	CLK 0 input status	Active	LOS	IE_CLK_0
ST_CLK_1	LS_CLK_1	CLK 1 input status	Active	LOS	IE_CLK_1
nST_LOLV	nLS_LOLV	VCXO-PLL loss of lock	Locked	Loss-of-lock	IE_LOLV
nST_LOLF	nLS_LOLF	FemtoClock NG-PLL loss of lock	Locked	Loss-of-lock	IE_LOLF
nST_HOLD	nLS_HOLD	Holdover	Not in holdover	Device in holdover	IE_HOLD
ST_VCOF	—	FemtoClock NG VCO calibration	Not completed	Completed	—
ST_SEL	—	Clock input selection	0 = CLK_0 1 = CLK_1		—
ST_REF	LS_REF	PLL reference status	Valid reference[a]	Reference lost	IE_REF

[a] Manual and short-term holdover mode: 0 indicates if the selected reference is lost, 1 if not lost.

Automatic mode: will transition to 0 while the input clock is lost and during input selection by priority. Will transition to 1 once a new reference is selected.

Automatic with holdover mode: 0 indicates the reference is lost and still in holdover.

Interrupts are cleared by resetting the appropriate bit(s) in the latched register after the underlying fault condition has been resolved. When all valid interrupt sources have been cleared in this manner, this will release the nINT output until the next unmasked fault.

Table 22. LOCK Function

Status Bit (PLL)		
nLS_LOLV (VCXO-PLL)	nLS_LOLF (FemtoClock NG)	Status Reported on LOCK[a] Output[b]
Locked	Locked	1
Locked	Not locked	0
Not locked	Locked	0
Not locked	Not locked	0

[a] Hardware interrupts on nINT required to set the IE_LOLV, IE_LOLF bits to "enable interrupt".

[b] SELSV1 controls the logic level 1.8V/3.3V of LOCK and nINT outputs.

Serial Control Port

Serial Control Port Configuration Description

The 8V19N478 has a serial control port that can respond as a slave in an I^2C compatible configuration at a base address of 11011[I2C_A1, I2C_A0]b, to allow access to any of the internal registers for device programming or examination of internal status. The I2C_A[1:0] bits of the I^2C interface address are set by the logic state of the three-level pin, I2C_A (see Table 17). If more than one 8V19N478 is connected to the same I^2C bus, set I2C_A to a different state on each device to avoid address conflicts.

All registers are configured to have default values. For details, see the specifics for each register. Default values for registers are set after reset by the configuration pins.

I^2C Mode Operation

The I^2C interface fully supports v1.2 of the I^2C Specification for Normal and Fast mode operation. The interface acts as a slave device on the I^2C bus at 100kHz or 400kHz using a fixed base address of 11011[I2C_A1, I2C_A0]b.

The I^2C interface accepts byte-oriented block write and block read operations (see Figure 3 and Figure 4). One address byte specifies the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data is moved into the registers byte by byte and before a STOP bit is received.

For full electrical I^2C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

Figure 3. I^2C Write Data (Master Transmit, Slave Receive) From Any Register Address

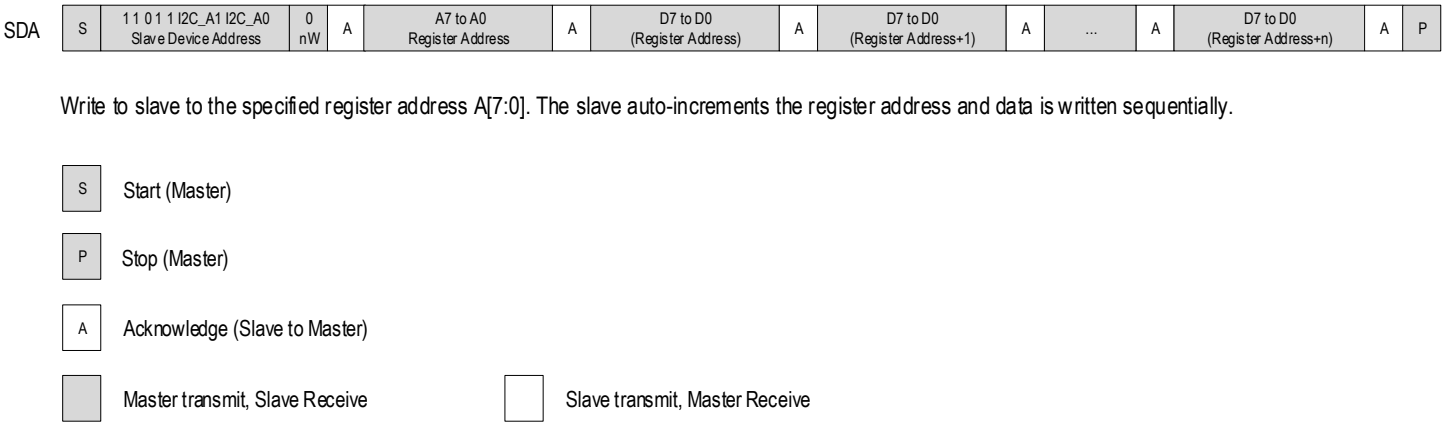
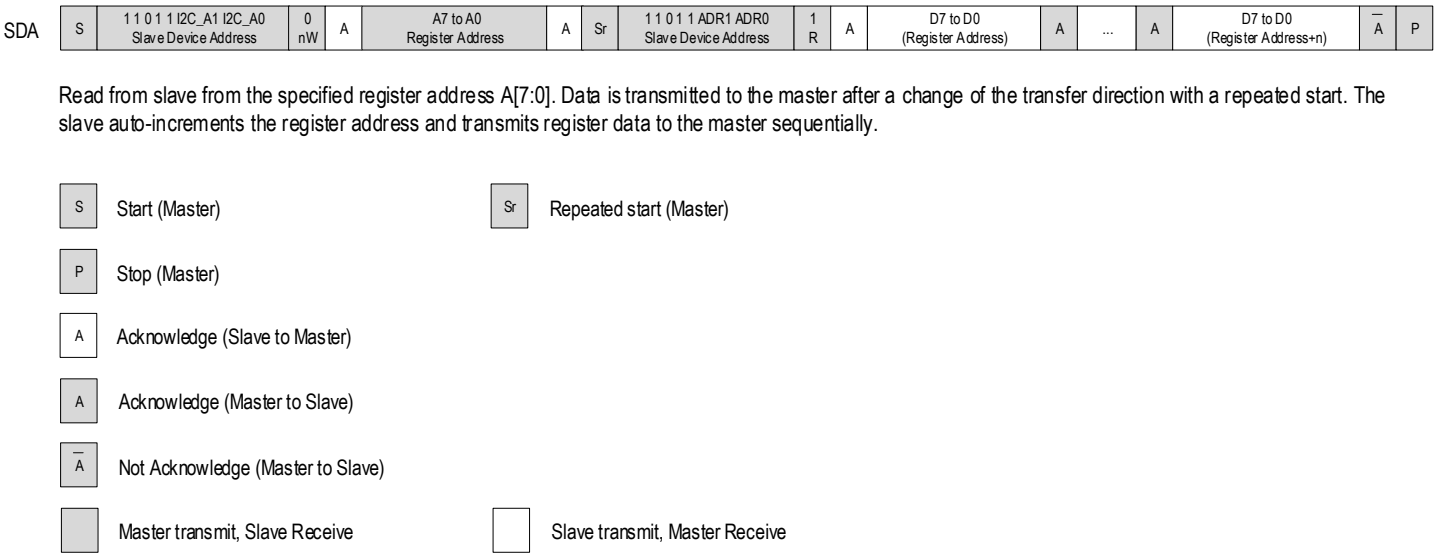


Figure 4. I²C Read Data (Slave Transmit, Master Receive) From Any Register Address



Register Descriptions

This section contains all addressable registers, sorted by function, followed by a detailed description of each bit field for each register. Several functional blocks with multiple instances in this device have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once, with an additional table to indicate their addresses and default values. All writable register fields will come up with a default values as indicated in the *Factory Defaults* column unless altered by values loaded from non-volatile storage during the initialization sequence.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are Reserved. Reserved bit fields may be used for an internal debug test and debug functions.

Table 23. Configuration Registers

Register Address	Register Description
0x00	SRESET
0x01	I²C Address (I²C only)
0x02–0x0F	Reserved
0x10–0x11	PLL Frequency Divider: PV
0x12–0x13	PLL Frequency Divider: MV
0x14	SEL_BITS_MASTER
0x15–0x16	LOCK_TH
0x17	PLL Control: BYPV
0x18	PLL Control: SRC
0x19	PLL Frequency Divider: PF, FDF
0x1A	PLL Frequency Divider: MF[7:0]
0x1B	PLL Frequency Divider: MF[8]
0x1C–0x1E	PLL Control

Table 23. Configuration Registers (Cont.)

Register Address	Register Description
0x1F	I/O Voltage Select
0x20–0x23	Input Selection
0x24–0x26	Channel A
0x27	Reserved
0x28–0x2B	Output States QCLK_A0 – QCLK_A3
0x2C–0x2E	Channel B
0x2F	Reserved
0x30–0x33	Output States QCLK_B0 – QCLK_B3
0x34–0x36	Channel C
0x37	Reserved
0x38–0x3B	Output States QCLK_C0 – QCLK_C3
0x3C–0x42	Channel D
0x43	Reserved
0x44–0x49	Output States QCLK_D0 – QCLK_D5
0x4A	Reserved
0x4B	QCLKV
0x4C	Interrupt Enable
0x4D	Reserved
0x4E–0x4F	Reserved
0x50	Status (Latched)
0x51	Status (Momentary)
0x52	Reserved
0x53	Reserved
0x54	Reserved
0x55–0x57	General Control
0x58	Channel Enable A–D, QCLKV
0x59–0x5B	Reserved
0x5C–0x5E	Reserved
0x5F–0x60	Reserved
0x61–0x62	Reserved
0x63	Reserved

Device Configuration Registers

Table 24. Device Configuration Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SRESET
0x01	Reserved	I2C_A[6:0]						
0x1F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SELSV

Table 25. Device Configuration Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
SRESET	R/W Auto-Clear	0 Value: not reset	Soft Reset: 0 = Normal operation. 1 = Register reset. The device loads the default values into the register 0x02-0xFF. The content of the register addresses 0x00, 0x01 and the serial interface engine are not reset.
I2C_A[6:0]	R	11011 [I2C_A1[1]] [I2C_A0[0]]	I^2C Device Address (I^2C only): This read-only register stores the binary I^2C device address: 11011[I2C_A[1]][I2C_A[0]]. Bits D1 and D0 are determined by the I2C_A pin. For I2C_A[1:0] values based on I2C_A level, see Table 15.
SELSV	Select LOCK/nINT voltage level R/W	1 Value: 3.3V	Selects the voltage level of the LOCK and nINT outputs: SELSV: 0 = LOCK, nINT interface pins are 1.8V 1 = LOCK, nINT interface pins are 3.3V (default)

PLL Frequency Divider Registers

Table 26. PLL Frequency Divider Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x10	PV[7:0]							
0x11	Reserved	PV[14:8]						
0x12	MV[7:0]							
0x13	Reserved	MV[14:8]						
0x14	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SEL_BITS_ MASTER
0x15	LOCK_TH[7:0]							
0x16	Reserved	LOCK_TH[14:8]						
0x19	FDF	Reserved	PF[5:0]					
0x1A	MF[7:0]							
0x1B	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MF8

Table 27. PLL Frequency Divider Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
PV[14:0]	R/W	000 0100 0000 0000 Value: ÷1024	VCXO-PLL Input Frequency Pre-Divider: The value of the frequency divider (binary coding). Range: ÷1 to ÷32767
MV[14:0]	R/W	000 0100 0000 0000 Value: ÷1024	VCXO-PLL Feedback-Divider: The value of the frequency divider (binary coding). Range: ÷1 to ÷32767
SEL_BITS_MASTER	R/W	0	Input Path Configuration Control: 0 = Input path settings determined by ADR3 control pin. 1 = Input path settings determined by register settings over I^2C. For input path configurations see Table 13.

Table 27. PLL Frequency Divider Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
LOCK_TH[14:0]	R/W	000 0000 1000 0000 Value: 128	PLL Lock Detect Phase Window Threshold: The device reports VCXO-PLL lock when the phase difference between the internal signals f_{REF} and f_{VCXO_REF} are lower than or equal to the phase difference set by LOCK_TH[14:0] for more than 1000 f_{VCXO_DIV} clock cycles. Requires $M_V \geq 4$. Set LOCK_TH[14:0] < M_V. ($f_{REF} = f_{CLK} \div P_V$ is the internal output of the PV divider, $f_{VCXO\_DIV} = f_{VCXO} \div M_V$ is the internal output of the MV divider.)
PF[5:0]	R/W	00 0001 Value: ÷1	FemtoClock NG Pre-Divider: The value of the frequency divider (binary coding) Range: ÷1 to ÷63 00 0000: PF is bypassed
FDF	R/W	0 Value: $f_{VCXO} \div PF$	Frequency Doubler: The input frequency of the FemtoClock NG PLL (2nd stage) is: 0 = The output signal of the BYPV multiplexer, divided by the PF divider. 1 = The output signal of the BYPV multiplexer, doubled in frequency. Use this setting to improve phase noise. The PF divider has no effect if FDF = 1.
MF[8:0]	R/W	0 0001 1000 Value: ÷24	FemtoClock NG Feedback-Divider: The value of the frequency divider (binary coding). Range: ÷8 to ÷511

PLL Control Registers

Table 28. PLL Control Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPV
0x18	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SRC
0x1C	POLV	FVCV	Reserved	CPV[4:0]				
0x1D	Reserved	Reserved	OSVEN	OFFSET[4:0]				
0x1E	Reserved	Reserved	Reserved	CPF[4:0]				

Table 29. PLL Control Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
BYPV	R/W	0 VCXO-PLL enabled	VCXO-PLL Bypass: 0 = VCXO-PLL is enabled. 1 = VCXO-PLL is disabled and bypassed.
SRC	R/W	0 PLL enabled	FemtoClock NG PLL Bypass: 0 = FemtoClock NG PLL is enabled. 1 = FemtoClock NG PLL is disabled and bypassed. The VCXO-PLL output signal is frequency divided by the channel dividers.
POLV	R/W	0 Value: Positive Polarity	VCXO Polarity: 0 = Positive polarity. Use for an external VCXO with a positive f(V_C) characteristics 1 = Negative polarity. Use for an external VCXO with a negative f(V_C) characteristics
FVCV	R/W	1 Value: Value: LFV = V_{DD_V}/2	VCXO-PLL Force VC Control Voltage: 0 = Normal operation. 1 = Forces the voltage at the LFV control pin (VCXO input) to V_{DD_V}/2. VCXO-PLL unlocks and the VCXO is forced to its mid-point frequency. FVCV = 1 is the default setting at startup to center the VCXO frequency. FVCV should be cleared after startup to enable the PLL to lock to the reference frequency.
CPV[4:0]	R/W	0 1111 Value: 0.8mA	VCXO-PLL Charge-Pump Current: Controls the charge-pump current I_{CPV} of the VCXO-PLL. Charge pump current is the binary value of this register plus one multiplied by 50µA. I_{CPV} = 50µA × (CPV[4:0] + 1) CPV[4:0] = 00000 sets ICPV to the min. current of 50µA. Maximum charge-pump current is 1.6 mA. Default setting is 0.8mA: ((15 + 1) × 50µA).

Table 29. PLL Control Register Descriptions (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
OSVEN	R/W	0	VCXO-PLL Offset Enable: 0 = No offset. 1 = Offset enabled. A static phase offset of OFFSET[4:0] is applied to the PFD of the VCXO-PLL.
OFFSET[4:0]	R/W	0 0000 Value: 0°	VCXO-PLL Static Phase Offset: Controls the static phase detector offset of the VCXO-PLL. Phase offset is the binary value of this register multiplied by 0.9° of the PFD input signal, (OFFSET [4:0] × f_{PFD} ÷ 400). The maximum offset is 31 × 0.9° = 27.9°. Setting OFFSET to 0.0° eliminates the thermal noise of an offset current. If the VCXO-PLL input jitter period T_{JIT} exceeds the average input period: set OFFSET to a value larger than $f_{PFD} \times T_{JIT} \times 400$ to achieve a better charge-pump linearity and lower in-band noise of the PLL.
CPF[4:0]	R/W	1 1000 Value: 1.4mA	FemtoClock NG PLL Charge-Pump Current: Controls the charge-pump current I_{CPF} of the FemtoClock NG PLL. The charge-pump current is the binary value of this register plus one multiplied by 200µA. I_{CPF} = 200µA × (CPF[4:0] + 1) CPV[4:0] = 00000 sets I_{CPF} to the minimum current of 200µA. Maximum charge-pump current is 6.4 mA. Default setting is 1.4 mA: ((6 + 1) × 200µA).

Input Selection Mode Registers

Table 30. Input Selection Mode Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x20	VCXO_DIV[4:0]					MODE_BLOCK	nHO_EN	nEXT_INT
0x21	Reserved	Reserved	Reserved	REVS	nM/A[1:0]		Reserved	INT_SEL
0x22	CNTH[7:0]							
0x23	CNTR[1:0]		Reserved	Reserved	Reserved	CNTV[1]	CNTV[0]	

Table 31. Input Selection Mode Registers

Register Description							
Bit Field Name	Field Type	Default (Binary)	Description				
VCXO_DIV[4:0]	R/W	00000 Value: ÷1	Clock Frequency Divider for the input activity monitor: The clock activity monitor compares the device input frequency (f_{IN}) to the frequency of the VCXO divided by VCXO_DIV. For optimal operation of the activity monitor, the frequency f_{VCXO} ÷ VCXO_DIV should match the input frequency. E.g. for f_{IN} = 61.44MHz and f_{VCXO} = 61.44MHz, set VCXO_DIV = ÷1. For f_{IN} = 25MHz and f_{VCXO} = 125MHz, set FCXO_DIV = ÷5. VCXO_DIV[4:0]				
			0XX 00 = ÷1 0XX 01 = ÷2 0XX 10 = ÷4 0XX 11 = ÷8	100 00 = ÷2 100 01 = ÷4 100 10 = ÷8 100 11 = ÷16	101 00 = ÷3 101 01 = ÷6 101 10 = ÷12 101 11 = ÷24	110 00 = ÷4 110 01 = ÷8 110 10 = ÷16 110 11 = ÷32	111 00 = ÷5 111 01 = ÷10 111 10 = ÷20 111 11 = ÷40
MODE_BLOCK	R/W	0 Value: Not blocked	Inactive Input Clock Block: 0 = Both input clock signals CLK0 and CLK1 are routed to the input clock multiplexer. 1 = The input clock that is currently not active is gated off (blocked).				
nHO_EN	R/W	1 Value: Enter Holdover Disabled	Manual Holdover Control: 0 = Enter holdover on a manual input reference switch. Using the EXT_SEL control pin or the INT_SEL control bit, as defined by nEXT_INT for manual reference switching. nMA[1:0] has no meaning. 1 = The device switching and holdover modes are controlled by nMA[1:0].				

Table 31. Input Selection Mode Registers (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
nEXT_INT	R/W	0 Value: External selection	Input Clock Selection: 0 = The EXT_SEL pin (B3) controls the input clock selection. 1 = The INT_SEL bit (register 0x21, D0) controls the input clock selection.
REVS	R/W	0 Value: Off	Revertive Switching: The revertive input switching setting is only applicable to the two automatic selection modes shown in Table 11. If nM/A[1:0] = X0, the REVS setting has no meaning. 0 = Disabled: Re-validation of the non-selected input clock has no impact on the clock selection. 1 = Enabled: Re-validation of the non-selected input clock will cause a new input selection according to the pre-set input priorities (revertive switch). Default setting is revertive switching turned off.
nM/A[1:0]	R/W	00 Value: Manual selection	Reference Input Selection Mode: In any of the manual selection modes (nM/A[1:0] = 00 or 10), the VCXO-PLL reference input is selected by INT_SEL. In any of the automatic selection modes, the VCXO-PLL reference input is selected by an internal state machine according to the input LOS states and the priorities in the input priority registers. 00 = Manual selection (no holdover) 01 = Automatic selection (no holdover) 10 = Short-term holdover 11 = Automatic selection with holdover
INT_SEL	R/W	0 Value: CLK0 selected	VCXO-PLL Input Reference Selection: Controls the selection of the VCXO-PLL reference input in internal (nEXT_INT = 1), and in manual selection mode (nHO_EN = 1, nM/A[1:0] = 00 or 10). In external (nEXT_INT = 0) and in automatic selection modes (nM/A[1:0] = X1), INT_SEL has no meaning. 0 = CLK_0 is the selected VCXO-PLL reference clock. 1 = CLK_1 is the selected VCXO-PLL reference clock.
CNTH[7:0]	R/W	1000 0000 Value: 134ms	Short-term Holdover: Hold-off counter period. The device initiates a clock fail-over switch upon counter expiration (zero transition). The counters start to counts backwards after an LOS event is detected. The hold-off counter period is determined by the binary number of VCXO-PLL output pulses divided by CNTR[1:0]. With a VCXO frequency of 125MHz and CNTR[1:0] = 10, the counter has a period of (1.048ms × binary setting). After each zero-transition, the counter automatically re-loads to the setting in this register. The default setting is 134ms (VCXO = 125MHz: 1/125MHz × 2^{17} × 128).

Table 31. Input Selection Mode Registers (Cont.)

<table>
<tr><th colspan="5">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="2">Description</th></tr>
<tr><td rowspan="5">CNTR[1:0]</td><td rowspan="5">R/W</td><td rowspan="5">10

Value: 2^{17}</td><td colspan="2">Short-term Holdover Reference Divider</td></tr>
<tr><td>CNTR[1:0]</td><td colspan="2">CNTH frequency (period; range)</td></tr>
<tr><td></td><td>125MHz VCXO</td><td>156.25MHz VCXO</td></tr>
<tr><td>00 = $f_{VCXO} \div 2^{15}$</td><td>3814Hz
(0.262ms; 0ms – 66.8ms)</td><td>4768Hz
(0.209ms; 0ms – 53.4ms)</td></tr>
<tr><td>01 = $f_{VCXO} \div 2^{16}$</td><td>1907Hz
(0.524ms; 0ms – 133ms)</td><td>2384Hz
(0.419ms; 0ms – 106.9ms)</td></tr>
<tr><td>CNTV[1:0]</td><td>R/W</td><td>10

Value: 32</td><td colspan="3">Revalidation Counter:
Controls the number of required consecutive, valid input reference pulses for clock re-validation on CLK_n for the number of input periods. At an LOS event, the re-validation counter loads this setting from the register and counts down by one with every valid, consecutive input signal period. Missing input edges (for one input period) will cause this counter to re-load its setting. An input is re-validated when the counter transitions to zero and the corresponding LOS flag is reset.
00 = 2 (shortest possible)
01 = 16
10 = 32
11 = 64</td></tr>
</table>

Channel Registers

The content of the channel registers set the channel state, the clock divider the clock phase delay and the power-down state.

Table 32. Channel Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x24: Channel A 0x2C: Channel B 0x34: Channel C 0x40: Channel D	N_*A*[7:0] N_*B*[7:0] N_*C*[7:0] N_*D*[7:0]							
0x25: Channel A 0x2D: Channel B 0x35: Channel C 0x41: Channel D	ΦCLK_*A*[7:0] ΦCLK_*B*[7:0] ΦCLK_*C*[7:0] ΦCLK_*D*[7:0]							
0x26: Channel A 0x2E: Channel B 0x36: Channel C	PD_*A* PD_*B* PD_*C*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SEL_ BITS_A SEL_ BITS_B SEL_BITS_C
0x42: Channel D	PD_*D*	Reserved	Reserved	Reserved	D_DIV_FRAC [1]	D_DIV_FRAC [0]	CH_D_OUT	SEL_BITS_D
0x3C: Channel D 0x3D: Channel D 0x3E: Channel D	N_*D*_FRAC[7:0] N_*D*_FRAC[15:8] N_*D*_FRAC[23:16]							
0x3F: Channel D	Reserved	Reserved	Reserved	Reserved	N_*D*_INT[3:0]			
0x58	Reserved	Reserved	Reserved	EN_QCLK_V	EN_QCLK_A	EN_QCLK_B	EN_QCLK_C	EN_QCLK_D

Table 33. Channel Register Descriptions[a]

Register Description				
Bit Field Name	Field Type	Default (Binary)	Description	
N_*x*[7:0]	R/W	0100 0110 Value: ÷16	Output Frequency Divider N: N_*x*[7:0] Divider Value	
			1000 0000 0000 0000 0000 0001 0000 0010 0000 0011 0000 0100 0000 0110	÷1 ÷2 ÷3 ÷4 ÷5 ÷6 ÷8
			0100 0011 0100 0100 0100 0110	÷10 ÷12 ÷16
			0100 1011 0100 1100	÷20 ÷24
			0101 0011 0100 1110 0101 0100	÷30 ÷32 ÷36
			0101 1011 0101 0110	÷40 ÷48
			0110 0011	÷50
			0110 0100 0101 1110	÷60 ÷64
			0101 1111	÷72
			0110 0110	÷80
			0110 1110	÷96
			0111 1011	÷100
			0111 1100 0111 0110	÷120 ÷128
			0111 1110	÷160
N_*D*_FRAC[23:0]	R/W	0110 0000 0000 0000 0000 0000 Value: 6,291,456	Fractional Output Divider, Fractional Part: Together with N_E_INT, forms the fractional output divider N*D* value. $N_E = 2 \times \left(N_{INT} + \frac{N_{FRAC}}{2^{24}}\right)$ The default value is N*D* = 2 × (9 + 0.4371839761732) = 18.8743679523. Greatest N*D* fractional divider is 2 × (14 + [2^{24} – 1] / 2^{24}) ≈ 29.99999988.	

Table 33. Channel Register Descriptions[a] (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
N_*D*_INT[3:0]	R/W	1001 Value: 9	Fractional Output Divider, Integer Part: See N_*D*_FRAC[23:0] Greatest N*D* fractional divider is $2 \times (14 + [2^{24} - 1] / 2^{24}) \approx 29.99999988$.
ΦCLK_*x*[7:0] f_{VCO} = 2500MHz	R/W	0000 0000	CLK_*x* Phase Delay: ΦCLK_*x*[7:0]
			f_{VCO} = 2500MHz: Delay in ps = ΦCLK_*x* × 400ps (256 steps) ΦCLK_*x*[7:0] Delay (f_{VCO} = 2500MHz)
			0000 0000 — 0ps 0000 0001 — 400ps … — … 1111 1111 — 102ns
PD_*x*	R/W	0 Value: Power-up	0 = Channel *x* is powered up 1 = Channel *x* is power down
EN_*x*	R/W	0 Value: Disabled	QCLK_*x* Channel Output Enable: 0 = All outputs of channel *x* are disabled at the logic low state. 1 = All outputs of channel *x* are enabled.
EN_QCLK_*V*	R/W	0 Value: Disabled	QCLK_*V* Output Enable: 0 = QCLK_*V* is disabled at the logic low state. 1 = QCLK_*V* is enabled.

Table 33. Channel Register Descriptions[a] (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
SEL_BITS_x	R/W	0	Bank *x* Configuration Control: 0 = Nx[5:0], PD_X, EN_X settings determined by ADR*n* control pin. 1 = Nx[5:0], PD_X, EN_X settings determined by register settings over I^2C. Where: *n* = 0 for Channels A and C *n* = 1 for Channel B *n* = 2 for Channel D
D_DIV_FRAC[1:0]	R/W	0	D_DIV_FRAC[1:0]: Post-divider ratio for Bank D fractional divider: 00 = ÷1 01 = ÷2 10 = ÷4 11 = Reserved
CH_D_OUT	R/W	0	CH_D_OUT: Controls which the divider is used to provide output frequency for Bank D: 0 = Integer divider D (ND configures this) 1 = Fractional mode (ND_FINT, ND_FRAC, and ND_DIVF configure this)

[a] *x* = A, B, C, D.

Output Registers

The content of the output registers set the power-down state, the output style and amplitude.

Table 34. Output Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x28: QCLK_A0 0x29: QCLK_A1 0x2A: QCLK_A2 0x2B: QCLK_A3	PD_*A0* PD_*A1* PD_*A2* PD_A3	Reserved	Reserved	Reserved	Reserved	STYLE_*A0* STYLE_*A1* STYLE_*A2* STYLE_A3	A_*A0*[1] A_*A1*[1] A_*A2*[1] A_*A3*[1]	A_*A0*[0] A_*A1*[0] A_*A2*[0] A_*A3*[0]
0x30: QCLK_B0 0x31: QCLK_B1 0x32: QCLK_B2 0x33: QCLK-B3	PD_*B0* PD_*B1* PD_*B2* PD_*B3*	Reserved	Reserved	Reserved	Reserved	STYLE_*B0* STYLE_*B1* STYLE_*B2* STYLE_A3	A_*B0*[1] A_*B1*[1] A_*B2*[1] A_*A3*[1]	A_*B0*[0] A_*B1*[0] A_*B2*[0] A_*A3*[0]
0x38: QCLK_A0 0x39: QCLK_A1 0x3A: QCLK_A2 0x3B: QCLK_A3	PD_*C0* PD_*C1* PD_*C2* PD_C3	Reserved	Reserved	Reserved	Reserved	STYLE_*C0* STYLE_*C1* STYLE_*C2* STYLE_C3	A_*C0*[1] A_*C1*[1] A_*C2*[1] A_*C3*[1]	A_*C0*[0] A_*C1*[0] A_*C2*[0] A_*C3*[0]
0x44: QCLK_D0 0x45: QCLK_D1 0x46: QCLK_D2 0x47: QCLK_D3 0x48: QCLK_D4 0x49: QCLK_D5	PD_*D0* PD_*D1* PD_*D2* PD_*D3* PD_*D4* PD_*D5*	Reserved	Reserved	Reserved	Reserved	STYLE_*D0* STYLE_*D1* STYLE_*D2* STYLE_D3 STYLE_D4 STYLE_D5	A_*D0*[1] A_*D1*[1] A_*D2*[1] A_*D3*[1] A_*D4*[1] A_*D5*[1]	A_*D0*[0] A_*D1*[0] A_*D2*[0] A_*D3*[0] A_*D4*[0] A_*D5*[0]
0x4B: QCLK_V	PD_*V*	Reserved	Reserved	Reserved	STYLE__*V*1	STYLE__*V*0	A_*V*[1]	A_*V*[0]

Table 35. Output Register Descriptions[a]

<table>
<tr><th colspan="4">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th>Description</th></tr>
<tr><td>PD_y</td><td>R/W</td><td>0

Value: Power-up</td><td>0 = Output QCLK_y is powered-up.
1 = Output QCLK_y is power-down.</td></tr>
<tr><td>PD_v</td><td>R/W</td><td>1

Value: Power-down</td><td>0 = Output QCLK_v is powered-up.
1 = Output QCLK_v is power-down.</td></tr>
<tr><td rowspan="3">A_y[1:0]</td><td rowspan="3">R/W</td><td rowspan="3">10

Value: 700mV</td><td colspan="2">QCLK_y, QCLK_V Output Amplitude</td></tr>
<tr><td>Setting for STYLE = 0 (LVDS)</td><td>Setting for STYLE = 1 (LVPECL)</td></tr>
<tr><td>A[1:0] = 00: 350mV
A[1:0] = 01: 500mV
A[1:0] = 10: 700mV
A[1:0] = 11: 850mV
Termination: 100Ω across</td><td>A[1:0] = 00: 350mV
A[1:0] = 01: 500mV
A[1:0] = 10: 700mV
A[1:0] = 11: 850mV
Termination: 50Ω to V_{TT}[b]</td></tr>
<tr><td>A_v[1:0]</td><td>R/W</td><td>10

Value: 700mV</td><td colspan="2">Same as A_y[1:0]</td></tr>
<tr><td>STYLE_y</td><td>R/W</td><td>1

Value: LVPECL</td><td colspan="2">QCLK_y Output Format:
0 = Output is LVDS (Requires LVDS 100Ω output termination)
1 = Output is LVPECL (Requires LVPECL 50Ω output termination of to the specified recommended termination voltage).</td></tr>
<tr><td>STYLE_v[1:0]</td><td>R/W</td><td>01

Value: LVPECL</td><td colspan="2">QCLK_v Output Format:
00 = Output is LVDS (Requires LVDS 100Ω output termination).
01 = Output is LVPECL (Requires LVPECL 50Ω termination to V_{TT}[b]).
1x = Both QCLK_v and nQCLK_v are single-ended LVCMOS 1.8V outputs, QCLK_V and nQCLK_V are complementary (180° phase difference).</td></tr>
</table>

[a] *y* = A0,A1,A2,A3,B0,B1,B2,B3,C0,C1,C2,C3,D0,D1,D2,D3,D4,D5.

[b] For V_{TT} (Termination voltage) values (Table 50).

Status Registers

Table 36. Status Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x4C	Reserved	Reserved	IE_LOLF	IE_LOLV	IE_REF	IE_HOLD	IE_CLK_1	IE_CLK_0
0x50	Reserved	Reserved	nLS_LOLF	nLS_LOLV	LS_REF	nLS_HOLD	LS_CLK_1	LS_CLK_0
0x51	Reserved	ST_SEL	nST_LOLF	nST_LOLV	ST_REF	nST_HOLD	ST_CLK_1	ST_CLK_0
0x53	Reserved	Reserved	Reserved	Reserved	Reserved	ST_CAL	Reserved	Reserved

Table 37. Status Register Descriptions[a]

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
IE_LOLF	R/W	0	Interrupt Enable for FemtoClock NG PLL Loss-of-lock: 0 = Disabled: Setting nLS_LOLF will not cause an interrupt on nINT. 1 = Enabled: Setting nLS_LOLF will assert the nINT output (nINT = 0, interrupt).
IE_LOLV	R/W	0	Interrupt Enable for VCXO-PLL Loss-of-lock: 0 = Disabled: Setting nLS_LOLV will not cause an interrupt on nINT. 1 = Enabled: Setting nLS_LOLV will assert the nINT output (nINT = 0, interrupt).
IE_CLK_*n*	R/W	0	Interrupt Enable for CLK*n* input Loss-of-signal: 0 = Disabled: Setting LS_CLK_*n* will not cause an interrupt on nINT. 1 = Enabled: Setting LS_CLK_*n* will assert the nINT output (nINT = 0, interrupt).
IE_REF	R/W	0	Interrupt Enable for LS_REF: 0 = Disabled: Any changes to LS_REF will not cause an interrupt on nINT. 1 = Enabled: Any changes to LS_REF will assert the nINT output (nINT = 0, interrupt).
IE_HOLD	R/W	0	Interrupt Enable for Holdover: 0 = Disabled: Setting nLS_HOLD will not cause an interrupt on nINT. 1 = Enabled: Setting nLS_HOLD will assert the nINT output (nINT = 0, interrupt).
nLS_LOLF	R/W	—	FemtoClock NG PLL Loss-of-lock (latched status of nST_LOLF): Read 0 = ≥1 Loss-of-lock events detected after the last status latch clear. Read 1 = No Loss-of-lock detected after the last status latch clear. Write 1 = Clear status latch (clears pending nLS_LOLF interrupt).
nLS_LOLV	R/W	—	VCXO-PLL Loss-of-lock (latched status of nST_LOLV): Read 0 = ≥1 Loss-of-lock events detected after the last status latch clear. Read 1 = No Loss-of-lock detected after the last nLS_LOLV clear. Write 1 = Clear status latch (clears pending nLS_LOLV interrupt).

Table 37. Status Register Descriptions[a] (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
LS_CLK_*n*	R/W	—	Input CLK_*n* Status (latched status of ST_CLK_*n*): Read 0 = ≥1 LOS events detected on CLK_*n* after the last LS_CLK_*n* clear. Read 1 = No loss-of-signal detected on CLK_*n* input after the last LS_CLK_*n* clear. Write 1 = Clear LS_CLK_*n* status latch (clears pending LS_CLK_*n* interrupts on nINT).
ST_SEL	R	—	Input Selection (momentary): Reference input selection status of the state machine. In any input selection mode, reflects the input selected by the state machine. 0 = CLK_0 1 = CLK_1
nST_LOLF	R	—	FemtoClock NG PLL Loss-of-lock (momentary): Read 0 = ≥1 Loss-of-lock events detected Read 1 = No Loss-of-lock detected A latched version of this status bit is available (nLS_LOLF).
nST_LOLV	R	—	VCXO-PLL Loss-of-lock (momentary): Read 0 = ≥1 Loss-of-lock events detected Read 1 = No Loss-of-lock detected A latched version of this status bits is available (nLS_LOLV).
ST_CLK_*n*	R	—	Input CLK_*n* Status (momentary): 0 = LOS detected on CLK_*n.* 1 = No LOS detected, CLK_*n* input is active. A latched version of this status bits are available (LS_CLK_*n*).
LS_REF	R/W	—	PLL Reference Status (latched status of ST_REF): Read 0 = Reference is lost since last reset of this status bit. Read 1 = Reference is valid since last reset of this status bit. Write 1 = Clear LS_REF status latch (clears pending LS_REF interrupts on nINT).
nLS_HOLD	R/W	—	Holdover Status Indicator (latched status of ST_HOLD): Read 0 = VCXO-PLL has entered holdover state ≥1 times after reset of this status bit. Read 1 = VCXO-PLL is (or attempts to) lock(ed) to an input clock. Write 1 = Clear status latch (clears pending nLS_HOLD interrupt).
ST_VCOF	R	—	FemtoClock NG PLL Calibration Status (momentary): Read 0 = FemtoClock NG PLL auto-calibration is completed. Read 1 = FemtoClock NG PLL calibration is active (not completed).
ST_REF	R	—	Input Reference Status. 0 = No input reference present. 1 = Input reference is present at the clock selected input clock.

Table 37. Status Register Descriptions[a] (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
nST_HOLD	R	—	Holdover Status Indicator (momentary): 0 = VCXO-PLL in holdover state, not locked to any input clock. 1 = VCXO-PLL is (or attempts to) lock(ed) to input clock. A latched version of this status bit is available (nLS_HOLD).
ST_CAL	R	—	FemtoClock NG PLL Calibration Status (momentary): Read 0 = FemtoClock NG PLL auto-calibration is completed. Read 1 = FemtoClock NG PLL calibration is active (not completed).

[a] CLK*n* = CLK*0*, CLK*1*.

General Control Registers

Table 38. General Control Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x55	INIT_CLK							
0x56	RELOCK							
0x57	PB_CAL							

Table 39. General Control Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
INIT_CLK	W only Auto-Clear	X	Set INIT_CLK = 1 to initialize divider functions. Required as part of the startup procedure.
RELOCK	W only Auto-Clear	X	Setting this bit to 1 will force the FemtoClock NG PLL to re-lock.
PB_CAL	W only Auto-Clear	X	Precision Bias Calibration: Setting this bit to 1 will start the calibration of an internal precision bias current source. The bias current is used as reference for outputs configured as LVDS, and as reference for the charge-pump currents. This bit will auto-clear after the calibration completed. Set as part of the startup procedure.

Electrical Characteristics

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V19N478 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 40. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD_V} and V_{DDO_V}	3.6V
Inputs	-0.5V to V_{DD_V} +0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DDO_V} +0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O (LVDS) Continuous Current Surge Current	 50mA 100mA
Operating Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD – Human Body Model[a]	2000V
ESD – Charged Device Model[a]	500V

[a] According to JEDEC JS-001-2012/JESD22-C101.

Pin Characteristics

Table 41. Input Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ±5%, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}[a]	Input Capacitance	OSC, nOSC		2	4	pF
		Other inputs		2	4	pF
R_{PU}	Input Pull-Up Resistor	nCLK_0, nCLK_1		51		kΩ
R_{PD}	Input Pull-Down Resistor	CLK_0, nCLK_0, CLK_1, nCLK_1, EXT_SEL, ADR1/MISO, I2C		51		kΩ
R_{OUT}	LVCMOS Output Impedance	nINT, LOCK		25[b]		W

[a] Guaranteed by design.

[b] Design target specifications.

DC Characteristics

The device is configured to the maximum values of register settings, all outputs enabled in LVDS mode, and amplitude of 850mV. Process variation is included for the maximum current consumption.

Table 42. Power Supply DC Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD_V}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO_V}	Output Supply Voltage		1.71	1.8, 2.5, 3.3	3.465	V
I_{DD_V}	Power Supply Current			580	1024	mA

Table 43. Typical Power Supply DC Current Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a]

Symbol	Supply Pin Current		Test Case 1[b]	2[b]	3[c]	4[c]	5[c]	6[c]	Units
–	QCLK_A[3:0], QCLK_B[3:0]	$V_{DDO\_QCLKA, \_QCLKB}$	3.3	3.3	3.3	3.3	1.8	1.8	V
		Style	LVDS	LVDS	LVPECL	LVPECL	LVPECL	LVPECL	–
		State	On	On	On	On	On	On	–
		Amplitude	700	850	850	700	500	350	mV
–	QCLK_C[3:0], QCLK_D[5:0]	$V_{DDO\_QCLKC, \_QCLKD}$	3.3	3.3	3.3	3.3	1.8	1.8	V
		Style	LVDS	LVDS	LVPECL	LVPECL	LVDS	LVDS	–
		State	On	On	On	On	On	On	–
		Amplitude	700	850	850	700	500	350	mV
I_{DD_COA}	Current through V_{DDO_QCLKA} pin		0.088	0.109	0.135	0.123	0.104	0.090	A
I_{DD_CA}	Current through V_{DD_QCLKA} pin		0.039	0.039	0.037	0.037	0.037	0.037	A
I_{DD_COB}	Current through V_{DDO_QCLKB} pin		0.088	0.109	0.131	0.118	0.099	0.087	A
I_{DD_CB}	Current through V_{DD_QCLKB} pin		0.034	0.034	0.038	0.038	0.038	0.038	A
I_{DD_COC}	Current through V_{DDO_QCLKC} pin		0.088	0.109	0.135	0.122	0.139	0.119	A
I_{DD_CC}	Current through V_{DD_QCLKC} pin		0.039	0.039	0.036	0.036	0.036	0.036	A
I_{DD_COD}	Current through V_{DDO_QCLKD} pin		0.132	0.164	0.188	0.170	0.196	0.167	A
I_{DD_CD}	Current through V_{DD_QCLKD} pin		0.044	0.044	0.045	0.045	0.045	0.045	A
I_{DD_SPI}	Current through V_{DD_I2C} pin		0.009	0.009	0.009	0.009	0.009	0.009	A
I_{DD_INP}	Current through V_{DD_INP} pin		0.013	0.013	0.013	0.013	0.013	0.013	A
I_{DD_LCV}	Current through V_{DD_LCV} pin		0.077	0.081	0.080	0.080	0.080	0.080	A
I_{DD_LCF}	Current through V_{DD_LCF} pin		0.060	0.060	0.060	0.060	0.060	0.060	A
I_{DD_CPV}	Current through V_{DD_CPV} pin		0.014	0.014	0.014	0.014	0.014	0.014	A
I_{DD_CPF}	Current through V_{DD_CPF} pin		0.056	0.056	0.055	0.055	0.055	0.055	A
I_{DD_OSC}	Current through V_{DD_OSC} pin		0.006	0.006	0.006	0.006	0.006	0.006	A
I_{DD_TOT}	Total Device Current Consumption		0.787	0.887	0.982	0.927	0.931	0.857	A
$P_{TOT, SYS}$	Total System Power Consumption[d]		2.596	2.928	3.242	3.058	2.267	2.132	W
P_{TOT}	Total Device Power Consumption		2.596	2.928	2.165	2.051	2.025	1.881	W

[a] Design target specifications.

[b] f_{CLK} (input) = 40MHz, f_{VCXO} = 156.25MHz, f_{VCO} = 2500MHz, PV = 160, MV = 625, MF = 8, FDF = 1. Supply current is independent of the output frequency configuration used for this table: QCLKA[3:0] = 41.66MHz, QCLKB[3:0] = 500MHz, QCLKC[3:0] = 31.25MHz, QCLKD[5:0] = 500MHz. QCLK_y outputs terminated according to amplitude settings: LVPECL outputs terminated to V_{TT}.

[c] f_{CLK} (input) = 125MHz, f_{VCXO} = 156.25MHz, f_{VCO} = 2500MHz, PV = 1024, MV = 1280, MF = 8, FDF = 1. Supply current is independent of the output frequency configuration used for this table: QCLKA[3:0] = 125MHz, QCLKB[3:0] = 156.25MHz, QCLKC[3:0] = 250MHz, QCLKD[5:0] = 312.5MHz. QCLK_y outputs terminated according to amplitude settings: LVPECL outputs terminated to V_{TT}.

[d] Includes total device power consumption and the power dissipated in external output termination components.

Table 44. LVCMOS DC Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Control inputs, (1.8V/JESD7A-8 logic, input hysteresis and 3.3V tolerance)							
V_I	Input Voltage			-0.3		V_{DD_V}	V
V_{T+}	Positive-going Input Threshold Voltage			0.660		1.365	V
V_{T-}	Negative-going Input Threshold Voltage			0.495		1.170	V
V_H	Hysteresis Voltage		$V_{T+} - V_{T-}$	0.165		0.780	V
I_{IH}	Input High Current	Input (PD)[b] and Input (PD/PU)[c]	V_{DD_V} = 3.3V, V_{IN} = 3.3V			150	µA
		Input (PU)[d]				5	
I_{IL}	Input Low Current	Input (PD)[b]	V_{DD_V} = 3.465V, V_{IN} = 0V	-5			µA
		Input (PU)[d] and Input (PD/PU)[c]		-150			
Control outputs ADR1/MISO (when output), nINT, LOCK configured to 3.3V (SELSV0 = 0, SELSV1 = 0)							
V_{OH}	Output High Voltage	ADR1/MISO (when output), nINT, LOCK	I_{OH} = -4mA	2.0			V
V_{OL}	Output Low Voltage		I_{OL} = 4mA			0.55	V
Control outputs ADR1/MISO (when output), nINT, LOCK configured to 1.8V (SELSV0 = 1, SELSV1 = 1)							
V_{OH}	Output High Voltage		I_{OH} = -4mA	1.35		1.8	V
V_{OL}	Output Low Voltage		I_{OL} = 4mA			0.45	V
Clock outputs QCLK_V, nQCLK_V configured to LVCMOS (STYLE_V[1:0] = 1×)							
V_{OH}	Output High Voltage		I_{OH} = -8mA	1.35		1.8	V
V_{OL}	Output Low Voltage		I_{OL} = 8mA			0.45	V

[a] Design target specifications.

[b] EXT_SEL.

[c] I2C_A, ADR3, ADR2, ADR1, ADR0.

[d] SDAT, SCL.

Table 45. Differential Input DC Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	Pull-down inputs[a]	V_{DD_V} = V_{IN} = 3.465V			150	µA
		Pull-down/pull-up inputs[b]				150	µA
I_{IL}	Input Low Current	Pull-down inputs[a]	V_{DD_V} = 3.465V, V_{IN} = 0V	-150			µA
		Pull-down/pull-up inputs[b]		-150			µA

[a] Non-Inverting inputs: CLK_0, CLK_1, OSC.

[b] Inverting inputs: nCLK_0, nCLK_1, nOSC.

Table 46. LVPECL DC Characteristics (QCLK_y, STYLE = 1), V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[b][c]	350mV amplitude setting	V_{DDO_V} - 1.034	V_{DDO_V} - 0.892	V_{DDO_V} - 0.750	V
		500mV amplitude setting	V_{DDO_V} - 1.057	V_{DDO_V} - 0.912	V_{DDO_V} - 0.768	V
		700mV amplitude setting	V_{DDO_V} - 1.092	V_{DDO_V} - 0.950	V_{DDO_V} - 0.808	V
		850mV amplitude setting	V_{DDO_V} - 1.087	V_{DDO_V} - 0.960	V_{DDO_V} - 0.833	V
V_{OL}	Output Low Voltage[b][c]	350mV amplitude setting	V_{DDO_V} - 1.413	V_{DDO_V} - 1.265	V_{DDO_V} - 1.117	V
		500mV amplitude setting	V_{DDO_V} - 1.574	V_{DDO_V} - 1.420	V_{DDO_V} - 1.266	V
		700mV amplitude setting	V_{DDO_V} - 1.782	V_{DDO_V} - 1.633	V_{DDO_V} - 1.485	V
		850mV amplitude setting	V_{DDO_V} - 1.918	V_{DDO_V} - 1.778	V_{DDO_V} - 1.638	V

[a] Design target specifications.

[b] Outputs terminated with 50Ω to V_{TT}. For termination voltage V_{TT} values (Table 50).

[c] 700mV and 850mV amplitude settings are only available at $V_{DDO\_V} \geq 2.5V$.

Table 47. LVDS DC Characteristics (QCLK_y, STYLE = 0), V_{DD_V} = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OS}	Offset Voltage[b][c]	350mV amplitude setting	V_{DDO_V} - 1.034	V_{DDO_V} - 0.947	V_{DDO_V} - 0.862	V
		500mV amplitude setting	V_{DDO_V} - 1.133	V_{DDO_V} - 1.045	V_{DDO_V} - 0.961	V
		700mV amplitude setting	V_{DDO_V} - 1.229	V_{DDO_V} - 1.142	V_{DDO_V} - 1.056	V
		850mV amplitude setting	V_{DDO_V} - 1.316	V_{DDO_V} - 1.226	V_{DDO_V} - 1.138	V
ΔV_{OS}	V_{OS} Magnitude Change			25	50	mV

[a] Design target specifications.

[b] V_{OS} changes with V_{DD}.

[c] 700mV and 850mV amplitude settings are only available at $V_{DDO\_V} \geq 2.5V$.

AC Characteristics

Table 48. AC Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a][b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency		CLK_*n*	0.008		250	MHz
f_{VCXO}	VCXO Frequency			10	156.25	250	MHz
$f_{PFD, F}$	Phase-Frequency Detector Frequency		FemtoClock NG			250	MHz
f_{VCO}	VCO Frequency Range			2400		2500	MHz
f_{OUT}	Output Frequency	Integer Divider	QCLK_*y*, N = ÷1	2400		2500	MHz
			QCLK_*y*, N = ÷2	1200		1250	MHz
			QCLK_*y*, N = ÷4	600		625	MHz
			QCLK_*y*, N = ÷8	300		312.5	MHz
			QCLK_*y*, N = ÷10	240		250	MHz
			QCLK_*y*, N = ÷16	150		156.25	MHz
			QCLK_*y*, N = ÷20	120		125	MHz
		Fractional Divider	QCLK_D, ND range: 29.99 to 8.33	80		300	MHz
Δf_{OUT}	Output Frequency Accuracy		Integer output divider N[A:C]			0	ppb
			Fractional output divider ND, f_{OUT} = 156.25MHz			10	ppb
V_{IN}	Input Voltage Amplitude[c]	CLK_*n*		0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Amplitude[c] [d]	CLK_*n*		0.3		2.4	V
V_{CMR}	Common Mode Input Voltage			1.0		$V_{DD\_V} - (V_{IN} / 2)$	V
odc	Output Duty Cycle		QCLK_*y*	45	50	55	%
t_R / t_F	Output Rise/Fall Time, Differential		QCLK_*y* (LVPECL), 20% to 80%			200	ps
			QCLK_*y* (LVDS), 20% to 80%			300	ps
	Output Rise/Fall Time		LVCMOS outputs, 20%-80%			1.2	ns
$V_{O(PP)}$[e]	LVPECL Output Voltage Swing, Peak-to-peak, 156.25MHz		350mV amplitude setting	351	388		mV
			500mV amplitude setting	477	528		mV
			700mV amplitude setting	645	711		mV
			850mV amplitude setting	770	850		mV
	LVPECL Differential Output Voltage Swing, Peak-to-peak, 156.25MHz		350mV amplitude setting	702	776		mV
			500mV amplitude setting	954	1055		mV
			700mV amplitude setting	1290	1422		mV
			850mV amplitude setting	1540	1700		mV

Table 48. AC Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a][b] (Cont.)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}[f]	LVDS Output Voltage Swing, Peak-to-peak, 156.25MHz	350mV amplitude setting	265	340		mV
		500mV amplitude setting	362	465		mV
		700mV amplitude setting	611	676		mV
		850mV amplitude setting	746	818		mV
	LVDS Differential Output Voltage Swing, Peak-to-peak, 156.25MHz	350mV amplitude setting	530	680		mV
		500mV amplitude setting	724	929		mV
		700mV amplitude setting	1222	1351		mV
		850mV amplitude setting	1492	1635		mV
*t*sk(o)	Output Skew[g] [h] All delays set to 0	QCLK_*y* (same N divider)			60	ps
		QCLK_*y* (any N divider, incident rising edge)			50	ps
$t_{D, LOS}$	LOS State Detected (measured in input reference periods)	$f_{IN} \leq 125MHz$			2	T_{IN}
		$f_{IN} > 125MHz$			3	
$t_{D, LOCK}$	PLL Lock Detect	PLL re-lock time after a short-term holdover scenario. Measured from LOS to both PLLs lock-detect asserted; hold-off timer = 200, VCXO-PLL bandwidth = 30Hz, 100Hz initial frequency error <200ppm		30Hz - 30.2 100Hz - 22.6	300	ms
$t_{D, RES}$	PLL Lock Residual Time Error	Refer to PLL lock detect $t_{D,LOCK}$. Reference point: final value of clock output phase after all phase transitions settled.		30Hz - 0.049 100Hz - 0.191	20	ns
Δf_{HOLD}	Holdover Accuracy	Max. frequency deviation during a holdover duration of 200ms and after the clock re-validate event		30Hz - 1.57 100Hz - 3.34	±5.0	ppm

[a] Design target specifications.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] V_{IL} should not be less than -0.3V and V_{IH} should not be greater than V_{DD_V}.

[d] Common Mode Input Voltage is defined as the cross-point voltage.

[e] LVPECL outputs terminated with 50Ω to V_{DDO_V} – 1.6V (350mV amplitude setting), V_{DDO_V} – 1.75V (500mV amplitude setting), V_{DDO_V} – 1.95V (700mV amplitude setting), V_{DDO_V} – 2.1V (850mV amplitude setting).

[f] LVDS outputs terminated 100Ω across terminals.

[g] This parameter is defined in accordance with JEDEC standard 65.

[h] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

Table 49. Clock Phase Noise Characteristics (f_{VCXO} = 156.25MHz), V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C [a][b][c]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
tjit(Ø)	Clock RMS Phase Jitter (Random)	156.25MHz	Integration Range: 12kHz – 20MHz		65		fs
		250MHz	Integration Range: 12kHz – 20MHz		58		fs
Φ_N(10)	Clock Single-side Band Phase Noise (integer divider)	500MHz	10Hz offset (determined by VCXO)		-66.8		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-85.7		dBc/Hz
Φ_N(1k)			1kHz offset from carrier		-116.3	-110	dBc/Hz
Φ_N(10k)			10kHz offset from carrier		-133	-120	dBc/Hz
Φ_N(100k)			100kHz offset from carrier		-137.6		dBc/Hz
Φ_N(1M)			1MHz offset from carrier		-145.4	-142	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from carrier and noise floor		-157.5	-150	dBc/Hz
Φ_N(10)	Clock Single-side Band Phase Noise (integer divider)	250MHz	10Hz offset (determined by VCXO)		-73.8		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-91.4		dBc/Hz
Φ_N(1k)			1kHz offset from carrier		-122.0		dBc/Hz
Φ_N(10k)			10kHz offset from carrier		-138.9	-130	dBc/Hz
Φ_N(100k)			100kHz offset from carrier		-143.8	-135	dBc/Hz
Φ_N(1M)			1MHz offset from carrier		-151.3	-150	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from carrier and noise floor		-160.9	-155	dBc/Hz
Φ_N(10)	Clock Single-side Band Phase Noise (integer divider)	156.25MHz	10Hz offset (determined by VCXO)		-77.8		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-95.8		dBc/Hz
Φ_N(1k)			1kHz offset from carrier		-126.9		dBc/Hz
Φ_N(10k)			10kHz offset from carrier		-142.9		dBc/Hz
Φ_N(100k)			100kHz offset from carrier		-148		dBc/Hz
Φ_N(1M)			1MHz offset from carrier		-155.3		dBc/Hz
Φ_N(≥10M)			≥10MHz offset from carrier and noise floor		-162.8		dBc/Hz
Φ_N(10)	Clock Single-side Band Phase Noise	125MHz	10Hz offset (determined by VCXO)		-80.8		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-97.9		dBc/Hz
Φ_N(1k)			1kHz offset from carrier		-128.5	-120	dBc/Hz
Φ_N(10k)			10kHz offset from carrier		-144.7	-130	dBc/Hz
Φ_N(100k)			100kHz offset from carrier		-149.9	-135	dBc/Hz
Φ_N(1M)			1MHz offset from carrier		-156.8	-150	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from carrier and noise floor		-162.2	-155	dBc/Hz

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Phase noise specifications are applicable for all outputs active, Nx not equal.

[c] VCXO characteristics: 156.25MHz and phase noise -67.9dBc/Hz at 10Hz, -97.9dBc/Hz at 100Hz, -121.9dBc/Hz at 1kHz, -141.9dBc/Hz at 10kHz, -152.9dBc/Hz at 100kHz.

Clock Phase Noise Characteristics

VCXO characteristics: 156.25MHz and phase noise -67.9dBc/Hz at 10Hz, -97.9dBc/Hz at 100Hz, -121.9dBc/Hz at 1kHz, -141.9dBc/Hz at 10kHz, -152.9dBc/Hz at 100kHz.

- Input reference frequency: 20MHz
- VCXO-PLL bandwidth: 30Hz
- VCXO-PLL charge pump current: 0.75mA
- FemtoClock-NG PLL bandwidth: 342kHz
- $V_{DD\_V} = 3.3V$, $T_A = 25°C$

Figure 5. 312.5MHz Output Phase Noise

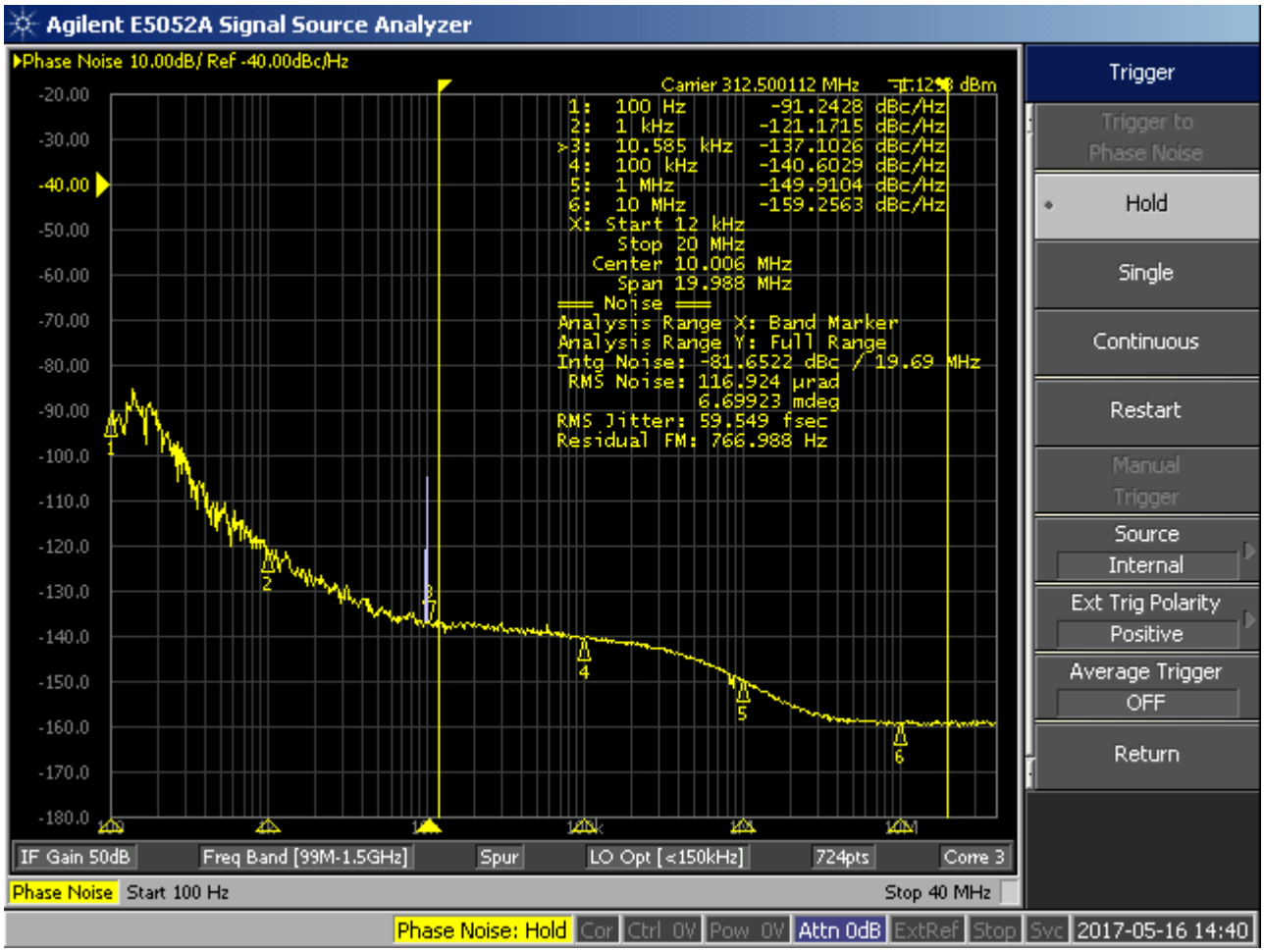


Figure 6. 125MHz Output Phase Noise

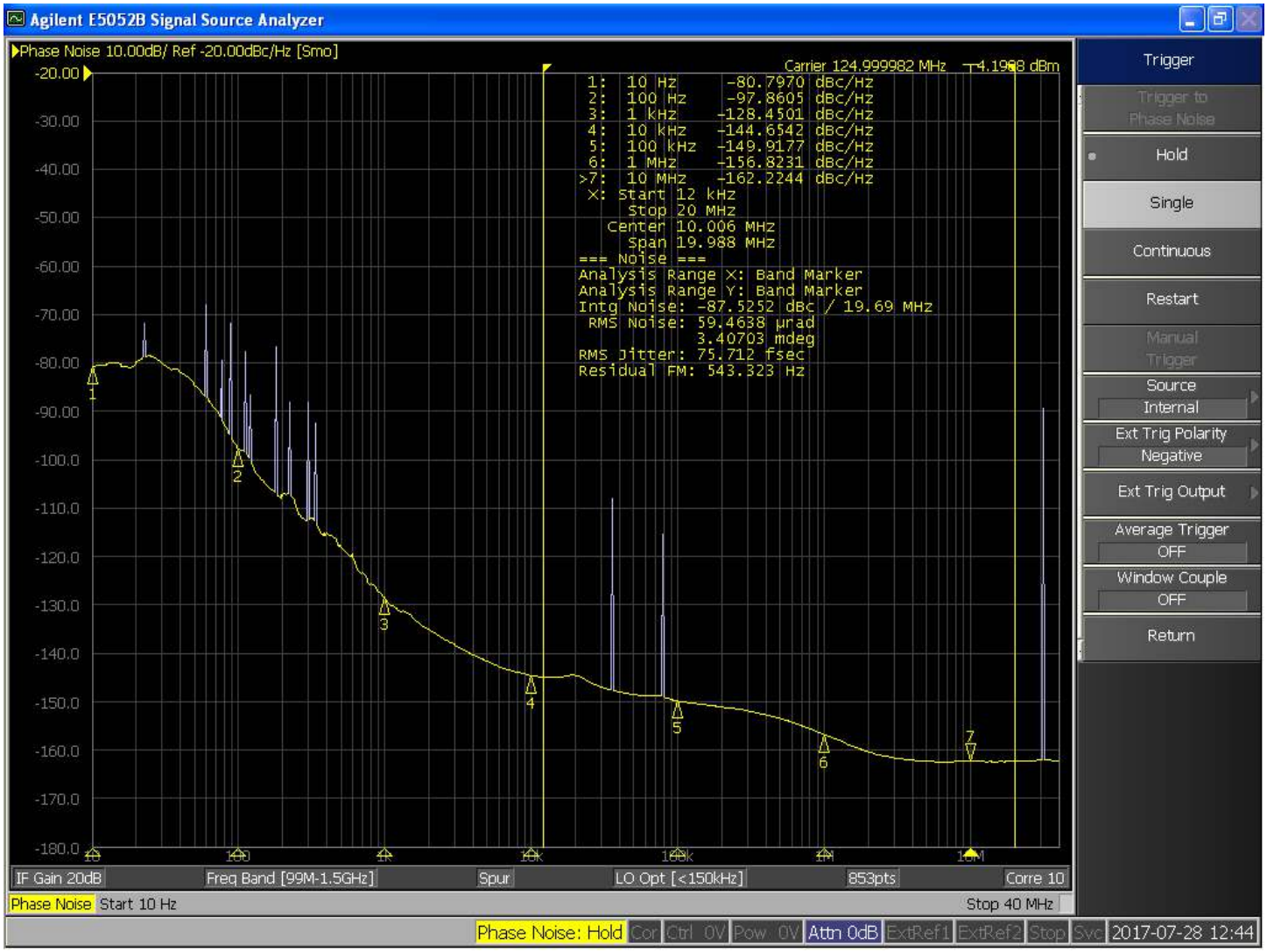


Figure 7. 156.25MHz Output Phase Noise

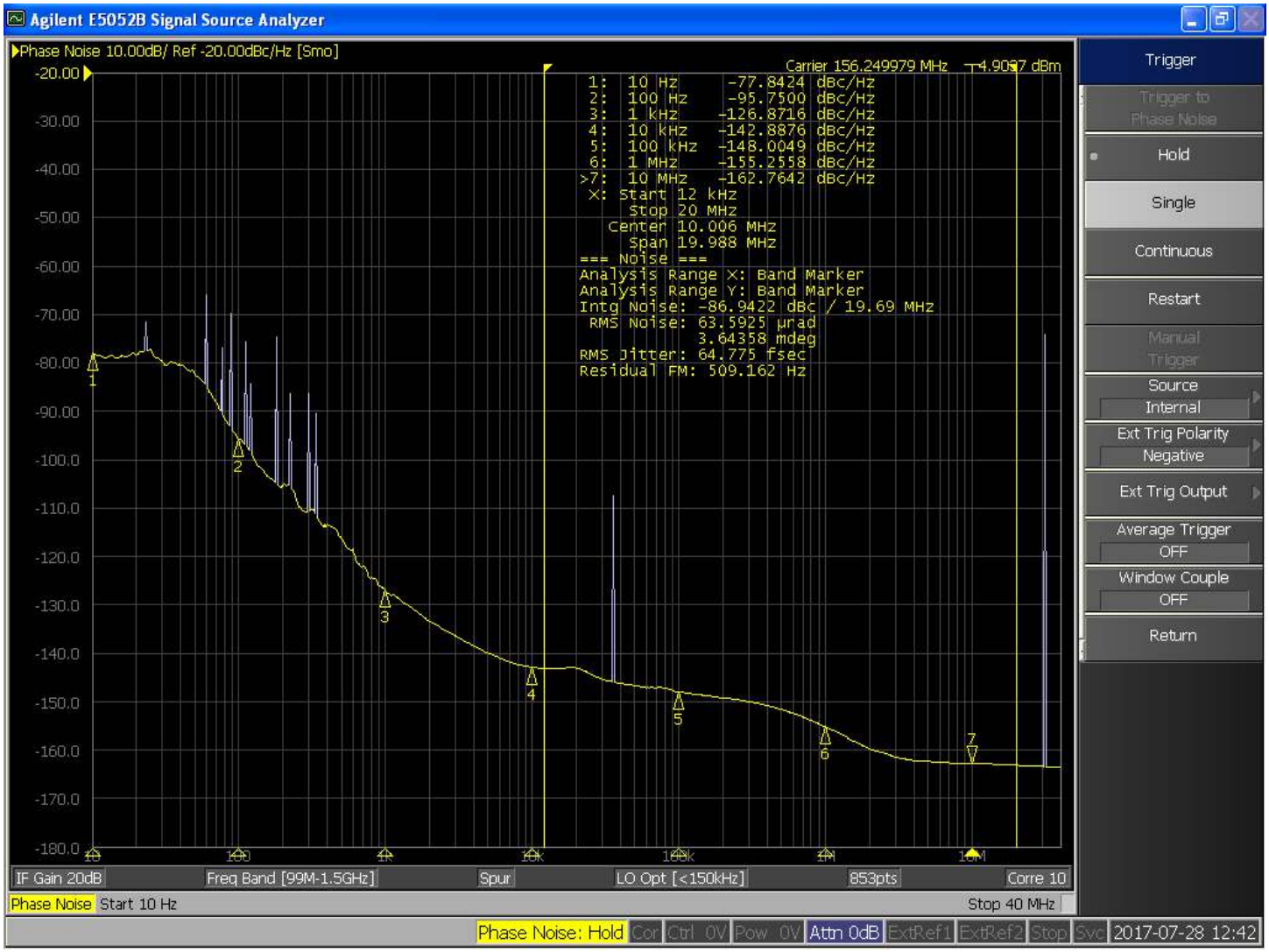


Figure 8. 250MHz Output Phase Noise

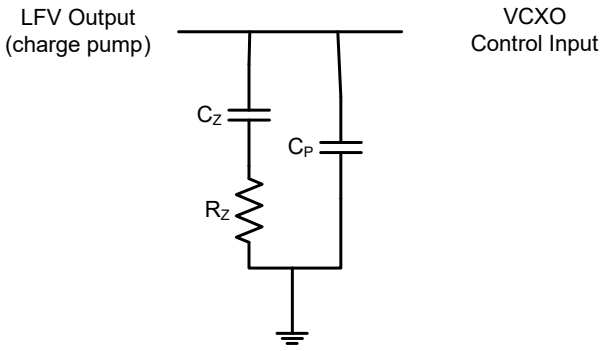
Figure 9. 500MHz Output Phase Noise

Applications Information

VCXO-PLL Loop Filter

Each of the two PLLs uses a loop filter with external components. The value of the external components depends on the desired loop bandwidth for each PLL, the input clock frequency, and in the case of the VCXO-PLL on the external VCXO component. For the VCXO-PLL (first PLL stage), a 2nd or 3rd order loop filter may be used. The loop filter of the VCXO-PLL is connected to the device through the LFV charge-pump input. The filter output is connected to the control voltage input of the external VCXO. The FemtoClock NG PLL (second PLL stage) may use a 2nd order loop filter. The LFF output of the device connects to filter input and LFFR to the filter output. Typical loop filters are shown in Figure 10 (2nd order) in Figure 11 (3rd order) and are discussed below. Step by step calculations to determine the value of the loop filter components values are shown.

Figure 10. Second-Order Loop Filter



Step-by-step Calculation

Step 1: Determine the desired loop bandwidth f_C. f_C must satisfy the following condition:

$$\frac{f_{PD}}{f_C} \gg 20$$

Where f_{PD} is the input frequency of the VCXO-PLL phase detector frequency.

Step 2: Calculate R_Z by:

$$R_Z = \frac{2 \times \pi \cdot f_C \times M_V}{I_{CP} \times K_{VCXO}}$$

Where I_{CP} is the VCXO-PLL charge-pump current and K_{VCXO} is the gain of the VCXO component (consult the datasheet of the external VCXO for its gain parameter). M_V is the effective feedback divider:

$$M_V = \frac{f_{VCXO}}{f_{PD}}$$

f_{VCXO} is the frequency of the external VCXO component.

Step 3: Calculate C_Z by:

$$\alpha = \frac{f_C}{f_Z}$$

$$C_Z = \frac{\alpha}{2 \times \pi \times f_C \times R_Z}$$

α is ratio between the loop bandwidth and the filter zero. f_Z is the filter zero. α should be greater than 3.

Step 4: Calculate C_P by:

$$C_P = \frac{C_Z}{\alpha \times \beta}$$

$$\beta = \frac{f_P}{f_C}$$

f_P is the pole and β is ratio between the pole and the loop bandwidth. β should be greater than 3.

Step 5: Verify that the phase margin PM is greater than 50°.

$$PM = \operatorname{atan}\frac{b-1}{2 \times \sqrt{b}}$$

$$b = \frac{C_Z}{C_P} + 1$$

Example calculation: The Block Diagram shows a 2nd order loop filter for the VCXO-PLL. In this example, the VCXO-PLL reference frequency is 122.88MHz, and an external VCXO component of 122.88MHz is used. The desired VCXO-PLL loop bandwidth f_C is 40Hz. To achieve the desired loop bandwidth with small size loop filter components, set the PLL frequency pre-divider P_V, and the PLL feedback divider M_V to 1024. According to the step 1 instruction, f_{PD} is 120kHz. This satisfies the condition $f_{PD}/f_C >> 20$. R_Z is calculated 32.2kΩ.

The VCXO gain K_{VCXO} used for the device reference circuit is 10kHz/V. The charge-pump current of the VCXO-PLL is configurable from 50µA to 1200µA. The charge-pump current is programmed to $I_{CP} = 800uA$. For $\alpha = 8$, C_Z is calculated to be 0.99µF. C_Z greater than this value assures α > 12. For example, the actual chosen value is the standard capacitor value of 1µF. For $\beta = 5$, C_P is calculated 24.7nF. The standard capacitor value of $C_P = 27ps$ ensures β > 7.

Figure 11. Third-Order Loop Filter

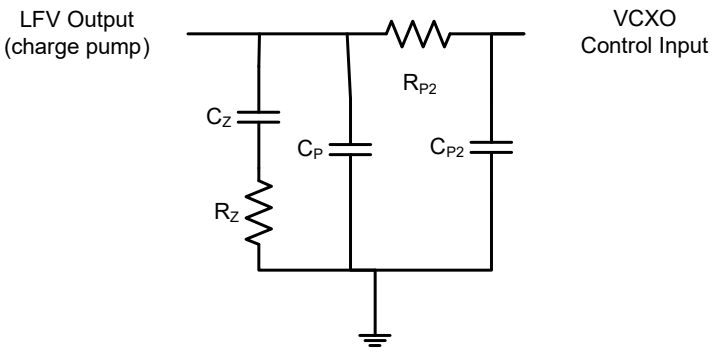


Figure 11 shows a third-order loop filter. The filter is equivalent to the 2nd order filter in Figure 12 with the addition components R_{P2} and C_{P2}. The additional components R_{P2} and C_{P2} should be calculated as shown:

$$C_{P2} = \frac{R_Z \times C_P}{R_{P2} \times \gamma}$$

$$R_{P2} \sim 1.5 \times R_Z$$

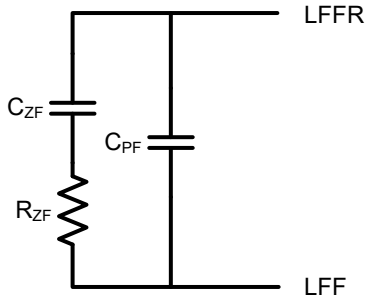
γ is the ratio between the 1st pole and the 2nd pole. γ should be greater than 3.

Example calculation for the 3rd order loop filter shown in Figure 11: Equivalent to the 2nd order loop filter calculation, $R_Z = 33k\Omega$, $C_Z = 1\mu F$, and $C_P = 27nF$. R_{P2} should be in the range of $0.5 \cdot R_Z < R_{P2} < 2.5 \cdot R_Z$, for instance $51k\Omega$. With $\gamma = 4$, C_{P2} is 4.37nF (select 4.7µF).

FemtoClock NG PLL Loop Filter

Figure 12 shows a 2nd order loop filter for the FemtoClock NG PLL. This loop filter is equivalent to Figure 10 and uses the loop filter components R_{ZF} (R_Z), C_{ZF} (C_Z), and C_{PZ} (C_P). The VCO frequency of the FemtoClock NG PLL is 2500MHz.

Figure 12. 2nd Order Loop Filer for FemtoClock NG PLL



Example calculation for the 2nd order loop filter shown in Figure 12: the FemtoClock NG receives its reference frequency from the VCXO output. With the P_F pre-divider set to 1, the phase detector frequency is also 122.88MHz. The PLL feedback divider must be set to $M_F = 24$ in order to locate the VCO frequencies in its center range. A target PLL loop bandwidth f_C is 80kHz satisfies the condition in step 1. The gain of the internal VCO is 30MHz/V and the charge-pump current I_{CP} is set to 3.6mA. Using the formula for R_Z in step 2, R_{ZF} is calculated 103Ω (chose the standard value of 100Ω); using the formula for C_Z in step 3, C_{ZF} is calculated 88nF for $\alpha = 4$. A capacitor larger than 88nF should be used for C_{ZF} to assure that the α is greater than 4, for instance the standard component capacitor value 100nF.

With $\beta = 6$, C_{PZ} is calculated to be 3.6nF as shown in step 4. A capacitor less than 3.6nF should be used for C_{PZ} to assure that β remains greater than 6, for instance the standard capacitor value of 1nF is selected for C_{PZ}. The selected 2nd order loop filter components are $R_{ZF} = 100\Omega$, $C_{ZF} = 100nF$ and $C_{PZ} = 1nF$.

Output Termination

LVPECL-style Outputs

Differential outputs configured to LVPECL-style are an open-emitter type, and require a termination with a DC current path to GND. This section displays parallel and thevenin termination, Y-termination and source termination for various output supply (V_{DDO_V}), and amplitude settings. V_{TT} is the termination voltage.

Figure 13. LVPECL Parallel Termination 1

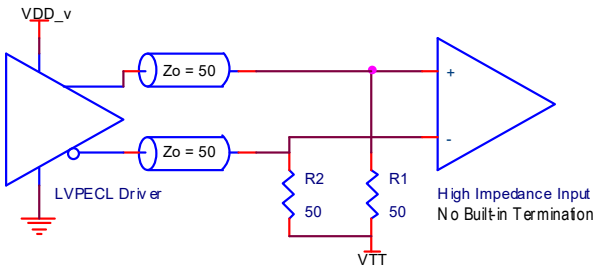


Table 50. Termination Voltage V_{TT} (Figure 13)[a]

LVPECL Amplitude (mV)	V_{TT} (V)
350	V_{DDO_V} – 1.60
500	V_{DDO_V} – 1.75
700	V_{DDO_V} – 1.95
850	V_{DDO_V} – 2.10

[a] Output power supplies supporting 3.3V, 2.5V and 1.8V are V_{DDO_QCLKA}, V_{DDO_QCLKB}, V_{DDO_QCLKC} and V_{DDO_QCLKD}.

Figure 14. LVPECL Parallel Termination 2

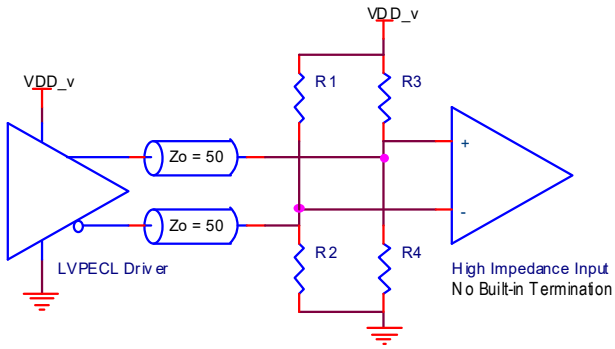


Table 51. Termination Resistor Values (Figure 14)

V_{DDO_V} (V)[a]	LVPECL Amplitude (mV)	R1, R3 (Ω)	R2, R4 (Ω)
3.3	350	97.1	103.1
	500	106.5	94.3
	700	122	84.6
	850	137.5	78.6
2.5	350	138.8	78.1
	500	166.7	71.4
	700	227.3	64.1
	850	312.5	59.5
1.8	350	450	56.3
	500	–	50

[a] Output power supplies supporting 3.3V, 2.5V, and 1.8V are V_{DDO_QCLKA}, V_{DDO_QCLKB}, V_{DDO_QCLKC} and V_{DDO_QCLKD}.

Figure 15. LVPECL Y-Termination

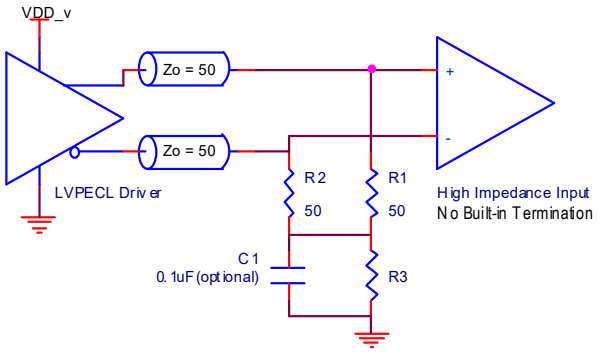


Table 52. Termination Resistor Values (Figure 15)

V_{DDO_V} (V)[a]	LVPECL Amplitude (mV)	R3 (Ω)
3.3	350, 500, 700, 850	50
2.5	350, 500, 700, 850	18
1.8	350, 500	0

[a] Output power supplies supporting 3.3V, 2.5V, and 1.8V are V_{DDO_QCLKA}, V_{DDO_QCLKB}, V_{DDO_QCLKC} and V_{DDO_QCLKD}.

Figure 16. LVPECL Source Termination

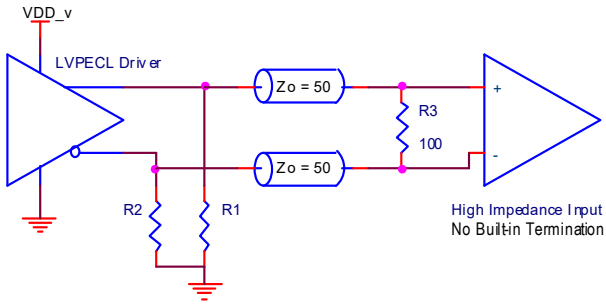


Table 53. Termination Resistor Values (Figure 16)

V_{DDO_V} (V)[a]	LVPECL Amplitude (mV)	R1, R2 (Ω)
3.3	350, 500, 700, 850	100 – 200
2.5	350, 500, 700, 850	80 – 150
1.8	350	50 – 100

[a] Output power supplies supporting 3.3V, 2.5V, and 1.8V are V_{DDO_QCLKA}, V_{DDO_QCLKB}, V_{DDO_QCLKC} and V_{DDO_QCLKD}.

LVDS-Style Outputs

LVDS style outputs support fully differential terminations. LVDS does not require board level pull-down resistors for DC termination. Figure 17 and Figure 18 show typical termination examples with DC coupling for the LVDS style driver. In these examples, the receiver is high input impedance without built-in termination. LVDS-style with a differential termination is preferred for best common-mode rejection and lowest device power consumption.

Figure 17. LVDS Termination

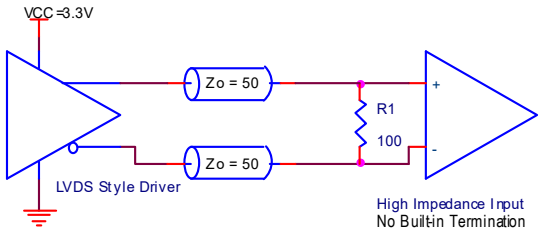
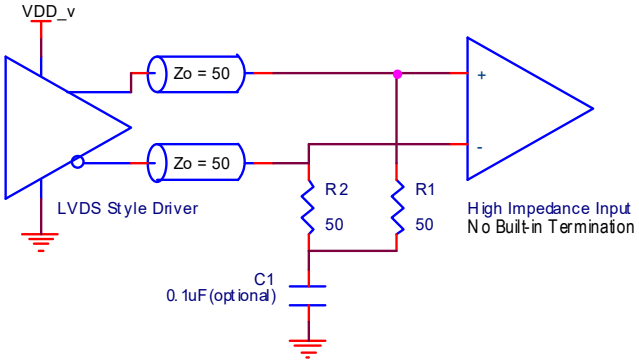


Figure 18. LVDS Termination (Alternative)



Power Supply Filtering

Please refer to the document *8V19N470 Hardware Design Guide* for comprehensive information about power supply and isolation, loop filter design for VCXO and VCO, schematics, input and output interfaces/terminations and an example schematics. This document shows a recommended power supply filter schematic in which the device is operated at V_{DD_V} = 3.3V (the output supply voltages of V_{DDO_V} = 3.3V, 2.5V, and 1.8V are supported). This example focuses on power supply connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

As with any high-speed analog circuitry, the power supply pins are vulnerable to the board supply or device generated noise. This device requires an external voltage regulator for the V_{DD_V} pins for isolation of board supply noise. This regulator (example component: PS7A8300RGT) is indicated in the schematic by the power supply, VREG_3.3V. Consult the voltage regulator specification for details for the required performance. To achieve optimum jitter performance, power supply isolation is required to minimize device generated noise. The V_{DD_LCF} terminal requires the cleanest power supply. The device provides separate power supplies to isolate any high switching noise from coupling into the internal PLLs and into other outputs as shown. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF and 0.01µF capacitors in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. To set configuration pins, pull-up and pull-down resistors can all be placed on the PCB side, opposite the device side, to free up device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

Thermal Characteristics

Table 54. Thermal Characteristics for the 100-FPBGA Package[a]

Multi-Layer PCB, JEDEC Standard Test Board				
Symbol	Thermal Parameter	Condition	Value[b]	Unit
Θ_{JA}	Junction-to-ambient	0m/s air flow	24.06	°C/W
		1m/s air flow	20.89	°C/W
		2m/s air flow	19.07	°C/W
		3m/s air flow	18.05	°C/W
		4m/s air flow	17.46	°C/W
		5m/s air flow	17.03	°C/W
Θ_{JC}	Junction-to-case		8.54	°C/W
Θ_{JB}	Junction-to-board[c]		6.43	°C/W
Ψ_{JB}	Junction-to-board[d]		4.15	°C/W

[a] Standard JEDEC 2S2P multilayer PCB.

[b] Estimated thermal values.

[c] Thermal model where the majority (>90%) of the heat dissipated in the component is conducted through the package bottom (balls). T_B is measured on or near the component lead.

[d] Thermal model where the heat dissipated to the ambient from all directions. T_B is measured on or near the component lead.

Temperature Considerations

The device supports applications in a natural convection environment as long as the junction temperature does not exceed the specified junction temperature T_J. In applications where the heat dissipates through the PCB, Ψ_{JB} is the correct metric to calculate the junction temperature. The following calculation uses the junction-to-board thermal characterization parameter Ψ_{JB} to calculate the junction temperature (T_J). Care must be taken to not exceed the maximum allowed junction temperature T_J of 125 °C.

The junction temperature T_J is calculated using the following equation: $T_J = T_B + P_{TOT} \times \theta_{JB}$

where:

- T_J is the junction temperature at steady state conditions in °C.
- T_B is the board temperature at steady state condition in °C, measured on or near the component lead.
- Θ_{JB} is the thermal characterization parameter to report the difference between T_J and T_B.
- P_{TOT} is the total device power dissipation.

Maximum power dissipation scenario: With the maximum allowed junction temperature and the maximum device power consumption and at the maximum supply voltage of 3.3V + 5%, the maximum supported board temperature can be determined. In the device configuration for the maximum power consumption, IDD_V is 1.024A. In this configuration, all outputs are active and configured to LVDS, the output amplitude is set to 850mV and outputs use a 100 Ohm termination:

- Total system power dissipation (incl. termination resistor power): PTOT = VDD_V, MAX · IDD_V, MAX = 3.465V · 1.024A = 3.548W

In this scenario and with the Theta_JB thermal model, the maximum supported board temperature is as follows:

TB, MAX = TJ_MAX - Theta_JB · PTOT

TB, MAX = 125°C - 6.43°C/W · 3.548W = 102.2°C

Table 55. Typical Power Consumption

	Device		Theta JB Thermal model	
	IDD_TOT	PTOT	T_J[a]	$T_{B, MAX}$[b]
Test Case	A	W	C	C
1b	0.787	2.596	101.7	108.3
2b	0.887	2.928	103.8	106.2
3c	0.982	2.165	98.9	111.1
4c	0.927	2.051	98.2	111.8
5c	0.931	2.025	98.0	112.0
6c	0.857	1.881	97.1	112.9

[a] Junction temperature at board temperature T_B = 85°C

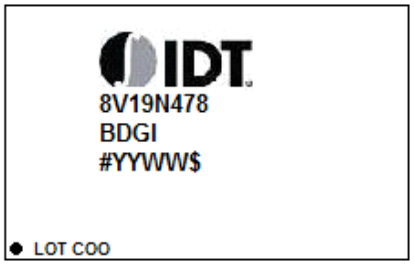
[b] Maximum board temperature for junction temperature < 125°C: $T_{B, MAX} = T_{J, MAX} - \theta_{JB} \times P_{TOT}$.

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/bdbdg100-package-outline-110-mm-sq-body-10-mm-pitch-cabga

Marking Diagram



1. Line 1 and Line 2 is the part number.
2. “#” denotes stepping.
3. “YYWW” denotes: “YY” is the last two digits of the year, and “WW” is a work week number that the part was assembled.
4. “$” denotes the mark code.

Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V19N478BDGI	IDT8V19N478BDGI	11 × 11 × 1 mm 100-FPBGA	Tray	-40°C to +85°C
8V19N478BDGI8	IDT8V19N478BDG	11 × 11 × 1 mm 100-FPBGA	Tape and Reel	-40°C to +85°C

Glossary

Abbreviation	Description
Index *n*	Denominates an clock input. Range: 0 to 1.
Index *x*	Denominates a channel, channel frequency divider and the associated configuration bits. Range: A, B, C, D.
Index y	Denominates a QCLK output and associated configuration bits. Range: A0, A1, A2, B0, B1, B2, C0, C1, D0, D1.
V_{DD_v}	Denominates core voltage supply pins. Range: V_{DD_QCLKA}, V_{DD_QCLKB}, V_{DD_QCLKC}, V_{DD_QCLKD}, V_{DD_I2C}, V_{DD_INP}, V_{DD_LCV}, V_{DD_LCF}, V_{DD_CPV}, V_{DD_CPF} and V_{DD_OSC}.
V_{DDO_v}	Denominates output voltage supply pins. Range: V_{DDO_QCLKA}, V_{DDO_QCLKB}, V_{DDO_QCLKC} and V_{DDO_QCLKD}.
status_condition	Status conditions are: LOLV (Loss of VCXO-PLL lock), LOLF (Loss of FemtoClock NG-PLL lock) and LOS (Loss of input signal).
[...]	Index brackets describe a group associated with a logical function or a bank of outputs.
{…}	List of discrete values.
Suffix V	Denominates a function associated with the VCXO-PLL.
Suffix F	Denominates a function associated with the 2nd stage PLL (FemtoClock NG).

Revision History

Revision Date	Description of Change
May 15, 2018	Added Figure 5 (312.5MHz Output Phase Noise)
May 2, 2018	Initial release.

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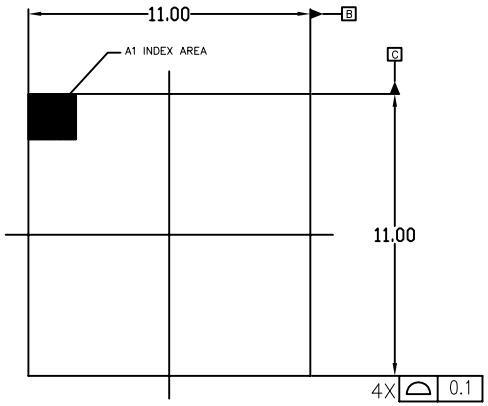
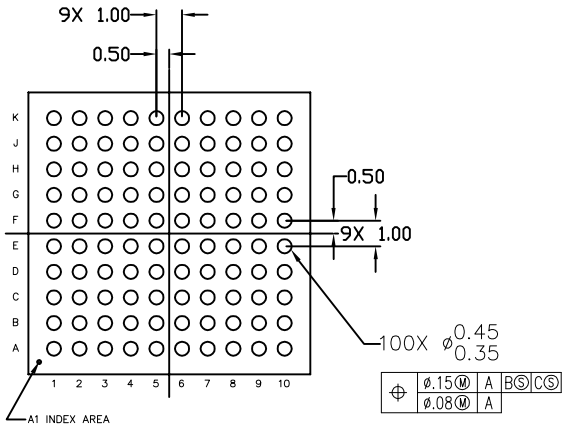
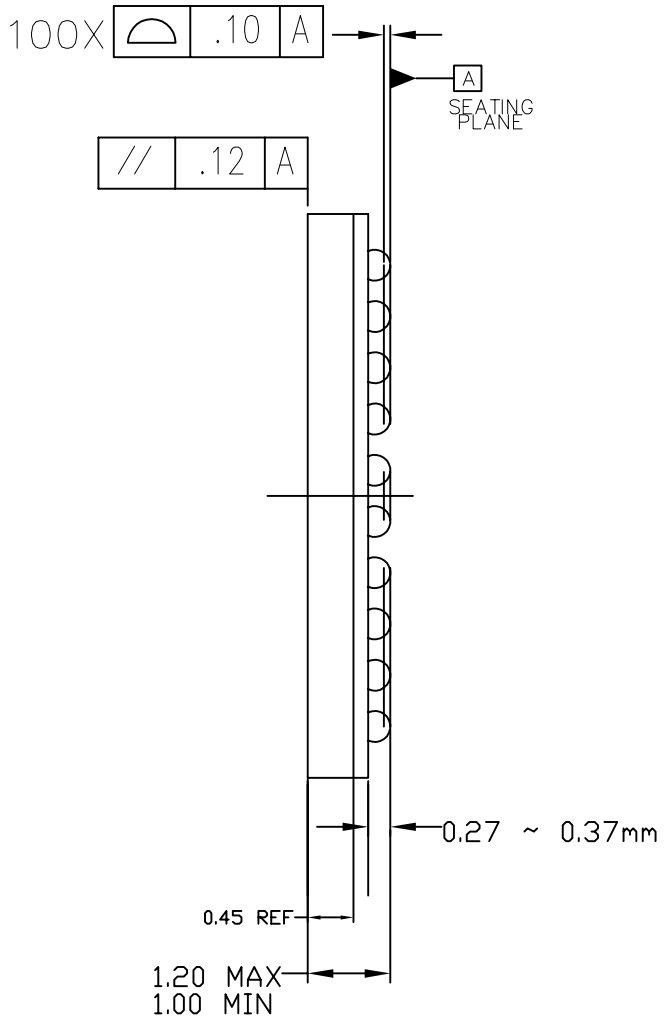
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/25/14	CM



TOP VIEW



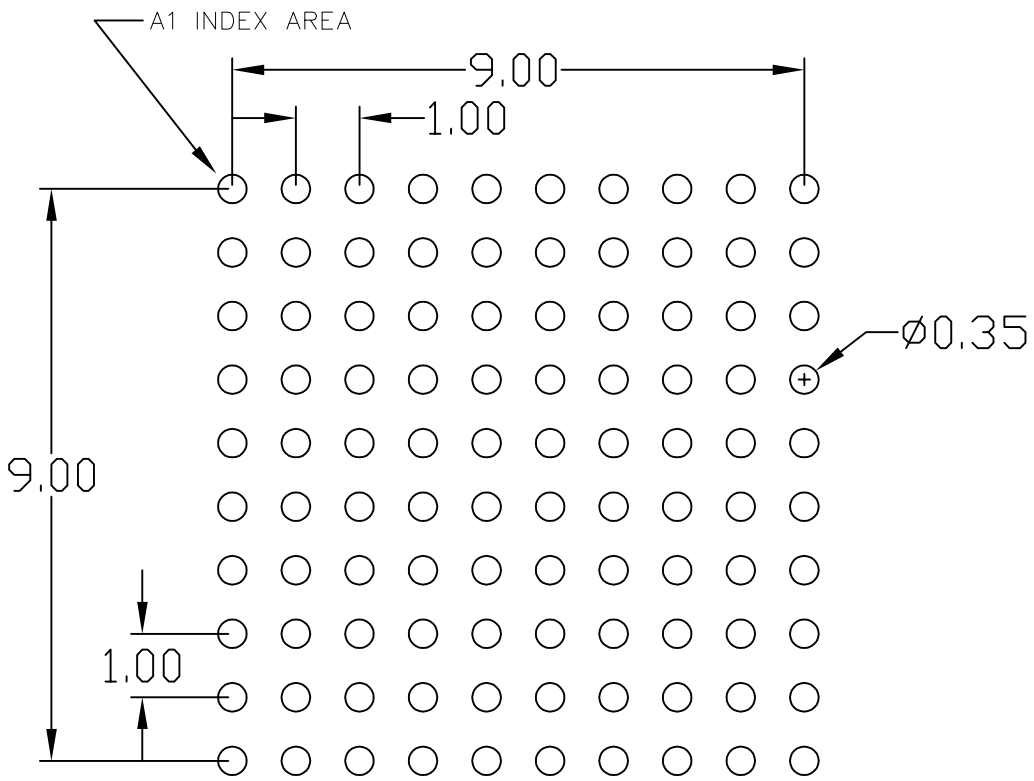
BOTTOM VIEW



SIDE VIEW

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX±0.10 ± XXX±0.050 XXXX±		IDT® 6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com
APPROVALS	DATE	TITLE BD/BDG100 PACKAGE OUTLINE 11.0 mm SQ BODY 1.0 mm PITCH CABGA
DRAWN CM	11/25/14	
CHECKED		
		SIZE C / DRAWING No. PSC-4491 / REV 00
		DO NOT SCALE DRAWING / SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/25/14	CM



RECOMMENDED LAND PATTERN

NOTE:

1) ALL dimensions are in mm, Angles in degrees.
2) Top down view, as view on PCB.
3) NSMD Land Pattern Assumed
4) Land Pattern Recommendation as per IPC-7351B generic requirement for surface mount design and Land Pattern.

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		DO NOT SCALE DRAWING	SHEET 2 OF 2