FEATURES OVERVIEW

- Interleaved PFC/PWM switching
- Green-mode PFC and PWM operation
- No switching of PFC at light loads for best power saving
- Low start-up and operating current
- Innovative switching-charge multiplier-divider
- Multi-vector control for improved PFC output transient response
- Average-current-mode Control for PFC
- Programmable two-level PFC output voltage
- PFC over-voltage and under-voltage protections
- PFC and PWM feedback open-loop protection
- Cycle-by-cycle current limiting for PFC/PWM
- Slope compensation for PWM
- Constant power limit for PWM
- Brownout protection

APPLICATIONS

Switching Power Suppliers with Active PFC

High-Power Adaptors

DESCRIPTION

The highly integrated SG6903 is specially designed for power supplies consist of boost PFC and flyback PWM. It requires very few external components to achieve green-mode operation and versatile protections. It is available in 16-pin SOP packages.

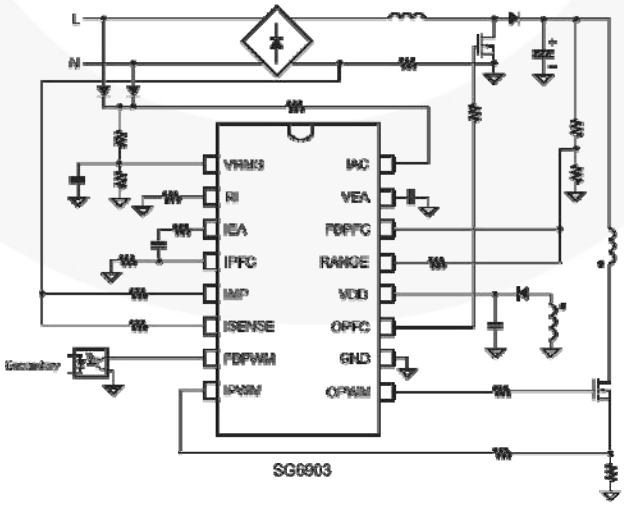
The proprietary interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light loads, the switching frequency is continuously decreased to reduce power consumption. If output loading is further reduced, the PFC stage is turned off to further reduce power consumption.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6903 will shut off PFC to prevent extra-high voltage on output. Programmable two-level output voltage control will reduce the PFC output voltage at low line input to increase the efficiency of the power supply.

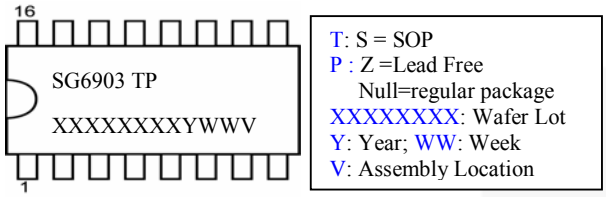
For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains constant output-power limit. Hiccup operation during output overloading is also guaranteed.

In addition, SG6903 provides complete protection functions such as brownout protection and RI pin open/short.

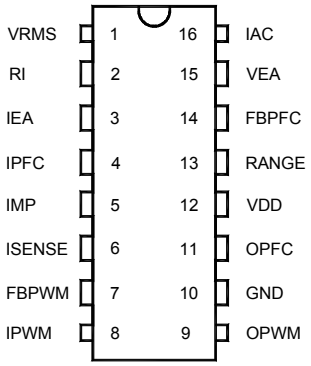
TYPICAL APPLICATION



MARKING DIAGRAMS



PIN CONFIGURATION



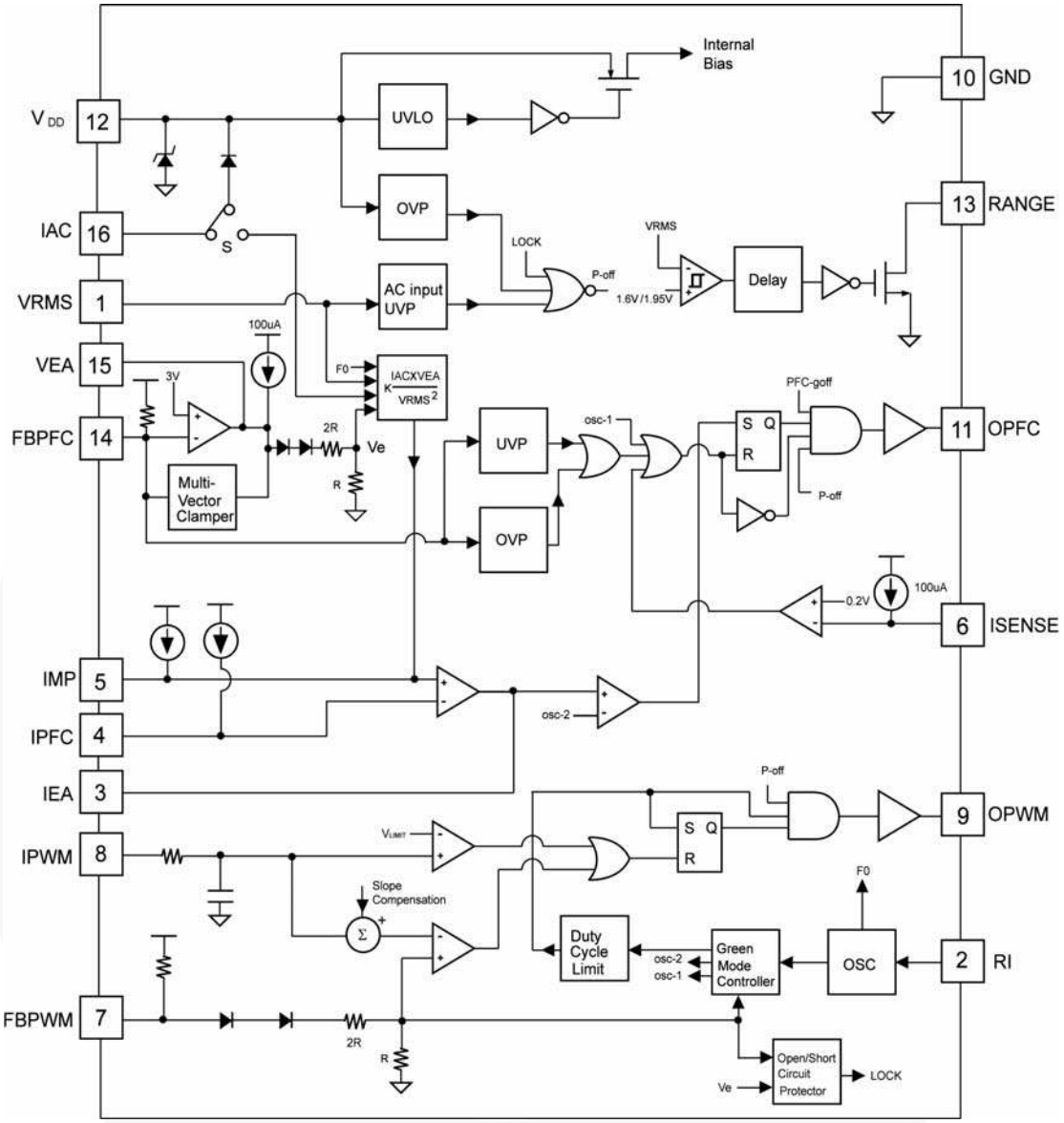
ORDERING INFORMATION

Part Number	Pb-Free	Package
SG6903SZ		16-pin SOP

PIN DESCRIPTIONS

Name	Pin No.	Type	Function
VRMS	1	Line-Voltage Detection	Line voltage detection. The pin is used for PFC multiplier, RANGE control of PFC output voltage, brownout protection. For brownout protection, the controller will be disabled after a delay time when the VRMS voltage drops below a threshold.
RI	2	Oscillator Setting	Reference setting. One resistor connected between RI and ground determines the switching frequency. The switching frequency is equal to [1560 / RI] KHz, where RI is in KΩ. For example, if RI is equal to 24KΩ, then the switching frequency will be 65 KHz.
IEA	3	Output for PFC Current Amplifier	This is the output of the PFC current amplifier. The signal from this pin will be compared with an internal saw-tooth and hence determine the pulse width for PFC gate drive.
IPFC	4	Inverting Input for PFC Current Amplifier	The inverting input of the PFC current amplifier. Proper external compensation circuits will result in excellent input power factor via average-current-mode control.
IMP	5	Non-inverting Input for PFC Current Amplifier	The non-inverting input of the PFC current amplifier and also the output of multiplier. Proper external compensation circuits will result in excellent input power factor via average-current-mode control.
ISENSE	6	Peak Current Limit Setting for PFC	The peak current setting for PFC.
FBPWM	7	PWM Feedback Input	The control input for voltage-loop feedback of PWM stage. It is internally pulled high through a 6.5 KΩ resistance. Usually an external opto-coupler from secondary feedback circuit is connected to this pin.
IPWM	8	PWM Current Sense	The current sense input for the Flyback PWM. Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle by cycle current limiting.
OPWM	9	PWM Gate Drive	The totem-pole output drive for the Flyback PWM MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
GND	10	Ground	Ground
OPFC	11	PFC Gate Drive	The totem-pole output drive for the PFC MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
VDD	12	Supply	The power supply pin.
RANGE	13	PFC Output-voltage Control	Two-level output-voltage setting for PFC. The PFC output voltage at low line can be reduced to improve efficiency. The RANGE pin has high impedance whenever the VRMS voltage is lower than a threshold.
FBPFC	14	Voltage Feedback Input for PFC	The feedback input for PFC voltage loop. The inverting input of PFC error amp. This pin is connected to the PFC output through a divider network.
VEA	15	Error-Amp Output for PFC voltage feedback loop	The error-amp output for PFC voltage feedback loop. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value will result in a narrow bandwidth and hence improve the power factor.
IAC	16	Input AC Current	Before start-up, this input is used to provide startup current for VDD. For normal operation, this input is used to provide current reference for the multiplier.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{VDD}	DC Supply Voltage*	25	V
I_{AC}	Input AC Current	2	mA
V_{High}	OPWM, OPFC, IAC	-0.3 to +25	V
V_{Low}	Others	-0.3 to +7	V
P_D	Power Dissipation At T_A < 50°C	0.8	W
T_J	Operating Junction Temperature	-40 to +125	℃
T_{STG}	Storage Temperature Range	-55 to +150	℃
$R_{\theta j\text{-}C}$	Thermal resistance (Junction to Case)	41.95	℃/W
T_L	Lead Temperature (Wave soldering or IR, 10seconds)	260	℃
$V_{ESD,HBM}$	ESD capability, HBM model	4.5	KV
$V_{ESD,MM}$	ESD capability, Machine model	250	V

*All voltage values, except differential voltages, are given with respect to GND pin.

*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
T_A	Operating Ambient Temperature*	-20 to +85	℃

*For proper operation, electrical characteristics ($12V<V_{DD}<20V$, $-20°C<T_A<85°C$ Unless noted)

VDD section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DD\text{-}OP}$	Continuously Operating Voltage				20	V
$I_{DD\text{-}ST}$	Start-up Current	$0V < V_{DD} < V_{DD\text{-}ON}$		10	25	μA
$I_{DD\text{-}OP}$	Operating Current	V_{DD} = 15V; OPFC, OPWM open; RI = 24KΩ		6	10	mA
$V_{DD\text{-}ON}$	Start Threshold Voltage		15	16	17	V
$V_{DD\text{-}OFF}$	Min. Operating Voltage		9	10	11	V
$V_{DD\text{-}OVP}$	VDD OVP Threshold		23.5	24.5	25.5	V
$t_{D\text{-}VDDOVP}$	Debounce Time of VDD OVP		8		25	μs
$V_{DD\text{-}TH\text{-}G}$	VDD Low-Threshold Voltage to Exit Green-OFF Mode		$V_{DD\text{-}OFF}$ +0.9	$V_{DD\text{-}OFF}$ +1.5	$V_{DD\text{-}OFF}$ +2.1	V

Oscillator & Green-Mode Operation

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{OSC}	PWM Frequency	RI = 24KΩ	62	65	68	KHz
$F_{OSC-MINFREQ}$	Minimum Frequency in Burst Mode	RI = 24KΩ	18	20	22	KHz
RI	RI Pin Resistance Range		15		47	KΩ
RI_{OPEN}	RI Pin Open Protection If RI> RI_{open} , SG6903 will turn off			200		KΩ
RI_{SHORT}	RI Pin Short Protection If RI< RI_{short} , SG6903 will turn off			2		KΩ

VRMS for UVP and RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{RMS-UVP-1}$	RMS AC Voltage Under Voltage Protection Threshold (with t_{UVP} delay)		0.75	0.8	0.85	V
$V_{RMS-UVP-2}$	Recovery level on VRMS		$V_{RMS-UVP-1}$+0.16V	$V_{RMS-UVP-1}$+0.18V	$V_{RMS-UVP-1}$+0.2V	V
t_{D-PWM}	When UVP Occurs ,The interval from PFC off to PWM off		$t_{UVP-Min}$+9		$t_{UVP-Min}$+14	ms
t_{UVP}	Under Voltage Protection Delay Time (No delay for startup)		150	195	240	ms
V_{RMS-H}	High V_{RMS} Threshold for RANGE Comparator		1.9	1.95	2.0	V
V_{RMS-L}	Low V_{RMS} Threshold for RANGE Comparator		1.55	1.6	1.65	V
t_{RANGE}	Range-Enable Delay Time		140	170	200	ms
V_{OL}	Output Low Voltage of RANGE Pin	I_o = 1mA			0.5	V
I_{OH}	Output High Leakage Current of RANGE Pin	RANGE = 5V			50	nA

PFC stage

Voltage Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage		2.95	3	3.05	V
Av	Open-loop Gain			60		dB
Z_o	Output Impedance			110		KΩ
OVP_{FBPFC}	PFC Over Voltage Protection		3.2	3.25	3.3	V
$\triangle OVP_{FBPFC}$	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
$t_{OVP-FBPFC}$	Debounce Time of PFC OVP		40	70	120	µs
$V_{FBPFC-H}$	Clamp-High Feedback Voltage		3.1	3.15	3.2	V
$G_{FBPFC-H}$	Clamp-High Gain			0.5		µA/mV
$V_{FBPFC-L}$	Clamp-Low Feedback Voltage		2.75	2.85	2.9	V
$G_{FBPFC-L}$	Clamp-Low Gain			6.5		mA/mV
$I_{FBPFC-L}$	Maximum Source Current		1.5	2		mA
$I_{FBPFC-H}$	Maximum Sink Current		70	110		µA
UVP_{FBPFC}	PFC Feedback Under Voltage Protection		0.35	0.4	0.45	V
$t_{UVP-FBPFC}$	Debounce Time of PFC UVP		40	70	120	µs

Current Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage ((-) > (+))			8		mV
A_I	Open-loop Gain			60		dB
BW	Unit Gain Bandwidth			1.5		MHz
CMRR	Common-mode Rejection Ratio	V_{CM} = 0 to +1.5V		70		dB
$V_{OUT-HIGH}$	Output High Voltage		3.2			V
$V_{OUT-LOW}$	Output Low Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current Source	RI = 24 KΩ (I_{MR}=20+I_{RI}*0.8)	50		70	μA
I_L	Maximum Source Current		3			mA
I_H	Maximum Sink Current			0.25		mA

Peak Current Limit

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_P	Constant Current Output	RI = 24KΩ	90	100	110	μA
V_{PK}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{SENSE} < V_{PK})	VRMS = 1.05V	0.15	0.2	0.25	V
		VRMS = 3V	0.35	0.4	0.45	V
t_{PD-PFC}	Propagation Delay				200	ns
$t_{LEB-PFC}$	Leading-Edge Blanking Time		270	350	450	ns

Multiplier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AC}	Input AC Current	Multiplier Linear Range	0		360	μA
I_{MO-max}	Maximum Multiplier Current Output;	RI = 24 KΩ		250		μA
I_{MO-1}	Multiplier Current Output (low-line, high-power)	V_{RMS} = 1.05V; I_{AC} = 90μA; VEA = 7.5V;RI = 24 kΩ	200	250	280	μA
I_{MO-2}	Multiplier Current Output (high-line, high-power)	V_{RMS} = 3V; I_{AC} = 264μA; V_{EA} = 7.5V;RI = 24 kΩ	65	85		μA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V

PFC Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_Z	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
V_{OL-PFC}	Output Voltage Low	V_{DD}=15V; I_O = 100mA			1.5	V
t_{PFC}	The interval of OPFC lags behind OPWM at startup		4.5	5.75	7	ms
V_{OH-PFC}	Output Voltage High	V_{DD}=13V; I_O = 100mA	8			V
t_{R-PFC}	Rising Time	V_{DD}=15V; C_L=5nF ;O/P= 2V to 9V	40	70	120	ns
t_{F-PFC}	Falling Time	V_{DD}=15V;C_L=5nF ;O/P= 9V to 2V	40	60	110	ns
DCY_{MAX}	Maximum Duty Cycle		93		98	%

PWM Stage

FBPWM

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$A_{V\text{-}PWM}$	FB to Current Comparator Attenuation		2.5	3.1	3.5	V/V
Z_{FB}	Input Impedance		4	5	7	KΩ
I_{FB}	Maximum Source Current		0.8	1.2	1.5	mA
$FB_{OPEN\text{-}LOOP}$	PWM Open Loop Protection voltage		4.2	4.5	4.8	V
$t_{OPEN\text{-}PWM}$	PWM Open Loop Protection Delay Time		45	56	70	ms
$V_{PFC\text{-}OFF\ 1}$	PFC off Voltage at FBPWM	RANGE = Ground		V_G+0.2 V		V
$V_{PFC\text{-}OFF\ 2}$	PFC off Voltage at FBPWM	RANGE = Open		V_G+0.2 V		V
$t_{PFC\text{-}OFF}$	PFC Off Propagation Delay Time		450	600	750	ms
$V_{PFC\text{-}ON\ 1.6}$	PFC on Voltage at FBPWM	RANGE = Ground; VRMS =1.6V		V_G+0.35V		V
$V_{PFC\text{-}ON\ 2.85}$	PFC on Voltage at FBPWM	RANGE = Ground; VRMS =2.85V		V_G+0.35V		V
$V_{PFC\text{-}ON\ 0.8}$	PFC on Voltage at FBPWM	RANGE = Open; VRMS =0.8V		V_G+0.85V		V
$V_{PFC\text{-}ON\ 1.95}$	PFC on Voltage at FBPWM	RANGE = Open; VRMS =1.95V		V_G+0.5 V		V
V_N	Frequency Reduction Threshold on FBPWM	RANGE = Ground	1.9	2.1	2.3	V
S_G	Green-Mode Modulation Slope		60	75	90	Hz/V
V_G	Voltage on FBPWM at Fs = 20KHz		1.35	1.6	1.75	V

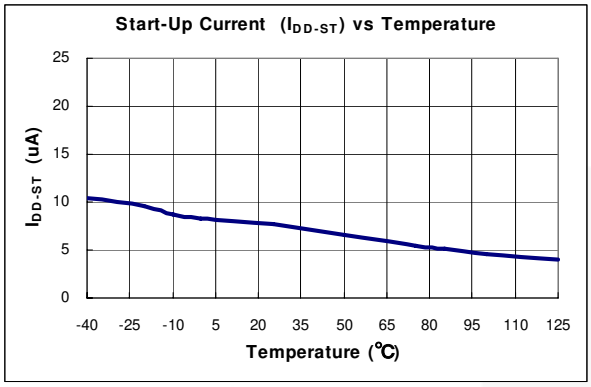
PWM-Current Sense

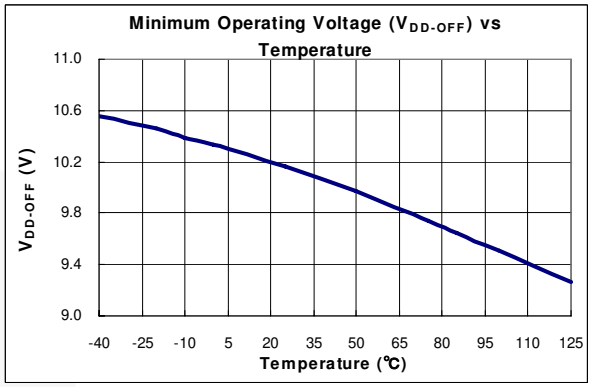
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{PD\text{-}PWM}$	Propagation Delay to Output	VDD = 15V,OPWM <= 9V	60		120	ns
$V_{LIMIT\text{-}1}$	Peak Current Limit Threshold Voltage1	RANGE = Open	0.65	0.7	0.75	V
$V_{LIMIT\text{-}2}$	Peak Current Limit Threshold Voltage2	RANGE = Ground	0.6	0.65	0.7	V
$t_{LEB\text{-}PWM}$	Leading-Edge Blanking Time		270	350	450	ns
$\triangle V_{SLOPE}$	Slope Compensation $\triangle V_S = \triangle V_{SLOPE} \times (T_{on}/T)$ $\triangle V_S$: Compensation Voltage Added to Current Sense		0.45	0.5	0.55	V

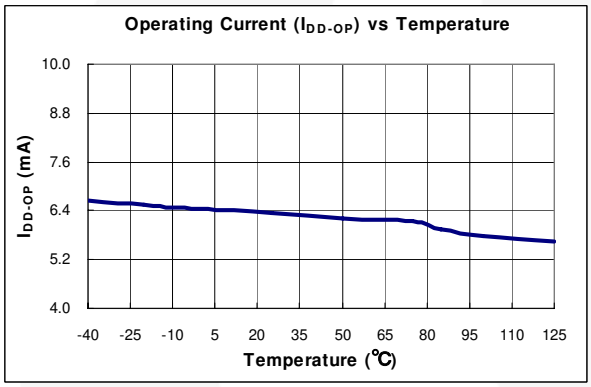
PWM Output Driver

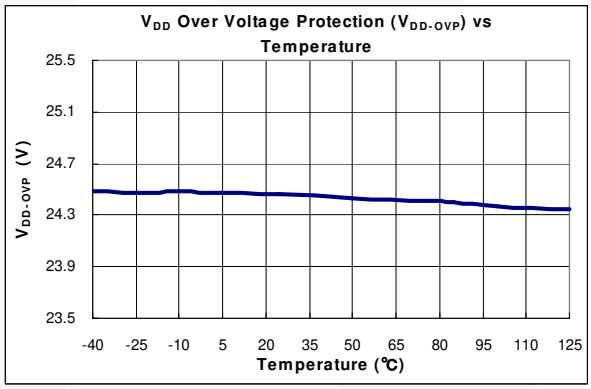
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{Z\text{-}PWM}$	Output Voltage Maximum (Clamp)	V_{DD} = 20V		16	18	V
$V_{OL\text{-}PWM}$	Output Voltage Low	V_{DD} = 15V; I_O = 100mA			1.5	V
$V_{OH\text{-}PWM}$	Output Voltage High	V_{DD} = 13V; I_O = 100mA	8			V
$t_{R\text{-}PWM}$	Rising Time	V_{DD} = 15V; C_L = 5nF; O/P= 2V to 9V	30	60	120	ns
$t_{F\text{-}PWM}$	Falling Time	V_{DD} = 15V; C_L = 5nF; O/P= 9V to 2V	30	50	110	ns
DCY_{MAXPWM}	Maximum Duty Cycle		73	78	83	%

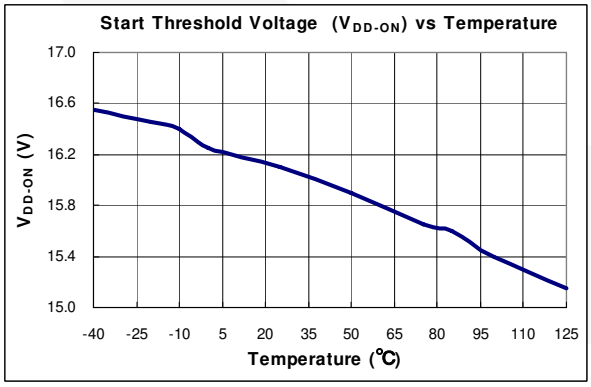
TYPICAL CHARACTERISTICS

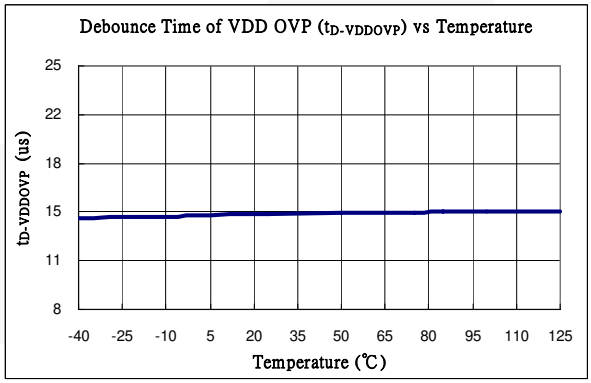


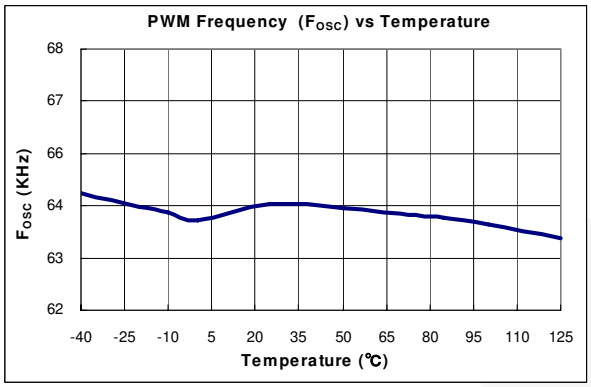


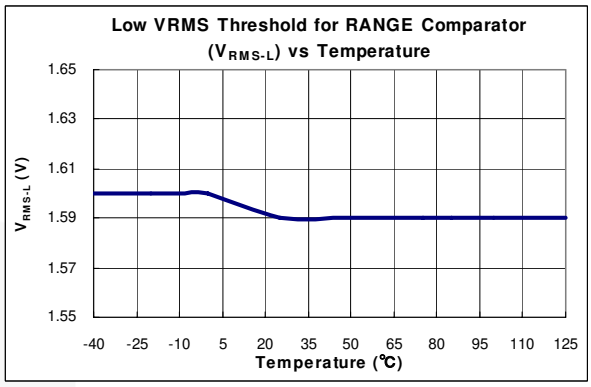


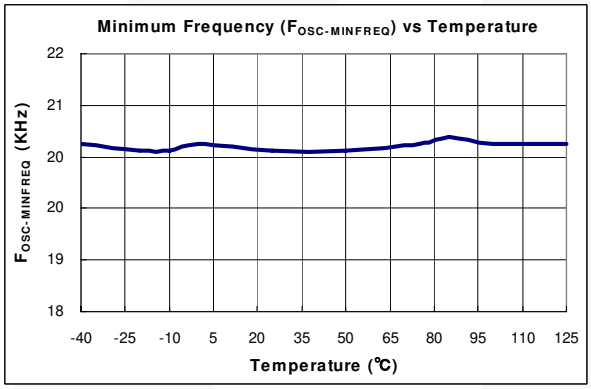


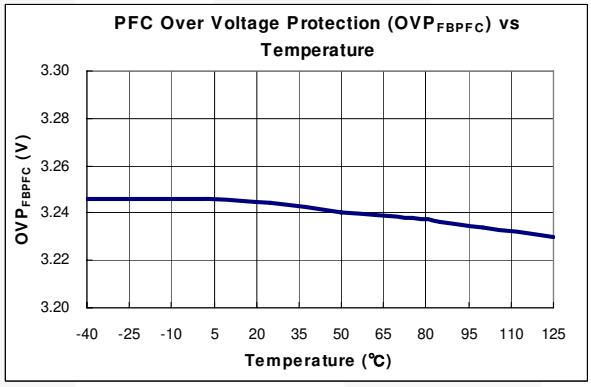


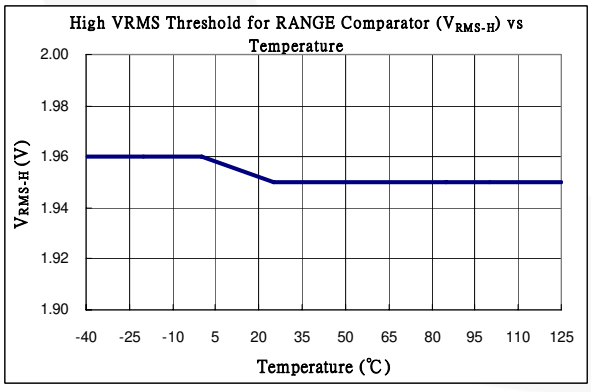


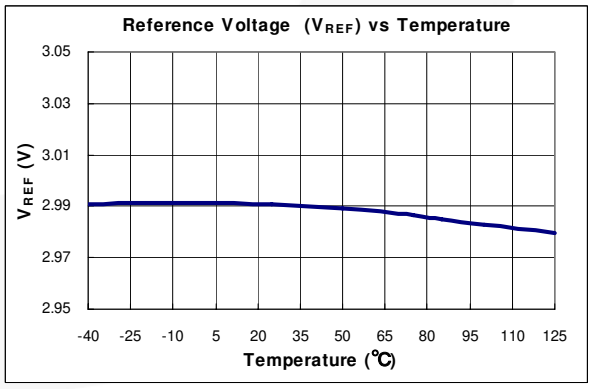

PWM Frequency (F_{OSC}) vs Temperature
F_{OSC} (KHz)
68
67
66
64
63
62
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

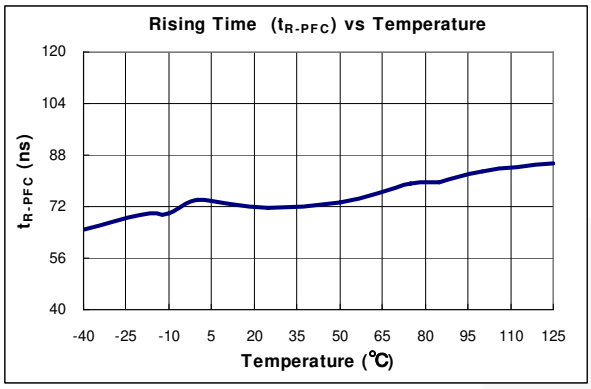

Low VRMS Threshold for RANGE Comparator (V_{RMS-L}) vs Temperature
V_{RMS-L} (V)
1.65
1.63
1.61
1.59
1.57
1.55
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

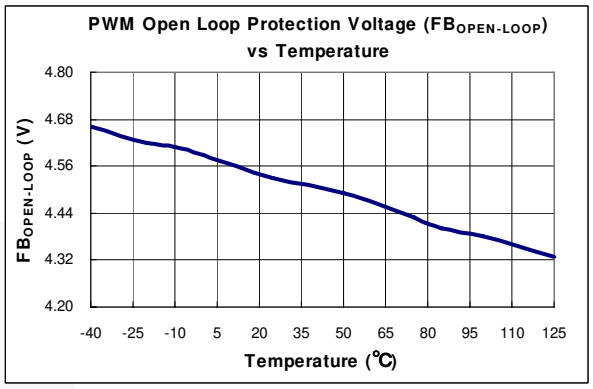

Minimum Frequency ($F_{OSC-MINFREQ}$) vs Temperature
$F_{OSC-MINFREQ}$ (KHz)
22
21
20
20
19
18
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

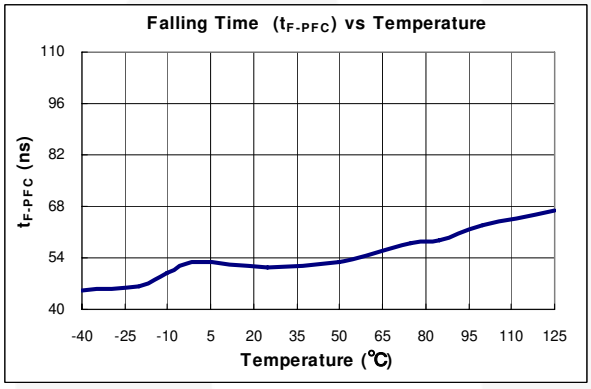

PFC Over Voltage Protection (OVP_{FBPFC}) vs Temperature
OVP_{FBPFC} (V)
3.30
3.28
3.26
3.24
3.22
3.20
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

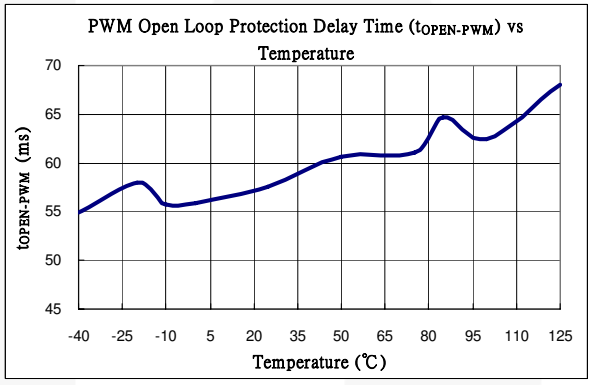

High VRMS Threshold for RANGE Comparator (V_{RMS-H}) vs Temperature
V_{RMS-H} (V)
2.00
1.98
1.96
1.94
1.92
1.90
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

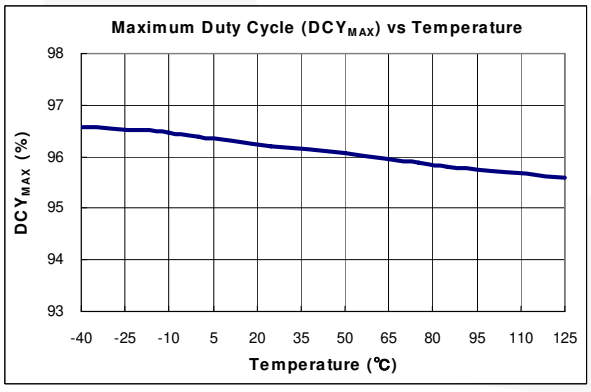

Reference Voltage (V_{REF}) vs Temperature
V_{REF} (V)
3.05
3.03
3.01
2.99
2.97
2.95
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

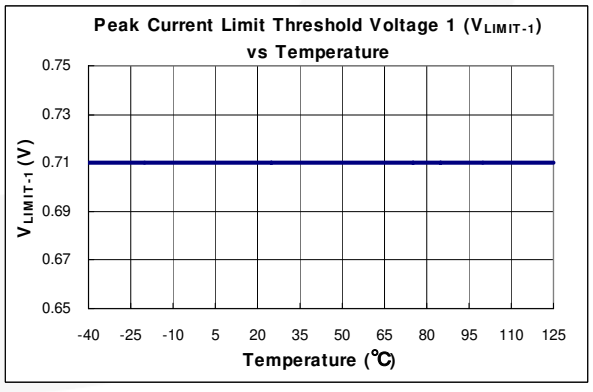

Rising Time (t_{R-PFC}) vs Temperature
t_{R-PFC} (ns)
120
104
88
72
56
40
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

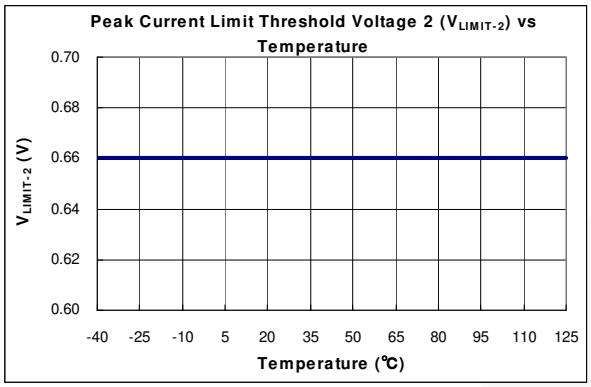

PWM Open Loop Protection Voltage ($FB_{OPEN-LOOP}$) vs Temperature
$FB_{OPEN-LOOP}$ (V)
4.80
4.68
4.56
4.44
4.32
4.20
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

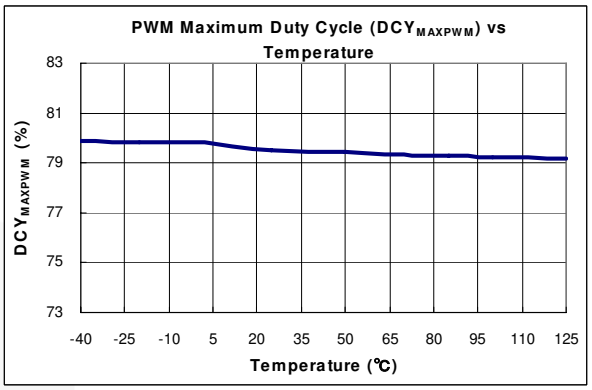

Falling Time (t_{F-PFC}) vs Temperature
t_{F-PFC} (ns)
110
96
82
68
54
40
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

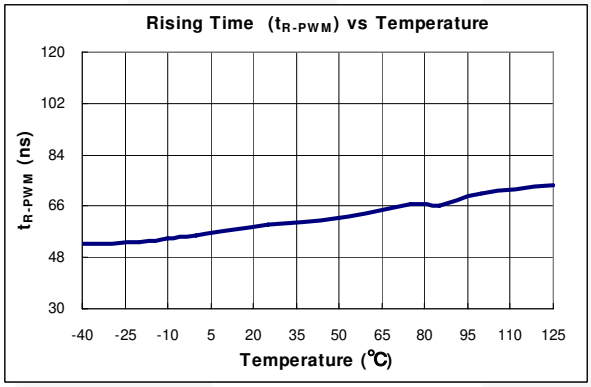

PWM Open Loop Protection Delay Time ($t_{OPEN-PWM}$) vs Temperature
$t_{OPEN-PWM}$ (ms)
70
65
60
55
50
45
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

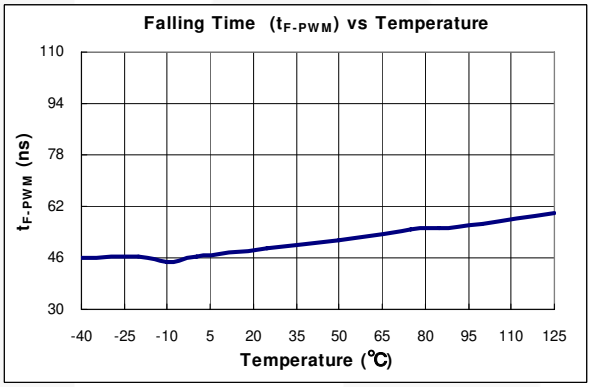

Maximum Duty Cycle (DCY_{MAX}) vs Temperature
DCY_{MAX} (%)
98
97
96
95
94
93
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Peak Current Limit Threshold Voltage 1 ($V_{LIMIT-1}$) vs Temperature
$V_{LIMIT-1}$ (V)
0.75
0.73
0.71
0.69
0.67
0.65
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Peak Current Limit Threshold Voltage 2 ($V_{LIMIT-2}$) vs Temperature
$V_{LIMIT-2}$ (V)
0.70
0.68
0.66
0.64
0.62
0.60
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


PWM Maximum Duty Cycle (DCY_{MAXPWM}) vs Temperature
DCY_{MAXPWM} (%)
83
81
79
77
75
73
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Rising Time (t_{R-PWM}) vs Temperature
t_{R-PWM} (ns)
120
102
84
66
48
30
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Falling Time (t_{F-PWM}) vs Temperature
t_{F-PWM} (ns)
110
94
78
62
46
30
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

OPERATION DESCRIPTION

SG6903 is a highly integrated PFC/PWM combo controller. Lots functions and protections are built in to provide a possible compact design. The following description will describe the operation and function in detail to give an overview of this chip.

Start-up

Figure 1 shows the start-up circuit of the SG6903. A resistor R_{AC} is utilized to charge V_{DD} capacitor through S1. The turn-on and turn-off threshold of SG6903 are fixed internally at 16V/10V. During start-up, the hold-up capacitor must be charged to 16V through the start-up resistor so that SG6903 will be enabled. The hold-up capacitor will continue to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 10V during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during start-up. Since SG6903 consumes less than 25μA startup current, the value of R_{AC} can be large to reduce power consumption. One 10μF capacitor should hold enough energy for successful start-up. After start-up, S1 will switch so that the current I_{AC} will be the input for PFC multiplier. This helps reduce circuit complexity and power consumption.

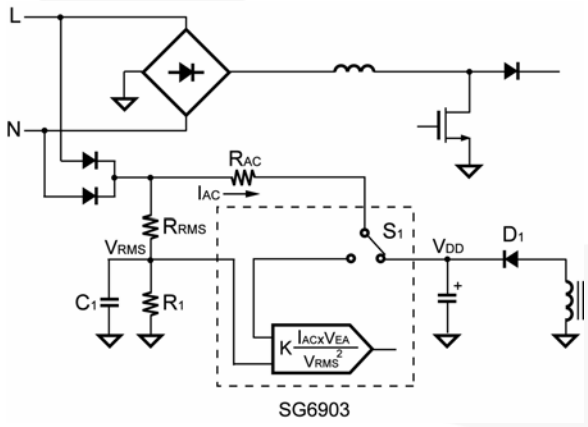


FIG.1 Start-up circuit of the SG6903

Switching Frequency and Current Sources

The switching frequency of SG6903 can be programmed by the resistor R_I connected between RI pin and GND. The relationship is:

$$F_{OSC} = \frac{1560}{R_I\ (k\Omega)}(KHz) \text{ ---------- (1)}$$

For example, a 24KΩ resistor R_I results in a 65 KHz switching frequency. Accordingly, a constant Current I_T will flow through R_I.

$$I_T = \frac{1.2V}{R_I\ (k\Omega)}(mA) \text{ ---------- (2)}$$

I_T is used to generate internal current reference.

Line Voltage Detection (VRMS)

Figure 2 shows a resistive divider with low-pass filtering for line-voltage detection on VRMS pin. The V_{RMS} voltage is used for the PFC multiplier, brownout protection, and range control.

For brownout protection, the SG6903 is disabled with 195ms delay time if the voltage V_{RMS} drops below 0.8V.

For PFC multiplier and range control, please refer to below section for more details.

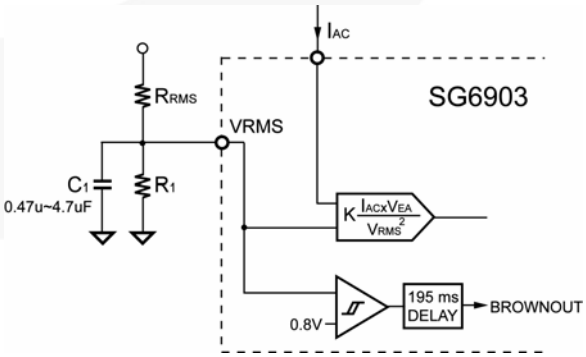


FIG.2 Line voltage detection circuit

PFC Output Voltage Control (RANGE)

For a universal input (90 ~ 264Vac) power supply applying active boost PFC and Flyback as a second stage, the output voltage of PFC is usually designed around 250V at low line while it is 390V at high line. This can improve the efficiency at low-line input. In SG6903, the RANGE pin (open-drain structure) is used for the two-level output voltage setting.

Figure 3 shows the RANGE output that programs the PFC output voltage. The RANGE output is shorted to ground when the V_{RMS} voltage exceeds V_{RMS-H} (1.95V) while it is of high impedance (open) whenever the V_{RMS} voltage drops below V_{RMS-L} (1.6V). The output voltages can be designed using below equations.

$$\text{Range} = \text{Open} \Rightarrow V_O = \frac{R_A + R_B}{R_B} \times 3V$$
$$\text{Range} = \text{Ground} \Rightarrow V_O = \frac{R_A + (R_B // R_C)}{(R_B // R_C)} \times 3V \quad \text{---- (3)}$$

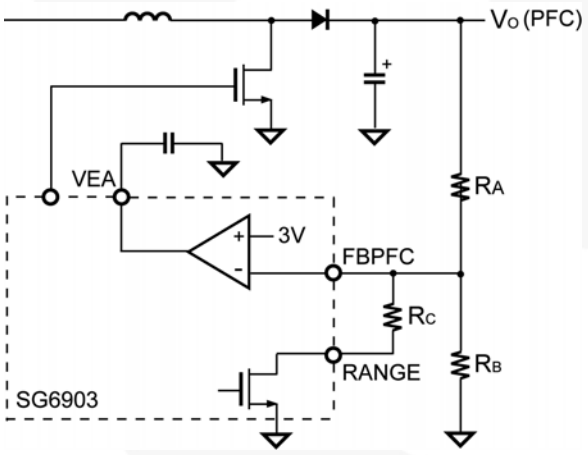


FIG.3 Range control two level output voltage

Interleave Switching

The SG6903 uses interleaved switching to synchronize the PFC and Flyback stages. This reduces switching noise and spreads the EMI emissions. Figure 4 shows that an off-time T_{OFF} is inserted in between the turn-off of the PFC gate drive and the turn-on of the PWM.

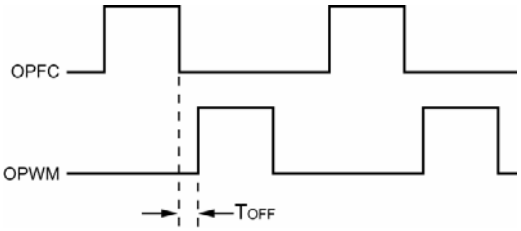


FIG.4 Interleaved switching pattern

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase will follow that of the input voltage. Using SG6903, average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and *Switching Charge*® multiplier/divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 5 shows the total control loop for the average-current-mode control circuit of SG6903.

The current source output from the *Switching Charge*® multiplier/divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (uA) \quad \text{---------- (4)}$$

Refer to Figure 5, the current output from IMP pin, I_{MP}, is the summation of I_{MO} and I_{MR1}. I_{MR1} and I_{MR2} are identical fixed current sources. They are used to pull high the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground. The constant current sources I_{MR1} and I_{MR2} are typically 60μA.

Through the differential amplification of the signal across Rs, better noise immunity is achieved. The output of IEA will be compared with an internal sawtooth and hence the pulse width for PFC is determined. Through the average current-mode control loop, the input current Is will be proportional to I_{MO}.

$$I_{MO} \times R_2 = I_S \times R_S \quad \text{---------- (5)}$$

According to Equation (5), the minimum value of R2 and maximum of Rs can be determined since I_{MO} should not exceed the specified maximum value.

There are different concerns in determining the value of the sense resistor Rs. The value of Rs should be small to reduce power consumption, but it should be large enough to maintain the resolution. A current transformer (CT) may be used to improve the efficiency of high power converters.

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as constant as possible according to Equation (4). In other words, good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The trans-conductance error amplifier has output impedance Z_O and a capacitor C_{EA} (1μF ~ 10μF) should be connected to ground. This establishes a dominant pole f1 (Equation (6)) for the voltage loop.

$$f_1 = \frac{1}{2\pi \times Z_O \times C_{EA}} \quad \text{---------- (6)}$$

The average total input power can be expressed as:

$$\begin{aligned} Pin &= Vin(rms) \times Iin(rms) \\ &\propto V_{RMS} \times I_{MO} \\ &\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} \quad \text{---------- (7)} \\ &\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^2} \\ &= \sqrt{2} \times \frac{V_{EA}}{R_{AC}} \end{aligned}$$

From Equation (7), V_{EA}, the output of the voltage error amplifier, actually controls the total input power and hence the power delivered to the load.

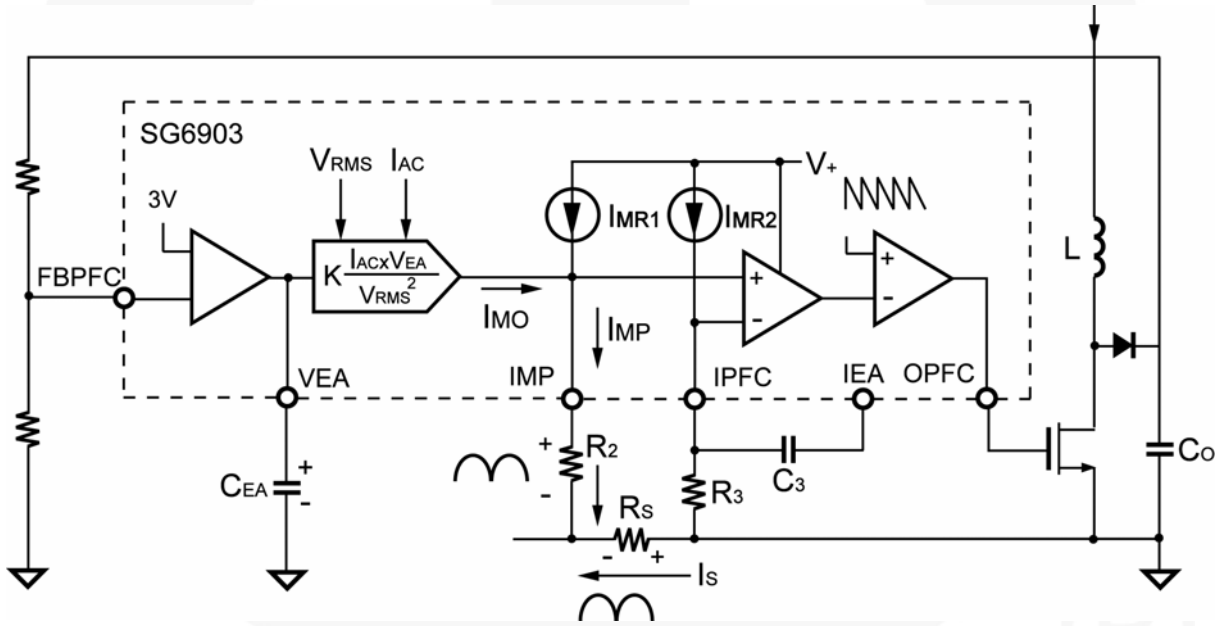


FIG.5 Average current mode control loop

Multi-vector Error Amplifier

Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative *Multi-Vector Error Amplifier* provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 6 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ± 5% of the reference voltage, the trans-conductance error amplifier will adjust its output impedance to increase the loop response.

Once the voltage on the FBPFC pin is over OVP_{FBPFC}, the OPFC of the SG6903 will be disabled. THE OPFC will not be enabled again until the FBPFC voltage falls below OVP_{FBPFC}.

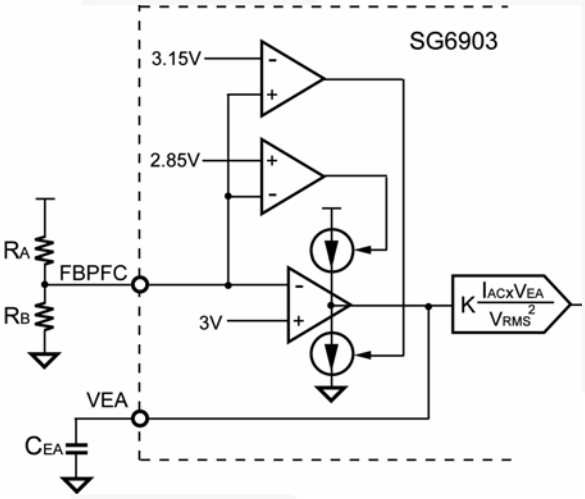


FIG. 6 Multi-vector error amplifier

Cycle-by-cycle Current Limiting

SG6903 provides cycle-by-cycle current limiting for both PFC and PWM stages. The voltage of V_{RMS} determines the voltage of V_{PK}. The relationship between V_{PK} and VRMS is also shown in Figure 7. The PFC gate drive will be terminated once the voltage on ISENSE pin goes below V_{PK}.

The amplitude of the constant current I_P is determined by the internal current reference according to the following equation:

$$I_P = 2 \times \frac{1.2V}{R_I} \quad \text{---------- (8)}$$

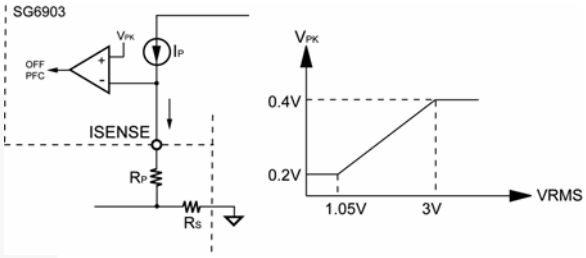


FIG. 7 VRMS controlled current limiting

Therefore the peak current of the I_{SENSE} is given by (V_{RMS}<1.05V),

$$I_{SENSE\_peak} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad \text{---------- (9)}$$

Flyback PWM and Slope Compensation

As shown in Figure 8, peak-current-mode control is utilized for Flyback PWM. The SG6903 inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation ensures stable operation for continuous current-mode operation.

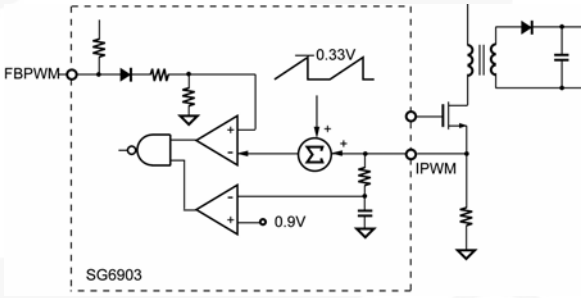


FIG. 8 Peak current control loop

When the IPWM voltage, across the sense resistor, reaches the threshold voltage (0.9V), the OPWM will be turned off after a small propagation delay t_{PD-PWM}.

To improve stability or prevent sub-harmonic oscillation, a synchronized positive-going ramp in inserted at every switching cycle.

Limited Power Control

Every time when the output of power supply is shorted or over loaded, the FBPWM voltage will increase. If the FBPWM voltage is higher than a designed threshold, $FB_{OPEN-LOOP}$ (4.5V), for longer than $t_{OPEN-PWM}$ (56ms), the OPWM will then be turned off.

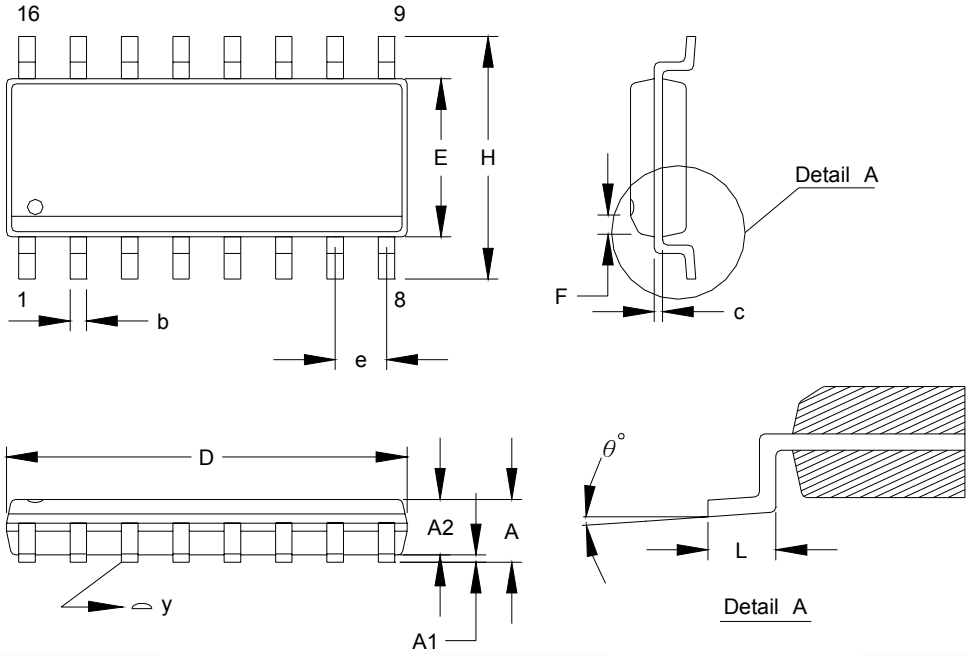
As long as the voltage on the VDD pin is larger than V_{DD-OFF} (minimum operating voltage), the OPWM will not be enabled. And this protection will be reset every $t_{OPEN-PWM-Hiccup}$ interval. A low frequency hiccup mode protection will then be achieved to prevent the power supply from being overheated under over loading condition.

Gate Drivers

SG6903 output stage is a fast totem-pole gate driver. The output driver is clamped by an internal 18V Zener diode in order to protect the external power MOSFET.

PACKAGE INFORMATION

16 PINS – PLASTIC SOP (S)



DIMENSION:

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.753	0.053		0.069
A1	0.101		0.254	0.004		0.010
A2	1.244		1.499	0.049		0.059
b		0.406			0.016	
c		0.203			0.008	
D	9.804		10.008	0.386		0.394
E	3.810		3.988	0.150		0.157
e		1.270			0.050	
H	5.791		6.198	0.228		0.244
L	0.406		1.270	0.016		0.050
F		0.381X45°			0.015X45°	
y			0.101			0.004
θ°	0°		8°	0°		8°

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i-Lo™
IntelliMAX™
ISOPLANAR™
MegaBuck™
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MicroPak™
MillerDrive™
Motion-SPM™
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PDP-SPM™
Power220®
Power247®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
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TinyPower™
TinyPWM™
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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