



# FOCUS LCDs

LCDs MADE SIMPLE®

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TFT | OLED | GRAPHIC | CHARACTER | UWVD | SEGMENT | CUSTOM

## Graphic OLED Module

Part Number

O12864A-GBY-TW3

### Overview:

- 128x64 Graphic OLED
- Light Blue & Yellow Pixel Color
- Overall Size: 26.70mm x 19.26mm
- Parallel Interface
- -40C to 70C Operating Temperature
- 2.8V
- Controller: SSD1306
- RoHS Compliant

**Graphic OLED Features:**

Resolution: 128 x 64

Interface: Parallel

Controller: SSD1306

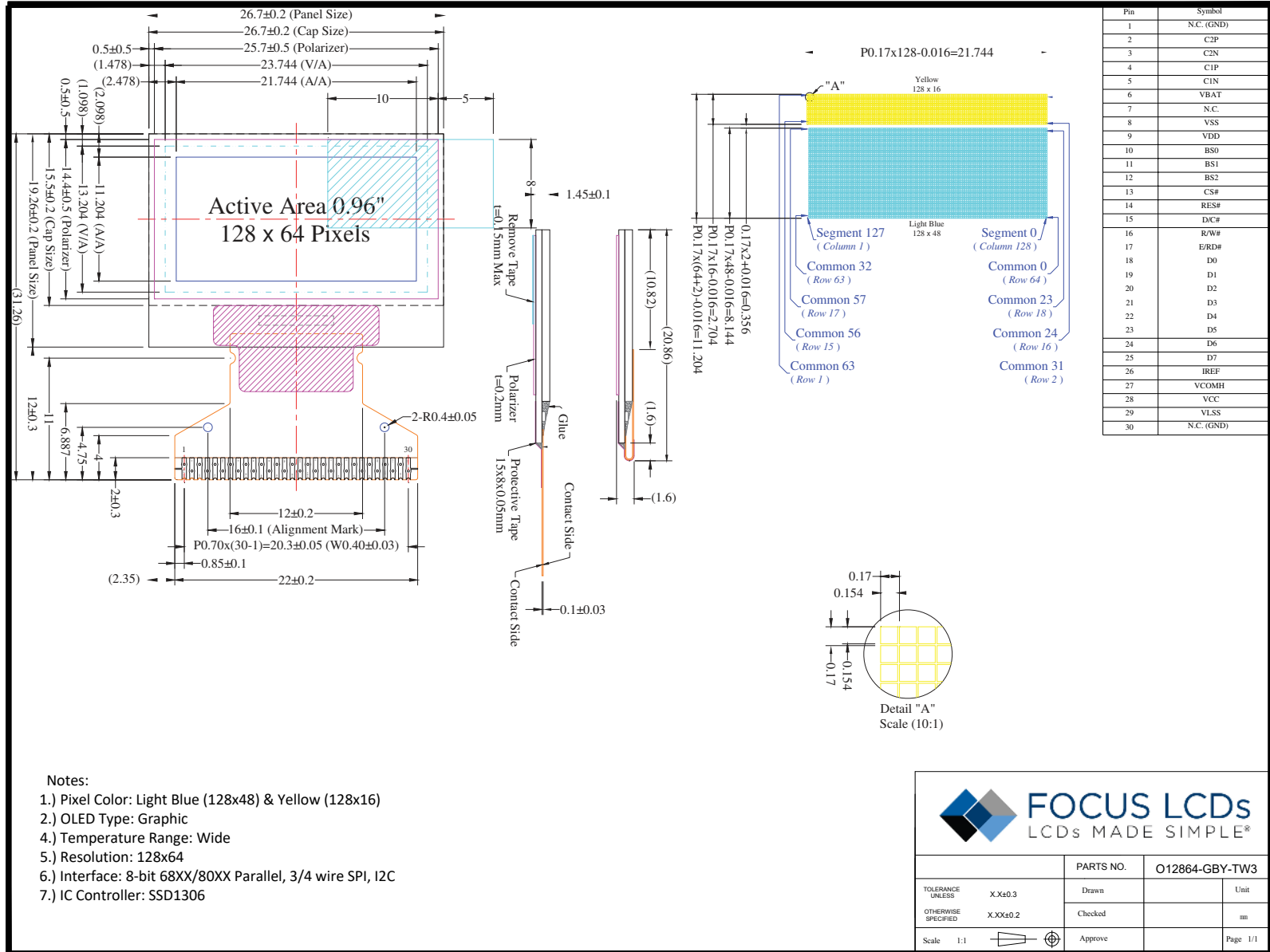
RoHS Compliant

General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area	23.744 x 13.204	mm	-
Pixel Color	Light Blue & Yellow	-	-
Viewing Direction	Full	-	-
Voltage	2.8	V	-
Resolution	128x64	-	-
Controller IC	SSD1306	-	-
Interface	Parallel	-	-
Operating temperature	-40~+70	°C	-
Storage temperature	-40~+85	°C	-


**Mechanical Information**

Item		Min	Typ.	Max	Unit	Note
Module size	X (Width)	-	26.70	-	mm	-
	Y (Height)	-	19.26	-	mm	-
	Z (Depth)	-	-	1.45	mm	-


# 1. Outline Dimensions



- Notes:
- 1.) Pixel Color: Light Blue (128x48) & Yellow (128x16)
  - 2.) OLED Type: Graphic
  - 4.) Temperature Range: Wide
  - 5.) Resolution: 128x64
  - 6.) Interface: 8-bit 68XX/80XX Parallel, 3/4 wire SPI, I2C
  - 7.) IC Controller: SSD1306



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		PARTS NO.	O12864-GBY-TW3
TOLERANCE UNLESS OTHERWISE SPECIFIED	X.X±0.3	Drawn	Unit
OTHERWISE SPECIFIED	X.XX±0.2	Checked	mm
Scale 1:1		Approve	Page 1/1

## 2. Input Terminal Pin Assignment

NO.	Symbol	Description	I/O
1	N.C.	No Connection / Reserved Pin	-
2	C2P	Positive Terminal of the Flying Inverting Capacitor	I
3	C2N	Negative Terminal of the Flying Boost Capacitor	I
4	C1P	Positive Terminal of the Flying Inverting Capacitor	I
5	C1N	Negative Terminal of the Flying Boost Capacitor	I
6	Vddb	Power Supply for DC/DC Converter Circuit	P
7	N.C.	Reserved Pin	-
8	VSS	Ground of Logic Circuit	P
9	VDD	Power Supply for Logic	P
10	BS0	BS0	I
		I <sup>2</sup> C	
11	BS1	3-Wire SPI	I
		4-Wire SPI	
12	BS2	8-bit 68xx Parallel	I
		8-bit 80xx Parallel	
13	CS#	Chip Select	O
14	RES#	Power Reset for Controller and Driver	P
15	D/C#	Data/Command Control	I
16	R/W#	Read/Write Select or Write	I
17	E/RD#	Read/Write Enable or Read	I
18-25	D0-D7	Host Data Input/Output Bus	I
26	IREF	Current Reference for Brightness Adjustment	I
27	VCOMH	Voltage Output High Level for COM Signal	O
28	VCC	Power Supply for OEL Panel	P
29	VLSS	Ground of Analog Circuit	P
30	N.C.	No Connection / Reserved Pin	-

I: Input, O: Output, P: Power

### 3. Optical Characteristics

Characteristic	Symbol	Condition	Min	Typ.	Max	Unit
Brightness (V <sub>CC</sub> Supplied Externally)	L <sub>br</sub>	V <sub>DD</sub> = 2.8V V <sub>CC</sub> = 9V	100	120	-	cd/m <sup>2</sup>
Brightness (V <sub>CC</sub> Generated by Internal DC/DC)	L <sub>br</sub>	V <sub>DD</sub> = 2.8V V <sub>CC</sub> = 7.25V	80	100	-	cd/m <sup>2</sup>
CIE (Light Blue)	X Y	-	0.12 0.22	0.16 0.26	0.20 0.30	-
CIE (Yellow)	X Y	-	0.46 0.45	0.50 0.49	0.54 0.53	-
Dark Room Contrast	-	-	-	>10000:1	-	-
Viewing Angle	-	-	-	Full	-	degrees

### 4. DC Electrical Characteristics

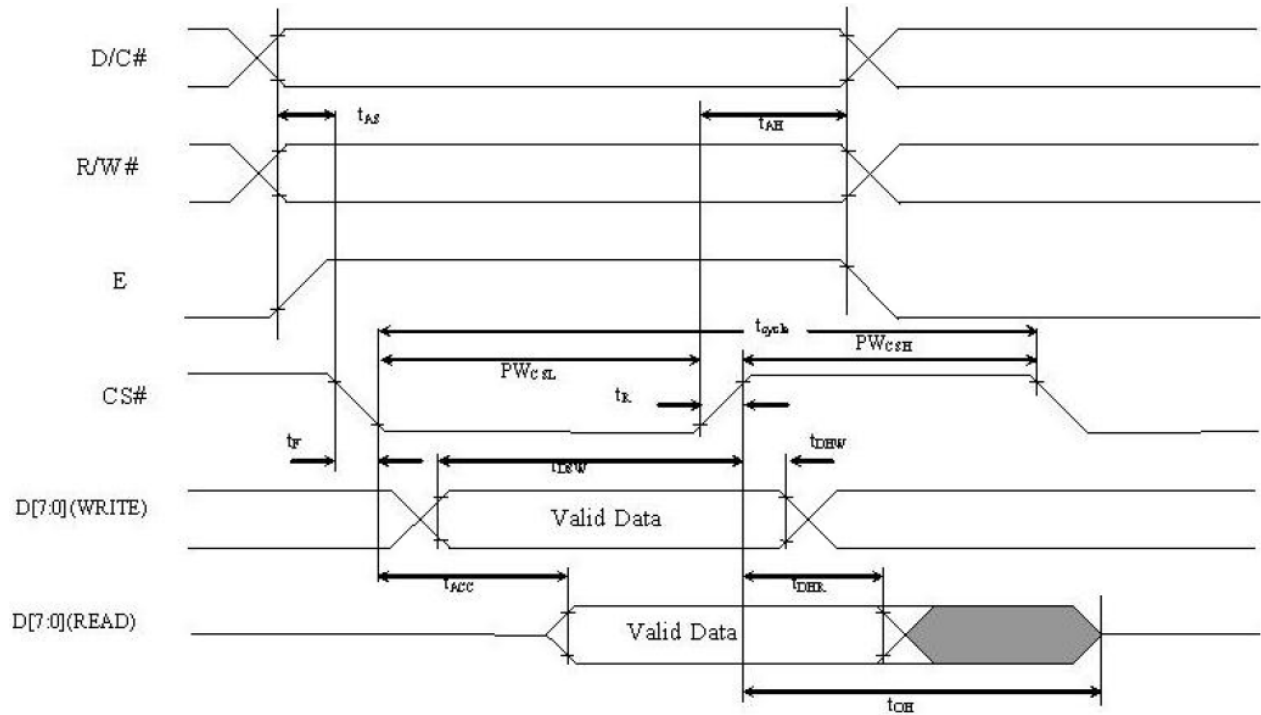
Characteristics	Symbol	Conditions	Min	Typ.	Max	Unit
Supply Voltage for Logic	V <sub>DD</sub>	-	1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V <sub>CC</sub>	Internal DC/DC Disable	8.5	9.0	9.5	V
Supply Voltage for DC/DC	V <sub>DDB</sub>	Internal DC/DC Enable	3.5	-	4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	V <sub>CC</sub>	Internal DC/DC Enable	7.0	-	7.5	V
High Level Input	V <sub>IH</sub>	I <sub>out</sub> =100μA, 3.3 MHz	0.8V <sub>DD</sub>	-	V <sub>DD</sub>	V
Low Level Input	V <sub>IL</sub>	I <sub>out</sub> =100μA, 3.3 MHz	0	-	0.2V <sub>DD</sub>	V
High Level Output	V <sub>OH</sub>	I <sub>out</sub> =100μA, 3.3 MHz	0.9V <sub>DD</sub>	-	V <sub>DD</sub>	V
Low Level Output	V <sub>OL</sub>	I <sub>out</sub> =100μA, 3.3 MHz	0	-	0.1V <sub>DD</sub>	V
Operating Current for V <sub>DD</sub>	I <sub>DD</sub>	-	-	180	300	μA
Operating Current for V <sub>CC</sub> (V <sub>CC</sub> Supplied Externally)	I <sub>CC</sub>	-	-	12.3	15.4	mA
Operating Current for V <sub>DDB</sub> (V <sub>CC</sub> Generated by Internal DC/DC)	I <sub>DDB</sub>	-	-	25.6	32.0	mA
Sleep Mode Current for V <sub>DD</sub>	I <sub>DD, SLEEP</sub>	-	-	1	5	μA
Sleep Mode Current for V <sub>CC</sub>	I <sub>CC, SLEEP</sub>	-	-	2	10	μA

*NOTE: If the maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. The maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the specified parameters.*

## 5. Timing Characteristics

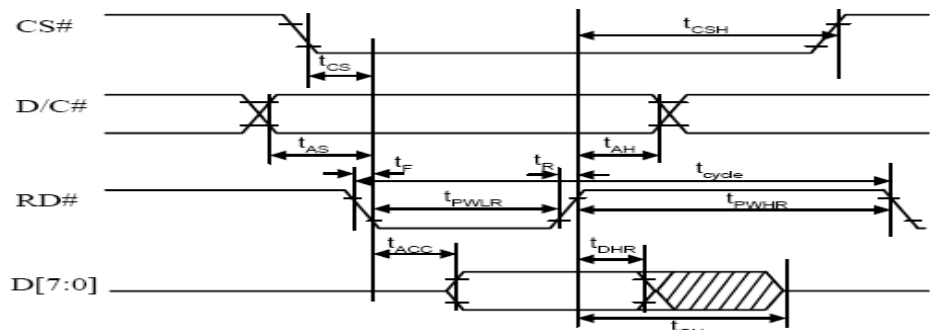
### 5.1 68XX-Series MPU Parallel Interface Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Clock Cycle Time	$t_{cyc}$	300	-	ns
Address Setup Time	$t_{AS}$	5	-	ns
Address Hold Time	$t_{AH}$	0	-	ns
Write Data Setup Time	$t_{DSW}$	40	-	ns
Write Data Hold Time	$t_{DHW}$	7	-	ns
Read Data Hold Time	$t_{DHR}$	20	-	ns
Output Disable Time	$t_{OH}$	-	70	ns
Access Time	$t_{ACC}$	-	140	ns
Chip Select Low Pulse Width (Read)	$PW_{CSL}$	120	-	ns
Chip Select Low Pulse Width (Write)		60		ns
Chip Select High Pulse Width (Read)	$PW_{CSH}$	60	-	ns
Chip Select High Pulse Width (Write)		60		ns
Rise Time	$t_r$	-	40	ns
Fall Time	$t_f$	-	40	ns

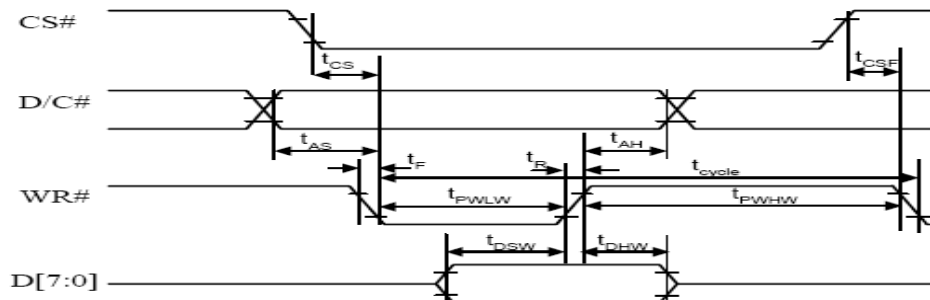


## 5.2 80XX-Series MPU Parallel Interface Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Clock Cycle Time	$t_{cycle}$	300	-	ns
Address Setup Time	$t_{AS}$	10	-	ns
Address Hold Time	$t_{AH}$	0	-	ns
Write Data Setup Time	$t_{DSW}$	40	-	ns
Write Data Hold Time	$t_{DHW}$	7	-	ns
Read Data Hold Time	$t_{DHR}$	20	-	ns
Output Disable Time	$t_{OH}$	-	70	ns
Access Time	$t_{ACC}$	-	140	ns
Read Low Time	$t_{PWLR}$	120	-	ns
Write Low Time	$t_{PWLW}$	60	-	ns
Read High Time	$t_{PWHR}$	60	-	ns
Write High Time	$t_{PWHW}$	60	-	ns
Chip Select Setup Time	$t_{CS}$	0	-	ns
Chip Select Hold Time to Read Signal	$t_{CSH}$	0	-	ns
Chip Select Hold Time	$t_{CSF}$	20	-	ns
Rise Time	$t_r$	-	40	ns
Fall Time	$t_f$	-	40	ns



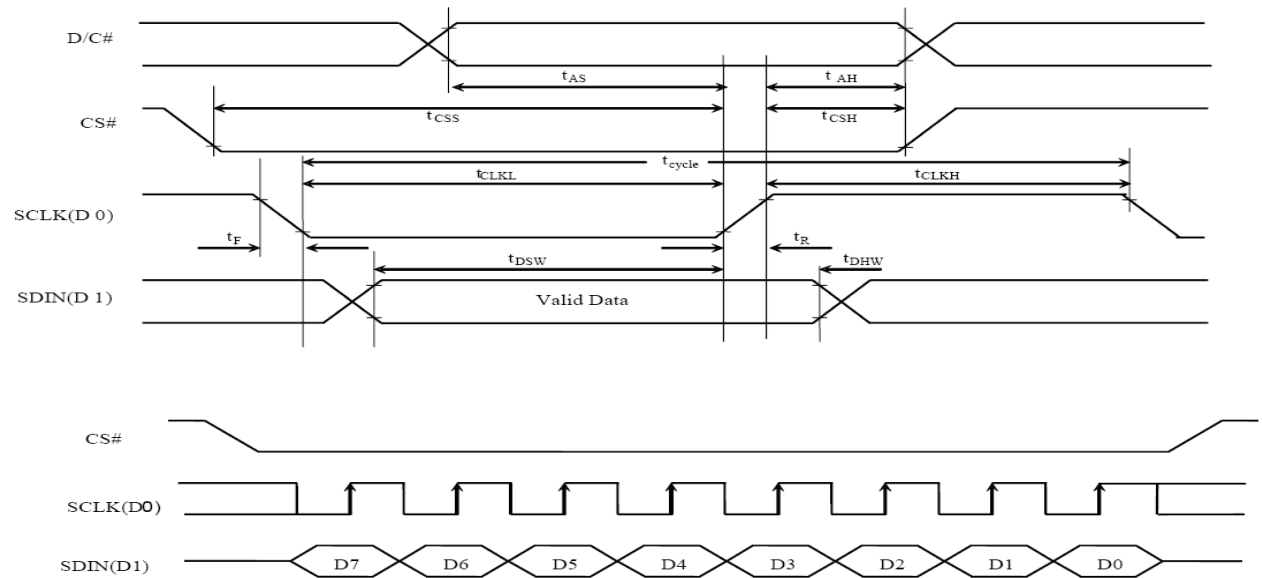
( Read Timing )



( Write Timing )

### 5.3 Serial Interface Timing Characteristics (4 wire SPI)

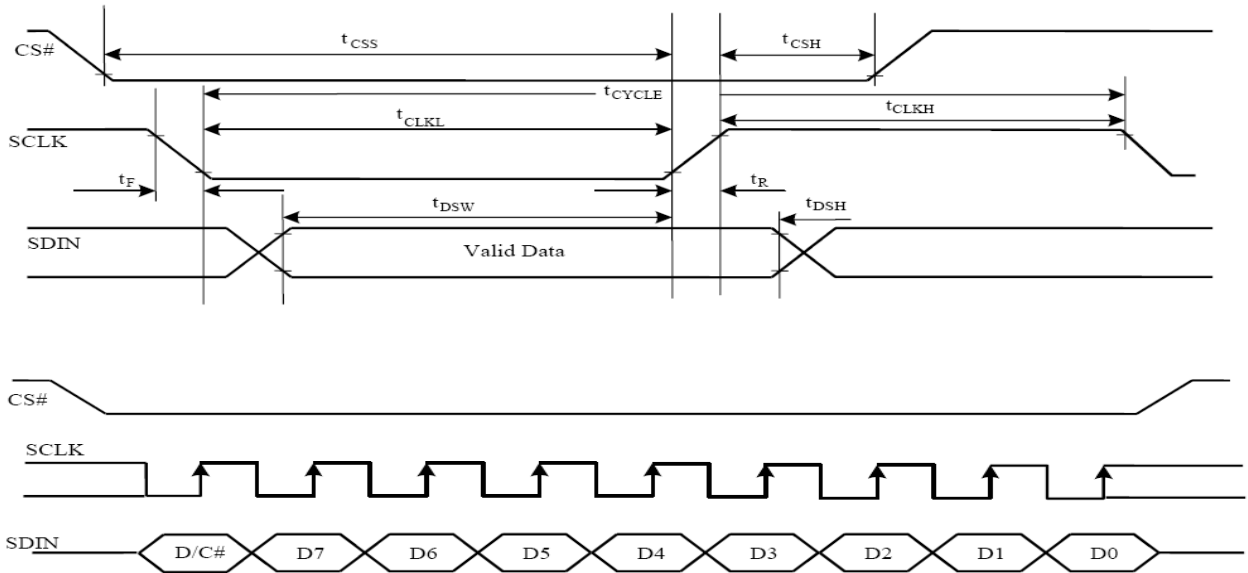
Parameter	Symbol	Min	Max	Unit
Clock Cycle Time	$t_{cycle}$	100	-	ns
Address Setup Time	$t_{AS}$	15	-	ns
Address Hold Time	$t_{AH}$	15	-	ns
Chip Select Setup Time	$t_{CSS}$	20	-	ns
Chip Select Hold Time	$t_{CSH}$	10	-	ns
Write Data Setup Time	$t_{DSW}$	15	-	ns
Write Data Hold Time	$t_{DHW}$	15	-	ns
Clock Low Time	$t_{CLKL}$	20	-	ns
Clock High Time	$t_{CLKH}$	20	-	ns
Rise Time	$t_r$	-	40	ns
Fall Time	$t_f$	-	40	ns



### 5.4 Serial Interface Timing Characteristics (3 wire SPI)

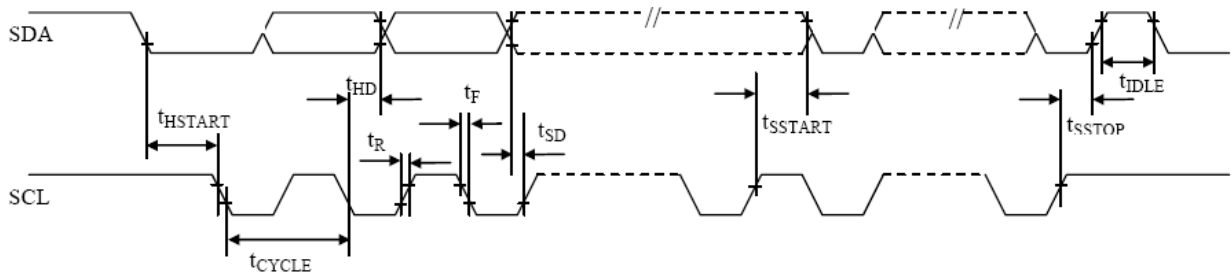
Parameter	Symbol	Min	Max	Unit
Clock Cycle Time	$t_{cycle}$	100	-	ns
Chip Select Setup Time	$t_{CSS}$	20	-	ns
Chip Select Hold Time	$t_{CSH}$	10	-	ns
Write Data Setup Time	$t_{DSW}$	15	-	ns
Write Data Hold Time	$t_{DHW}$	15	-	ns
Clock Low Time	$t_{CLKL}$	20	-	ns
Clock High Time	$t_{CLKH}$	20	-	ns
Rise Time	$t_r$	-	40	ns
Fall Time	$t_f$	-	40	ns





## 5.5 I<sup>2</sup>C Interface Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Clock Cycle Time	$t_{cycle}$	2.5	-	$\mu s$
Start Condition Hold Time	$t_{HSTART}$	0.6	-	$\mu s$
Data Hold Time (for "SDA <sub>OUT</sub> " Pin)	$t_{HD}$	0	-	ns
Data Hold Time (for "SDA <sub>IN</sub> " Pin)		300		
Data Setup Time	$t_{SD}$	100	-	ns
Start Condition Setup Time (Only relevant for a repeated Start Condition)	$t_{SSTART}$	0.6	-	$\mu s$
Stop Condition Setup Time	$t_{SSTOP}$	0.6	-	$\mu s$
Rise Time for Data and Clock Pin	$t_r$	-	300	ns
Fall Time for Data and Clock Pin	$t_f$	-	300	ns
Idle Time before a New Transmission can Start	$t_{IDLE}$	1.3	-	$\mu s$



## **6. Cautions and Handling Precautions**

### **6.1 Handling and Operating the Module**

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static, it may cause damage to the CMOS ICs.
9. Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the "Power ON" condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

### **6.2 Storage and Transportation**

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
2. Do not store the OLED module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.