Rev 2; 8/07

DALLAS SEMICONDUCTOR MAXIM

3.3V, 8-Bit, Programmable Timing Element

DS1123L

General Description

The DS1123L is an 8-bit programmable timing element similar in function to the DS1023, but operating at 3.3V. Like the DS1023, the DS1123L can delay signals up to a full period or more when used as a delay line, and an on-chip reference delay can be used to offset the inherent "step-zero" delay. This allows the DS1123L to shift a clock signal over the full 0 to 360° phase range. In addition to functioning as a delay line, it can be configured as a free-running oscillator or an externally triggered monostable vibrator.

Features

- **Step Sizes of 0.25ns, 0.5ns, 1ns, 2ns**
- **On-Chip Reference Delay**
- **Configurable as a Delay Line, Monostable Vibrator, or Free-Running Oscillator**
- **Can Delay Signals by a Full Period or More**
- **Guaranteed Monotonicity**
- **Parallel and 3-Wire Serial Programming Interface**
- **Single 3.3V Power Supply**
- **16-pin TSSOP**

Applications

Telecommunications

Digital Test Equipment

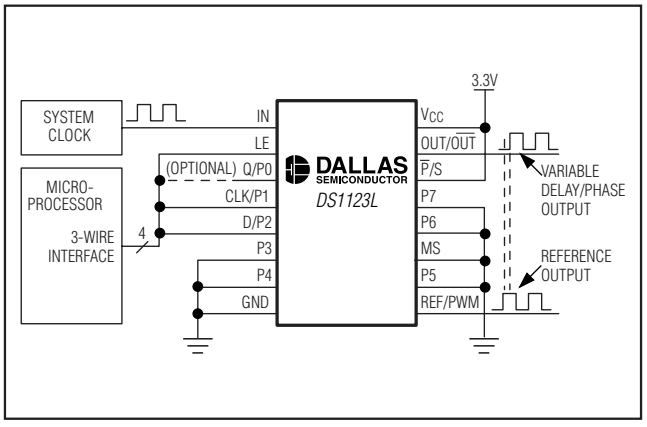
Digital Video Projection

Signal Generators and Analyzers

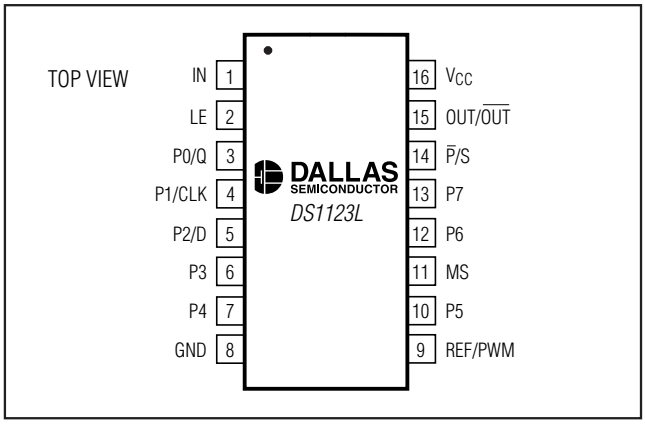
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE (150-mil)	STEP SIZE/ NO. OF STEPS
DS1123LE-25	0°C to +70°C	16 TSSOP	0.25/256
DS1123LE-50	0°C to +70°C	16 TSSOP	0.5/256
DS1123LE-100	0°C to +70°C	16 TSSOP	1/256
DS1123LE-200	0°C to +70°C	16 TSSOP	2/256

Typical Operating Circuit



Pin Configuration



3.3V, 8-Bit, Programmable Timing Element

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Pin Relative to Ground .....-0.5V to +6.0V
*Voltage Range on IN, LE, Q/P0, CLK/P1, D/P2, P3, P4, P5, MS, P6, P7, and $\overline{P}$/S Relative to Ground .....-0.5V to V_{CC} + 0.5V
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Short-Circuit Output Current .....50mA for 1s
Soldering Temperature .....See IPC/JEDEC J-STD-020A Specification

**Not to exceed +6.0V*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+3.0		+3.6	V
Input Logic 1	V_{IH}	(Note 2)	0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		-0.3		+0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0 to 3.6V, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active and Standby Current	I_{CC}			16	30	mA
High-Level Output Current	I_{OH}	V_{CC} = min, V_{OH} = 2.3V			-1.0	mA
Low-Level Output Current	I_{OL}	Q output, V_{CC} = min, V_{OL} = 0.5V			4.0	mA
		All other outputs, V_{CC} = min, V_{OL} = 0.5V			8.0	
Input Leakage	I_L		-1.0		+1.0	µA

AC ELECTRICAL CHARACTERISTICS (ALL SPEED OPTIONS)

(V_{CC} = +3.0V to 3.6V, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{CLK}				10	MHz
Input Pulse Width (LE, CLK)	T_W		50			ns
Data Setup to Clock	t_{DSC}		30			ns
Data Hold from Clock	t_{DHC}		0			ns
Data Setup to Enable	t_{DSE}		30			ns
Data Hold to Enable	t_{DHE}		0			ns
Enable Setup to Clock	t_{ES}		0			ns
Enable Hold from Clock	t_{EH}		30			ns
LE to Q Valid	t_{EQV}				50	ns
LE to Q High-Z	t_{EQZ}		0		50	ns
CLK to Q Valid	t_{CQV}				50	ns
CLK to Q Invalid	t_{CQX}		0			ns
Parallel Input to Delay Valid	t_{PDV}				500	ns
Parallel Input to Delay Invalid	t_{PDX}		0			ns
LE to Delay Valid	t_{EDV}				500	ns
LE to Delay Invalid	t_{EDX}		0			ns
Power-Up Time	t_{PU}				100	ms

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AC ELECTRICAL CHARACTERISTICS (DS1123L-25)

(V_{CC} = +3.0V to 3.6V, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Delay	t_{REF}	(Notes 3, 4)		18	22	ns
Delay Step Size	t_{STEP}	T_A = +25°C	0	0.25	1.75	ns
Step-Zero Delay with Respect to IN	t_{D0}	(Notes 4, 5)		16.5	22	ns
Step-Zero Delay with Respect to REF	t_{D0REF}	(Notes 6, 7)	-2.5	-1.5	0	ns
Maximum Delay with Respect to IN	t_{DMAX}	(Notes 4, 8)		80		ns
Delay with Respect to REF	t_{DREF}	Position FO (Notes 7, 9)		60		ns
Delay with Respect to REF Tolerance	$\frac{\Delta t_{DREF}}{t_{DREF}}$	V_{CC} = 3.3V, T_A = +25°C (Notes 7, 9)	-0.75		+0.75	%
Voltage Delay Variation	$\frac{\Delta t_{DV}}{t_{DREF}}$	(Notes 7, 9)	-1		+1	%
Temperature Delay Variation	$\frac{\Delta t_{DT}}{t_{DREF}}$	V_{CC} = 3.3V (Notes 7, 9)	-2.5		+2.5	%
Integral Nonlinearity (Deviation from Straight Line)	t_{err}	(Note 10)	-2	0	+2	ns
$\overline{OUT}$ Delta Delay	t_{INV0}	(Note 11)	0	1	2.5	ns
IN High to PWM High	t_{PWM0}	(Notes 4, 12)		16.5	22	ns
Minimum PWM Output Pulse Width	t_{PWM}	(Note 13)	5			ns
Minimum Input Pulse Width	t_{WI}	(Note 14)	40			ns
Minimum Input Period		(Note 15)	80			ns
Input Rise and Fall Times	t_r, t_f	(Note 16)	0		1	µs

AC ELECTRICAL CHARACTERISTICS (DS1123L-50)

(V_{CC} = +3.0V to 3.6V, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Delay	t_{REF}	(Notes 3, 4)		18	22	ns
Delay Step Size	t_{STEP}	T_A = +25°C	0	0.5	1.75	ns
Step-Zero Delay with Respect to IN	t_{D0}	(Notes 4, 5)		16.5	22	ns
Step-Zero Delay with Respect to REF	t_{D0REF}	(Notes 6, 7)	-2.5	-1.5	0	ns
Maximum Delay with Respect to IN	t_{DMAX}	(Notes 4, 8)		144		ns
Delay with Respect to REF	t_{DREF}	Position FF (Notes 7, 9)		127.5		ns
Delay with Respect to REF Tolerance	$\frac{\Delta t_{DREF}}{t_{DREF}}$	V_{CC} = 3.3V, T_A = +25°C (Notes 7, 9)	-0.75		+0.75	%
Voltage Delay Variation	$\frac{\Delta t_{DV}}{t_{DREF}}$	(Notes 7, 9)	-0.75		+0.75	%
Temperature Delay Variation	$\frac{\Delta t_{DT}}{t_{DREF}}$	V_{CC} = 3.3V (Notes 7, 9)	-2.5		+2.5	%
Integral Nonlinearity (Deviation from Straight Line)	t_{err}	(Note 10)	-2	0	+2	ns
$\overline{OUT}$ Delta Delay	t_{INV0}	(Note 11)	0	1	2.5	ns
IN High to PWM High	t_{PWM0}	(Notes 4, 12)		16.5	22	ns
Minimum PWM Output Pulse Width	t_{PWM}	(Note 13)	5			ns
Minimum Input Pulse Width	t_{WI}	(Note 14)	40			ns
Minimum Input Period		(Note 15)	80			ns
Input Rise and Fall Times	t_r, t_f	(Note 16)	0		1	µs

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AC ELECTRICAL CHARACTERISTICS (DS1123L-100)

(V_{CC} = +3.0V to 3.6V, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Delay	t_{REF}	(Notes 3, 4)		18	22	ns
Delay Step Size	t_{STEP}	T_A = +25°C	0	1	2.25	ns
Step-Zero Delay with Respect to IN	t_{D0}	(Notes 4, 5)		16.5	22	ns
Step-Zero Delay with Respect to REF	t_{D0REF}	(Notes 6, 7)	-2.5	-1.5	0	ns
Maximum Delay with Respect to IN	t_{DMAX}	(Notes 4, 8)		272		ns
Delay with Respect to REF	t_{DREF}	Position FF (Notes 7, 9)		255		ns
Delay with Respect to REF Tolerance	$\frac{\Delta t_{DREF}}{t_{DREF}}$	V_{CC} = 3.3V, T_A = +25°C (Notes 7, 9)	-0.75		+0.75	%
Voltage Delay Variation	$\frac{\Delta t_{DV}}{t_{DREF}}$	(Notes 7, 9)	-0.5		+0.5	%
Temperature Delay Variation	$\frac{\Delta t_{DT}}{t_{DREF}}$	V_{CC} = 3.3V (Notes 7, 9)	-2.5		+2.5	%
Integral Nonlinearity (Deviation from Straight Line)	t_{err}	(Note 10)	-4	0	+4	ns
$\overline{OUT}$ Delta Delay	t_{INV0}	(Note 11)	0	1	2.5	ns
IN High to PWM High	t_{PWM0}	(Notes 4, 12)		16.5	22	ns
Minimum PWM Output Pulse Width	t_{PWM}	(Note 13)	5			ns
Minimum Input Pulse Width	t_{WI}	(Note 14)	40			ns
Minimum Input Period		(Note 15)	80			ns
Input Rise and Fall Times	t_r, t_f	(Note 16)	0		1	µs

Note 1: All voltages are referenced to ground.

Note 2: If IN is high during power-up, the output remains low until IN is toggled low and back high again.

Note 3: The reference delay is closely matched to the step-zero delay to allow relative timings down to zero or less.

Note 4: Measured from rising edge of the input to the rising edge of the output (t_{DR}).

Note 5: Delay from input to output with a programmed delay value of zero.

Note 6: This is the relative delay between REF and OUT. The device is designed such that when programmed to zero delay the OUT output always appears before the REF output. This parameter is numerically equal to t_{D0} - t_{REF} (see Figure 8).

Note 7: From rising edge to rising edge.

Note 8: This is the actual measured delay from IN to OUT. This parameter exhibits greater temperature variation than the relative delay parameter.

Note 9: This is the actual measured delay with respect to the REF output. This parameter more closely reflects the programmed delay value than the absolute delay parameter (see Figure 8). Typical delay shift due to aging is within ±0.85%. Aging stressing includes level 1 moisture reflow preconditioning (24hr +125°C bake, 168hr +85°C/85%RH moisture soak, and three solder reflow passes +260°C +0°C/-5°C peak) followed by 1000hr (max) V_{CC} biased +125°C OP/L, 1000hr unbiased +150°C bake, and 1000 temperature cycles at -55°C to +125°C.

AC ELECTRICAL CHARACTERISTICS (DS1123L-200)

(V_{CC} = +3.0V to 3.6V, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Delay	t_{REF}	(Notes 3, 4)		18	22	ns
Delay Step Size	t_{STEP}	T_A = +25°C	1.0	2	3.0	ns
Step-Zero Delay with Respect to IN	t_{D0}	(Notes 4, 5)		16.5	22	ns
Step-Zero Delay with Respect to REF	t_{D0REF}	(Notes 6, 7)	-2.5	-1.5	0	ns
Maximum Delay with Respect to IN	t_{DMAX}	(Notes 4, 8)		527		ns
Delay with Respect to REF	t_{DREF}	Position FF (Notes 7, 9)		510		ns
Delay with Respect to REF Tolerance	$\frac{\Delta t_{DREF}}{t_{DREF}}$	V_{CC} = 3.3V, T_A = +25°C (Notes 7, 9)	-0.75		+0.75	%
Voltage Delay Variation	$\frac{\Delta t_{DV}}{t_{DREF}}$	(Notes 7, 9)	-0.5		+0.5	%
Temperature Delay Variation	$\frac{\Delta t_{DT}}{t_{DREF}}$	V_{CC} = 3.3V	-2.5		+2.5	%
Integral Nonlinearity (Deviation from Straight Line)	t_{err}	(Note 10)	-5	0	+5	ns
$\overline{OUT}$ Delta Delay	t_{INV0}	(Note 11)	0	1	2.5	ns
IN High to PWM High	t_{PWM0}	(Notes 4, 12)		16.5	22	ns
Minimum PWM Output Pulse Width	t_{PWM}	(Note 13)	5			ns
Minimum Input Pulse Width	t_{WI}	(Note 14)	40			ns
Minimum Input Period		(Note 15)	80			ns
Input Rise and Fall Times	t_r, t_f	(Note 16)	0		1	s

Note 10: See the *Integral Nonlinearity* section and Figure 9.

Note 11: Change in delay value when the inverted output is selected instead of the normal, noninverting output.

Note 12: In PWM mode, the delay between the rising edge of the input and the rising edge of the output.

Note 13: The minimum value for which the monostable-vibrator pulse width should be programmed. Narrower pulse widths can be programmed, but output levels may be impaired and ultimately no output pulse is produced.

Note 14: This is the minimum allowable interval between transitions on the input to assure accurate device operation. This parameter may be violated, but timing accuracy may be impaired and ultimately very narrow pulse widths result in no output from the device.

Note 15: This parameter applies to normal delay mode only. When a 50% duty cycle input clock is used this defines the highest usable clock frequency. When asymmetrical clock inputs are used, the maximum usable clock frequency must be reduced to conform to the minimum input pulse-width requirement. In PWM mode, the minimum input period is equal to the step-zero delay and the programmed delay (t_{DO} + t_D).

Note 16: Faster rise and fall times give the greatest accuracy in measured delay. Slow edges (outside the specification maximum) can result in erratic operations.

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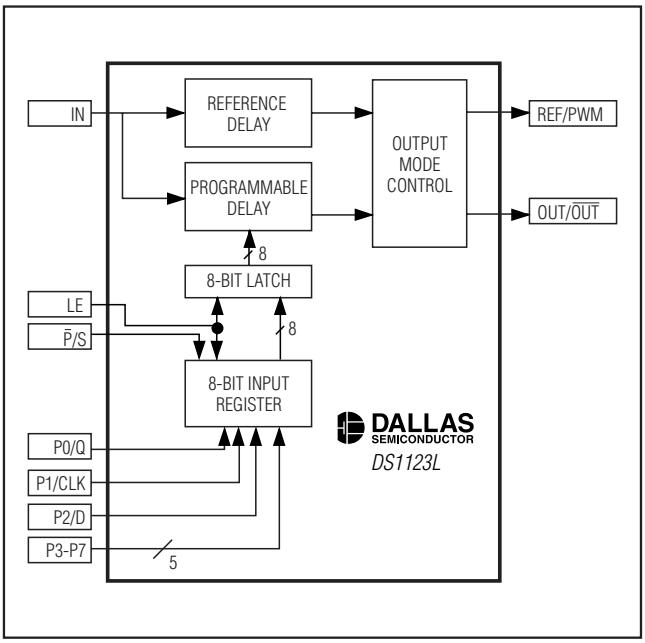
Pin Description

PIN	NAME	FUNCTION
1	IN	Input Signal to be Delayed, PWM Trigger
2	LE	Input-Latch Enable
3	P0/Q	Input P0 (Parallel Mode)/ Serial Data Output (Serial Mode)
4	P1/CLK	Input P1 (Parallel Mode)/ Serial Clock (Serial Mode)
5	P2/D	Input P2 (Parallel Mode)/ Serial Data Input (Serial Mode)
6	P3	Input P3
7	P4	Input P4
8	GND	Ground
9	REF/PWM	Reference Output/PWM Output
10	P5	Input P5
11	MS	Input Mode Select MS = 0 for Delay Function, MS = 1 for Oscillator or PWM
12	P6	Input P6
13	P7	Input P7
14	$\overline{P}$/S	Parallel/Serial Programming Select
15	OUT/$\overline{OUT}$	Delay Output or Inverted Output
16	V_{CC}	Power Supply (3.3V)

Functional Diagram



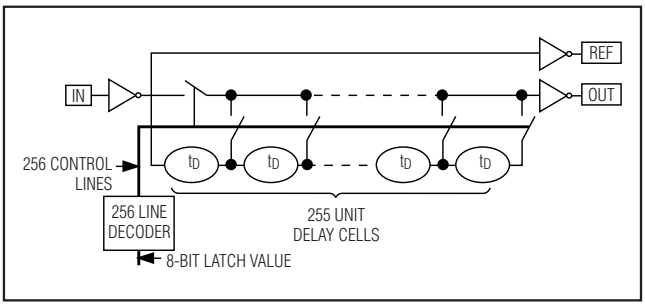


Figure 1. DS1123L Conceptual Design

Detailed Description

The DS1123L is an 8-bit programmable delay line that can be adjusted between 256 different delay intervals. Because of the design (see Figure 1) of the DS1123L, it is possible to delay a signal by a whole period or more, which allows the phase of the signal to be adjusted up to a full 360°. Programming may be done using either an 8-bit parallel interface or a 3-wire serial interface. Using the 3-wire interface, it is possible to cascade multiple devices together for systems requiring multiple programmable delays without using additional I/O resources. The DS1123L also features a reference delay that is approximately equal to the step-zero delay, which can be used to realize small relative delays. Additionally, the DS1123L can function as a monostable vibrator or an adjustable frequency oscillator.

Device Operation

This section details how to program the DS1123L using both the parallel and serial interfaces, using the reference delay, and how to configure the chip to function as a monostable vibrator or adjustable frequency oscillator.

Using the Parallel Programming Interface

To enable the DS1123L's parallel interface, $\overline{P}$/S must be connected to ground. This allows the data on the parallel inputs (P0 to P7) to pass through the latch, which are transparent when latch enable (LE) is at a high input level. When LE is at a low level, the data is latched until LE is returned to a high state. If the parallel inputs are going to be used to hardwire a delay, LE must be connected to V_{CC} to allow the setting to take

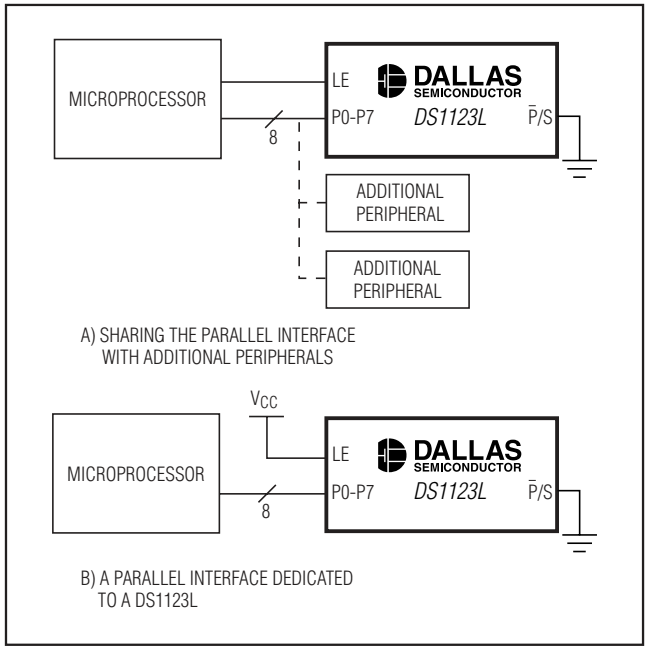


Figure 2. Parallel Interface Options for DS1123L

effect on power-up. The most flexibility when using parallel mode occurs when the delay is being controlled by a microprocessor.

There are two common parallel interface implementations used to control the DS1123L using a microprocessor (see Figure 2). LE can be used to latch the data from the microprocessor, which allows the data bus to be shared with other peripherals, or LE can be tied high, which causes the DS1123L to adjust its delay immediately following a change to the parallel inputs. For each configuration, a settling time (t_{EDV} or t_{PDV}) is required after an adjustment is made before the input signal is accurately delayed according to the new setting. Figures 3 and 4 show the timing required for these implementations.

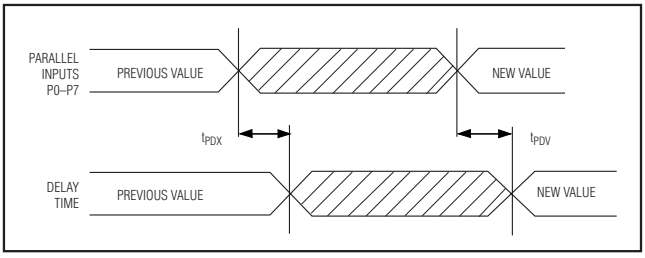


Figure 3. Nonlatched Parallel Timing Diagram

Using the Serial Programming Interface

The 3-wire serial interface is enabled by connecting $\overline{P}/S$ to V_{CC}. Serial mode operates similar to a shift register. When LE is set at a high logic level, it enables the register and CLK clocks the data, D, into the register one bit at a time starting with the most significant bit. After all 8 bits are shifted into the DS1123L, LE is pulled low to end the data transfer and activate the new value. A settling time (t_{EDV}) is required after LE is pulled low before the signal delay meets its specified accuracy. A timing diagram for the serial interface is shown in Figure 6. The 3-wire interface also has an output (Q) that can be used to cascade multiple 3-wire devices, and it can be used to read the current value of the devices on the bus.

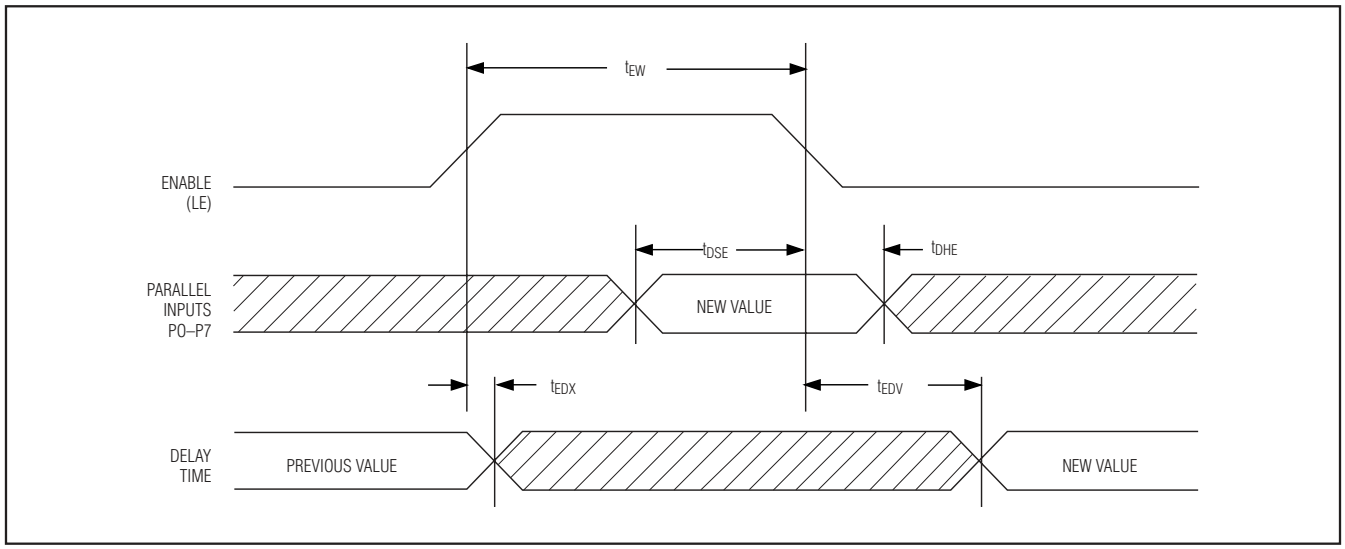


Figure 4. Latched Parallel Timing Diagram

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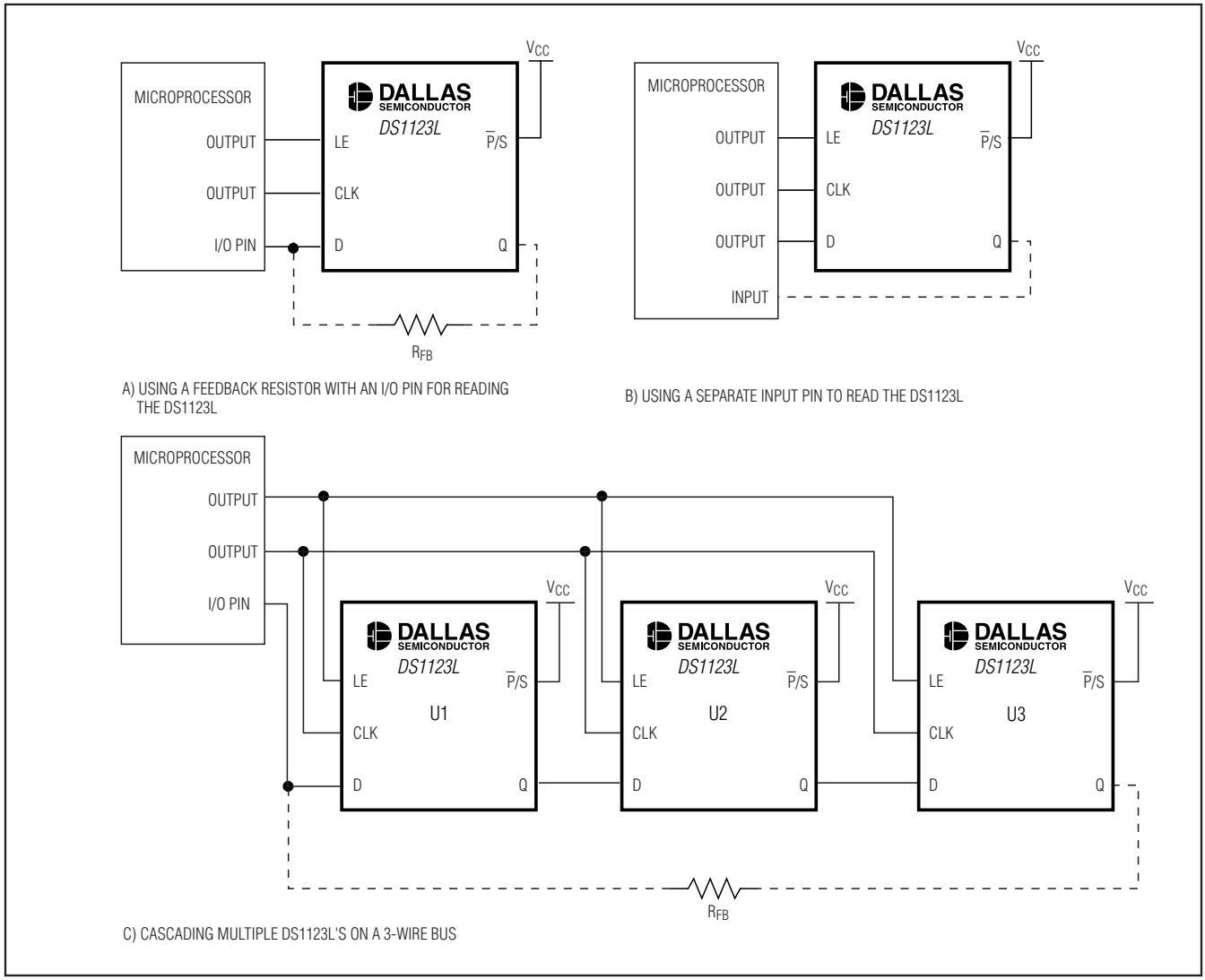

Figure 5. Using the Serial Interface

To read the current values stored by the 3-wire device(s), the latch must be enabled and the value of Q must be read and then written back to D before the register is clocked. This causes the current value of the register to be written back into the DS1123L as it is being read. This can be accomplished in a couple of different ways. If the microprocessor has an I/O pin that is high impedance when set as an input, a feedback resistor (generally between 1kΩ and 10kΩ) can be used to write the data on Q back to D as the value is read (see Figure 5a). If the microprocessor has an internal pullup on its I/O pins, or only offers separate input and output pins, the value in the register can still be read. The circuit shown in Figure 5b allows the Q values to read by the microprocessor, which must write the Q value to D before it can clock the bus to read the next bit. If the Q values are read without writing them to D (with the pullup or otherwise), the read is destructive. A destructive read cycle likely results in an undesirable change in the delay setting.

Figure 5c shows how to cascade multiple DS1123L's onto the same 3-wire bus. One important detail of writing software for cascaded 3-wire devices is that all the devices on the bus must be written to or read from during each read or write cycle. Attempting to write to only the first device (U1) would cause the data stored in U1

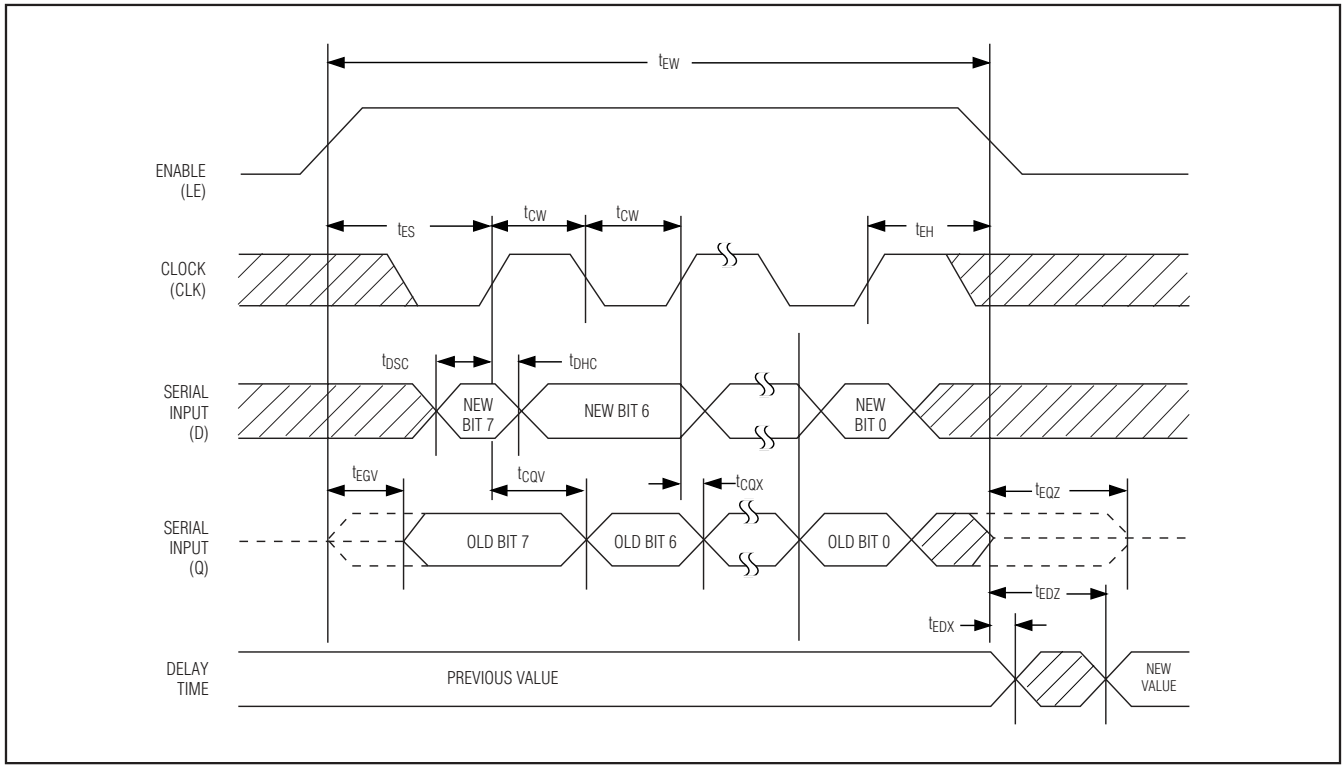

Figure 6. Serial Interface Timing Diagram

to be shifted to U2, U2's data would be shifted to U3, etc. As shown, the microprocessor would have to shift 24 bits during each read or write cycle to avoid inadvertently changing the settings in any of the 3-wire devices. Also note that the feedback resistor or a separate input (not shown) can still be used to read the 3-wire device settings when multiple devices are cascaded.

Configuring the DS1123L as a Delay Line

To use the DS1123L as a delay line, the MS pin must be tied to ground. When used as a delay line, the internal architecture of the DS1123L allows the output delay time to be considerably longer than the input pulse width (see AC specifications). This feature is useful in many applications, in particular in clock phase control, where delays up to and beyond one full clock period can be achieved. Table 1 lists some of the delay characteristics of the different speed options available for the DS1123L device.

Using the Reference Delay

All delay lines have an inherent step-zero delay between IN and OUT (t_{D0}) due to the propagation delay through the input and output buffers. To simplify system design, a reference delay has been included on the DS1123L that can be used to compensate for the step-zero delay. The reference output allows the DS1123L to be used to generate small differential delays that cannot be generated when the OUT delay is referenced to the input. The step-zero OUT delay is always approximately 1ns faster than the REF delay (see Figure 8). This allows the DS1123L to generate a nondelayed output with respect to the reference output. In addition, the reference output driver is sized similarly to the OUT output driver, both outputs act similarly over temperature, and they are both triggered at the same time regardless of the exact input threshold. These features make the output delay with respect to the reference act more ideally because both of these outputs are skewed approximately the same amount due to these phenomena.

Integral Nonlinearity

Integral nonlinearity (INL) is defined as the deviation from a straight line response drawn between the measured step-zero delay and the measured step 255 delay with respect to the reference output. INL measured with respect to IN is not specified, but should be slightly higher than when measured with respect to the reference output. This is because measurements taken with respect to

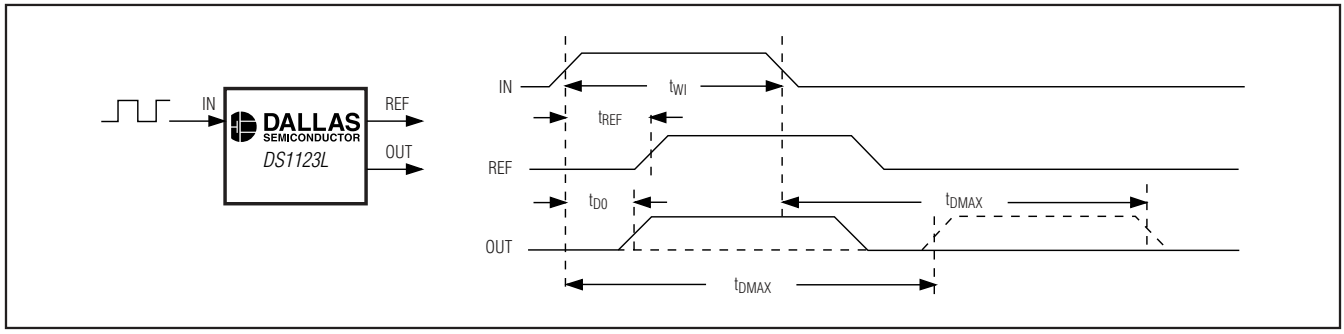

Figure 7. Reference Delay Timing, MS = 0

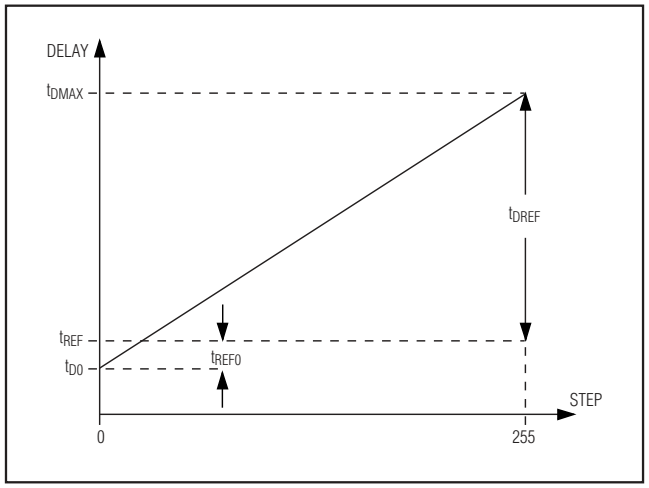

Figure 8. Delay Parameters

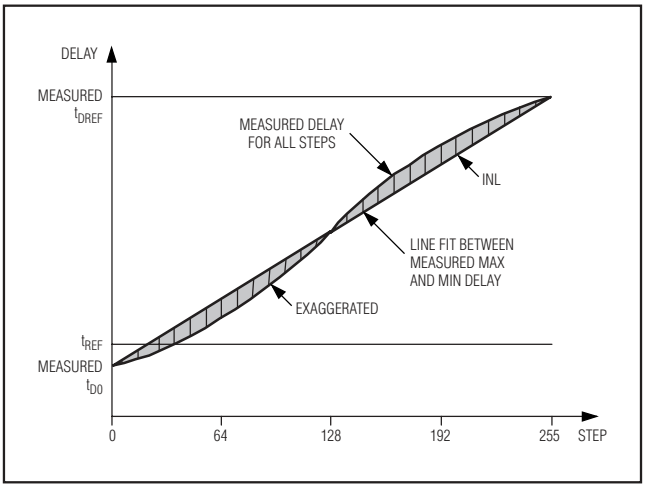

Figure 9. Integral Nonlinearity

IN do not benefit from the REF output's tendency to track OUT over temperature and voltage. Figure 9 shows INL's effect on delay performance graphically.

Configuring the DS1123L as a Monostable Vibrator or PWM

To configure the DS1123L as a monostable vibrator, set MS = 1. This causes the reference output (PWM) to be set high between t_{REF} and t_D when it is triggered by the input. After time period t_D has elapsed, the output returns low, and the monostable vibrator can be retriggered. See Figure 10 for the timing of the $\overline{OUT}$ and PWM signals. When MS = 1 and the DS1123L is triggered by an external free-running oscillator, reference output becomes a pulse-width modulator (PWM). When using the DS1123L as a PWM, the free-running oscillator should not be generated by connecting $\overline{OUT}$ to the input. This causes the PWM period to change in addition to the duty cycle as different values are programmed, which is most likely not the desired functionality.

The minimum pulse width that can be practically generated is approximately 5ns. This is because a 5ns pulse is approximately the shortest pulse that can be produced with the DS1123L's output driver. The monostable vibrator cannot be retriggered, so subsequent triggering pulses into IN should not be present until after the output has returned low.

Configuring the DS1123L as an Oscillator

To configure the DS1123L as an adjustable oscillator, set MS = 1 and externally connect $\overline{OUT}$ to IN. Setting MS = 1 by itself inverts the input signal in addition to delaying it (see Figure 10). Connecting $\overline{OUT}$ to the input then causes the circuit to oscillate with the period being twice the programmed delay. Table 2 shows the oscillator frequency ranges that the different speed grades of DS1123Ls provide.

Table 1. DS1123L Delay Line/PWM Ranges and Tolerances

PART	STEP SIZE (ns)	MAX DELAY TIME AND MAX PULSE WIDTH* (ns)	MAX INTEGRAL NONLINEARITY (ns)	MAX INPUT FREQUENCY (MHz)	MIN INPUT PULSE WIDTH (ns)
DS1123L-25	0.25	63.75	±2	25	40
DS1123L-50	0.5	127.5	±2	25	40
DS1123L-100	1.0	255	±4	25	40
DS1123L-200	2.0	510	±5	25	40

**This is the maximum delay in normal mode (MS = 0) measured with respect to the reference output, and the maximum pulse width in monostable vibrator mode (MS = 1).*

Table 2. DS1123L Adjustable Oscillator Characteristics

PART	PERIOD CHANGE/STEP (ns)	MIN OSCILLATOR FREQUENCY (MHz)	MAX OSCILLATOR FREQUENCY* (MHz)
DS1123L-25	0.5	6.6	22
DS1123L-50	1.0	3.6	22
DS1123L-100	2.0	1.9	22
DS1123L-200	4.0	0.98	22

**Maximum output frequency depends on the actual step-zero delay value. Worst-case values are shown in the table. Output period is equal to 2 x tD, where tD = delay value referenced to IN.*

Application Information

Power-Supply Decoupling

To achieve the best results when using the DS1123L, decouple the power supply with a 0.01µF and a 0.1µF capacitor. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the V_{CC} and GND pins of the DS1123L to minimize lead inductance. The DS1123L may not perform as specified if good decoupling practices are not followed.

Unused Inputs When Using the Serial-Programming Mode

When using the serial-programming mode, the unused parallel inputs must be connected to V_{CC} or GND to prevent them from floating and drawing excessive current.

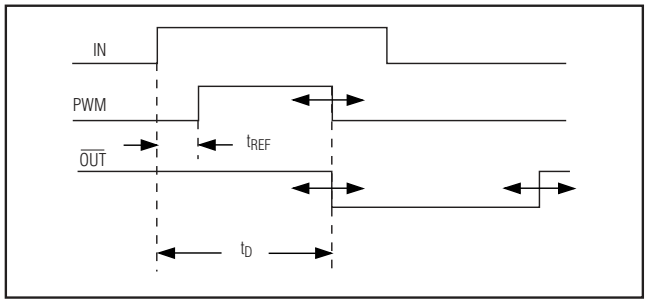

Figure 10. Output Timing Diagram for MS = 1

Test Conditions

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	3.3V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50Ω (Max)
Rise and Fall Times:	3.0ns (Max) (Measured Between 0.6V and 2.4V)
Pulse Width:	500ns
Period:	1µs

OUTPUT: The outputs are loaded with a 74F04. Delay is measured between the 1.5V level of the rising or falling edge of the input signal and the corresponding edge of the output signal.

NOTE: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

3.3V, 8-Bit, Programmable Timing Element

Chip Topology

TRANSISTOR COUNT: 6057

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

Revision History

Pages changed at Rev 2: 1, 6, 14