

# Am82S62

## Nine-Input Parity Checker/Generator

### Distinctive Characteristics

- ODD/EVEN parity outputs
- Inhibit input to disable both outputs
- High-speed expansion input – P<sub>9</sub>

- PNP inputs
- Advanced Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883.

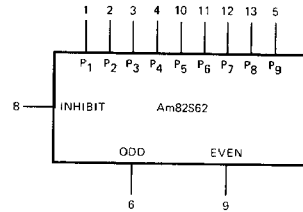
### FUNCTIONAL DESCRIPTION

The Am82S62 is a 9-bit parity generator/parity checker with both an ODD parity output and an EVEN parity output. The device can be used to detect errors in data transmission or data retrieval systems as well as to generate this parity check bit.

The Am82S62 features one special high-speed input (P<sub>9</sub>) to facilitate expansion. The propagation delay to the outputs through this path is considerably reduced when compared to the P<sub>1</sub> through P<sub>8</sub> paths. This short delay path allows parity checkers/generators of larger size than 9-bits to be built with a minimum of additional delay.

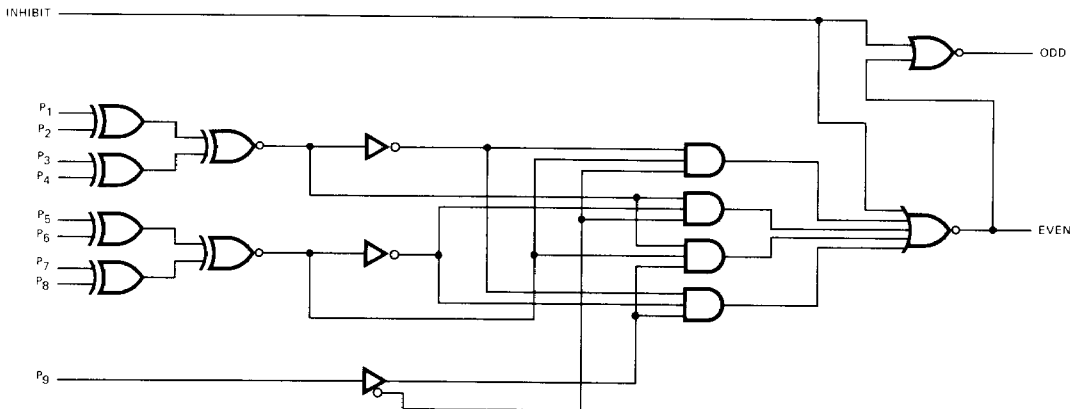
The device is built using advanced Schottky technology and incorporates PNP input transistors to reduce input loading to 0.4 STTL unit loads. The EVEN output is one gate propagation delay time shorter than the ODD output.

### LOGIC SYMBOL



V<sub>CC</sub> = Pin 14  
GND = Pin 7

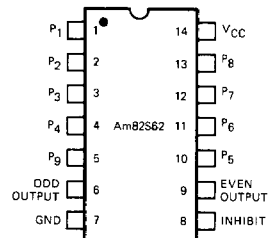
### LOGIC DIAGRAM



### ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	N82S62A
Hermetic DIP	0°C to +75°C	N82S62F
Dice	0°C to +75°C	N82S62X
Hermetic DIP	-55°C to +125°C	S82S62F
Dice	-55°C to +125°C	S82S62X

### CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

**MAXIMUM RATINGS** (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	-0.5V to +7V
V <sub>CC</sub> Voltage Applied to Outputs for HIGH Output State	-0.5V to +V <sub>CC</sub> max.
V <sub>CC</sub> Input Voltage	-0.5V to +5.5V
V <sub>CC</sub> Output Current, Into Outputs	30mA
V <sub>CC</sub> Input Current	-30mA to +5.0mA

**ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (Unless otherwise noted)

N82S62 T<sub>A</sub> = 0°C to +75°C V<sub>CC</sub> = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V  
 S82S62 T<sub>A</sub> = -55°C to +125°C

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = MIN., I <sub>OH</sub> = -1mA	S82	2.5		Volts
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	N82	2.7		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = MIN., I <sub>OL</sub> = 20mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.5	Volts
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = MIN., I <sub>IN</sub> = -18mA			-1.2	Volts
I <sub>IL</sub> (Note 3)	Input LOW Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 0.5V	P9		-0.4	mA
			Others		-0.8	
I <sub>IH</sub> (Note 3)	Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 4.5V			10	μA
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 5.5V			1.0	mA
I <sub>SC</sub>	Output Short Circuit Current (Note 4)	V <sub>CC</sub> = MAX., V <sub>OUT</sub> = 0.0V	-40		-100	mA
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = MAX. (Note 5)			67	mA

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.  
 2. Typical limits are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading.  
 3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).  
 4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 5. P<sub>1</sub> through P<sub>9</sub> grounded; inhibit at 4.5V; outputs open.

**Switching Characteristics** (T<sub>A</sub> = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t <sub>PLH</sub>	P <sub>1</sub> through P <sub>8</sub> to Even Output	V <sub>CC</sub> = 5.0V, R <sub>L</sub> = 280Ω, C <sub>L</sub> = 15 pF			23	ns
t <sub>PHL</sub>					28	ns
t <sub>PLH</sub>	P <sub>1</sub> through P <sub>8</sub> to Odd Output				12	ns
t <sub>PHL</sub>					18	ns
t <sub>PLH</sub>	P <sub>9</sub> to Even Output				9	ns
t <sub>PHL</sub>					9	ns
t <sub>PLH</sub>	P <sub>9</sub> to Odd Output					
t <sub>PHL</sub>						
t <sub>PLH</sub>	Inhibit to Even Output					
t <sub>PHL</sub>						
t <sub>PLH</sub>	Inhibit to Odd Output					
t <sub>PHL</sub>						

## TRUTH TABLE

INHIBIT	NUMBER OF P INPUTS		OUTPUT	
	LOW	HIGH	ODD	EVEN
L	0	9	H	L
L	1	8	L	H
L	2	7	H	L
L	3	6	L	H
L	4	5	H	L
L	5	4	L	H
L	6	3	H	L
L	7	2	L	H
L	8	1	H	L
L	9	0	L	H
H	X	X	L	L

H = HIGH  
L = LOW  
X = Don't Care

## LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output	
			HIGH	LOW
P <sub>1</sub>	1	0.4	—	—
P <sub>2</sub>	2	0.4	—	—
P <sub>3</sub>	3	0.4	—	—
P <sub>4</sub>	4	0.4	—	—
P <sub>9</sub>	5	0.2	—	—
ODD	6	—	20	10
GND	7	—	—	—
INHIBIT	8	0.4	—	—
EVEN	9	—	20	10
P <sub>5</sub>	10	0.4	—	—
P <sub>6</sub>	11	0.4	—	—
P <sub>7</sub>	12	0.4	—	—
P <sub>8</sub>	13	0.4	—	—
V <sub>CC</sub>	14	—	—	—

A Schottky TTL Unit Load is defined as 50 $\mu$ A measured at 2.7V HIGH and -2.0mA measured at 0.5V LOW.

## DEFINITION OF FUNCTIONAL TERMS

**P<sub>1</sub> through P<sub>9</sub>** The nine inputs to the parity tree.

**INHIBIT** A HIGH on the inhibit input forces both the odd output and even output LOW regardless of the P inputs. When the inhibit is LOW, the odd and even outputs will always be of opposite phase.

**ODD** The odd parity output of the device. When an odd number of P inputs are at a HIGH level, the odd output will be HIGH.

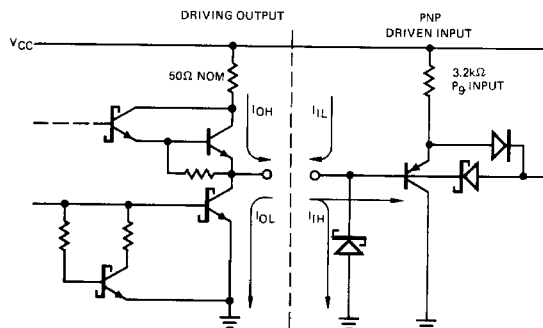
**EVEN** The even parity output of the device. When an even number of P inputs are at a HIGH level, the even output will be HIGH.

## LOGIC EQUATIONS

$$\text{ODD Output} = P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$$

$$\text{EVEN Output} = P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$$

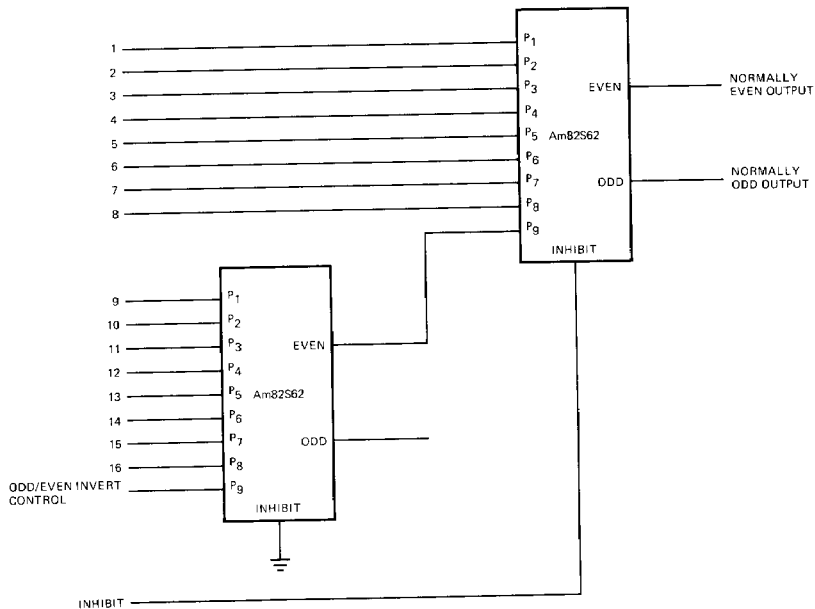
## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



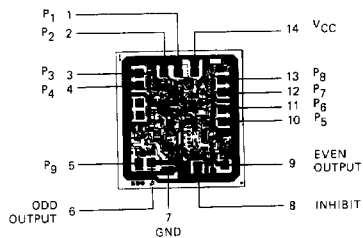
Note: Actual current flow direction shown.

## APPLICATION

## 16-BIT PARITY GENERATOR WITH INVERT CONTROL



## Metallization and Pad Layout



DIE SIZE 0.067" X 0.072"