TOSHIBA Field Effect Transistor Silicon N Channel MOS Type $(\pi - MOSVII)$

TK4A55D

Switching Regulator Applications

• Low drain-source ON resistance: RDS (ON) = 1.5Ω (typ.)

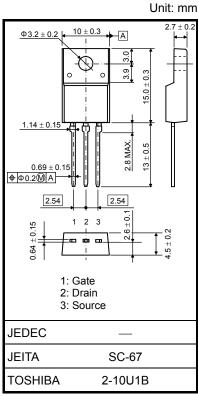
• High forward transfer admittance: $|Y_{fs}| = 2.0 \text{ S}$ (typ.)

• Low leakage current $: I_{DSS} = 10 \mu A \text{ (max) (V}_{DS} = 550 \text{ V)}$

• Enhancement-mode : $V_{th} = 2.4 \text{ to } 4.4 \text{ V (V}_{DS} = 10 \text{ V, I}_{D} = 1 \text{ mA)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		V_{DSS}	550	V	
Gate-source voltage		V _{GSS}	±30	V	
Drain current	DC (Note 1)	ID	4	Α	
	Pulse (Note 1)	I _{DP}	16	_ ^	
Drain power dissipati	on (Tc = 25°C)	P _D	35	W	
Single pulse avalance	ne energy (Note 2)	E _{AS}	137	mJ	
Avalanche current		I _{AR}	4	А	
Repetitive avalanche	energy (Note 3)	E _{AR}	3.5	mJ	
Channel temperature		T _{ch}	150	°C	
Storage temperature	range	T _{stg}	-55 to 150	°C	



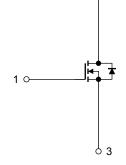
Weight: 1.7 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	R _{th (ch-c)}	3.57	°C/W
Thermal resistance, channel to ambient	R _{th (ch-a)}	62.5	°C/W

Internal Connection



Note 1: Please use devices on conditions that the channel temperature is below 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 14.8 mH, R_G = 25 Ω , I_{AR} = 4 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device. Please handle with caution.

Start of commercial production 2009-01

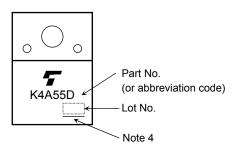
Electrical Characteristics (Ta = 25°C)

Chara	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА
Drain cut-off current		I _{DSS}	V _{DS} = 550 V, V _{GS} = 0 V	_	_	10	μА
Drain-source breakdown voltage		V _{(BR)DSS}	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	550	_	_	V
Gate threshold voltage		V _{th}	V _{DS} = 10 V, I _D = 1 mA	2.4	_	4.4	V
Drain-source ON	resistance	R _{DS} (ON)	V _{GS} = 10 V, I _D = 2 A	_	1.5	1.88	Ω
Forward transfer	admittance	Y _{fs}	V _{DS} = 10 V, I _D = 2 A	0.5	2.0	_	S
Input capacitance		C _{iss}		_	490	_	
Reverse transfer capacitance		C _{rss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	_	3	_	pF
Output capacitance		C _{oss}		_	55	_	
Switching time	Rise time	t _r	V_{GS} V_{OD} $V_{DD} \approx 200 \text{ V}$	_	18	_	. ns
	Turn-on time	t _{on}			40	_	
	Fall time	t _f			8		
	Turn-off time	t _{off}	Duty \leq 1%, $t_W = 10 \ \mu s$	_	55	_	
Total gate charge		Qg		_	11	_	
Gate-source charge		Q _{gs}	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$	_	6	_	nC
Gate-drain charge		Q _{gd}		_	5	_	

Source-Drain Ratings and Characteristics (Ta = 25°C)

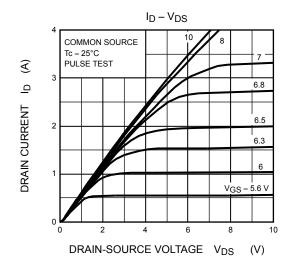
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	_	_	_	4	Α
Pulse drain reverse current (Note 1)	I _{DRP}	_	_	_	16	Α
Forward voltage (diode)	V_{DSF}	I _{DR} = 4 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	I _{DR} = 4 A, V _{GS} = 0 V,	_	900	_	ns
Reverse recovery charge	Q _{rr}	dI _{DR} /dt = 100 A/μs	_	5	_	μС

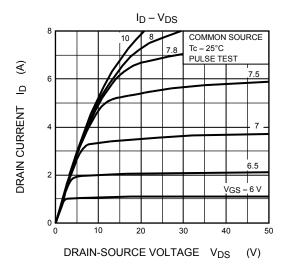
Marking

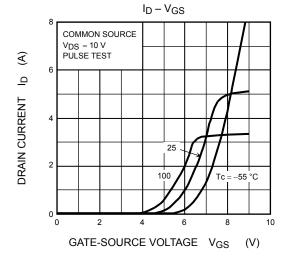


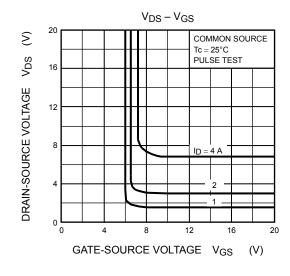
Note 4 : A line under a Lot No. identifies the indication of product Labels [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

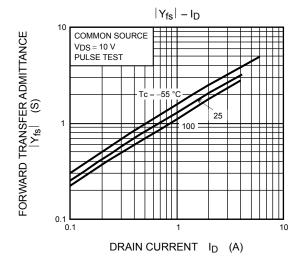
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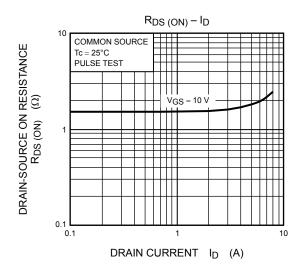


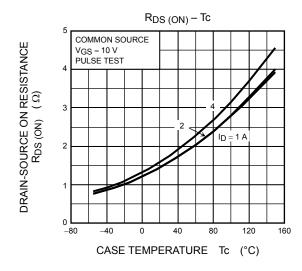


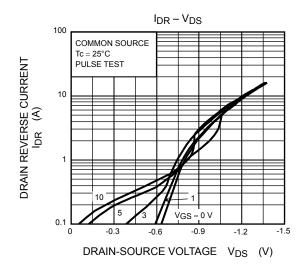


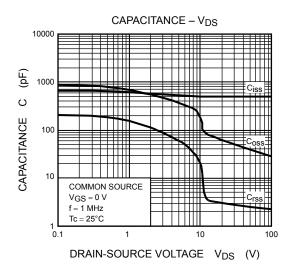


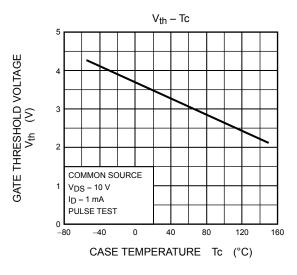


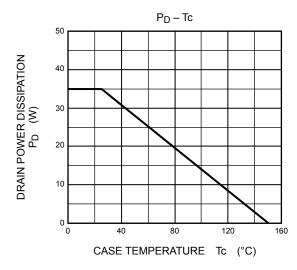


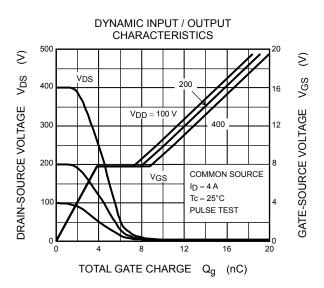


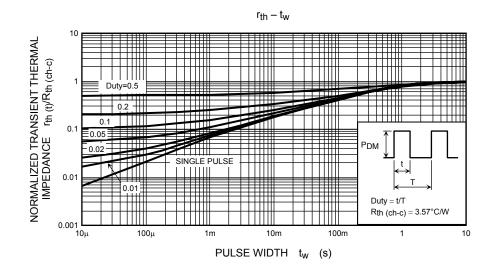


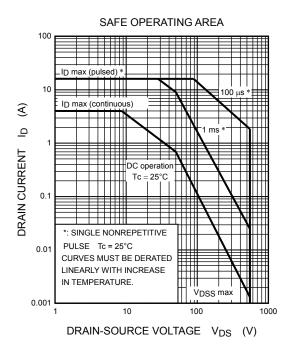


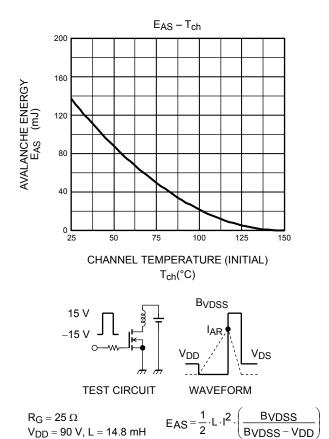












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