Toshiba CMOS Digital Integrated Circuit Silicon Monolithic

TC7MB3245FT, TC7MB3245FK

Octal Bus Switch

The TC7MB3245 provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

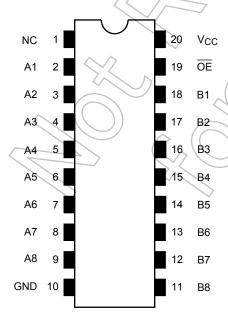
The device is organized as one 8-bit switch. When output enable (\overline{OE}) is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

All inputs are equipped with protection circuits against static discharge.

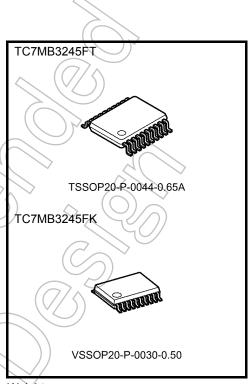
Features

- Operating voltage: $V_{CC} = 4.5$ to 5.5 V
- High speed: $t_{pd} = 0.25 \text{ ns (max)}$
- Low on resistance: $RON = 5 \Omega$ (typ.)
- ESD performance: Machine model $\geq \pm 200 \text{ V}$ Human body model $\geq \pm 2000 \text{ V}$
- Compatible with TTL outputs (control inputs)
- Package: TSSOP20, VSSOP20 (US20)
- Pin compatible with the 74xx245 type.
 Functionally equivalent to (FST/CBT) 3245

Pin Assignment (top view)



NC-No Internal Connection



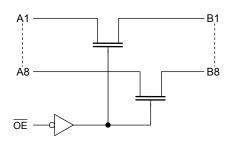
Weight

TSSOP20-P-0044-0.65A : 0.08 g (typ.) VSSOP20-P-0030-0.50 : 0.03 g (typ.)

Truth Table

Inputs	Function				
ŌĒ	runction				
L	A port = B port				
Н	Disconnect				

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply range	V _{CC}	-0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to 7.0	V
DC switch voltage	Vs	-0.5 to 7.0	/N
Input diode current	I _{IK}	-50	mA
Continuous channel circuit	Is)) 128	mA
Power dissipation	Po	180	mW
DC V _{CC} /ground current	ICC/IGND	±100	mA
Storage temperature	Tstg	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	4.5 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Switch voltage	Vs	0 to 5.5	V
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

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Electrical Characteristics

DC Characteristics ($Ta = -40 \text{ to } 85^{\circ}\text{C}$)

Charac	teristics	Symbol	Test Condition		V _{CC} (V)	Min	Typ. (Note 1)	Max	Unit
Input voltage	"H" level	V_{IH}	_		4.5 to 5.5	2.0	_	_	V
Input voltage	"L" level	V _{IL}	_		4.5 to 5.5		_	0.8	V
Input leakage o	urrent	I _{IN}	V _{IN} = 0 to 5.5 V		4.5 to 5.5	1))′_	±1.0	μА
Power off leaka	ige current	l _{OFF}	A, B, $\overline{OE} = 0 \text{ to } 5.5 \text{ V}$		0) 	_	±1.0	μА
Off-STATE leak (switch off)	kage current	I _{SZ}	A, B = 0 to 5.5 V, $\overline{OE} = V_{CC}$		4.5 to 5.5		_	±1.0	μА
			V 0V	I _{IS} = 64 mA	4.5	_	5	7	
ON resistance (Note 2)	Ron	$V_{IS} = 0 V$	I _{IS} = 30 mA	4.5	_	5	7	Ω	
		/ _{IS} = 2.4 V, I _{IS} = 15 mA		4.5	/	<10	15		
Quiescent supp	oly current	Icc	V _{IN} = V _{CC} or GND, I _{OUT} = 0		5.5	-6	7-//	7 10	μΑ
Increase in I _{CC}	per input	Δlcc	V _{IN} = 3.4 V (one input)		5.5	7-6	(A)	2.5	mA

Note 1: Typical values are at $V_{CC} = 5 \text{ V}$, $Ta = 25^{\circ}\text{C}$.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay time (bus to bus)	tpLH Figure 1, Figure 2 (Note)	4.5	_	0.25	ns
Output enable time	tpZL Figure 1, Figure 3	4.5	_	5.9	ns
Output disable time	t _{pLZ} t _{pHZ} Figure 1, Figure 3	4.5	_	5.9	ns

Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Control pin input capacitance	ÇIN	(Note	5.0	3	pF
Switch terminal capacitance	C _{I/O}	$\overline{OE} = V_{CC}$ (Note	5.0	10	pF

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Note: Parameter guaranteed by design.

AC Test Circuit

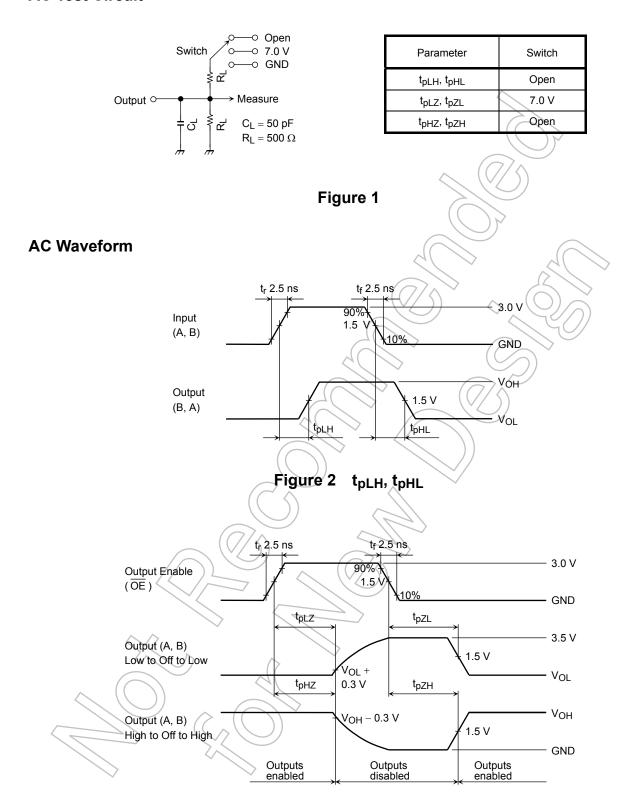
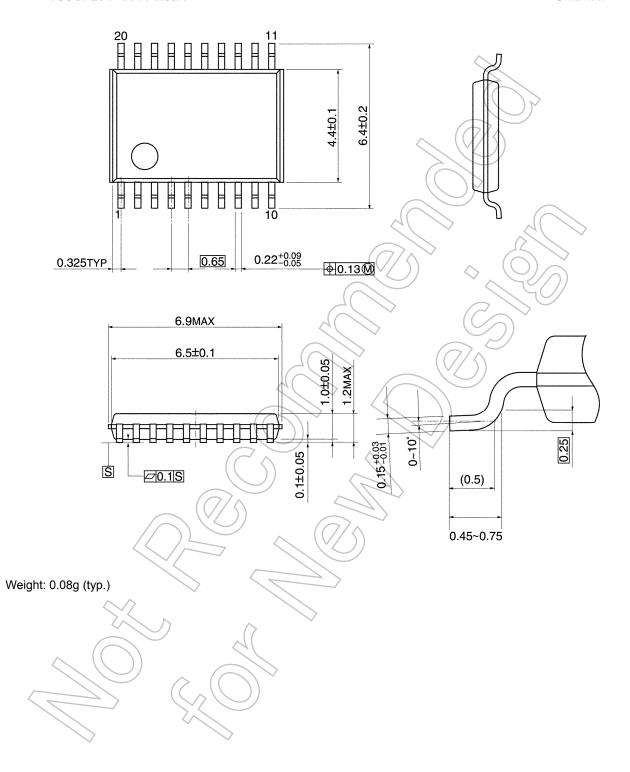


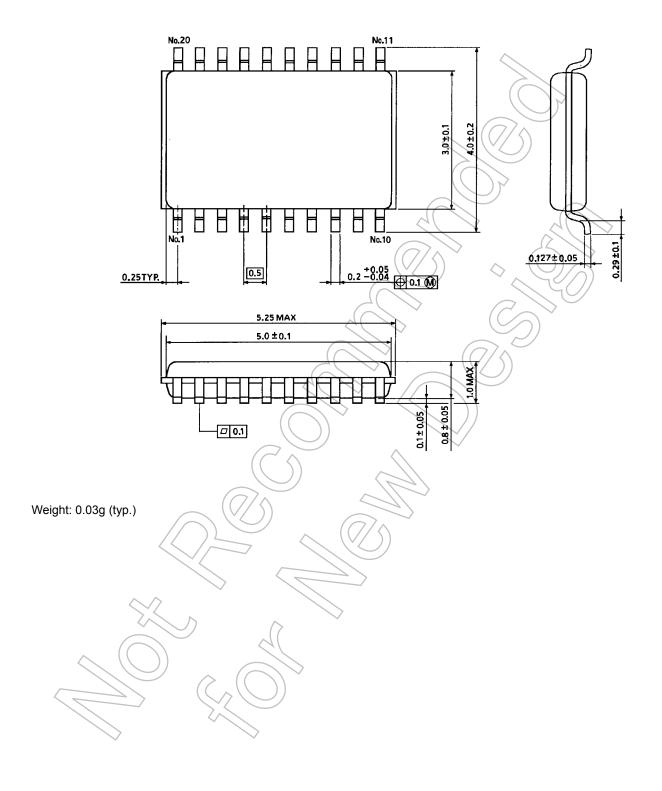
Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Package Dimensions

TSSOP20-P-0044-0.65A Unit: mm



Package Dimensions



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