

### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 5V to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Lower di/dt gate driver for better noise immunity
- Leadfree, RoHS compliant
- Automotive qualified\*

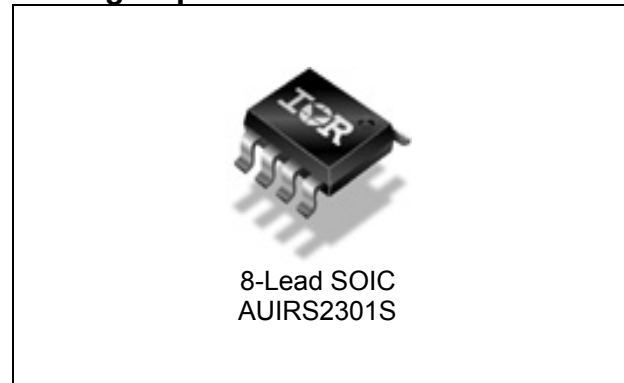
### Typical Applications

- Automotive motor drives
- Servo drives
- Micro inverter drives
- General purpose three phase inverters

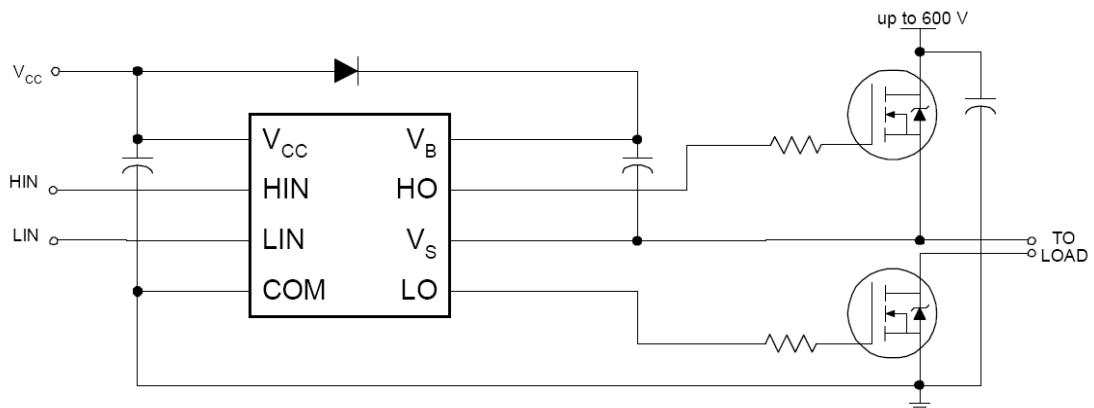
### Product Summary

$V_{\text{OFFSET}}$	600V Max
$V_{\text{OUT}}$	5V – 20V
$I_{\text{O+}} \& I_{\text{O-}}$ (typical)	200mA / 350mA
$t_{\text{ON}} \& t_{\text{OFF}}$ (typical)	220ns / 200ns
Delay Matching	50ns

### Package Options



### Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

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## **Description**

The AUIRS2301S is a high voltage, high speed power MOSFET and IGBT driver with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600V.

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Automotive (per AEC-Q100 <sup>††</sup> )
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.
<b>Moisture Sensitivity Level</b>		MSL3 <sup>†††</sup> 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class M2 (Pass +/-200V) (per AEC-Q100-003)
	Human Body Model	Class H1C (Pass +/-2000V) (per AEC-Q100-002)
	Charged Device Model	Class C5 (Pass +/-1000V) (per AEC-Q100-011)
<b>IC Latch-Up Test</b>		Class II , Level B (per AEC-Q100-004)
<b>RoHS Compliant</b>		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

**Absolute Maximum Ratings**

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_B$	High-side floating absolute voltage	-0.3	625	V
$V_S$	High-side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
$V_{HO}$	High-side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
$V_{CC}$	Low-side and logic fixed supply voltage	-0.3	25	
$V_{LO}$	Low-side output voltage	-0.3	$V_{CC} + 0.3$	
$V_{IN}$	Logic input voltage (HIN & LIN)	COM -0.3	$V_{CC} + 0.3$	
$dV_S/dt$	Allowable offset supply voltage transient	—	50	V/ns
$P_D$	Package power dissipation @ $T_A \leq 25^\circ\text{C}$	—	0.625	W
$R_{thJA}$	Thermal resistance, junction to ambient	—	200	$^\circ\text{C}/\text{W}$
$T_J$	Junction temperature	—	150	$^\circ\text{C}$
$T_S$	Storage temperature	-50	150	
$T_L$	Lead temperature (soldering, 10 seconds)	—	300	

**Recommended Operating Conditions**

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_B$	High-side floating supply absolute voltage	$V_S + 5$	$V_S + 20$	V
$V_S$	High-side floating supply offset voltage	† 1	600	
$V_{HO}$	High-side floating output voltage	$V_S$	$V_B$	
$V_{CC}$	Low-side and logic fixed supply voltage	5	20	
$V_{LO}$	Low-side output voltage	0	$V_{CC}$	
$V_{IN}$	Logic input voltage (HIN & LIN)	COM	$V_{CC}$	
$T_A$	Ambient temperature	-40	125	$^\circ\text{C}$

†: Logic operational for  $V_S$  of -5 V to +600 V. Logic state held for  $V_S$  of -5 V to  $-V_{BS}$ .  
 (Please refer to the Design Tip DT97 -3 for more details).

**Static Electrical Characteristics**

Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  with bias conditions of  $V_{\text{BIAS}} (V_{\text{CC}}, V_{\text{BS}}) = 15\text{V}$ . The  $V_{\text{IL}}$ ,  $V_{\text{IH}}$  and  $I_{\text{IN}}$  parameters are referenced to COM and are applicable to the respective input leads: HIN and LIN. The  $V_{\text{O}}$ ,  $I_{\text{O}}$  and  $R_{\text{on}}$  parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

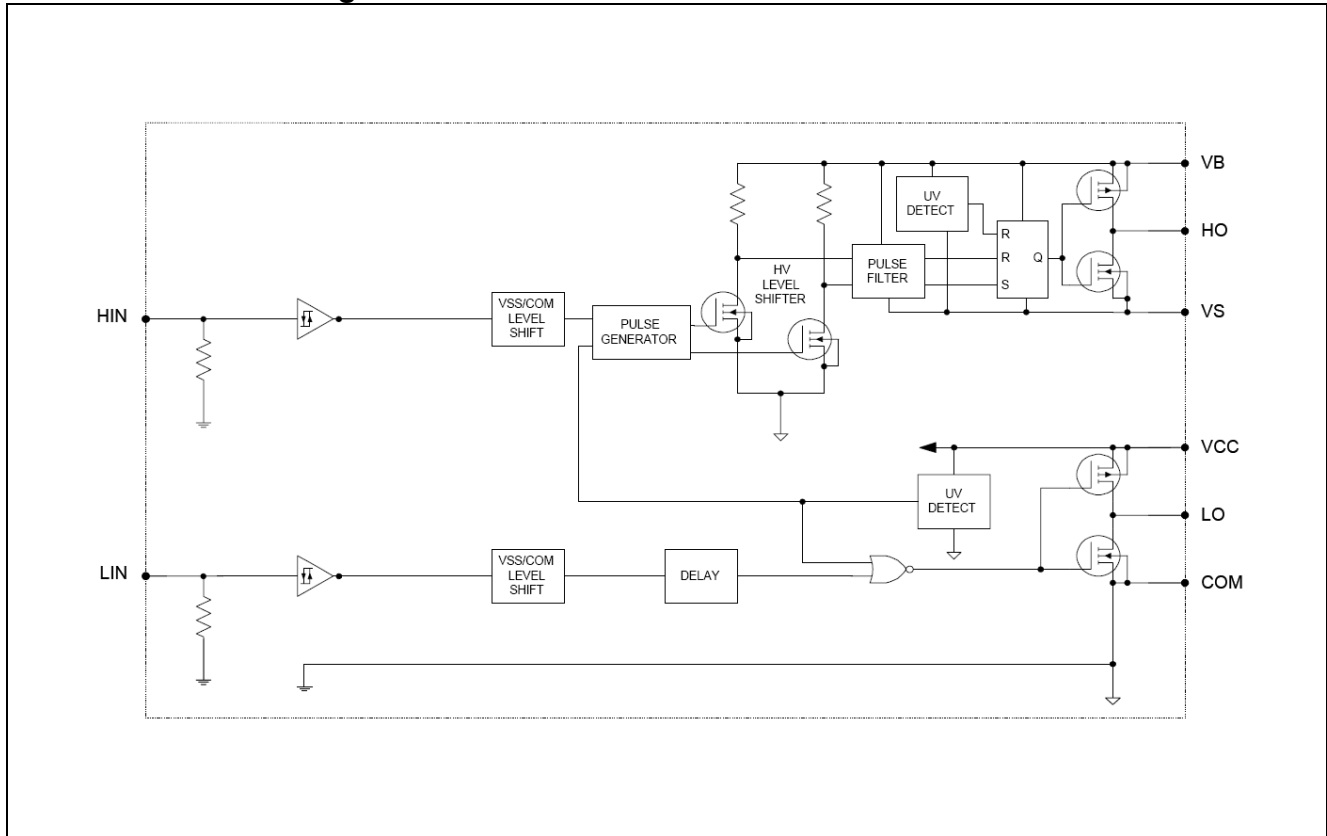
Symbol	Definition	Min	Typ	Max	Units	Test conditions
$V_{\text{IH}}$	Logic "1" input voltage	2.5	—	—	V	$V_{\text{CC}} = 10\text{V to } 20\text{V}$
$V_{\text{IL}}$	Logic "0" input voltage	—	—	0.8		
$V_{\text{OH}}$	High level output voltage, $V_{\text{BIAS}} - V_{\text{O}}$	—	—	0.2	V	$I_{\text{O}} = 2\text{mA}$
$V_{\text{OL}}$	Low level output voltage, $V_{\text{O}}$	—	—	0.1		
$I_{\text{LK}}$	Offset supply leakage current	—	—	50	$\mu\text{A}$	$V_{\text{B}} = V_{\text{S}} = 600\text{V}$
$I_{\text{QBS}}$	Quiescent $V_{\text{BS}}$ supply current	60	160	260		$V_{\text{IN}} = 0\text{V or } 5\text{V}$
$I_{\text{QCC}}$	Quiescent $V_{\text{CC}}$ supply current	60	160	260		$V_{\text{IN}} = 5\text{V}$
$I_{\text{IN+}}$	Logic "1" input bias current	—	5	20		$V_{\text{IN}} = 0\text{V}$
$I_{\text{IN-}}$	Logic "0" input bias current	—	—	5		
$V_{\text{CCUV+}}$ $V_{\text{BSUV+}}$	$V_{\text{CC}}$ and $V_{\text{BS}}$ supply undervoltage positive going threshold	3.3	4.1	5	V	
$V_{\text{CCUV-}}$ $V_{\text{BSUV-}}$	$V_{\text{CC}}$ and $V_{\text{BS}}$ supply undervoltage negative going threshold	3	3.8	4.7		
$V_{\text{CCUVH}}$ $V_{\text{BSUVH}}$	Hysteresis	0.1	0.3	—		
$I_{\text{O+}}$	Output high short circuit pulsed current	—	200	—	mA	$V_{\text{O}} = 0\text{V},$ $\text{PW} \leq 10\mu\text{s}$
$I_{\text{O-}}$	Output low short circuit pulsed current	—	350	—		$V_{\text{O}} = 15\text{V},$ $\text{PW} \leq 10\mu\text{s}$

**Dynamic Electrical Characteristics**

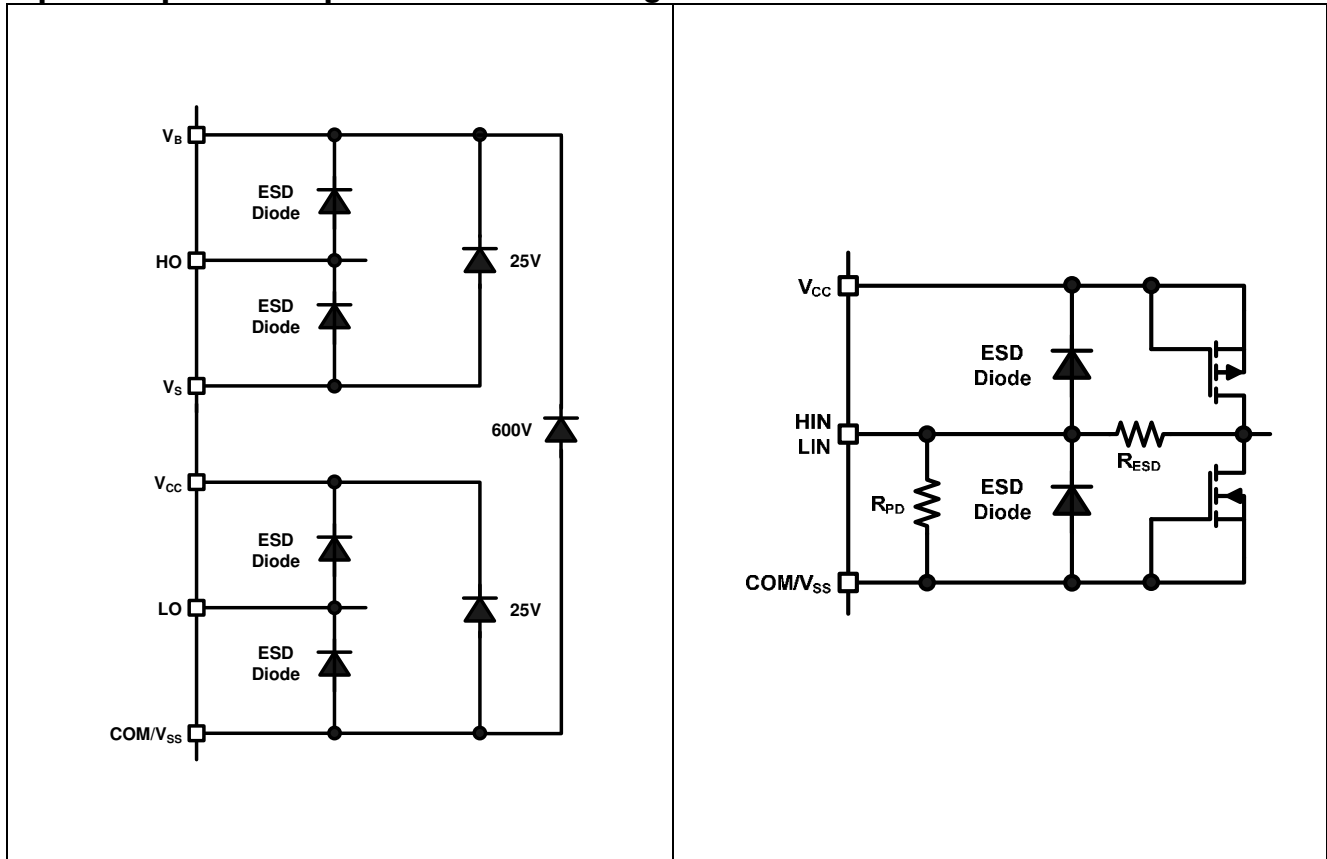
Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  with bias conditions of  $V_{\text{BIAS}} (V_{\text{CC}}, V_{\text{BS}}) = 15\text{V}$ ,  $C_{\text{L}} = 1000\text{pF}$ .

Symbol	Definition	Min	Typ	Max	Units	Test conditions
$t_{\text{on}}$	Turn-on propagation delay	—	220	300	ns	$V_{\text{S}} = 0\text{V}$
$t_{\text{off}}$	Turn-off propagation delay	—	200	280		$V_{\text{S}} = 0\text{V or } 600\text{V}$
MT	Delay matching, HS & LS turn-on/off	—	0	50		
$t_{\text{r}}$	Turn-on rise time	—	130	220		$V_{\text{S}} = 0\text{V}$
$t_{\text{f}}$	Turn-off fall time	—	50	80		

**Functional Block Diagram:**



**Input/Output Pin Equivalent Circuit Diagrams:**

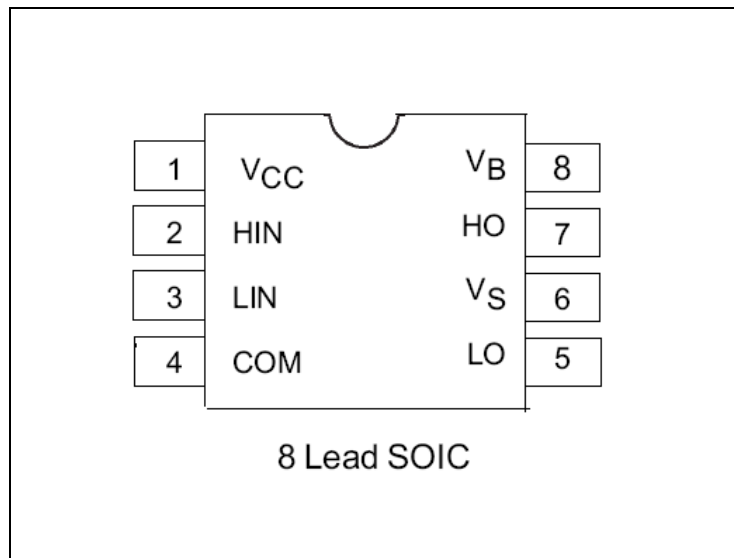




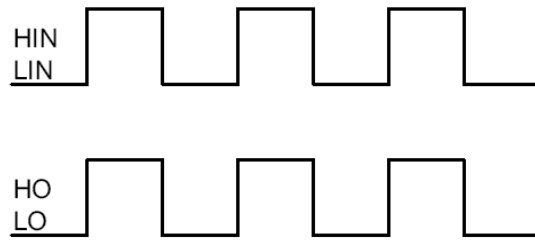
**Lead Definitions:**

PIN#	Symbol	Description
1	V <sub>CC</sub>	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver outputs (HO), in phase with HO
3	LIN	Logic input for low-side gate driver outputs (LO), in phase with LO
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V <sub>S</sub>	High-side floating supply return
7	HO	High-side gate drive output
8	V <sub>B</sub>	High-side floating supply

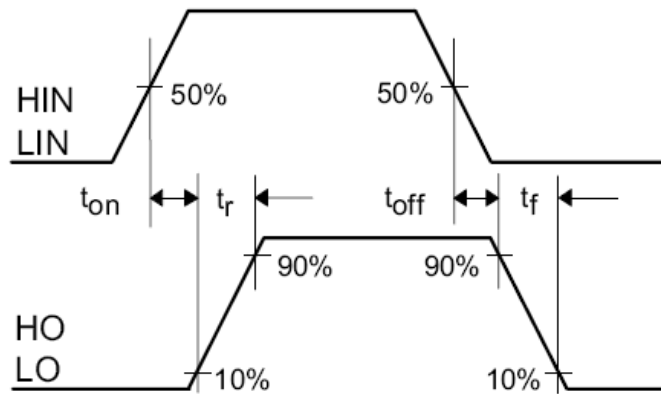
**Lead Assignments**



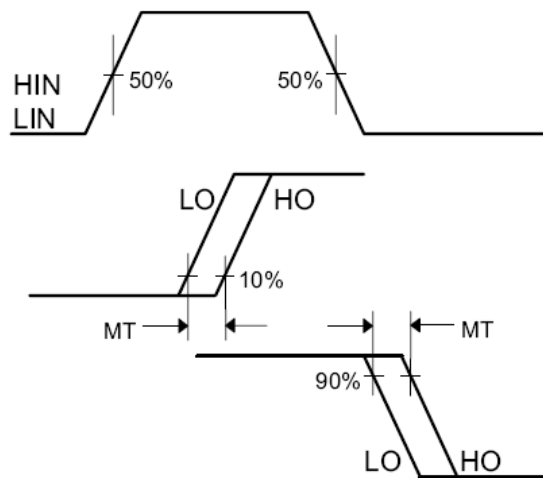
**Application Information and Additional Details**



**Figure 1: Input/Output Timing Diagram**



**Figure 2: Switching Time Waveform Definitions**



**Figure 3: Delay Matching Waveform Definitions**

**Tolerability to Negative Vs Transients**

The AUIRS2301S has been seen to withstand negative Vs transient conditions on the order of -25V for a period of 100 ns ( $V_{BIAS} (V_{CC}, V_{BS}) = 15V$  and  $T_A = 25^\circ C$ ).

An illustration of the AUIRS2301S performance can be seen in Figure 4.

Even though the AUIRS2301S has been shown able to handle these negative Vs transient conditions, it is highly recommended that the circuit designer always limit the negative Vs transients as much as possible by careful PCB layout and component use.

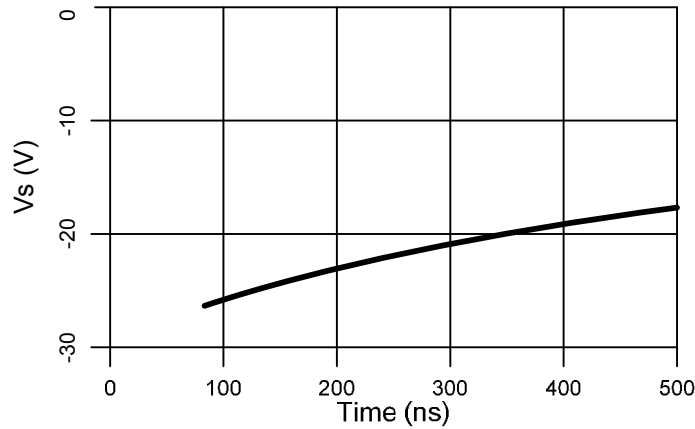
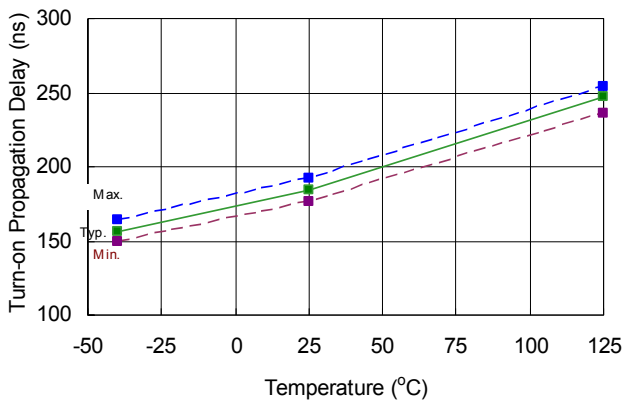


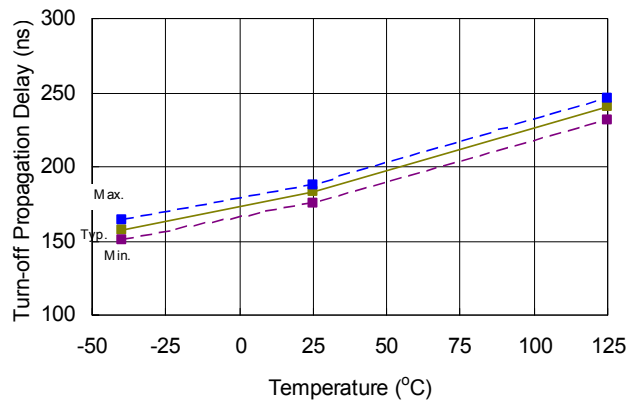
Figure 4: -Vs Transient results

**Parameter Temperature Trends**

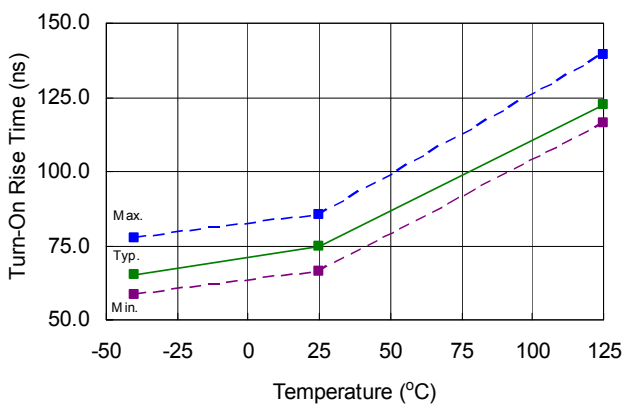
Figures illustrated in this chapter provide information on the experimental performance of the AUIRS2301S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).



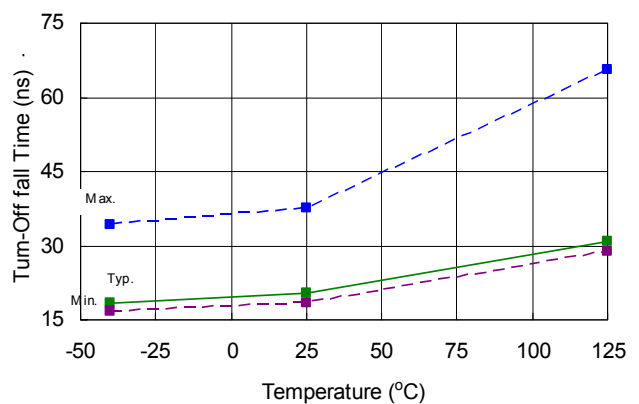
**Figure 5: T<sub>ON</sub> vs. temperature**



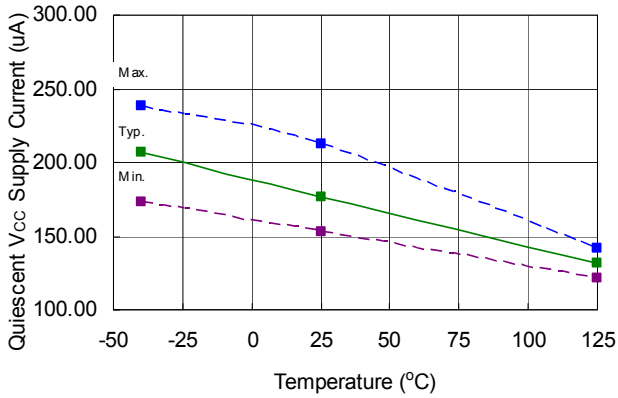
**Figure 6: T<sub>OFF</sub> vs. temperature**



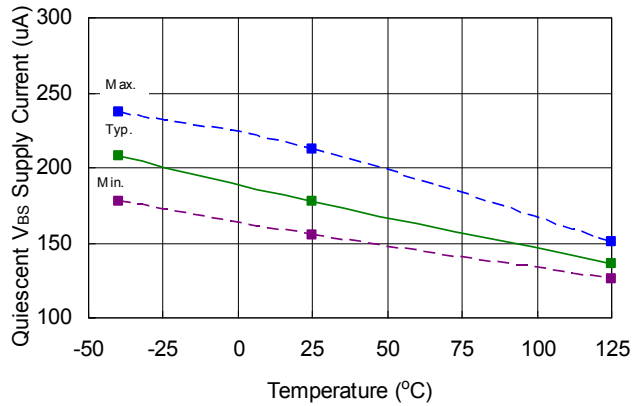
**Figure 7: T<sub>R</sub> vs. temperature**



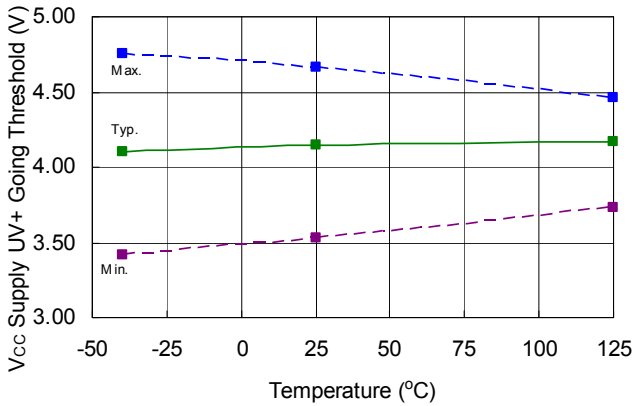
**Figure 8: T<sub>F</sub> vs. temperature**



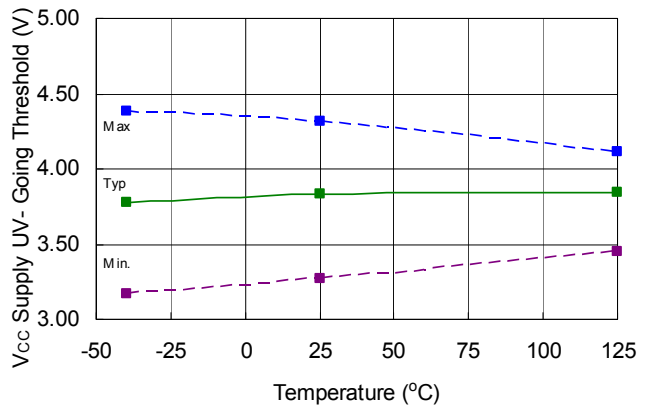
**Figure 9: V<sub>CC</sub> supply current vs. temperature**



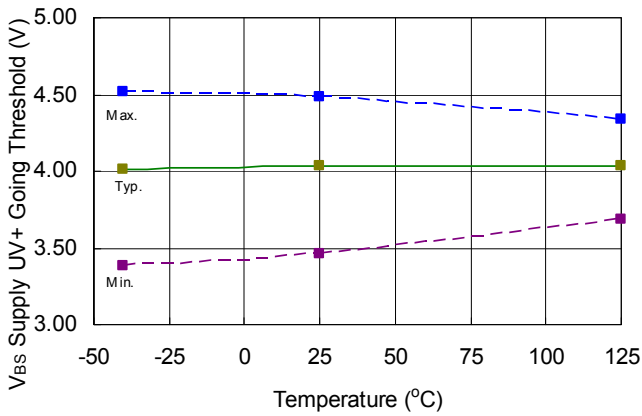
**Figure 10: V<sub>BS</sub> supply current vs. temperature**



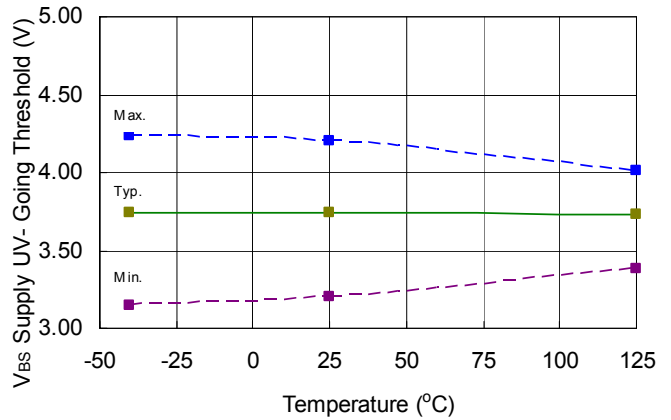
**Figure 11: V<sub>CCUV+</sub> vs. temperature**



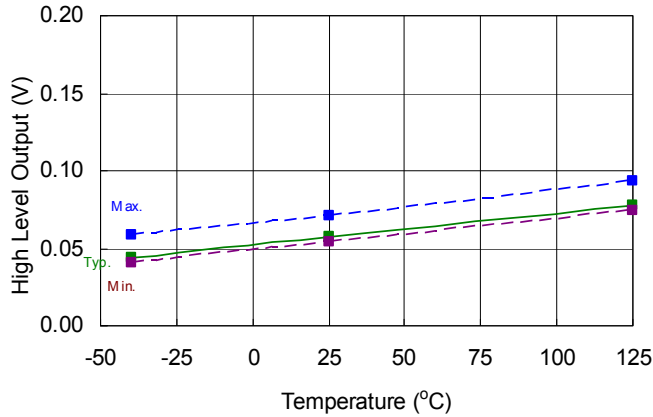
**Figure 12: V<sub>CCUV-</sub> vs. temperature**



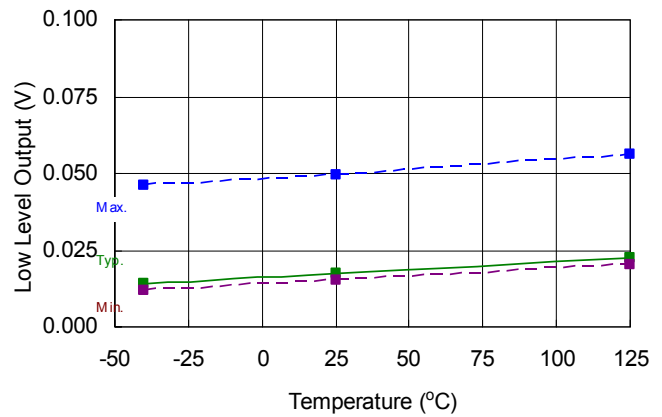
**Figure 13: V<sub>BSUV+</sub> vs. temperature**



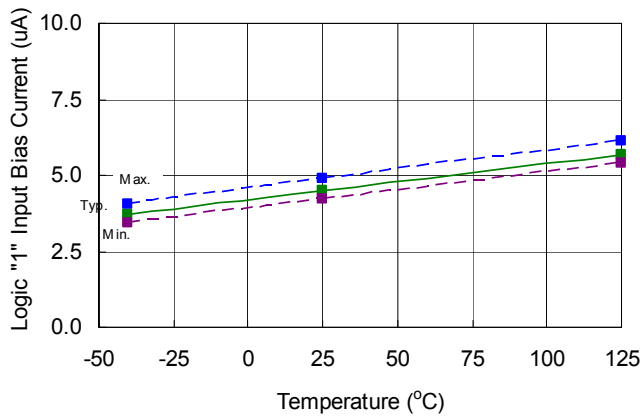
**Figure 14: V<sub>BSUV-</sub> vs. temperature**



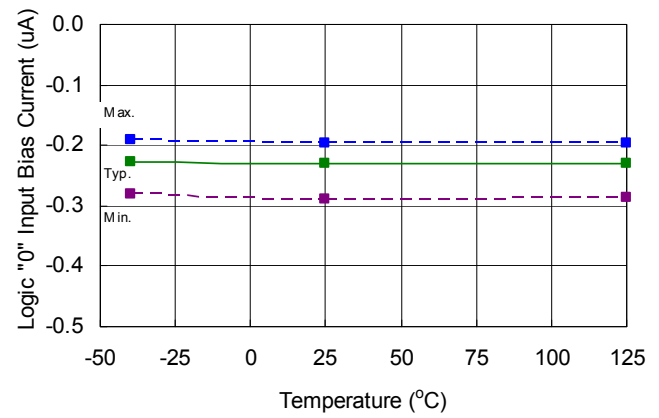
**Figure 15:  $V_{OH}$  ( $I_O = 2mA$ ) vs. temperature**



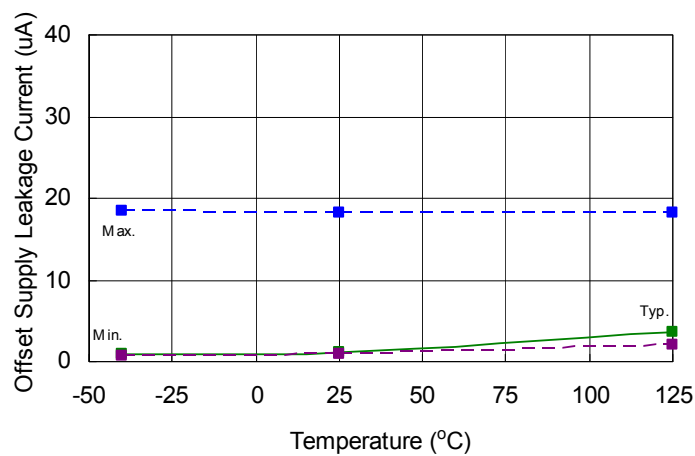
**Figure 16:  $V_{OL}$  ( $I_O = 2mA$ ) vs. temperature**



**Figure 17: Logic "1" input Bias current vs. temperature**

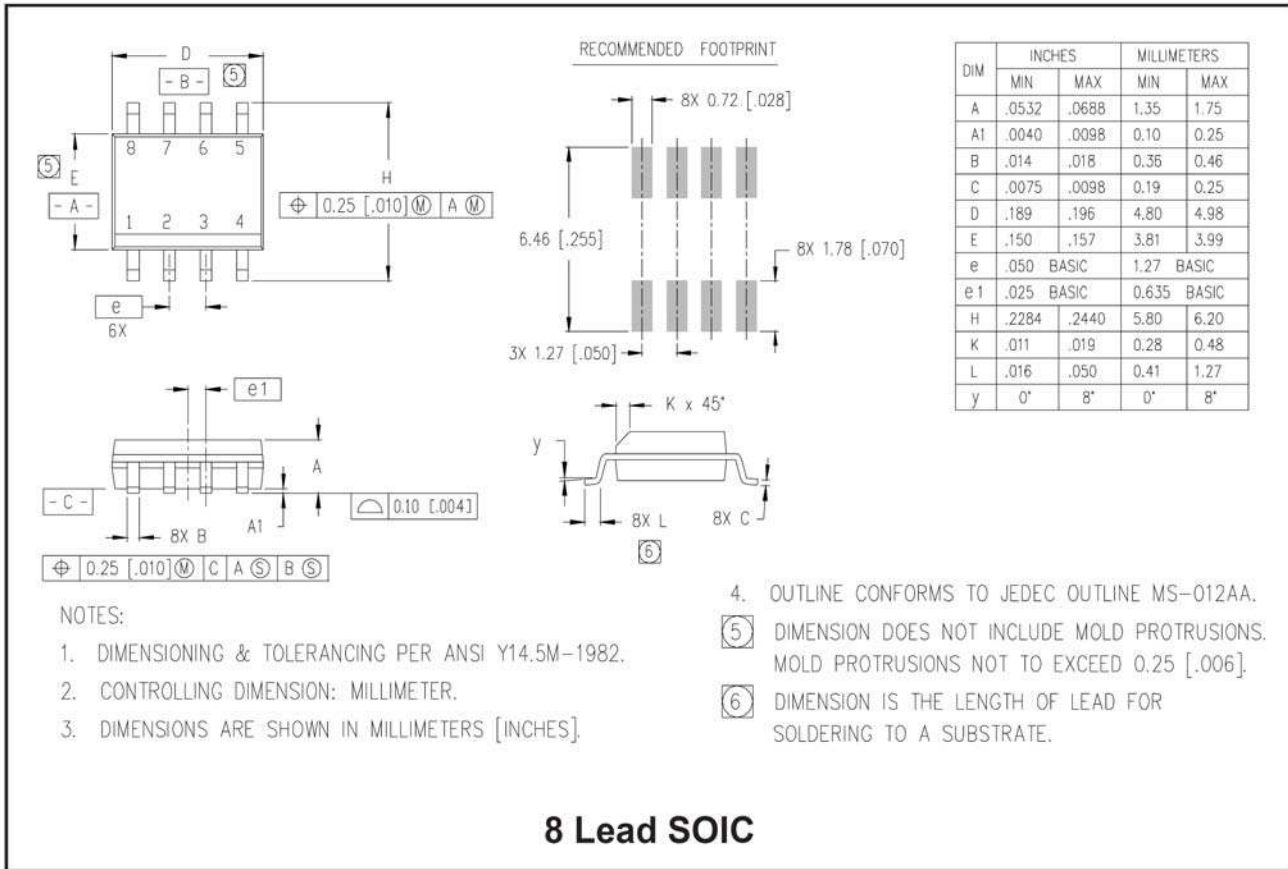


**Figure 18: Logic "0" input bias current vs. temperature**

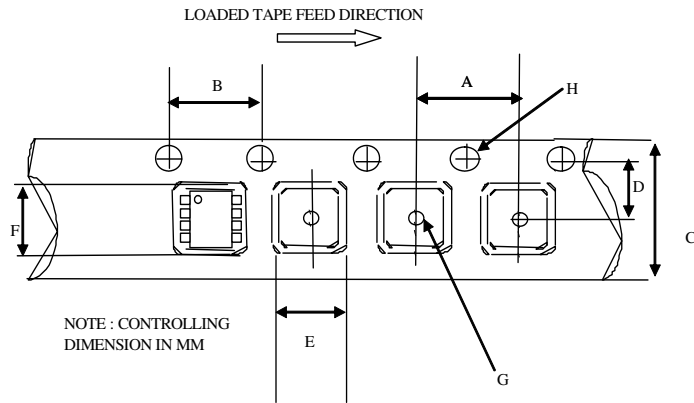


**Figure 19: Offset leakage current vs. temperature**

**Package Details**

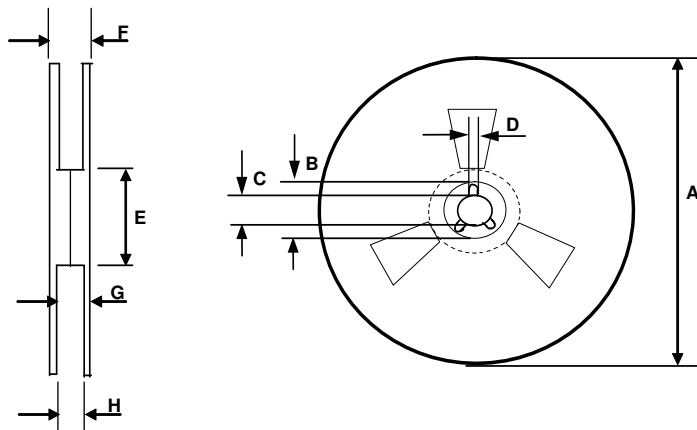


**Tape and Reel Details**



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

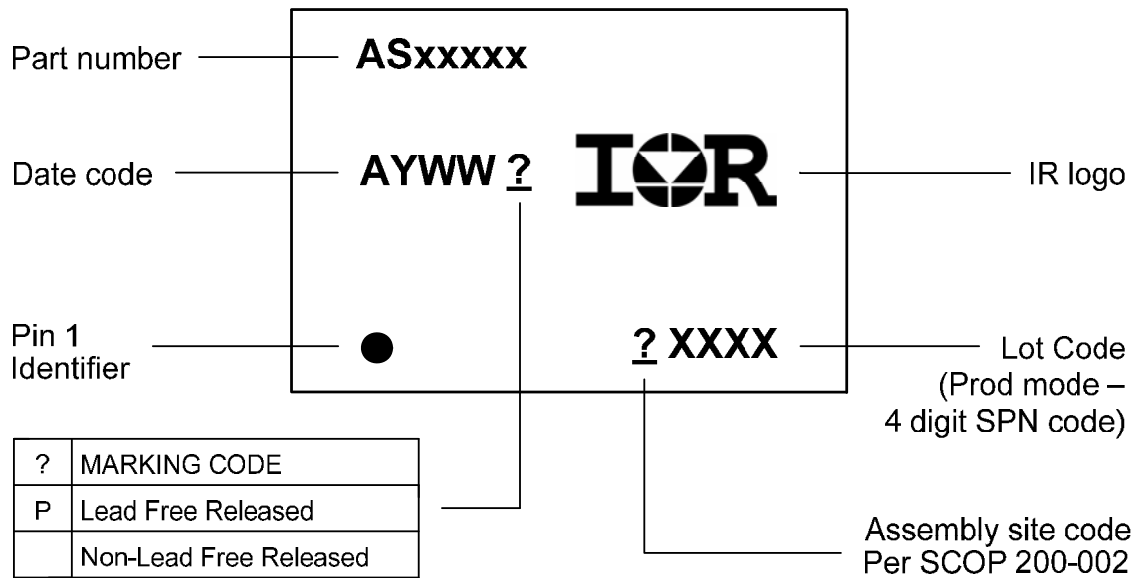


REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566



**Part Marking Information**



**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2301	SOIC8	Tube/Bulk	95	AUIRS2301S
		Tape and Reel	2500	AUIRS2301STR

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Tel: (310) 252-7105

**Revision History**

<b>Date</b>	<b>Comment</b>
11/18/08	New template, standard pack quantity corrected
12/1/08	Removed Typical Applications section from the first page Changed I <sub>O+</sub> & I <sub>O-</sub> text from typ to min, min values were reported Updated all parameters to reflect the previously released Gen2 part, modifications can be made at a later date if need be Imported correct I/O diagrams
12/9/08	Added Pin# in lead assignment table and changed the order
2/6/09	Changed ESD/LU ratings to TBD pending data
3/3/09	Removed PDIP
3/4/09	Removed "Parameter Temp Trend" section (updated page number references as well) Modified page header to read "2301" in place of "2103" Changed IQCC from 50/120/190uA to 60/150/240uA Changed IQBS from 20/60/100uA to 60/150/240uA
6/2/09	Feature comparison removed on p3 Qual table updated
6/9/09	F front page: - HIGH AND LOW SIDE DRIVER in place of HALF BRIDGE DRIVER (no cross conduction prevention logic, no dead time). - "Logic and power ground ± 5V offset" sentence removed (only COM exists as ground pin). Page3: "designed for minimum driver cross-conduction" sentence erased. Page 11: added this page with section "Tolerability to Negative VS Transients" (APBU review)
7/2/09	Updated IQCC/IQBS UL to 260uA from 240uA
7/9/09	Changed the year to 2009 in footer Removed "( )" in the part number in the description and file name Removed rows for PDIP in the Absolute Maximum Ratings Removed min spec on I <sub>O+</sub> /I <sub>O-</sub> since we don't test this parameter on ATE Deleted "SOIC8" from qual table
7/15/09	T <sub>A</sub> max temp changed from 150 to 125
7/28/09	Remove preliminary sign (DR3 approved)
7/30/09	Application section added in front page
9/8/09	ESD class modified MM M2 (was M3 based on the incorrect ESD summary)
9/14/09	Added ESD passing voltages
1/13/11	Added parameter temperature trends, updated test condition to tri-temp and important notice
1/14/11	Revised I <sub>O</sub> +/- to be typical value on front page