High-Speed CMOS 10-Bit Bus Exchange Switches

QS3383
QS32383

3

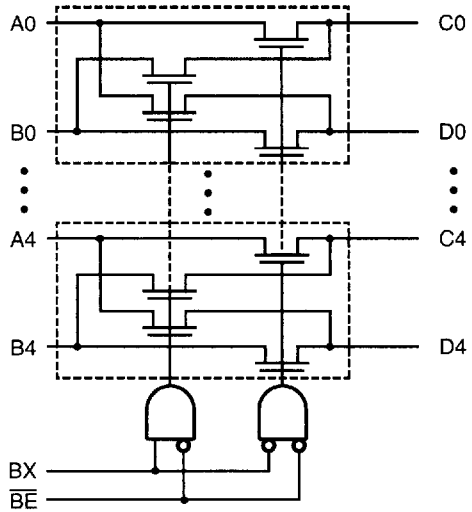
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Direct bus connection when switches on
- Zero propagation delay (QS3383)
- Low power CMOS proprietary technology
- QS32383 is 25Ω version for low noise
- Bus exchange allows nibble swap
- Zero ground bounce
- Available in 24-pin DIP, SOIC (SO), QSOP, and HQSOP

DESCRIPTION

The QS3383 and QS32383 each provide two sets of five high-speed CMOS TTL-compatible bus switches. The low ON resistance of the QS3383 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The QS32383 adds an internal 25Ω resistor to reduce reflection noise in high-speed applications. The Bus Enable ($\overline{BE}$) signal turns the switches on. The Bus Exchange (BX) signal provides nibble swap of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a 5-wide 2-to-1 multiplexer and to create low delay barrel shifters, etc.

FUNCTIONAL BLOCK DIAGRAM

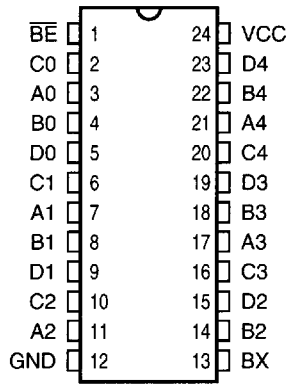


PIN DESCRIPTION

Name	I/O	Function
A4-A0, B4-B0	I/O	Buses A, B
C4-C0, D4-D0	I/O	Buses C, D
$\overline{BE}$	I	Bus Switch Enable
BX	I	Bus Exchange

PIN CONFIGURATION (All Pins Top View)

PDIP, SOIC (SO), QSOP, HQSOP



FUNCTION TABLE

$\overline{BE}$	BX	A4-A0	B4-B0	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C4-C0	D4-D0	Connect
L	H	D4-D0	C4-C0	Exchange

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Switch Voltage V_S	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

	SOIC		QSOP		PDIP		HQSOP		
Pins	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit
Control Pins	3	4	3	4	4	5	6	7	pF
QuickSwitch Channels	7	8	7	8	8	9	10	11	pF

Note: Capacitance is characterized but not tested.

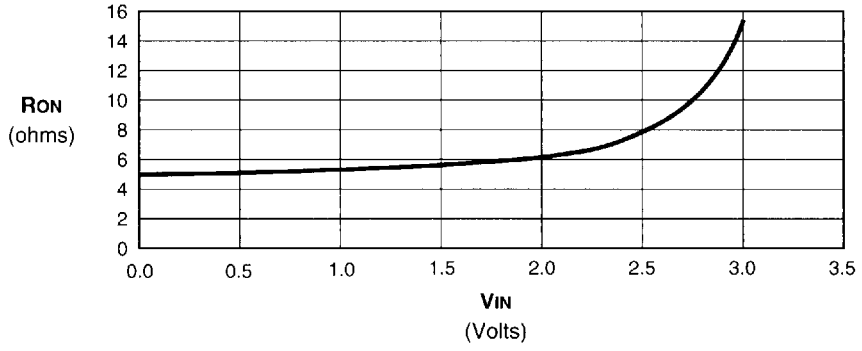
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military: T_A = −55°C to 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions		Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
$\lvert I_{IN} \rvert$	Input Leakage Current(2)	0 ≤ V_{IN} ≤ Vcc		—	—	1	µA
$\lvert I_{OZ} \rvert$	Off-State Current (Hi-Z)	0 ≤ AB, CD ≤ Vcc		—	.001	1	µA
I_{OS}	Short Circuit Current(3)	AB(CD) = 0V, CD(AB) = Vcc		—	300	—	mA
R_{ON}	Switch ON Resistance(4,5)	Vcc = Min.,	3383 (Com)	—	5	7	Ω
		V_{IN} = 0.0V	3383 (Mil)	—	10	12	
		I_{ON} = 30 mA	32383 (Com)	20	28	40	
			32383 (Mil)	—	35	45	
R_{ON}	Switch ON Resistance(4,5)	Vcc = Min.,	3383 (Com)	—	10	15	Ω
		V_{IN} = 2.4V	3383 (Mil)	—	15	20	
		I_{ON} = 15 mA	32383 (Com)	20	35	48	
			32383 (Mil)	—	40	55	

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. During input/output leakage, testing all pins are at a HIGH or LOW state, and the $\overline{BE}$ control is HIGH.
3. Not more than one output should be used to test this high power condition and the duration is ≤1 second.
4. Measured by voltage drop between A,B and C,D pins at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A or B, C or D) pins.
5. Max. value R_{ON} guaranteed but not tested.

Typical ON Resistance vs V_{IN} at 4.75 Vcc (QS3383 Only)



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	1.5	mA
ΔI_{CC}	Power Supply Current per Input HIGH[2]	V_{CC} = Max., V_{IN} = 3.4V, f = 0 per Control Input	2.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[3]	V_{CC} = Max., A and B Pins Open, Control Inputs Toggling @ 50% Duty Cycle	0.25	mA/ MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A, B, C, D pins do not contribute to Icc.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military: T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

			QS3383			QS32383			
Symbol	Description[1]		Min	Typ	Max	Min	Typ	Max	Unit
t_{PLH}	Data Propagation Delay[2,4]	COM	—	—	0.25[3]	—	—	1.25[4]	ns
t_{PHL}	AiBi to CiDi, CiDi to AiBi	MIL	—	—	0.25[3]	—	—	1.50[4]	
t_{PZL}	Switch Turn-on Delay[1]	COM	1.5	—	6.5	1.5	—	7.5	ns
t_{PZH}	$\overline{BE}$ to Ai, Bi, Ci, Di	MIL	1.5	—	7.5	1.5	—	8.5	
t_{PLZ}	Switch Turn-off Delay[1,2]	COM	1.5	—	5.5	—	—	—	ns
t_{PHZ}	$\overline{BE}$ to Ai, Bi, Ci, Di	MIL	1.5	—	6.5	—	—	—	
t_{BX}	Switch Multiplex Delay	COM	1.5	—	6.5	1.5	—	7.5	ns
	BX to Ai, Bi, Ci, Di[1]	MIL	1.5	—	7.5	1.5	—	8.5	
$\lvert Q_{CI} \rvert$	Charge Injection[5,7]	COM	—	1.5	—	—	1.5	—	pC
		MIL	—	1.5	—	—	1.5	—	
$\lvert Q_{DCI} \rvert$	Differential Charge	COM	—	<0.5	—	—	<0.5	—	pC
	Injection[6,7]	MIL	—	<0.5	—	—	<0.5	—	

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The time constant for the switch alone is of the order of 0.25 ns for 50 pF.
4. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this delay is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, V_{IN} at I = 0.0V.
6. Measured at switch turn off through bus multiplex, A to C ≥ A to D, B connected to C, load = 50 pF in parallel with 10 meg scope probe, V_{IN} at A = 0.0V. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.
7. Characterized parameter but not 100% tested.